2 – 26 GHz GaAs Distributed Self-Biased LNA

MMA042AA

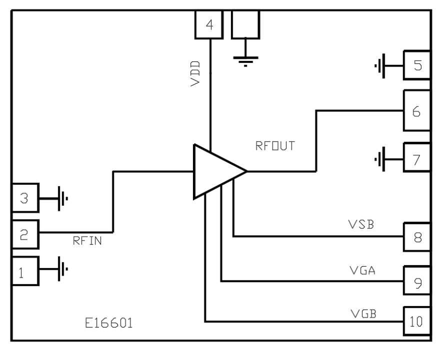
Product Overview

MMA042AA is a Gallium Arsenide (GaAs) monolithic microwave integrated circuit (MMIC) pseudomorphic high-electron mobility transistor (pHEMT) distributed amplifier die that operates between 2 GHz and 26 GHz. It is ideal for test instrumentation, defense, and space applications. The amplifier provides a 2 dB positive gain slope with a typical gain of 18 dB, 2 dB noise figure, 19 dBm of output power at 1 dB gain compression, and 29 dBm output IP3 at 10 GHz. The MMA042AA amplifier features RF I/Os that are internally matched to 50Ω, which allows for easy integration into multi-chip modules (MCMs).

Key Features

- Frequency range: 2 GHz to 26 GHz
- High gain: 18 dB with +2 dB upslope
- Low noise figure: 2 dB
- High output IP3: +29 dBm
- Maximum RF input power: +24 dBm
- Single positive supply with on–chip bias
- ESD Protection on RF and DC ports
- Die size : 2.020 mm × 1.630 mm
- Capable of 3V–5V operation, optimized for 7V

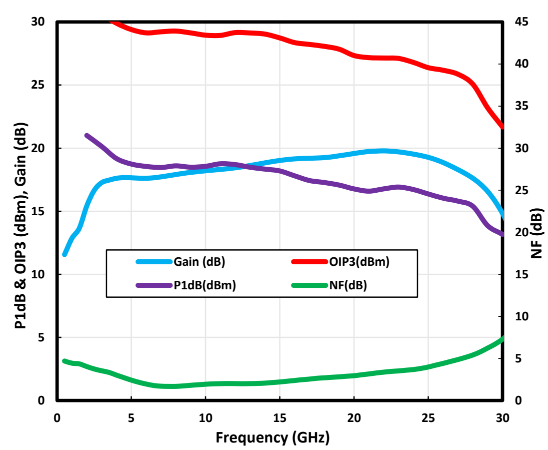
Functional Block Diagram



Applications

- Test and measurement instrumentation
- Electronic warfare (EW), electronic countermeasures (ECM), and electronic counter-countermeasures (ECCM)
- Military and space
- Telecom infrastructure
- Wideband microwave radios
- Microwave and millimeter-wave communication systems

Performance Curves



Performance Overview

Parameter	Typ.	Units
Frequency range	2 – 26	GHz
Gain	18	dB
Gain flatness	± 0.75	dB
NF	2	dB
Output IP3	+29	dBm

Export Classification: EAR99

Table of Contents

1. Electrical Specifications

1.1 Typical Electrical Performance

Table 1-1. Typical Electrical Performance at 25 °C, Vdd = 6V, Idd = 120 mA (Unless otherwise specified)

Parameter	Frequency Range	Min.	Typ.	Max.	Units
Frequency range		2		26	GHz
Gain	3 GHz – 8 GHz	16	18		dB
	8 GHz – 15 GHz	17	18.5		dB
	15 GHz – 26 GHz	18	20		dB
Gain flatness (0.1 dB/GHz upslope subtracted)	3 GHz – 8 GHz		± 0.5		dB
	15 GHz – 26 GHz		± 0.5		dB
Noise figure	3 GHz – 8 GHz		2.5	3.5	dB
	8 GHz – 15 GHz		2	2.5	dB
	15 GHz – 26 GHz		3.5	5.5	dB
P1dB	3 GHz – 8 GHz	18	20		dBm
	8 GHz – 15 GHz	18	20		dBm
	15 GHz – 26 GHz	16	18		dBm
OIP3	3 GHz – 8 GHz		30		dBm
	8 GHz – 15 GHz		30		dBm
	15 GHz – 26 GHz		28		dBm
Input return loss	3 GHz – 8 GHz		12		dB
	8 GHz – 15 GHz		12		dB
	15 GHz – 26 GHz		10		dB
Output return loss	3 GHz – 8 GHz		10		dB
	8 GHz – 15 GHz		10		dB
	15 GHz – 26 GHz		8		dB
V_{DD} (drain voltage supply)			6		V
I_{DD} (drain current)			120		mA

1.2 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the MMA042AA device at 25 °C, unless otherwise specified. Exceeding one or any of the maximum ratings potentially could cause damage or latent defects to the device.

Table 1-2. Absolute Maximum Ratings

Parameter	Rating
Drain bias voltage (VDD)	8V
Gate bias voltage (VG)	–1V to + 0.5V
RF input power (Pin)	24 dBm
Channel temperature	150 °C
VDD current (IDD)	200 mA
DC power dissipation (T = 85 °C)	1.6W
Thermal resistance	17 °C/W
Storage temperature	–65 °C to + 150 °C
Operating temperature	–55 °C to + 85 °C

ESD Sensitive Device

1.3 Typical Performance Curves

1.3.1 Typical Performance vs. Temperature

The following graphs shows the typical performance curves of the MMA042AA device at specific bias conditions.

Figure 1-1. Gain vs. Temperature at 3.5V/60 mA

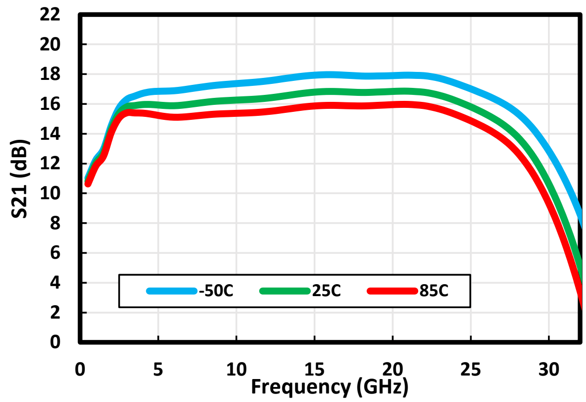


Figure 1-2. Gain vs. Temperature at 5V/100 mA

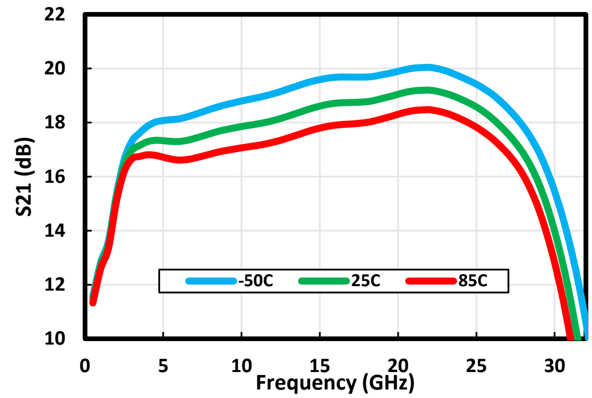


Figure 1-3. Gain vs. Temperature at 6V/120 mA

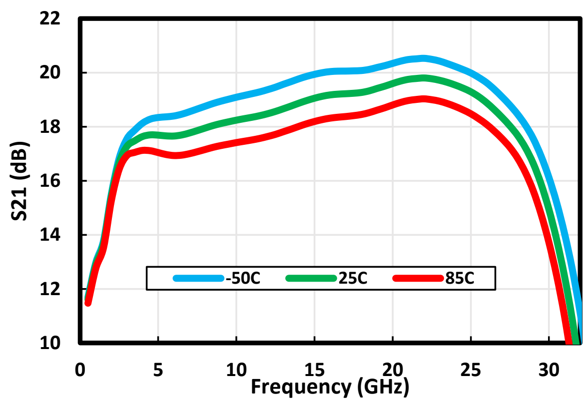


Figure 1-4. Gain vs. Temperature at 7V/140 mA

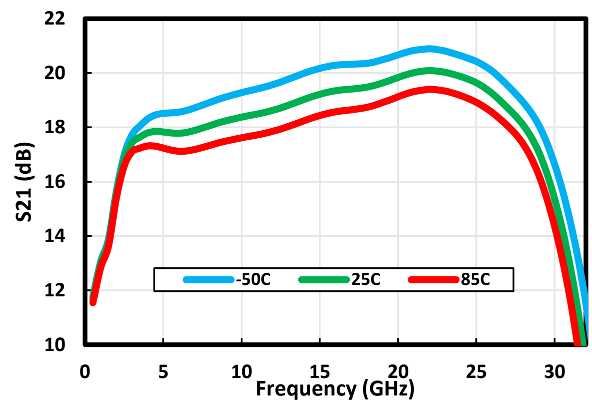


Figure 1-5. S11 vs. Temperature at 3.5V/60 mA

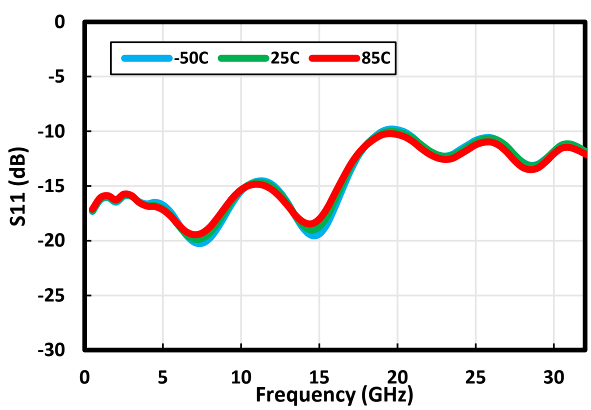


Figure 1-6. S11 vs. Temperature at 5V/100 mA

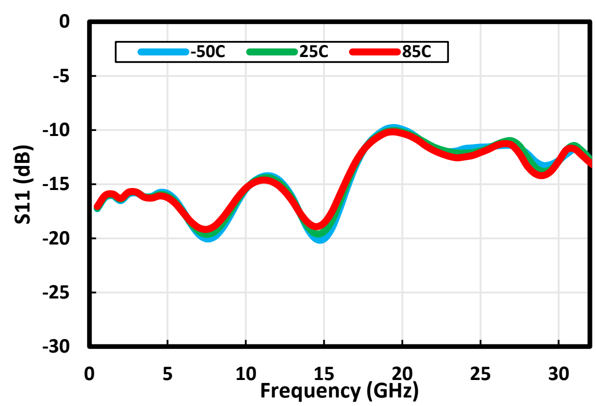


Figure 1-7. S11 vs. Temperature at 6V/120 mA

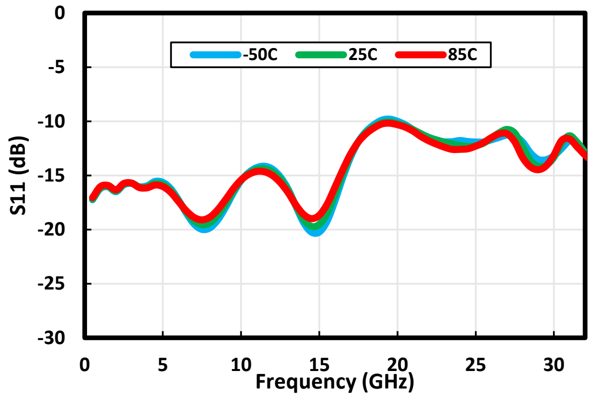


Figure 1-8. S11 vs. Temperature at 7V/140 mA

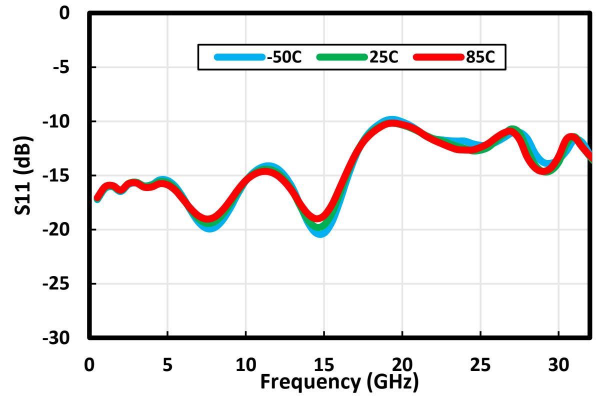


Figure 1-9. S22 vs. Temperature at 3.5V/60 mA

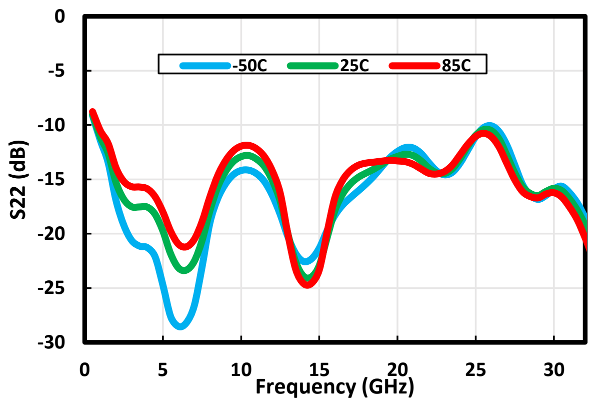


Figure 1-10. S22 vs. Temperature at 5V/100 mA

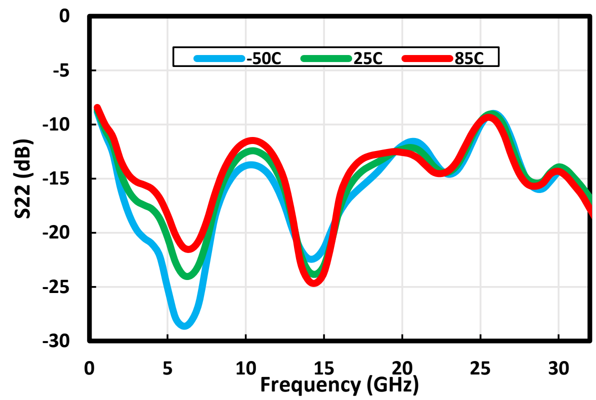


Figure 1-11. S22 vs. Temperature at 6V/120 mA

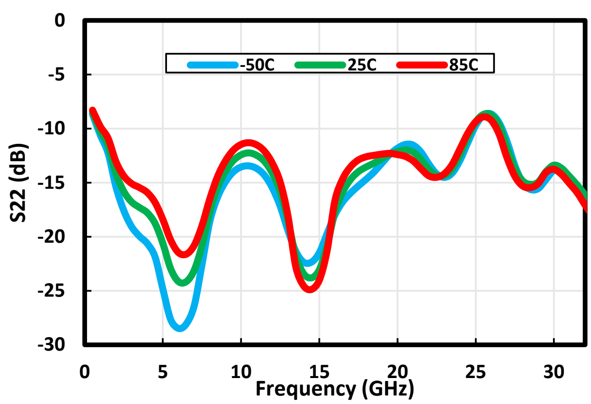


Figure 1-12. S22 vs. Temperature at 7V/140 mA

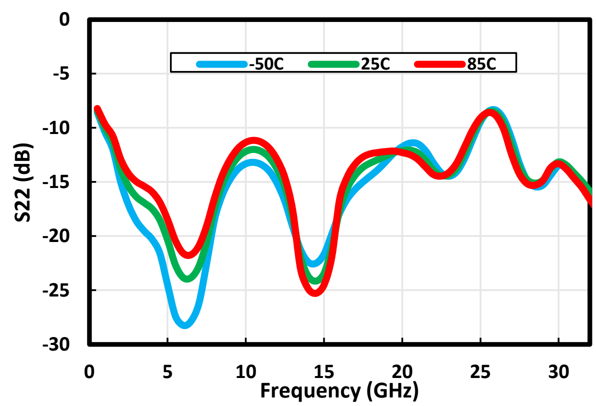


Figure 1-13. S12 vs. Temperature at 3.5V/60 mA

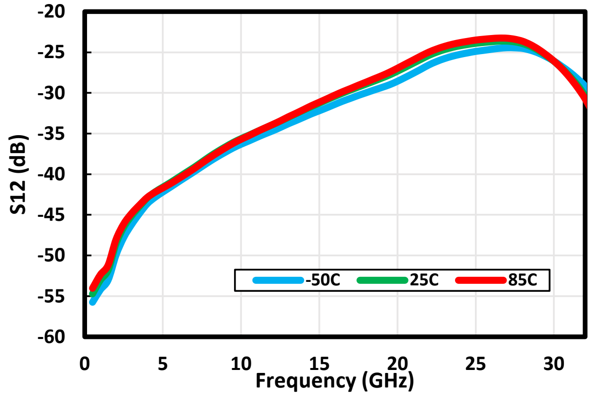


Figure 1-14. S12 vs. Temperature at 5V/100 mA

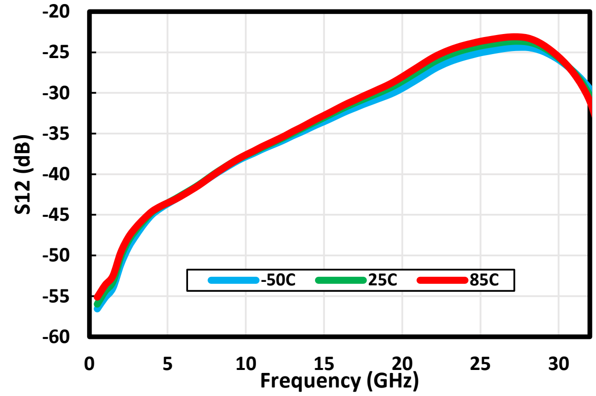


Figure 1-15. S12 vs. Temperature at 6V/120 mA

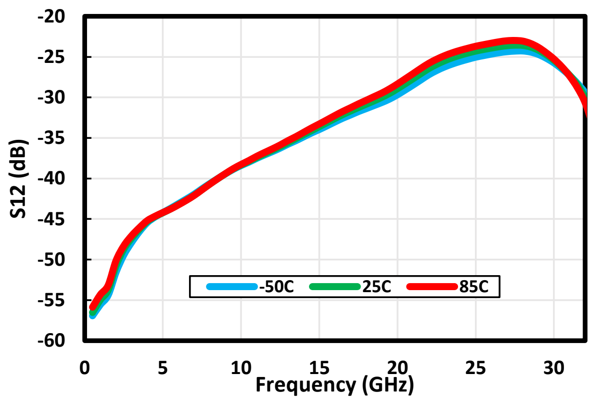


Figure 1-16. S12 vs. Temperature at 7V/140 mA

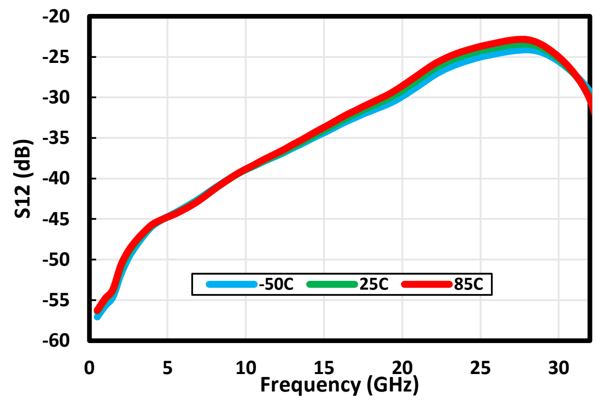


Figure 1-17. NF vs. Temperature at 3.5V/60 mA

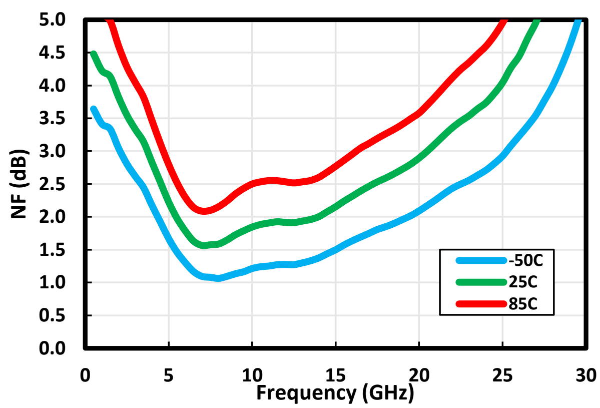


Figure 1-18. NF vs. Temperature at 5V/100 mA

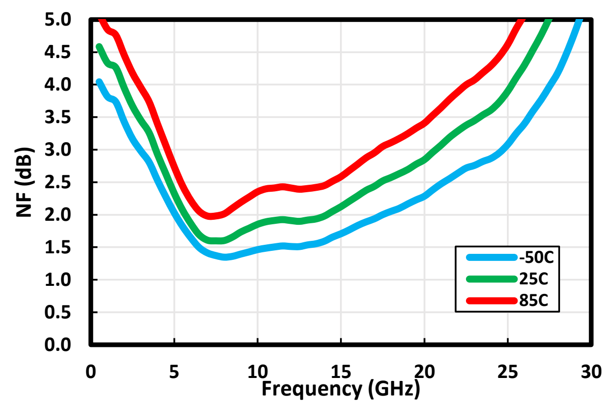


Figure 1-19. NF vs. Temperature at 6V/120 mA

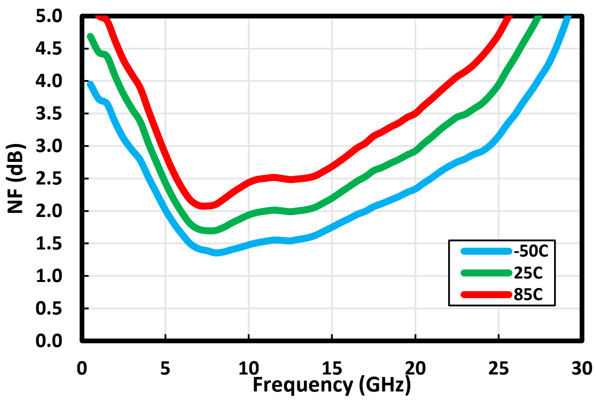


Figure 1-20. NF vs. Temperature at 7V/140 mA

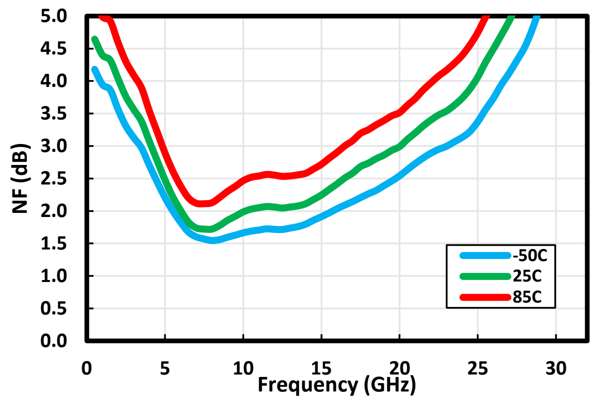


Figure 1-21. P1 dB vs. Temperature at 3.5V/60 mA

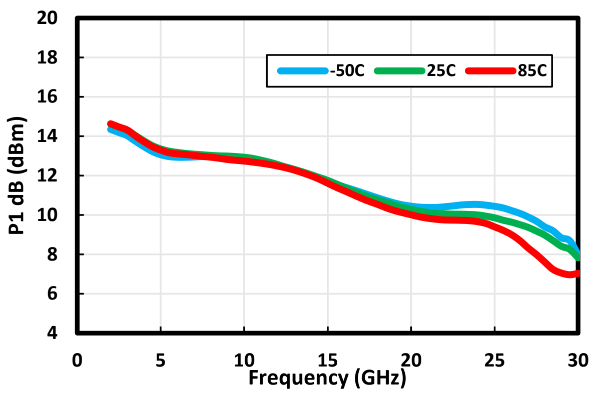


Figure 1-22. P1 dB vs. Temperature at 5V/100 mA

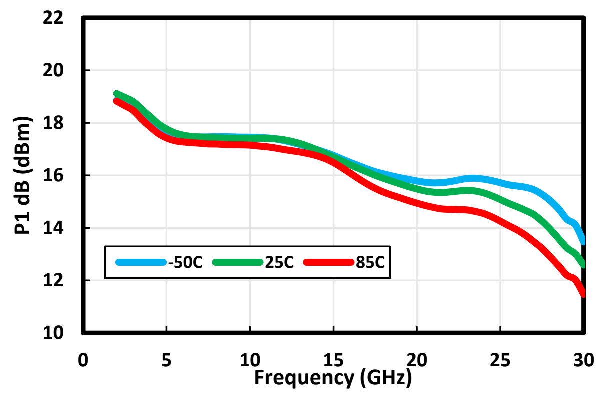


Figure 1-23. P1 dB vs. Temperature at 6V/120 mA

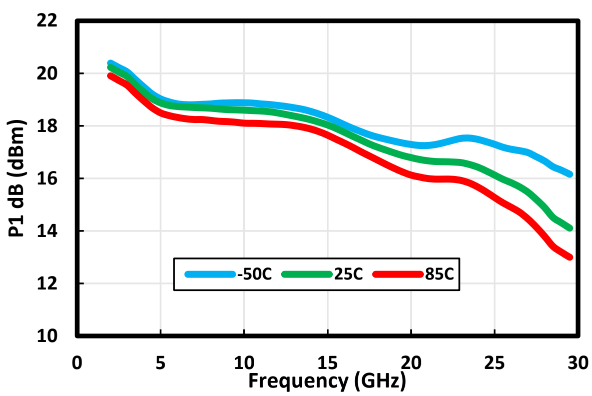


Figure 1-24. P1 dB vs. Temperature at 7V/140 mA

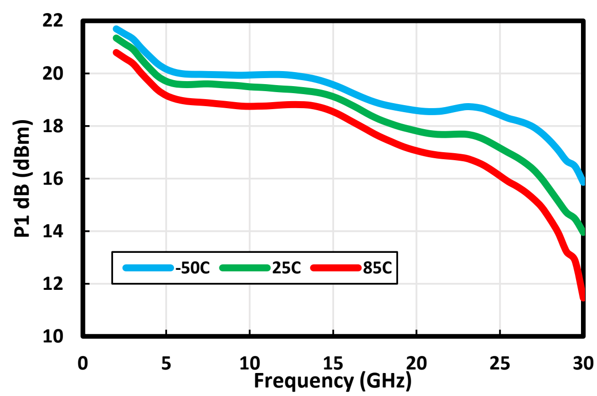


Figure 1-25. P3 dB vs. Temperature at 3.5V/60 mA

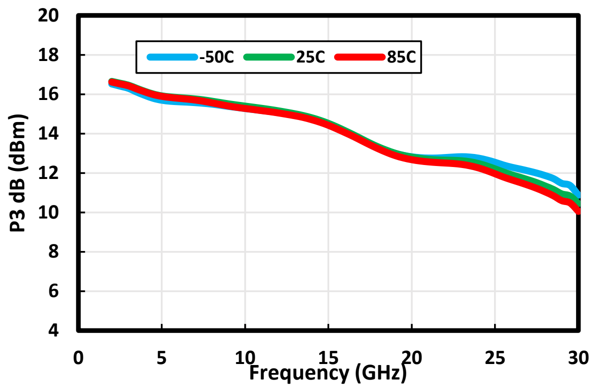


Figure 1-26. P3 dB vs. Temperature at 5V/100 mA

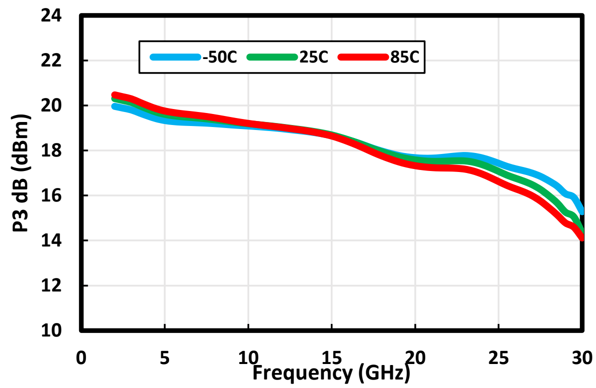


Figure 1-27. P3 dB vs. Temperature at 6V/120 mA

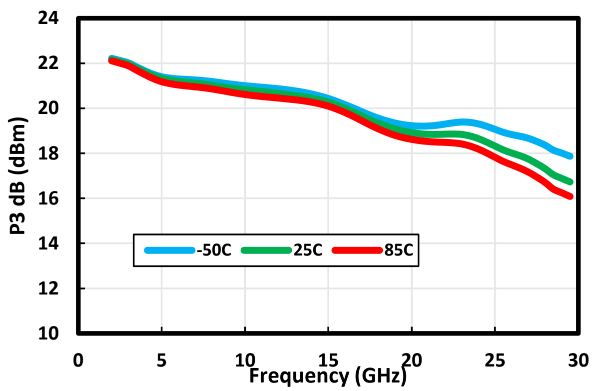


Figure 1-28. P3 dB vs. Temperature at 7V/140 mA

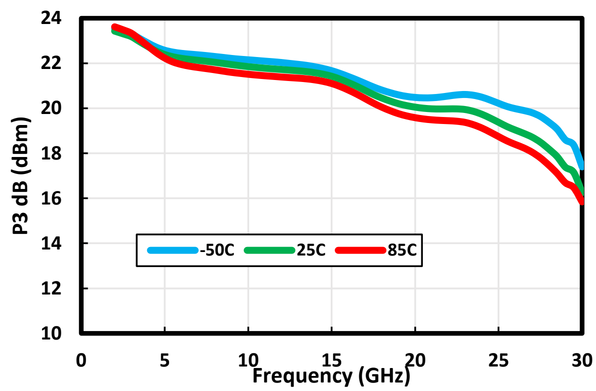


Figure 1-29. OIP3 vs. Temperature at 3.5V/60 mA

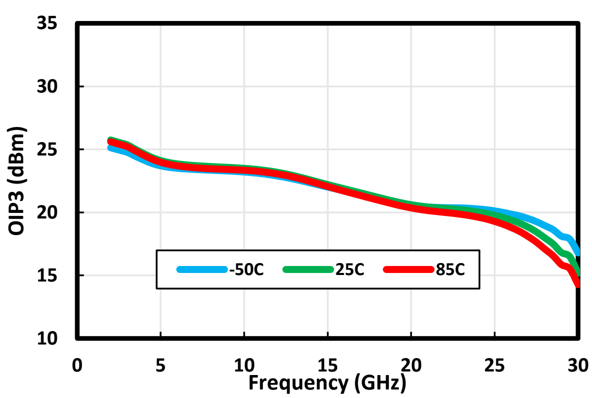


Figure 1-30. OIP3 vs. Temperature at 5V/100 mA

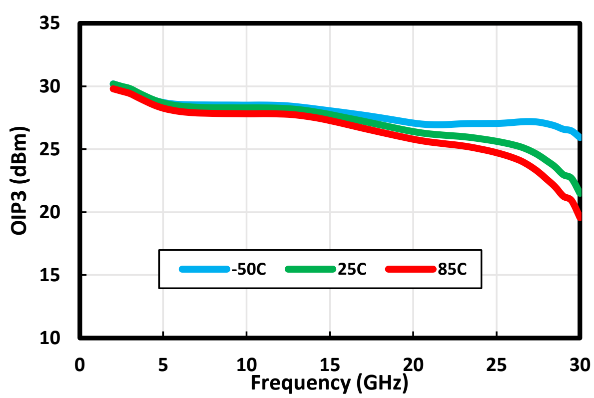


Figure 1-31. OIP3 vs. Temperature at 6V/120 mA

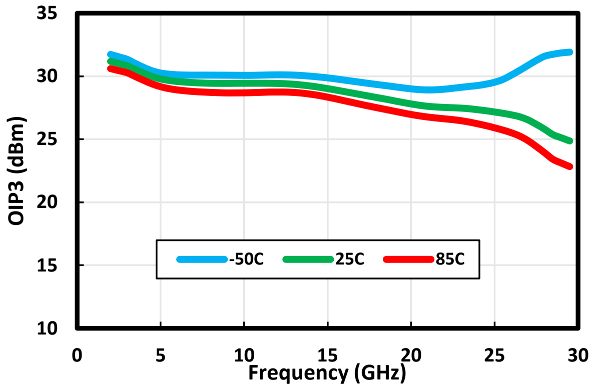


Figure 1-32. OIP3 vs. Temperature at 7V/140 mA

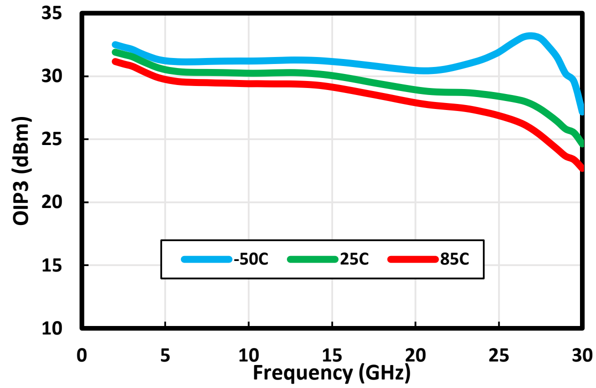


Figure 1-33. OIP2 vs. Temperature at 3.5V/60 mA

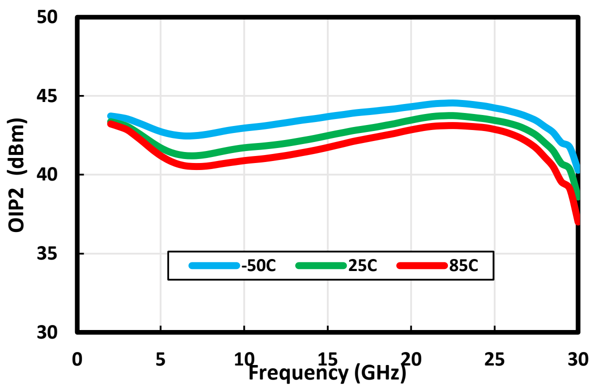


Figure 1-34. OIP2 vs. Temperature at 5V/100 mA

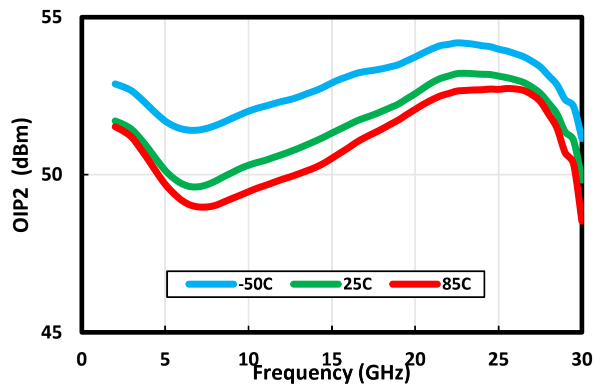


Figure 1-35. OIP2 vs. Temperature at 6V/120 mA

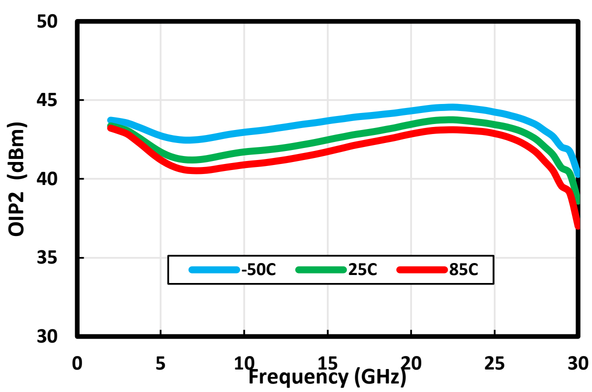


Figure 1-36. OIP2 vs. Temperature at 7V/140 mA

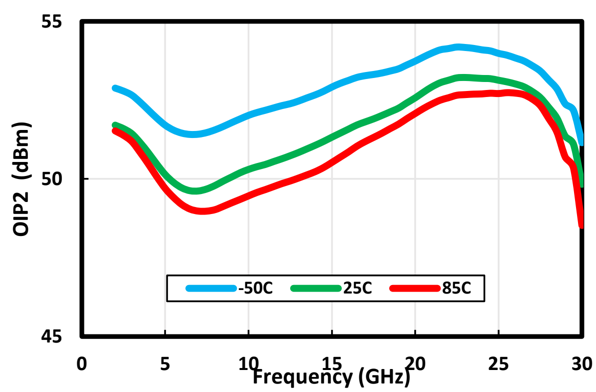


Figure 1-37. OIM3 vs. Temperature at 3.5V/60 mA

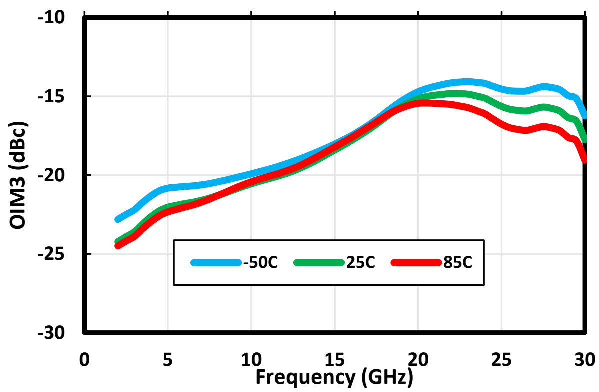


Figure 1-38. OIM3 vs. Temperature at 5V/100 mA

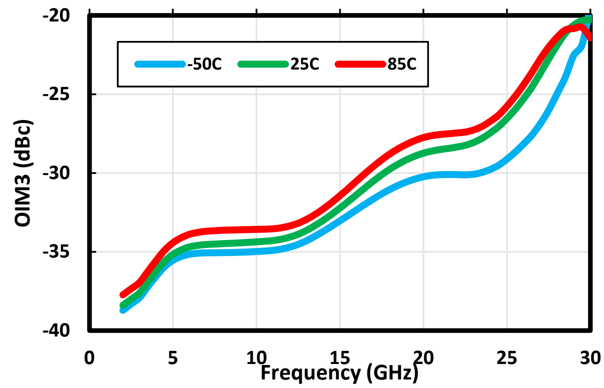


Figure 1-39. OIM3 vs. Temperature at 6V/120 mA

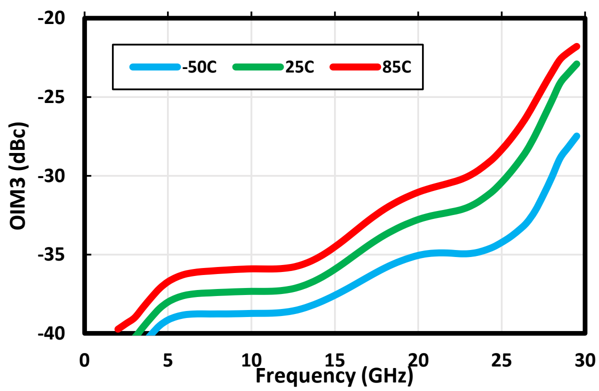
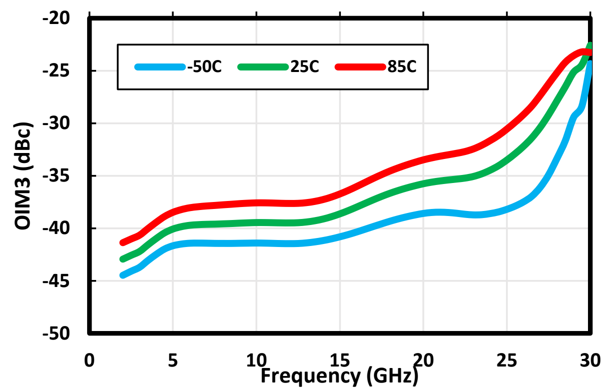


Figure 1-40. OIM3 vs. Temperature at 7V/140 mA



1.3.2 Typical Performance vs. Bias

The following graphs show the typical performance curves of the MMA042AA device at specific bias conditions.

Figure 1-41. Gain vs. V_{DD} at 100 mA

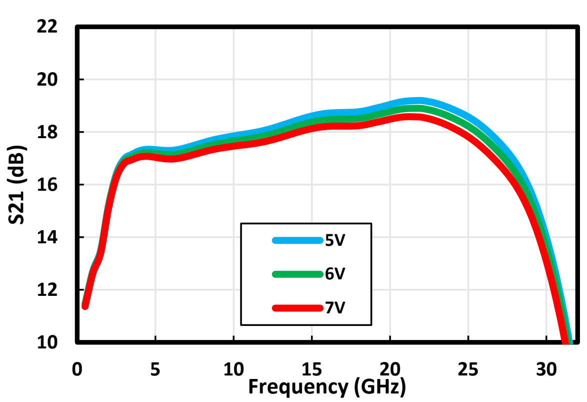


Figure 1-42. Gain vs. V_{DD} at 120 mA

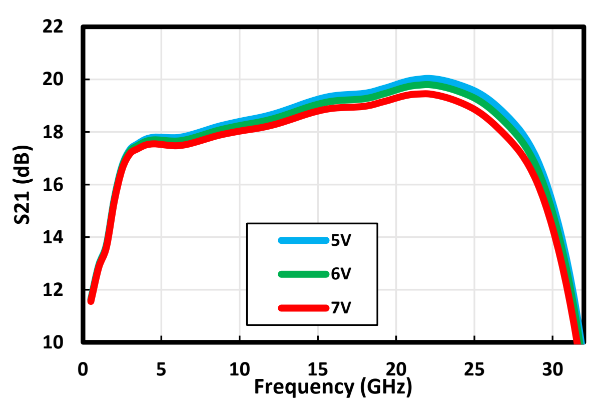


Figure 1-43. Gain vs. V_{DD} at 130 mA

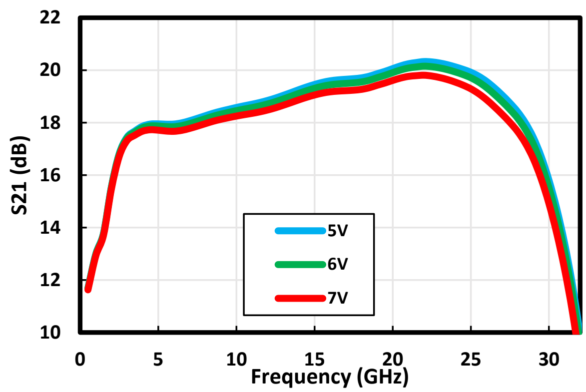


Figure 1-44. NF vs. V_{DD} at 100 mA

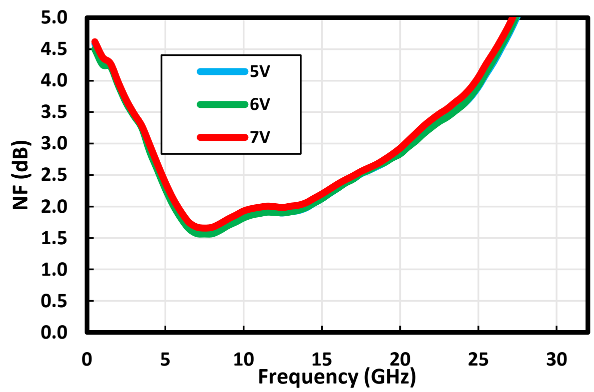


Figure 1-45. NF vs. V_{DD} at 120 mA

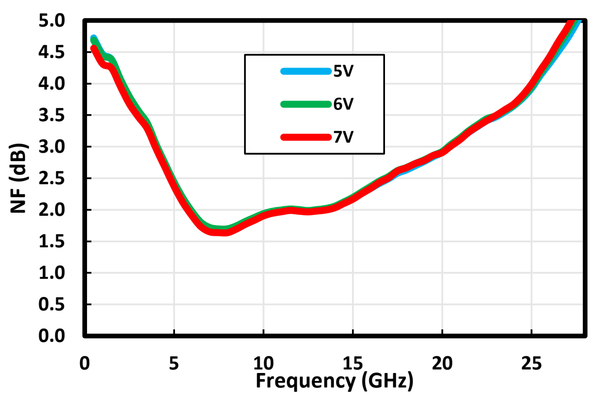


Figure 1-46. NF vs. V_{DD} at 130 mA

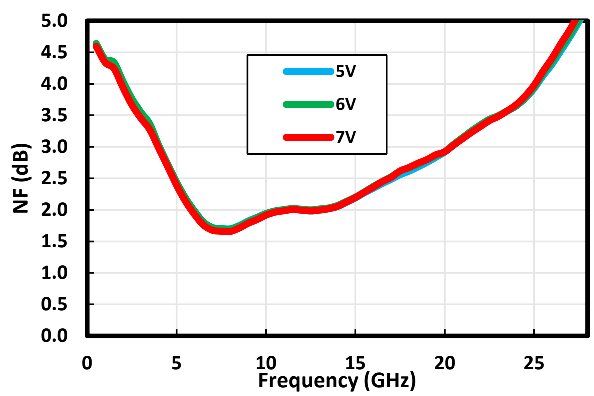


Figure 1-47. S11 vs. V_{DD} at 100 mA

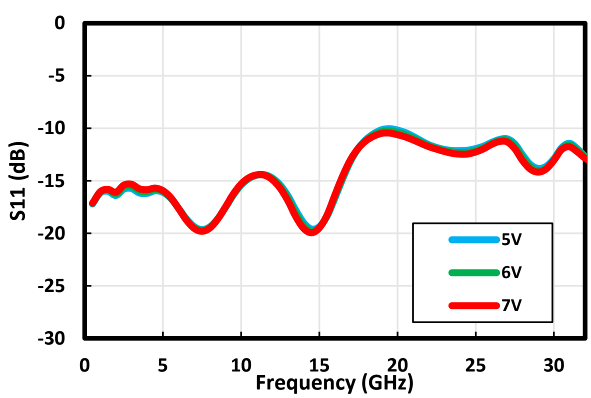


Figure 1-48. S11 vs. V_{DD} at 120 mA

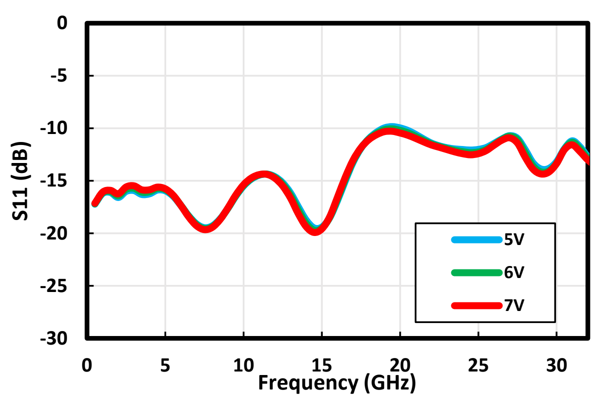


Figure 1-49. S11 vs. V_{DD} at 130 mA

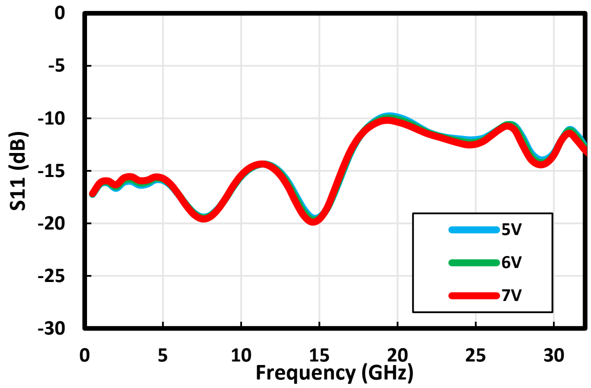


Figure 1-50. S12 vs. V_{DD} at 100 mA

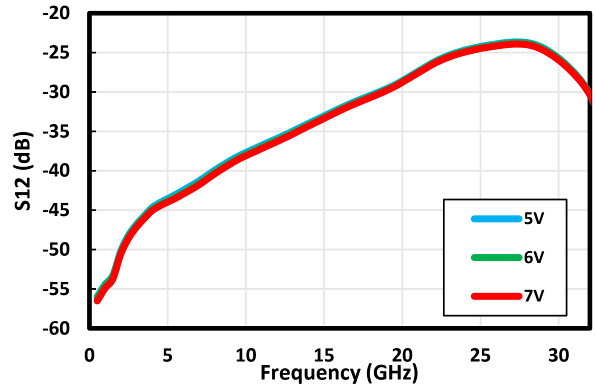


Figure 1-51. S12 vs. V_{DD} at 120 mA

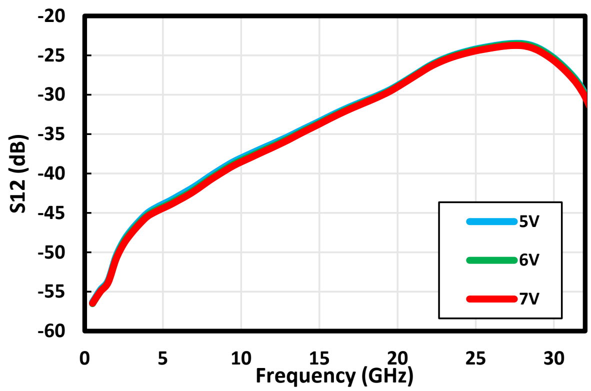


Figure 1-52. S12 vs. V_{DD} at 130 mA

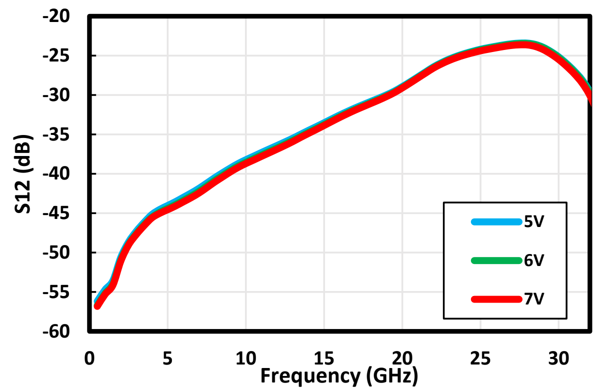


Figure 1-53. S22 vs. V_{DD} at 100 mA

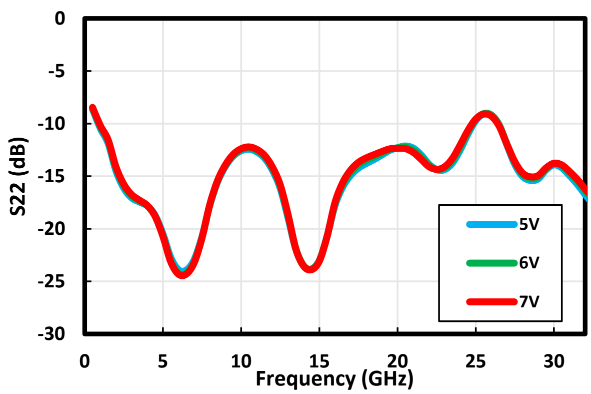


Figure 1-54. S22 vs. V_{DD} at 120 mA

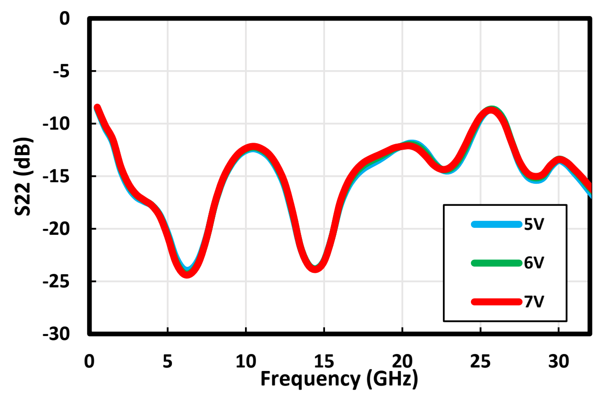


Figure 1-55. S22 vs. V_{DD} at 130 mA

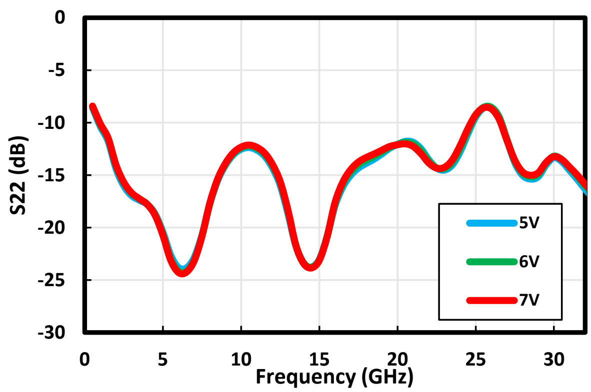


Figure 1-56. P1 dB vs. V/I

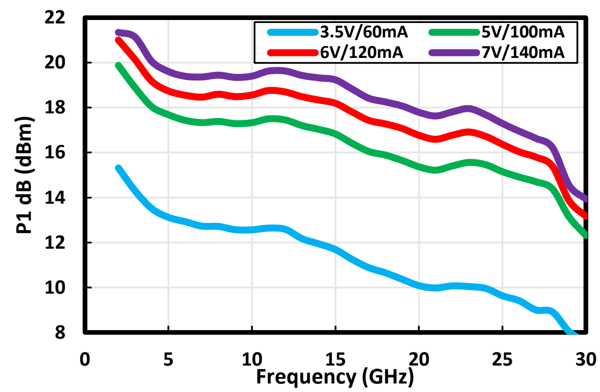


Figure 1-57. P1 dB vs. V_{DD} at 100 mA

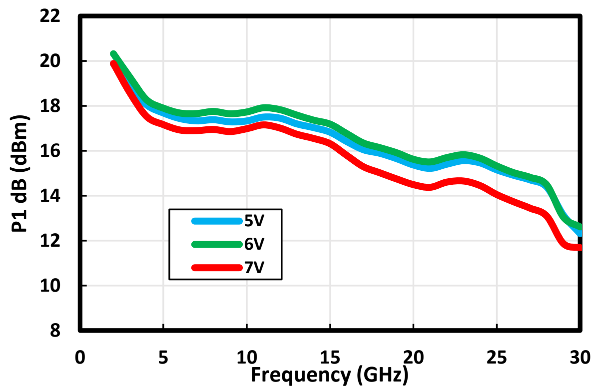


Figure 1-58. P1 dB vs. V_{DD} at 120 mA

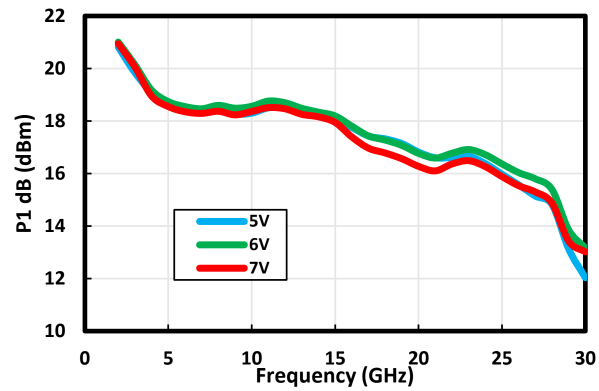


Figure 1-59. P1 dB vs. V_{DD} at 140 mA

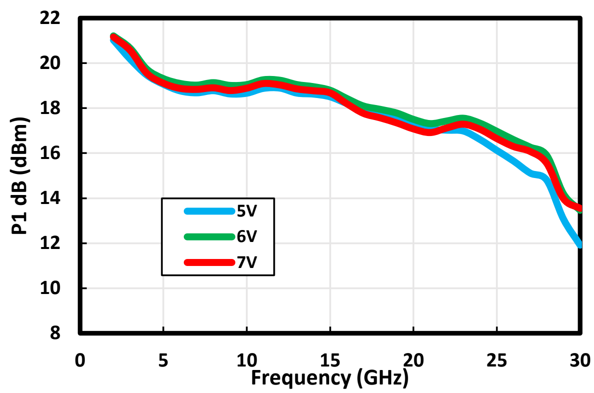


Figure 1-60. P3 dB vs. V/I

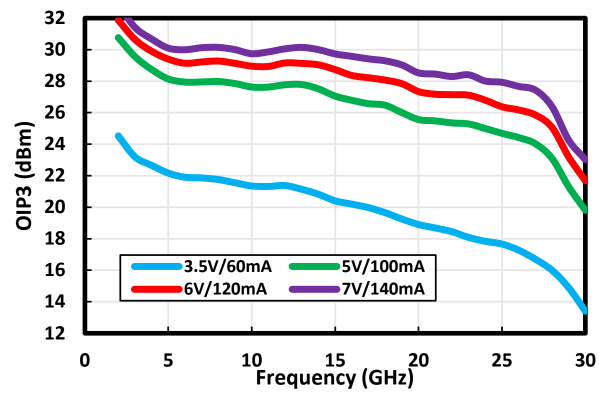


Figure 1-61. P3 dB vs. V_{DD} at 100 mA

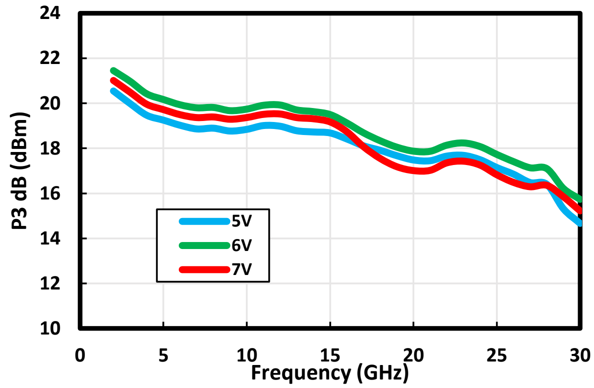


Figure 1-62. P3 dB vs. V_{DD} at 120 mA

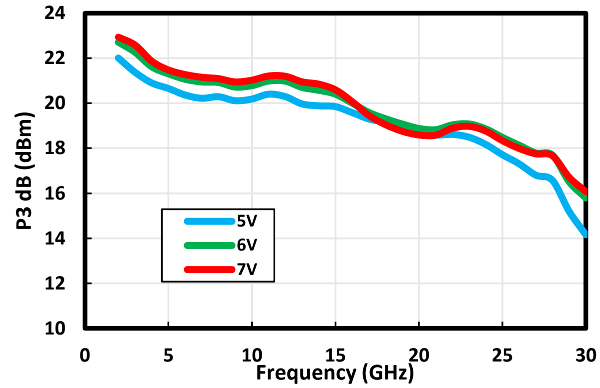


Figure 1-63. OIP2 vs. V/I

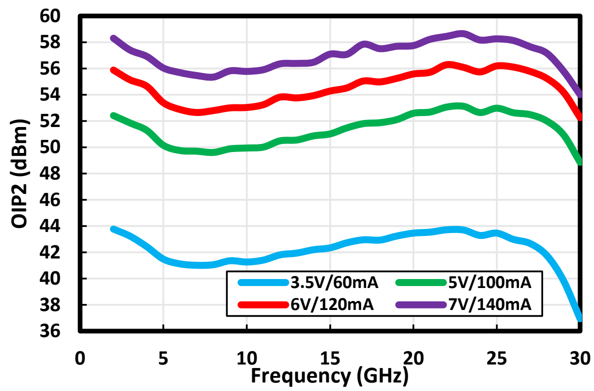


Figure 1-64. OIP2 vs. V_{DD} at 100 mA

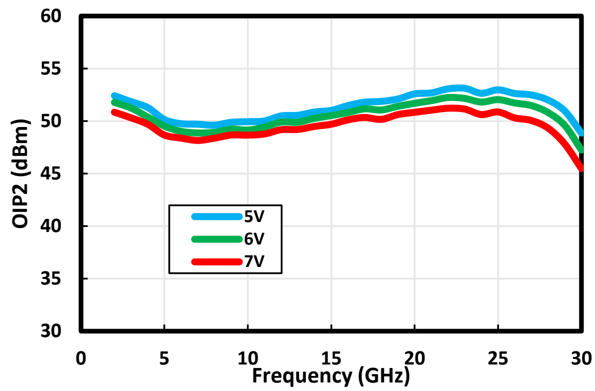


Figure 1-65. OIP2 vs. V_{DD} at 120 mA

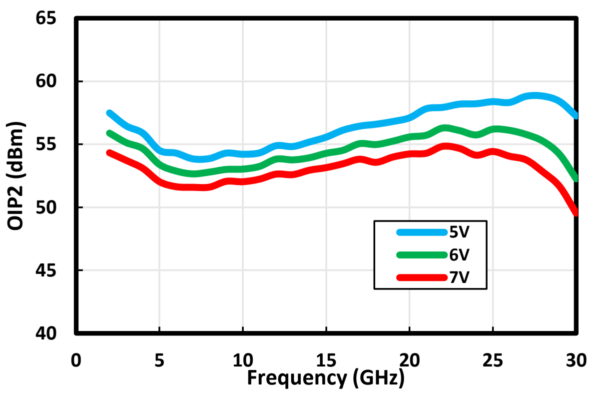


Figure 1-66. OIP2 vs. V_{DD} at 140 mA

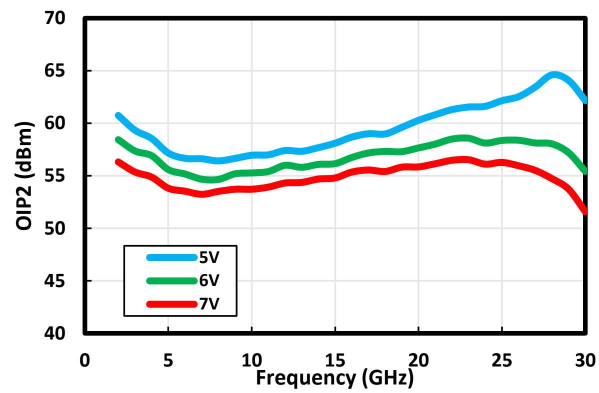


Figure 1-67. OIP3 vs. V/I

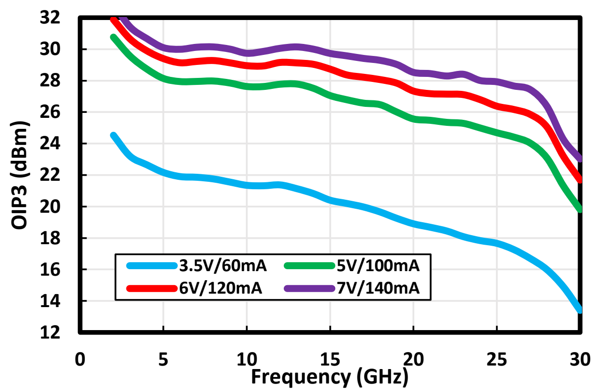


Figure 1-68. OIP3 vs. V_{DD} at 100 mA

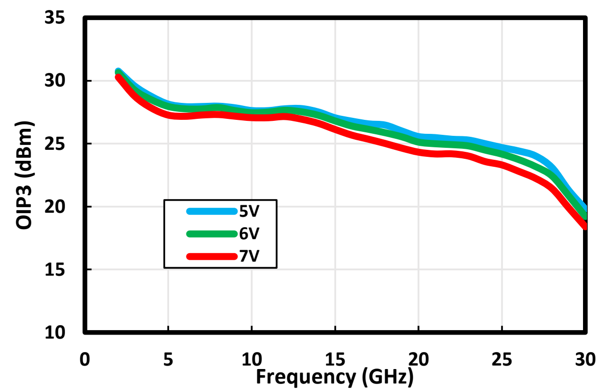


Figure 1-69. OIP3 vs. V_{DD} at 120 mA

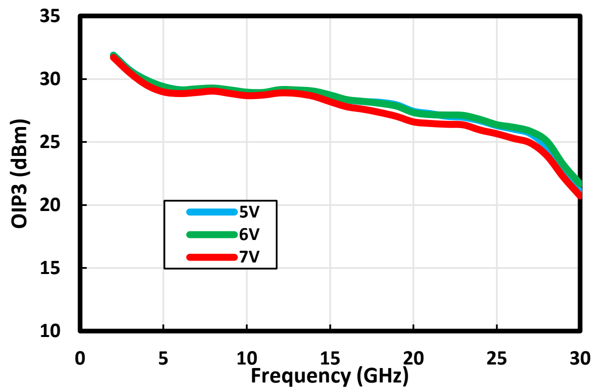


Figure 1-70. OIP3 vs. V_{DD} at 140 mA

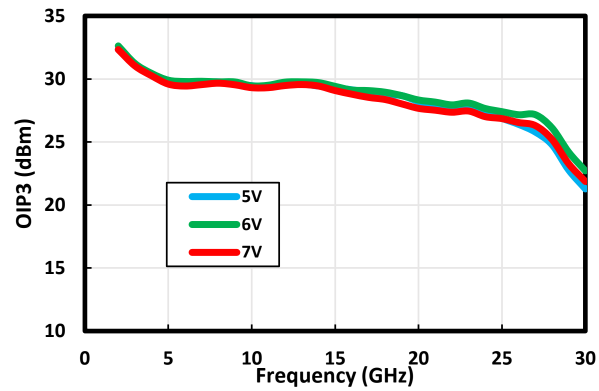


Figure 1-71. OIM3 vs. V/I

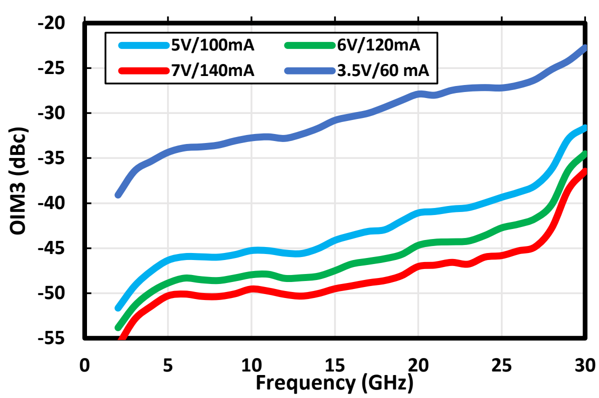


Figure 1-72. OIM3 vs. V_{DD} at 100 mA

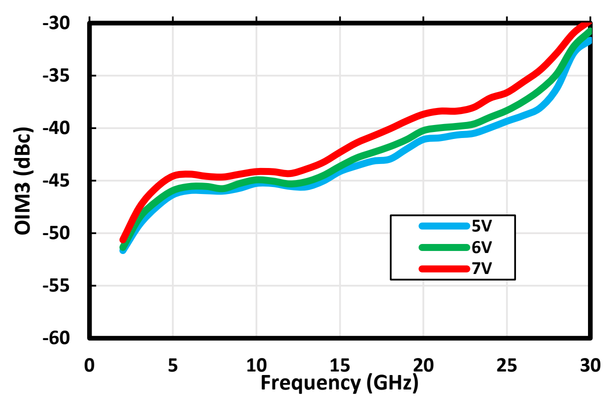


Figure 1-73. OIM3 vs. V_{DD} at 120 mA

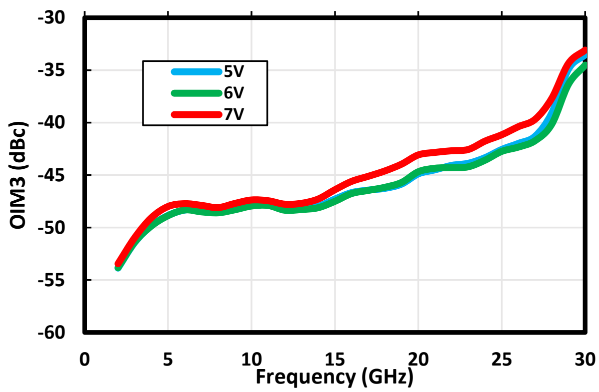
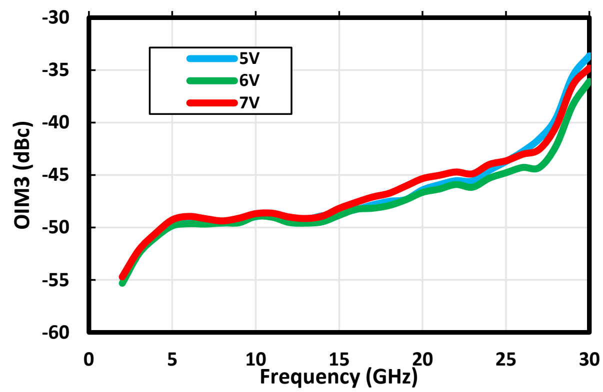


Figure 1-74. OIM3 vs. V_{DD} at 140 mA



1.3.3 Typical Performance vs. Output Power

The following graphs show the typical performance curves of the MMA042AA device at 25 °C vs. Output Power.

Figure 1-75. OIM2 vs. Power at 3.5V/60 mA

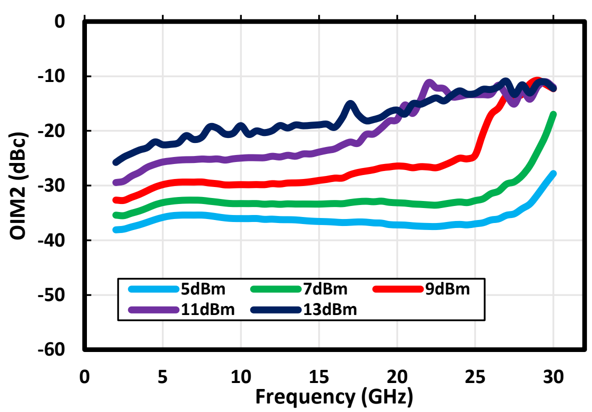


Figure 1-76. OIM2 vs. Power at 5V/100 mA

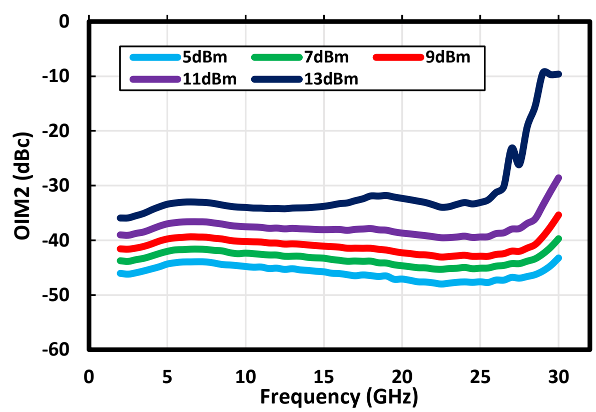


Figure 1-77. OIM2 vs. Power at 6V/120 mA

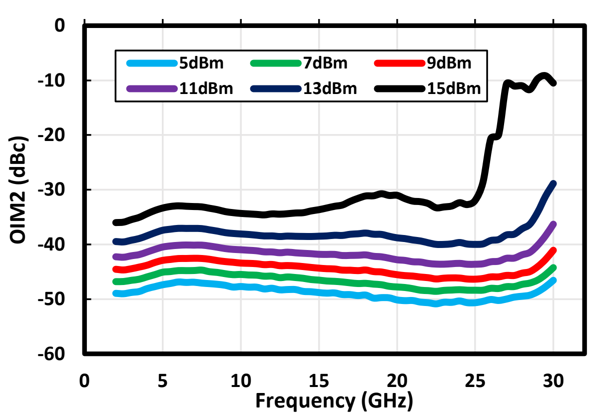


Figure 1-78. OIM2 vs. Power at 7V/140 mA

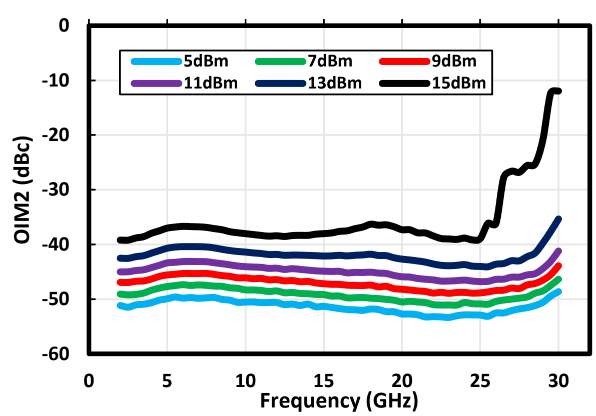


Figure 1-79. OIM3 vs. Power at 3.5V/60 mA

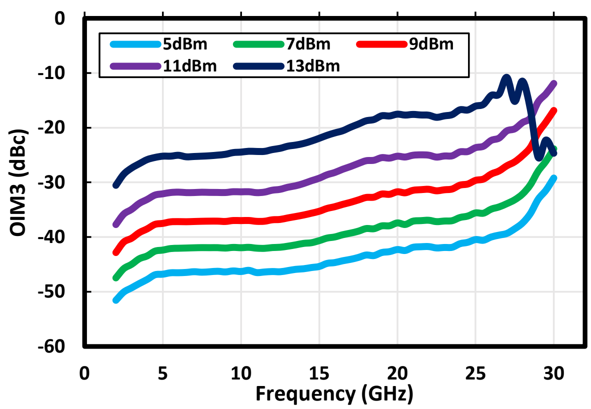


Figure 1-80. OIM3 vs. Power at 5V/100 mA

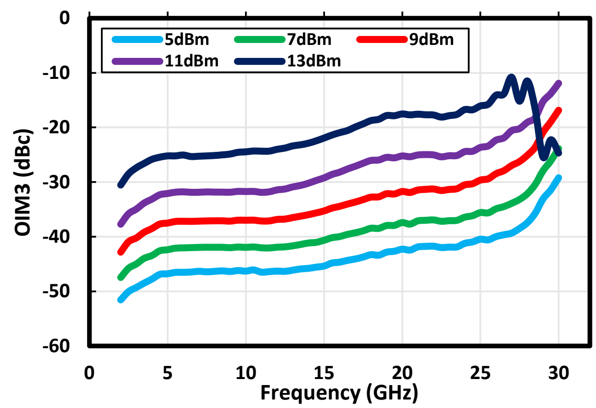


Figure 1-81. OIM3 vs. Power at 6V/120 mA

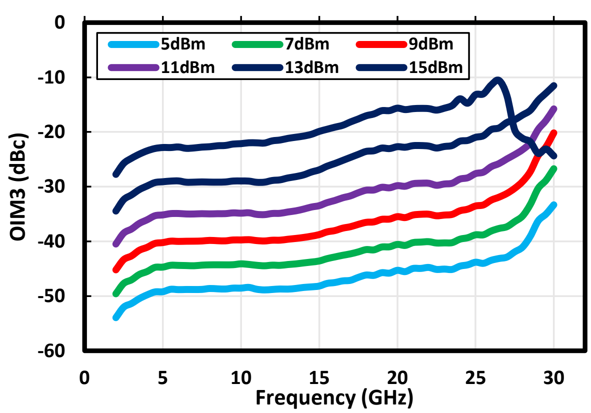


Figure 1-82. OIM3 vs. Power at 7V/140 mA

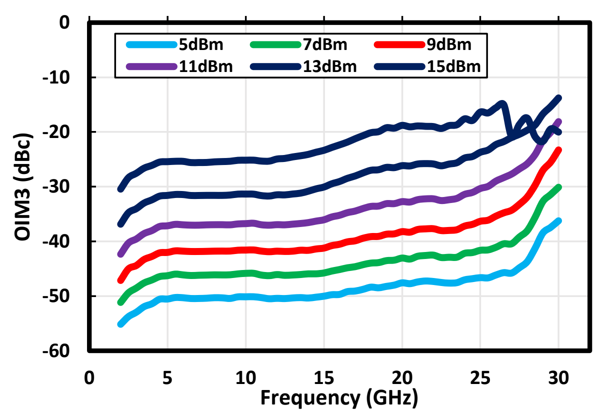


Figure 1-83. 2nd Harmonic vs. Power at 3.5V/60 mA

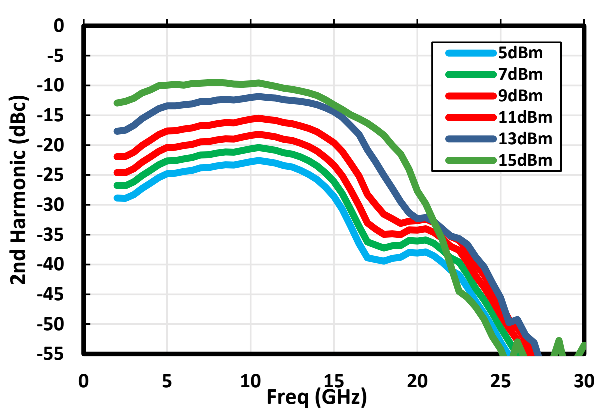


Figure 1-84. 2nd Harmonic vs. Power at 5V/100 mA

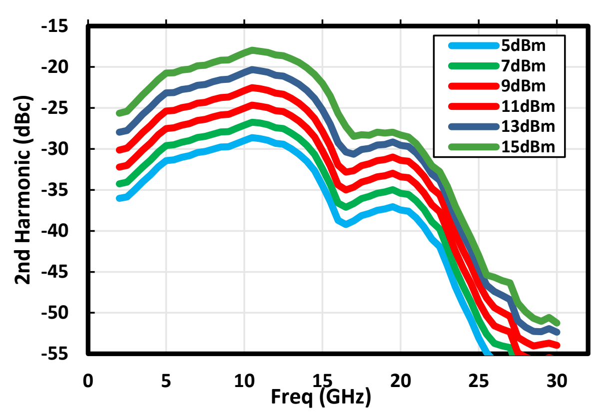


Figure 1-85. 2nd Harmonic vs. Power at 6V/120 mA

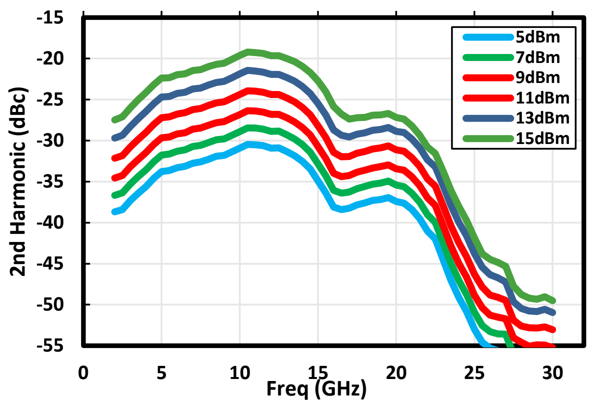
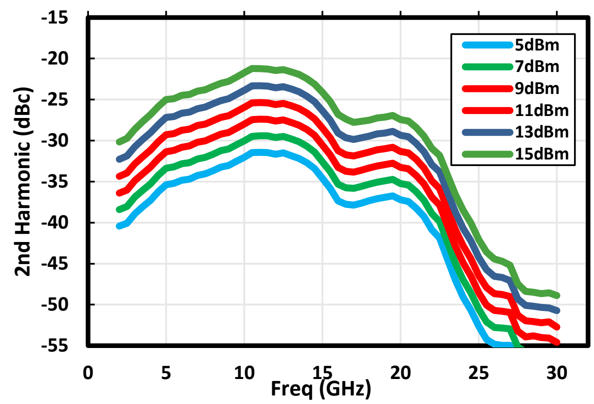


Figure 1-86. 2nd Harmonic vs. Power at 7V/140 mA



2. Die Specifications

The following illustration shows the chip outline of the MMA042AA device. Dimensions are in µm and are relative to the zero datum locations shown in the drawing. The minimum bond pad size is 100 µm × 100 µm. Both the bond pad surface and the backside metal are 3 µm gold. The die thickness is 100 µm. The backside is the DC/RF ground. The airbridge keepout region is in crosshatch, and the unlabeled pads should not be bonded.

For additional packaging information, contact your Microchip sales representative.

Figure 2-1. Die Outline Drawing

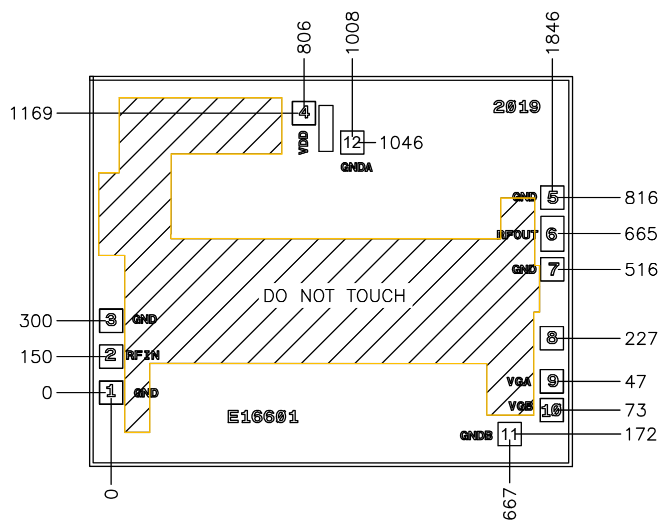


Table 2-1. PAD Dimensions

PAD No.	Description	PAD Sizes (µm)
1	GND	97 × 97
2	RFIN	97 × 97
3	GND	97 × 97
4	VDD	97 × 97
5	GND	97 × 97
6	RFOUT	97 × 146
7	GND	97 × 97
8	VSB	97 × 97
9	VGA	97 × 97
10	VGB	97 × 97
11	GNDB	97 × 97
12	GNDA	97 × 97

Table 2-2. I/O Pad Description

Pad Number	Pad Name	Pad Description
2	RFIN	This pad is DC–decoupled and matched to 50Ω.
6	RFOUT	This pad is DC–decoupled and matched to 50Ω.
4	V_{DD}	VDD Supply

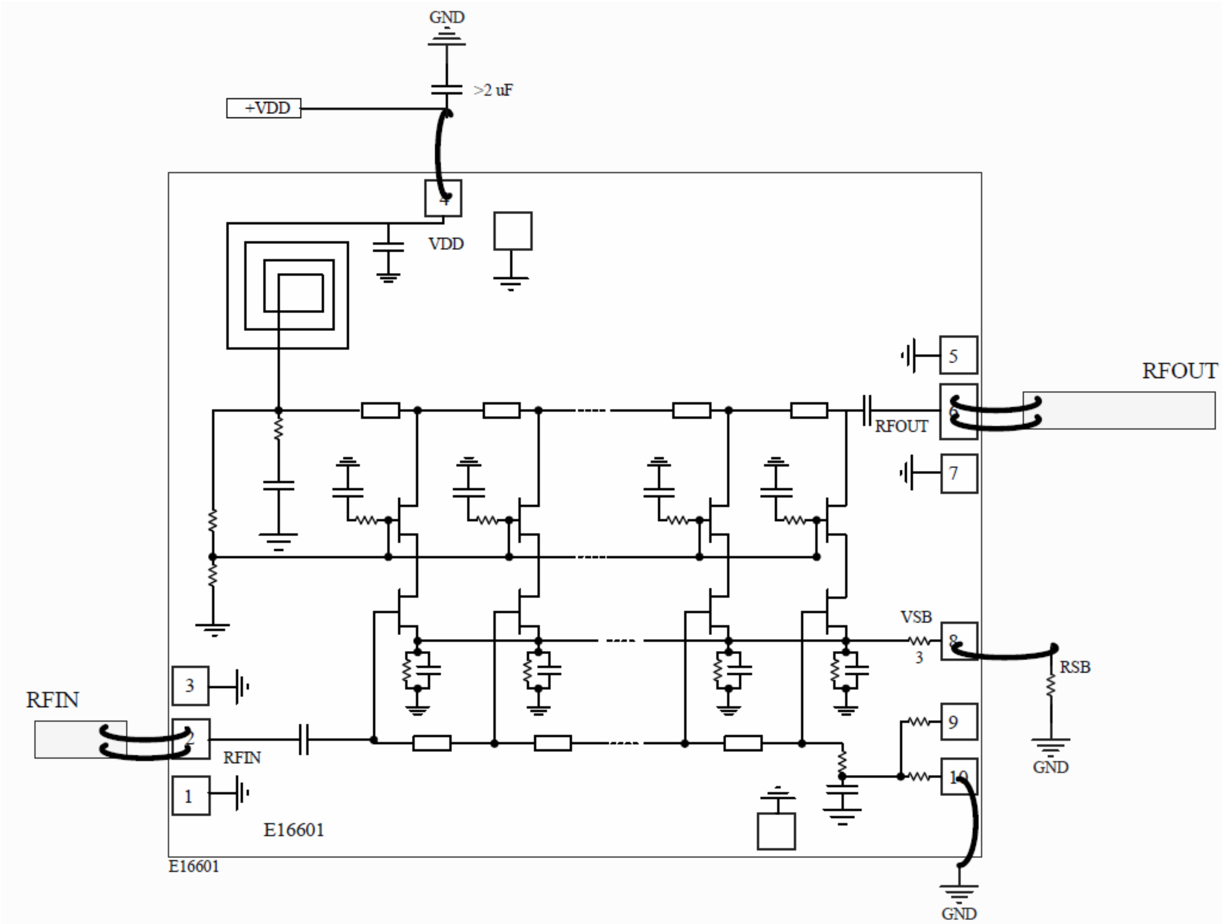
...........continued

Pad Number	Pad Name	Pad Description
8	V_{SB}	Used to set I_{DD}through external optional resistor RSB, see Table 5 below.
9, 10	V_{GA}, V_{GB}	Access to Gate 1 bias, Connect to Ground either for one nominal operation. See drawing on Figure 3-2 for correct bond-wire orientation
1, 3, 5, 7, 11, 12	GND	RF/DC ground pads, not used in typical applications
Backside Paddle	RF/DC GND	Must be connected to RF/DC ground

3. Application Circuit

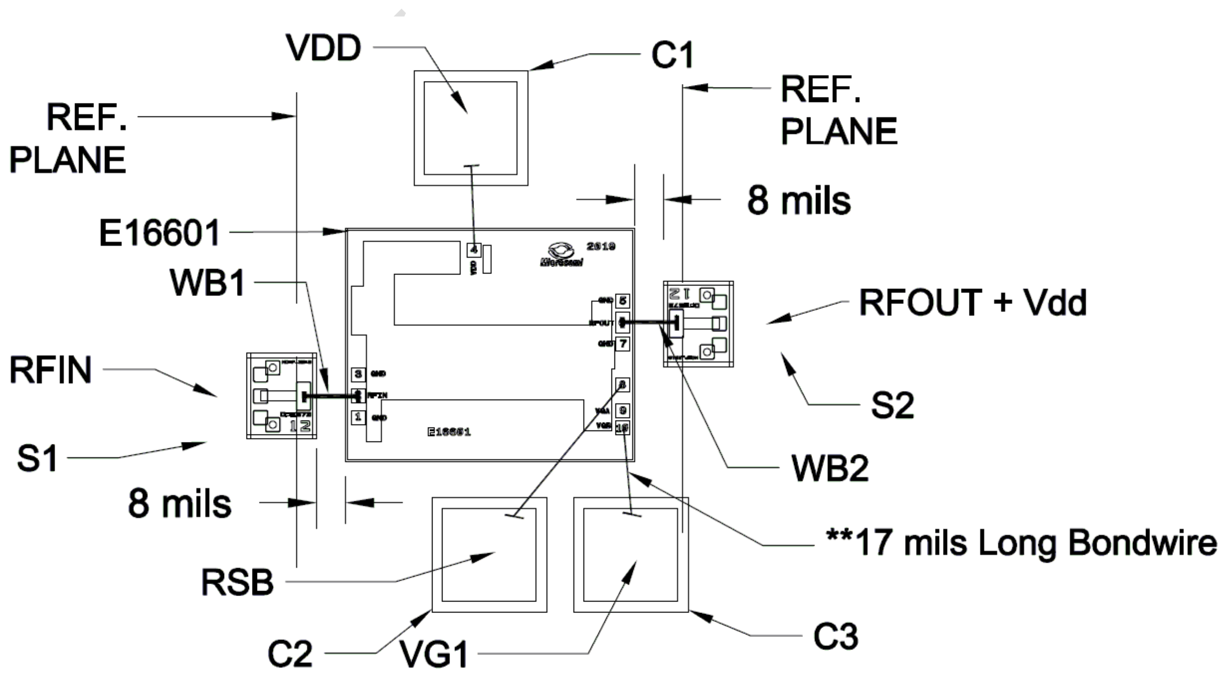
The following figure shows the application circuit schematic for this device.

Figure 3-1. Application Circuit: Schematic



The following figure shows the 2 GHz – 26 GHz test circuit assembly drawing for this device.

Figure 3-2. Test Circuit 2 GHz–26 GHz: Assembly Drawing



The following table lists the materials used in Figure 3-2 Assembly Drawing.

Table 3-1. List of Material for Figure 3-2: Assembly Drawing

Reference	Part Number	Description
E16601	MMA042AA	Amplifier Die
C1...C3	160U02A102MT4W	Johanson Dielectric SLC 1 nF (Values could be different from the Application Circuit Schematic for ease of Test Circuit Assembly)
S1, S2	E57312	Microchip Probe Launchers, calibrated with TRL kit to Ref. Planes shown
WB1, WB2	744–903–06	Microchip 2 mils Gold Ribbon, Should be as short as possible
RFIN/RFOUT		Location of the Input/Output GSG (150 μm) probes
VG1		Needle contact location for DC connection to VG1 (should be grounded if not used)
RSB		Contact for complimentary resistor (RSB) connection see table 5

The following table shows the RSB values versus drain current at 6V.

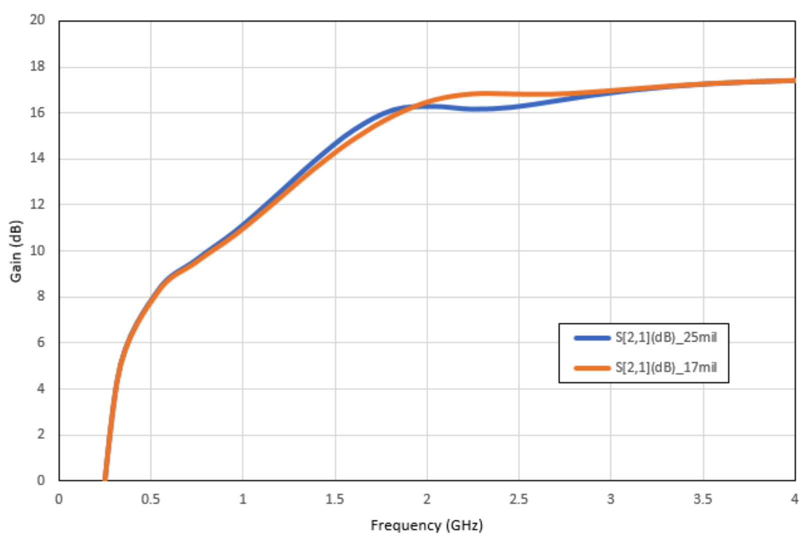
Table 3-2. RSB Values vs. Drain Current at 6V

RSB (Ω)	I_{DD}(mA) at 5V	I_{DD}(mA) at 6V	I_{DD} (mA) at 7V
0	130	131	136
1	122	125	129
2	116	120	123

...........continued			
RSB (Ω)	I_{DD}(mA) at 5V	I_{DD}(mA) at 6V	I_{DD} (mA) at 7V
3	112	115	119
4	108	112	116
5	106	109	113
6	103	107	110
7	101	104	108
8	100	103	106
9	98	101	105
10	96	100	103
11	95	98	102
12	94	97	101
13	93	97	100
14	92	96	99
15	92	95	98
16	91	94	97
17	90	94	97
18	90	93	96
19	89	92	96
20	89	92	95

The following figure shows the low-frequency S21 curve of this device.

Figure 3-3. Low Frequency S21: Comparison of 17 mils and 25 mils Bond-wire at VG1B at 6V/120 mA



4. Ordering, Shipping, and Handling

4.1 Handling Recommendations

Gallium arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

4.2 Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package	Note
MMA042AA	Die	
MMA042PP4	4 mm × 4 mm, 24L Plastic QFN	Refer to corresponding MMA042PP4 datasheet
MMA042PP4E	Evaluation board for MMA042PP4	
MMA042PP4/TR	Tape and reel	

4.3 Packing Information

Standard Format
Gel Pack

Note: Contact your Microchip sales representative for the minimum quantity order

5. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 5-1. Revision History

Revision	Date	Description
A	05/2024	Document migrated from Microsemi template to Microchip template; Assigned Microchip literature number DS-00005448.
Initial release (Microsemi Revision A)	2018	Document created.

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