

4-Kbit SPI Bus Serial EEPROM

Device Selection Table

Part Number	Vcc Range	Page Size	Temp. Ranges	Packages
25AA040A	1.8V-5.5V	16 bytes	I	MC, MS, P, OT, SN, MN, ST
25LC040A	2.5V-5.5V	16 bytes	I, E	MC, MS, P, OT, SN, MN, ST

Features

- 10 MHz Maximum Clock Speed
- Low-Power CMOS Technology:
 - Maximum Write current: 5 mA at 5.5V
 - Read current: 5 mA at 5.5V, 10 MHz
 - Standby current: 5 μ A at 5.5V
- 512 x 8-bit Organization
- 16-Byte Page
- Sequential Read
- Self-Timed Erase and Write Cycles (5 ms maximum)
- Block Write Protection:
 - Protect none, 1/4, 1/2 or all of array
- Built-In Write Protection:
 - Power-on/off data protection circuitry
 - Write enable latch
 - Write-protect pin
- High Reliability:
 - Endurance: 1M erase/write cycles
 - Data retention: > 200 years
 - ESD protection: > 4000V
- Temperature Ranges Supported:
 - Industrial (I): -40°C to +85°C
 - Extended (E): -40°C to +125°C
- RoHS Compliant
- Automotive AEC-Q100 Qualified

Packages

- 8-Lead DFN, 8-Lead MSOP, 8-Lead PDIP, 8-Lead SOIC, 6-Lead SOT23, 8-Lead TDFN and 8-Lead TSSOP

Pin Function Table

Name	Function
\overline{CS}	Chip Select Input
SO	Serial Data Output
\overline{WP}	Write-Protect Pin
Vss	Ground
SI	Serial Data Input
SCK	Serial Clock Input
HOLD	Hold Input
Vcc	Supply Voltage

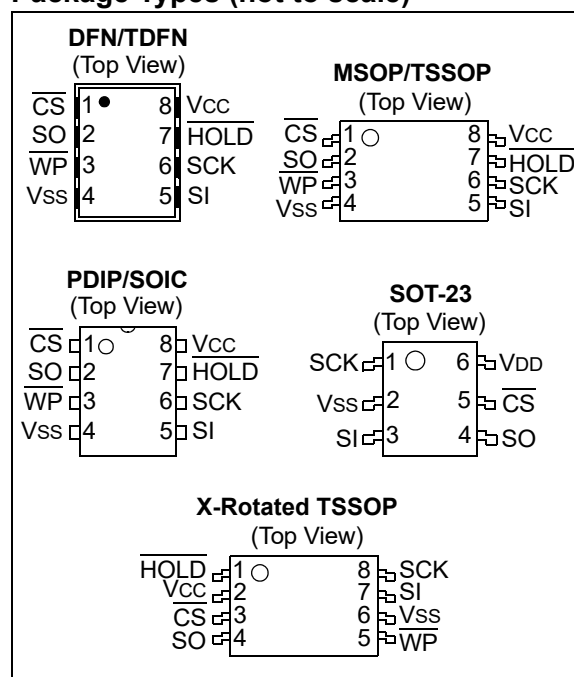
Description

The Microchip Technology Inc. 25XX040A⁽¹⁾ is a 4-Kbit Serial Electrically Erasable PROM (EEPROM). The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select (\overline{CS}) input.

Communication to the device can be paused via the hold pin (HOLD). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

Note 1: 25XX040A is used in this document as a generic part number for the 25AA040A and 25LC040A devices.

Package Types (not to scale)



25AA040A/25LC040A

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings^(†)

V _{CC}	6.5V
All inputs and outputs w.r.t. V _{SS}	-0.6V to V _{CC} +1.0V
Storage temperature	-65°C to +150°C
Ambient temperature under bias	-40°C to +125°C
ESD protection on all pins	4 kV

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Electrical Characteristics: Industrial (I): TA = -40°C to +85°C Vcc = 1.8V to 5.5V Extended (E): TA = -40°C to +125°C Vcc = 2.5V to 5.5V			
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Test Conditions
D001	VIH1	High-Level Input Voltage	0.7 Vcc	Vcc +1	V	
D002	VIL1	Low-Level Input Voltage	-0.3	0.3 Vcc	V	Vcc ≥ 2.7V (Note 1)
D003	VIL2		-0.3	0.2 Vcc	V	Vcc < 2.7V (Note 1)
D004	VOL	Low-Level Output Voltage	—	0.4	V	IoL = 2.1 mA
D005	VOL		—	0.2	V	IoL = 1.0 mA, Vcc = 2.5V
D006	VOH	High-Level Output Voltage	Vcc -0.5	—	V	IoH = -400 µA
D007	ILI	Input Leakage Current	—	±1	µA	CS = Vcc, VIN = Vss or Vcc
D008	ILO	Output Leakage Current	—	±1	µA	CS = Vcc, VOUT = Vss or Vcc
D009	CINT	Internal Capacitance (all inputs and outputs)	—	7	pF	TA = +25°C, CLK = 1.0 MHz, Vcc = 5.0V (Note 1)
D010	Icc Read	Operating Current	—	5	mA	Vcc = 5.5V; FCLK = 10.0 MHz; SO = Open
			—	2.5	mA	Vcc = 2.5V; FCLK = 5.0 MHz; SO = Open
D011	Icc Write		—	5	mA	Vcc = 5.5V
			—	3	mA	Vcc = 2.5V
D012	Iccs	Standby Current	—	5	µA	CS = Vcc = 5.5V, Inputs tied to Vcc or Vss, TA = +125°C
			—	1	µA	CS = Vcc = 2.5V, Inputs tied to Vcc or Vss, TA = +85°C

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): TA = -40°C to +85°C VCC = 1.8V to 5.5V Extended (E): TA = -40°C to +125°C VCC = 2.5V to 5.5V			
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Test Conditions
1	FCLK	Clock Frequency	—	10	MHz	4.5V ≤ VCC < 5.5V
			—	5	MHz	2.5V ≤ VCC < 4.5V
			—	3	MHz	1.8V ≤ VCC < 2.5V
2	TCSS	$\overline{\text{CS}}$ Setup Time	50	—	ns	4.5V ≤ VCC < 5.5V
			100	—	ns	2.5V ≤ VCC < 4.5V
			150	—	ns	1.8V ≤ VCC < 2.5V
3	TCSH	$\overline{\text{CS}}$ Hold Time	100	—	ns	4.5V ≤ VCC < 5.5V
			200	—	ns	2.5V ≤ VCC < 4.5V
			250	—	ns	1.8V ≤ VCC < 2.5V
4	TCSD	$\overline{\text{CS}}$ Disable Time	50	—	ns	
5	Tsu	Data Setup Time	10	—	ns	4.5V ≤ VCC < 5.5V
			20	—	ns	2.5V ≤ VCC < 4.5V
			30	—	ns	1.8V ≤ VCC < 2.5V
6	THD	Data Hold Time	20	—	ns	4.5V ≤ VCC < 5.5V
			40	—	ns	2.5V ≤ VCC < 4.5V
			50	—	ns	1.8V ≤ VCC < 2.5V
7	TR	CLK Rise Time	—	100	ns	Note 1
8	TF	CLK Fall Time	—	100	ns	Note 1
9	THI	Clock High Time	50	—	ns	4.5V ≤ VCC < 5.5V
			100	—	ns	2.5V ≤ VCC < 4.5V
			150	—	ns	1.8V ≤ VCC < 2.5V
10	TLO	Clock Low Time	50	—	ns	4.5V ≤ VCC < 5.5V
			100	—	ns	2.5V ≤ VCC < 4.5V
			150	—	ns	1.8V ≤ VCC < 2.5V
11	TCLD	Clock Delay Time	50	—	ns	
12	TCLE	Clock Enable Time	50	—	ns	
13	Tv	Output Valid from Clock Low	—	50	ns	4.5V ≤ VCC < 5.5V
			—	100	ns	2.5V ≤ VCC < 4.5V
			—	160	ns	1.8V ≤ VCC < 2.5V
14	THO	Output Hold Time	0	—	ns	Note 1
15	TDIS	Output Disable Time	—	40	ns	4.5V ≤ VCC < 5.5V (Note 1)
			—	80	ns	2.5V ≤ VCC < 4.5V (Note 1)
			—	160	ns	1.8V ≤ VCC < 2.5V (Note 1)

Note 1: This parameter is periodically sampled and not 100% tested.

2: Twc begins on the rising edge of $\overline{\text{CS}}$ after a valid write sequence and ends when the internal write cycle is complete.

3: This parameter is not tested but ensured by characterization.

25AA040A/25LC040A

TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): TA = -40°C to +85°C VCC = 1.8V to 5.5V Extended (E): TA = -40°C to +125°C VCC = 2.5V to 5.5V			
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Test Conditions
16	THS	$\overline{\text{HOLD}}$ Setup Time	20	—	ns	$4.5\text{V} \leq V_{CC} < 5.5\text{V}$
			40	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
			80	—	ns	$1.8\text{V} \leq V_{CC} < 2.5\text{V}$
17	THH	$\overline{\text{HOLD}}$ Hold Time	20	—	ns	$4.5\text{V} \leq V_{CC} < 5.5\text{V}$
			40	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
			80	—	ns	$1.8\text{V} \leq V_{CC} < 2.5\text{V}$
18	THZ	$\overline{\text{HOLD}}$ Low to Output High-Z	—	30	ns	$4.5\text{V} \leq V_{CC} < 5.5\text{V}$ (Note 1)
			—	60	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$ (Note 1)
			—	160	ns	$1.8\text{V} \leq V_{CC} < 2.5\text{V}$ (Note 1)
19	THV	$\overline{\text{HOLD}}$ High to Output Valid	—	30	ns	$4.5\text{V} \leq V_{CC} < 5.5\text{V}$
			—	60	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
			—	160	ns	$1.8\text{V} \leq V_{CC} < 2.5\text{V}$
20	TWC	Internal Write Cycle Time (byte or page)	—	5	ms	Note 2
21		Endurance	1M	—	E/W Cycles	+25°C, VCC = 5.5V, Page Mode (Note 3)

Note 1: This parameter is periodically sampled and not 100% tested.

2: TWC begins on the rising edge of CS after a valid write sequence and ends when the internal write cycle is complete.

3: This parameter is not tested but ensured by characterization.

TABLE 1-3: AC TEST CONDITIONS

AC Waveform	
VLO = 0.2V	—
VHI = VCC - 0.2V	Note 1
VHI = 4.0V	Note 2
CL = 100 pF	—
Timing Measurement Reference Level	
Input	0.5 VCC
Output	0.5 VCC

Note 1: For VCC ≤ 4.0V

2: For VCC ≥ 4.0V

FIGURE 1-1: HOLD TIMING

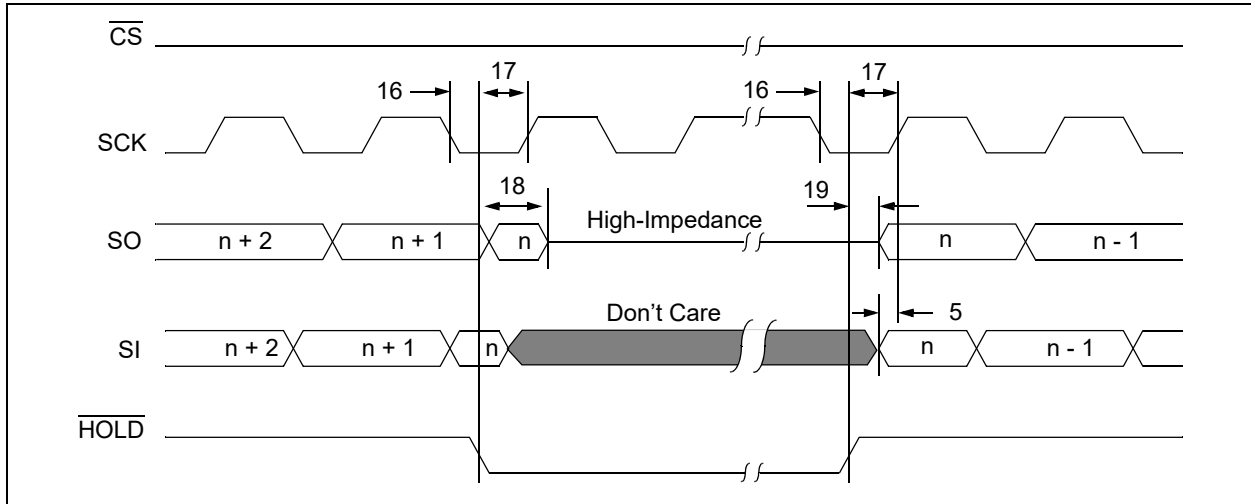


FIGURE 1-2: SERIAL INPUT TIMING

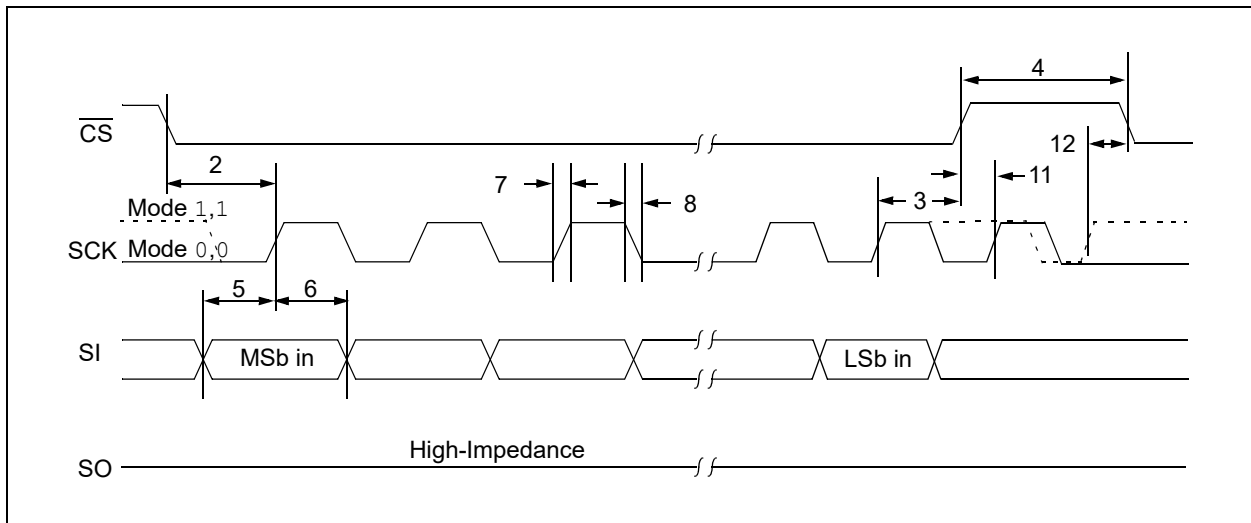
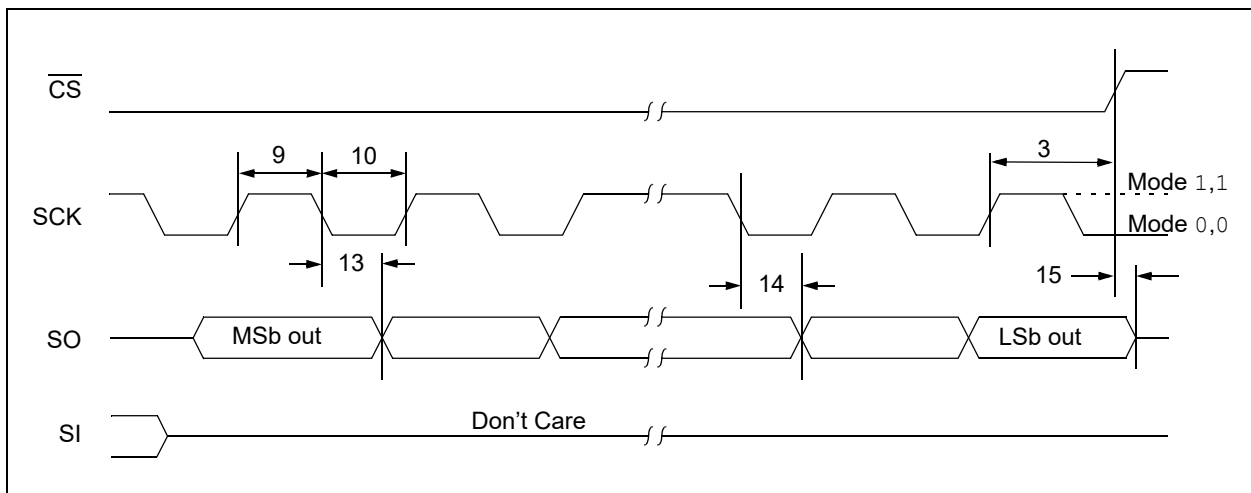


FIGURE 1-3: SERIAL OUTPUT TIMING



25AA040A/25LC040A

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

TABLE 2-1: PIN FUNCTION TABLE

Name	DFN ⁽¹⁾	MSOP	PDIP	SOIC	SOT-23	TDFN ⁽¹⁾	TSSOP	Rotated TSSOP	Function
$\overline{\text{CS}}$	1	1	1	1	5	1	1	3	Chip Select Input
SO	2	2	2	2	4	2	2	4	Serial Data Output
$\overline{\text{WP}}$	3	3	3	3	—	3	3	5	Write-Protect Pin
Vss	4	4	4	4	2	4	4	6	Ground
SI	5	5	5	5	3	5	5	7	Serial Data Input
SCK	6	6	6	6	1	6	6	8	Serial Clock Input
HOLD	7	7	7	7	—	7	7	1	Hold Input
Vcc	8	8	8	8	6	8	8	2	Supply Voltage

Note 1: The exposed pad on the DFN/TDFN packages can be connected to Vss or left floating.

2.1 Chip Select ($\overline{\text{CS}}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{\text{CS}}$ input signal. If $\overline{\text{CS}}$ is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus.

A low-to-high transition on $\overline{\text{CS}}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{\text{CS}}$ is required prior to any sequence being initiated.

2.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25XX040A. During a read cycle, data are shifted out on this pin after the falling edge of the serial clock.

2.3 Write-Protect ($\overline{\text{WP}}$)

The $\overline{\text{WP}}$ pin is a hardware write-protect input pin. When it is low, all writes to the array or STATUS registers are disabled, but any other operations function normally. When $\overline{\text{WP}}$ is high, all functions, including nonvolatile writes, operate normally. At any time, when $\overline{\text{WP}}$ is low, the write enable latch will be reset and programming will be inhibited. However, if a write cycle is already in progress, $\overline{\text{WP}}$ going low will not change or disable the write cycle. See [Table 3-4](#) for the Write-Protect Functionality Matrix.

2.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data are latched on the rising edge of the serial clock.

2.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a host and the 25XX040A. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin are updated after the falling edge of the clock input.

2.6 Hold (HOLD)

The HOLD pin is used to suspend transmission to the 25XX040A while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the HOLD pin may be pulled low to pause further serial communication without resetting the serial sequence.

The HOLD pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-to-low transition. The 25XX040A must remain selected during this sequence. The SI and SCK levels are “don’t cares” during the time the device is paused and transitions on these pins will be ignored. To resume serial communication, HOLD must be brought high while the SCK pin is low, otherwise serial communication will not be resumed until the next SCK high-to-low transition.

The SO line will tri-state immediately upon a high-to-low transition of the HOLD pin and will begin outputting again immediately upon a subsequent low-to-high transition of the HOLD pin, independent of the state of SCK.

3.0 FUNCTIONAL DESCRIPTION

3.1 Principles of Operation

The 25XX040A is a 512-byte Serial EEPROM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in firmware to match the SPI protocol.

The 25XX040A contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{\text{CS}}$ pin must be low and the $\overline{\text{HOLD}}$ pin must be high for the entire operation.

Table 3-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses and data are transferred Most Significant bit (MSb) first, Least Significant bit (LSb) last.

Data (SI) are sampled on the first rising edge of SCK after $\overline{\text{CS}}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{\text{HOLD}}$ input and place the 25XX040A in 'HOLD' mode. After releasing the $\overline{\text{HOLD}}$ pin, operation will resume from the point when the $\overline{\text{HOLD}}$ was asserted.

BLOCK DIAGRAM

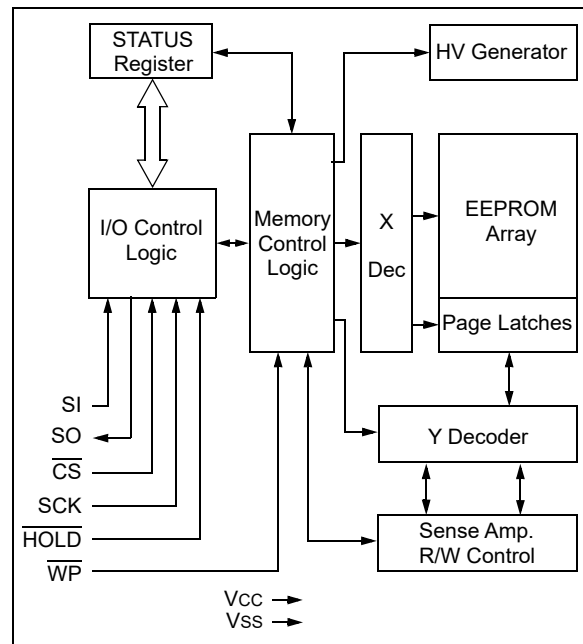


TABLE 3-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 A_8 011 ⁽¹⁾	Read data from memory array beginning at selected address
WRITE	0000 A_8 010 ⁽¹⁾	Write data to memory array beginning at selected address
WRDI	0000 x100 ⁽²⁾	Reset the write enable latch (disable write operations)
WREN	0000 x110 ⁽²⁾	Set the write enable latch (enable write operations)
RDSR	0000 x101 ⁽²⁾	Read STATUS register
WRSR	0000 x001 ⁽²⁾	Write STATUS register

Note 1: A_8 is the 9th address bit, which is used to address the entire 512-byte array.

Note 2: x = don't care

25AA040A/25LC040A

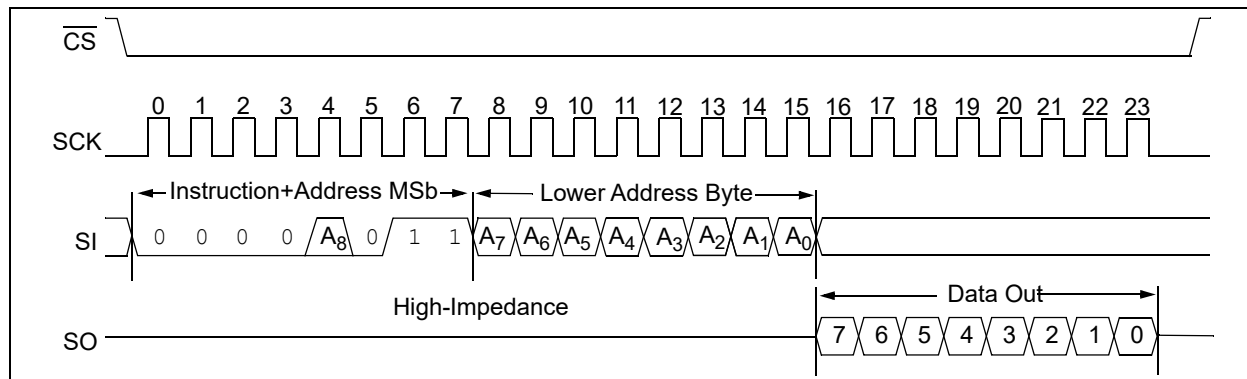
3.2 Read Sequence

The device is selected by pulling \overline{CS} low. The 8-bit `READ` instruction is transmitted to the 25XX040A followed by a 9-bit address. The MSb (A_8) is sent to the client during the instruction sequence. See [Figure 3-1](#) for more details.

After the correct `READ` instruction and address are sent, the data stored in the memory at the selected address are shifted out on the `SO` pin. Data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses to the client.

The internal Address Pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (1FFh), the address counter rolls over to address 000h, allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the \overline{CS} pin ([Figure 3-1](#)).

FIGURE 3-1: READ SEQUENCE



3.3 Write Sequence

Prior to any attempt to write data to the 25XX040A, the write enable latch must be set by issuing the `WREN` instruction (Figure 3-4). This is done by setting \overline{CS} low and then clocking out the proper instruction into the 25XX040A. After all eight bits of the instruction are transmitted, \overline{CS} must be driven high to set the write enable latch.

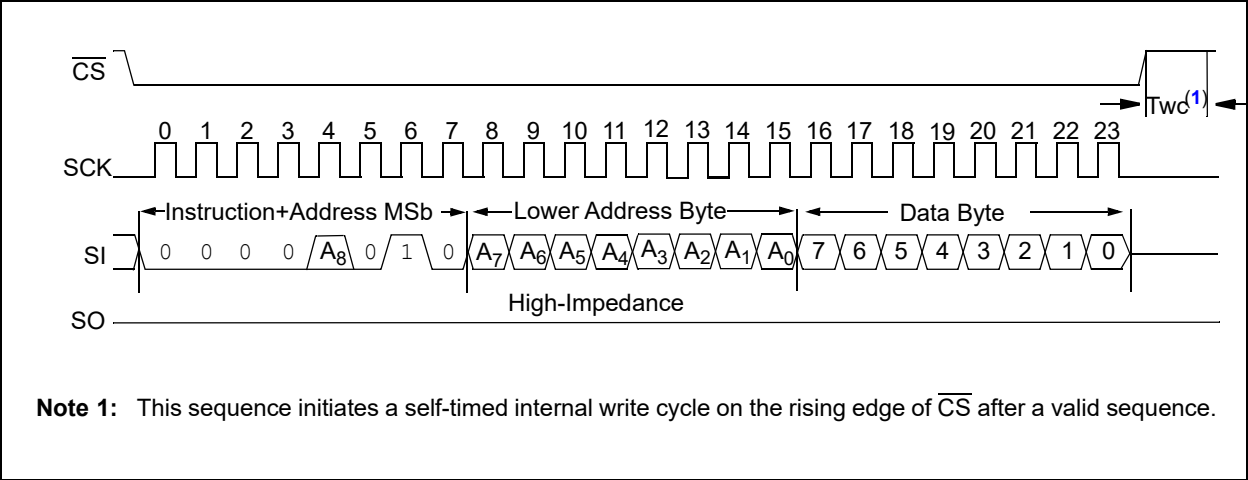
If the write operation is initiated immediately after the `WREN` instruction without \overline{CS} driven high, data will not be written to the array since the write enable latch was not properly set.

After setting the write enable latch, the user may proceed by driving \overline{CS} low, issuing a `WRITE` instruction, followed by the remainder of the address and then the data to be written. Keep in mind that the Most Significant address bit (A_8) is included in the instruction byte for the 25XX040A. Up to 16 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. Additionally, a page address begins with `XXXX 0000` and ends with `XXXX 1111`. If the internal address counter reaches `XXXX 1111` and clock signals continue to be applied to the chip, the address counter will roll back to the first address of the page and overwrite any data that previously existed in those locations.

Note: Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of page size - 1. If a Page Write command attempts to write across a physical page boundary, the result is that the data wrap around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

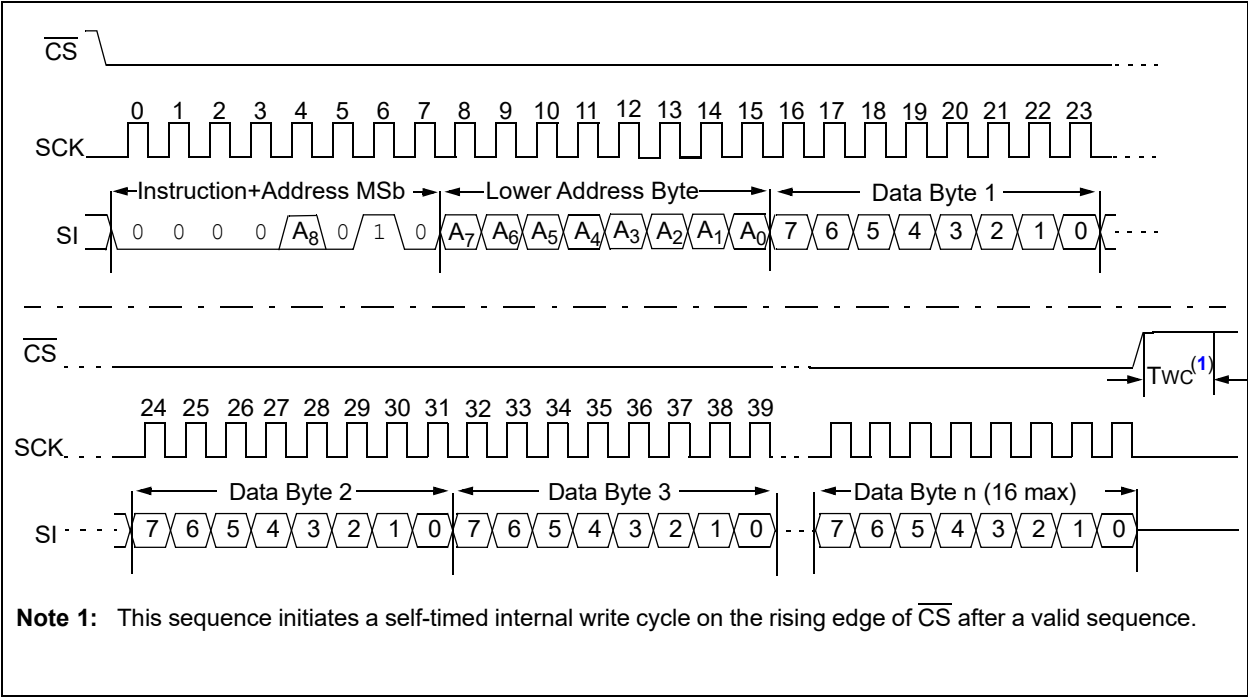
For the data to be actually written to the array, the \overline{CS} must be brought high after the Least Significant bit (D_0) of the n^{th} data byte has been clocked in. If \overline{CS} is driven high at any other time, the write operation will not be completed. Refer to Figure 3-2 and Figure 3-3 for more detailed illustrations on the byte write sequence and the page write sequence, respectively. While the write is in progress, the STATUS register may be read to check the status of the WPEN, WIP, WEL, BP1 and BP0 bits (Figure 3-6). Attempting to read a memory array location will not be possible during a write cycle. Polling the WIP bit in the STATUS register is recommended in order to determine if a write cycle is in progress. When the write cycle is completed, the write enable latch is reset.

FIGURE 3-2: BYTE WRITE SEQUENCE



25AA040A/25LC040A

FIGURE 3-3: PAGE WRITE SEQUENCE



3.4 Write Enable (WREN) and Write Disable (WRDI)

The 25XX040A contains a write enable latch. See [Table 3-4](#) for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed
- \overline{WP} pin is brought low

FIGURE 3-4: WRITE ENABLE SEQUENCE (WREN)

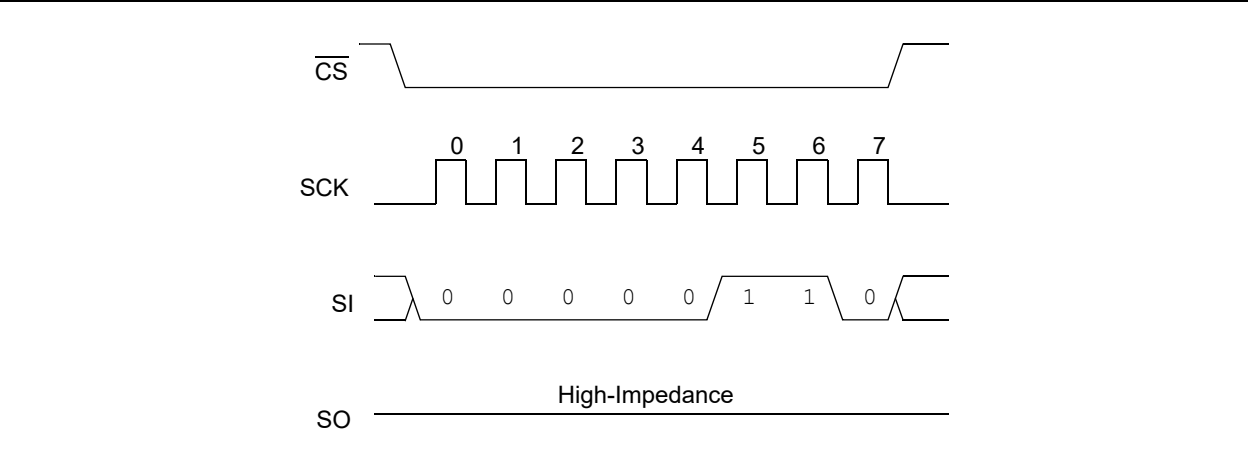
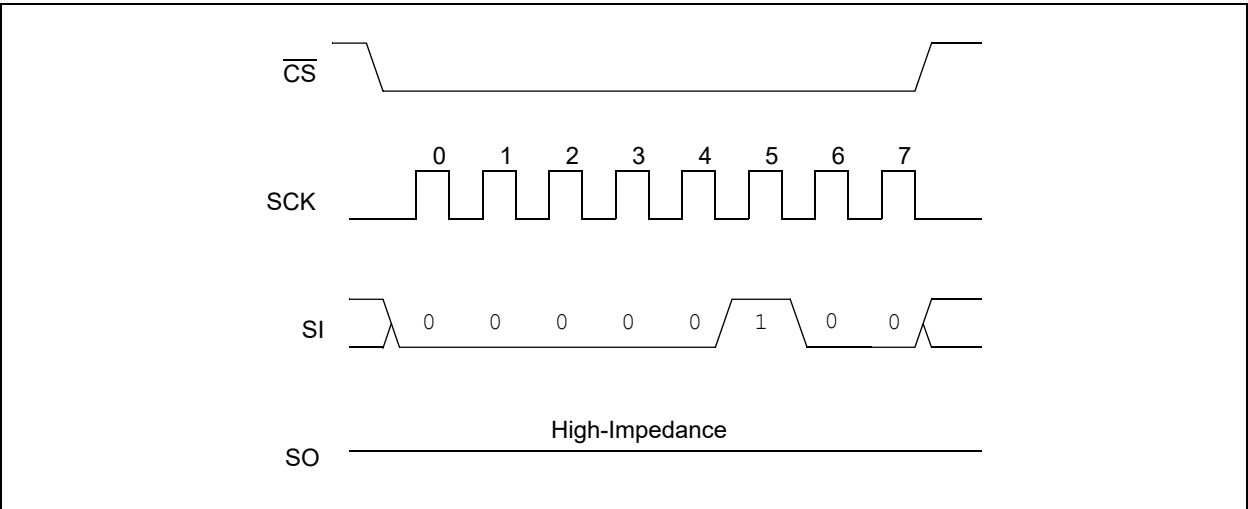


FIGURE 3-5: WRITE DISABLE SEQUENCE (WRDI)



3.5 Read Status Register Instruction (RDSR)

The Read Status Register instruction (RDSR) provides access to the STATUS register. See Figure 3-6 for the RDSR timing sequence. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

TABLE 3-2: STATUS REGISTER

7	6	5	4	3	2	1	0
–	–	–	–	W/R	W/R	R	R
X	X	X	X	BP1	BP0	WEL	WIP

Note 1: W/R = writable/readable. R = read-only.

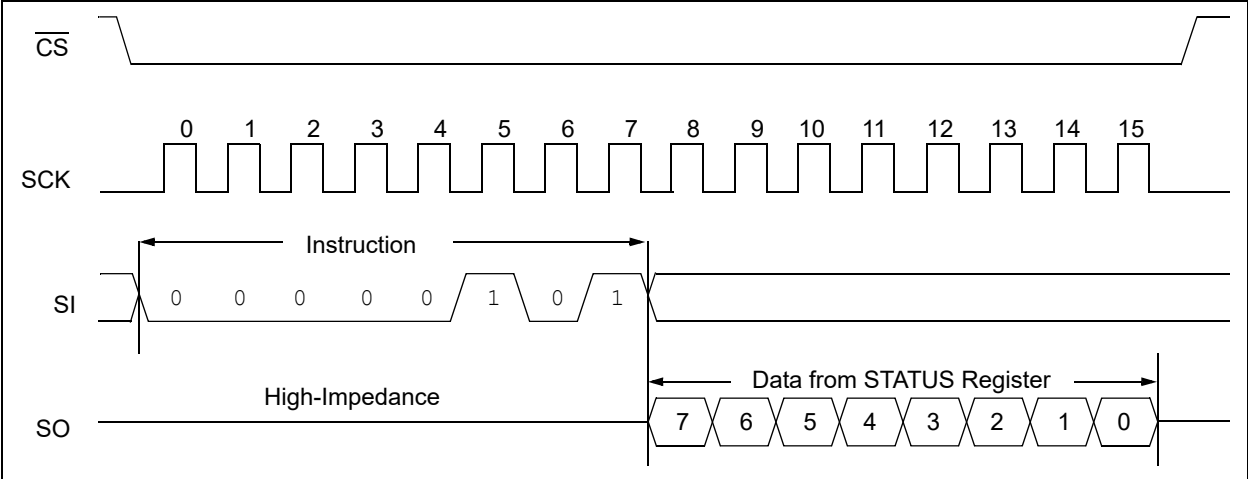
The Write-In-Process (WIP) bit indicates whether the 25XX040A is busy with a write operation. When set to a ‘1’, a write is in progress, when set to a ‘0’, no write is in progress. This bit is read-only.

The Write Enable Latch (WEL) bit indicates the status of the write enable latch and is read-only. When set to a ‘1’, the latch allows writes to the array, when set to a ‘0’, the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the STATUS register. These commands are shown in Figure 3-4 and Figure 3-5.

The Block Protection (BP0 and BP1) bits indicate which blocks are currently write-protected. These bits are set by the user issuing the WRSR instruction (see Figure 3-7). These bits are nonvolatile and are described in more detail in Table 3-3.

See Figure 3-6 for the RDSR timing sequence.

FIGURE 3-6: READ STATUS REGISTER TIMING SEQUENCE (RDSR)



3.6 Write Status Register Instruction (WRSR)

The Write Status Register instruction (WRSR) allows the user to write to the nonvolatile bits in the STATUS register as shown in Table 3-2. Four levels of protection for the array are selectable by writing to the appropriate bits in the STATUS register. The user has the ability to write-protect none, one, two or all four of the segments of the array as shown in Table 3-3. See Figure 3-7 for the WRSR timing sequence.

TABLE 3-3: ARRAY PROTECTION

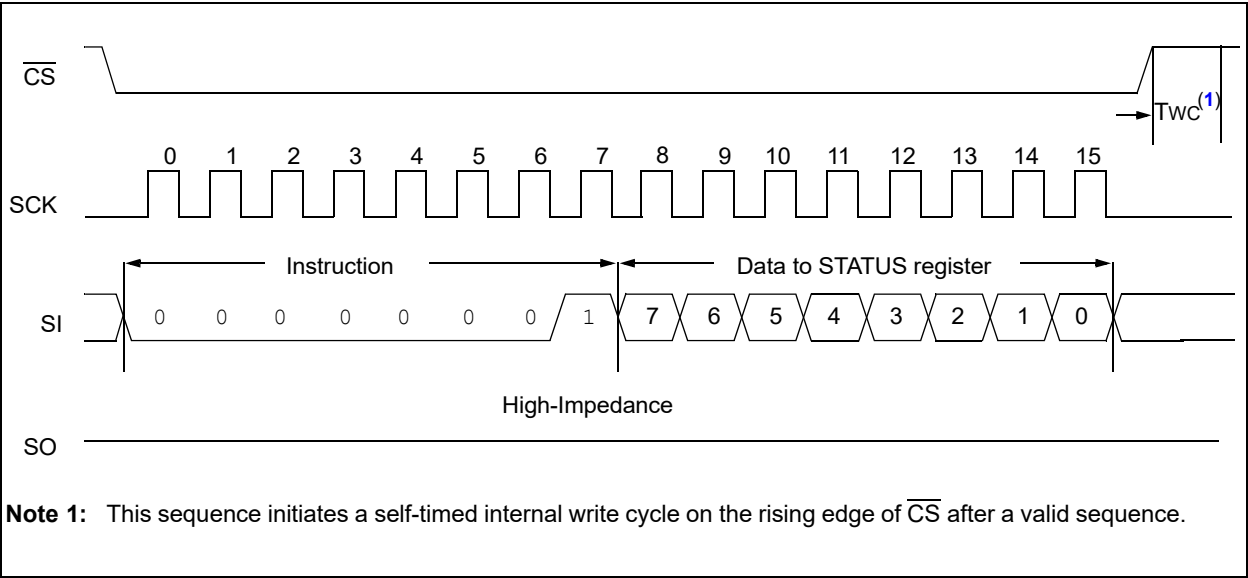
BP1	BP0	Array Addresses Write-Protected
0	0	none
0	1	upper 1/4 (180h-1FFh)
1	0	upper 1/2 (100h-1FFh)
1	1	all (000h-1FFh)

TABLE 3-4: WRITE-PROTECT FUNCTIONALITY MATRIX

WP (pin 3)	WEL (SR bit 1)	Protected Blocks	Unprotected Blocks	STATUS Register
0 (low)	x	Protected	Protected	Protected
1 (high)	0	Protected	Protected	Protected
1 (high)	1	Protected	Writable	Writable

Note 1: x = don't care

FIGURE 3-7: WRITE STATUS REGISTER TIMING SEQUENCE (WRSR)



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of \overline{CS} after a valid sequence.

4.0 DATA PROTECTION

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or STATUS register write, the write enable latch is reset
- \overline{CS} must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

5.0 POWER-ON STATE

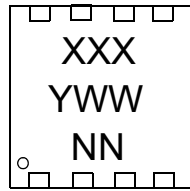
The 25XX040A powers on in the following state:

- The device is in low-power Standby mode ($\overline{CS} = 1$)
- The write enable latch is reset
- SO is in high-impedance state
- A high-to-low-level transition on \overline{CS} is required to enter active state

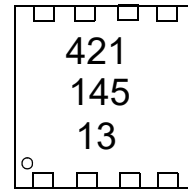
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

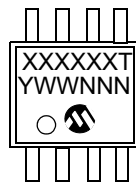
8-Lead 2X3 DFN



Example



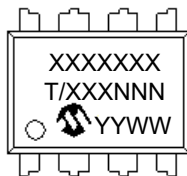
8-Lead MSOP (150 mil)



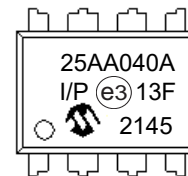
Example



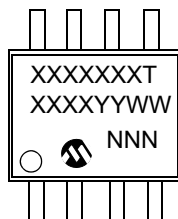
8-Lead PDIP (300 mil)



Example



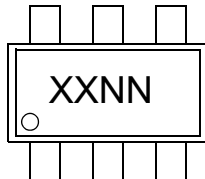
8-Lead SOIC



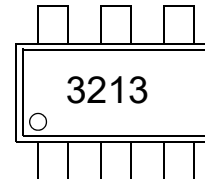
Example



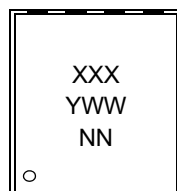
6-Lead SOT-23



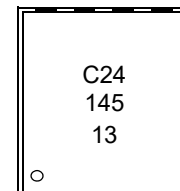
Example



8-Lead 2x3 TDFN



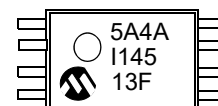
Example



8-Lead TSSOP



Example



25AA040A/25LC040A

Part Number	1 st Line Marking Codes								
	DFN		MSOP	SOT-23		TDFN		TSSOP	
	I-Temp.	E-Temp.		I-Temp.	E-Temp.	I-Temp.	E-Temp.	Standard	Rotated
25AA040A	421	—	5A4AT	32NN	—	C21	—	5A4A	A4AX
25LC040A	424	425	5L4AT	35NN	36NN	C24	C25	5L4A	L4AX

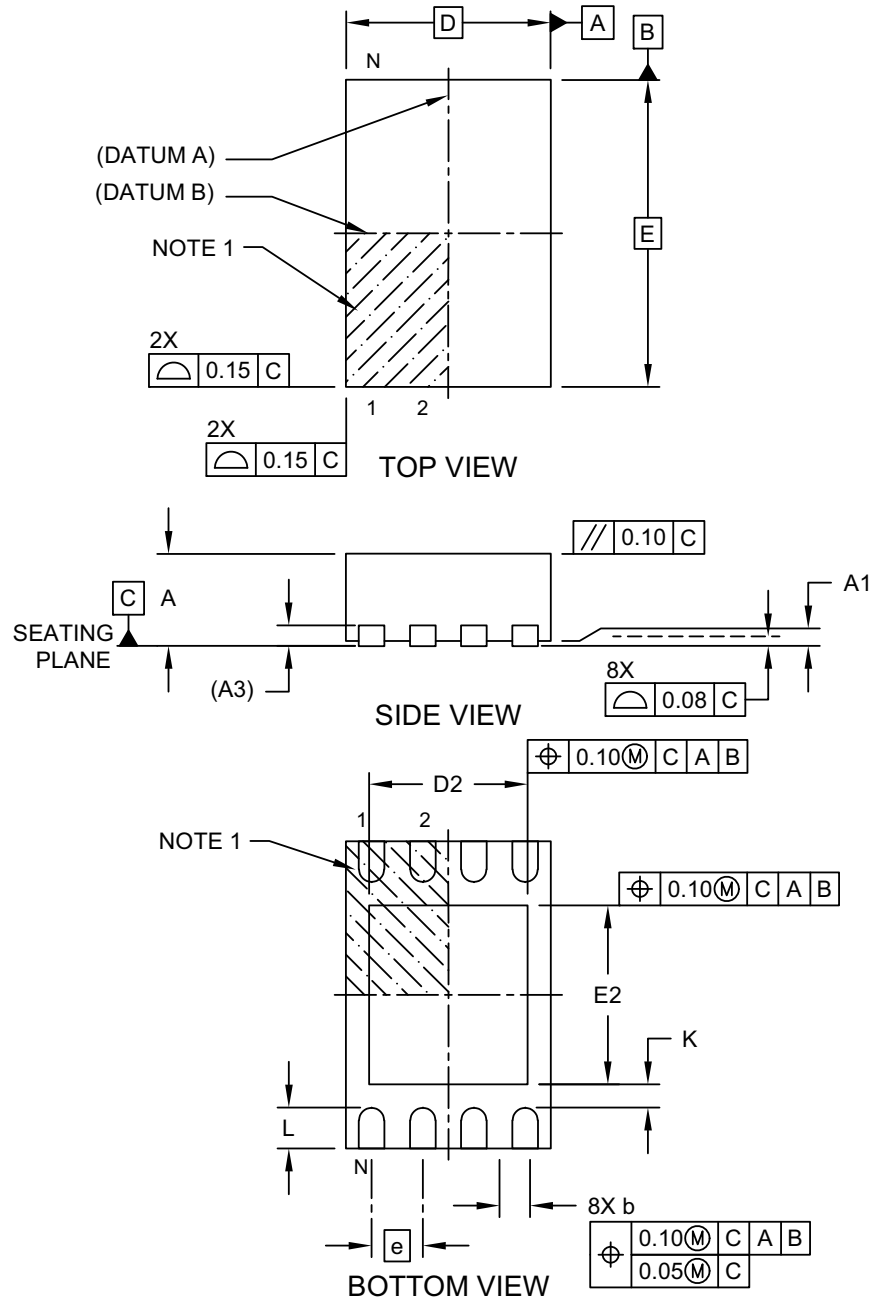
Legend: XX...X Part number or part number code
T Temperature (I, E)
Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code (2 characters for small packages)
Ⓔ3 RoHS-compliant JEDEC[®] designator for Matte Tin (Sn)

Note: For very small packages with no room for the RoHS-compliant JEDEC[®] designator Ⓔ3, the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x1 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

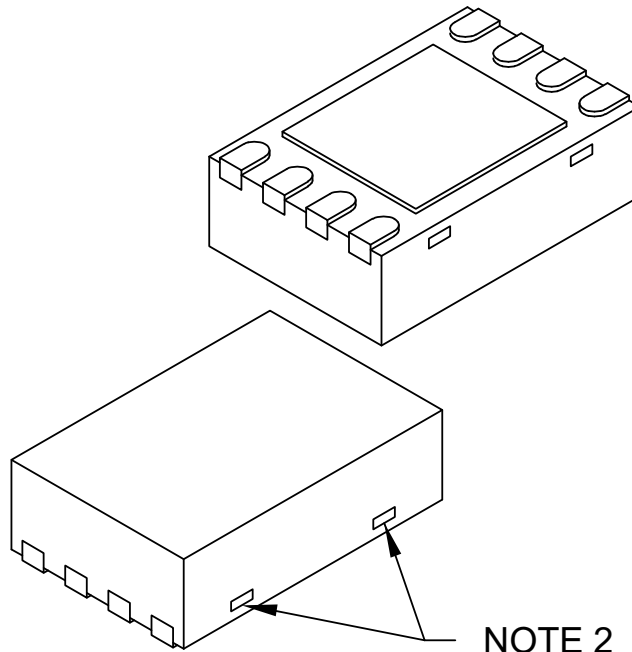


Microchip Technology Drawing C04-123 Rev E Sheet 1 of 2

25AA040A/25LC040A

8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x1 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Length	D	2.00 BSC		
Exposed Pad Length	D2	1.30	-	1.55
Overall Width	E	3.00 BSC		
Exposed Pad Width	E2	1.50	-	1.75
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

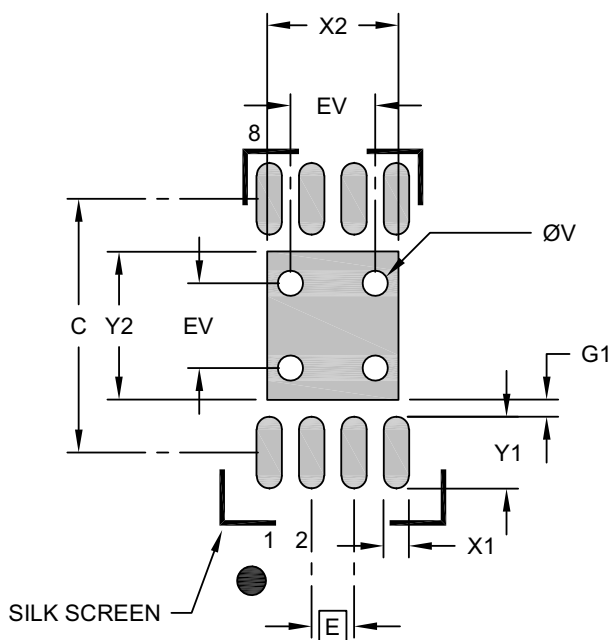
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123 Rev E Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x1 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			1.55
Optional Center Pad Length	Y2			1.75
Contact Pad Spacing	C		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

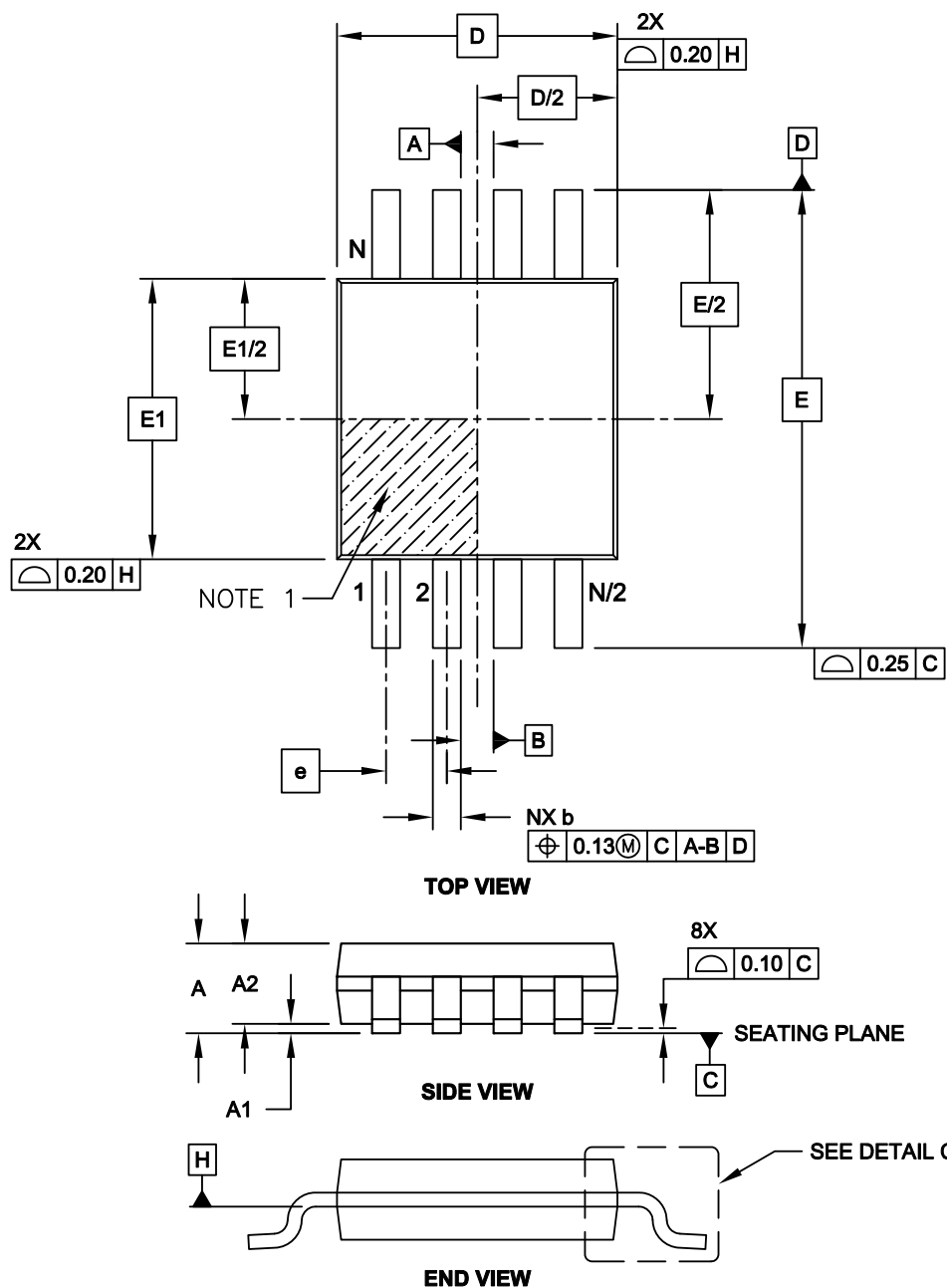
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2123 Rev E

25AA040A/25LC040A

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

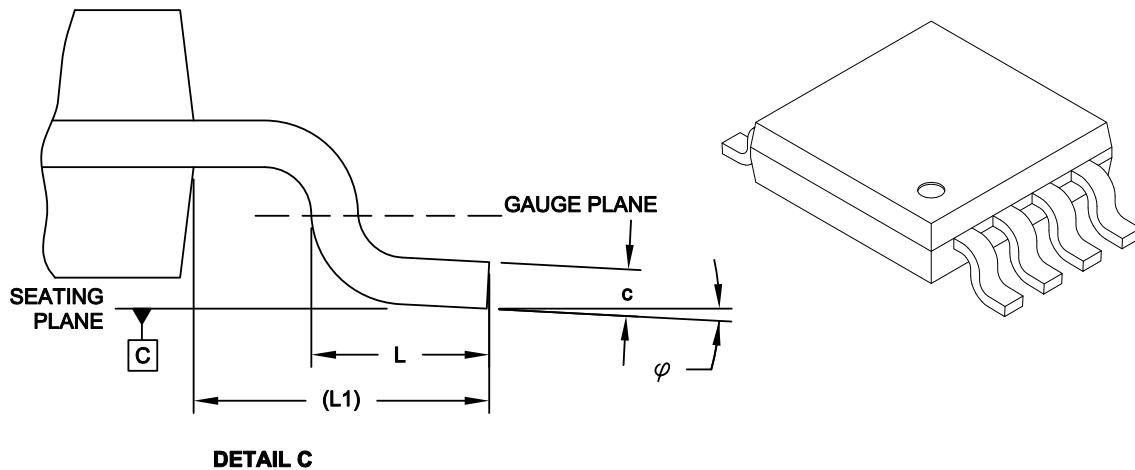
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e	0.65 BSC		
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Overall Length	D	3.00 BSC		
Foot Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

Notes:

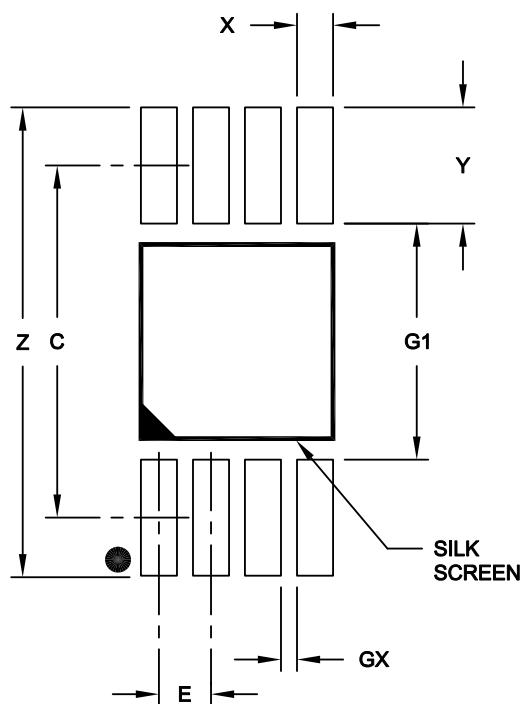
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

25AA040A/25LC040A

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

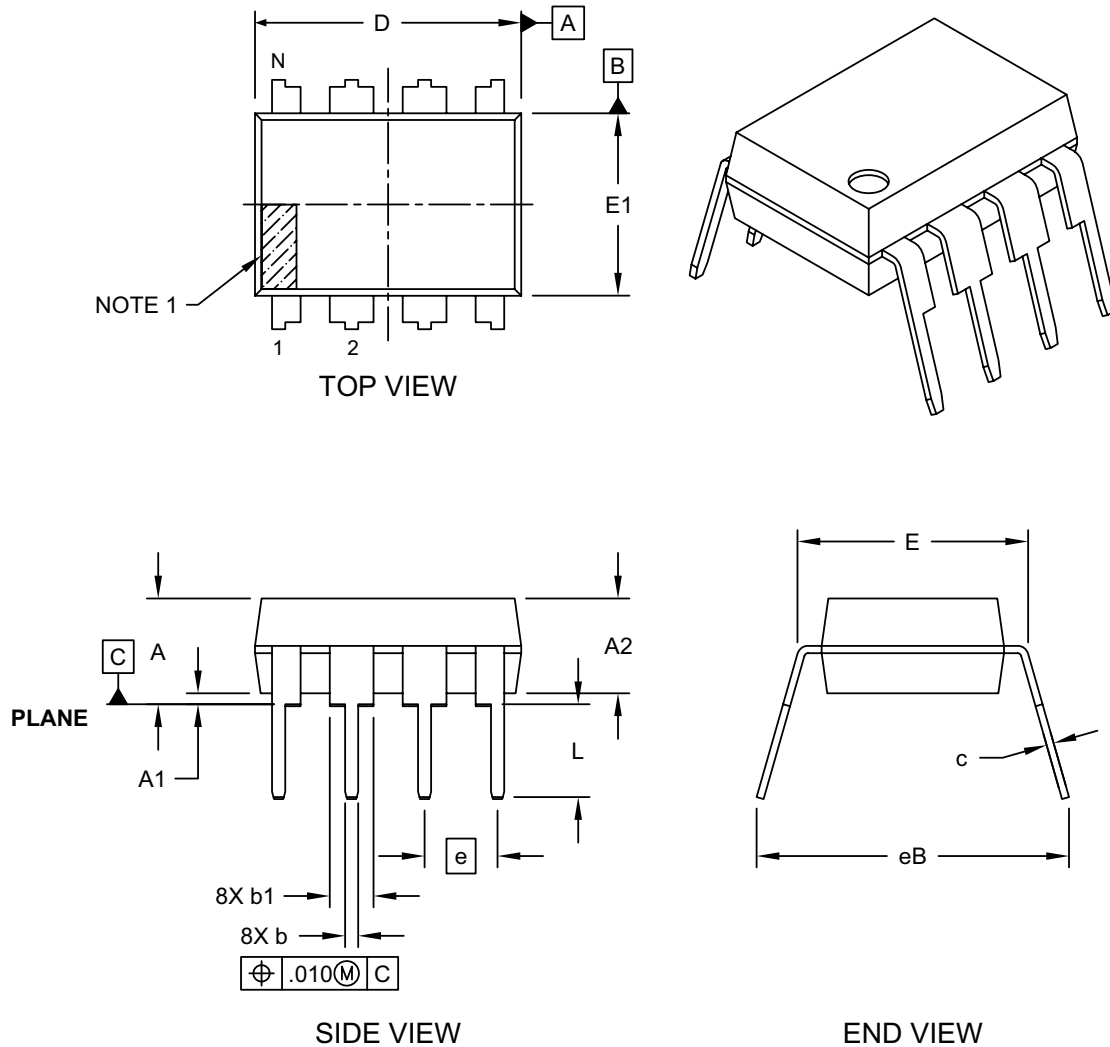
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

25AA040A/25LC040A

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



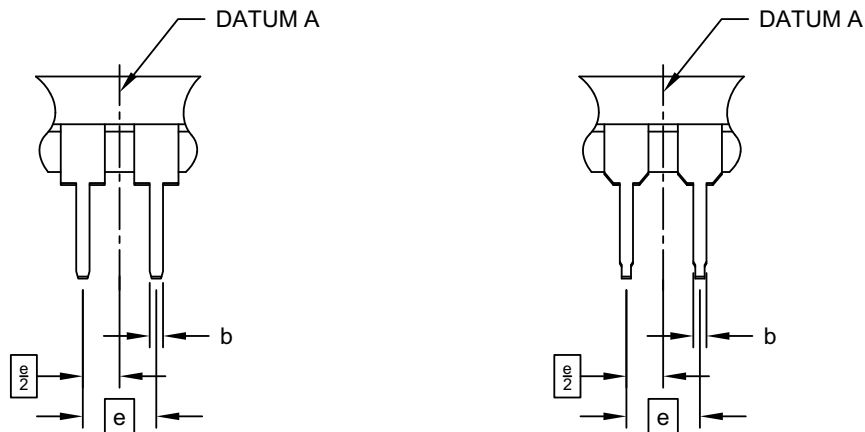
Microchip Technology Drawing No. C04-018-P Rev E Sheet 1 of 2

25AA040A/25LC040A

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

ALTERNATE LEAD DESIGN (NOTE 5)



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing	§	eB	-	.430

Notes:

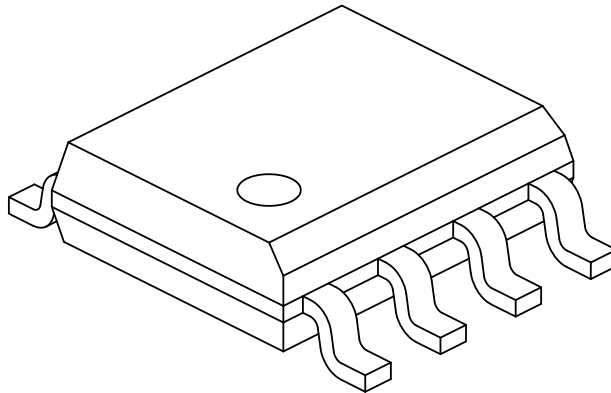
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev E Sheet 2 of 2

25AA040A/25LC040A

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

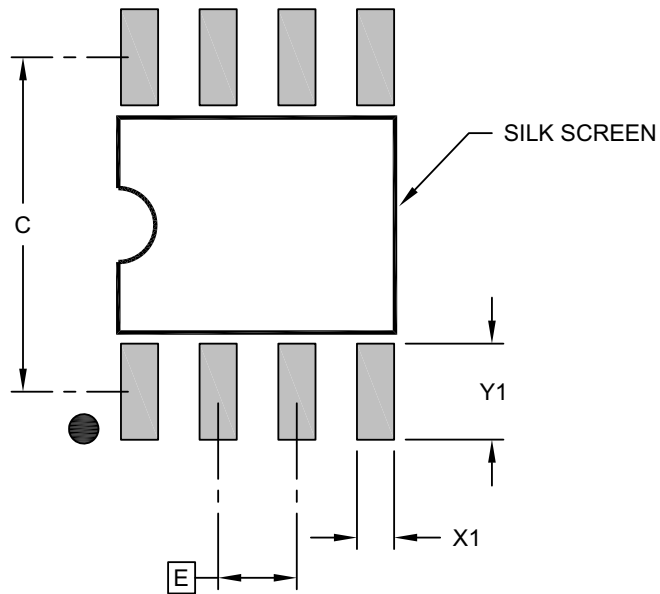
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev F Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

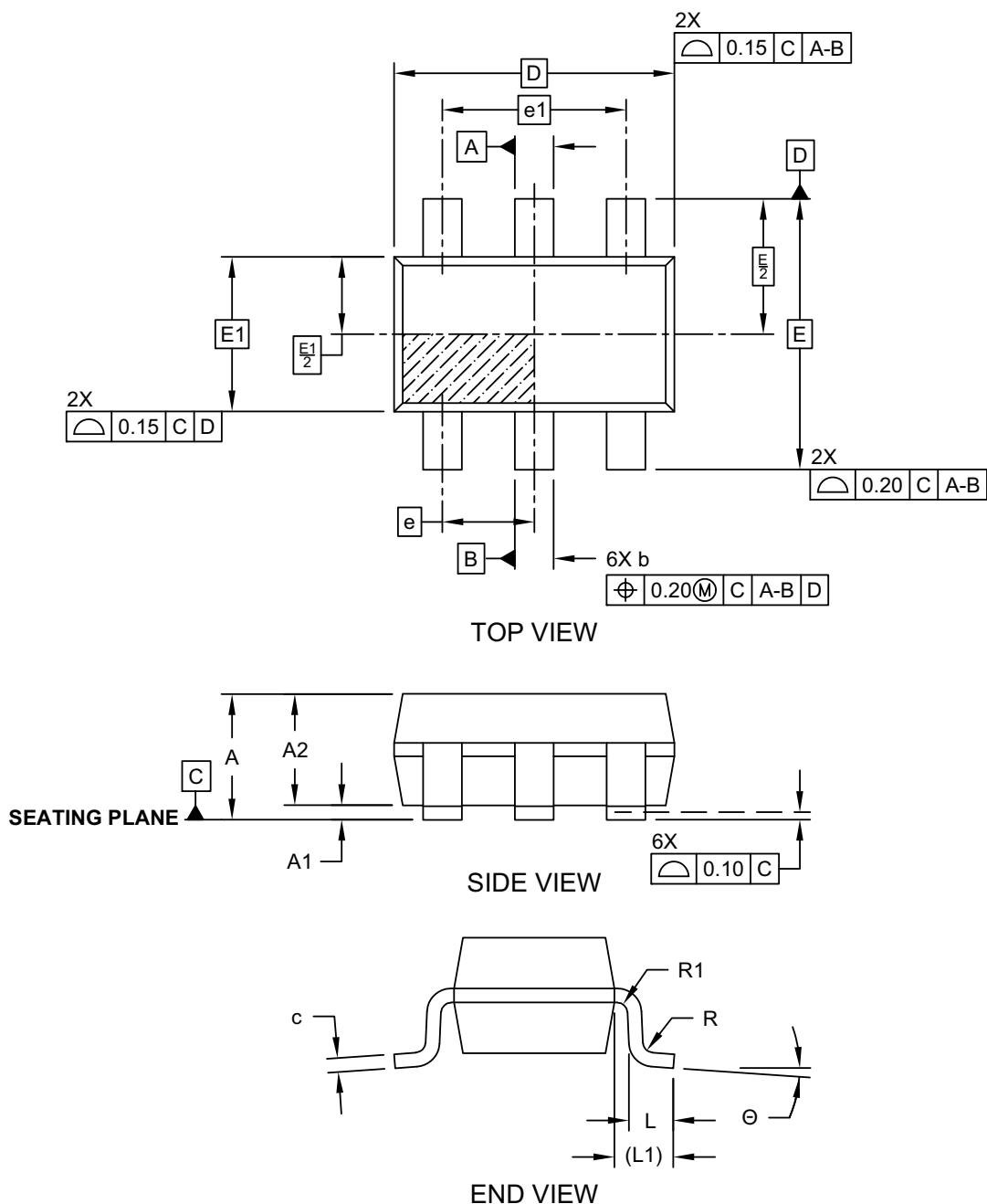
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev F

25AA040A/25LC040A

6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

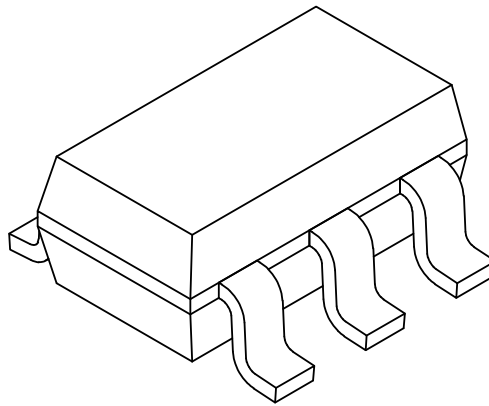
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-028D (OT) Sheet 1 of 2

6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	6		
Pitch	e	0.95 BSC		
Outside lead pitch	e1	1.90 BSC		
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	1.15	1.30
Standoff	A1	0.00	-	0.15
Overall Width	E	2.80 BSC		
Molded Package Width	E1	1.60 BSC		
Overall Length	D	2.90 BSC		
Foot Length	L	0.30	0.45	0.60
Footprint	L1	0.60 REF		
Foot Angle	ϕ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

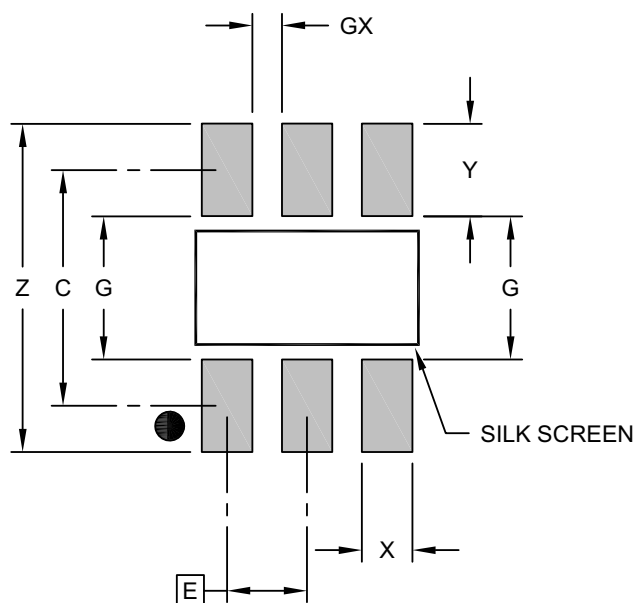
Notes:

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-028D (OT) Sheet 2 of 2

6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X3)	X			0.60
Contact Pad Length (X3)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

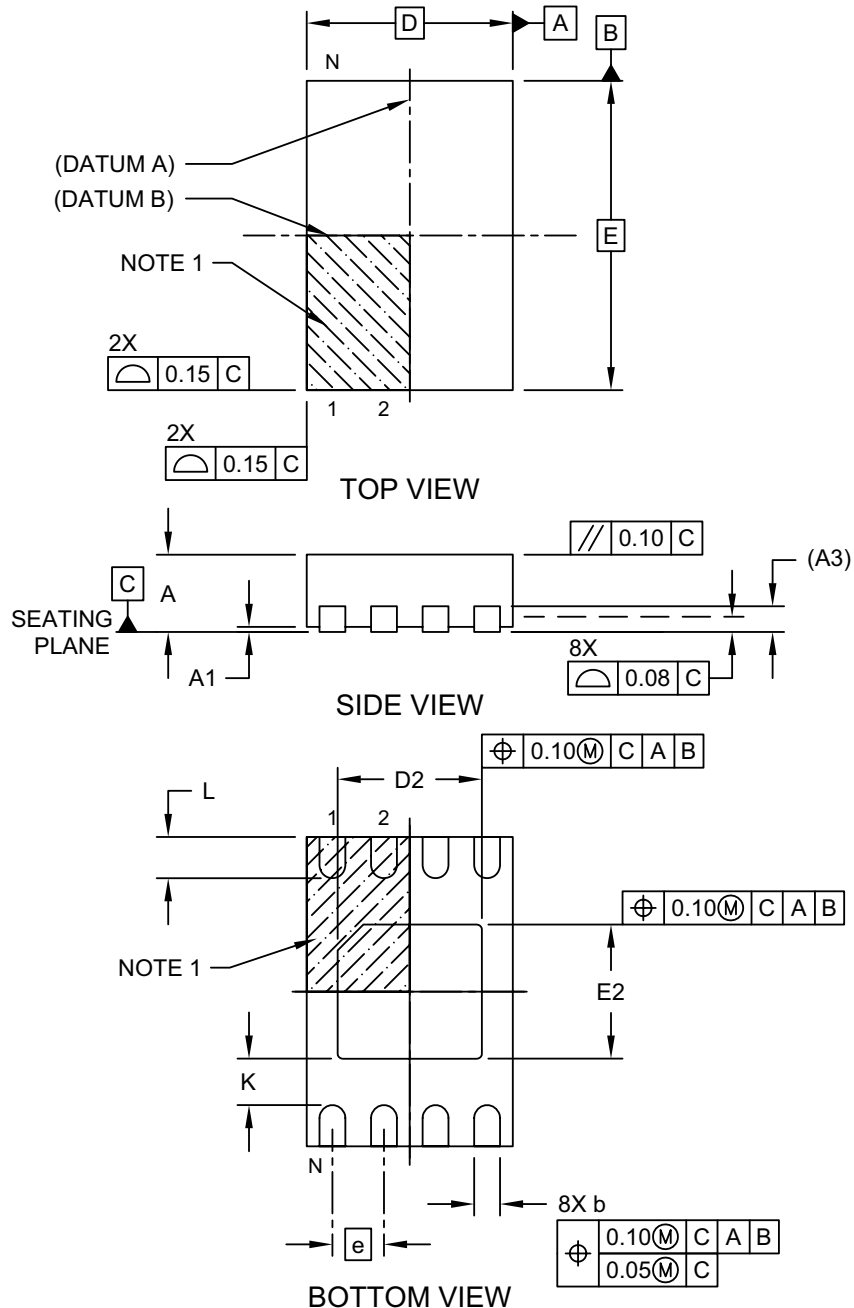
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028D (OT)

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

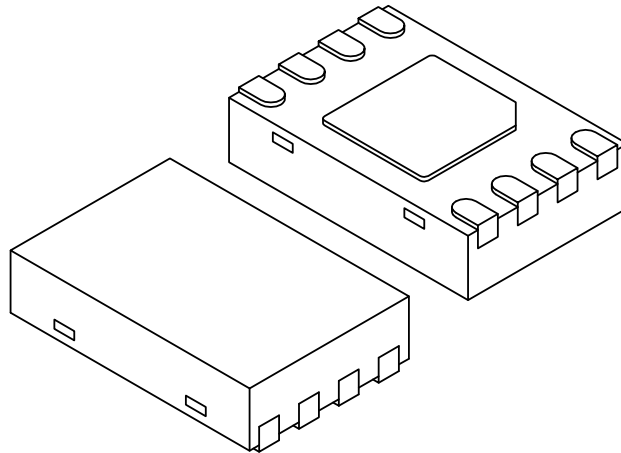


Microchip Technology Drawing No. C04-129-MN Rev E Sheet 1 of 2

25AA040A/25LC040A

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	2.00 BSC		
Overall Width	E	3.00 BSC		
Exposed Pad Length	D2	1.35	1.40	1.45
Exposed Pad Width	E2	1.25	1.30	1.35
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

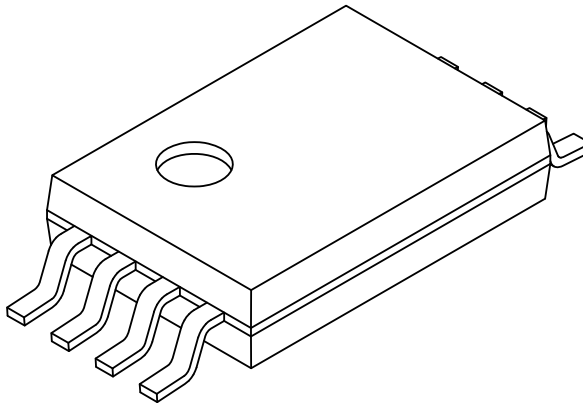
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129-MN Rev E Sheet 2 of 2

25AA040A/25LC040A

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		8		
Pitch	e		0.65 BSC		
Overall Height	A		-	-	1.20
Molded Package Thickness	A2		0.80	1.00	1.05
Standoff	A1		0.05	-	-
Overall Width	E		6.40 BSC		
Molded Package Width	E1		4.30	4.40	4.50
Overall Length	D		2.90	3.00	3.10
Foot Length	L		0.45	0.60	0.75
Footprint	L1		1.00 REF		
Lead Thickness	c		0.09	-	0.25
Foot Angle	φ		0°	4°	8°
Lead Width	b		0.19	-	0.30

Notes:

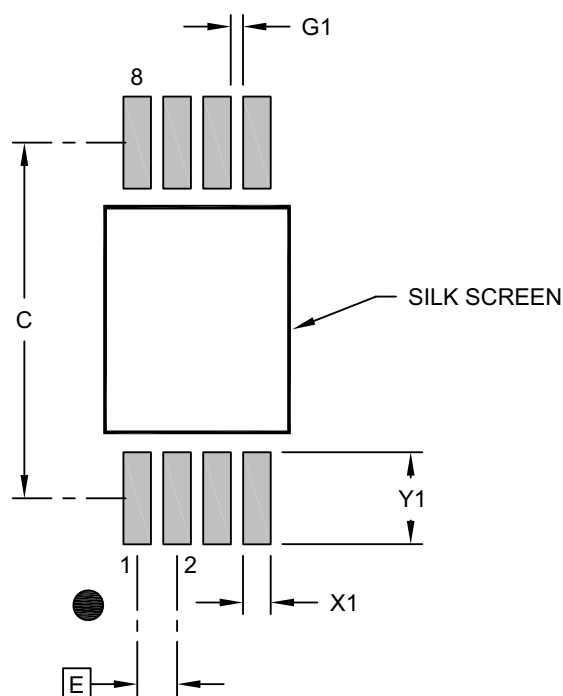
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086 Rev C Sheet 2 of 2

25AA040A/25LC040A

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.80	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.50
Contact Pad to Center Pad (X6)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2086 Rev B

APPENDIX A: REVISION HISTORY

Revision J (12/2021)

Added Product Identification System section for Automotive; Updated DFN, PDIP, SOIC, SOT23, TDFN and TSSOP package drawings; Replaced terminology “Master” and “Slave” with “Host” and “Client”, respectively; Replaced “Automotive (E):” designation with “Extended (E):” designation; Reformatted some sections for better readability.

Revision H (12/2012)

Revised Table 1-2, Param. 21.

Revision G (11/2011)

Added TDFN Package.

Revision F (7/2009)

Replaced 6-Lead SOT-23 package drawing (from CH to OT); Revised 8-Lead DFN (MC); Added 8-Lead DFN (MC) Land Pattern.

Revision E (10/2007)

Revised Features (Pb-free); Replaced Package Drawings.

Revision D (5/2007)

Removed Preliminary status; Replaced package drawings (Rev. AP); Revise Table 1-1, Param. D004, D007, D008; Revise Table 1-2, Param. 7, 8, 9, 10.

Revision C (2/2006)

Added Packages SOT-23, DFN and X-rotated TSSOP; Revised AC Char., Params. 9, 10; Revised Package Legend.

Revision B (12/2003)

Corrections to Section 1.0, Electrical Characteristics

Revision A (9/2003)

Initial Release.

THE MICROCHIP WEBSITE

Microchip provides online support via our website at www.microchip.com. This website is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the website contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip website at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the website at: <http://microchip.com/support>

25AA040A/25LC040A

PRODUCT IDENTIFICATION SYSTEM (NON-AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.		X ⁽¹⁾	-X	XX	Examples
Device		Tape and Reel Option	Temperature Range	Package	
Device:	25AA040A	=	4-Kbit, 1.8V, 16-Byte Page SPI Serial EEPROM		a) 25AA040A-I/MS: 4-Kbit, 1.8V Serial EEPROM, Industrial temp., MSOP package.
	25AA040AX	=	4-Kbit, 1.8V, 16-Byte Page SPI Serial EEPROM, in alternate pinout (ST only)		b) 25AA040AT-I/SN: 4-Kbit, 1.8V Serial EEPROM, Tape and Reel, Industrial temp., SOIC package.
	25LC040A	=	4-Kbit, 2.5V, 16-Byte Page SPI Serial EEPROM		c) 25LC040AT-I/SN: 4-Kbit, 2.5V Serial EEPROM, Tape and Reel, Industrial temp., SOIC package.
	25LC040AX	=	4-Kbit, 2.5V, 16-Byte Page SPI Serial EEPROM, in alternate pinout (ST only)		d) 25LC040AT-I/ST: 4-Kbit, 2.5V Serial EEPROM, Tape and Reel, Industrial temp., TSSOP package.
Tape and Reel Option:	Blank	=	Standard packaging (tube)		e) 25LC040AT-E/SN: 4-Kbit, 2.5V Serial EEPROM, Tape and Reel, Extended temp., SOIC package.
	T	=	Tape and Reel ⁽¹⁾		f) 25LC040AX-E/ST: 4-Kbit, 2.5V Serial EEPROM, Rotated pinout, Extended temp., TSSOP package.
Temperature Range:	I	=	-40°C to +85°C (Industrial)		g) 25LC040AT-I/MNY: 4-Kbit, 2.5V Serial EEPROM, Tape and Reel, Industrial temp., TDFN package.
	E	=	-40°C to +125°C (Extended)		
Package:	MC	=	Plastic Dual Flat, No Lead – 2x3x1 mm Body 8-Lead (DFN)		
	MS	=	Plastic Micro Small Outline – 8-Lead (MSOP)		
	P	=	Plastic Dual In-Line – 300 mil Body, 8-Lead (PDIP)		
	OT	=	Plastic Small Outline Transistor – 6-Lead (SOT-23)		
	SN	=	Plastic Small Outline - Narrow, 3.90 mm (.150 In) Body, 8-Lead (SOIC)		
	MNY ⁽²⁾	=	Plastic Dual Flat, No Lead Package – 2x3x0.8 mm Body, 8-Lead (TDFN)		
	ST	=	Plastic Thin Shrink Small Outline – 4x4 mm Body, 8-Lead (TSSOP)		

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: “Y” indicates a Nickel Palladium Gold (NiPdAu) finish.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: "Y" indicates a Nickel Palladium Gold (NiPdAu) finish.

25AA040A/25LC040A

PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>		<u>X</u> ⁽¹⁾	<u>-X</u>	<u>/XX</u>	<u>XXX</u> ^(2,3)	Examples
Device	Tape and Reel Option	Temperature Range	Package	Variant		
<div></div>						
Device:	25AA040A	=	4-Kbit, 1.8V, 16-Byte Page SPI Serial EEPROM			a) 25LC040AT-I/SN16KVAO: 4-Kbit, 2.5V Serial EEPROM, Tape and Reel, Automotive Grade 3, SOIC package.
	25LC040A	=	4-Kbit, 2.5V, 16-Byte Page SPI Serial EEPROM			b) 25LC040A-E/SN16KVAO: 4-Kbit, 1.8V Serial EEPROM, Automotive Grade 1, SOIC package.
Tape and Reel Option:	Blank	=	Standard packaging (tube)			c) 25LC040A-E/ST16KVAO: 4-Kbit, 2.5V, Serial EEPROM, Automotive Grade 1, TSSOP package.
	T	=	Tape and Reel			d) 25LC040AT-E/SN16KVAO: 4-Kbit, 2.5V, Serial EEPROM, Tape and Reel, Automotive Grade 1, SOIC package.
Temperature Range:	I	=	-40°C to +85°C ⁽¹⁾ (AEC-Q100 Grade 3)			e) 25LC040AT-E/ST16KVAO: 4-Kbit, 2.5V, Serial EEPROM, Tape and Reel, Automotive Grade 1, TSSOP package.
	E	=	-40°C to +125°C (AEC-Q100 Grade 1)			f) 25LC040AT-E/MS16KVAO: 4-Kbit, 2.5V Serial EEPROM, Tape and Reel, Automotive Grade 1, MSOP package.
Package:	MS	=	Plastic Micro Small Outline – 8-Lead (MSOP)			g) 25LC040AT-E/OT16KVAO: 4-Kbit, 2.5V Serial EEPROM, Tape and Reel, Automotive Grade 1, SOT-23 package.
	OT	=	Plastic Small Outline Transistor – 6-Lead (SOT-23)			
	SN	=	Plastic Small Outline - Narrow, 3.90 mm (.150 In) Body, 8-Lead (SOIC)			
	ST	=	Plastic Thin Shrink Small Outline – 4x4 mm Body, 8-Lead (TSSOP)			
Variant: ^(2,3)	16KVAO	=	Standard Automotive, 16K Process			Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
	16KVXX	=	Customer-Specific Automotive, 16K Process			
3: For customers requesting a PPAP, a customer-specific part number will be generated and provided. A PPAP is not provided for VAO part numbers.						

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
 - Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
 - Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
 - Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.
-

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at <https://www.microchip.com/en-us/support/design-help/client-support-services>.

THIS INFORMATION IS PROVIDED BY MICROCHIP “AS IS”. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP’S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

For information regarding Microchip’s Quality Management Systems, please visit www.microchip.com/quality.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AnyRate, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Klear, LANCheck, LinkMD, maxStylus, maxTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzr, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, IntelliMOS, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, QuietWire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, TrueTime, WinPath, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, GridTime, IdealBridge, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, NVm Express, NVMe, Omniscent Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQL, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, TSHARC, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, Symmcom, and Trusted Time are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2003-2022, Microchip Technology Incorporated and its subsidiaries.

All Rights Reserved.

ISBN: 978-1-5224-9452-2

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880-3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Microchip:](#)

[25LC040A-H/SN](#) [25LC040AT-H/SN](#) [25AA040A-I/MS](#) [25AA040A-I/P](#) [25AA040A-I/SN](#) [25AA040A-I/ST](#) [25AA040AT-I/MC](#) [25AA040AT-I/MS](#) [25AA040AT-I/OT](#) [25AA040AT-I/SN](#) [25AA040AT-I/ST](#) [25AA040AX-I/ST](#) [25AA040AXT-I/ST](#) [25LC040A-E/MS](#) [25LC040A-E/P](#) [25LC040A-E/SN](#) [25LC040A-E/ST](#) [25LC040A-I/MS](#) [25LC040A-I/P](#) [25LC040A-I/SN](#) [25LC040A-I/ST](#) [25LC040AT-E/MC](#) [25LC040AT-E/MS](#) [25LC040AT-E/OT](#) [25LC040AT-E/SN](#) [25LC040AT-E/ST](#) [25LC040AT-I/MC](#) [25LC040AT-I/MS](#) [25LC040AT-I/OT](#) [25LC040AT-I/SN](#) [25LC040AT-I/ST](#) [25LC040AX-E/ST](#) [25LC040AX-I/ST](#) [25LC040AXT-E/ST](#) [25LC040AXT-I/ST](#) [25AA040AT-I/MNY](#) [25LC040AT-E/MNY](#) [25LC040AT-I/MNY](#) [25AA040A/S16K](#) [25AA040A/W16K](#) [25AA040A/WF16K](#) [25LC040A/S16K](#) [25LC040A/W16K](#) [25LC040A/WF16K](#)