24AA08H/24LC08BH

8K I^{2}C Serial EEPROM with Half-Array Write-Protect

Device Selection Table

Part Number	Vcc Range	Max. Clock Frequency	Temp. Ranges	Available Packages
24AA08H	1.7V-5.5V	400 kHz[1]	I	MS, P, SN, OT, MNY, ST
24LC08BH	2.5V-5.5V	400 kHz	I, E	MS, P, SN, OT, MNY, ST

Note 1: 100 kHz for V$_{CC}$ < 2.5V

Features

- Single Supply with Operation Down to 1.7V for 24AA08H Devices, 2.5V for 24LC08BH Devices
- Low-Power CMOS Technology:
  - Read current 1 mA, maximum
  - Standby current 1 µA, maximum (I-temp.)
- Two-Wire Serial Interface, I^{2}C Compatible
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kHz and 400 kHz Clock Compatibility
- Page Write Time: 5 ms, Maximum
- Self-Timed Erase/Write Cycle
- 16-Byte Page Write Buffer
- Hardware Write-Protect for Half-Array (200h-3FFh)
- ESD Protection >4,000V
- More than 1 Million Erase/Write Cycles
- Data Retention >200 Years
- Factory Programming Available
- RoHS Compliant
- Temperature Ranges:
  - Industrial (I):   -40°C to +85°C
  - Extended (E):   -40°C to +125°C
- Automotive AEC-Q100 Qualified

Packages

- 8-Lead MSOP, 8-Lead PDIP, 8-Lead SOIC, 5-Lead SOT-23, 8-Lead TDFN and 8-Lead TSSOP
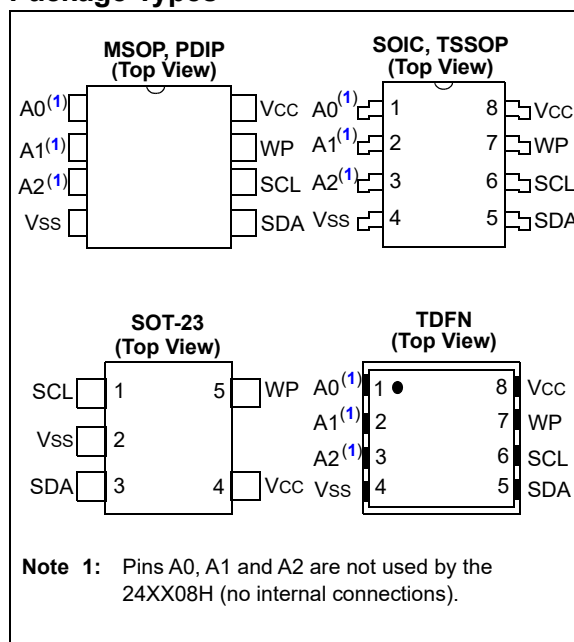
Description

The Microchip Technology Inc. 24XX08H[1] is an 8-Kbit Electrically Erasable PROM (EEPROM). The device is organized as one block of 1024 x 8-bit memory with a two-wire serial interface.

Its low-voltage design permits operation down to 1.7V, with standby and active currents of only 1 µA and 1 mA, respectively. The 24XX08H also has a page write capability for up to 16 bytes of data.

Note 1: 24XX08H is used in this document as a generic part number for the 24AA08H/24LC08BH devices.

Package Types

Note 1: Pins A0, A1 and A2 are not used by the 24XX08H (no internal connections).

24AA08H/24LC08BH

Block Diagram

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [†]

V_{CC}...6.5V

All inputs and outputs w.r.t. V_{SS} ....-0.3V to V_{CC} +1.0V

Storage temperature ....-65°C to +150°C

Ambient temperature with power applied..-40°C to +125°C

ESD protection on all pins ....$\geq$ 4 kV

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† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial (I): T_A = -40°C to +85°C, V_{CC} = +1.7V to +5.5V Extended (E): T_A = -40°C to +125°C, V_{CC} = +1.7V to +5.5V				
Param. No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
D1	V_{IH}	High-Level Input Voltage	0.7 V_{CC}	—	—	V	
D2	V_{IL}	Low-Level Input Voltage	—	—	0.3 V_{CC}	V	
D3	V_{HYS}	Hysteresis of Schmitt Trigger Inputs	0.05 V_{CC}	—	—	V	**Note 1**
D4	V_{OL}	Low-Level Output Voltage	—	—	0.40	V	I_{OL} = 3.0 mA, V_{CC} = 2.5V
D5	I_{LI}	Input Leakage Current	—	—	±1	µA	V_{IN} = V_{SS} to V_{CC}
D6	I_{LO}	Output Leakage Current	—	—	±1	µA	V_{OUT} = V_{SS} to V_{CC}
D7	C_{IN}, C_{OUT}	Pin Capacitance (all inputs/outputs)	—	—	10	pF	V_{CC} = 5.0V (**Note 1**) T_A = +25°C, F_{CLK} = 1 MHz
D8	$I_{CCWRITE}$	Operating Current	—	0.1	3	mA	V_{CC} = 5.5V, SCL = 400 kHz
D9	I_{CCREAD}		—	0.05	1	mA	
D10	I_{CCS}	Standby Current	—	0.01	1	µA	SDA = SCL = V_{CC} WP = V_{SS}, I-Temp.
			—	—	5	µA	SDA = SCL = V_{CC} WP = V_{SS}, E-Temp.

Note 1: This parameter is periodically sampled and not 100% tested.

24AA08H/24LC08BH

TABLE 1-2: AC CHARACTERISTICS

| AC CHARACTERISTICS						Industrial (I): T_A = -40°C to +85°C, V_{CC} = +1.7V to +5.5V Extended (E): T_A = -40°C to +125°C, V_{CC} = +2.5V to +5.5V
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Conditions
1	F_{CLK}	Clock Frequency	—	400	kHz	$2.5V \leq V_{CC} \leq 5.5V$
			—	100	kHz	$1.7V \leq V_{CC} < 2.5V$ (**24AA08H**)
2	T_{HIGH}	Clock High Time	600	—	ns	$2.5V \leq V_{CC} \leq 5.5V$
			4000	—	ns	$1.7V \leq V_{CC} < 2.5V$ (**24AA08H**)
3	T_{LOW}	Clock Low Time	1300	—	ns	$2.5V \leq V_{CC} \leq 5.5V$
			4700	—	ns	$1.7V \leq V_{CC} < 2.5V$ (**24AA08H**)
4	T_R	SDA and SCL Rise Time	—	300	ns	$2.5V \leq V_{CC} \leq 5.5V$ (**Note 1**)
			—	1000	ns	$1.7V \leq V_{CC} < 2.5V$ (**24AA08H**) (**Note 1**)
5	T_F	SDA and SCL Fall Time	—	300	ns	**Note 1**
6	$T_{HD:STA}$	Start Condition Hold Time	600	—	ns	$2.5V \leq V_{CC} \leq 5.5V$
			4000	—	ns	$1.7V \leq V_{CC} < 2.5V$ (**24AA08H**)
7	$T_{SU:STA}$	Start Condition Setup Time	600	—	ns	$2.5V \leq V_{CC} \leq 5.5V$
			4700	—	ns	$1.7V \leq V_{CC} < 2.5V$ (**24AA08H**)
8	$T_{HD:DAT}$	Data Input Hold Time	0	—	ns	**Note 2**
9	$T_{SU:DAT}$	Data Input Setup Time	100	—	ns	$2.5V \leq V_{CC} \leq 5.5V$
			250	—	ns	$1.7V \leq V_{CC} < 2.5V$ (**24AA08H**)
10	$T_{SU:STO}$	Stop Condition Setup Time	600	—	ns	$2.5V \leq V_{CC} \leq 5.5V$
			4000	—	ns	$1.7V \leq V_{CC} < 2.5V$ (**24AA08H**)
11	$T_{SU:WP}$	WP Setup Time	600	—	ns	$2.5V \leq V_{CC} \leq 5.5V$
			4000	—	ns	$1.7V \leq V_{CC} < 2.5V$ (**24AA08H**)
12	$T_{HD:WP}$	WP Hold Time	1300	—	ns	$2.5V \leq V_{CC} \leq 5.5V$
			4700	—	ns	$1.7V \leq V_{CC} < 2.5V$ (**24AA08H**)
13	T_{AA}	Output Valid from Clock	—	900	ns	$2.5V \leq V_{CC} \leq 5.5V$ (**Note 2**)
			—	3500	ns	$1.7V \leq V_{CC} < 2.5V$ (**24AA08H**) (**Note 2**)
14	T_{BUF}	Bus Free Time: The time the bus must be free before a new transmission can start	1300	—	ns	$2.5V \leq V_{CC} \leq 5.5V$
			4700	—	ns	$1.7V \leq V_{CC} < 2.5V$ (**24AA08H**)
15	T_{OF}	Output Fall Time from V_{IH} Minimum to V_{IL} Maximum	—	250	ns	$2.5V \leq V_{CC} \leq 5.5V$
			—	250	ns	$1.7V \leq V_{CC} < 2.5V$ (**24AA08H**)
16	T_{SP}	Input Filter Spike Suppression (SDA and SCL pins)	—	50	ns	**Notes 1** and **3**
17	T_{WC}	Write Cycle Time (byte or page)	—	5	ms	
18		Endurance	1,000,000	—	cycles	+25°C, V_{CC} = 5.5V, Page Mode (**Note 4**)

Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined T_{SP} and V_{HYS} specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a T_I specification for standard operation.

4: This parameter is not tested but ensured by characterization.

FIGURE 1-1:   BUS TIMING DATA
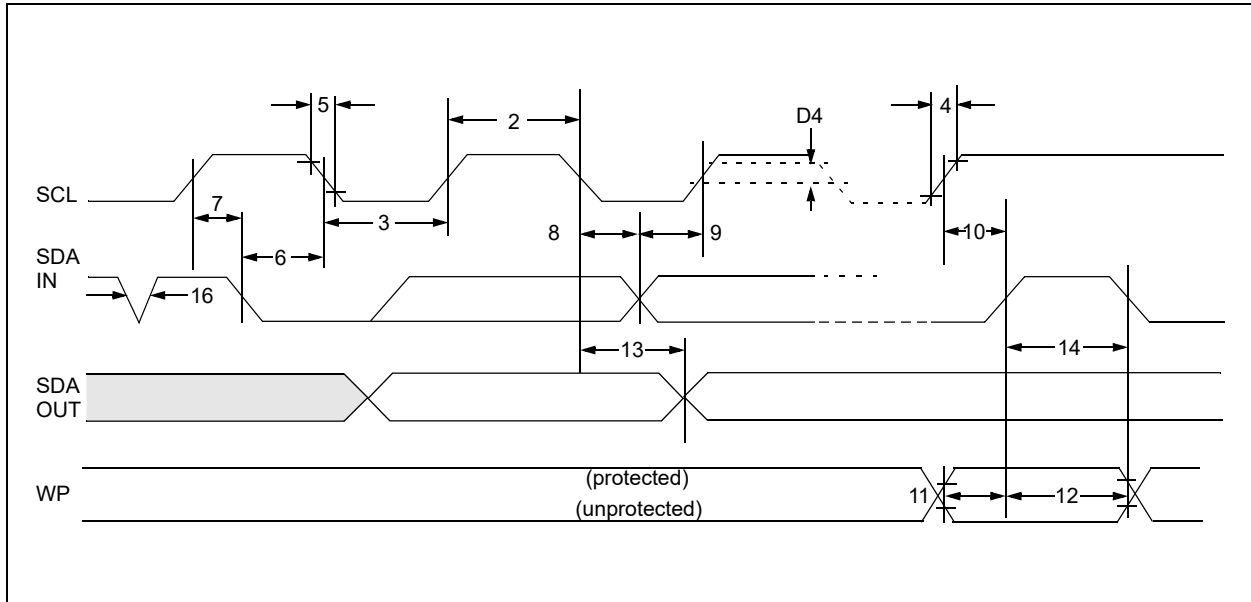
24AA08H/24LC08BH

2.0   PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1:   PIN FUNCTION TABLE

Name	MSOP	PDIP	SOIC	SOT23	TDFN[1]	TSSOP	Description
A0	1	1	1	—	1	1	Not Connected
A1	2	2	2	—	2	2	Not Connected
A2	3	3	3	—	3	3	Not Connected
Vss	4	4	4	2	4	4	Ground
SDA	5	5	5	3	5	5	Serial Address/Data I/O
SCL	6	6	6	1	6	6	Serial Clock
WP	7	7	7	5	7	7	Write-Protect Input
Vcc	8	8	8	4	8	8	Power Supply

Note 1:   The exposed pad on the TDFN package can be connected to Vss or left floating.

2.1   A0, A1, A2

The A0, A1 and A2 pins are not used by the 24XX08H. They may be left floating or tied to either Vss or Vcc.

2.2   Serial Address/Data Input/Output (SDA)

The SDA input is a bidirectional pin used to transfer addresses and data into and out of the device. Since it is an open-drain terminal, the SDA bus requires a pull-up resistor to Vcc (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating Start and Stop conditions.

2.3   Serial Clock (SCL)

The SCL input is used to synchronize the data transfer to and from the device.

2.4   Write-Protect (WP)

The WP pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000-03FF).

If tied to Vcc, write operations are inhibited, half of the memory will be write-protected (200h-3FFh). Read operations are not affected.

3.0 FUNCTIONAL DESCRIPTION

The 24XX08H supports a bidirectional, two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, while a device receiving data is defined as a receiver. The bus has to be controlled by a host device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24XX08H works as client. Both host and client can operate as transmitter or receiver, but the host device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus Not Busy (A)

Both data and clock lines remain high.

4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the host device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a First-In First-Out (FIFO) principle.

4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge after the reception of each byte. The host device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note:	The 24XX08H does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable-low during the high period of the Acknowledge-related clock pulse. Moreover, setup and hold times must be taken into account. During reads, a host must signal an end of data to the client by not generating an Acknowledge bit on the last byte that has been clocked out of the client. In this case, the client (24XX08H) will leave the data line high to enable the host to generate the Stop condition.

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS
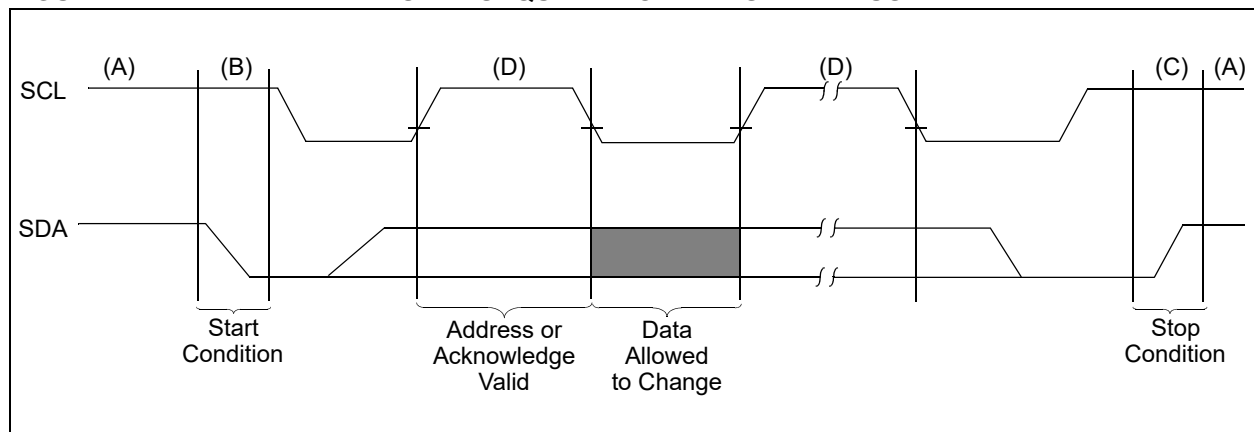
24AA08H/24LC08BH

5.0 DEVICE ADDRESSING

A control byte is the first byte received following the Start condition from the host device. The control byte consists of a four-bit control code. For the 24XX08H, this is set as '1010' binary for read and write operations. The next bit of the control byte is a "don't care" for the 24XX08H. The last two bits, B1 and B0, are used by the host device to select which of the four 256-word blocks of memory are to be accessed. These bits, in effect, are the Most Significant bits of the word address. The combination of the 4-bit control code and the next three bits are called the client address.

The last bit of the control byte is the Read/Write (R/$\overline{W}$) bit and it defines the operation to be performed. When set to '1', a read operation is selected. When set to '0', a write operation is selected. Following the Start condition, the 24XX08H monitors the SDA bus, checking the device type identifier being transmitted. Upon receiving a valid client address and the R/$\overline{W}$ bit, the client device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24XX08H will select a read or write operation.

The next byte received defines the address of the first data byte within the selected block (Figure 5-2). The word address byte uses all eight bits.

Operation	Control Code	Block Select	R/$\overline{W}$
Write	1010	Block Address	0

FIGURE 5-1:   CONTROL BYTE ALLOCATION

x = "don't care"
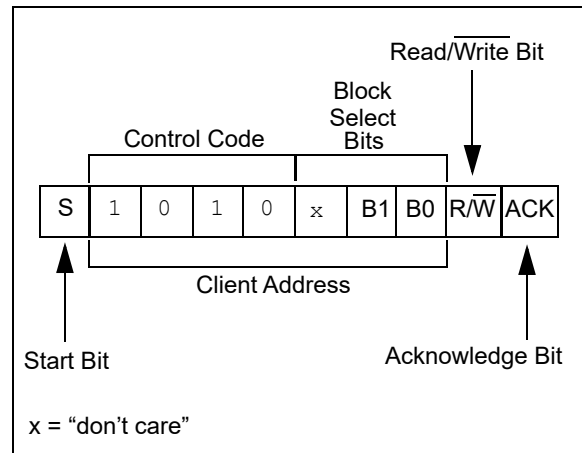
Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1

FIGURE 5-2:   ADDRESS SEQUENCE BIT ASSIGNMENTS

x = "don't care"
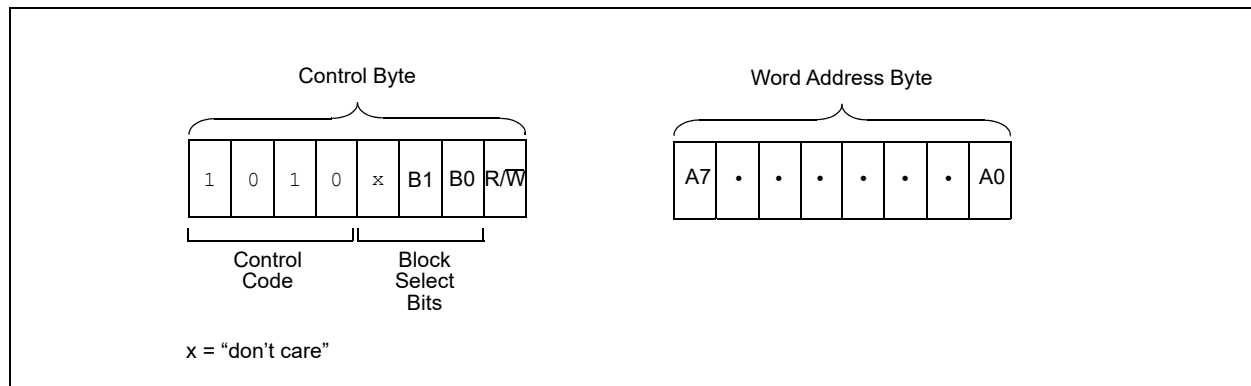
6.0 WRITE OPERATION

6.1 Byte Write

Following the Start condition from the host, the device code (4 bits), the block address (3 bits) and the R/$\overline{W}$ bit, which is a logic-low, are placed onto the bus by the host transmitter. This indicates to the addressed client receiver that a byte with a word address will follow once it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the host is the word address and will be written into the Address Pointer of the 24XX08H. After receiving another Acknowledge signal from the 24XX08H, the host device will transmit the data word to be written into the addressed memory location. The 24XX08H acknowledges again and the host generates a Stop condition. This initiates the internal write cycle and, during this time, the 24XX08H will not generate Acknowledge signals (Figure 6-1).

6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24XX08H in the same way as in a byte write. However, instead of generating a Stop condition, the host transmits up to 16 data bytes to the 24XX08H, which are temporarily stored in the on-chip page buffer and will be written into memory once the host has transmitted a Stop condition. Upon receipt of each word, the four lower-order Address Pointer bits, which form the byte counter, are internally incremented by one.

The higher-order four bits of the word address remain constant. If the host should transmit more than 16 words prior to generating the Stop condition, the Address Pointer will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-2).

> **Note:** Page write operations are limited to writing bytes within a single physical page **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of page size – 1. If a page write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

6.3 Write Protection

The WP pin allows the user to write-protect half of the array (200h-3FFh) when the pin is tied to V$_{CC}$. If the pin is tied to V$_{SS}$, the write protection is disabled.

FIGURE 6-1: BYTE WRITE
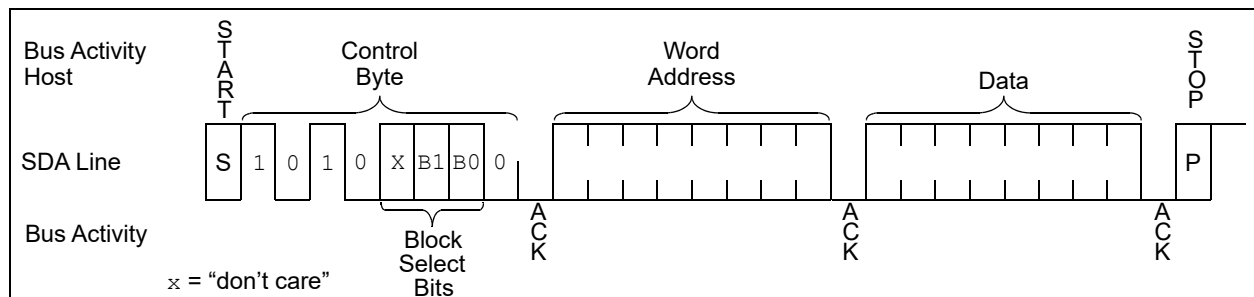
FIGURE 6-2: PAGE WRITE
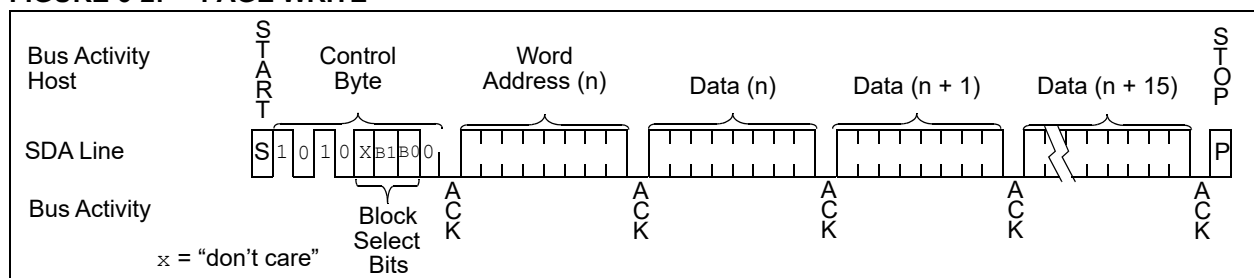
7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a write command has been issued from the host, the device initiates the internally-timed write cycle and ACK polling can then be initiated immediately. This involves the host sending a Start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, no ACK will be returned. If the cycle is complete, the device will return the ACK and the host can then proceed with the next read or write operation. See Figure 7-1 for a flow diagram of this operation.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW
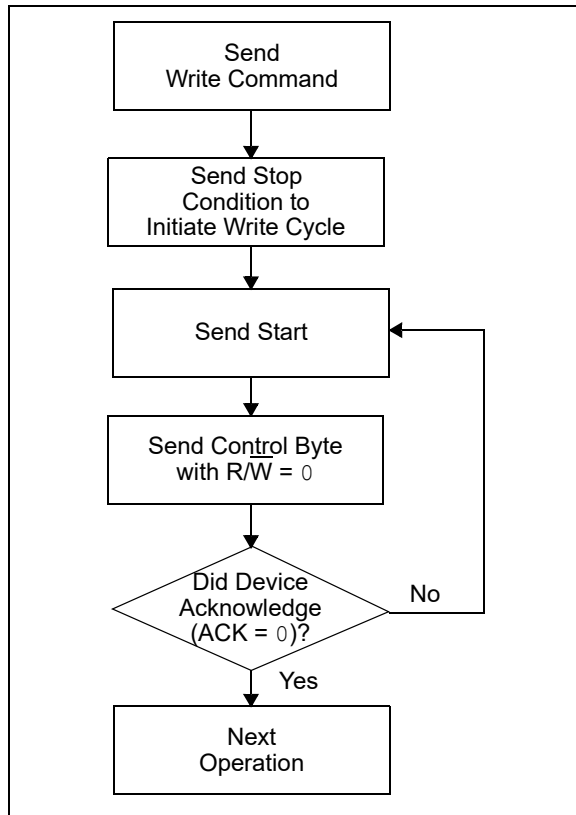
8.0 READ OPERATION

Read operations are initiated in the same way as write operations, with the exception that the R/$\overline{W}$ bit of the client address is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

8.1 Current Address Read

The 24XX08H contains an Address Pointer that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the client address with R/$\overline{W}$ bit set to '1', the 24XX08H issues an Acknowledge and transmits the 8-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition and the 24XX08H discontinues transmission (Figure 8-1).

8.2 Random Read

Random read operations allow the host to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is accomplished by sending the word address to the 24XX08H as part of a write operation. Once the word address is sent, the host generates a Start condition following the Acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The host then issues the control byte again, but with the R/$\overline{W}$ bit set to a '1'. The 24XX08H will then issue an Acknowledge and transmit the 8-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition and the 24XX08H will discontinue transmission (Figure 8-2).

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read, except that once the 24XX08H transmits the first data byte, the host issues an Acknowledge as opposed to a Stop condition in a random read. This directs the 24XX08H to transmit the next sequentially-addressed 8-bit word (Figure 8-3).

To provide sequential reads, the 24XX08H contains an internal Address Pointer that is incremented by one upon completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation.

8.4 Noise Protection

The SCL and SDA inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation, even on a noisy bus.

FIGURE 8-1:   CURRENT ADDRESS READ
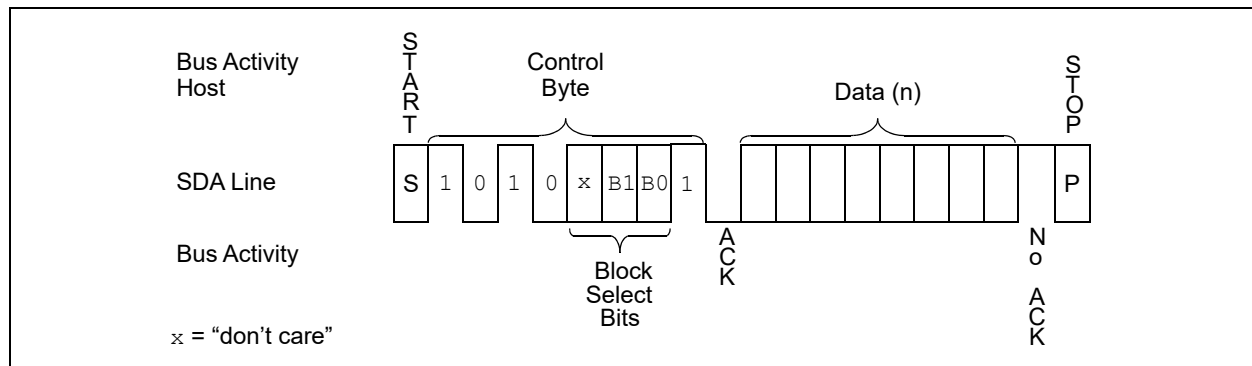
24AA08H/24LC08BH

FIGURE 8-2: **RANDOM READ**
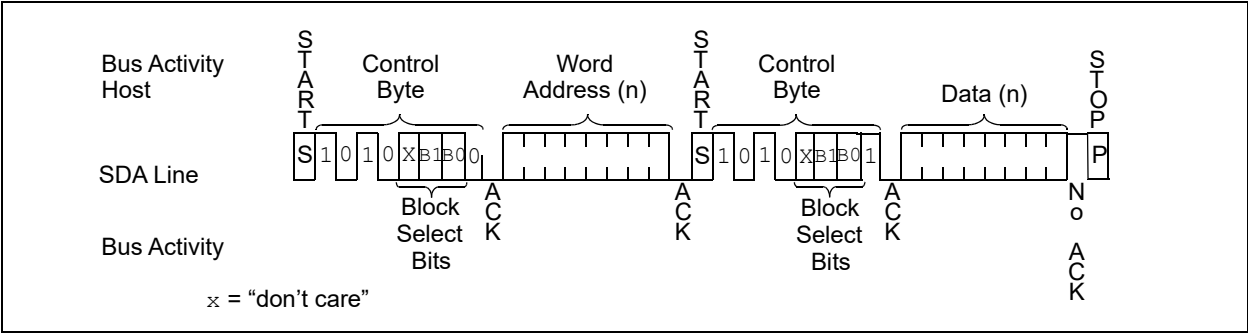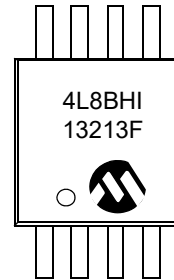

FIGURE 8-3: **SEQUENTIAL READ**
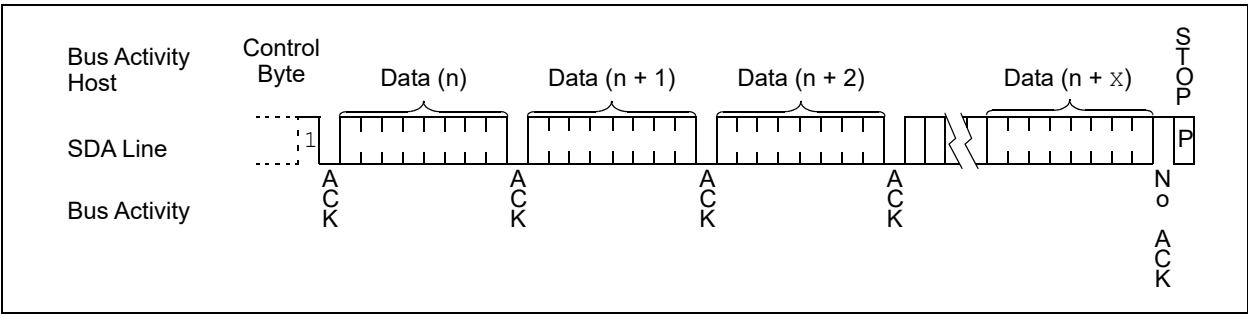
9.0   PACKAGING INFORMATION
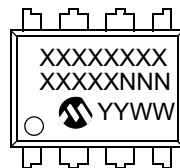
9.1   Package Marking Information

8-Lead MSOP
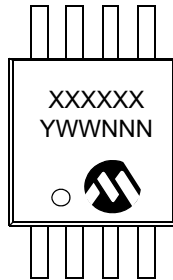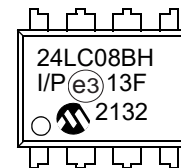
XXXXXX
YWWNNN

Example
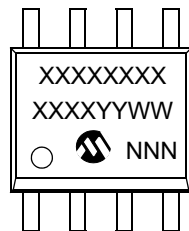
4L8BHI
13213F

8-Lead PDIP (300 mil)

XXXXXXXX
XXXXXNNN
YYWW

Example

24LC08BH
I/P (e3) 13F
2132

8-Lead SOIC (3.90 mm)

XXXXXXXX
XXXXXYYWW
NNN

Example

24LC08BHI
SN (e3) 2132
13F

5-Lead SOT-23

XXNN

Example

4QNN

8-Lead 2x3 TDFN

XXX
YWW
NN

Example

AS5
132
13

8-Lead TSSOP

XXXX
TYWW
NNN

Example

4L8H
I132
13F
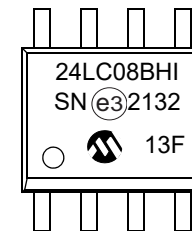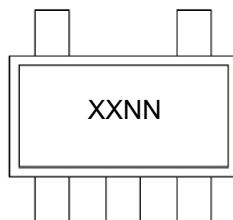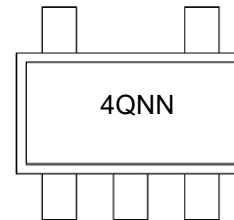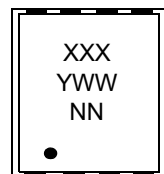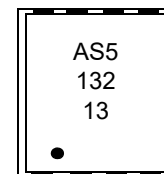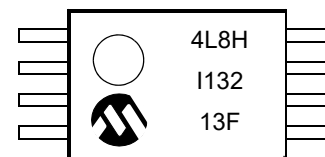
24AA08H/24LC08BH

Part Number	1st Line Marking Codes							
	MSOP	**PDIP**	**SOIC**	**TSSOP**	**SOT-23**		**TDFN**	
					I-Temp.	**E-Temp.**	**I-Temp.**	**E-Temp.**
24AA08H	4A8HT[1]	24AA08H	24AA08HT[1]	4A8H	4MNN[2]	—	AS1	—
24LC08BH	4L8BHT[1]	24L08BH	24LC08BHT[1]	4L8H	4QNN[2]	4RNN[2]	AS4	AS5

Note 1: T = Temperature grade (I, E)

2: NN = Alphanumeric traceability code

Legend: XX...X   Part number or part number code
   T   Temperature (I, E)
   Y   Year code (last digit of calendar year)
   YY   Year code (last 2 digits of calendar year)
   WW   Week code (week of January 1 is week '01')
   NNN   Alphanumeric traceability code (2 characters for small packages)
   (e3)   JEDEC® designator for Matte Tin (Sn)

* Standard OTP marking consists of Microchip part number, year code, week code and traceability code.

Note: For very small packages with no room for the JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

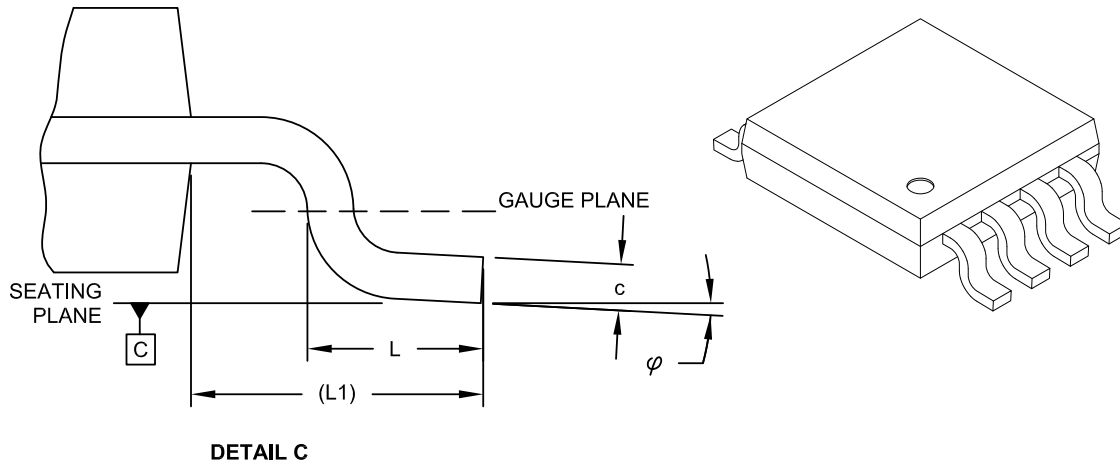**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TOP VIEW

SIDE VIEW

END VIEW

Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

GAUGE PLANE

SEATING PLANE

C

L

(L1)

c

φ

DETAIL C
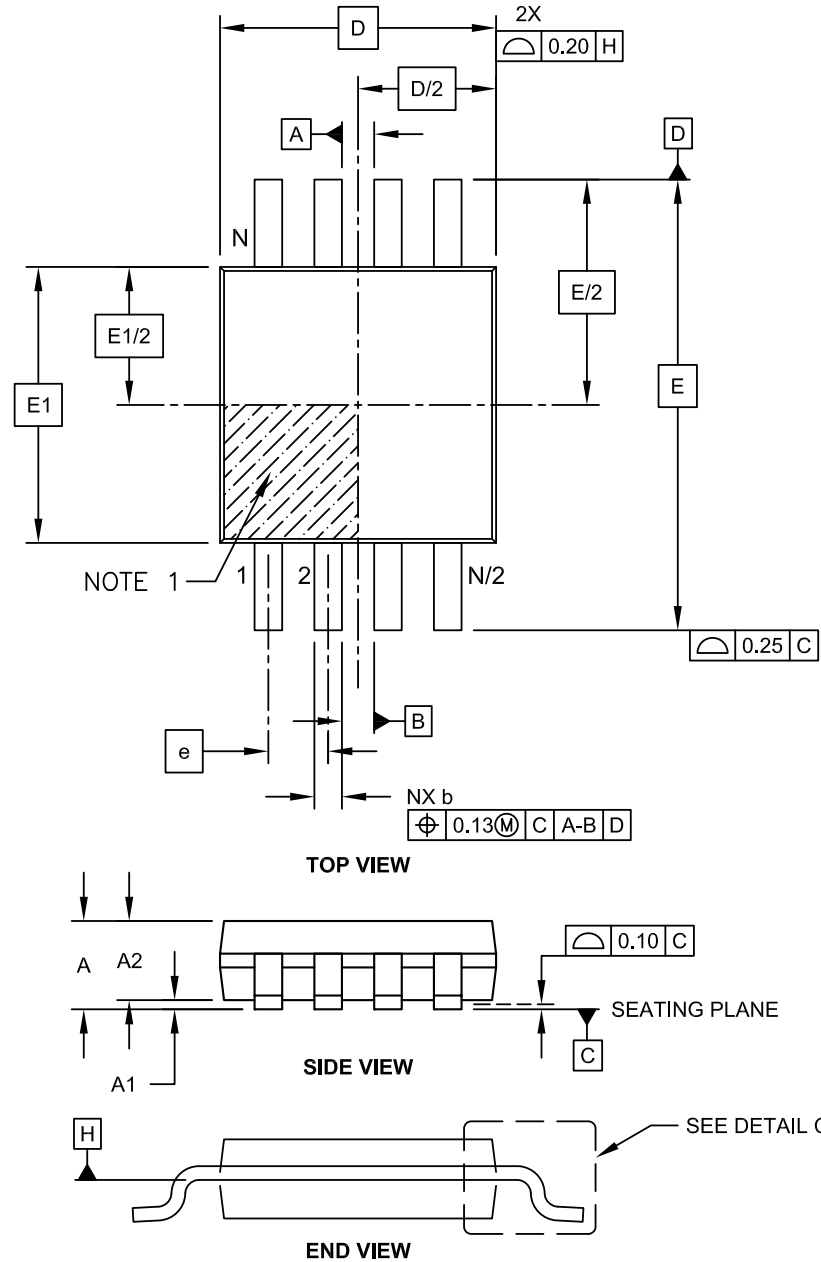
	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
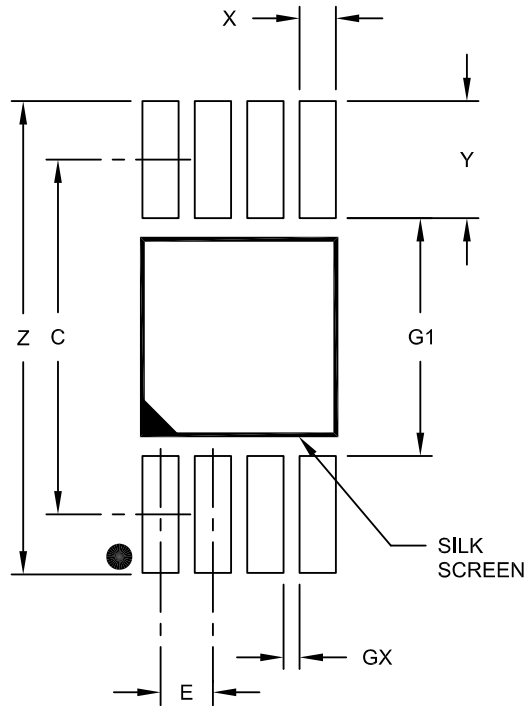
RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
    BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TOP VIEW

NOTE 1

N

D

A

B

E1

1   2

SIDE VIEW

PLANE

C   A

A1

A2

L

e

8X b1

8X b

⊕ | .010 Ⓜ | C

END VIEW

E

c

eB
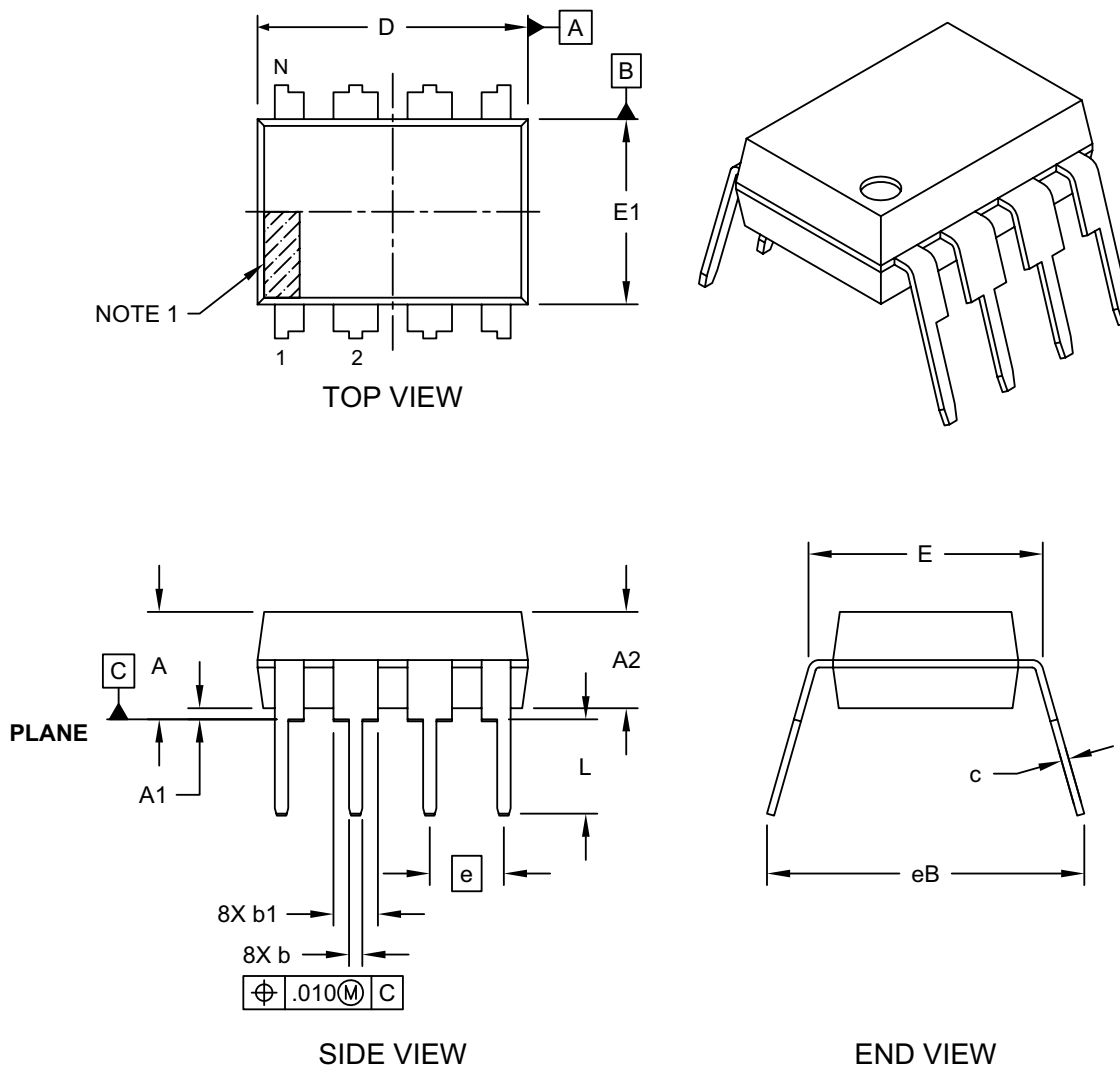
Microchip Technology Drawing No. C04-018-P Rev E Sheet 1 of 2

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

ALTERNATE LEAD DESIGN
(NOTE 5)
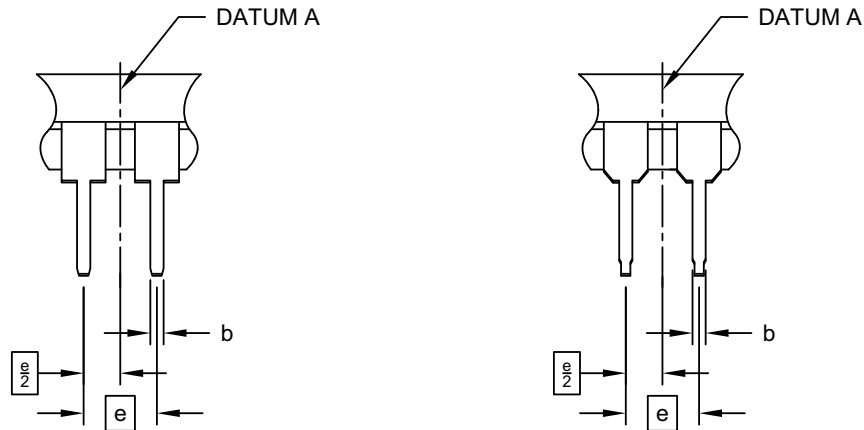
|	Units		INCHES		
Dimension Limits			MIN	NOM	MAX
Number of Pins		N		8	
Pitch		e		.100 BSC	
Top to Seating Plane		A	-	-	.210
Molded Package Thickness		A2	.115	.130	.195
Base to Seating Plane		A1	.015	-	-
Shoulder to Shoulder Width		E	.290	.310	.325
Molded Package Width		E1	.240	.250	.280
Overall Length		D	.348	.365	.400
Tip to Seating Plane		L	.115	.130	.150
Lead Thickness		c	.008	.010	.015
Upper Lead Width		b1	.040	.060	.070
Lower Lead Width		b	.014	.018	.022
Overall Row Spacing §		eB	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev E Sheet 2 of 2

24AA08H/24LC08BH

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TOP VIEW

SIDE VIEW

VIEW A–A

VIEW C
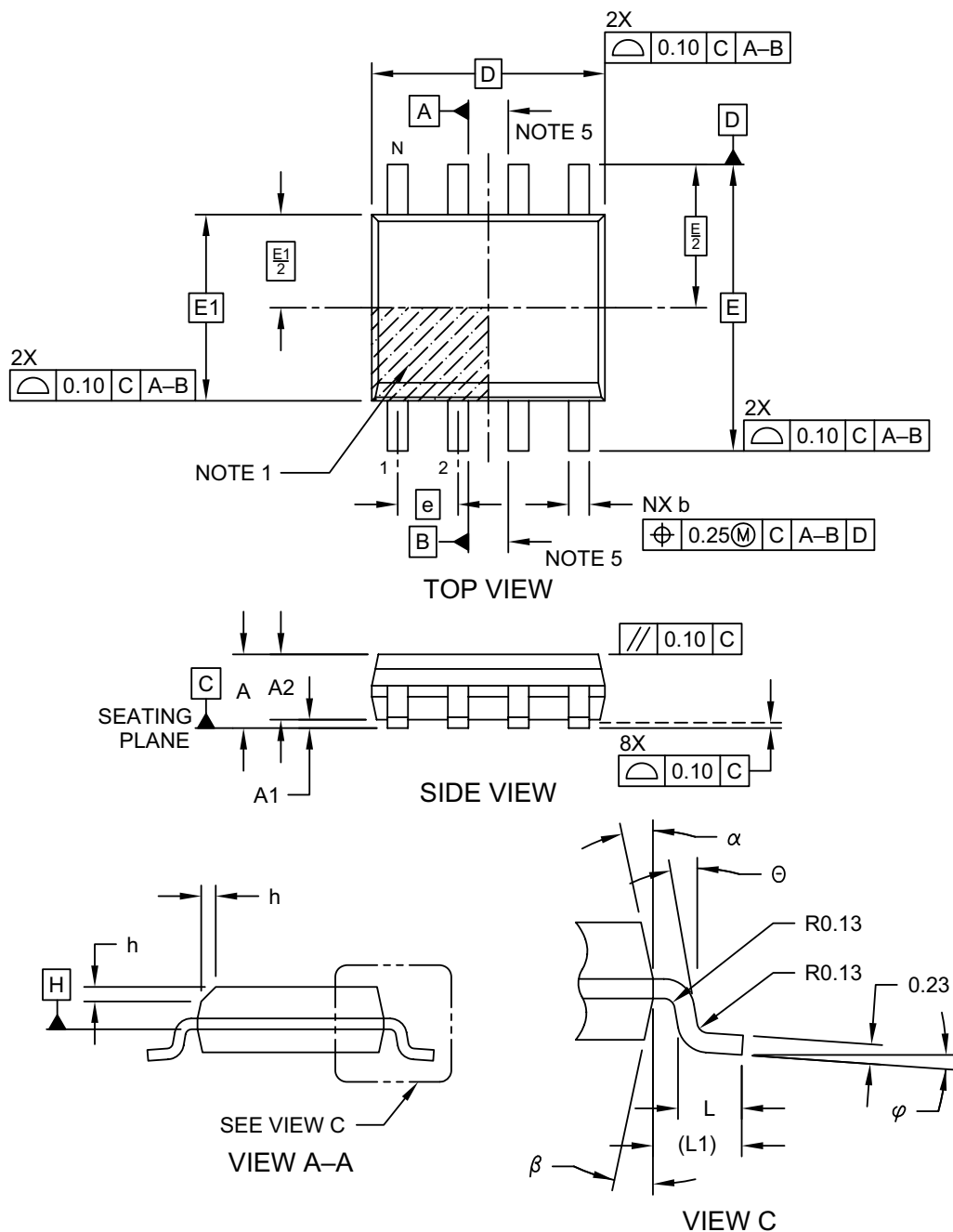
Microchip Technology Drawing No. C04-057-SN Rev F Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
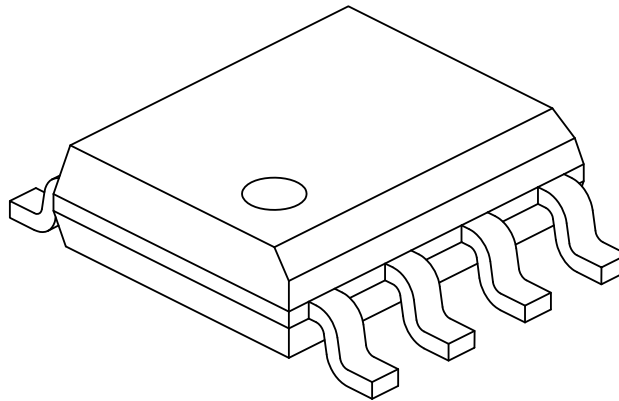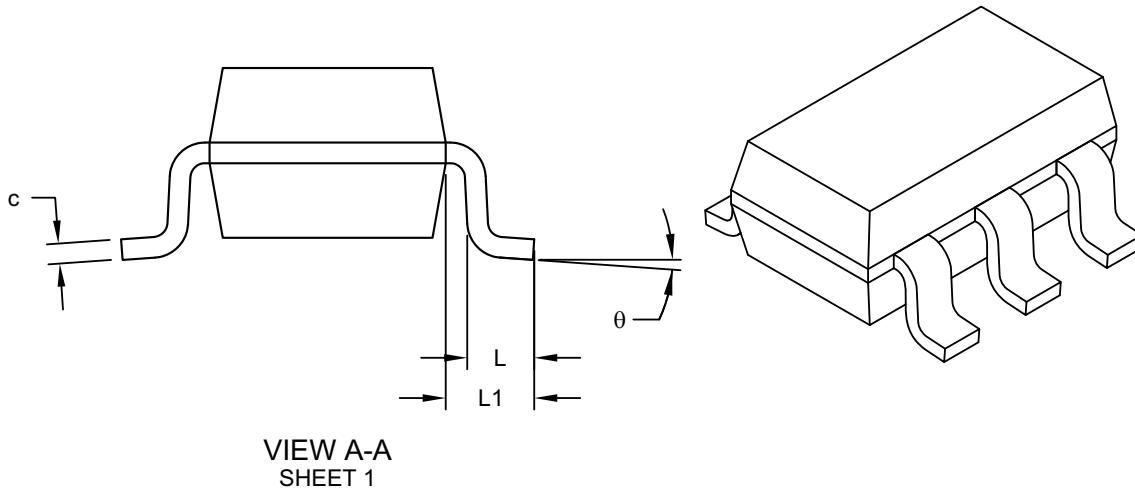

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

     BSC: Basic Dimension. Theoretically exact value shown without tolerances.
     REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev F Sheet 2 of 2

24AA08H/24LC08BH

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
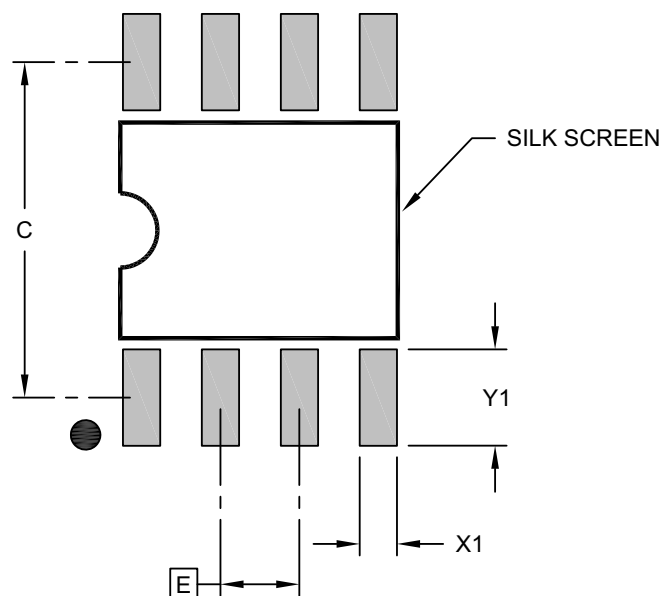
RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

 BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev F

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

> **Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TOP VIEW

SIDE VIEW
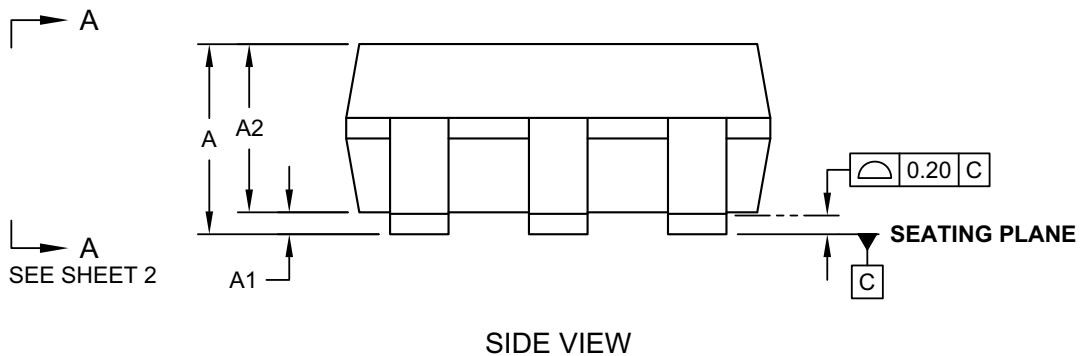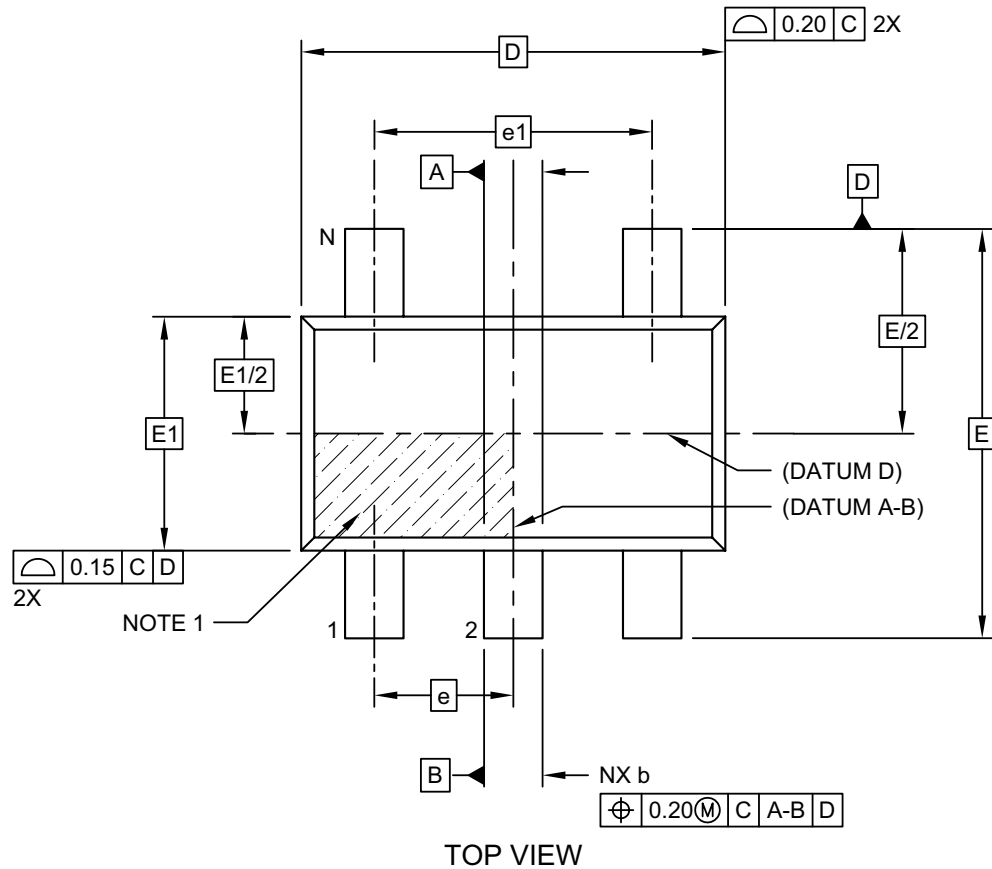
Microchip Technology Drawing C04-091-OT Rev F Sheet 1 of 2

24AA08H/24LC08BH

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

VIEW A-A
SHEET 1

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	5		
Pitch	e	0.95 BSC		
Outside lead pitch	e1	1.90 BSC		
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E	2.80 BSC		
Molded Package Width	E1	1.60 BSC		
Overall Length	D	2.90 BSC		
Foot Length	L	0.30	-	0.60
Footprint	L1	0.60 REF		
Foot Angle	φ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

Notes:
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
     REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev F Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
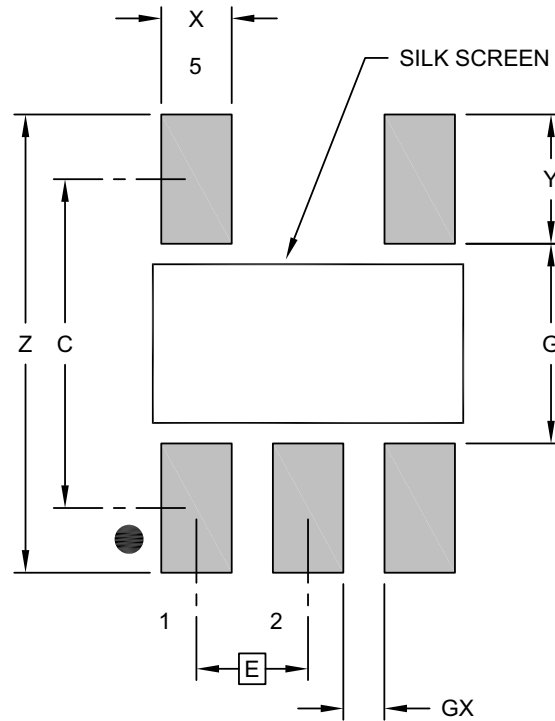
RECOMMENDED LAND PATTERN

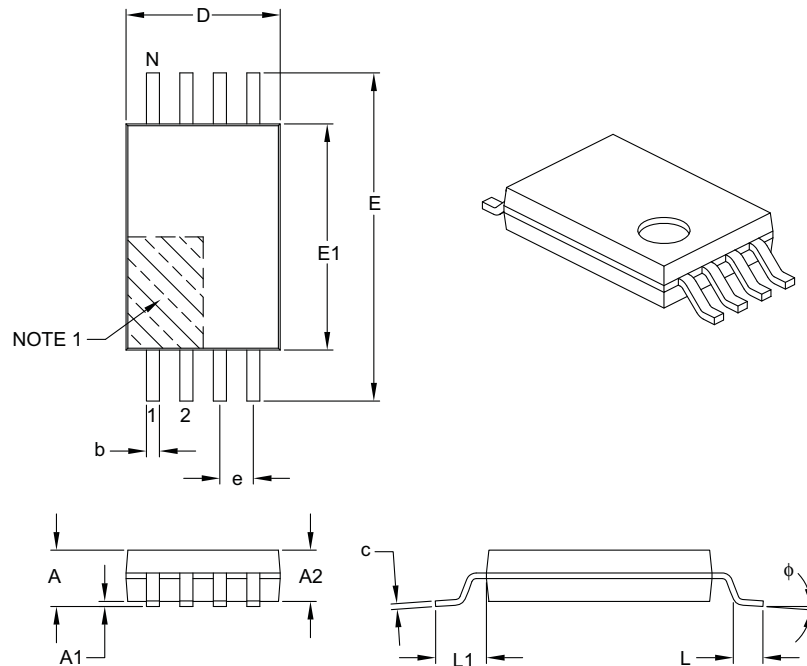|	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091-OT Rev F

24AA08H/24LC08BH

**8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN]
With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at
http://www.microchip.com/packaging

TOP VIEW

SIDE VIEW

BOTTOM VIEW
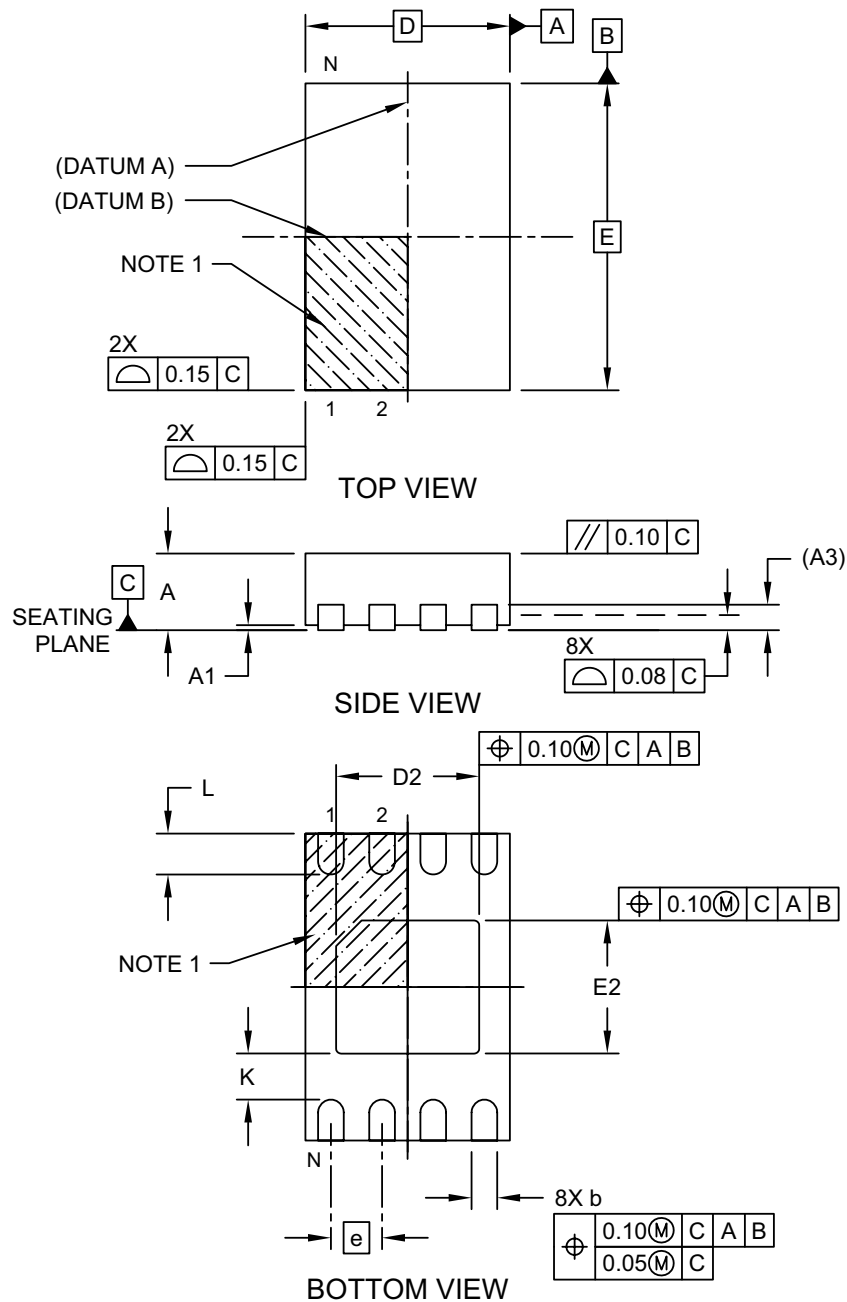
Microchip Technology Drawing No. C04-129-MN Rev E Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN]
With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
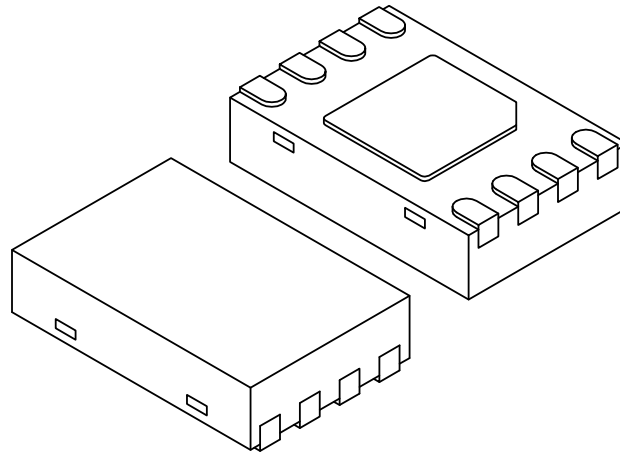
	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.35	1.40	1.45
Exposed Pad Width	E2	1.25	1.30	1.35
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
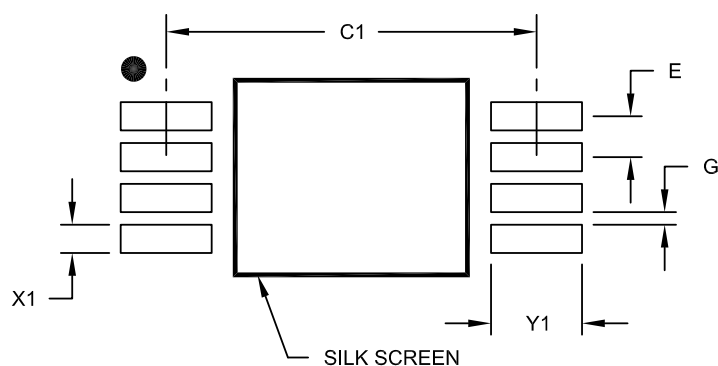REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129-MN Rev E Sheet 2 of 2

24AA08H/24LC08BH

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN]
With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

> **Note:** For the most current package drawings, please see the Microchip Packaging Specification located at
> http://www.microchip.com/packaging
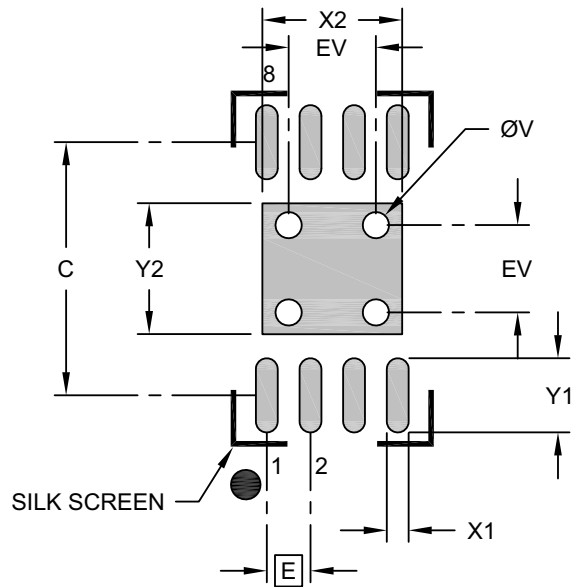
RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			1.50
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.25
Contact Pad Length (X8)	Y1			0.85
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

    BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-129-MN Rev. B

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging		

RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
    BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

APPENDIX A: REVISION HISTORY

Revision C (09/2021)

Updated formatting to current template; Replaced terminology "Master" and "Slave" with "Host" and "Client", respectively; Updated PDIP, SOIC, SOT-23 and TDFN package drawings.

Revision B (11/2013)

Correcting typo in TDFN markings and other miscellaneous corrections.

Revision A (04/2008)

Initial release of this document.

24AA08H/24LC08BH

THE MICROCHIP WEBSITE

Microchip provides online support via our website at www.microchip.com. This website is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the website contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip website at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the website at: http://microchip.com/support

PRODUCT IDENTIFICATION SYSTEM (NON-AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.   [X][1]   -X   /XX

| Device | Tape and Reel Option | Temperature Range | Package |

| Device: | 24AA08H | = | 1.7V, 8-Kbit I^{2}C Serial EEPROM |
| | 24LC08BH | = | 2.5V, 8-Kbit I^{2}C Serial EEPROM |

| Tape and Reel Option: | Blank | = | Standard packaging (tube or tray) |
| | T | = | Tape and Reel[1] |

| Temperature Range: | I | = | -40°C to +85°C (Industrial) |
| | E | = | -40°C to +125°C (Extended) |

Package:	MS	=	Plastic Micro Small Outline Package, 8-Lead (MSOP)
	P	=	Plastic Dual In-Line – 300 mil Body, 8-Lead (PDIP)
	SN	=	Plastic Small Outline - Narrow, 3.90 mm Body, 8-Lead (SOIC)
	OT	=	Plastic Small Outline Transistor, 5-Lead (SOT-23) (Tape and Reel only)
	MNY	=	Plastic Dual Flat, No Lead Package - 2x3x0.8 mm Body, 8-Lead (TDFN)
	ST	=	Plastic Thin Shrink Small Outline – 4.4 mm, 8-Lead (TSSOP)

Examples:

a) 24AA08H-I/P: Industrial Temperature,1.7V, PDIP package.

b) 24AA08H-I/SN: Industrial Temperature,1.7V, SOIC package.

c) 24AA08HT-I/OT: Tape and Reel, Industrial Temperature, 1.7V, SOT-23 package.

d) 24LC08BH-I/P: Industrial Temperature, 2.5V, PDIP package.

e) 24LC08BH-E/SN: Extended Temp.,2.5V SOIC package.

f) 24LC08BHT-I/OT: Tape and Reel, Industrial Temperature, 2.5V, SOT-23 package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

24AA08H/24LC08BH

PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X] [1]	X	/XX	XXX [2,3]
Device	Tape and Reel Option	Temperature Range	Package	Variant

Device:	24LC08BH = 2.5V, 8-Kbit I²C Serial EEPROM
Tape and Reel Option:	Blank = Standard packaging (tube or tray) T = Tape and Reel[1]
Temperature Range:	I = -40°C to +85°C (AEC-Q100 Grade 3) E = -40°C to +125°C (AEC-Q100 Grade 1)
Package:	MS = Plastic Micro Small Outline Package, 8-Lead (MSOP) SN = Plastic Small Outline - Narrow, 3.90 mm Body, 8-Lead (SOIC) OT = Plastic Small Outline Transistor, 5-Lead (SOT-23) ST = Plastic Thin Shrink Small Outline – 4.4 mm, 8-Lead (TSSOP)
Variant[2,3]:	16KVAO = Standard Automotive, 16K Process 16KVXX = Customer-Specific Automotive, 16K Process

Examples:

a) 24LC08BHT-I/SN16KVAO: Tape and Reel, Automotive Grade 3, 2.5V, SOIC Package.

b) 24LC08BHT-E/ST16KVAO: Tape and Reel, Automotive Grade 1, 2.5V, TSSOP Package.

c) 24LC08BHT-E/MS16KVAO: Tape and Reel, Automotive Grade 1, 2.5V, MSOP Package.

d) 24LC08BHT-E/OT16KVAO: Tape and Reel, Automotive Grade 1, 2.5V, SOT-23 Package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: The VAO/VXX automotive variants have been designed, manufactured, tested and qualified in accordance with AEC-Q100 requirements for automotive applications.

3: For customers requesting a PPAP, a customer-specific part number will be generated and provided. A PPAP is not provided for VAO part numbers.

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.

- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.

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