48L256

256-Kbit SPI Serial EERAM

Serial SRAM Features

- Unlimited Reads/Unlimited Writes:
  - Standard serial SRAM protocol
  - Symmetrical timing for reads and writes
- SRAM Array:
  - 32,768 x 8 bit
- High-Speed SPI Interface:
  - Up to 66 MHz
  - Schmitt Trigger inputs for noise suppression
- Low-Power CMOS Technology:
  - Active current: 5 mA (maximum)
  - Standby current: 300 µA (at 85°C maximum)
  - Hibernate current: 3 µA (at 85°C maximum)

Hidden EEPROM Backup Features

- Cell-Based Nonvolatile Backup:
  - Mirrors SRAM array cell-for-cell
  - Transfers all data to/from SRAM cells in parallel (all cells at same time)
- Invisible-to-User Data Transfers:
  - V_{CC} level monitored inside device
  - SRAM automatically saved on power disrupt
  - SRAM automatically restored on V_{CC} return
- 100,000 Backups Minimum (at 85°C)
- 100 Years Retention (at 55°C)

Other Features of the 48L256

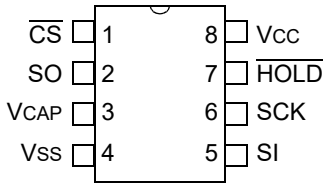
- Operating Voltage Range: 2.7V-3.6V
- Temperature Ranges:
  - Industrial (I): -40°C to +85°C
- ESD Protection: >2,000V

Packages

- 8-Lead SOIC

Package Types (not to scale)

8-Lead SOIC
(Top View)



Pin Function Table

Name	Function
$\overline{CS}$	Chip Select Input
SO	Serial Data Output
V_{CAP}	External Capacitor
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Hold Input
V_{CC}	Supply Voltage

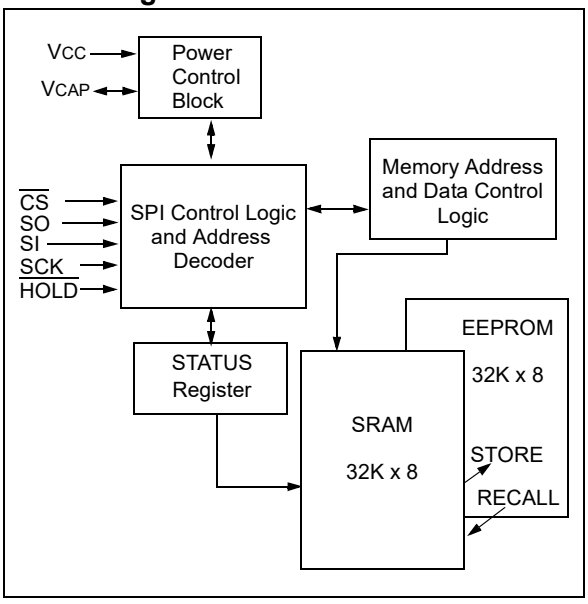
General Description

The Microchip Technology Inc. 48L256 serial EERAM has an SRAM memory core with hidden EEPROM backup. The device can be treated by the user as a full symmetrical read/write SRAM. Backup to EEPROM is handled by the device on any power disrupt, so the user can effectively view this device as an SRAM that never loses its data.

The device is structured as a 256-Kbit SRAM with EEPROM backup in each memory cell. The SRAM is organized as 32,768 x 8 bits and uses the SPI serial interface. The SPI bus uses three signal lines for communication: clock input (SCK), data in (SI), and data out (SO). Access to the device is controlled through a Chip Select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The SRAM is a conventional serial SRAM: it allows symmetrical reads and writes and has no limits on cell usage. The backup EEPROM is invisible to the user and cannot be accessed by the user independently. The device includes circuitry that detects VCC dropping below a certain threshold, shuts its connection to the outside environment, and transfers all SRAM data to the EEPROM portion of each cell for safe keeping. When VCC returns, the circuitry automatically returns the data to the SRAM and the user's interaction with the SRAM can continue with the same data set.

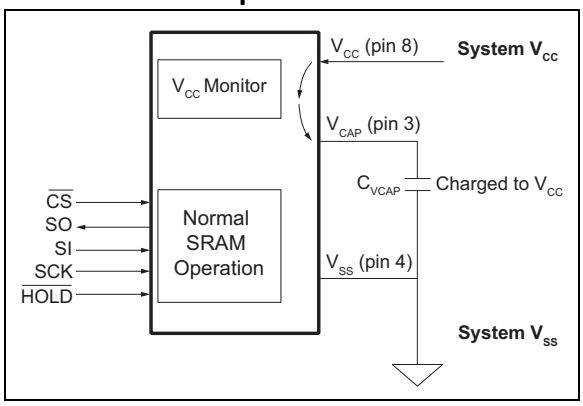
Block Diagram



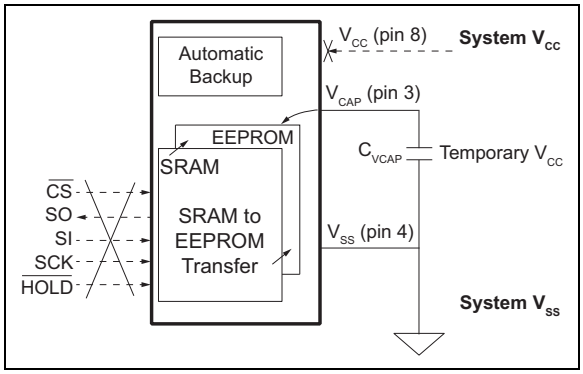
Powering the Device During SRAM to EEPROM Backup (VCAP)

A small capacitor (typically 33 µF) is required for the proper operation of the device. This capacitor is placed between VCAP (pin 3) and the system VSS (see Normal Device Operation). When power is first applied to the device, this capacitor is charged to VCC through the device (see Normal Device Operation). During normal SRAM operation, the capacitor remains charged to VCC and the level of system VCC is monitored by the device. If system VCC drops below a set threshold, the device interprets this as a power-off or brown-out event. The device suspends all I/O operation, shuts off its connection with the VCC pin, and uses the saved energy in the capacitor to power the device through the VCAP pin as it transfers all SRAM data to EEPROM (see Vcc Power-Off Event). On the next power-up of VCC, the data is transfered back to SRAM, the capacitor is recharged, and the SRAM operation continues.

Normal Device Operation



VCC Power-Off Event



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

VCC.....4.5V

All inputs and outputs w.r.t. VSS ..... -0.6V to 4.5V

Storage temperature .....-65°C to +150°C

Ambient temperature under bias.....-40°C to +85°C

ESD protection on all pins..... 2 kV

† NOTICE: Stresses above those listed under 'Maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			**Electrical Characteristics:** Industrial (I): TA = -40°C to +85°C VCC = 2.7V to 3.6V				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
D1	VIH	High-Level Input Voltage	VCC x 0.8	—	VCC + 0.5	V	
D2	VIL	Low-Level Input Voltage	-0.5	—	VCC x 0.2	V	
D3	VOH	High-Level Output Voltage	VCC - 0.5	—	—	V	IOH = -0.4 mA
D4	VOL	Low-Level Output Voltage	—	—	0.4	V	IOL = 2.0 mA
D5	ILI	Input Leakage Current	—	—	±3	µA	VIN = VSS or VCC
D6	ILO	Output Leakage Current	—	—	±3	µA	$\overline{CS}$ = VCC, VOUT = VSS or VCC
D7	CIN	Internal Capacitance (all input pins)	—	—	5	pF	TA = 25°C, FREQ = 1 MHz, VCC = 3.6V (**Note 1**)
D8	COUT	Internal Capacitance (SO pin)	—	—	7	pF	TA = 25°C, FREQ = 1 MHz, VCC = 3.6V (**Note 1**)
D9	ICC Active	Operating Current	—	—	5	mA	TA = 85°C, VCC = 3.6V, FCLK = 66 MHz (**Note 2**)
D10	ICC Store	Store Current	—	—	2	mA	TA = 85°C, 2.7V < VCC ≤ 3.6V (**Note 3**)
D11	ICCS	Standby Current	—	—	300	µA	TA = 85°C, SI, $\overline{CS}$, VCAP, VCC = 3.6V
D12	ICCH	Hibernate Current	—	—	3	µA	TA = 85°C, SI, $\overline{CS}$, VCAP, VCC = 3.6V
D13	VTRIP	AutoStore/AutoRecall Trip Voltage	2.30	—	2.65	V	
D14	VHYS	Trip Voltage Hysteresis	—	300	—	mV	**Note 1**
D15	VPOR	Power-on Reset Voltage	—	1.8	—	V	**Note 1**
D16	CVCAP	VCAP Capacitance	22	33	50	µF	Rated 6.3V or higher (**Note 1**)

Note 1: This parameter is periodically sampled and not 100% tested.

2: ICC Active measured with SO pin unloaded. Current can vary with output loading and clock frequency.

3: Store current is specified as an average current across the entire store operation.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): TA = -40°C to +85°C VCC = 2.7V to 3.6V			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	FCLK	Clock Frequency	—	66	MHz	
2	TCSS	$\overline{CS}$ Setup Time	6	—	ns	
3	TCSH	$\overline{CS}$ Hold Time	6	—	ns	
4	TCSD	$\overline{CS}$ Disable Time	7	—	ns	
5	TSU	Data Setup Time	4	—	ns	
6	THD	Data Hold Time	4	—	ns	
7	TR	CLK Rise Time	—	100	ns	**Note 1**
8	TF	CLK Fall Time	—	100	ns	**Note 1**
9	THI	Clock High Time	7	—	ns	
10	TLO	Clock Low Time	7	—	ns	
11	TCLD	Clock Delay Time	7	—	ns	
12	TCLE	Clock Enable Time	3	—	ns	
13	TV	Output Valid from Clock Low	—	10	ns	
14	THO	Output Hold Time	0	—	ns	**Note 1**
15	TDIS	Output Disable Time	—	20	ns	**Note 1**
16	THZ	$\overline{HOLD}$ Low to Output High-Z	—	10	ns	**Note 1**
17	THV	$\overline{HOLD}$ High to Output Valid	—	10	ns	
18	THS	$\overline{HOLD}$ Setup Time	0		ns	
19	THH	$\overline{HOLD}$ Hold Time	5		ns	
20	TRESTORE	Power-up AutoRecall/Hibernation Wake-up Operation Duration	—	200	µs	
21	TRECALL	SW Recall Operation Duration	—	50	µs	
22	TSTORE	Store Operation Duration	—	10	ms	
23	TVRISE	VCC Rise Rate	30	—	µs/V	**Note 1**
24	TVFALL	VCC Fall Rate	30	—	µs/V	**Note 1**
25		Endurance	100,000	—	Store Cycles	**Note 1**
26		Retention	100	—	Years	At 55°C
			10	—	Years	At 85°C

Note 1: This parameter is not tested but ensured by characterization.

FIGURE 1-1: HOLD TIMING

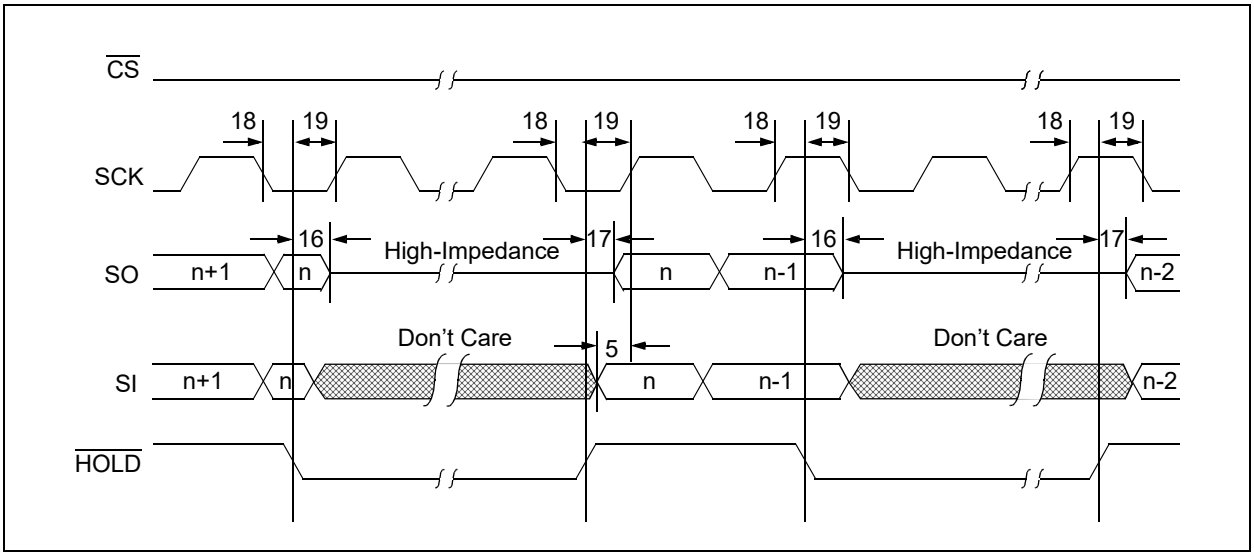


FIGURE 1-2: SERIAL INPUT TIMING MODE 0,0

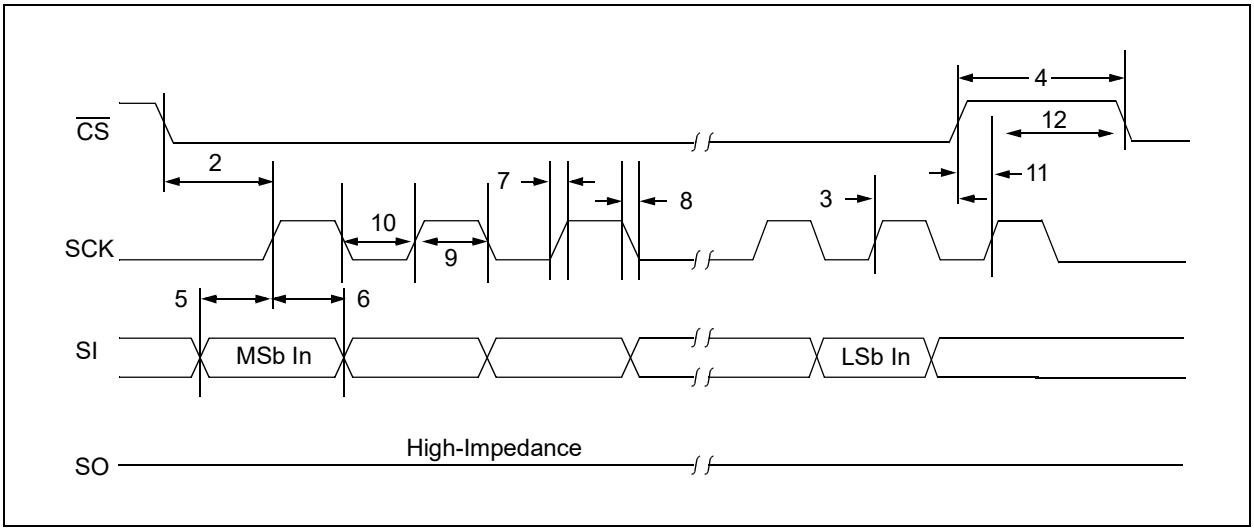


FIGURE 1-3: SERIAL INPUT TIMING MODE 1,1

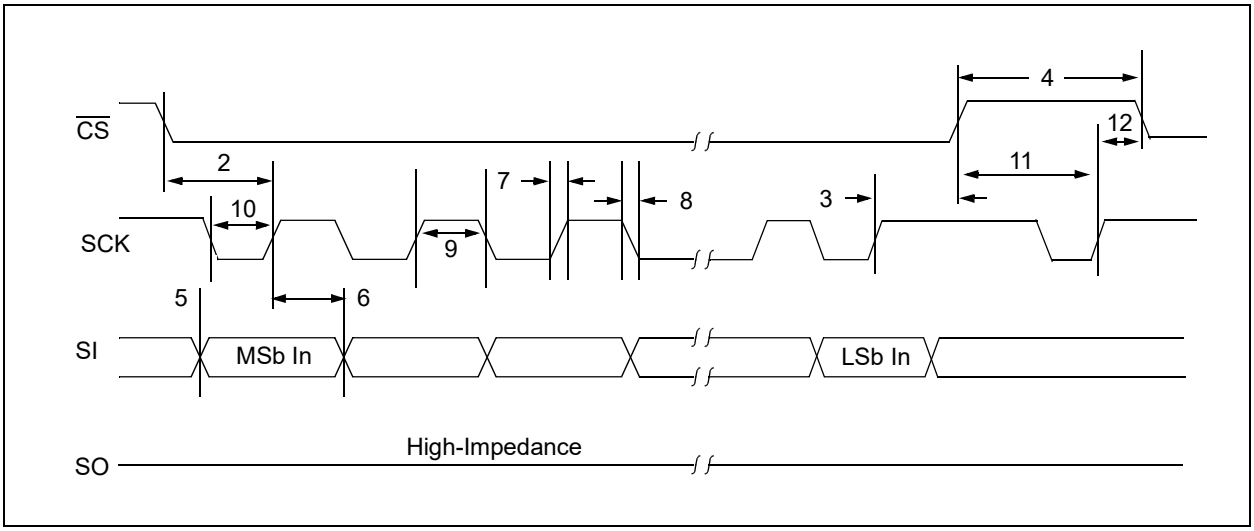


FIGURE 1-4: SERIAL OUTPUT TIMING

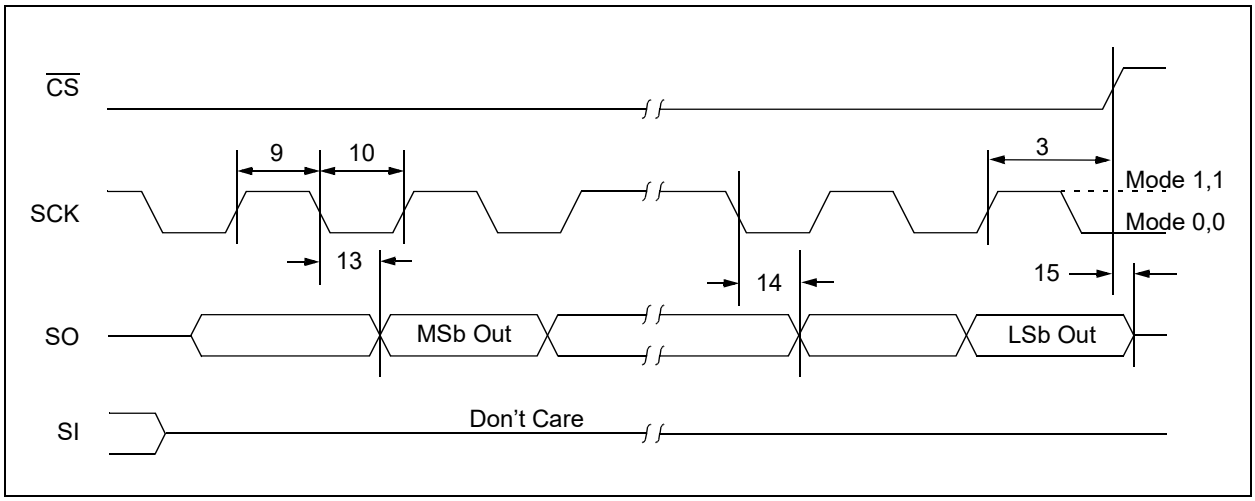
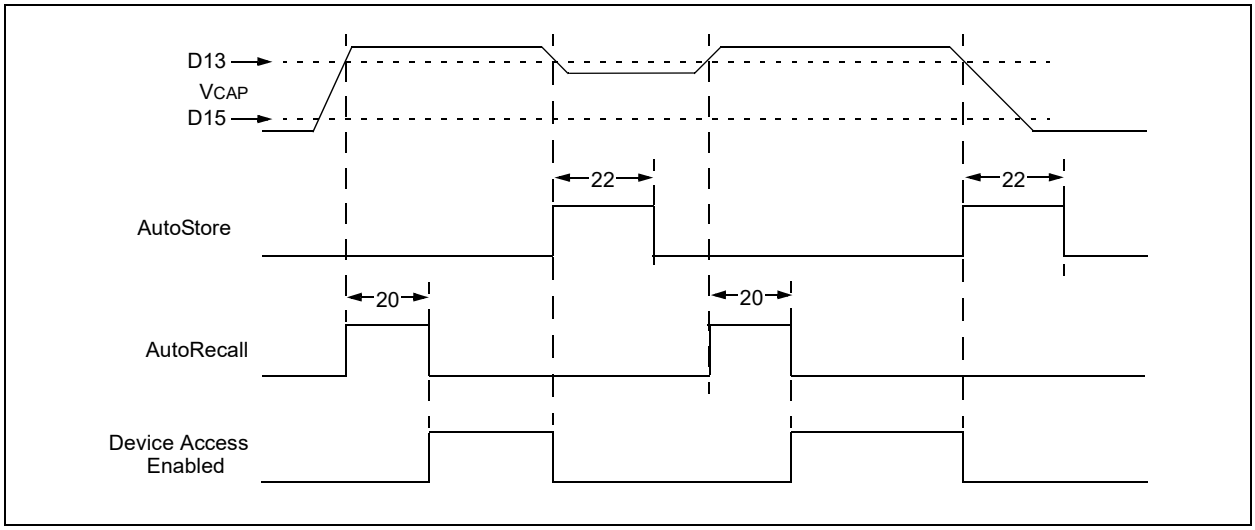


TABLE 1-3: AC TEST CONDITIONS

AC Waveform	
V_{LO} = 0.2V	
V_{HI} = V_{CC} - 0.2V	
C_L = 30 pF	
Timing Measurement Reference Level	
Input	0.5 V_{CC}
Output	0.5 V_{CC}

FIGURE 1-5: AUTOSTORE/AUTORECALL TIMING DATA



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	8-Lead SOIC	Description
$\overline{CS}$	1	Chip Select Input
SO	2	Serial Data Output
VCAP	3	External Capacitor
VSS	4	Ground
SI	5	Serial Data Input
SCK	6	Serial Clock Input
$\overline{HOLD}$	7	Hold Input
VCC	8	Supply Voltage

2.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{CS}$ after a valid write sequence completes the SRAM write cycle. After power-up, a high-to-low transition on $\overline{CS}$ is required prior to any sequence being initiated.

2.2 Serial Output (SO)

The SO pin is used to transfer data out of the 48L256. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

2.3 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses, and data. Data is latched on the rising edge of the serial clock.

2.4 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 48L256. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

2.5 Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to suspend transmission to the 48L256 while in the middle of a serial sequence without having to retransmit the entire sequence over again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence.

The $\overline{HOLD}$ pin should be brought low while SCK is low, otherwise the Hold function will not be invoked until the next SCK high-to-low transition. The 48L256 must remain selected during this sequence. The SI and SCK levels are “don’t cares” during the time the device is paused and any transitions on these pins will be ignored. To resume serial communication, the $\overline{HOLD}$ pin should be brought high while the SCK pin is low, otherwise serial communication will not be resumed until the next SCK high-to-low transition.

The SO line will tri-state immediately upon a high-to-low transition of the $\overline{HOLD}$ pin, and will begin outputting again immediately upon a subsequent low-to-high transition of the $\overline{HOLD}$ pin, independent of the state of SCK.

3.0 MEMORY ORGANIZATION

3.1 Data Array Organization

The 48L256 is internally organized as a continuous SRAM array for both reading and writing, along with a nonvolatile EEPROM array that is not directly accessible to the user, but which can be refreshed or recalled on power cycles or on software commands. The array can be configured either as a continuous range or into pages. The page size in this device is 64 bytes. The Page mode option is controlled by the PRO bit in the STATUS register.

3.2 16-Bit Nonvolatile User Space

The 48L256 device contains a 16-bit (2-byte) nonvolatile user space, separate from the SRAM memory array. The nonvolatile user space can be written with the Write Nonvolatile User Space command and read with the Read Nonvolatile User Space command. Once written, these 2 bytes remain volatile and can be rewritten. They are copied to nonvolatile memory – at the same time as the SRAM array and STATUS register – automatically on any power disruption or by using the Software Store command described in **Section 11.0 "Store/Recall Operations"**.

Reading and writing to the nonvolatile user space does not use address bits, only the specific access instruction to precede the operation. Writing to the nonvolatile user space requires writing all of its bits in one operation. Failing to write to all nonvolatile user space bits will abort the write operation and leave the nonvolatile user space value unchanged from its previous value. Similarly, reading the nonvolatile user space memory uses no address bits, but partial reads are allowed.

3.3 Device Registers

The 48L256 contains a STATUS register for controlling and monitoring functions of the device.

3.3.1 STATUS REGISTER

The STATUS register is an 8-bit combination of writable and read-only bits. It is used to modify the write protection functions as well as store various aspects of the current status of the device. The writable bit values written to the STATUS register are volatile – until they are copied to nonvolatile memory automatically on any power disruption or by using the Software Store command described in **Section 11.0 "Store/Recall Operations"** – and can be overwritten from a previous status in a recall operation. Details about the STATUS register are covered in **Section 6.0 "STATUS Register"**.

4.0 FUNCTIONAL DESCRIPTION

The 48L256 is controlled by a set of instructions that are sent from a host controller, commonly referred to as the SPI Master. The SPI Master communicates with the 48L256 via the SPI bus which is comprised of four signal lines:

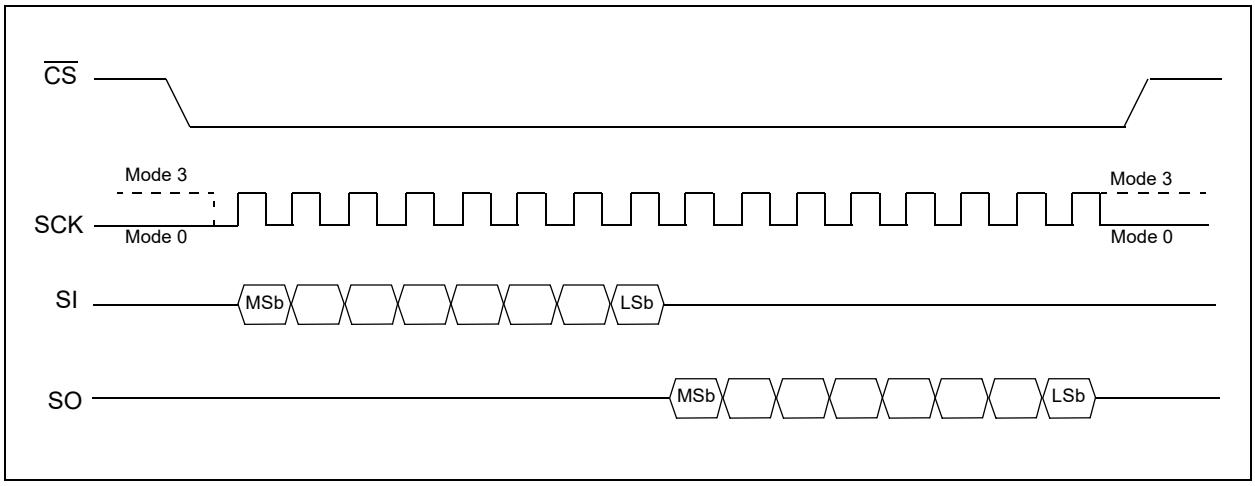
- Chip Select ($\overline{CS}$)
- Serial Clock (SCK)
- Serial Input (SI)
- Serial Output (SO)

The SPI protocol defines a total of four modes of operation (Mode 0, 1, 2 or 3) with each mode differing in respect to the SCK polarity and phase and how the polarity and phase control the flow of data on the SPI bus.

The 48L256 supports the two most common modes, SPI Modes 0 and 3. With SPI Modes 0 and 3, data is always latched in on the rising edge of SCK and always output on the falling edge of SCK. The only difference between SPI Modes 0 and 3 is the polarity of the SCK signal when in the Inactive state (when the SPI Master is in Standby mode and not transferring any data). SPI Mode 0 is defined as a low SCK while $\overline{CS}$ is not asserted (high) and SPI Mode 3 has SCK high in the Inactive state. The SCK Idle state must match when the $\overline{CS}$ is deasserted both before and after the communication sequence in SPI Mode 0 and 3.

The figures in this document depict Mode 0 with a solid line on SCK while $\overline{CS}$ is inactive and Mode 3 with a dotted line.

FIGURE 4-1: SPI MODE 0 AND MODE 3



4.1 Interfacing the 48L256 on the SPI Bus

Communication to and from the 48L256 must be initiated by the SPI Master device. The SPI Master device must generate the serial clock for the 48L256 on the SCK pin. The 48L256 always operates as a slave due to the fact that the Serial Clock pin (SCK) is always an input.

4.1.1 SELECTING THE DEVICE

The 48L256 is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted via the SI pin and the SO pin will remain in a high-impedance state.

4.1.2 SENDING DATA TO THE DEVICE

The 48L256 uses the Serial Data Input (SI) pin to receive information. All instructions, addresses and data input bytes are clocked into the device with the Most Significant bit (MSb) first.

The SI pin samples on the first rising edge of the SCK line after the $\overline{CS}$ has been asserted.

4.1.3 RECEIVING DATA FROM THE DEVICE

Data output from the device is transmitted on the Serial Data Output (SO) pin with the MSb output first. The SO data is latched on the falling edge of the first SCK clock cycle after the instruction has been clocked into the device, such as the Read from Memory Array and Read STATUS Register instructions. See **Section 6.0 "STATUS Register"** for more details.

4.2 DEVICE OPCODES

4.2.1 SERIAL OPCODE

After the device is selected by driving $\overline{CS}$ low, the first byte sent must be the opcode that defines the operation to be performed.

The 48L256 utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Table 4-1. All instructions, addresses and data are transferred with the MSb first and are initiated with a high-to-low $\overline{CS}$ transition and completed with a low-to-high $\overline{CS}$ transition.

TABLE 4-1: INSTRUCTION SET FOR 48L256

Command	Operation Description	Opcode		Address Bytes	Data Bytes	Reference Section
Write Control Commands						
WREN	Set Write Enable Latch (WEL)	06h	0000 0110	0	0	5.1
WRDI	Reset Write Enable Latch (WEL)	04h	0000 0100	0	0	5.2
SRAM Commands						
WRITE	Write to SRAM Array	02h	0000 0010	2	1+	8.0
READ	Read from SRAM Array	03h	0000 0011	2	1+	7.1
RDLSWA	Read Last Successfully Written Address	0Ah	0000 1010	0	2	7.2
Secure WRITE	Secure Write to SRAM Array with CRC	12h	0001 0010	2	64	10.1
Secure READ	Secure Read from SRAM Array with CRC	13h	0001 0011	2	64	10.2
STATUS Register Commands						
WRSR	Write STATUS Register (SR)	01h	0000 0001	0	1	6.5
RDSR	Read STATUS Register (SR)	05h	0000 0101	0	1	6.4
Store/Recall Commands						
STORE	Store SRAM data to EEPROM array	08h	0000 1000	0	0	11.3
RECALL	Copy EEPROM data to SRAM array	09h	0000 1001	0	0	11.4
Nonvolatile User Space Commands						
WRNUR	Write Nonvolatile User Space	C2h	1100 0010	0	2	9.1
RDNUR	Read Nonvolatile User Space	C3h	1100 0011	0	2	9.2
Hibernate Commands						
Hibernate	Enter Hibernate mode	B9h	1011 1001	0	0	12.0

4.2.2 HOLD FUNCTION

The $\overline{HOLD}$ pin is used to pause the serial communication with the device without having to stop or reset the clock sequence. The Hold mode, however, does not have an effect on the internal write cycle. Therefore, if a write cycle is in progress, asserting the $\overline{HOLD}$ pin will not pause the operation and the write cycle will continue until it is finished.

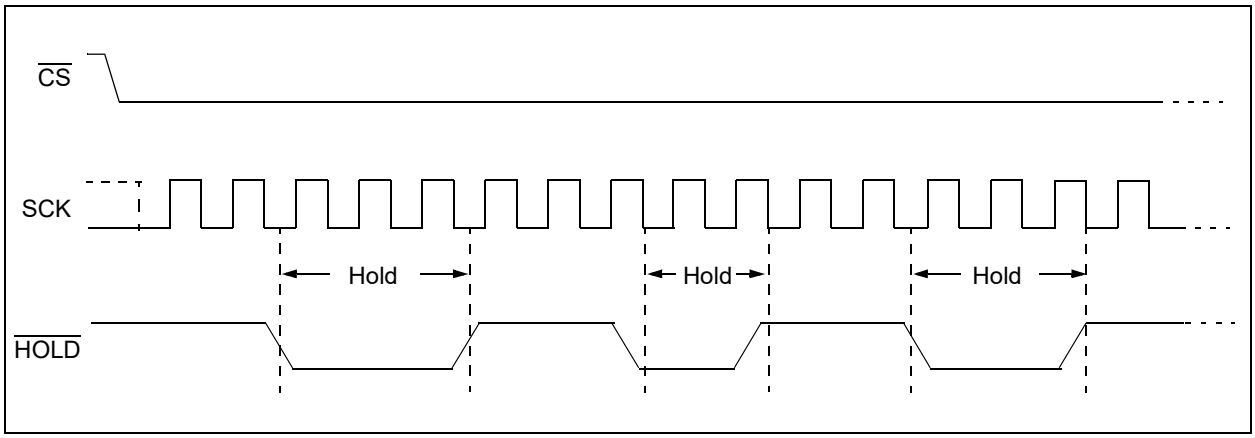
The Hold mode can only be entered while the $\overline{CS}$ pin is asserted. The Hold mode is activated by asserting the $\overline{HOLD}$ pin during the SCK low pulse. If the $\overline{HOLD}$ pin is asserted during the SCK high pulse, then the Hold mode will not be started until the beginning of the next SCK low pulse. The device will remain in the Hold mode as long as the $\overline{HOLD}$ pin and $\overline{CS}$ pin are asserted.

While in Hold mode, the SO pin will be in a high-impedance state. In addition, both the SI pin and the SCK pin will be ignored.

To end the Hold mode and resume serial communication, the $\overline{HOLD}$ pin must be deasserted during the SCK low pulse. If the $\overline{HOLD}$ pin is deasserted during the SCK high pulse, then the Hold mode will not end until the beginning of the next SCK low pulse.

If the $\overline{CS}$ pin is deasserted while the $\overline{HOLD}$ pin is still asserted, then any operation that may have been started will be aborted and the device will reset the WEL bit in the STATUS register back to the logic '0' state.

FIGURE 4-2: HOLD MODE



5.0 WRITE ENABLE AND DISABLE

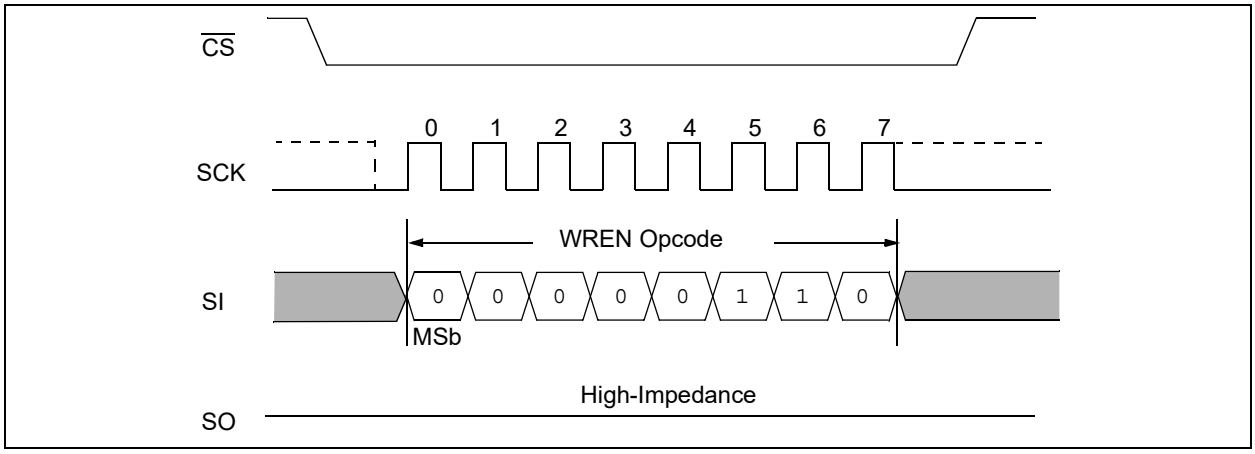
5.1 Write Enable Instruction (WREN)

The Write Enable Latch (WEL) bit of the STATUS register must be set to a logic '1' prior to each WRSR or WRITE instruction. The WEL bit is set to a logic '1' by sending a WREN (06h) command to the 48L256. First, the $\overline{CS}$ pin is driven low to select the device and then a 06h instruction is clocked in on the SI pin. Then the $\overline{CS}$ pin is driven high. The WEL bit will be immediately updated in the STATUS register to a logic '1'.

The WEL bit will also be reset to a logic '0' in the following circumstances:

- Upon power-up as the power on default condition is the Write Disable state (**Section 6.2 "Write Enable Latch"**)
- The completion of any write operation (WRITE, WRSR)
- A write operation of any type to a memory location or register that is protected or locked
- Executing a Write Disable (WRDI) instruction (**Section 5.2 "Write Disable Instruction (WRDI)"**)
- A Hold abort occurs as noted in **Section 4.2.2 "Hold Function"** ($\overline{CS}$ deasserted while $\overline{HOLD}$ pin is low)

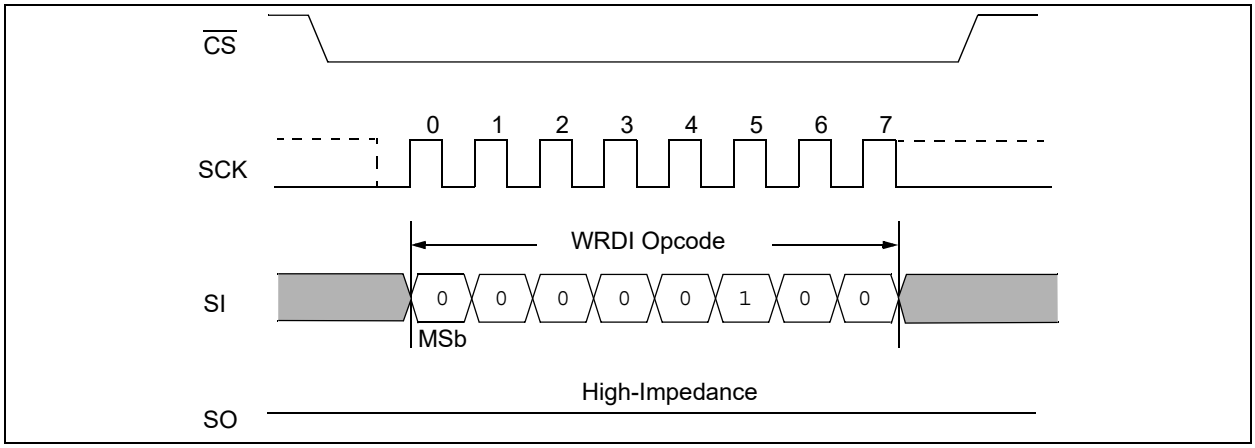
FIGURE 5-1: WREN WAVEFORM



5.2 Write Disable Instruction (WRDI)

To protect the device against inadvertent writes, the Write Disable instruction (opcode 04h) disables all programming modes by setting the WEL bit to a logic '0'.

FIGURE 5-2: WRDI WAVEFORM



6.0 STATUS REGISTER

The 48L256 includes a 1-byte STATUS register which is a combination of four nonvolatile bits and four volatile bits. The STATUS register bits control or indicate various features of the device as shown in Register 6-1. These bits can be read or modified by specific instructions that are detailed in the subsequent sections.

REGISTER 6-1: STATUS REGISTER

R/W	R/W	R/W	R-0	R/W	R/W	R-0	R-0
Reserved	$\overline{ASE}$	$\overline{PRO}$	$\overline{SWM}$	BP1	BP0	WEL	$\overline{RDY}$/BSY
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Reserved:** Must be set to '0'

bit 6 $\overline{\textbf{ASE}}$**:** AutoStore Enable bit
1 = AutoStore is disabled
0 = AutoStore is enabled (factory default)

bit 5 $\overline{\textbf{PRO}}$**:** Page Rollover bit
1 = Continuous writes are enabled, page emulation mode disabled
0 = Writes crossing page boundary causes address to roll over to beginning of page (factory default)

bit 4 $\overline{\textbf{SWM}}$**:** Secure Write Monitoring bit – Read-Only
1 = The last secure write operation has failed
0 = No error reported in Secure Write

bit 3-2 **BP[1:0]:** Block Protection bits (see Table 6-2)
00 = (Level 0) No SRAM array write protection
01 = (Level 1) Upper quarter SRAM memory array protection
10 = (Level 2) Upper half SRAM memory array protection
11 = (Level 3) Entire SRAM memory array protection

bit 1 **WEL:** Write Enable Latch bit – Read-Only
1 = WREN has been executed and device is enabled for writing
0 = Device is not write-enabled

bit 0 $\overline{\textbf{RDY}}$**/BSY:** $\overline{\text{Ready}}$/Busy Status bit – Read-Only
1 = Device is busy with an internal store or recall operation
0 = Device is ready for standard SRAM Read/Write commands

6.1 Block Write-Protect Bits

The 48L256 contains four levels of SRAM write protection using the block protection function. The nonvolatile Block Write-Protect bits (BP1, BP0) are located in bits three and two of the first STATUS register byte and define the region of the SRAM that are to be treated as read-only.

The address ranges that are protected for each SRAM Block Write Protection level and the corresponding STATUS register control bits are shown in Table 6-2.

TABLE 6-2: BLOCK WRITE-PROTECT BITS

Level	STATUS Register Bits [3:2]		Protected Address Range
	BP1	BP0	48L256
0	0	0	None
1	0	1	6000-7FFF
2	1	0	4000-7FFF
3	1	1	0000-7FFF

6.2 Write Enable Latch

Enabling and disabling writing to the STATUS register and the SRAM array is accomplished through the Write Enable (WREN) instruction as shown in **Section 5.1 "Write Enable Instruction (WREN)"** and the Write Disable (WRDI) instruction as shown in **Section 5.2 "Write Disable Instruction (WRDI)"**. These functions change the status of the WEL bit (bit 1) in the STATUS register.

6.3 Ready/Busy Status Latch

The Ready/Busy Status Latch is used to indicate whether the device is currently active in a nonvolatile write operation. This bit is read-only and automatically updated by the device. This bit is provided in bit position '0'.

A logic '1' bit indicates that the device is currently busy performing an SRAM to EEPROM transfer or EEPROM to SRAM restore operation. During this time, only the Read STATUS Register (RDSR) command will be executed by the device.

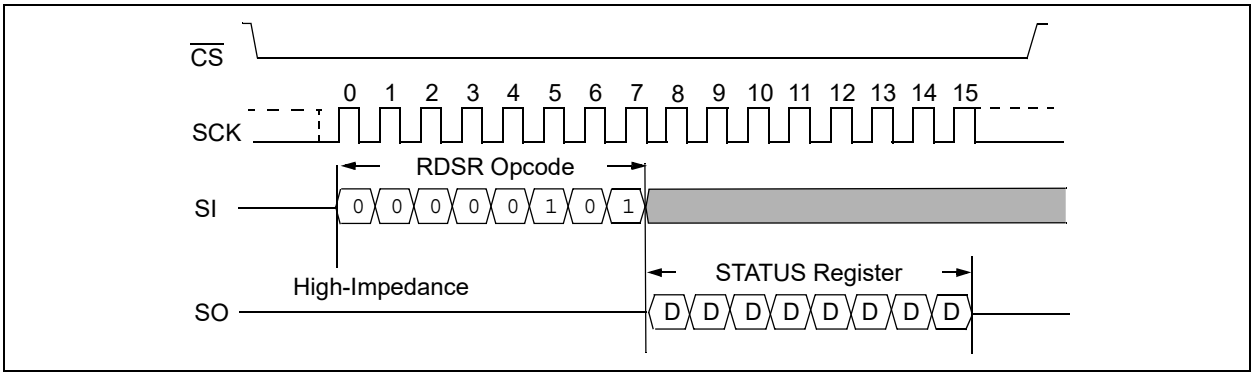
A logic '0' bit in this position indicates the device is ready to accept new SRAM Read/Write commands.

6.4 Read STATUS Register (RDSR)

The Read STATUS Register (RDSR) instruction provides access to the contents of the STATUS register. The STATUS register is read by asserting the CS pin followed by sending in a 05h opcode. The device will return the 8-bit STATUS register value on the SO pin.

The STATUS register can be continuously read for data by continuing to read beyond the first 8-bit value returned. The 48L256 will update the STATUS register value upon the completion of every eight bits, thereby allowing new STATUS register values to be read without having to issue a new RDSR instruction.

FIGURE 6-1: RDSR WAVEFORM



6.5 Write STATUS Register (WRSR)

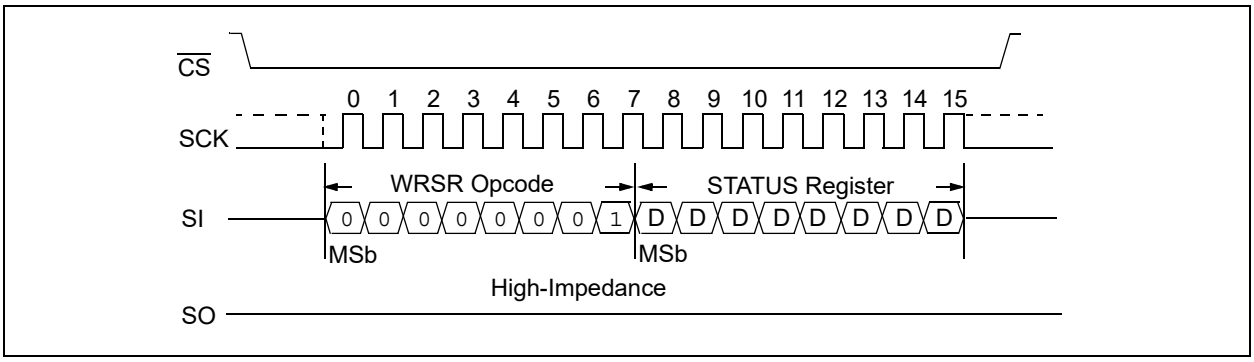
The Write STATUS Register (WRSR) instruction enables the SPI Master to change selected bits of the STATUS register. Before a WRSR sequence can be initiated, a WREN instruction must be executed to set the WEL bit to logic '1'. Upon completion of a WREN sequence, a WRSR sequence can be executed.

The WRSR command can be used to modify the writable bits in the STATUS register. The $\overline{SWM}$ and $\overline{RDY}$/BSY bits are read-only.

The 48L256 will respond to commands immediately after a WRSR sequence.

Note: The updated STATUS register value will only be stored into nonvolatile memory when there is a store operation.

FIGURE 6-2: WRSR WAVEFORM



7.0 READ OPERATIONS

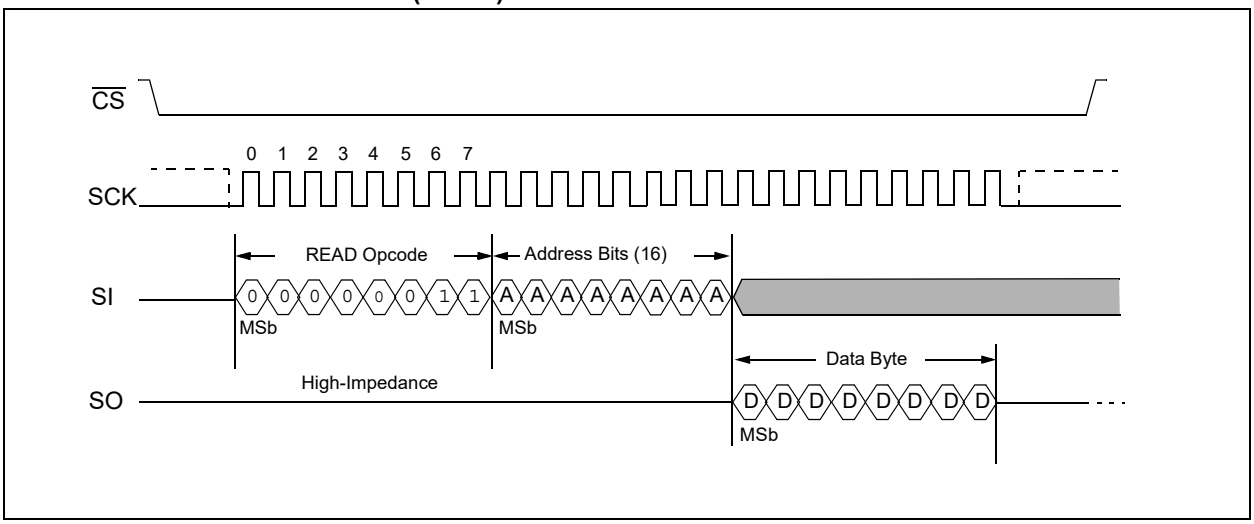
7.1 Reading from the SRAM (READ)

Reading the SRAM contents can be done whenever the device is not in an internal store or recall cycle, as indicated by the Ready/Busy bit of the STATUS register. To read the SRAM, first the $\overline{CS}$ line is pulled low to select the device and the Read opcode 03h is transmitted via the SI line followed by the 16-bit address to be read.

Upon completion of the address bytes, any data on the SI line will be ignored. The data (D7–D0) at the specified address is then shifted out onto the SO line. Any number of bytes can be clocked out, and if the address reaches the end of the array, it can continue at the beginning of the array. Read operations are not limited by page boundaries.

The read sequence can be terminated at any point of the operation. The $\overline{CS}$ line should be driven high after the data is clocked out.

FIGURE 7-1: READ SRAM (READ) WAVEFORM

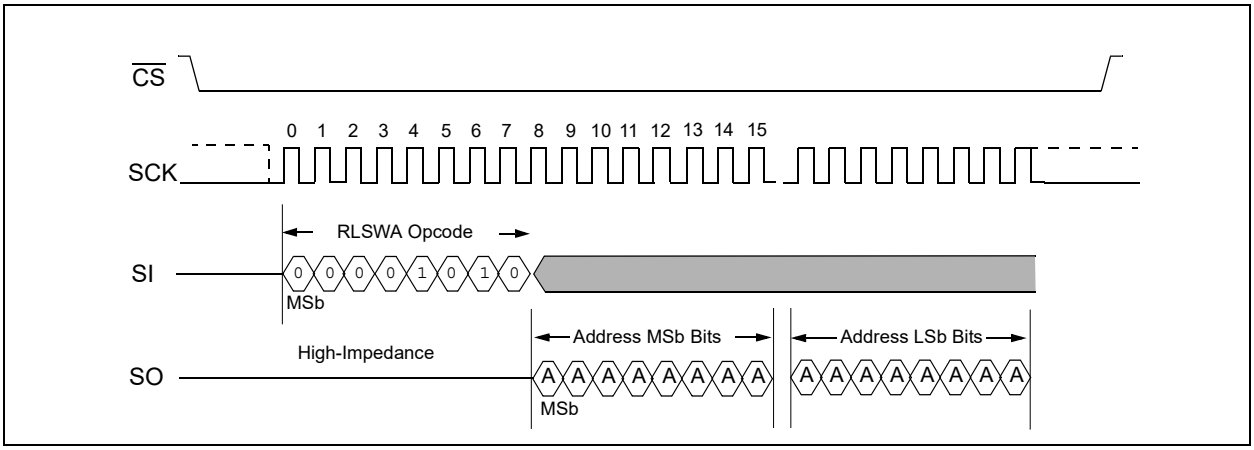


7.2 Read Last Successfully Written Address (RDLSWA)

The 48L256 devices offer a function to read out the last successfully written address. The value of the last written address is held in a memory location with the same ability to be stored into nonvolatile memory during a store operation so that the value can be made available after a power cycle with the AutoStore function.

To read the address of the last written byte, the SPI command 0x0A is clocked in on SI, then the address bits are clocked out on the SO pin. The number of address bytes returned corresponds to the size of the memory array, which is 2 bytes in the 256K device. Any MSb bits that are beyond the address range will return as zero.

FIGURE 7-2: READ LAST SUCCESSFULLY WRITTEN ADDRESS WAVEFORM



8.0 WRITE COMMANDS

In order to write to the SRAM in the 48L256, the device must be write-enabled via the Write Enable (WREN) instruction. If the device is not Write Enabled (WREN), the device will ignore the SRAM Write instruction and will return to the Standby state when $\overline{CS}$ is brought high. Each unique write to the SRAM array is immediately transferred to SRAM, not to EEPROM, so there is no delay after one write to begin another SRAM read/write operation. Contents of the SRAM are only transferred to EEPROM upon a store operation, such as a Software Store command, or upon an AutoStore operation at power-down (if enabled). (see **Section 11.3 "Software Store Command"**).

Note: If the $\overline{CS}$ pin is deselected at somewhere other than the end of an 8-bit byte boundary, the last partial byte operation will be aborted, the completed bytes will be written to the SRAM array. The RLSWA register will indicate the address of the last successfully written byte.

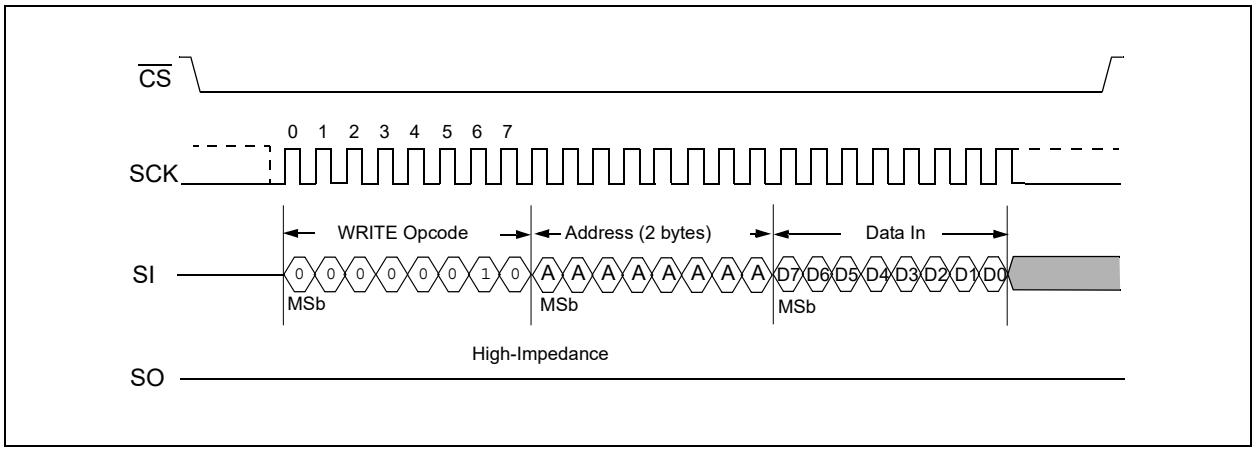
The 48L256 is automatically returned to the Write Disable state (STATUS register bit WEL = 0) at the completion of an SRAM write operation.

8.1 Write Instruction Sequences

8.1.1 SRAM BYTE WRITE

Once a WREN command has been completed, an SRAM byte write sequence can be performed as shown in Figure 8-1. After the $\overline{CS}$ line is pulled low to select the device, the opcode is transmitted via the SI line, followed by the 15-bit address, proceeded by stuff bits to total 16 address bits and the data (D7-D0) to be programmed.

FIGURE 8-1: SRAM BYTE WRITE WAVEFORM



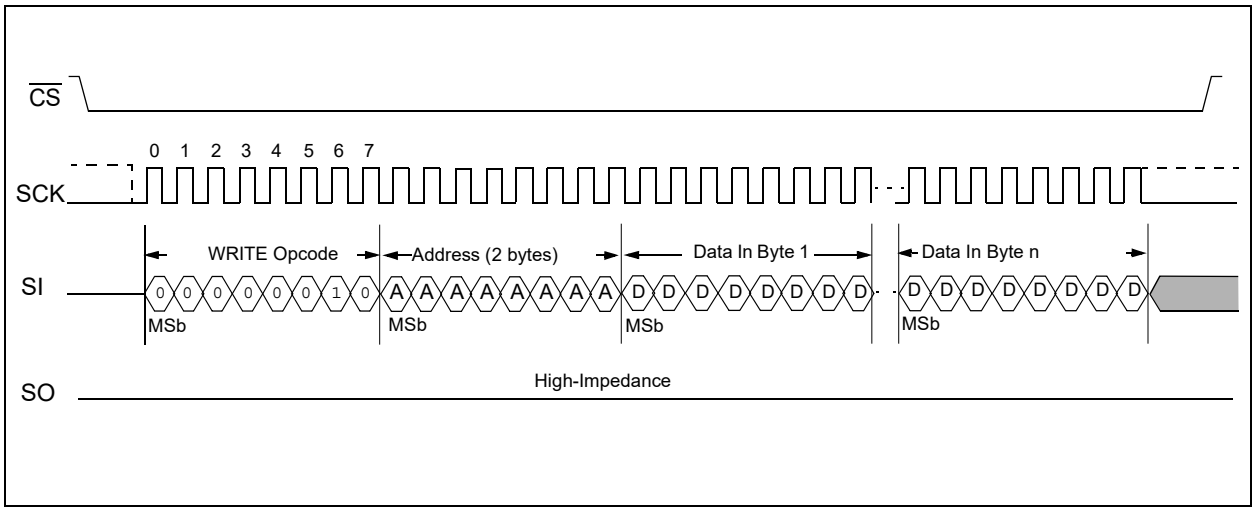
8.1.2 CONTINUOUS WRITE

Writing to a number of SRAM bytes is similar to a byte write, however, more bytes can be added after the first byte in the same write cycle. If more bytes of data are transmitted than what will fit to the end of that memory page or array, the address counter will “roll over” to the beginning of the SRAM page or array. Previously written data will be overwritten. The behavior of the rollover will depend on whether the $\overline{PRO}$ bit is set in the STATUS register. If $\overline{PRO}$ is set to 0, then the address wraps back to the beginning of the page. If $\overline{PRO}$ is set to 1, then data can continue past the page boundary, only to wrap at the end of the memory array. This 256K device has 64-byte pages.

Upon completion of the write, the 48L256 automatically returns to the Write Disable state (STATUS register bit WEL = 0).

Note:	If the $\overline{CS}$ pin is deselected at somewhere other than the end of an 8-bit boundary, the last partial byte operation will be aborted and the completed bytes will be written to the SRAM array.

FIGURE 8-2: CONTINUOUS SRAM WRITE WAVEFORM



9.0 NONVOLATILE USER SPACE ACCESS

The 256K device has 2 bytes (16 bits) of nonvolatile user space memory.

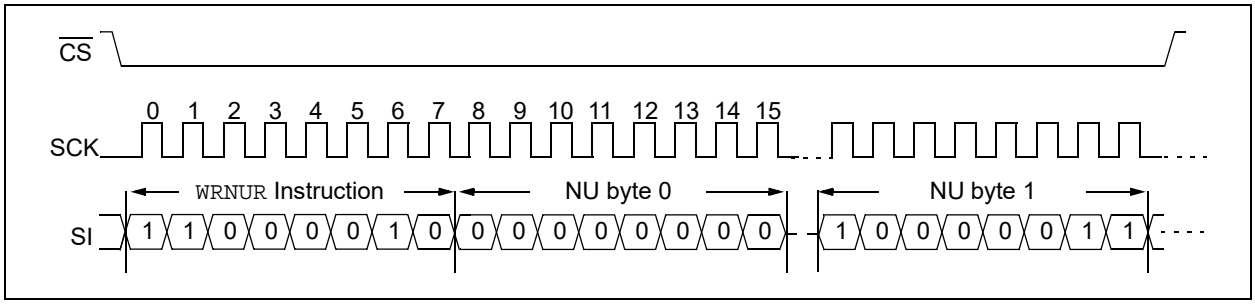
The nonvolatile user space memory is accessed through the WRNUR and RDNUR instructions. Data written to the nonvolatile user space memory is volatile but will be transferred to EEPROM automatically on any power disruption. The last content will then be restored from EEPROM on the next power-up. Software Store and Software Recall can also be executed by the user as described in **Section 11.0 "Store/Recall Operations"**.

9.1 Write Nonvolatile User Space (WRNUR)

Writing to the 16-bit nonvolatile user space requires the WEL bit to be set, such as with a WREL instruction. The nonvolatile user space write operation must include the $\overline{CS}$ pin to be brought low, the WRNUR instruction to be sent on SI, and the whole NU value clocked in (16 bits). Then the $\overline{CS}$ pin is set high. The value is stored immediately in the volatile memory. The nonvolatile user space value is not transferred to EEPROM until the next power disruption, though a Software Store can be executed at any time.

The nonvolatile user space content is then permanent only until rewritten by the user.

FIGURE 9-1: NONVOLATILE USER SPACE WRITE

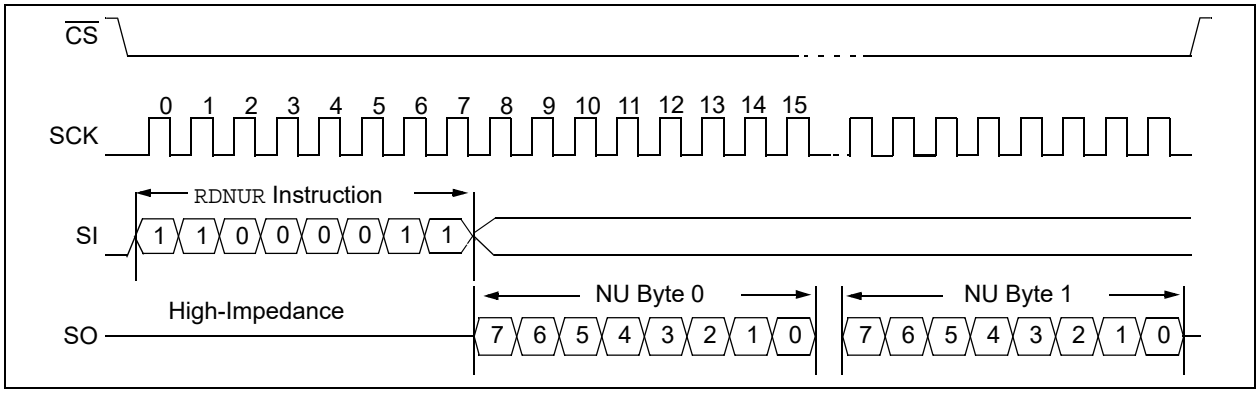


9.2 Read Nonvolatile User Space (RDNUR)

Reading the nonvolatile user space is possible with the RDNUR command. The nonvolatile user space read operation must include the $\overline{CS}$ pin to be brought low, the RDNUR instruction to be sent on SI, and the whole NU value clocked out on SO (2 bytes). Then the $\overline{CS}$ pin is set high. The value read is from the volatile SRAM memory, so this will be the last value restored from EEPROM on power-up or any new value written into these 16 bits since the last power-up.

The user can also use the Software Recall command (**Section 11.0 "Store/Recall Operations"**) to recover the nonvolatile user space content moved to EEPROM on the last power event or the last Software Store event.

FIGURE 9-2: READ NONVOLATILE USER SPACE



10.0 SECURE OPERATIONS

The 48L256 devices support secure write and read operations, which add another layer of protection to data. The secure write and read operations use a CRC checksum on a fixed number of bytes and the address bits, to be sure the data beginning at that address matches the given checksum before it is considered valid.

The 48L256 uses a 64-byte and address CRC calculation. The devices accept or transmit a 2-byte CRC value calculated from the SRAM data and address bits. Only valid address bits are used in the calculation (upper address bits that extend beyond the array size are ignored in the CRC calculation). The boundary of the secure write and read operations must align to a 64-byte boundary.

10.1 Secure Write

To enable the secure write operation, a WEL bit has to be set first. The $\overline{CS}$ line is set low, the Secure Write command is sent, followed by the address bytes. Only the valid address bits are used in the CRC calculation (see Table 10-1 below). Then, data is sent to the required number of bytes, and the expected CRC value is calculated internally as bytes are sent in. After the last byte is written, the 16-bit CRC is to be clocked in on SI, then the $\overline{CS}$ pin is set high. The CRC16-CCITT polynomial used is $x^{16}+x^{12}+x^5+1$. The boundary for the write operation must align with the size of the range, 64 bytes. The initial value for the CRC calculation is 0xFFFF. The checksum must be transmitted with MSb first. In addition, the internally calculated CRC has to match the transmitted CRC. If they match, the data will be accepted and written to the array. If the CRC values do not match, data will be ignored and the existing memory data will stay as it was and the $\overline{SWM}$ bit in the STATUS register will be set to '1', indicating a secure write error. The status of the $\overline{SWM}$ bit should be read after every secure write operation to confirm the operation was successful. The $\overline{SWM}$ bit in the STATUS register is read-only and will automatically reset to '0' at the beginning of the next secure write operation.

With the low-to-high transition of the $\overline{CS}$ pin, the device is automatically returned to the Write Disable state, with the WEL bit returning to '0'.

10.2 Secure Read

The secure read operation requires the $\overline{CS}$ pin to be brought low and the secure read opcode sent in on the SI pin. Following that is the address (2 bytes).
The valid address bits are part of the CRC calculation. Only the correct number of bits can be read, which are 64 bytes clocked out on the SO pin (see Table 10-1 for details). As the data is sent out, a CRC checksum is calculated. The CRC16-CCITT polynomial used is $x^{16}+x^{12}+x^5+1$. After the data bytes are sent, then the two CRC bytes are sent, and the master sets the $\overline{CS}$ pin high to finish the operation. The master reading the SRAM can do a CRC calculation to confirm that the address and data agree with the checksum bytes provided by the device.

The secure read must be aligned with a SRAM address boundary of 64 bytes.

The $\overline{SWM}$ bit in the STATUS register is not affected by secure read operations.

TABLE 10-1: SECURE WRITE BITS

Device	Address Bytes	Address Bits	Data Bytes Required	CRC Bits
48L256	2	15	64	16

TABLE 10-1: SECURE SRAM WRITE WAVEFORM

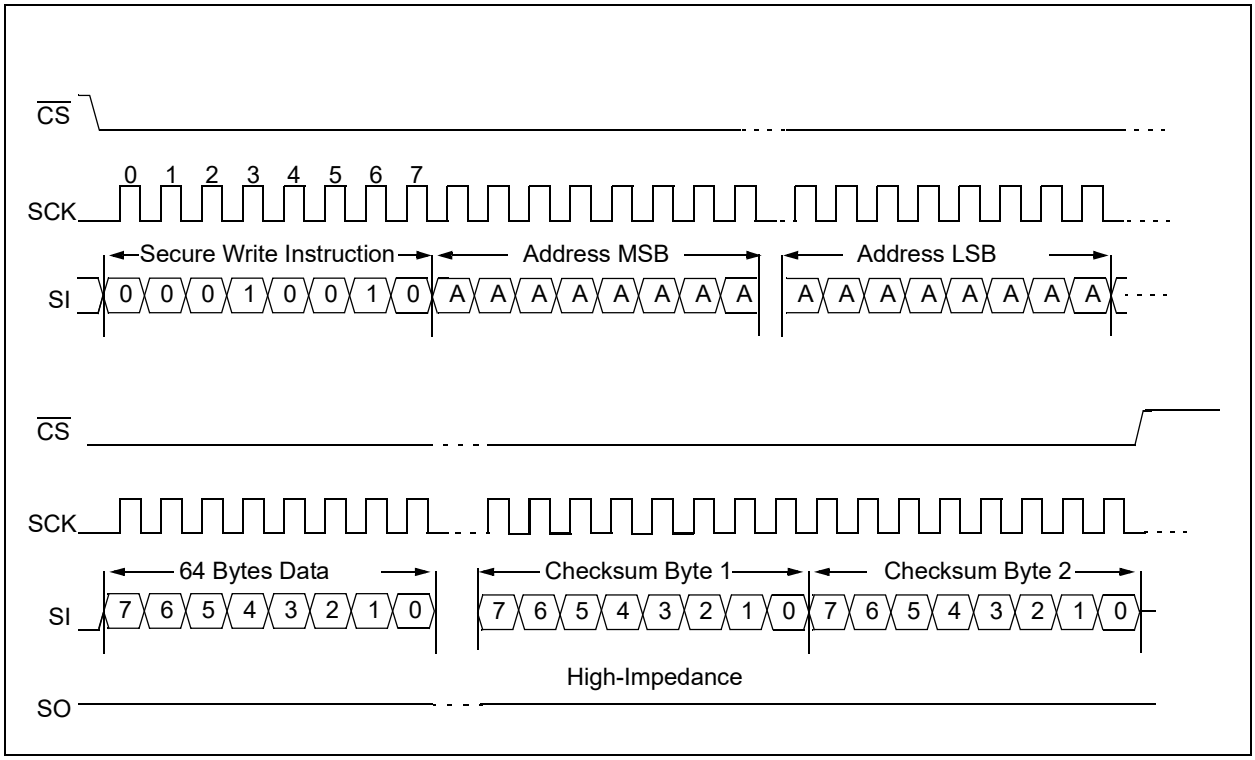
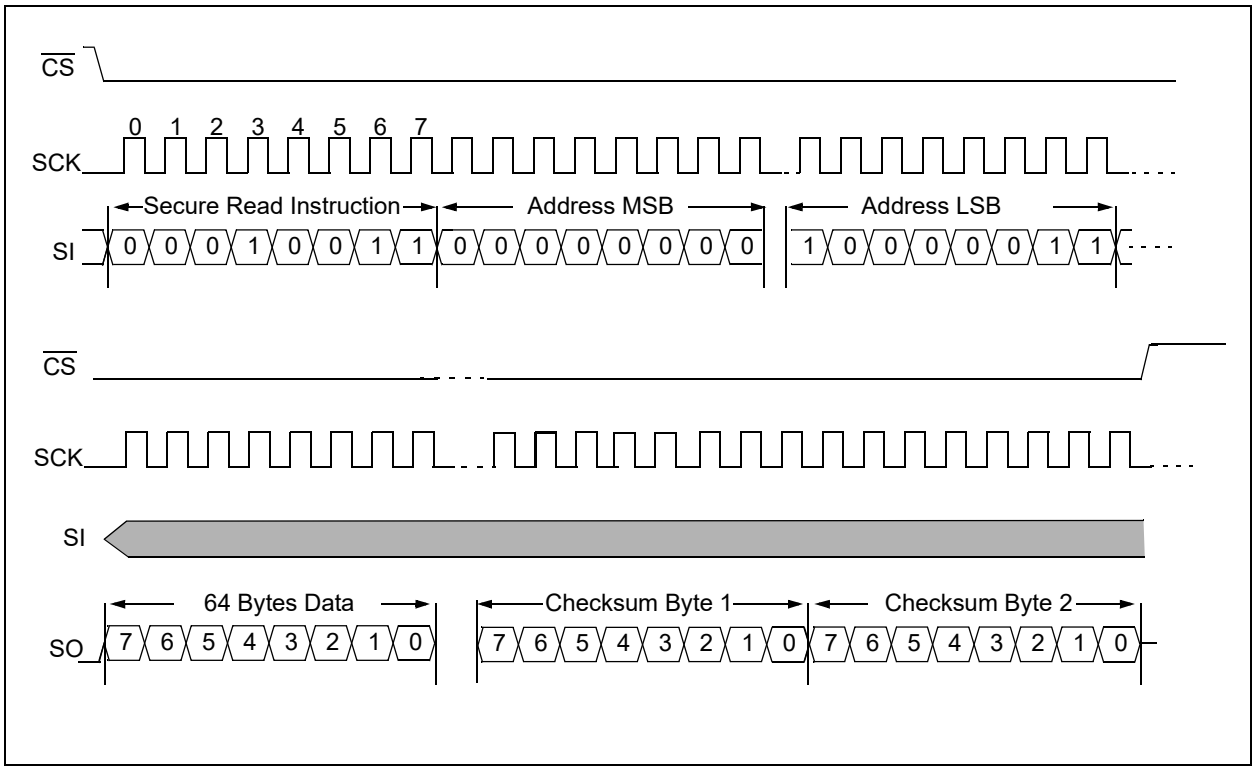


FIGURE 10-1: SECURE SRAM READ WAVEFORM



11.0 STORE/RECALL OPERATIONS

This EERAM device is intended to be serial SRAM with internal management of all backup transfers to and from EEPROM on power disruption, so the EEPROM portion of the SRAM memory cell is not directly accessible to the user.
However, user-managed Software Store and Software Recall commands are included. The factory default for the $\overline{ASE}$ bit in the STATUS register is '0', enabling the AutoStore function.

11.1 Automatic Store on Any Power Disruption

To enable this feature, the user must place a capacitor on the VCAP pin and ensure the $\overline{ASE}$ bit in the STATUS register is set to '0'. The capacitor is charged through the VCC pin. When the 48L256 detects a power-down event, the device automatically switches to the capacitor for power and initiates the AutoStore operation.

Note that to minimize the transfer events to EEPROM, this automatic store will only be initiated if the SRAM array has been modified since the last store or recall operation.

The automatic store cycle (AutoStore) is initiated when VCAP falls below VTRIP. Even if power is restored, the 48L256 cannot be accessed for TSTORE time after the AutoStore is initiated.

Note:	If power is restored during an AutoStore operation, the AutoStore will continue and the AutoRecall will not be performed because the SRAM content is still valid.

11.2 Automatic Recall to SRAM

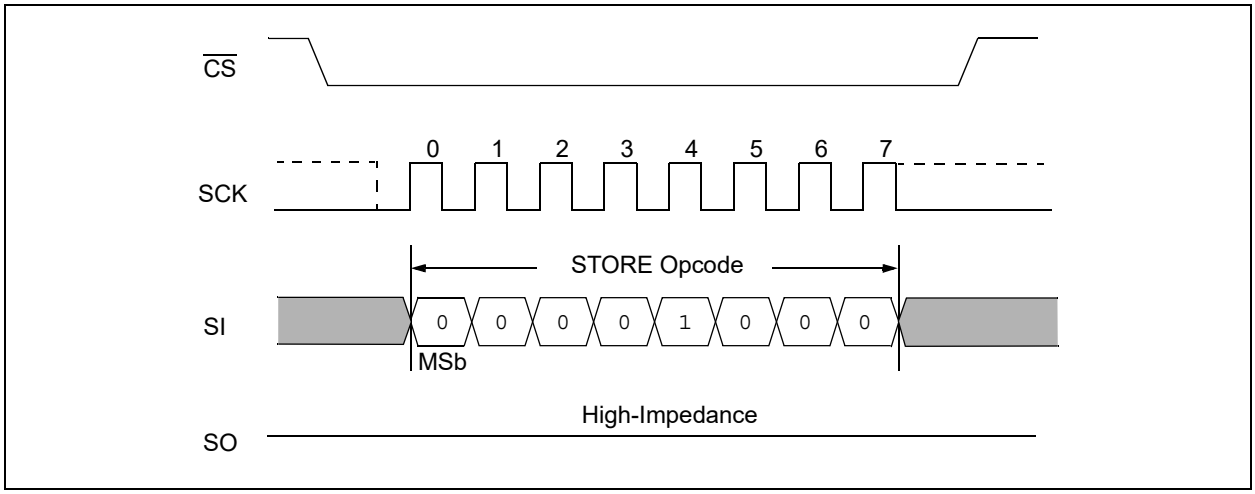
An automatic recall of EEPROM to SRAM (AutoRecall) is performed on power-up, regardless of the state of the $\overline{ASE}$ bit. This feature ensures that the SRAM data duplicates the EEPROM data on power-up. The AutoRecall is initiated when VCAP rises above VTRIP, and the 48L256 cannot be accessed for TRESTORE time after the AutoRecall is initiated.

Note 1:	If power is lost during an AutoRecall operation, the AutoRecall is aborted and the AutoStore is not performed.
2:	AutoRecall is performed every time VCAP rises above VTRIP.

11.3 Software Store Command

The Software Store command must be user-initiated and will store the contents of the SRAM bits, the nonvolatile user space and the Configuration bits of the STATUS register (BP[1:0], $\overline{PRO}$ and $\overline{ASE}$) into nonvolatile storage. The Software Store command functions even if the contents of the array and registers have not changed since the last store or recall. Reading the STATUS register during the store cycle will indicate a busy bit. Other operations will be ignored.

FIGURE 11-1: SOFTWARE STORE



11.4 Software Recall Command

The Software Recall command must be user-initiated and replaces the contents of the SRAM array, the nonvolatile user space and the Configuration bits of the STATUS register (BP[1:0], $\overline{PRO}$ and $\overline{ASE}$) from a previous store into the user corresponding user-accessible areas.

The Software Recall command can be given and the operation completed, even if the contents of the array and registers have not changed since the last store or recall. Reading the STATUS register during the recall cycle will indicate a busy bit. Other operations will be ignored.

FIGURE 11-2: SOFTWARE RECALL

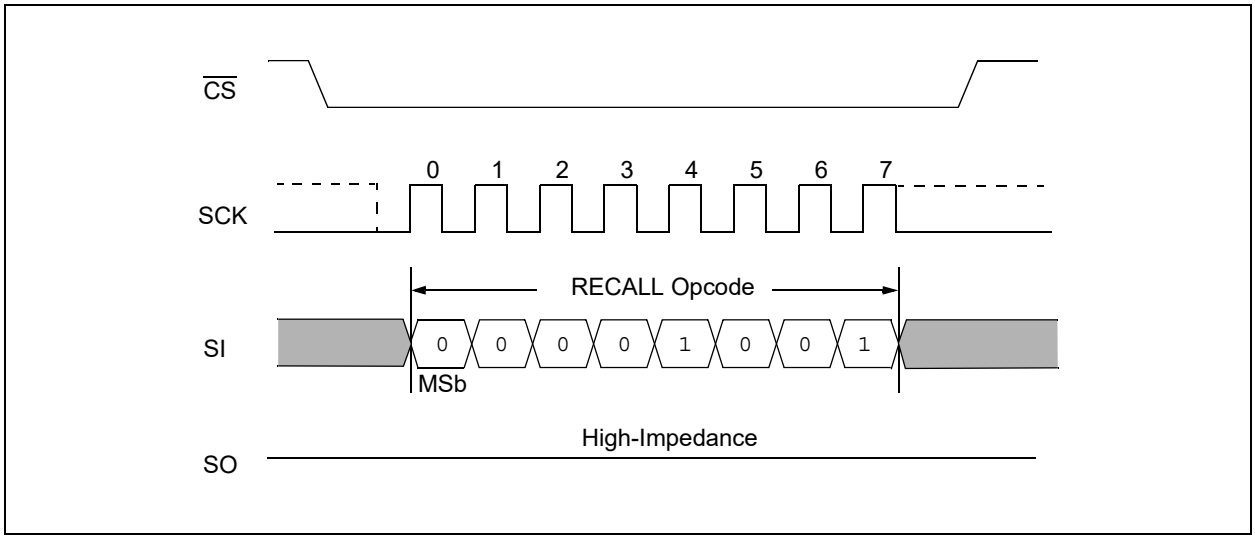


TABLE 11-1: STORE ENABLE TRUTH TABLE

$\overline{ASE}$ Bit	Array Modified	AutoStore Enabled	Software Store Enabled	AutoRecall Enabled	Software Recall Enabled
x	No	No	Yes	Yes	Yes
1	Yes	No	Yes	Yes	Yes
0	Yes	Yes	Yes	Yes	Yes

11.5 Polling Routine

When operating in the more common automatic store and recall mode (AutoStore/AutoRecall), the master can poll the RDY/BSY bit on power-up to see when the SRAM is ready for new Read/Write commands. See Figure 11-3 beginning with the "Send RDSR Instruction to the Device".

Polling can also be used if the user-initiated Software Store and Software Recall commands are used. Polling allows the application to query whether the EERAM has completed the transfer operations between the SRAM and EEPROM portions of the memory cell. This polling routine can be initiated after every power-up to confirm that AutoRecall has completed, or after the user-executed Software Store and Software Recall commands have started processing.

The polling routine is repeatedly sending the Read STATUS Register (RDSR) command to determine if the device has completed its self-timed internal store or recall cycles (see Figure 11-3). If the RDY/BSY bit = 1 from RDSR, the write cycle is still in progress. If RDY/BSY bit = 0 from RDSR, this indicates the operation has ended. If the device is still in a busy state, repeated RDSR commands can be executed until the RDY/BSY bit = 0, signaling that the device is ready to execute a new instruction.

With the 48L256 device, it is also possible to poll the busy flag by sending the RDSR command only once, and repeatedly clocking out the data until the busy bit is clear. Only the RDSR instruction is enabled during the store and recall cycles.

FIGURE 11-3: POLLING FLOW

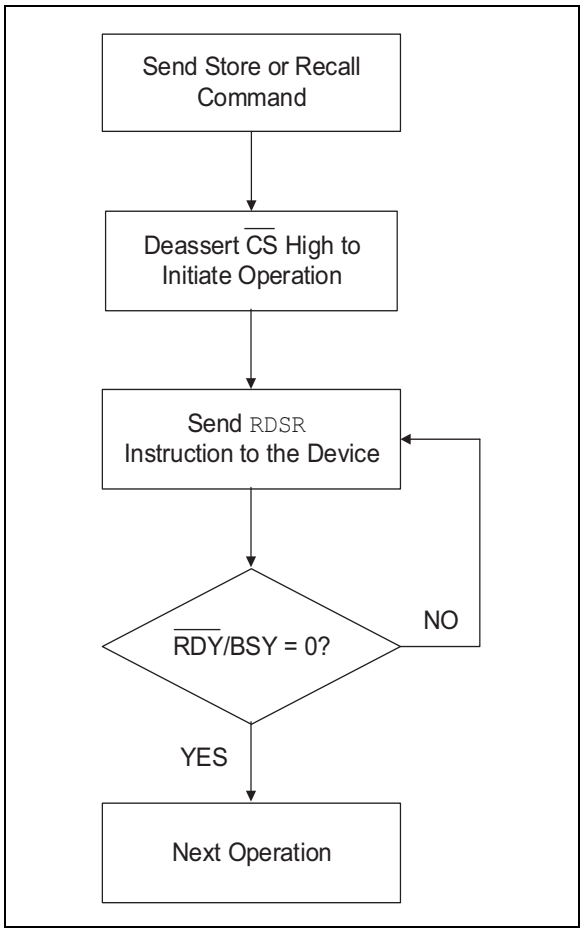
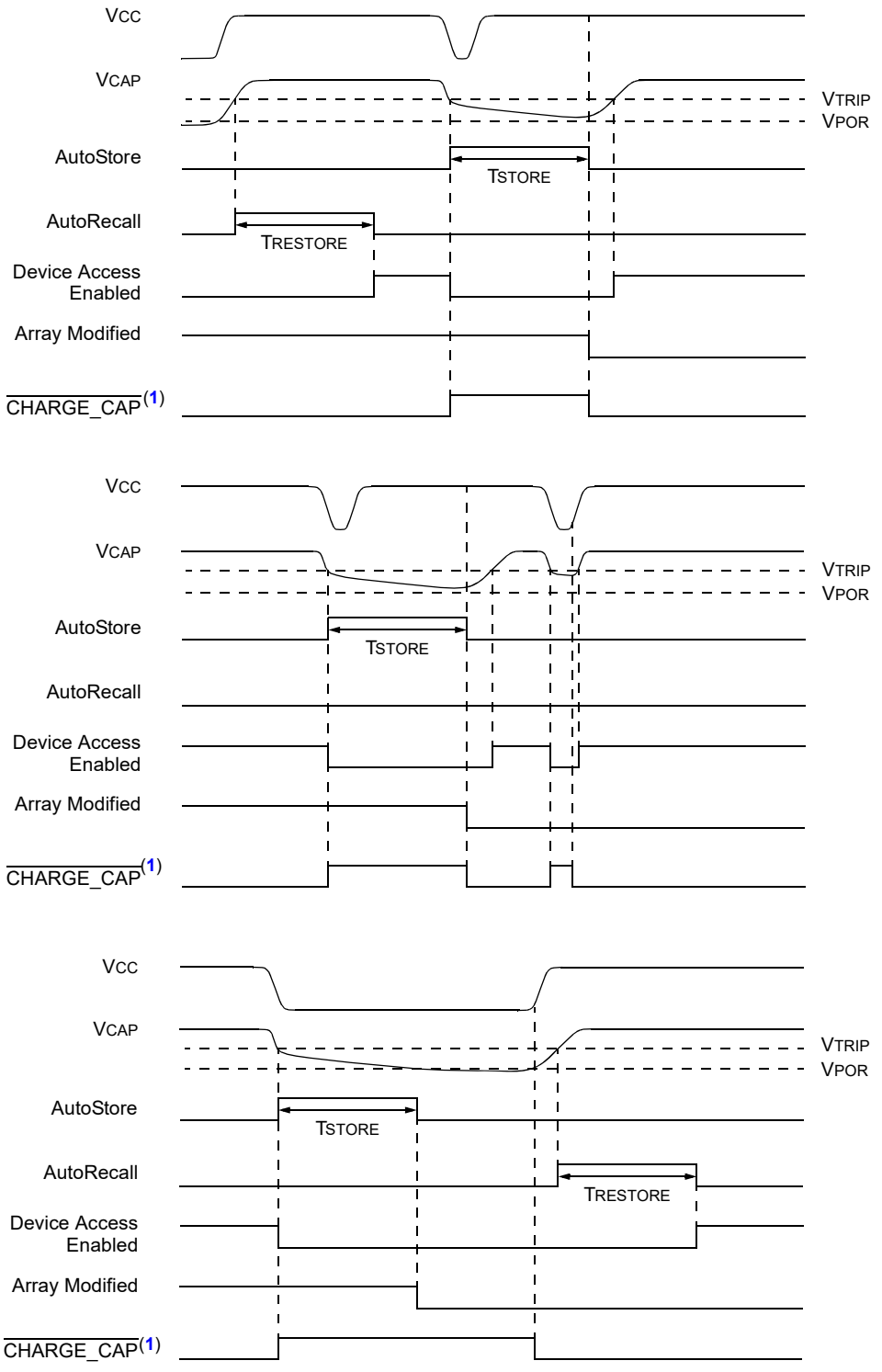
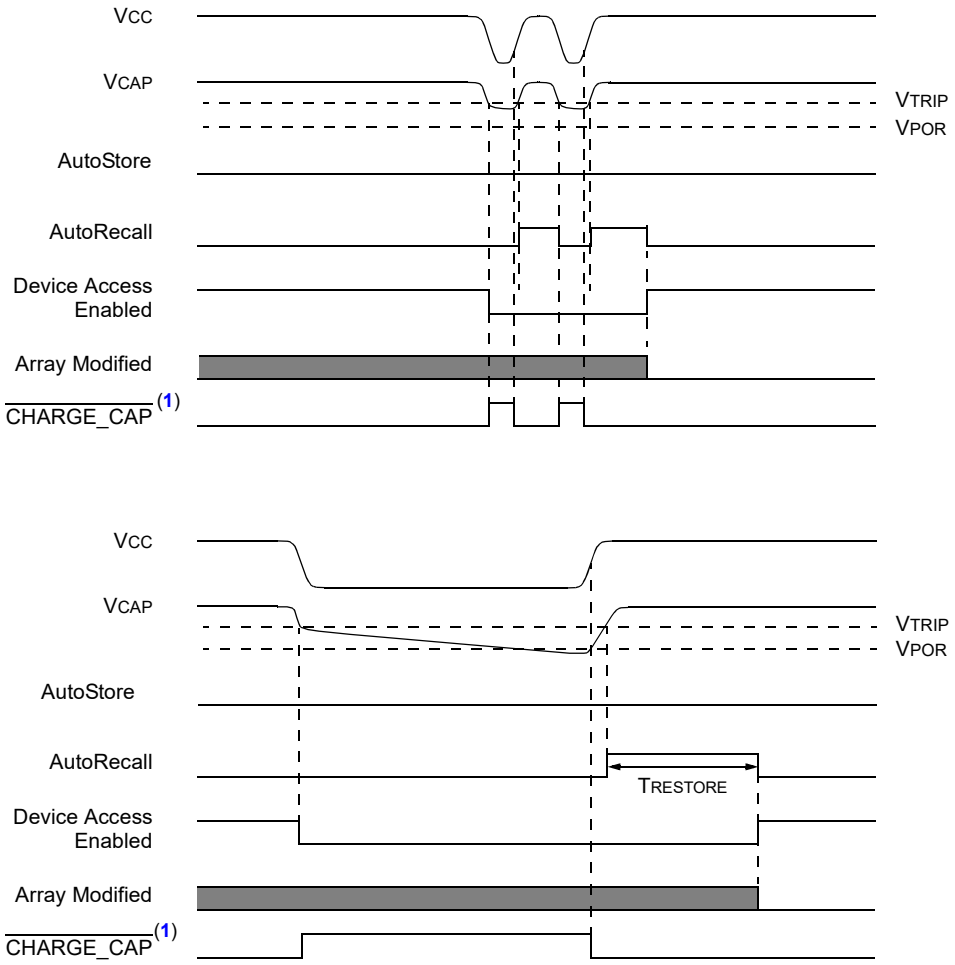


FIGURE 11-1: AUTOSTORE/AUTORECALL SCENARIOS (WITH $\overline{ASE}$ = 0, ARRAY MODIFIED)



Note 1: When $\overline{CHARGE\_CAP}$ is a '0', VCC is connected to VCAP, allowing VCC to charge the external capacitor. See **Section 13.1 "Power Switchover"** for details.

FIGURE 11-2: AUTOSTORE/AUTORECALL SCENARIOS (WITH $\overline{ASE}$ = 1 OR ARRAY NOT MODIFIED)



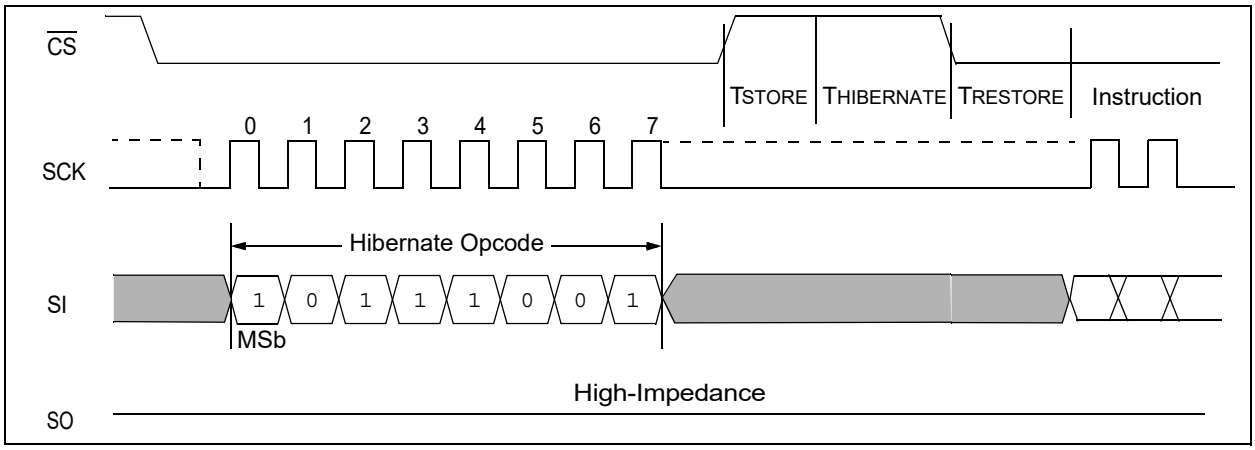
Note 1: When $\overline{CHARGE\_CAP}$ is a '0', VCC is connected to VCAP, allowing VCC to charge the external capacitor. See **Section 13.1 "Power Switchover"** for details.

12.0 HIBERNATION

The 48L256 device includes a very low-power Hibernation mode. The Hibernation mode is initiated by sending the Hibernate instruction. Once received, the $\overline{CS}$ pin returns high, the device performs a store operation if the array has been modified since the last store or recall, and then the device enters a low-power state.

Exiting the Hibernation state requires either a power cycle, or that the $\overline{CS}$ pin be brought low to begin awakening from hibernation. After a time of TRESTORE, the device will again be ready to operate. All data in the EEPROM portion of the memory cells will be transferred back to the SRAM portion of the memory cells, and the nonvolatile user space and register values will also be restored.

FIGURE 12-1: HIBERNATE WAVEFORM



13.0 TRIP VOLTAGE

The 48L256 has an internal voltage reference that is used to create a trip voltage threshold (VTRIP). When VCAP rises above VTRIP, a power-up event is detected. If this is the first power-up event after a POR, then an AutoRecall operation is initiated. When VCAP falls below VTRIP, a power-down event is detected and an AutoStore operation is initiated if the $\overline{ASE}$ in the STATUS register is set to '0' and if the array has been modified.

Note:	When VCAP is below VTRIP, the 48L256 cannot be accessed and will not respond to any commands.

13.1 Power Switchover

To support the AutoStore feature, the 48L256 must be able to charge the capacitor connected to the VCAP pin when power is available on VCC, and also automatically switch to being powered from the VCAP pin when power is removed internal to the device from VCC. Since the VCAP pin is used as part of the internal power bus, this means that the VCC pin must be disconnected internally to the device when power to the system ceases.

To accomplish this, the 48L256 has an intelligent power switchover circuit that continuously monitors the voltages on both the VCC and VCAP pins.

During a power-up event, VCC is initially connected internally in the device to the VCAP pin, allowing it to rise above the VCAP pin voltage level. Once the VCC pin voltage level is above the VCAP pin voltage level, the VCAP pin is connected to the VCC pin internally, charging the external capacitor back through the device. When the VCAP pin voltage level rises to VTRIP, the AutoRecall operation is triggered.

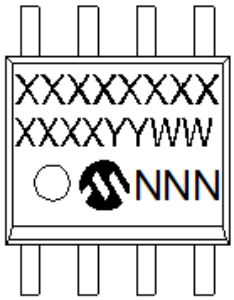
During a power-down event, the VCC pin is initially connected to the internal power bus. As Vcc falls, it discharges the external cap, causing VCAP to also fall. Once the VCAP pin voltage level falls below VTRIP, the AutoStore operation is triggered, and the VCC pin is disconnected internally to prevent discharging the external VCAP capacitor any further through the VCC pin.

Once the VCC pin is disconnected internally, it will not be reconnected until both the VCC pin voltage is greater than the VCAP pin voltage and any internal store cycles (AutoStore or Software Store) are complete. This guards against continuously internally connecting and disconnecting the VCC pin to the VCAP pin when the VCAP voltage falls faster than the VCC voltage as it moves the SRAM data to EEPROM backup.

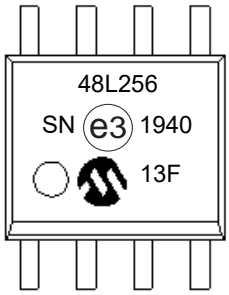
14.0 PACKAGING INFORMATION

14.1 Package Marking Information

8-Lead SOIC

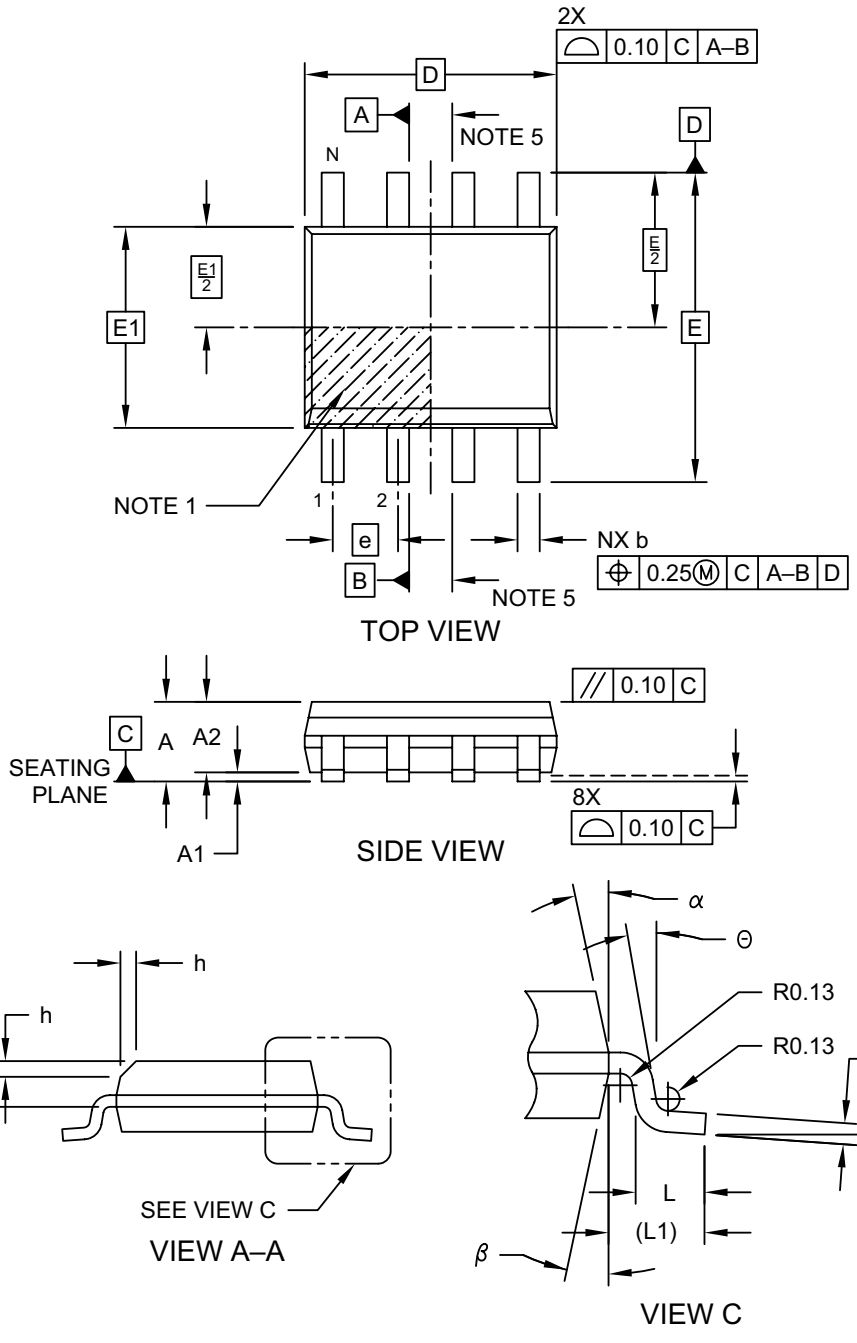


Example



8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

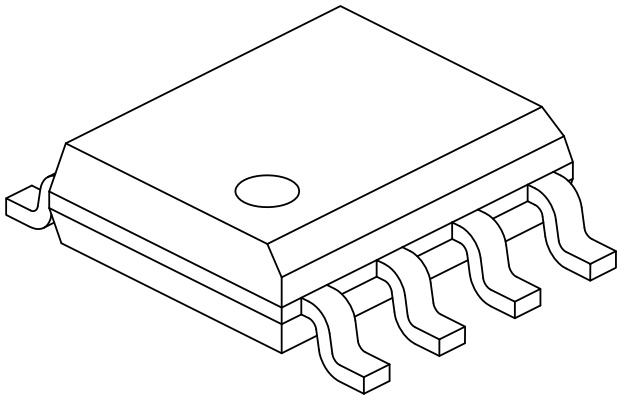
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev E Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

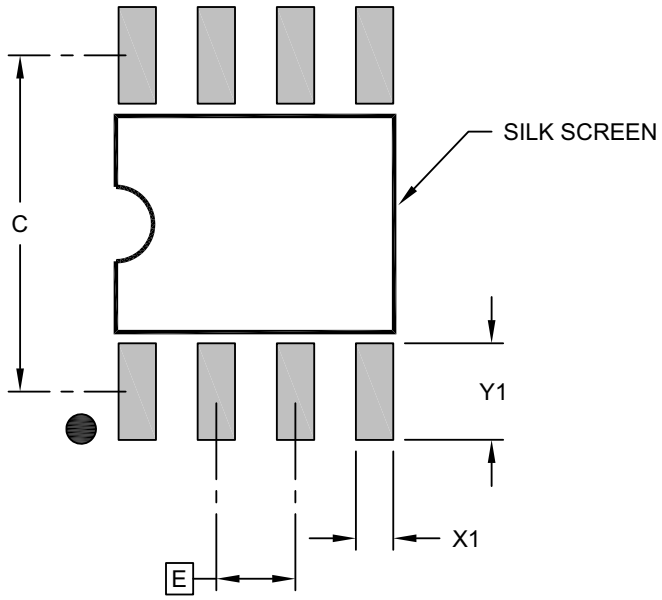
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev E Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev E

APPENDIX A: REVISION HISTORY

Revision B (10/2019)

Changed storage time maximum; added typical capacitor value; added default value setting for ASE bit.

Revision A (07/2019)

Initial release of this document.

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PART NO.	[X](1)	-X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	48L256 = 256-Kbit SPI Serial EERAM	
Tape and Reel Option:	Blank = Standard packaging (tube or tray) T = Tape and Reel(1)	
Temperature Range:	I =	-40°C to +85°C (Industrial)
Package:	SN =	8-Lead Plastic Small Outline – Narrow, 3.90 mm Body SOIC

Examples:

a) 48L256-I/SN = Industrial Temp., 2.7V-3.6V, SOIC Package.

b) 48L256T-I/SN = Tape and Reel, Industrial Temp., 2.7V-3.6V, SOIC Package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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