HV574

80-Channel 100 MHz Serial-to-Parallel Converter with Push-Pull Outputs

Features

- 5V CMOS Logic
- 80V Maximum Output Voltage
- Low-power Level Shifting
- 100 MHz Equivalent Data Rate using Four Dynamic Shift Registers
- Latched Data Outputs
- Forward and Reverse Shifting Options (DIR Pin)
- Diode to V_{PP} allows Efficient Power Recovery
- Outputs may be Hot Switched

Applications

- Display Driver
- Inkjet Driver
- Microelectromechanical Systems Applications

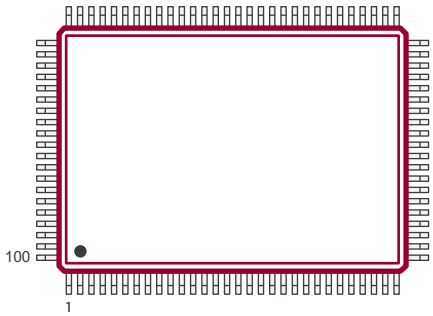
General Description

The HV574 is a low-voltage to high-voltage serial-to-parallel converter with push-pull outputs. This device is designed as a driver for printer applications. It can also be used in any application requiring multiple-output high-voltage current sourcing-and-sinking capability such as driving plasma panels, vacuum fluorescent displays and large matrix LCD displays.

The device has four parallel 20-bit dynamic Shift registers, permitting data rates four times the speed of one in a single clock cycle. There are 80 static latches and control logic to perform the polarity select and blanking of the outputs. $HV_{OUT}1$ is connected to the first stage of the first Shift register through the polarity and blanking logic. Data is shifted through the Shift registers on the logic low-to-high transition of the clock. The DIR pin causes counter-clockwise shifting when connected to GND and clockwise shifting when connected to V_{DD}. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the Shift register, $HV_{OUT}80$. The operation of the Shift register is not affected by the latch enable ($\overline{LE}$), blanking ($\overline{BL}$) and polarity ($\overline{POL}$) inputs. Transfer of data from the Shift registers to the latches occurs when the $\overline{LE}$ input is high. The data in the latches is stored when $\overline{LE}$ is low.

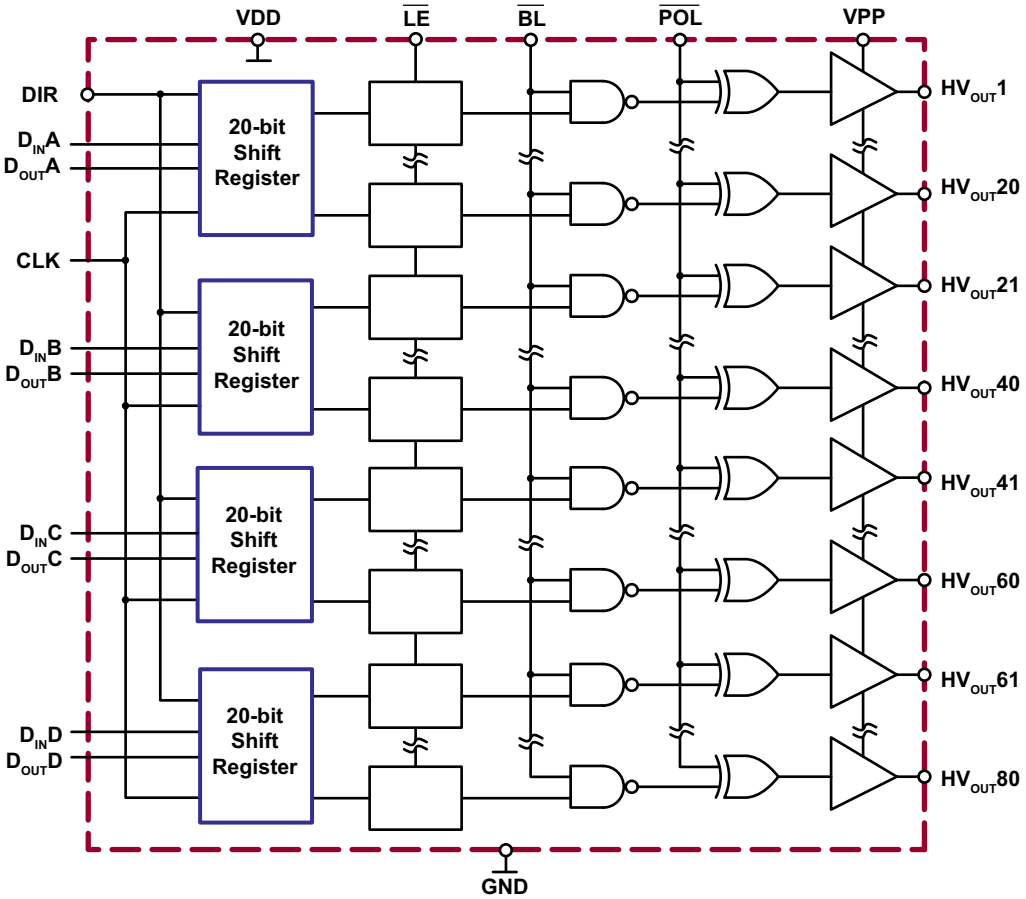
Package Type

100-lead PQFP
(Top view)

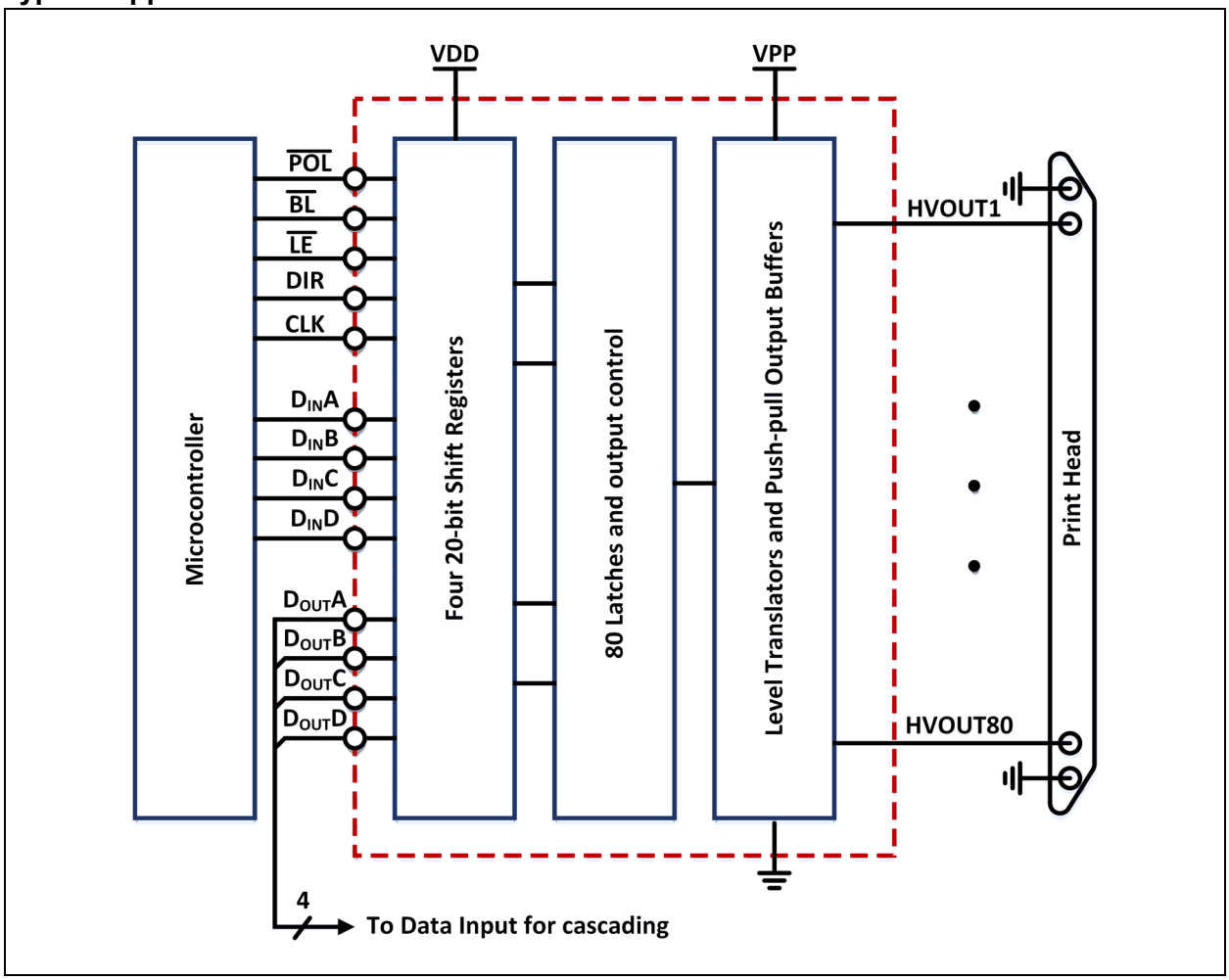


See Table 2-1 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Low-voltage Supply Voltage, V_{DD} ..... –0.5V to +7.5V
High-voltage Supply Voltage, V_{PP} ..... –0.5V to +90V
Logic Input Levels ..... –0.3V to V_{DD} +0.3V
Ground Current (**Note 1**) 1.5A
Maximum Junction Temperature, $T_{J(MAX)}$ ..... +125°C
Storage Temperature, T_S ..... –65°C to +150°C
Continuous Total Power Dissipation:
100-lead PQFP (**Note 2**) ..... 1200 mW

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Limited by the total power dissipated in the package
2: For operations above 25°C ambient, derate linearly to 85°C at 20 mW/°C.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply Voltage	V_{DD}	4.5	—	5.5	V	
Output Voltage	V_{PP}	12	—	80	V	
High-level Input Voltage	V_{IH}	V_{DD}–0.5V	—	—	V	
Low-level Input Voltage	V_{IL}	0	—	0.5	V	
Clock Frequency per Register	f_{CLK}	0.001	—	25	MHz	
Operating Ambient Temperature	T_A	–40	—	+85	°C	

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions unless otherwise noted							
Parameter		**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
V_{DD} Supply Current		I_{DD}	—	—	30	mA	$V_{DD} = V_{DD}$ maximum f_{CLK} = 25 MHz
Quiescent V_{PP} Supply Current		I_{PP}	—	—	100	µA	Outputs high
			—	—	100	µA	Outputs low
Quiescent V_{DD} Supply Current		I_{DDQ}	—	—	100	µA	All $V_{IN} = V_{DD}$
High-level Output	HV_{OUT}	V_{OH}	V_{PP}–9	—	—	V	I_O = –30 mA, V_{PP} = +80V
	Data Out		V_{DD}–0.5	—	—	V	I_O = –100 µA
Low-level Output	HV_{OUT}	V_{OL}	—	—	3.75	V	I_O = +15 mA, V_{DD} = +5V
	Data Out		—	—	0.5	V	I_O = +100 µA
High-level Logic Input Current		I_{IH}	—	—	1	µA	$V_{IH} = V_{DD}$
Low-level Logic Input Current		I_{IL}	—	—	–1	µA	V_{IL} = 0V

AC ELECTRICAL CHARACTERISTICS

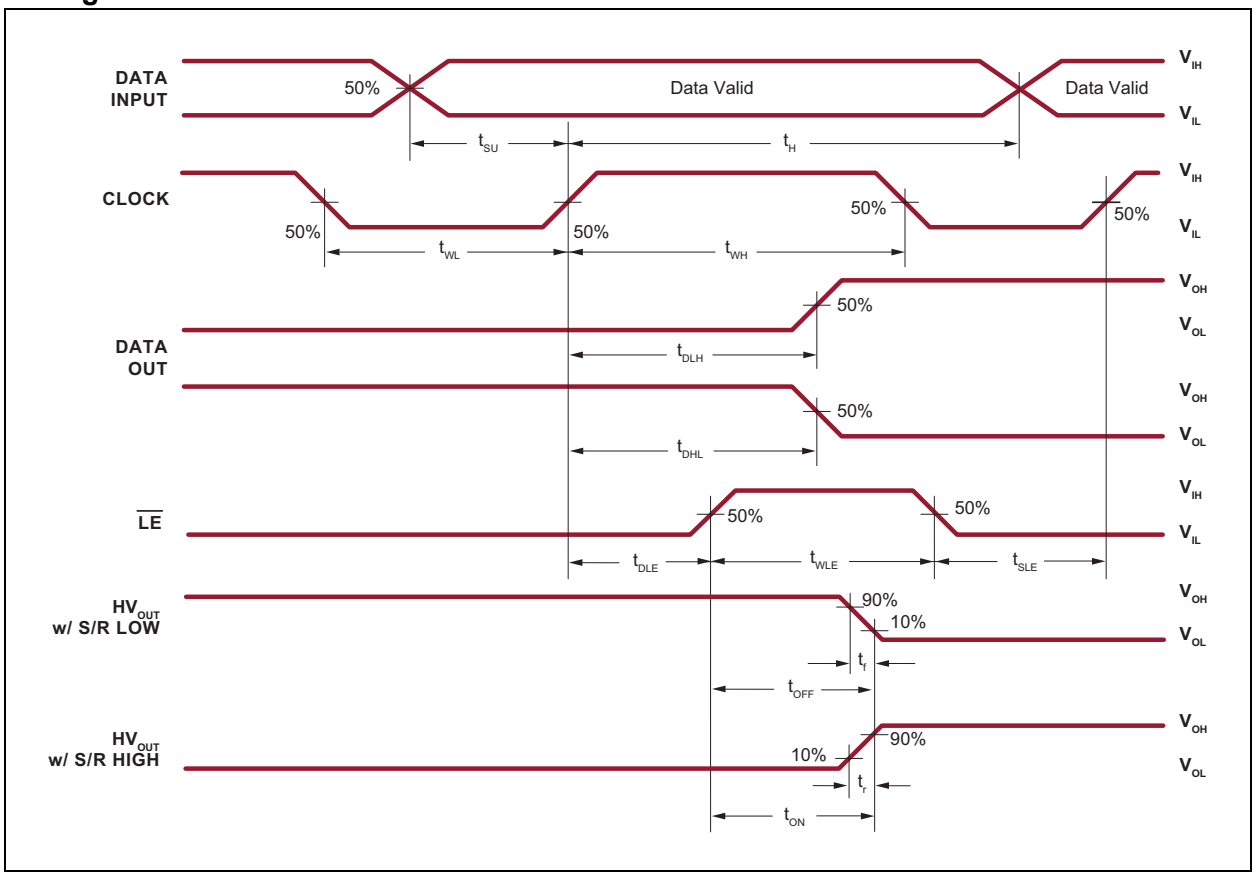
Electrical Specifications: T_A = 85°C maximum. Logic signal inputs and data inputs have t_r, $t_f \leq$ 5 ns (10% and 90% points).						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Clock Frequency	f_{CLK}	0.001	—	25	MHz	V_{DD} = 4.5V, T_J = 25°C
		0.001	—	20	MHz	V_{DD} = 4.5V, T_J = 125°C
Clock Width High or Low	t_{WL}, t_{WH}	20	—	—	ns	
Data Set-up Time before Clock Rises	t_{SU}	0	—	—	ns	
Data Hold Time after Clock Rises	t_H	15	—	—	ns	
Time from Latch Enable to HV_{OUT}	t_{ON}, t_{OFF}	—	—	500	ns	C_L = 15 pF
Latch Enable Pulse Width	t_{WLE}	25	—	—	ns	
Delay Time Clock to Latch Enable Low to High	t_{DLE}	25	—	—	ns	**Note 1**
Latch Enable Set-up Time before Clock Rises	t_{SLE}	0	—	—	ns	
Delay Time Clock to Data Low to High	t_{DLH}	—	—	38	ns	C_L = 15 pF, V_{DD} = 5V
Delay Time Clock to Data High to Low	t_{DHL}	—	—	38	ns	C_L = 15 pF, V_{DD} = 5V
Output Rise and Fall Time	t_r, t_f	—	—	1	ns	C_L = 600 pF, HV_{OUT} from 0V–60V

Note 1: t_{DLE} is not required but is recommended to produce stable HV outputs and minimize power dissipation and current spikes. t_{DLE} allows the internal SR output to stabilize.

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–40	—	+85	°C	
Maximum Junction Temperature	$T_{J(MAX)}$	—	—	+125	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
100-lead PQFP	θ_{JA}	—	39	—	°C/W	

Timing Waveforms



2.0 PIN DESCRIPTION

The details on the pins of HV574 are listed on Table 2-1. Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HVOUT30	High-voltage output
2	HVOUT29	High-voltage output
3	HVOUT28	High-voltage output
4	HVOUT27	High-voltage output
5	HVOUT26	High-voltage output
6	HVOUT25	High-voltage output
7	HVOUT24	High-voltage output
8	HVOUT23	High-voltage output
9	HVOUT22	High-voltage output
10	HVOUT21	High-voltage output
11	HVOUT20	High-voltage output
12	HVOUT19	High-voltage output
13	HVOUT18	High-voltage output
14	HVOUT17	High-voltage output
15	HVOUT16	High-voltage output
16	HVOUT15	High-voltage output
17	HVOUT14	High-voltage output
18	HVOUT13	High-voltage output
19	HVOUT12	High-voltage output
20	HVOUT11	High-voltage output
21	HVOUT10	High-voltage output
22	HVOUT9	High-voltage output
23	HVOUT8	High-voltage output
24	HVOUT7	High-voltage output
25	HVOUT6	High-voltage output
26	HVOUT5	High-voltage output
27	HVOUT4	High-voltage output
28	HVOUT3	High-voltage output
29	HVOUT2	High-voltage output
30	HVOUT1	High-voltage output
31	NC	No connection
32	VPP	High-voltage supply pin
33	HVGND	High-voltage supply ground
34	DINA	Data Input A pin
35	DINB	Data Input B pin
36	DINC	Data Input C pin

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
37	DIND	Data Input D pin
38	VDD	Low-voltage supply pin
39	$\overline{POL}$	Polarity pin
40	$\overline{LE}$	Latch Enable pin
41	CLK	Clock pin
42	DIR	Direction pin
43	$\overline{BL}$	Blanking pin
44	GND	Low-voltage supply ground
45	DOUTD	Data Output D pin
46	DOUTC	Data Output C pin
47	DOUTB	Data Output B pin
48	DOUTA	Data Output A pin
49	HVGND	High-voltage supply ground
50	VPP	High-voltage supply pin
51	HVOUT80	High-voltage output
52	HVOUT79	High-voltage output
53	HVOUT78	High-voltage output
54	HVOUT77	High-voltage output
55	HVOUT76	High-voltage output
56	HVOUT75	High-voltage output
57	HVOUT74	High-voltage output
58	HVOUT73	High-voltage output
59	HVOUT72	High-voltage output
60	HVOUT71	High-voltage output
61	HVOUT70	High-voltage output
62	HVOUT69	High-voltage output
63	HVOUT68	High-voltage output
64	HVOUT67	High-voltage output
65	HVOUT66	High-voltage output
66	HVOUT65	High-voltage output
67	HVOUT64	High-voltage output
68	HVOUT63	High-voltage output
69	HVOUT62	High-voltage output
70	HVOUT61	High-voltage output
71	HVOUT60	High-voltage output
72	HVOUT59	High-voltage output
73	HVOUT58	High-voltage output
74	HVOUT57	High-voltage output
75	HVOUT56	High-voltage output
76	HVOUT55	High-voltage output

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
77	HVOUT54	High-voltage output
78	HVOUT53	High-voltage output
79	HVOUT52	High-voltage output
80	HVOUT51	High-voltage output
81	HVOUT50	High-voltage output
82	HVOUT49	High-voltage output
83	HVOUT48	High-voltage output
84	HVOUT47	High-voltage output
85	HVOUT46	High-voltage output
86	HVOUT45	High-voltage output
87	HVOUT44	High-voltage output
88	HVOUT43	High-voltage output
89	HVOUT42	High-voltage output
90	HVOUT41	High-voltage output
91	HVOUT40	High-voltage output
92	HVOUT39	High-voltage output
93	HVOUT38	High-voltage output
94	HVOUT37	High-voltage output
95	HVOUT36	High-voltage output
96	HVOUT35	High-voltage output
97	HVOUT34	High-voltage output
98	HVOUT33	High-voltage output
99	HVOUT32	High-voltage output
100	HVOUT31	High-voltage output

3.0 FUNCTIONAL DESCRIPTION

Follow the steps in Table 3-1 to power up and power down the HV574.

TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE

Power-up		Power-down	
Step	**Description**	**Step**	**Description**
1	Connect ground.	1	Remove V_{PP}. (**Note 1**)
2	Apply V_{DD}.	2	Remove all inputs.
3	Set all inputs (Data, CLK, Enable, etc.) to a known state.	3	Remove V_{DD}.
4	Apply V_{PP}. (**Note 1**)	4	Disconnect ground.

Note 1: The V_{PP} should not drop below V_{DD} or float during operation.

TABLE 3-2: TRUTH FUNCTION TABLE

Function	Inputs						Outputs		
	Data	**CLK**	**$\overline{LE}$**	**$\overline{BL}$**	**$\overline{POL}$**	**DIR**	**Shift Register**	**High-voltage Output**	**Data Out**
All O/P High	X	X	X	L	L	X	—	H	—
All O/P Low	X	X	X	L	H	X	—	L	—
O/P Normal	X	X	X	H	H	X	—	No inversion	—
O/P Inverted	X	X	X	H	L	X	—	Inversion	—
Data Falls through Latches (Latches Transparent)	L	↑	H	H	H	X	L	L	—
	H	↑	H	H	H	X	H	H	—
	L	↑	H	H	L	X	L	H	—
	H	↑	H	H	L	X	H	L	—
Data Stored/Latches Loaded	X	X	L	H	H	X	*	Stored data	—
	X	X	L	H	L	X	*	Inversion of stored data	—
I/O Relation	$D_{IN}X$	↑	H	H	H	H	$Q_n \rightarrow Q_{n+1}$	New H or L	$D_{OUT}X$
	$D_{IN}X$	↑	L	H	H	H	$Q_n \rightarrow Q_{n+1}$	Previous H or L	$D_{OUT}X$
	$D_{OUT}X$	↑	L	H	H	L	$Q_n \rightarrow Q_{n-1}$	Previous H or L	$D_{IN}X$
	$D_{OUT}X$	↑	H	H	H	L	$Q_n \rightarrow Q_{n-1}$	New H or L	$D_{IN}X$

Note: H = High-logic level
L = Low-logic level
X = Irrelevant
↑ = Low-to-high transition
* = Dependent on the previous stage's state. See **Package Type** for D_{IN} and D_{OUT} pin designation for clockwise and counter-clockwise shifts.

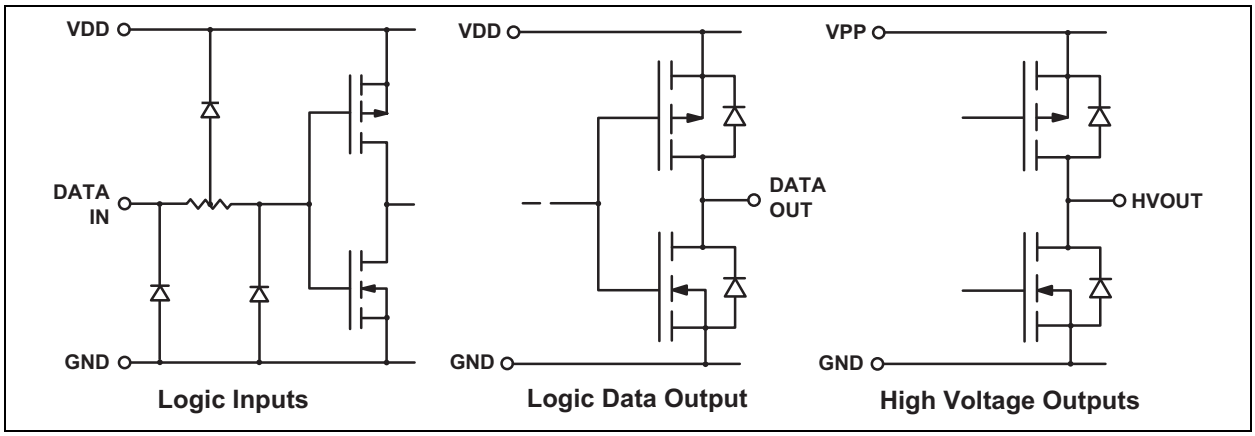
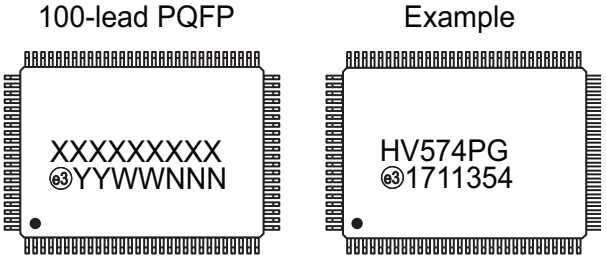


FIGURE 3-1: *Input and Output Equivalent Circuits.*

4.0 PACKAGE MARKING INFORMATION

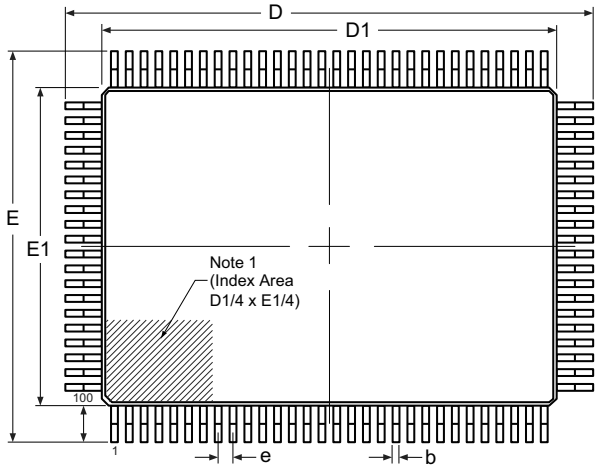
4.1 Packaging Information



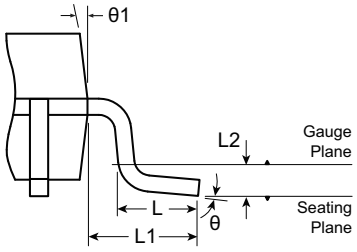
Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

100-Lead PQFP Package Outline (PG)

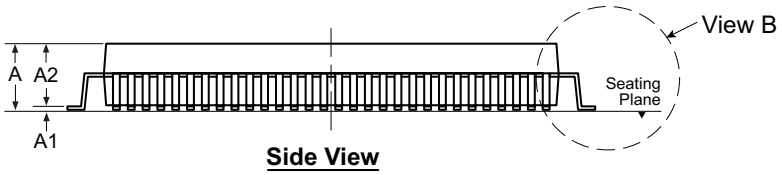
20.00x14.00mm body, 3.40mm height (max), 0.65mm pitch, 3.90mm footprint



Top View



View B



Side View

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.80*	0.25	2.55	0.22	23.65*	19.80*	17.65*	13.80*	0.65 BSC	0.73	1.95 REF	0.25 BSC	0	5°
	NOM	-	-	2.80	-	23.90	20.00	17.90	14.00		0.88			3.5°	-
	MAX	3.40	0.50*	3.05	0.38	24.15*	20.20*	18.15*	14.20*		1.03			7°	16°

JEDEC Registration MO-112, Variation CC-1, Issue B, Sept.1995.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2017)

- Converted Supertex Doc # DSFP-HV574 to Microchip DS20005859A
- Removed “HVCMOS® Technology” in the Features section
- Changed the package marking format
- Made minor changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV574	=	80-Channel 100 MHz Serial-to-Parallel Converter with Push-Pull Outputs
Package:	PG	=	100-lead PQFP
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	66/Tray for a PG Package

Example:

a) HV574PG-G:	80-Channel 100 MHz Serial-to-Parallel Converter with Push-Pull Outputs, 100-lead PQFP, 66/Tray

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