MIC45208-1/-2

26V, 10A DC-to-DC Power Module

Features

- No Compensation Required
- Up to 10A Output Current
- >93% Peak Efficiency
- Output Voltage: 0.8V to 0.85*V_{IN} with ±1% Accuracy
- Adjustable Switching Frequency from 200 kHz to 600 kHz
- Enable Input and Open-Drain Power Good (PG) Output
- Hyper Speed Control® (MIC45208-2) Architecture enables Fast Transient Response
- HyperLight Load® (MIC45208-1) improves Light Load Efficiency
- Supports Safe Start-up into Pre-Biased Output
- –40 C to +125°C Junction Temperature Range
- Thermal Shutdown Protection
- Short-Circuit Protection with Hiccup mode
- Adjustable Current Limit
- Available in 52-Pin 10 mm x 10 mm x 4 mm QFN Package

Applications

- High-Power Density Point-of-Load (POL) Conversion
- Servers, Routers, Networking and Base Stations
- FPGAs, DSP and Low-Voltage ASIC Power Supplies
- Industrial and Medical Equipment

General Description

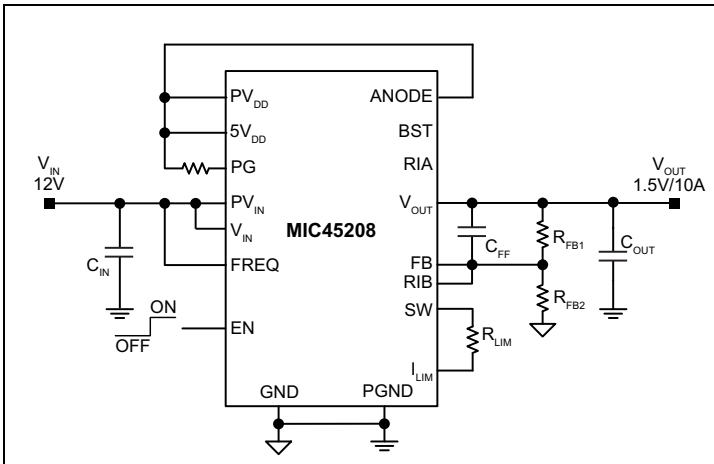
The MIC45208-1/-2 is a synchronous, step-down regulator module, featuring a unique adaptive ON-time control architecture. The module incorporates a DC-to-DC controller, power MOSFETs, bootstrap diode, bootstrap capacitor and an inductor in a single package, simplifying the design and layout process for the end user.

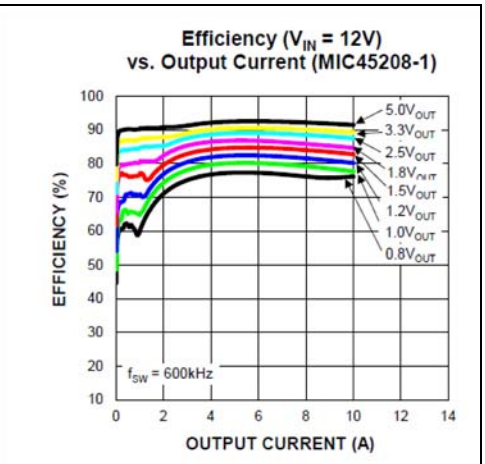
This highly integrated solution expedites system design and improves product time-to-market. The internal MOSFETs and inductor are optimized to achieve high efficiency at a low-output voltage. The fully optimized design can deliver up to 10A current under a wide input voltage range of 4.5V to 26V, without requiring additional cooling.

The MIC45208-1 uses the HyperLight Load (HLL) while the MIC45208-2 uses Hyper Speed Control (HSC) architecture, which enables ultra-fast load transient response, allowing for a reduction of output capacitance. The MIC45208 offers 1% output accuracy that can be adjusted from 0.8V to 0.85*V_{IN} with two external resistors. Additional features include thermal shutdown protection, input undervoltage lockout, adjustable current limit and short-circuit protection. The MIC45208 allows for safe start-up into a pre-biased output.

Data sheet and other support documentation can be found on the Microchip web site at: www.microchip.com.

Typical Application Schematic





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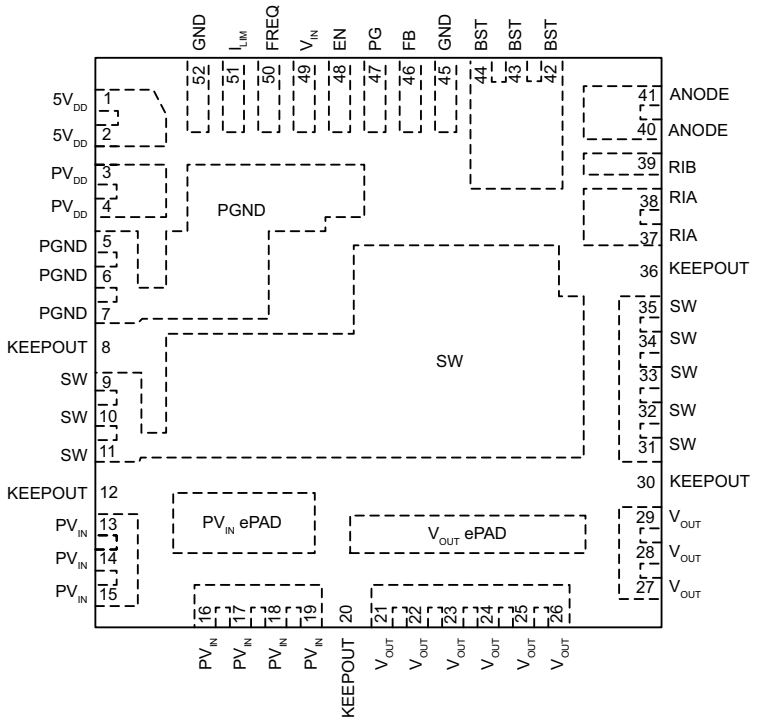
Package Types

MIC45208-1/-2
52-Pin 10 mm x 10 mm QFN (MP)
(Top View)



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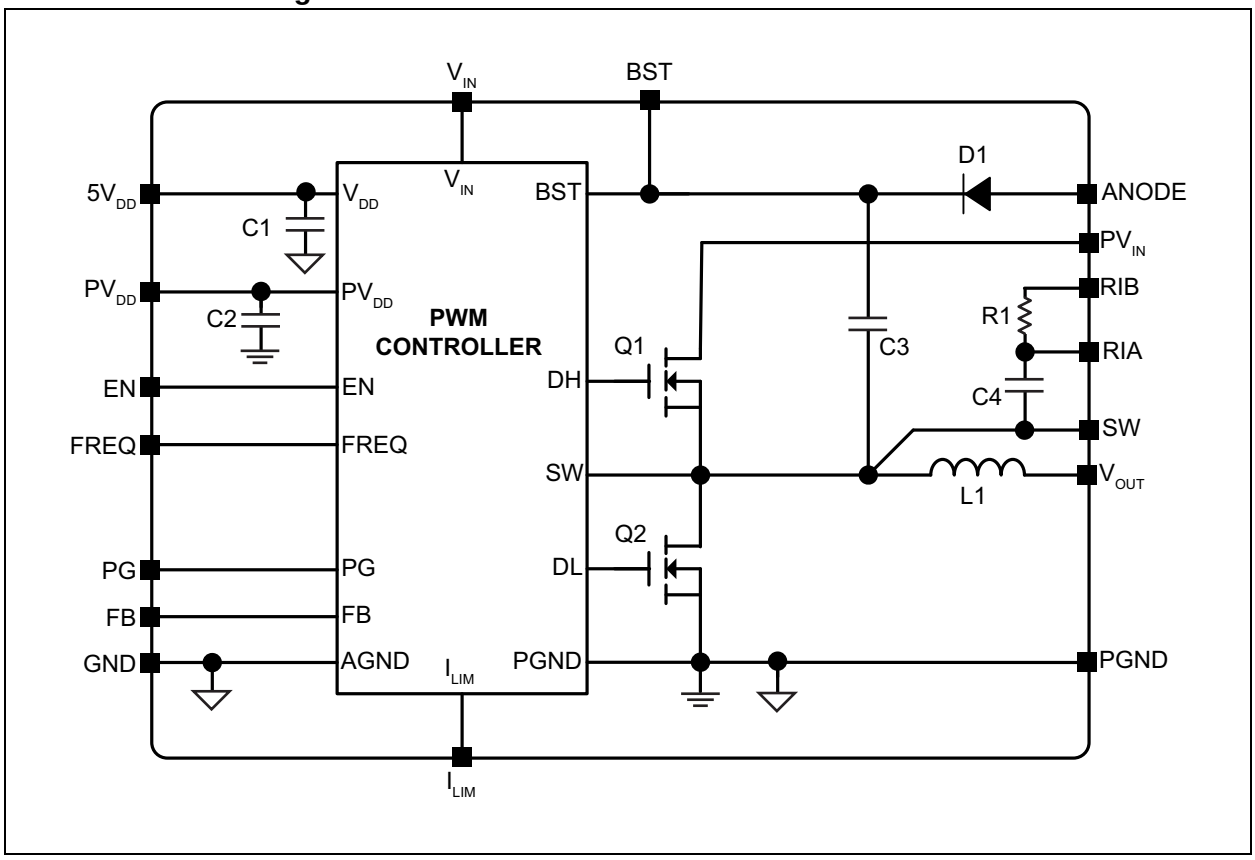
Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{PVIN}, V_{VIN} to PGND ..... –0.3V to +30V
V_{PVDD}, V_{5VDD}, V_{ANODE} to PGND ..... –0.3V to +6V
V_{SW}, V_{FREQ}, V_{ILIM}, V_{EN} to PGND ..... –0.3V to (V_{IN} + 0.3V)
V_{BST} to V_{SW} ..... –0.3V to +6V
V_{BST} to PGND ..... –0.3V to +36V
V_{PG} to PGND ..... –0.3V to (5 V_{DD} + 0.3V)
V_{FB}, V_{RIB} to PGND ..... –0.3V to (5 V_{DD} + 0.3V)
PGND to GND ..... –0.3V to +0.3V
Junction Temperature ..... +150°C
Storage Temperature (T_S) ..... –65°C to +150°C
Lead Temperature (soldering, 10s) ..... +260°C
ESD Rating ..... ESD Sensitive

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Operating Ratings[1]

Supply Voltage (V_{PVIN}, V_{VIN}) ..... 4.5V to 26V
Output Current 10A
Enable Input (V_{EN}) ..... 0V to V_{IN}
Power-Good (V_{PG}) ..... 0V to 5V_{DD}
Junction Temperature (T_J) ..... –40°C to +125°C
Junction Thermal Resistance[2]
10 mm x 10 mm x 4 mm QFN-52 (θ_{JA}) ..... 16.6°C/W
10 mm x 10 mm 4 mm QFN-52 (θ_{JC}) ..... 4°C/W

Note 1: The device is not ensured to function outside the operating range.
2: θ_{JA} and θ_{JC} were measured using the MIC45208 evaluation board.

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TABLE 1-1: ELECTRICAL CHARACTERISTICS[1]

Electrical Specifications: unless otherwise specified, $PV_{IN} = V_{IN} = V_{EN} = 12V$; $V_{OUT} = 3.3V$; $V_{BST} – V_{SW} = 5V$; $T_J = +25°C$. **Boldface** values indicate $–40°C \le T_J \le +125°C$.

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Power Supply Input						
V_{IN}, PV_{IN}	Input Voltage Range	**4.5**	—	**26**	V	—
I_Q	Quiescent Supply Current (MIC45208-1)	—	—	**0.75**	mA	$V_{FB} = 1.5V$
I_Q	Quiescent Supply Current (MIC45208-2)	—	2.1	**3**	mA	$V_{FB} = 1.5V$
I_{IN}	Operating Current: MIC45208-1	—	0.4	—	mA	$V_{PVIN} = V_{IN} = 12V$, $V_{OUT} = 1.8V$, $I_{OUT} = 0A$, $f_{SW} = 600$ kHz
	MIC45208-2	—	43	—		
I_{SHDN}	Shutdown Supply Current	—	4	**10**	µA	SW = Unconnected, $V_{EN} = 0V$
$5V_{DD}$ Output						
V_{DD}	$5V_{DD}$ Output Voltage	**4.8**	5.1	**5.4**	V	$V_{IN} = 7V$ to 26V, $I_{5VDD} = 10$ mA
UVLO	$5V_{DD}$ UVLO Threshold	**3.8**	4.2	**4.6**	V	V_{5VDD} Rising
UVLO_HYS	$5V_{DD}$ UVLO Hysteresis	—	400	—	mV	V_{5VDD} Falling
$V_{DD(LR)}$	LDO Load Regulation	0.6	2	3.6	%	$I_{5VDD} = 0$ to 40 mA
Reference						
V_{FB}	Feedback Reference Voltage	0.792	0.8	0.808	V	$T_J = +25°C$
		0.784	0.8	**0.816**		$–40°C \le T_J \le +125°C$
I_{FB_BIAS}	Feedback Bias Current	—	5	**500**	nA	$V_{FB} = 0.8V$
Enable Control						
EN_{HIGH}	EN Logic Level High	**1.8**	—	—	V	—
EN_{LOW}	EN Logic level Low	—	—	**0.6**	V	—
EN_{HYS}	EN Hysteresis	—	200	—	mV	—
I_{ENBIAS}	EN Bias Current	—	5	**10**	µA	$V_{EN} = 12V$
Oscillator						
f_{SW}	Switching Frequency	**400**	600	**750**	kHz	$V_{FREQ} = V_{IN}$, $I_{OUT} = 2A$
		—	350	—		$V_{FREQ} = 50\%\ V_{IN}$, $I_{OUT} = 2A$
D_{MAX}	Maximum Duty Cycle	—	85	—	%	—
D_{MIN}	Minimum Duty Cycle	—	0	—	%	$V_{FB} = 1V$
$t_{OFF(MIN)}$	Minimum OFF-Time	140	200	260	ns	—
Soft Start						
t_{SS}	Soft Start Time	—	3	—	ms	FB from 0V to 0.8V
Short-Circuit Protection						
V_{CL_OFFSET}	Current-Limit Threshold	–30	–14	0	mV	$V_{FB} = 0.79V$
V_{SC}	Short-Circuit Threshold	–23	–7	9	mV	$V_{FB} = 0V$
I_{CL}	Current-Limit Source Current	50	70	90	µA	$V_{FB} = 0.79V$
I_{SC}	Short-Circuit Source Current	25	35	45	µA	$V_{FB} = 0V$
Leakage						
$I_{SW_Leakage}$	SW, BST Leakage Current	—	—	10	µA	—
I_{FREQ_LEAK}	FREQ Pin Leakage Current	—	—	10	µA	—

Note 1: Specification for packaged product only.

TABLE 1-1: ELECTRICAL CHARACTERISTICS[1] (CONTINUED)

Electrical Specifications: unless otherwise specified, $PV_{IN} = V_{IN} = V_{EN} = 12V$; $V_{OUT} = 3.3V$; $V_{BST} – V_{SW} = 5V$; $T_J = +25°C$. **Boldface** values indicate $–40°C \le T_J \le +125°C$.						
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Power Good (PG)						
V_{PG_TH}	PG Threshold Voltage	**85**	90	**95**	$\%V_{OUT}$	Sweep V_{FB} from Low-to-High
V_{PG_HYS}	PG Hysteresis	—	6	—	$\%V_{OUT}$	Sweep V_{FB} from High-to-Low
t_{PG_DLY}	PG Delay Time	—	100	—	µs	Sweep V_{FB} from Low-to-High
V_{PG_LOW}	PG Low Voltage	—	70	**200**	mV	$V_{FB} < 90\% \times V_{NOM}$, $I_{PG} = 1$ mA
Thermal Protection						
T_{SHD}	Overtemperature Shutdown	—	160	—	°C	T_J Rising
T_{SHD_HYS}	Overtemperature Shutdown Hysteresis	—	15	—	°C	—

Note 1: Specification for packaged product only.

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2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{IN} = 12V, f_{SW} = 600 kHz, T_J = +25°C.

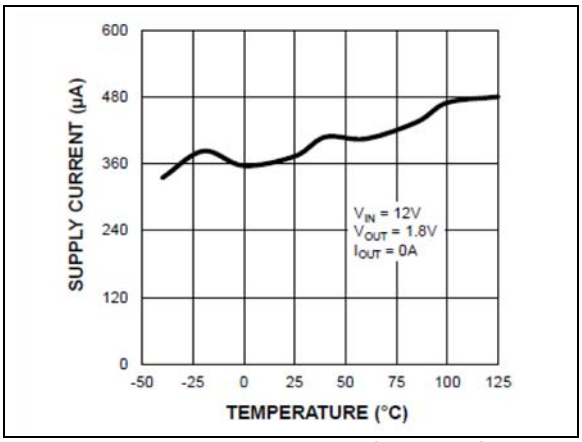

FIGURE 2-1: *V_{IN} Operating Supply Current vs. Temperature (MIC45208-1).*

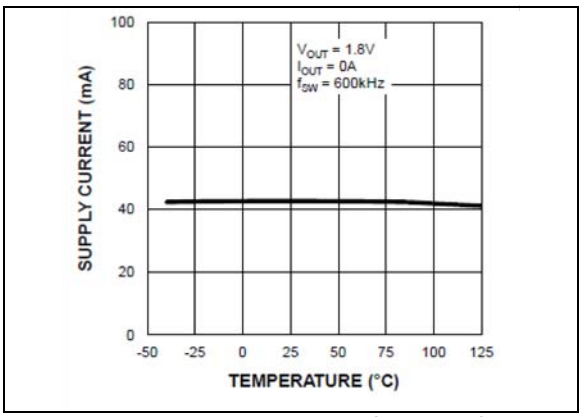

FIGURE 2-2: *V_{IN} Operating Supply Current vs. Temperature (MIC45208-2).*

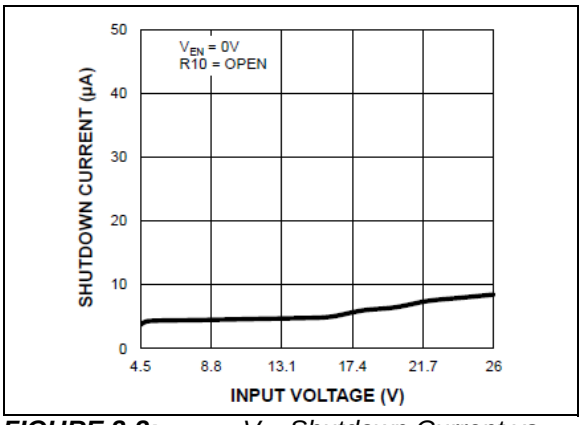

FIGURE 2-3: *V_{IN} Shutdown Current vs. Input Voltage.*

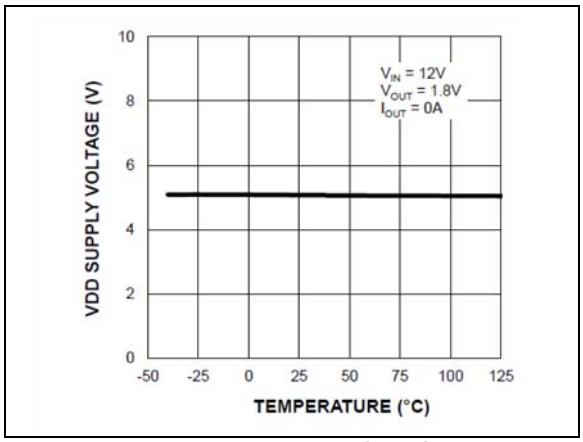

FIGURE 2-4: *V_{DD} Supply Voltage vs. Temperature.*

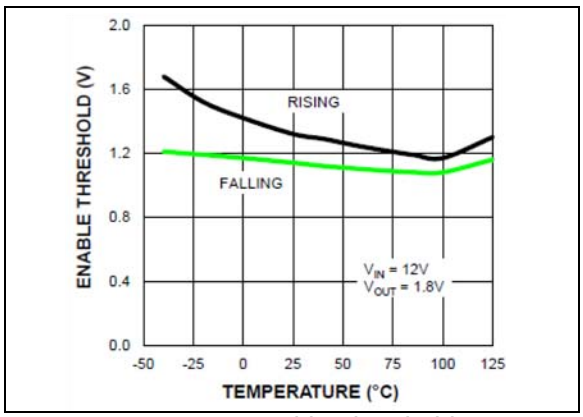

FIGURE 2-5: *Enable Threshold vs. Temperature.*

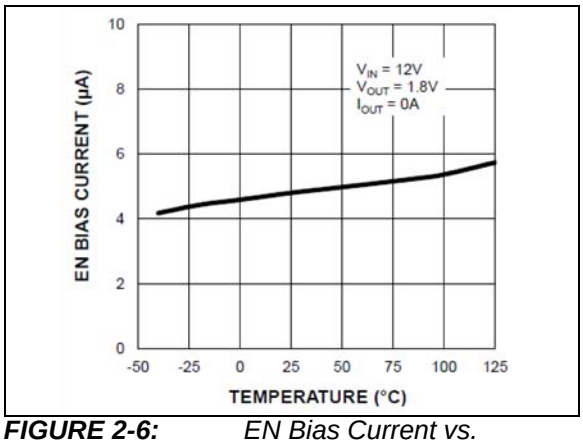

FIGURE 2-6: *EN Bias Current vs. Temperature.*

Note: Unless otherwise indicated, V_{IN} = 12V, f_{SW} = 600 kHz, T_J = +25°C.

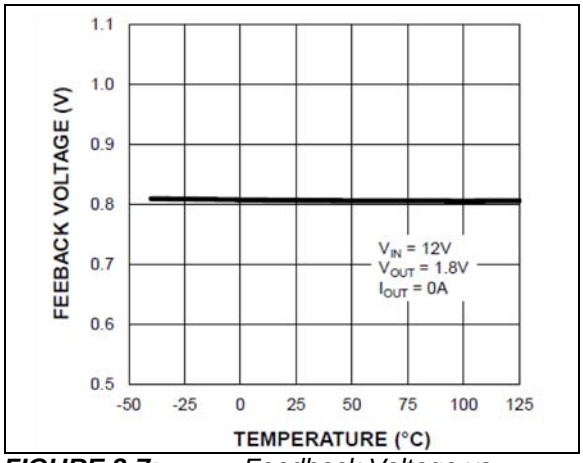

FIGURE 2-7: *Feedback Voltage vs. Temperature.*

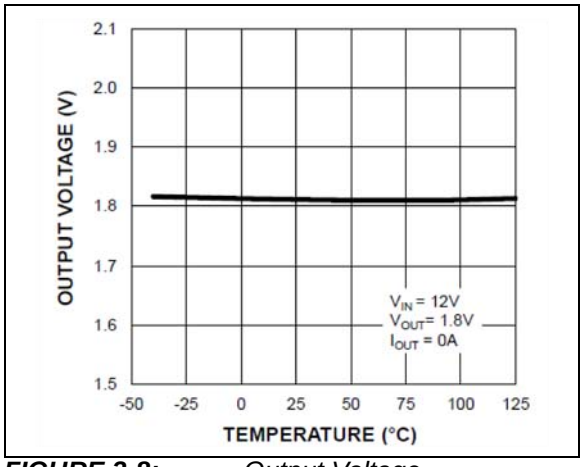

FIGURE 2-8: *Output Voltage vs.Temperature.*

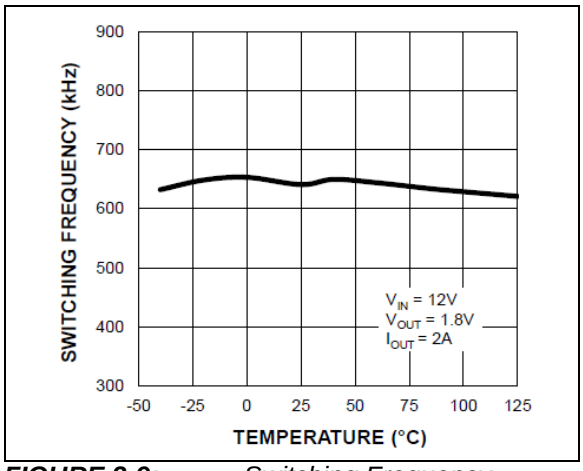

FIGURE 2-9: *Switching Frequency vs.Temperature.*

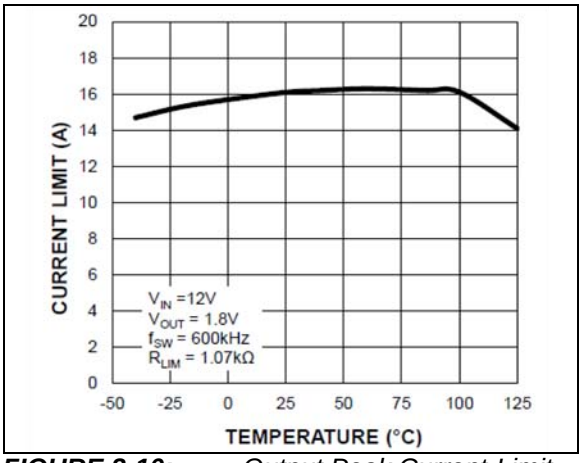

FIGURE 2-10: *Output Peak Current-Limit vs. Temperature.*

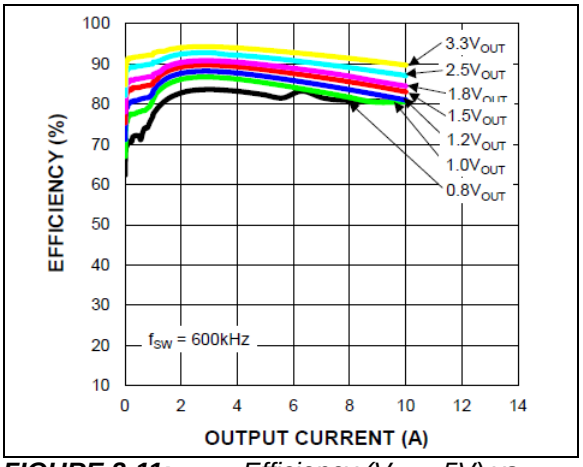

FIGURE 2-11: *Efficiency (V_{IN} = 5V) vs. Output Current (MIC45208-1).*

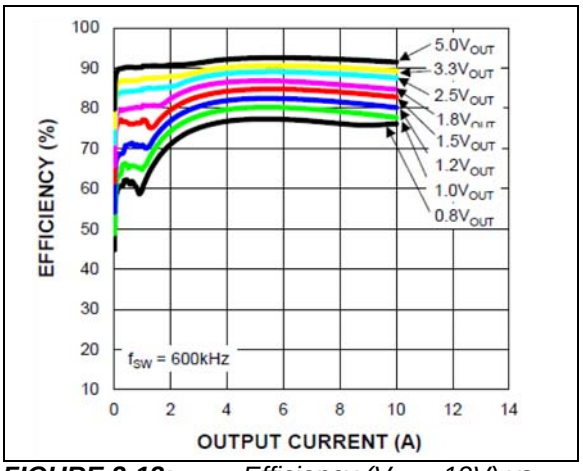

FIGURE 2-12: *Efficiency (V_{IN} = 12V) vs. Output Current (MIC45208-1).*

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Note: Unless otherwise indicated, V_{IN} = 12V, f_{SW} = 600 kHz, T_J = +25°C.

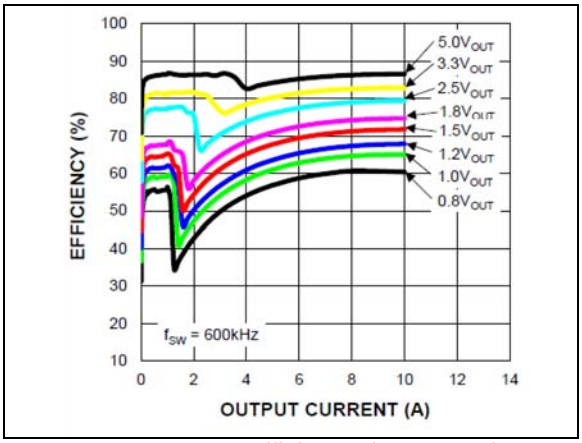

FIGURE 2-13: *Efficiency (V_{IN} = 24V) vs. Output Current (MIC45208-1).*

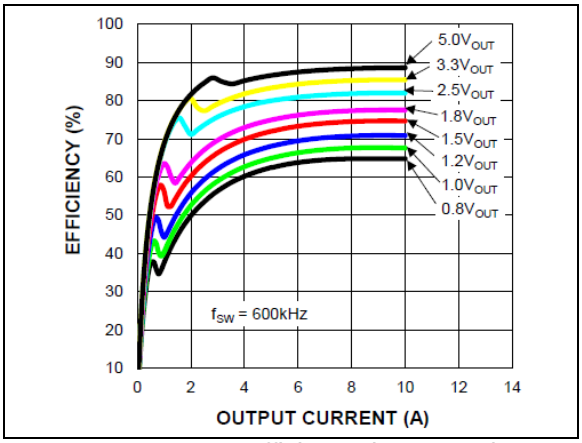

FIGURE 2-16: *Efficiency (V_{IN} = 24V) vs. Output Current (MIC45208-2).*

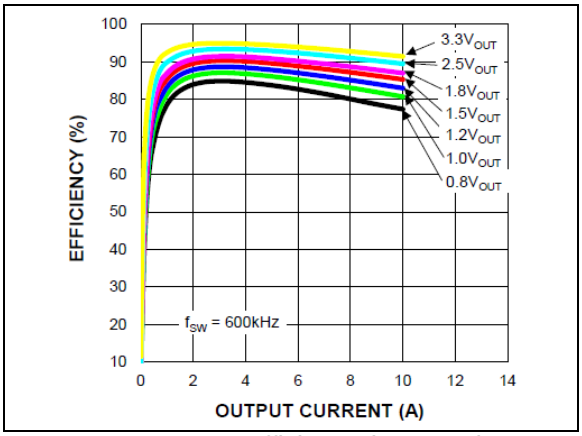

FIGURE 2-14: *Efficiency (V_{IN} = 5V) vs. Output Current (MIC45208-2).*

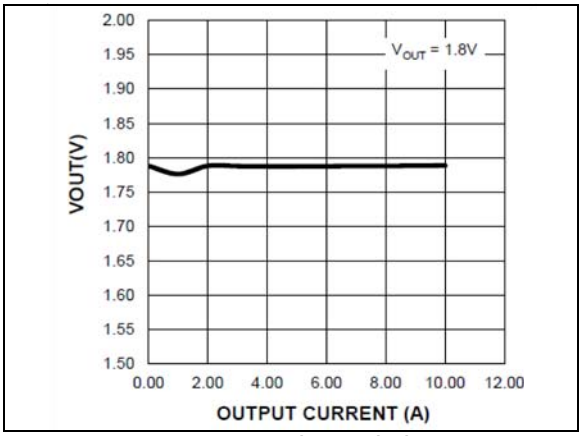

FIGURE 2-17: *Load Regulation vs. Input Voltage.*

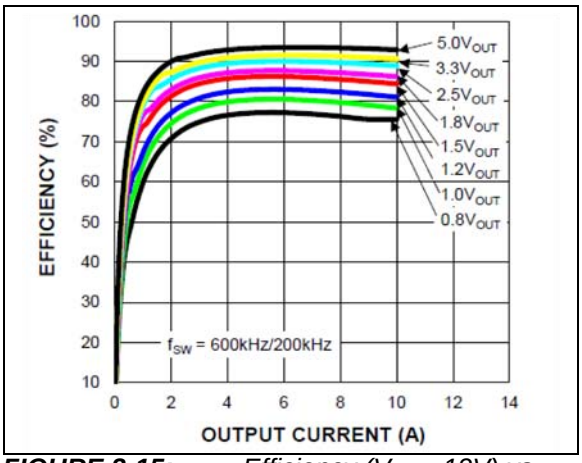

FIGURE 2-15: *Efficiency (V_{IN} = 12V) vs. Output Current (MIC45208-2).*

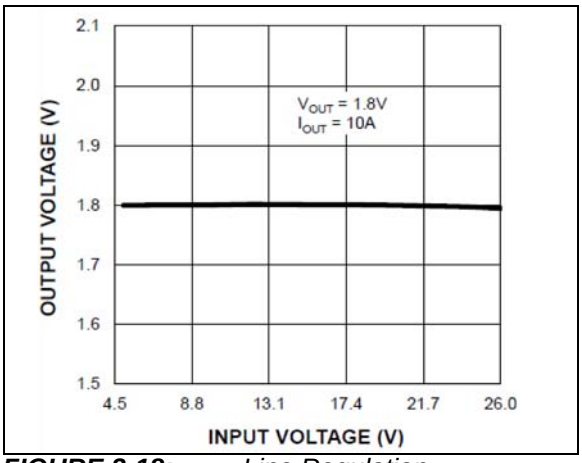

FIGURE 2-18: *Line Regulation.*

Note: Unless otherwise indicated, V_{IN} = 12V, f_{SW} = 600 kHz, T_J = +25°C.

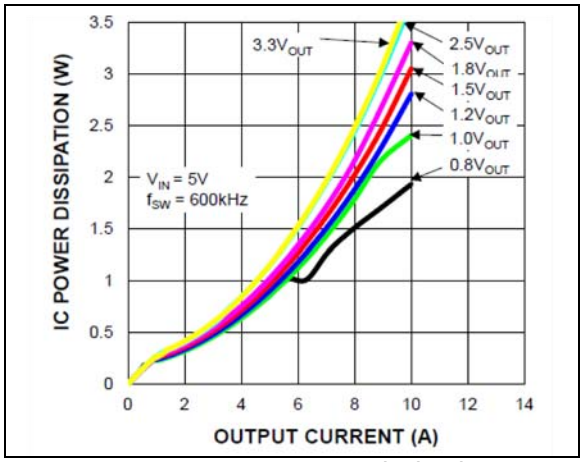

FIGURE 2-19: *IC Power Dissipation (V_{IN} = 5V) vs. Output Current (MIC-45208-1).*

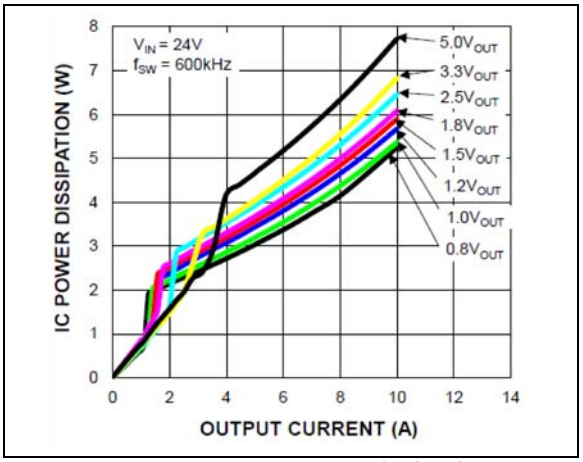

FIGURE 2-21: *IC Power Dissipation (V_{IN} = 24V) vs. Output Current (MIC45208-1).*

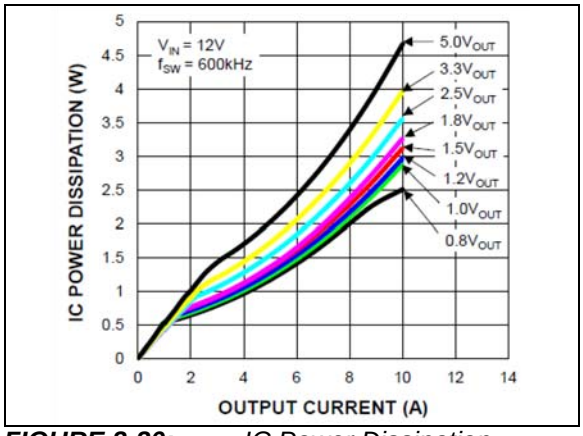

FIGURE 2-20: *IC Power Dissipation (V_{IN} = 12V) vs. Output Current (MIC45208-1).*

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Note: Unless otherwise indicated, V_{IN} = 12V, f_{SW} = 600 kHz, T_J = +25°C.

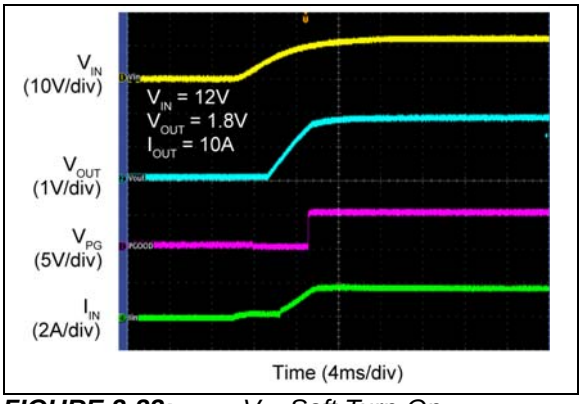

FIGURE 2-22: *V_{IN} Soft Turn-On.*

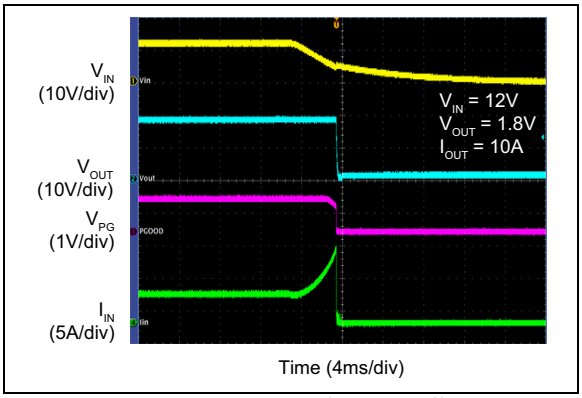

FIGURE 2-23: *V_{IN} Soft Turn-Off.*

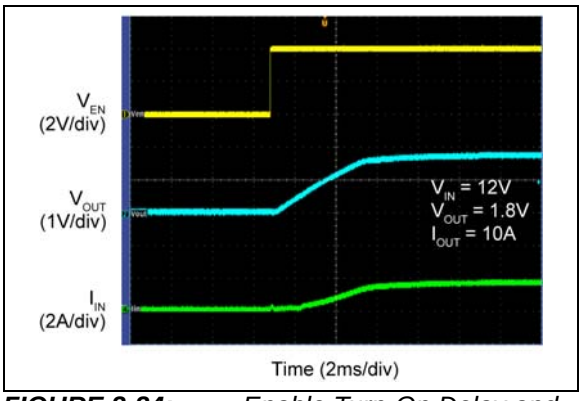

FIGURE 2-24: *Enable Turn-On Delay and Rise Time.*

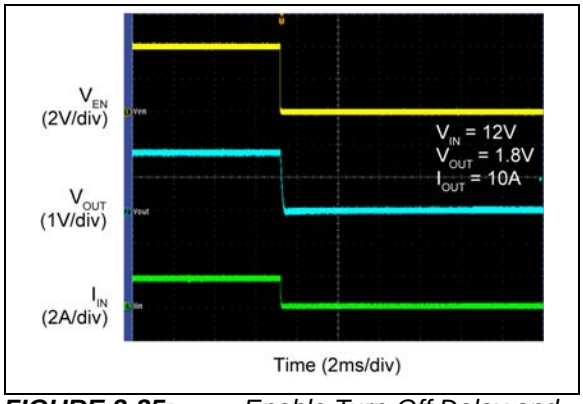

FIGURE 2-25: *Enable Turn-Off Delay and Fall Time.*

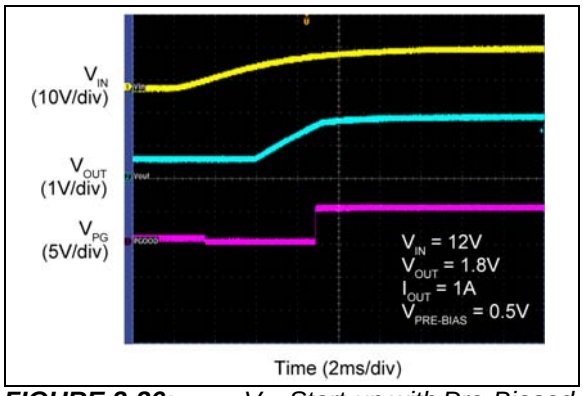

FIGURE 2-26: *V_{IN} Start-up with Pre-Biased Output.*

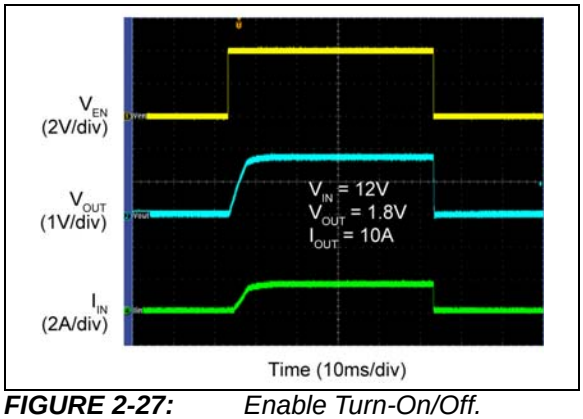

FIGURE 2-27: *Enable Turn-On/Off.*

Note: Unless otherwise indicated, V_{IN} = 12V, f_{SW} = 600 kHz, T_J = +25°C.

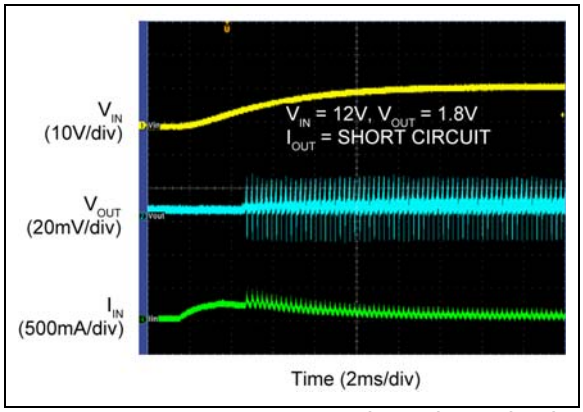

FIGURE 2-28: *Power-up into Short Circuit.*

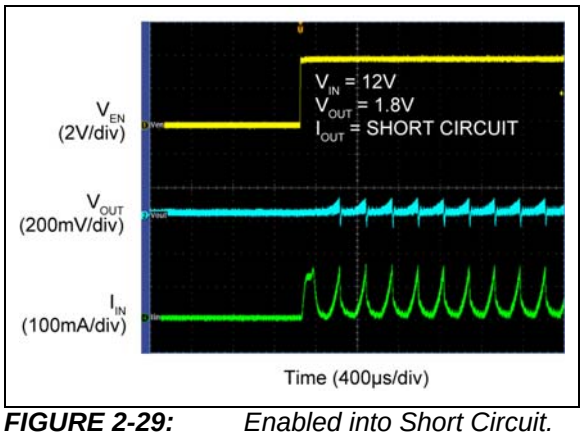

FIGURE 2-29: *Enabled into Short Circuit.*

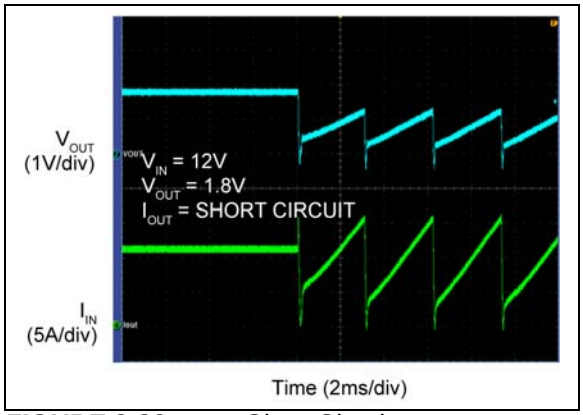

FIGURE 2-30: *Short Circuit.*

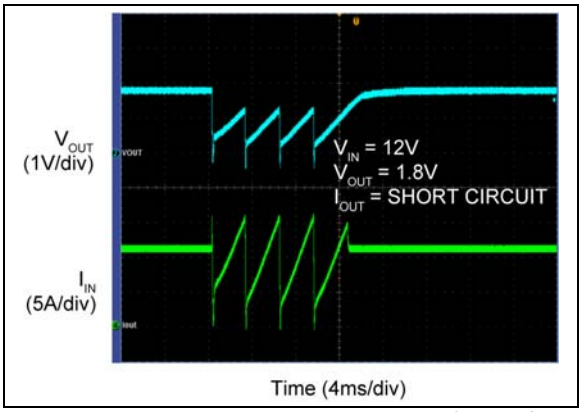

FIGURE 2-31: *Output Recovery from Short Circuit.*

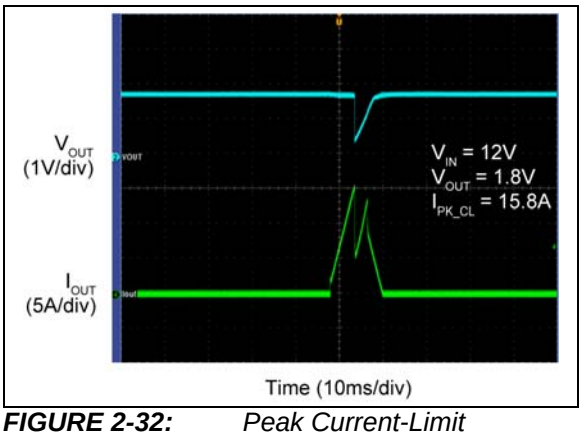

FIGURE 2-32: *Peak Current-Limit Threshold.*

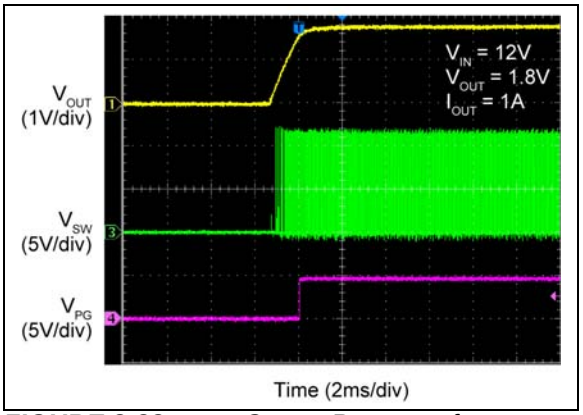

FIGURE 2-33: *Output Recovery from Thermal Shutdown.*

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Note: Unless otherwise indicated, V_{IN} = 12V, f_{SW} = 600 kHz, T_J = +25°C.

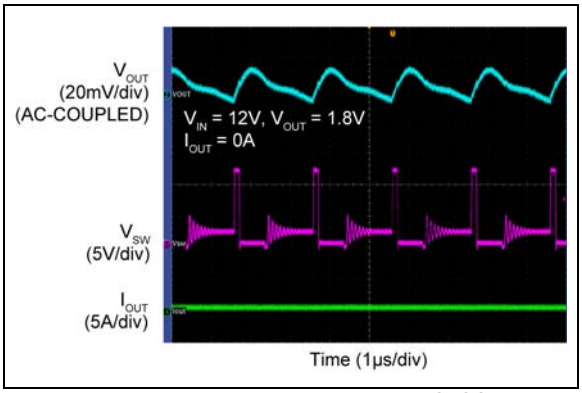

FIGURE 2-34: *MIC45208-1 Switching Waveforms.*

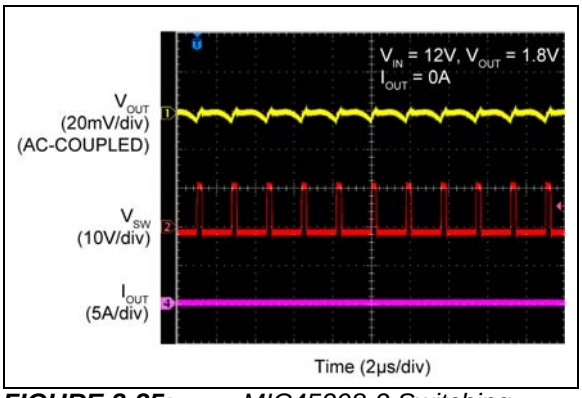

FIGURE 2-35: *MIC45208-2 Switching Waveforms.*

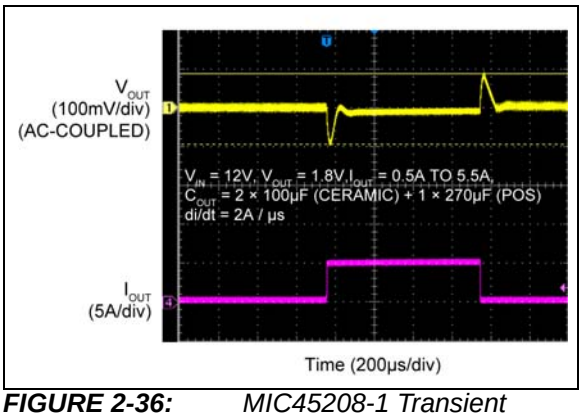

FIGURE 2-36: *MIC45208-1 Transient Response.*

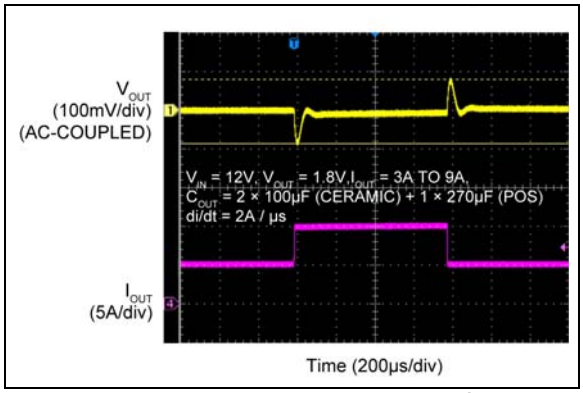

FIGURE 2-37: *MIC45208-2 Transient Response.*

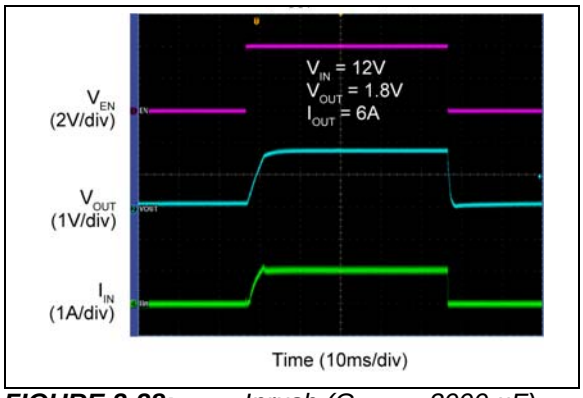

FIGURE 2-38: *Inrush (C_{OUT} = 3000 µF).*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MIC45208 Pin Number	Pin Name	Pin Function
1, 2	$5V_{DD}$	Internal +5V Linear Regulator Output: Powered by V_{IN}, $5V_{DD}$ is the internal supply bus for the device. In the applications with V_{IN} < +5.5V, $5V_{DD}$ should be tied to V_{IN} to bypass the linear regulator.
3, 4	PV_{DD}	PV_{DD}: Supply input for the internal low-side power MOSFET driver.
5, 6, 7	PGND	Power Ground: PGND is the return path for the step-down power module power stage. The PGND pin connects to the sources of the internal low-side power MOSFET, the negative terminals of input capacitors and the negative terminals of output capacitors.
9-11, 31-35	SW	The SW pin connects directly to the switch node. Due to the high-speed switching on this pin, the SW pin should be routed away from sensitive nodes. The SW pin also senses the current by monitoring the voltage across the low-side MOSFET during off time.
12-19	PV_{IN}	Power Input Voltage: Connection to the drain of the internal high-side power MOSFET. Connects an input capacitor from PV_{IN} to PGND.
20-29	V_{OUT}	Power Output Voltage: Connected to the internal inductor. The output capacitor should be connected from this pin to PGND as close to the module as possible.
37, 38	RIA	Ripple Injection Pin A: Leave floating, no connection.
39	RIB	Ripple Injection Pin B: Connect this pin to FB.
40, 41	ANODE	Anode Bootstrap Diode: Anode connection of internal bootstrap diode; this pin should be connected to the PV_{DD} pin.
42, 43, 44	BST	Connection to the internal bootstrap circuitry and high-side power MOSFET drive circuitry. Leave floating, no connection.
45, 52	GND	Analog Ground: Connect bottom feedback resistor to GND. GND and PGND are internally connected.
46	FB	Feedback: Input to the transconductance amplifier of the control loop. The FB pin is referenced to 0.8V. A resistor divider connecting the feedback to the output is used to set the desired output voltage. Connects the bottom resistor from FB to GND.
47	PG	Power Good: Open-Drain Output. If used, connect to an external pull-up resistor of at least 10 kOhm between PG and the external bias voltage.
48	EN	Enable: A logic signal to enable or disable the step-down regulator module operation. The EN pin is TTL/CMOS compatible. Logic high = enable, logic low = disable or shutdown. Do not leave floating.
49	V_{IN}	Internal 5V Linear Regulator Input: A 1 µF ceramic capacitor from V_{IN} to GND is required for decoupling.
50	FREQ	Switching Frequency Adjust: Use a resistor divider from V_{IN} to GND to program the switching frequency. Connecting FREQ to V_{IN} sets frequency = 600 kHz.
51	I_{LIM}	Current Limit: Connect a resistor between I_{LIM} and SW to program the current limit.
8, 12, 20, 30, 36	KEEPOUT	Depopulated pin positions.
—	PV_{IN} ePAD	PV_{IN} Exposed Pad: Internally connected to the PV_{IN} pins.
—	V_{OUT} ePAD	V_{OUT} Exposed Pad: Internally connected to the V_{OUT} pins.

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4.0 FUNCTIONAL DESCRIPTION

The MIC45208 is an adaptive on-time synchronous buck regulator module, built for high-input voltage to low-output voltage conversion applications. The MIC45208 is designed to operate over a wide input voltage range, from 4.5V to 26V, and the output is adjustable with an external resistor divider. An adaptive on-time control scheme is employed to obtain a constant switching frequency in steady state and to simplify the control compensation. Hiccup mode over-current protection is implemented by sensing the low-side MOSFET's $R_{DS(ON)}$. The device features an internal soft-start enable, UVLO, and thermal shutdown. The module has integrated switching FETs, inductor, bootstrap diode, resistor, capacitor and controller.

4.1 Theory of Operation

As shown in Figure 4-1, in association with Equation 4-1, the output voltage is sensed by the MIC45208 feedback pin, FB, via the voltage dividers, R_{FB1} and R_{FB2}. The output voltage is then compared to a 0.8V reference voltage, V_{REF}, at the error comparator, through a low-gain transconductance (g_M) amplifier. If the feedback voltage decreases and falls below 0.8V, then the error comparator will trigger the control logic and generate an ON-time period. The ON-time period length is predetermined by the "Fixed t_{ON} Estimator" circuitry:

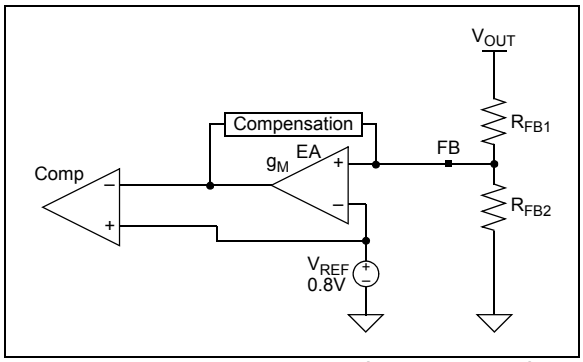

FIGURE 4-1: *Output Voltage Sense via FB Pin.*

EQUATION 4-1: ON-TIME ESTIMATION

$$t_{ON(ESTIMATED)} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

Where:

V_{OUT} = Output voltage

V_{IN} = Power stage input voltage

f_{SW} = Switching frequency

At the end of the ON-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. In most cases, the OFF-time period length depends upon the feedback voltage. When the feedback voltage decreases and the output of the g_M amplifier falls below 0.8V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period, determined by the feedback voltage, is less than the minimum OFF-time, $t_{OFF(MIN)}$, which is about 200 ns, the MIC45208 control logic will apply the $t_{OFF(MIN)}$ instead. $t_{OFF(MIN)}$ is required to maintain enough energy in the Boost Capacitor (C_{BST}) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 200 ns $t_{OFF(MIN)}$:

EQUATION 4-2: MAXIMUM DUTY CYCLE

$$D_{MAX} = \frac{t_S - t_{OFF(MIN)}}{t_S} = 1 - \frac{200\text{ ns}}{t_S}$$

Where:

$t_S = 1/f_{SW}$

It is not recommended to use the MIC45208 device with an OFF-time close to $t_{OFF(MIN)}$ during steady-state operation.

The adaptive ON-time control scheme results in a constant switching frequency in the MIC45208 during steady-state operation. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications. During load transients, the switching frequency is changed due to the varying OFF-time.

To illustrate the control loop operation, we will analyze both the steady-state and load transient scenarios. For easy analysis, the gain of the g_M amplifier is assumed to be 1. With this assumption, the inverting input of the error comparator is the same as the feedback voltage.

Figure 4-2 shows the MIC45208 control loop timing during steady-state operation. During steady state, the g_M amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple plus the injected voltage ripple, to trigger the ON-time period. The ON-time is predetermined by the t_{ON} estimator. The termination of the OFF-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when V_{FB} falls below V_{REF}, the OFF-time period ends and the next ON-time period is triggered through the control logic circuitry.

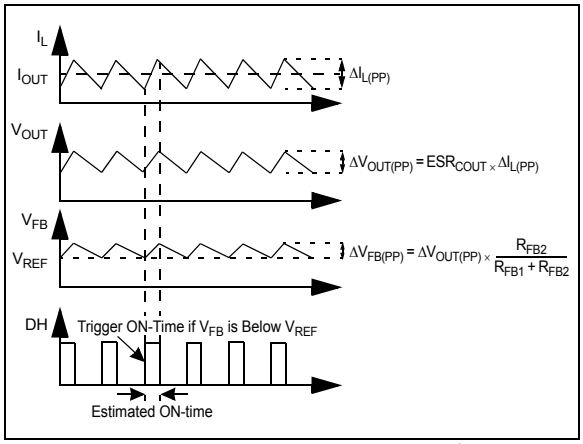

FIGURE 4-2: *MIC45208 Control Loop Timing.*

Figure 4-3 shows the operation of the MIC45208 during a load transient. The output voltage drops due to the sudden load increase, which causes the V_{FB} to be less than V_{REF}. This will cause the error comparator to trigger an ON-time period. At the end of the ON-time period, a minimum OFF-time, $t_{OFF(MIN)}$, is generated to charge the Bootstrap Capacitor (C_{BST}), since the feedback voltage is still below V_{REF}. Then, the next ON-time period is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small. Note that the instantaneous switching frequency during load transient remains bounded and cannot increase arbitrarily. The minimum is limited by $t_{ON} + t_{OFF(MIN)}$. Since the variation in V_{OUT} is relatively limited during load transient, t_{ON} stays virtually close to its steady-state value.

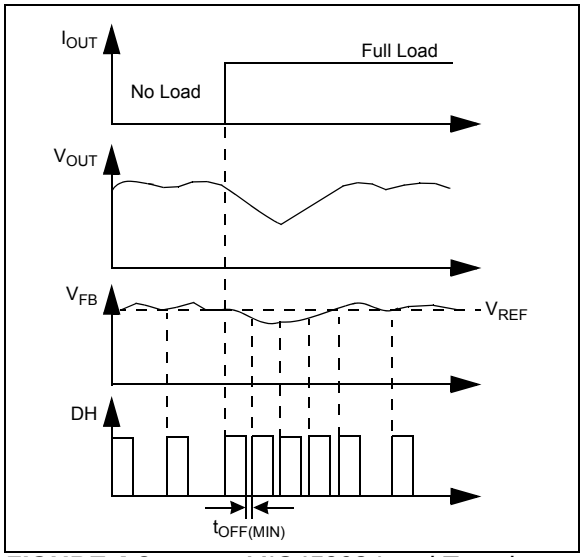

FIGURE 4-3: *MIC45208 Load Transient Response.*

Unlike true Current mode control, the MIC45208 uses the output voltage ripple to trigger an ON-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough.

In order to meet the stability requirements, the MIC45208 feedback voltage ripple should be in phase with the inductor current ripple, and are large enough to be sensed by the g_M amplifier and the error comparator. The recommended feedback voltage ripple is 20 mV ~ 100 mV over full input voltage range. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the g_M amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation. Please refer to **Section 5.5 "Ripple Injection"** in **Section 5.0 "Application Information"** for more details about the ripple injection technique.

4.2 Discontinuous Mode (MIC45208-1 only)

In Continuous mode, the inductor current is always greater than zero; however, at light loads, the MIC45208-1 is able to force the inductor current to operate in Discontinuous mode. Discontinuous mode is where the inductor current falls to zero, as indicated by trace (I_L) shown in Figure 4-4. During this period, the efficiency is optimized by shutting down all the non-essential circuits and minimizing the supply current as the switching frequency is reduced. The MIC45208-1 wakes up and turns on the high-side MOSFET when the feedback voltage, V_{FB}, drops below 0.8V.

The MIC45208-1 has a Zero-Crossing (ZC) comparator that monitors the inductor current by sensing the voltage drop across the low-side MOSFET during its ON-time. If the V_{FB} > 0.8V and the inductor current goes slightly negative, then the MIC45208-1 automatically powers down most of the IC circuitry and goes into a Low-Power mode.

Once the MIC45208-1 goes into Discontinuous mode, both DL and DH are low, which turns off the high-side and low-side MOSFETs. The load current is supplied by the output capacitors and V_{OUT} drops. If the drop of V_{OUT} causes V_{FB} to go below V_{REF}, then all the circuits will wake-up into normal Continuous mode. First, the bias currents of most circuits that were reduced, during the Discontinuous mode, are restored and then a t_{ON} pulse is triggered before the drivers are turned on to avoid any possible glitches. Finally, the high-side driver is turned on. Figure 4-4 shows the control loop timing in Discontinuous mode.

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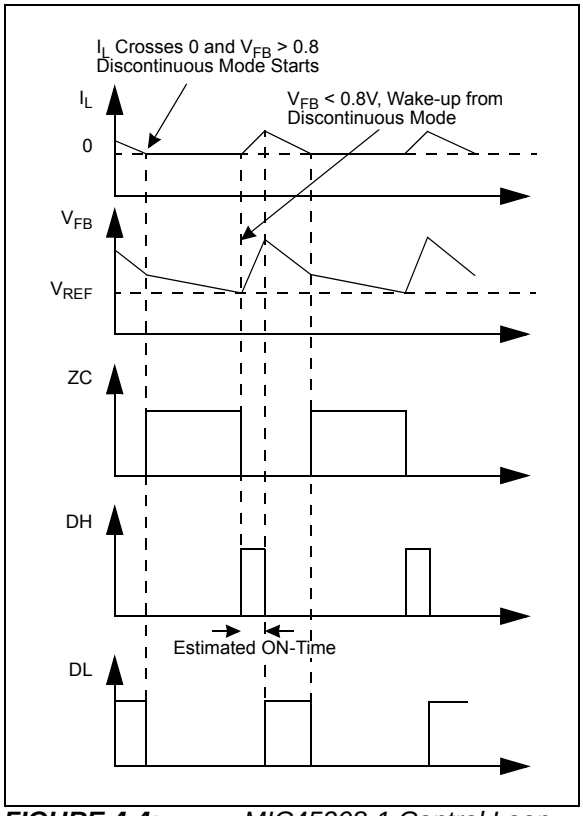

FIGURE 4-4: *MIC45208-1 Control Loop Timing (Discontinuous Mode).*

During Discontinuous mode, the bias current of most circuits is substantially reduced. As a result, the total power supply current during Discontinuous mode is only about 350 µA, allowing the MIC45208-1 to achieve high efficiency in light load applications.

4.3 Soft Start

Soft start reduces the input power supply surge current at start-up by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up.

The MIC45208 implements an internal digital soft start by making the 0.8V reference voltage, V_{REF}, ramp from 0 to 100% in about 3 ms with 9.7 mV steps. Therefore, the output voltage is controlled to increase slowly by a staircase V_{FB} ramp. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption. PV_{DD} must be powered up at the same time or after V_{IN} to make the soft start function correctly.

4.4 Current Limit

The MIC45208 uses the $R_{DS(ON)}$ of the low-side MOSFET and the external resistor connected from the I_{LIM} pin to the SW node to set the current limit.

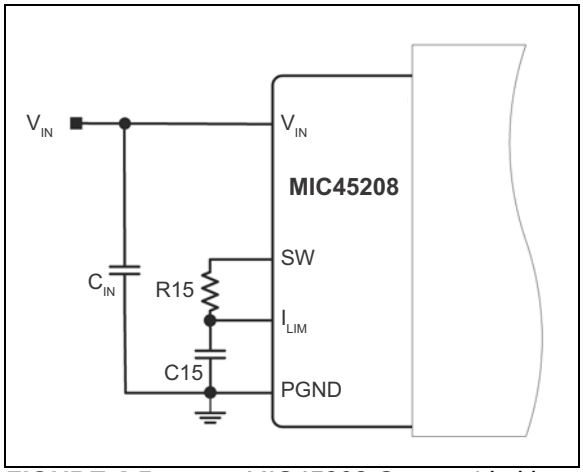

FIGURE 4-5: *MIC45208 Current-Limiting Circuit.*

In each switching cycle of the MIC45208, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. The sensed voltage, V_{ILIM}, is compared with the Power Ground (PGND) after a blanking time of 150 ns. In this way, the drop voltage over the resistor, R15 (V_{CL}), is compared with the drop over the bottom FET generating the short current limit. The small capacitor (C15) connected from the I_{LIM} pin to PGND filters the switching node ringing during the OFF-time, allowing a better short limit measurement. The time constant created by R15 and C15 should be much less than the minimum OFF-time.

The V_{CL} drop allows programming of short limit through the value of the resistor (R15). If the absolute value of the voltage drop on the bottom FET becomes greater than V_{CL}, and the V_{ILIM} falls below PGND, an overcurrent is triggered, causing the IC to enter Hiccup mode. The hiccup sequence, including the soft start, reduces the stress on the switching FETs, and protects the load and supply for severe short conditions.

The short-circuit current limit can be programmed by using Equation 4-3.

EQUATION 4-3: PROGRAMMING CURRENT LIMIT

$$R15 = \frac{(I_{CLIM} + \Delta I_{L(PP)} \times 0.5) \times R_{DS(ON)} + V_{CL_OFFSET}}{I_{CL}}$$

Where:

I_{CLIM} = Desired current limit

$R_{DS(ON)}$ = On resistance of low-side power MOSFET, 6 mΩ typically

V_{CL_OFFSET} = Current-limit threshold (typical absolute value is 14 mV per Table 1-1)

I_{CL} = Current-limit source current (typical value is 70 µA per Table 1-1)

$\Delta I_{L(PP)}$ = Inductor current peak-to-peak; because the inductor is integrated, use Equation 4-4 to calculate the inductor ripple current

The peak-to-peak inductor current ripple is:

EQUATION 4-4: PEAK-TO-PEAK INDUCTOR CURRENT RIPPLE

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times L}$$

The MIC45208 has a 0.8 µH inductor integrated into the module. In case of a hard short, the short limit is folded down to allow an indefinite hard short on the output without any destructive effect. It is mandatory to make sure that the inductor current used to charge the output capacitance during soft start is under the folded short limit; otherwise, the supply will go into hiccup mode and may not finish the soft start successfully.

The MOSFET $R_{DS(ON)}$ varies 30% to 40% with temperature; therefore, it is recommended to add a 50% margin to I_{CLIM} in Equation 4-3 to avoid false current limiting due to increased MOSFET junction temperature rise.

With R15 = 1.37 kΩ and C15 = 15 pF, the typical output current limit is 16A.

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5.0 APPLICATION INFORMATION

5.1 Setting the Switching Frequency

The MIC45208 switching frequency can be adjusted by changing the value of resistors, R1 and R2.

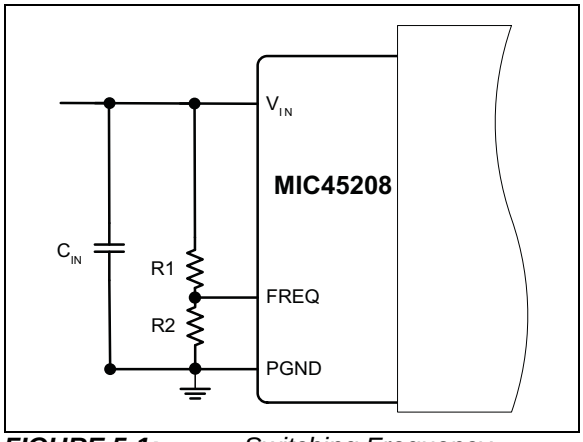

FIGURE 5-1: *Switching Frequency Adjustment.*

Equation 5-1 gives the estimated switching frequency:

EQUATION 5-1: ESTIMATED SWITCHING FREQUENCY

$$f_{SW} = f_O \times \frac{R2}{R1 + R2}$$

Where:

f_O = 600 kHz (typical per Table 1-1)

$R1$ = 100 kΩ is recommended

$R2$ = Needs to be selected in order to set the required switching frequency

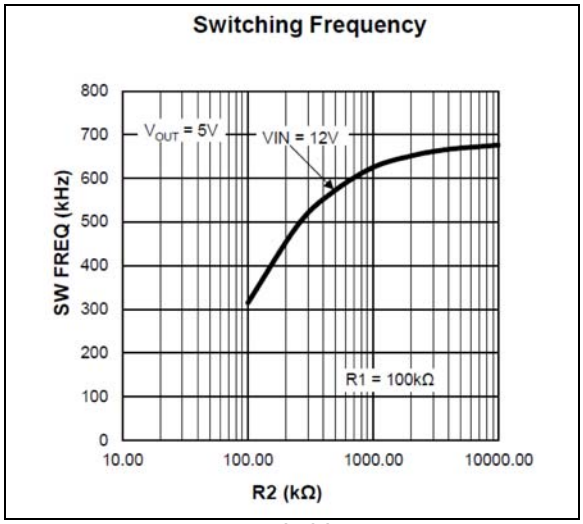

FIGURE 5-2: *Switching Frequency vs. R2.*

5.2 Output Capacitor Selection

The type of output capacitor is usually determined by the application and its Equivalent Series Resistance (ESR). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are MLCC, OS-CON and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple. The MIC45208 requires ripple injection and the output capacitor ESR affects the control loop from a stability point of view.

The maximum value of ESR is calculated as in Equation 5-2:

EQUATION 5-2: ESR MAXIMUM VALUE

$$ESR_{COUT} \leq \frac{\Delta V_{OUT(PP)}}{\Delta I_{L(PP)}}$$

Where:

$\Delta V_{OUT(PP)}$ = Peak-to-peak output

$\Delta I_{L(PP)}$ = Peak-to-peak inductor current ripple

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated in Equation 5-3:

EQUATION 5-3: TOTAL OUTPUT RIPPLE

$$\Delta V_{OUT(PP)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + (\Delta I_{L(PP)} \times ESR_{COUT})^2}$$

Where:

C_{OUT} = Output capacitance value

f_{SW} = Switching frequency

As described in **Section 4.1 "Theory of Operation"** in **Section 4.0 "Functional Description"**, the MIC45208 requires at least a 20 mV peak-to-peak ripple at the FB pin to make the g_M amplifier and the error comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors' value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide enough feedback voltage ripple. Please refer to **Section 5.5 "Ripple Injection"** in **Section 5.0 "Application Information"** for more details.

The output capacitor RMS current is calculated in Equation 5-4:

EQUATION 5-4: OUTPUT CAPACITOR RMS CURRENT

$$I_{COUT(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}}$$

The power dissipated in the output capacitor is:

EQUATION 5-5: DISSIPATED POWER IN OUTPUT CAPACITOR

$$P_{DISS(COUT)} = I_{COUT(RMS)}^2 \times ESR_{COUT}$$

5.3 Input Capacitor Selection

The input capacitor for the Power Input Voltage, PV_{IN}, should be selected for ripple current rating and voltage rating. The input voltage ripple will primarily depend on the input capacitor's ESR. The peak input current is equal to the peak inductor current, so:

EQUATION 5-6: CONFIGURING RIPPLE CURRENT AND VOLTAGE RATINGS

$$\Delta V_{IN} = I_{L(pk)} \times ESR_{CIN}$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

EQUATION 5-7: RMS VALUE OF INPUT CAPACITOR CURRENT

$$I_{CIN(RMS)} \approx I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$$

Where:

D = Duty cycle

The power dissipated in the input capacitor is:

EQUATION 5-8: POWER DISSIPATED IN INPUT CAPACITOR

$$P_{DISS(CIN(RMS))} = I_{CIN(RMS)}^2 \times ESR_{CIN}$$

The general rule is to pick the capacitor with a ripple current rating equal to or greater than the calculated worst-case RMS capacitor current.

Equation 5-9 should be used to calculate the input capacitor. Also, it is recommended to keep some margin on the calculated value:

EQUATION 5-9: INPUT CAPACITOR CALCULATION

$$C_{IN} \approx \frac{I_{OUT(MAX)} \times (1 - D)}{f_{SW} \times dV}$$

Where:

dV = Input ripple

f_{SW} = Switching frequency

5.4 Output Voltage Setting Components

The MIC45208 requires two resistors to set the output voltage, as shown in Figure 5-3:

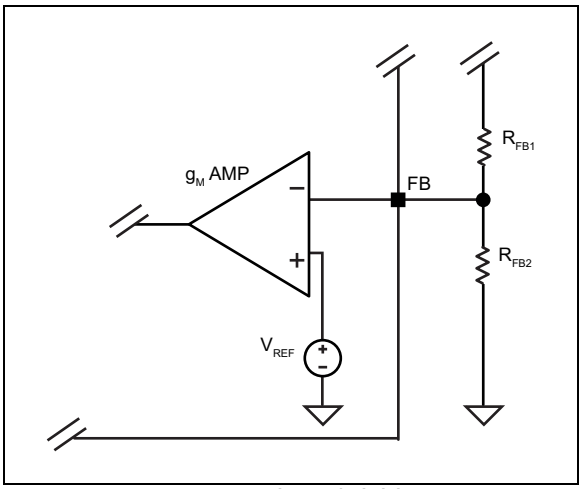

FIGURE 5-3: *Voltage/Divider Configuration.*

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The output voltage is determined by Equation 5-10:

EQUATION 5-10: OUTPUT VOLTAGE DETERMINATION

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

Where:

V_{FB} = 0.8V

A typical value of R_{FB1} used on the standard evaluation board is 10 kΩ. If R_{FB1} is too large, it may allow noise to be introduced into the voltage feedback loop. If R_{FB1} is too small in value, it will decrease the efficiency of the power supply, especially at light loads. Once R_{FB1} is selected, R_{FB2} can be calculated using Equation 5-11:

EQUATION 5-11: CALCULATING R_{FB2}

$$R_{FB2} = \frac{V_{FB} \times R_{FB1}}{V_{OUT} - V_{FB}}$$

For fixed R_{FB1} = 10 kΩ, the output voltage can be selected by R_{FB2}. Table 5-1 provides R_{FB2} values for some common output voltages.

TABLE 5-1: V_{OUT} PROGRAMMING RESISTOR LOOK-UP

R_{FB2}	V_{OUT}
OPEN	0.8V
40.2 kΩ	1.0V
20 kΩ	1.2V
11.5 kΩ	1.5V
8.06 kΩ	1.8V
4.75 kΩ	2.5V
3.24 kΩ	3.3V
1.91 kΩ	5.0V

5.5 Ripple Injection

The V_{FB} ripple required for proper operation of the MIC45208 g_M amplifier and error comparator is 20 mV to 100 mV. However, the output voltage ripple is generally too small to provide enough ripple amplitude at the FB pin and this issue is more visible in lower output voltage applications. If the feedback voltage ripple is so small that the g_M amplifier and error comparator cannot sense it, then the MIC45208 will lose control and the output voltage is not regulated. In order to have some amount of V_{FB} ripple, a ripple injection method is applied for low output voltage ripple applications.

The applications are divided into two situations according to the amount of the feedback voltage ripple:

1. Enough ripple at the feedback voltage due to the large ESR of the output capacitors:

   As shown in Figure 5-4, the converter is stable without any ripple injection.

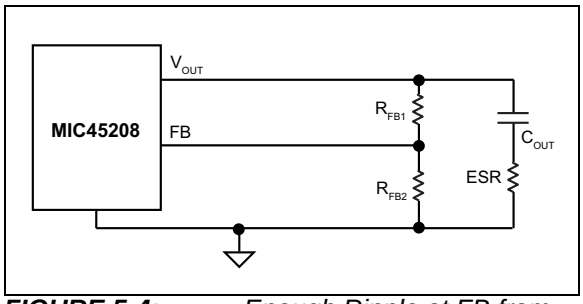

FIGURE 5-4: *Enough Ripple at FB from ESR.*

The feedback voltage ripple is:

EQUATION 5-12: FEEDBACK VOLTAGE RIPPLE

$$\Delta V_{FB(PP)} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \times ESR_{COUT} \times \Delta I_{L(PP)}$$

Where:

$\Delta I_{L(PP)}$ = The peak-to-peak value of the inductor current ripple

2. There is virtually inadequate or no ripple at the FB pin voltage due to the very low-ESR of the output capacitors; such is the case with the ceramic output capacitor. In this case, the V_{FB} ripple waveform needs to be generated by injecting a suitable signal. MIC45208 has provisions to enable an internal series RC injection network, R_{INJ} and C_{INJ}, as shown in Figure 5-5, by connecting RIB to the FB pin. This network injects a square wave current waveform into the FB pin, which by means of integration across the capacitor (C14), generates an appropriate sawtooth FB ripple waveform.

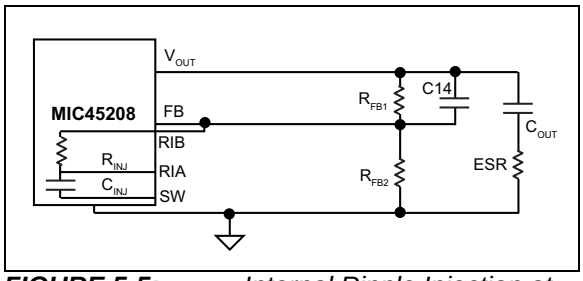

FIGURE 5-5: *Internal Ripple Injection at FB via RIB Pin.*

The injected ripple is:

EQUATION 5-13: INJECTED RIPPLE

$$\Delta V_{FB(PP)} = V_{IN} \times K_{div} \times D \times (1 - D) \times \frac{1}{f_{SW} \times \tau}$$

$$K_{div} = \frac{R_{FB1}//R_{FB2}}{R_{INJ} + R_{FB1}//R_{FB2}}$$

Where:

V_{IN} = Power stage input voltage

D = Duty cycle

f_{SW} = Switching frequency

$\tau = (R_{FB1}//R_{FB2}//R_{INJ}) \times C14$

R_{INJ} = 10 kΩ

C_{INJ} = 0.1 µF

In Equation 5-13 and Equation 5-14, it is assumed that the time constant associated with C14 must be much greater than the switching period:

EQUATION 5-14: CONDITION ON TIME CONSTANT OF C14

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} << 1$$

If the voltage divider resistors, R_{FB1} and R_{FB2}, are in the kΩ range, then a C14 of 1 nF to 100 nF can easily satisfy the large time constant requirements.

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5.6 Thermal Measurements and Safe Operating Area (SOA)

Measuring the IC's case temperature is recommended to ensure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22 gauge, and behaves like a heat sink, resulting in a lower case measurement.

Two methods of temperature measurement are using a smaller thermal couple wire or an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36-gauge wire or higher (smaller wire size) to minimize the wire heat sinking effect. In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to make sure that the thermal couple junction is making good contact with the case of the IC. Omega® Engineering brand thermal couple (5SC-TT-K-36-36) is adequate for most applications.

Wherever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor IC. However, an IR thermometer from Optris® has a 1 mm spot size, which makes it a good choice for measuring the hottest point on the case. An optional stand makes it easy to hold the beam on the IC for long periods of time.

The Safe Operating Area (SOA) of the MIC45208 is shown in Figure 5-6 through Figure 5-10. These thermal measurements were taken on the MIC45208 evaluation board. Since the MIC45208 is an entire system comprised of a switching regulator controller, MOSFETs and inductor, the part needs to be considered as a system. The SOA curves will give guidance to reasonable use of the MIC45208.

SOA curves should only be used as a point of reference. SOA data was acquired using the MIC45208 evaluation board. Thermal performance depends on the PCB layout, board size, copper thickness, number of thermal vias and actual airflow.

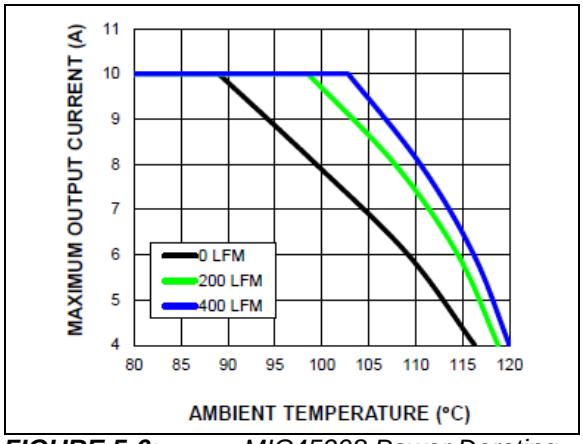

FIGURE 5-6: *MIC45208 Power Derating vs. Airflow (5 V_{IN} to 1.5 V_{OUT}).*

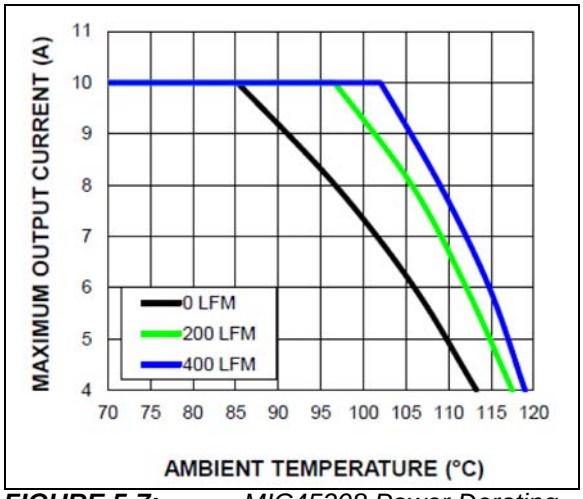

FIGURE 5-7: *MIC45208 Power Derating vs. Airflow (12 V_{IN} to 1.5 V_{OUT}).*

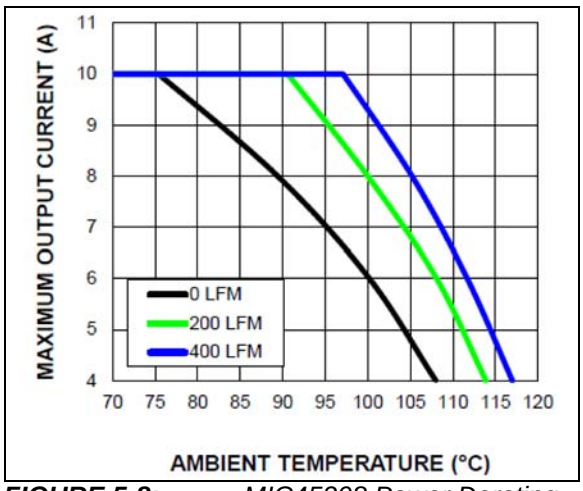

FIGURE 5-8: *MIC45208 Power Derating vs. Airflow (12 V_{IN} to 3.3 V_{OUT}).*

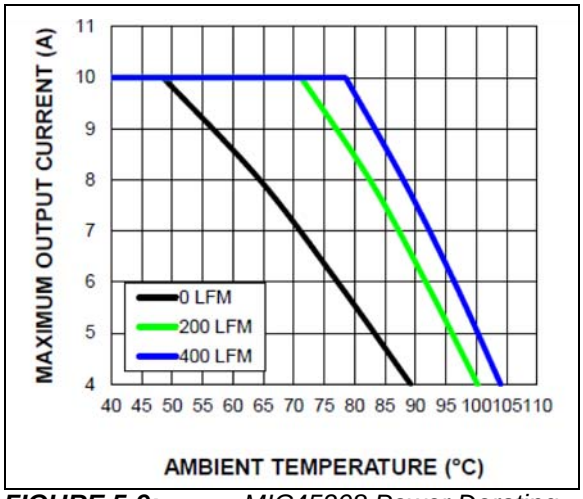

FIGURE 5-9: *MIC45208 Power Derating vs. Airflow (24 V_{IN} to 1.5 V_{OUT}).*

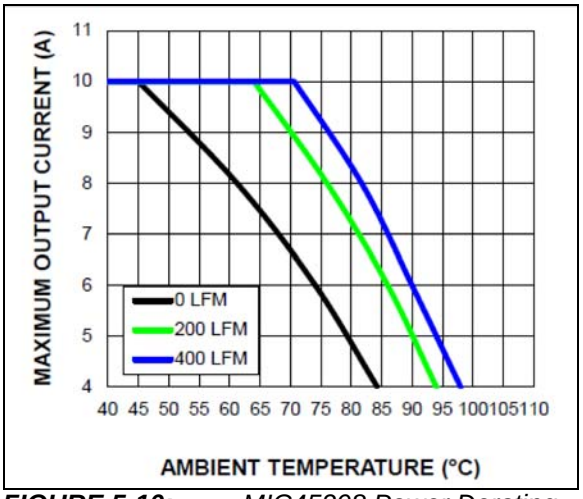

FIGURE 5-10: *MIC45208 Power Derating vs. Airflow (24 V_{IN} to 3.3 V_{OUT}).*

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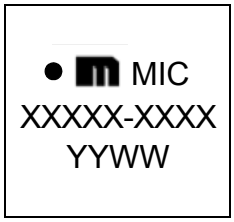
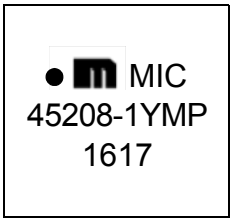
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

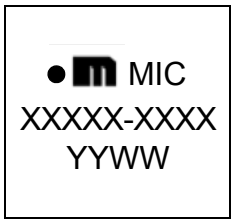
52-Lead 10 mm x 10 mm B2QFN



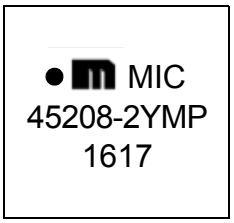
Example



52-Lead 10 mm x 10 mm B2QFN



Example



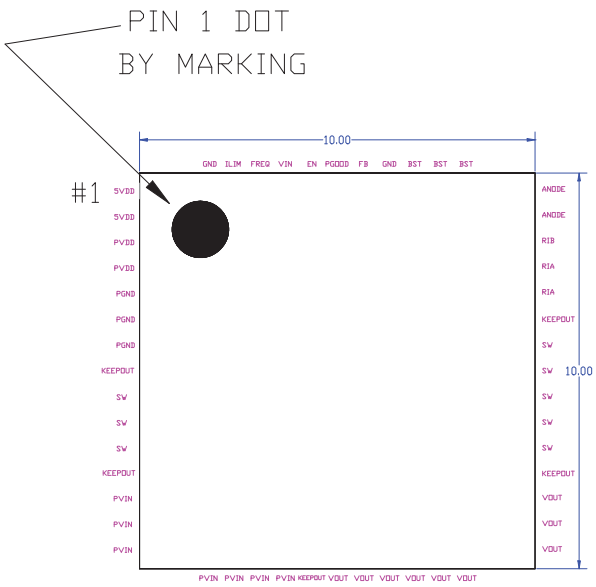
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

6.2 Package Details

The following sections give the technical details of the package.

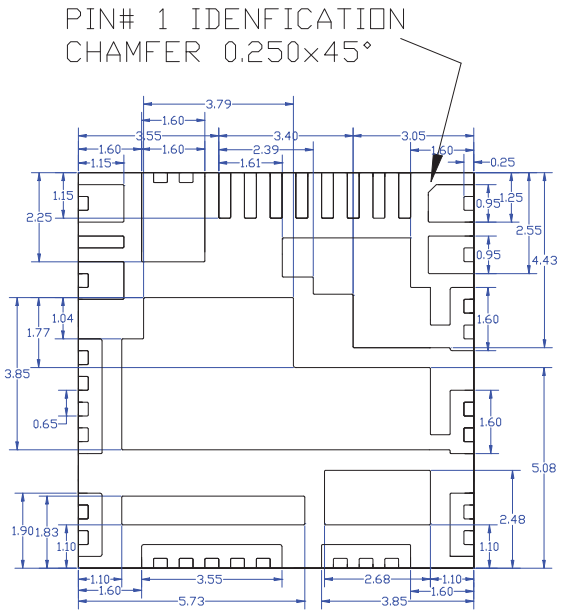
> Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

DRAWING #	B2QFN1010-52LD-PL-1	UNIT	MM
Lead Frame	Copper	Lead Finish	Matte Tin



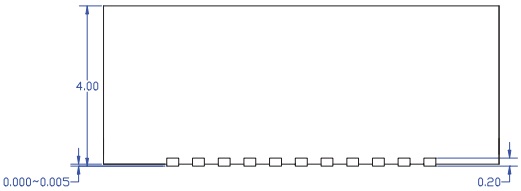
Top View

NOTE: 1, 2, 3



Bottom View

NOTE: 1, 2, 3



Side View

NOTE: 1, 2, 3

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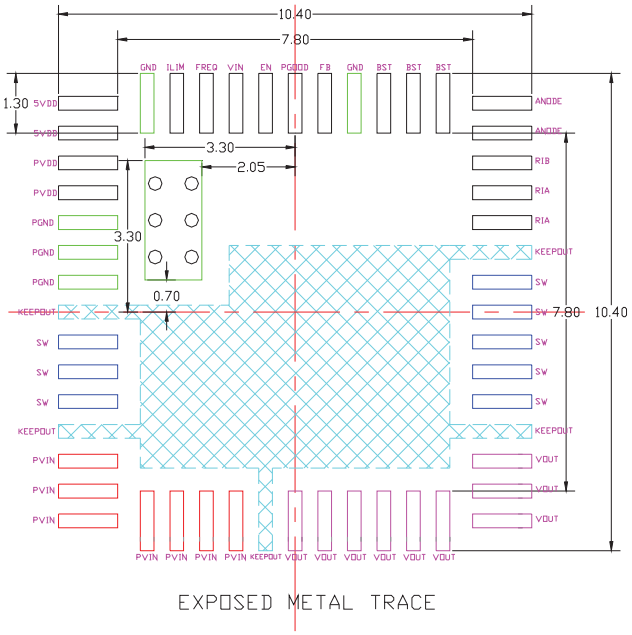
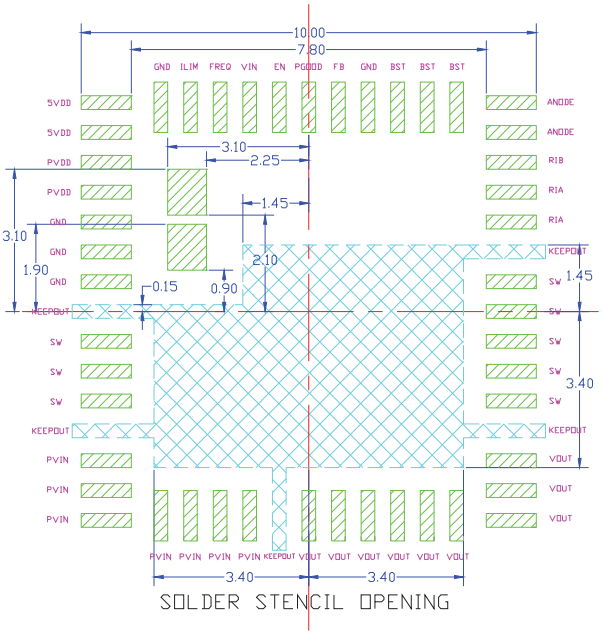
Recommended Land Pattern

NOTE: 4, 5, 6

Simplified LP

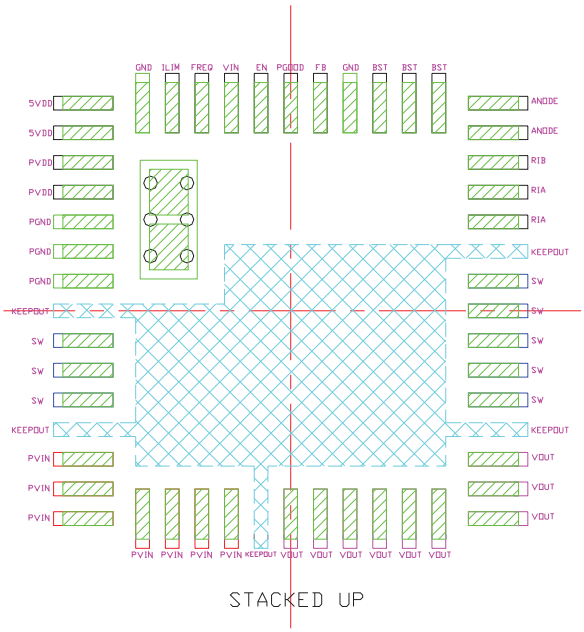




Recommended Land Pattern

NOTE: 4, 5, 6

Simplified LP



NOTE:

1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. BLACK CIRCLES IN LAND PATTERN REPRESENT THERMAL VIA, RECOMMENDED SIZE IS 0.30-0.35mm, AT 0.80mm PITCH & SHOULD BE CONNECTED TO GND FOR MAXIMUM PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA.
6. CYAN COLORED SHADED PAD REPRESENT EXPOSED TRACE KEEP OUT AREA.

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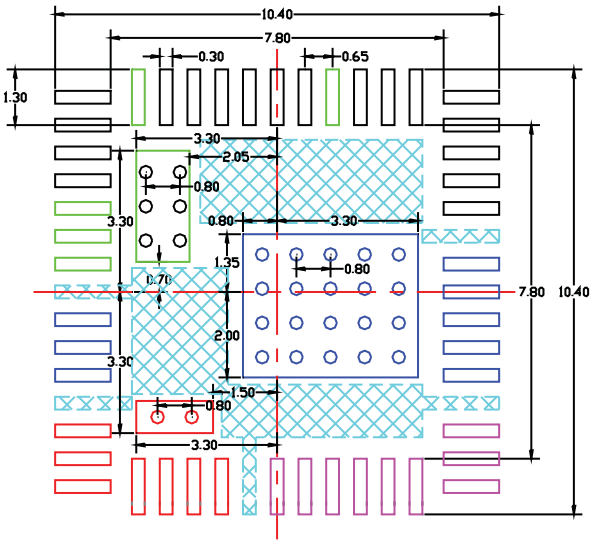
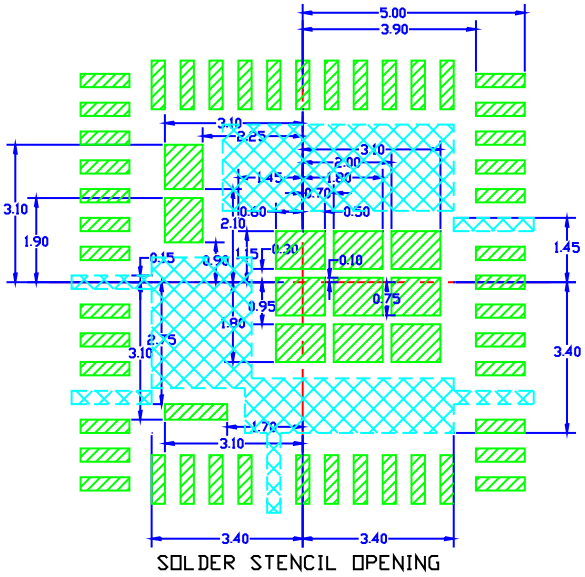
6.3 Thermally Enhanced Landing Pattern





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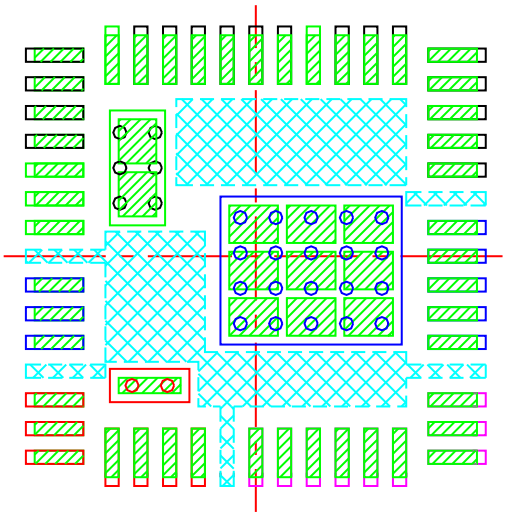
6.3 Thermally Enhanced Landing Pattern (Continued)



STACKED UP

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. BLACK CIRCLES IN LAND PATTERN REPRESENT THERMAL VIA, RECOMMENDED SIZE IS 0.30-0.35mm, AT 0.80mm PITCH & SHOULD BE CONNECTED TO GND FOR MAXIMUM PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA.
6. CYAN COLORED SHADED PAD REPRESENT EXPOSED TRACE KEEP OUT AREA.

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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APPENDIX A: REVISION HISTORY

Revision A (November 2017)

- Converted Micrel document MIC45208-1/-2 to Microchip data sheet DS20005603A.
- Minor text changes throughout document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	–	X	XXX	–	XX
Device		Option	Package		Media Type

Device:	MIC45208:	26V, 10A DC-to-DC Power Module	
Option:	1	=	HLL
	2	=	HSC
Package:	YMP	=	52-Pin 10 mm x 10 mm B2QFN
Media Type:	T1	=	100/Reel
	TR	=	5,000/Reel

Examples:

a) MIC45208-1YMP-T1: MIC45208, HLL, 52-Pin B2QFN, 100/Reel

b) MIC45208-1YMP-TR: MIC45208, HLL, 52-Pin B2QFN, 5,000/Reel

c) MIC45208-2YMP-T1: MIC45208, HSC, 52-Pin B2QFN, 100/Reel

d) MIC45208-2YMP-TR: MIC45208-2, HSC, 52-Pin B2QFN, 5,000/Reel

NOTES:

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