25AA1024

1-Mbit SPI Bus Serial EEPROM

Device Selection Table

Part Number	Vcc Range	Page Size	Temp. Ranges	Packages
25AA1024	1.8-5.5V	256 Byte	I	MF, P, SM

Features

- Maximum Clock: 20 MHz
- Byte and Page-level Write Operations:
  - 256 byte page
  - 6 ms maximum write cycle time
  - No page or sector erase required
- Low-Power CMOS Technology:
  - Max. Write current: 7 mA at 5.5V
  - Max. Read current: 10 mA at 5.5V, 20 MHz
  - Standby current: 1 µA at 2.5V, 85°C (Deep Power-down)
- Electronic Signature for Device ID
- Self-Timed Erase and Write Cycles:
  - Page Erase (6 ms maximum)
  - Sector Erase (10 ms maximum)
  - Chip Erase (10 ms maximum)
- Sector Write Protection (32K byte/sector):
  - Protect none, 1/4, 1/2 or all of array
- Built-in Write Protection:
  - Power-on/off data protection circuitry
  - Write enable latch
  - Write-protect pin
- High Reliability:
  - Endurance: 1M erase/write cycles
  - Data Retention: >200 years
  - ESD Protection: 4000V
- Temperature Ranges Supported:
  - Industrial (I):-40°C to +85°C
- RoHS Compliant
- Automotive AEC-Q100 Qualified

Pin Function Table

Name	Function
$\overline{\text{CS}}$	Chip Select Input
SO	Serial Data Output
$\overline{\text{WP}}$	Write-Protect
Vss	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{\text{HOLD}}$	Hold Input
Vcc	Supply Voltage

Description

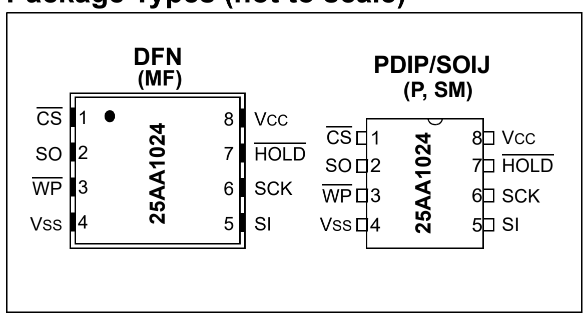
The Microchip Technology Inc. 25AA1024 is a 1024-Kbit serial EEPROM memory with byte-level and page-level serial EEPROM functions. It also features Page, Sector and Chip erase instructions typically associated with Flash-based products. These instructions are not required for byte or page write operations. The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled by a Chip Select ($\overline{\text{CS}}$) input.

Communication to the device can be paused via the hold pin ($\overline{\text{HOLD}}$). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

Packages

- 8-Lead DFN, 8-Lead PDIP and 8-Lead SOIJ

Package Types (not to scale)



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

V_{CC} 6.5V
All inputs and outputs w.r.t. V_{SS} .... -0.6V to V_{CC} +1.0V
Storage temperature .... -65°C to 150°C
Ambient temperature under bias .... -40°C to 125°C
ESD protection on all pins .... 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			**Electrical Characteristics:** Industrial (I)*: T_A = 0°C to +85°C, V_{CC} = 1.8V to 5.5V Industrial (I): T_A = -40°C to +85°C, V_{CC} = 2.0V to 5.5V * Limited industrial temperature range.			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
D001	V_{IH1}	High-level Input Voltage	0.7 V_{CC}	V_{CC} +1	V	
D002	V_{IL1}	Low-level Input Voltage	-0.3	0.3 V_{CC}	V	$V_{CC} \geq 2.7V$
D003	V_{IL2}		-0.3	0.2 V_{CC}	V	V_{CC} < 2.7V
D004	V_{OL}	Low-level Output Voltage	—	0.4	V	I_{OL} = 2.1 mA
D005	V_{OL}		—	0.2	V	I_{OL} = 1.0 mA, V_{CC} < 2.5V
D006	V_{OH}	High-level Output Voltage	V_{CC} -0.2	—	V	I_{OH} = -400 µA
D007	I_{LI}	Input Leakage Current	—	±1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}
D008	I_{LO}	Output Leakage Current	—	±1	µA	$\overline{CS}$ = V_{CC}, V_{OUT} = V_{SS} or V_{CC}
D009	C_{INT}	Internal Capacitance (all inputs and outputs)	—	7	pF	T_A = 25°C, CLK = 1.0 MHz, V_{CC} = 5.0V (**Note**)
D010	I_{CC}read	Operating Current	—	10	mA	V_{CC} = 5.5V; F_{CLK} = 20.0 MHz; SO = Open
			—	5	mA	V_{CC} = 2.5V; F_{CLK} = 10.0 MHz; SO = Open
D011	$I_{CCWRITE}$		—	7	mA	V_{CC} = 5.5V
			—	5	mA	V_{CC} = 2.5V
D012	I_{CCS}	Standby Current	—	12	µA	$\overline{CS}$ = V_{CC} = 5.5V, Inputs tied to V_{CC} or V_{SS}, 85°C
D013	I_{CCSPD}	Deep Power-down Current	—	1	µA	$\overline{CS}$ = V_{CC} = 2.5V, Inputs tied to V_{CC} or V_{SS}, 85°C

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I)*: T_A = 0°C to +85°C V_{CC} = 1.8V to 5.5V Industrial (I): T_A = -40°C to +85°C V_{CC} = 2.0V to 5.5V *Limited industrial temperature range.			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	F_{CLK}	Clock Frequency	—	20	MHz	$4.5 \le V_{CC} \le 5.5$
			—	10	MHz	$2.5 \le V_{CC} < 4.5$
			—	2	MHz	$2.0 \le V_{CC} < 2.5$ $1.8 \le V_{CC} < 2.0$, 0°C to +85°C
2	T_{CSS}	$\overline{CS}$ Setup Time	25	—	ns	$4.5 \le V_{CC} \le 5.5$
			50	—	ns	$2.5 \le V_{CC} < 4.5$
			250	—	ns	$2.0 \le V_{CC} < 2.5$ $1.8 \le V_{CC} < 2.0$, 0°C to +85°C
3	T_{CSH}	$\overline{CS}$ Hold Time	50	—	ns	$4.5 \le V_{CC} \le 5.5$
			100	—	ns	$2.5 \le V_{CC} < 4.5$
			500	—	ns	$2.0 \le V_{CC} < 2.5$ $1.8 \le V_{CC} < 2.0$, 0°C to +85°C (**Note 3**)
4	T_{CSD}	$\overline{CS}$ Disable Time	50	—	ns	
5	T_{SU}	Data Setup Time	5	—	ns	$4.5 \le V_{CC} \le 5.5$
			10	—	ns	$2.5 \le V_{CC} < 4.5$
			50	—	ns	$2.0 \le V_{CC} < 2.5$ $1.8 \le V_{CC} < 2.0$, 0°C to +85°C
6	T_{HD}	Data Hold Time	10	—	ns	$4.5 \le V_{CC} \le 5.5$
			20	—	ns	$2.5 \le V_{CC} < 4.5$
			100	—	ns	$2.0 \le V_{CC} < 2.5$ $1.8 \le V_{CC} < 2.0$, 0°C to +85°C
7	T_R	CLK Rise Time	—	20	ns	(**Note 1**)
8	T_F	CLK Fall Time	—	20	ns	(**Note 1**)
9	T_{HI}	Clock High Time	25	—		$4.5 \le V_{CC} \le 5.5$
			50	—	ns	$2.5 \le V_{CC} < 4.5$
			250	—	ns	$2.0 \le V_{CC} < 2.5$ $1.8 \le V_{CC} < 2.0$, 0°C to +85°C
10	T_{LO}	Clock Low Time	25	—	ns	$4.5 \le V_{CC} \le 5.5$
			50	—	ns	$2.5 \le V_{CC} < 4.5$
			250	—	ns	$2.0 \le V_{CC} < 2.5$ $1.8 \le V_{CC} < 2.0$, 0°C to +85°C
11	T_{CLD}	Clock Delay Time	50	—	ns	
12	T_{CLE}	Clock Enable Time	50	—	ns	
13	T_V	Output Valid from Clock Low	—	25	ns	$4.5 \le V_{CC} \le 5.5$
			—	50	ns	$2.5 \le V_{CC} < 4.5$
			—	250	ns	$2.0 \le V_{CC} < 2.5$ $1.8 \le V_{CC} < 2.0$, 0°C to +85°C

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but established by characterization and qualification.

3: Includes T_{HI} time.

TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I)*: TA = 0°C to +85°C VCC = 1.8V to 5.5V Industrial (I): TA = -40°C to +85°C VCC = 2.0V to 5.5V *Limited industrial temperature range.			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
14	THO	Output Hold Time	0	—	ns	(Note 1)
15	TDIS	Output Disable Time	—	25	ns	4.5 ≤ VCC ≤ 5.5
			—	50	ns	2.5 ≤ VCC < 4.5
			—	250	ns	2.0 ≤ VCC < 2.5 1.8 ≤ VCC < 2.0, 0°C to +85°C (Note 1)
16	THS	$\overline{\text{HOLD}}$ Setup Time	10	—	ns	4.5 ≤ VCC ≤ 5.5
			20	—	ns	2.5 ≤ VCC < 4.5
			100	—	ns	2.0 ≤ VCC < 2.5 1.8 ≤ VCC < 2.0, 0°C to +85°C
17	THH	$\overline{\text{HOLD}}$ Hold Time	10	—	ns	4.5 ≤ VCC ≤ 5.5
			20	—	ns	2.5 ≤ VCC < 4.5
			100	—	ns	2.0 ≤ VCC < 2.5 1.8 ≤ VCC < 2.0, 0°C to +85°C
18	THZ	$\overline{\text{HOLD}}$ Low to Output High Z	—	15	ns	4.5 ≤ VCC ≤ 5.5
			—	30	ns	2.5 ≤ VCC < 4.5
			—	150	ns	2.0 ≤ VCC < 2.5 1.8 ≤ VCC < 2.0, 0°C to +85°C (Note 1)
19	THV	$\overline{\text{HOLD}}$ High to Output Valid	—	15	ns	4.5 ≤ VCC ≤ 5.5
			—	30	ns	2.5 ≤ VCC < 4.5
			—	150	ns	2.0 ≤ VCC < 2.5 1.8 ≤ VCC < 2.0, 0°C to +85°C
20	TREL	$\overline{\text{CS}}$ High to Standby mode	—	100	µs	VCC = 1.8V to 5.5V
21	TPD	$\overline{\text{CS}}$ High to Deep Power-down	—	100	µs	VCC = 1.8V to 5.5V
22	TCE	Chip Erase Cycle Time	—	10	ms	VCC = 1.8V to 5.5V
23	TSE	Sector Erase Cycle Time	—	10	ms	VCC = 1.8V to 5.5V
24	TWC	Internal Write Cycle Time	—	6	ms	Byte or Page mode and Page Erase
25	—	Endurance	1M	—	E/W cycles	Page mode, 25°C, 5.5V (Note 2)

Note 1: This parameter is periodically sampled and not 100% tested.
2: This parameter is not tested but established by characterization and qualification.
3: Includes THI time.

TABLE 1-3: AC TEST CONDITIONS

AC Waveform	
VLO = 0.2V	—
VHI = VCC - 0.2V	(Note 1)
VHI = 4.0V	(Note 2)
CL = 30 pF	—
Timing Measurement Reference Level	
Input	0.5 VCC
Output	0.5 VCC

Note 1: For VCC ≤ 4.0V
2: For VCC > 4.0V

FIGURE 1-1: HOLD TIMING

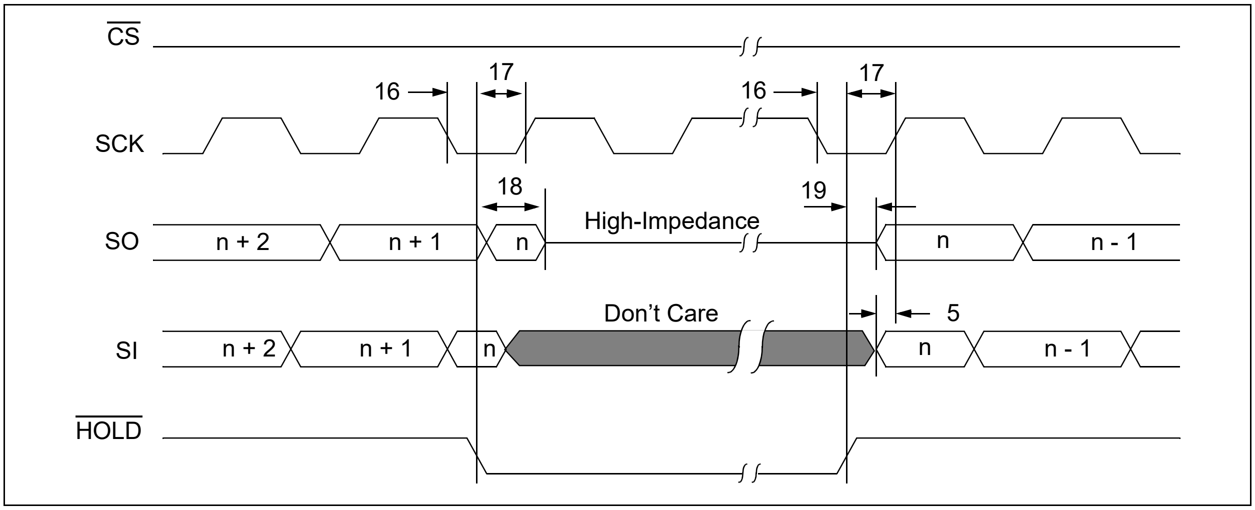


FIGURE 1-2: SERIAL INPUT TIMING

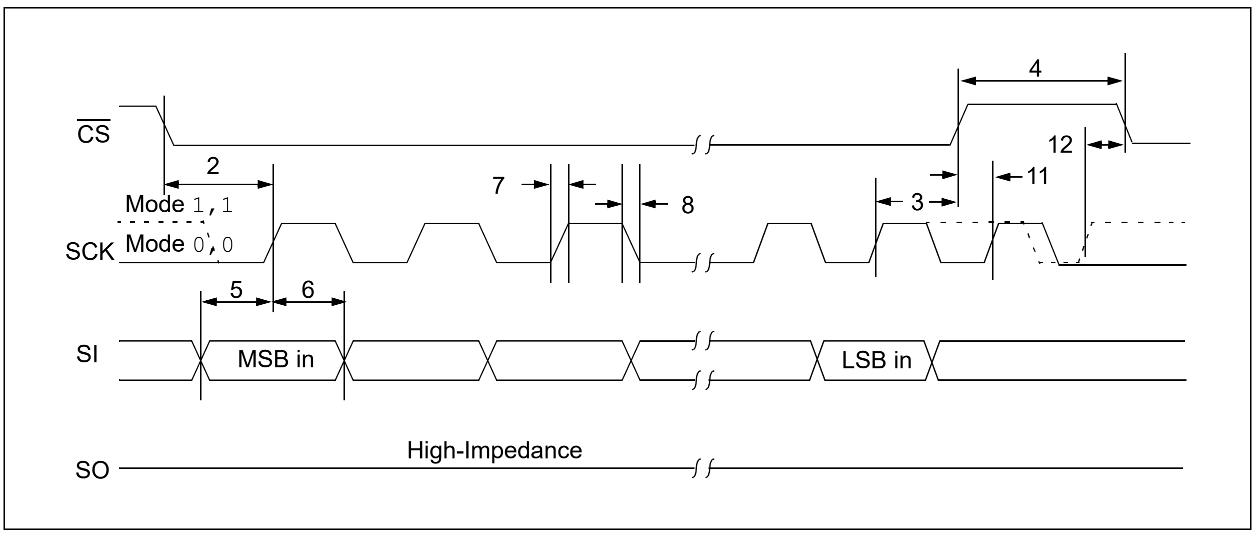
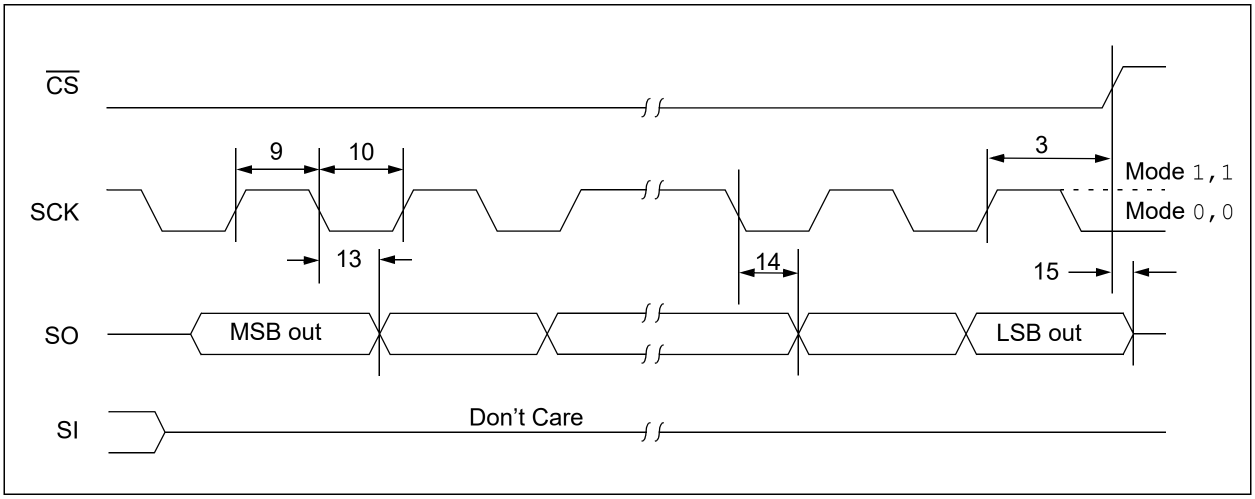


FIGURE 1-3: SERIAL OUTPUT TIMING



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	8-Lead DFN-S(1)	8-Lead PDIP	8-Lead SOIJ	Function
CS	1	1	1	Chip Select Input
SO	2	2	2	Serial Data Output
WP	3	3	3	Write-Protect Pin
Vss	4	4	4	Ground
SI	5	5	5	Serial Data Input
SCK	6	6	6	Serial Clock Input
HOLD	7	7	7	Hold Input
Vcc	8	8	8	Supply Voltage

Note 1: The exposed pad on DFN-S package can be connected to VSS or left floating.

2.1 Chip Select (CS)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the CS input signal. If CS is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on CS after a valid write sequence initiates an internal write cycle. After power-up, a low level on CS is required prior to any sequence being initiated.

2.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25AA1024. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

2.3 Write-Protect (WP)

This pin is used in conjunction with the WPEN bit in the STATUS register to prohibit writes to the nonvolatile bits in the STATUS register. When WP is low and WPEN is high, writing to the nonvolatile bits in the STATUS register is disabled. All other operations function normally. When WP is high, all functions, including writes to the nonvolatile bits in the STATUS register, operate normally. If the WPEN bit is set, WP low during a STATUS register write sequence will disable writing to the STATUS register. If an internal write cycle has already begun, WP going low will have no effect on the write.

The WP pin function is blocked when the WPEN bit in the STATUS register is low. This allows the user to install the 25AA1024 in a system with WP pin grounded and still be able to write to the STATUS register. The WP pin functions will be enabled when the WPEN bit is set high.

2.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

2.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a host and the 25AA1024. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

2.6 Hold (HOLD)

The HOLD pin is used to suspend transmission to the 25AA1024 while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the HOLD pin may be pulled low to pause further serial communication without resetting the serial sequence.

The HOLD pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-to-low transition. The 25AA1024 must remain selected during this sequence. The SI and SCK levels are “don’t care” during the time the device is paused and any transitions on these pins will be ignored. To resume serial communication, HOLD must be brought high while the SCK pin is low, otherwise serial communication will not be resumed until the next SCK high-to-low transition.

The SO line will tri-state immediately upon a high-to-low transition of the HOLD pin and will begin outputting again immediately upon a subsequent low-to-high transition of the HOLD pin, independent of the state of SCK.

3.0 FUNCTIONAL DESCRIPTION

3.1 Principles of Operation

The 25AA1024 is a 131,072 byte Serial EEPROM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in firmware to match the SPI protocol.

The 25AA1024 contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The CS pin must be low and the HOLD pin must be high for the entire operation.

Table 3-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses and data are transferred MSB first, LSB last.

Data (SI) is sampled on the first rising edge of SCK after CS goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the HOLD input and place the 25AA1024 in 'HOLD' mode. After releasing the HOLD pin, operation will resume from the point when the HOLD was asserted.

BLOCK DIAGRAM

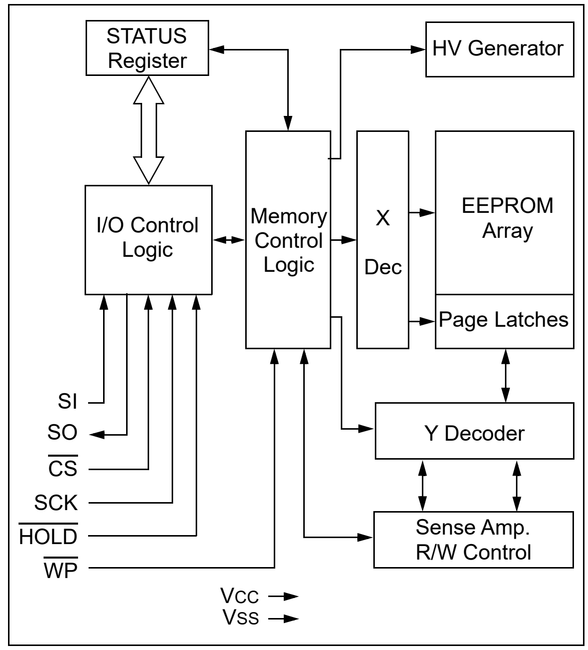


TABLE 3-1: INSTRUCTION SET

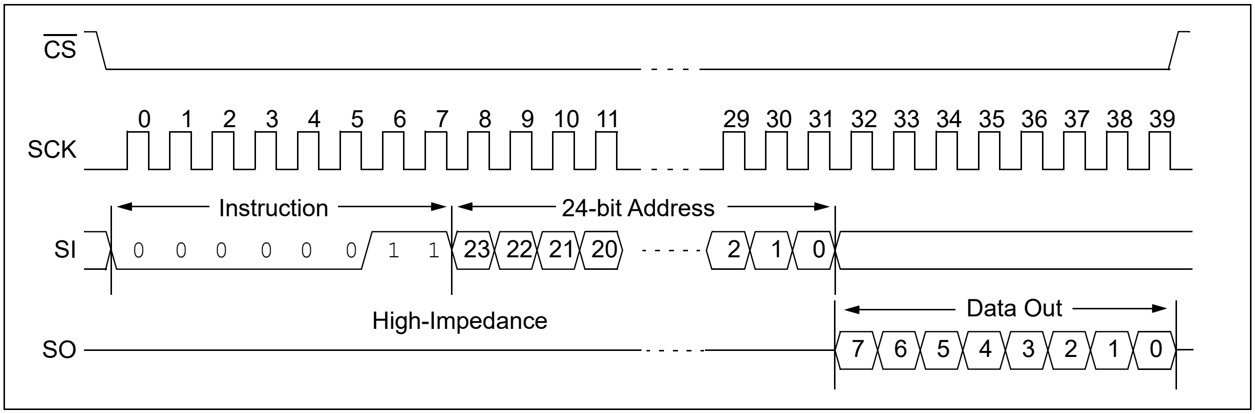
Instruction Name	Instruction Format	Description
READ	0000 0011	Read data from memory array beginning at selected address
WRITE	0000 0010	Write data to memory array beginning at selected address
WREN	0000 0110	Set the write enable latch (enable write operations)
WRDI	0000 0100	Reset the write enable latch (disable write operations)
RDSR	0000 0101	Read STATUS register
WRSR	0000 0001	Write STATUS register
PE	0100 0010	Page Erase – erase one page in memory array
SE	1101 1000	Sector Erase – erase one sector in memory array
CE	1100 0111	Chip Erase – erase all sectors in memory array
RDID	1010 1011	Release from Deep Power-down and Read Electronic Signature
DPD	1011 1001	Deep Power-Down mode

3.2 Read Sequence

The device is selected by pulling $\overline{CS}$ low. The 8-bit `READ` instruction is transmitted to the 25AA1024 followed by the 24-bit address, with seven MSBs of the address being "don't care" bits. After the correct `READ` instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin.

The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal Address Pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (1FFFFh), the address counter rolls over to address, 00000h, allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin (Figure 3-1).

FIGURE 3-1: READ SEQUENCE



3.3 Write Sequence

Prior to any attempt to write data to the 25AA1024, the write enable latch must be set by issuing the `WREN` instruction (Figure 3-4). This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25AA1024. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch. If the write operation is initiated immediately after the `WREN` instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

A write sequence includes an automatic, self-timed erase cycle. It is not required to erase any portion of the memory prior to issuing a Write command.

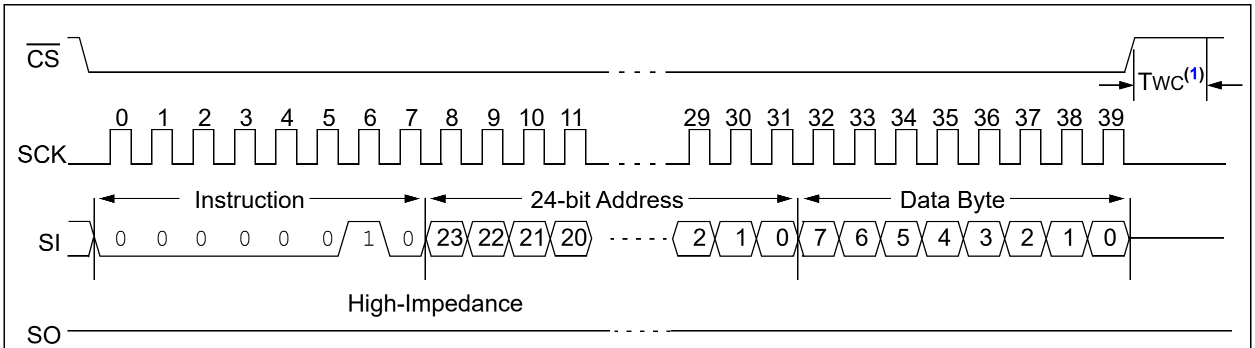
Once the write enable latch is set, the user may proceed by setting the $\overline{CS}$ low, issuing a `WRITE` instruction, followed by the 24-bit address, with seven MSBs of the address being "don't care" bits, and then the data to be written. Up to 256 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page.

Note: When doing a write of less than 256 bytes the data in the rest of the page is refreshed along with the data bytes being written. This will force the entire page to endure a write cycle, for this reason endurance is specified per page.

Note: Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size'), and end at addresses that are integer multiples of page size – 1. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

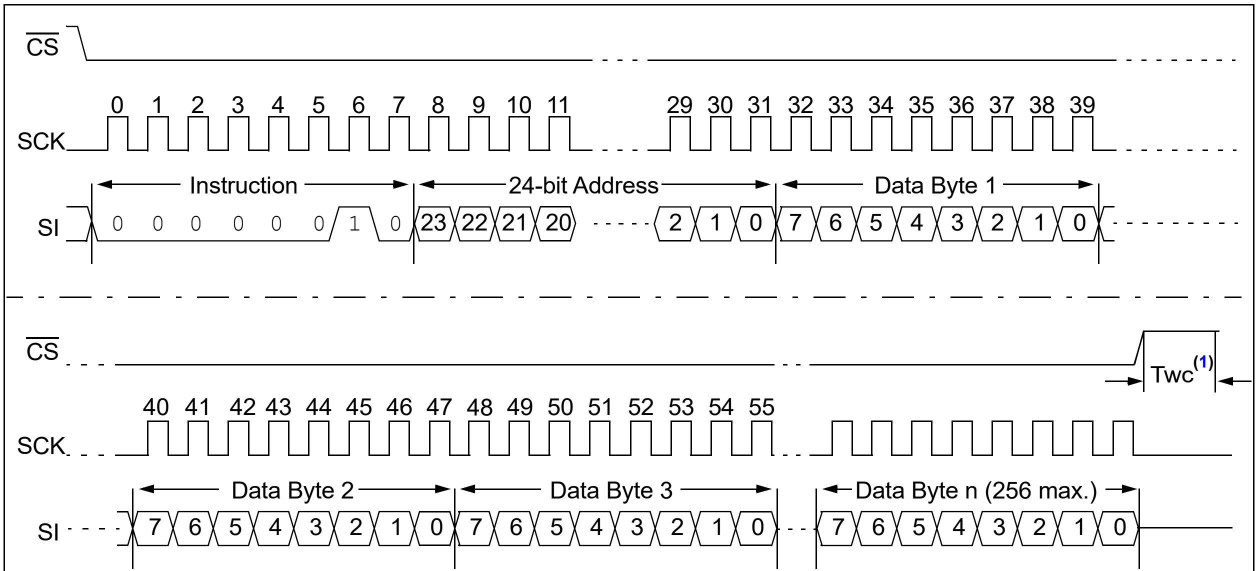
For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the Least Significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{CS}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 3-2 and Figure 3-3 for more detailed illustrations on the byte write sequence and the page write sequence, respectively. While the write is in progress, the STATUS register may be read to check the status of the WPEN, WIP, WEL, BP1 and BP0 bits (Figure 3-6). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

FIGURE 3-2: BYTE WRITE SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

FIGURE 3-3: PAGE WRITE SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of CS after a valid sequence.

3.4 Write Enable (WREN) and Write Disable (WRDI)

The 25AA1024 contains a write enable latch. See Table 3-4 for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed
- PE instruction successfully executed
- SE instruction successfully executed
- CE instruction successfully executed

FIGURE 3-4: WRITE ENABLE SEQUENCE (WREN)

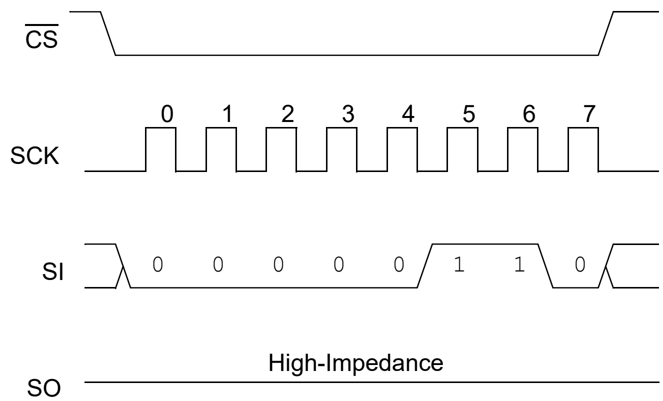
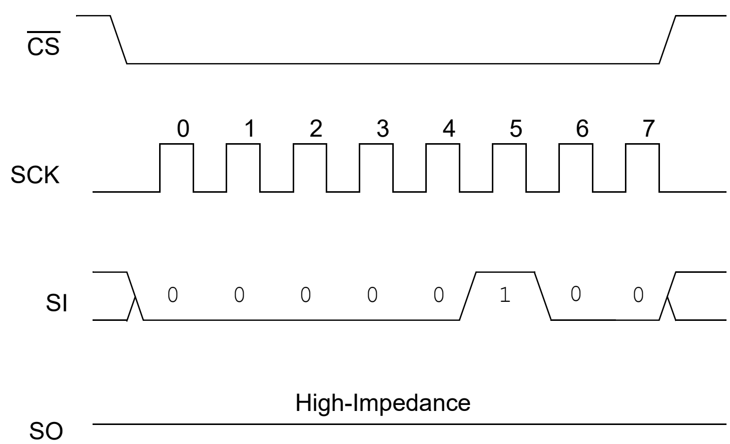


FIGURE 3-5: WRITE DISABLE SEQUENCE (WRDI)



3.5 Read Status Register Instruction (RDSR)

The Read Status Register instruction (RDSR) provides access to the STATUS register. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

TABLE 3-2: STATUS REGISTER

7	6	5	4	3	2	1	0
W/R	–	–	–	W/R	W/R	R	R
WPEN	X	X	X	BP1	BP0	WEL	WIP

Note: W/R = writable/readable. R = read-only.

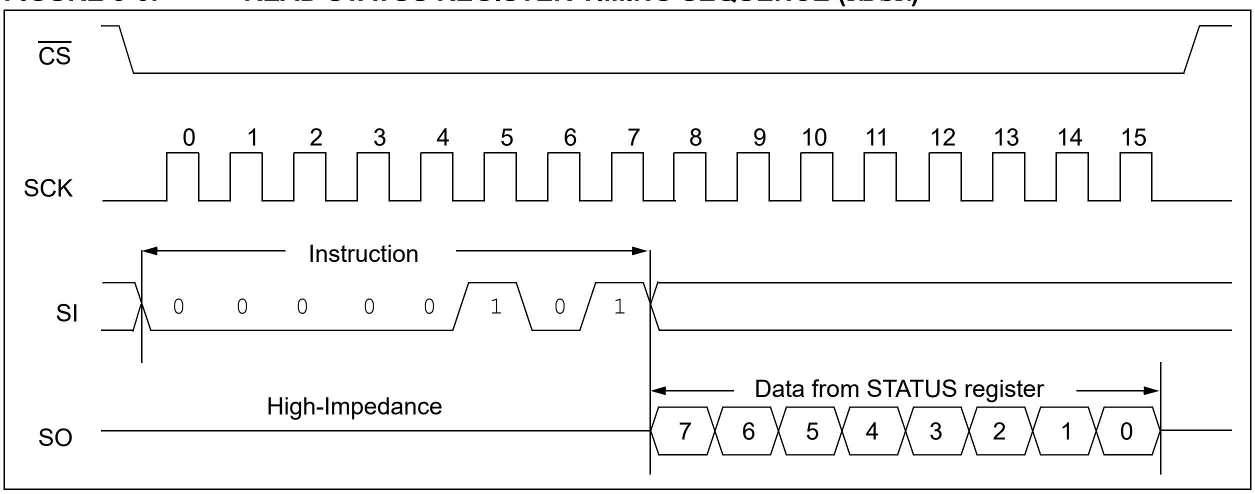
The **Write-In-Process (WIP)** bit indicates whether the 25AA1024 is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch and is read-only. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the STATUS register. These commands are shown in Figure 3-4 and Figure 3-5.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user issuing the WRSR instruction. These bits are nonvolatile and are shown in Table 3-3.

See Figure 3-6 for the RDSR timing sequence.

FIGURE 3-6: READ STATUS REGISTER TIMING SEQUENCE (RDSR)



3.6 Write Status Register Instruction (WRSR)

The Write Status Register instruction (WRSR) allows the user to write to the nonvolatile bits in the STATUS register, as shown in Table 3-2. The user is able to select one of four levels of protection for the array by writing to the appropriate bits in the STATUS register. The array is divided up into four segments. The user has the ability to write-protect none, one, two, or all four of the segments of the array. The partitioning is controlled, as shown in Table 3-3.

The Write-Protect Enable (WPEN) bit is a nonvolatile bit that is available as an enable bit for the $\overline{WP}$ pin. The Write-Protect ($\overline{WP}$) pin and the Write-Protect Enable (WPEN) bit in the STATUS register control the programmable hardware write-protect feature. Hardware write protection is enabled when the $\overline{WP}$ pin is low and the WPEN bit is high. Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is low. When the chip is hardware write-protected, only writes to nonvolatile bits in the STATUS register are disabled. See Table 3-4 for a matrix of functionality on the WPEN bit.

See Figure 3-7 for the WRSR timing sequence.

TABLE 3-3: ARRAY PROTECTION

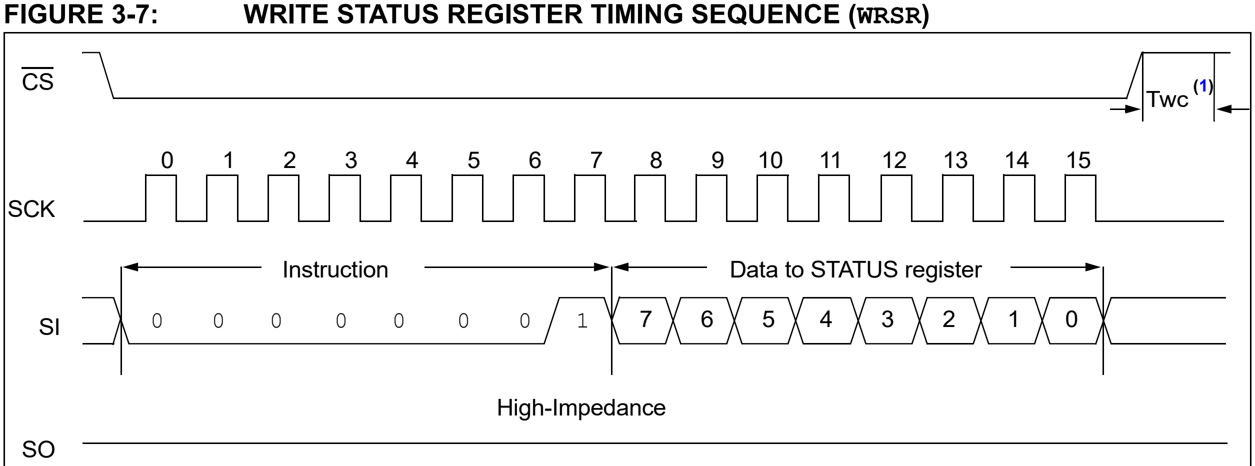
BP1	BP0	Array Addresses Write-Protected	Array Addresses Unprotected
0	0	none	All (Sectors 0, 1, 2 & 3) (00000h-1FFFFh)
0	1	Upper 1/4 (Sector 3) (18000h-1FFFFh)	Lower 3/4 (Sectors 0, 1 & 2) (00000h-17FFFh)
1	0	Upper 1/2 (Sectors 2 & 3) (10000h-1FFFFh)	Lower 1/2 (Sectors 0 & 1) (00000h-0FFFFh)
1	1	All (Sectors 0, 1, 2 & 3) (00000h-1FFFFh)	none

TABLE 3-4: WRITE-PROTECT FUNCTIONALITY MATRIX

WEL (SR bit 1)	WPEN (SR bit 7)	$\overline{WP}$ (pin 3)	Protected Blocks	Unprotected Blocks	STATUS Register
0	x	x	Protected	Protected	Protected
1	0	x	Protected	Writable	Writable
1	1	0 (low)	Protected	Writable	Protected
1	1	1 (high)	Protected	Writable	Writable

x = don't care

FIGURE 3-7: WRITE STATUS REGISTER TIMING SEQUENCE (WRSR)



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of CS after a valid sequence.

3.7 PAGE ERASE

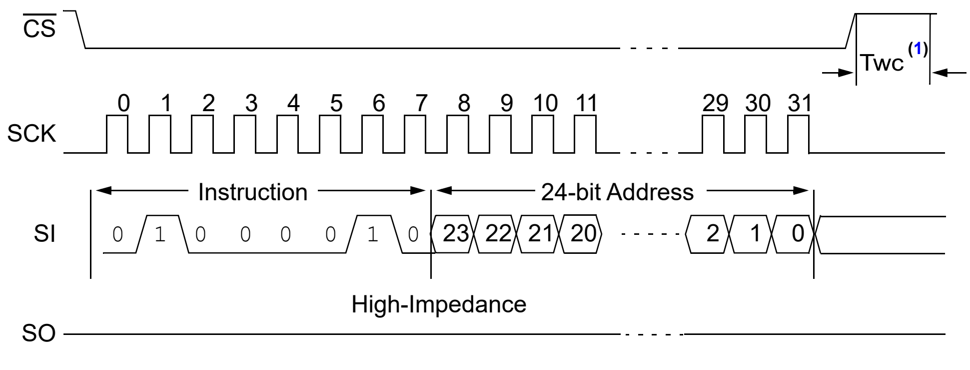
The PAGE ERASE instruction will erase all bits (FFh) inside the given page. A Write Enable (WREN) instruction must be given prior to attempting a Page Erase. This is done by setting CS low and then clocking out the proper instruction into the 25AA1024. After all eight bits of the instruction are transmitted, the CS must be brought high to set the write enable latch.

The PAGE ERASE instruction is entered by driving CS low, followed by the instruction code (Figure 3-8), and three address bytes. Any address inside the page to be erased is a valid address.

CS must then be driven high after the last bit if the address or the PAGE ERASE will not execute. Once the CS is driven high, the self-timed Page Erase cycle is started. The WIP bit in the STATUS register can be read to determine when the Page Erase cycle is complete.

If a Page Erase instruction is given to an address that has been protected by the Block Protect bits (BP0, BP1) then the sequence will be aborted and no erase will occur.

FIGURE 3-8: PAGE ERASE SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of CS after a valid sequence.

3.8 SECTOR ERASE

The SECTOR ERASE instruction will erase all bits (FFh) inside the given sector. A Write Enable (WREN) instruction must be given prior to executing a Sector Erase. This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25AA1024. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch.

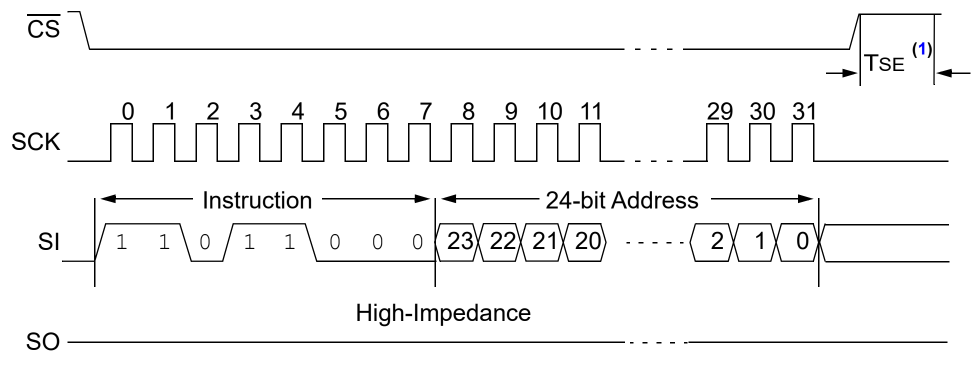
The SECTOR ERASE instruction is entered by driving $\overline{CS}$ low, followed by the instruction code (Figure 3-9), and three address bytes. Any address inside the sector to be erased is a valid address.

$\overline{CS}$ must then be driven high after the last bit if the address or the SECTOR ERASE will not execute. Once the $\overline{CS}$ is driven high, the self-timed Sector Erase cycle is started. The WIP bit in the STATUS register can be read to determine when the Sector Erase cycle is complete.

If a SECTOR ERASE instruction is given to an address that has been protected by the Block Protect bits (BP0, BP1) then the sequence will be aborted and no erase will occur.

See Table 3-3 for Sector Addressing.

FIGURE 3-9: SECTOR ERASE SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of CS after a valid sequence.

3.9 CHIP ERASE

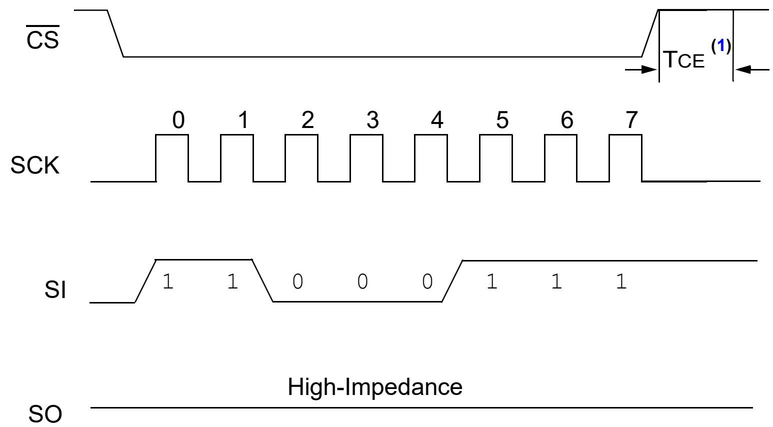
The CHIP ERASE instruction will erase all bits (FFh) in the array. A Write Enable (WREN) instruction must be given prior to executing a CHIP ERASE. This is done by setting CS low and then clocking out the proper instruction into the 25AA1024. After all eight bits of the instruction are transmitted, the CS must be brought high to set the write enable latch.

The CHIP ERASE instruction is entered by driving the CS low, followed by the instruction code (Figure 3-10) onto the SI line.

The CS pin must be driven high after the eighth bit of the instruction code has been given or the CHIP ERASE instruction will not be executed. Once the CS pin is driven high, the self-timed CHIP ERASE instruction begins. While the device is executing the CHIP ERASE instruction the WIP bit in the STATUS register can be read to determine when the CHIP ERASE instruction is complete.

The CHIP ERASE instruction is ignored if either of the Block Protect bits (BP0, BP1) are not 0, meaning ¼, ½, or all of the array is protected.

FIGURE 3-10: CHIP ERASE SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of CS after a valid sequence.

3.10 DEEP POWER-DOWN MODE

Deep Power-Down mode of the 25AA1024 is its lowest power consumption state. The device will not respond to any of the Read or Write commands while in Deep Power-Down mode, and therefore it can be used as an additional software write protection feature.

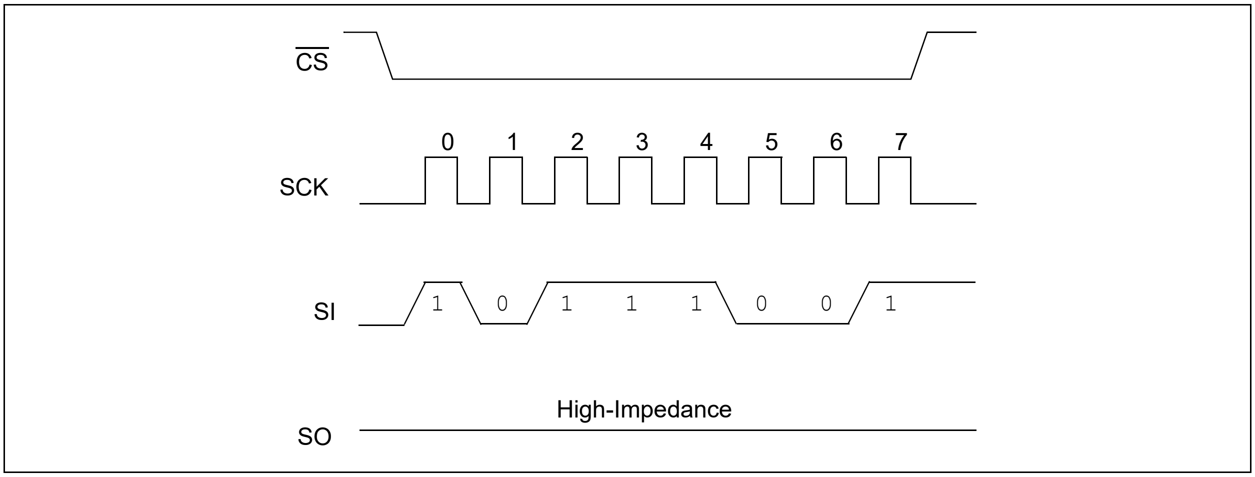
The Deep Power-Down mode is entered by driving $\overline{CS}$ low, followed by the instruction code (Figure 3-11) onto the SI line, followed by driving $\overline{CS}$ high.

If the $\overline{CS}$ pin is not driven high after the eighth bit of the instruction code has been given, the device will not execute Deep Power-down. Once the $\overline{CS}$ line is driven high, there is a delay (T_{DP}) before the current settles to its lowest consumption.

All instructions given during Deep Power-Down mode are ignored except the Read Electronic Signature Command (RDID). The RDID command will release the device from Deep Power-down and outputs the electronic signature on the SO pin, and then returns the device to Standby mode after delay (T_{REL}).

Deep Power-Down mode automatically releases at device power-down. Once power is restored to the device, it will power-up in the Standby mode.

FIGURE 3-11: DEEP POWER-DOWN SEQUENCE



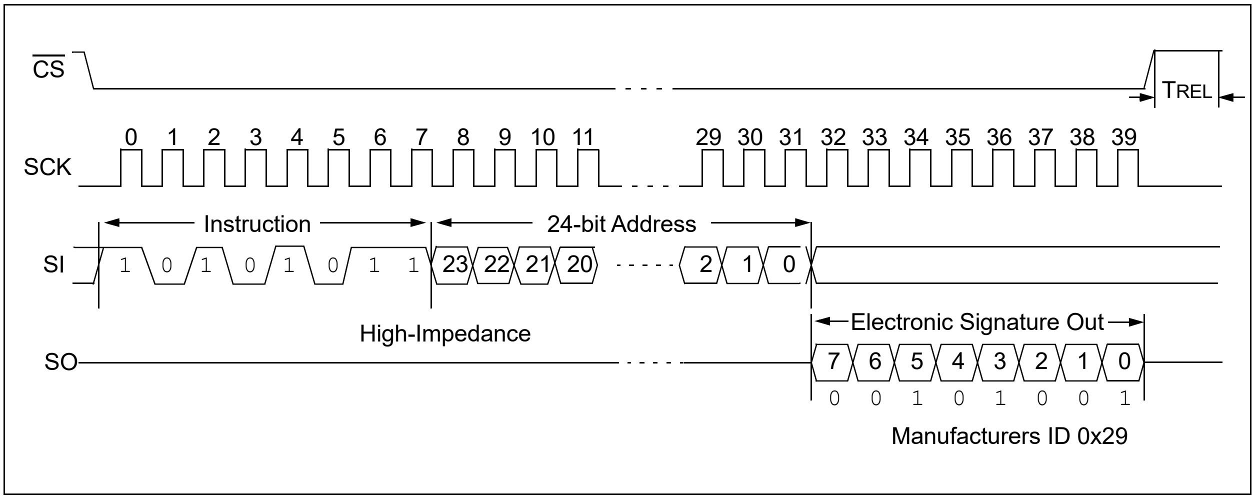
3.11 RELEASE FROM DEEP POWER-DOWN AND READ ELECTRONIC SIGNATURE

Once the device has entered Deep Power-Down mode, all instructions are ignored except the release from Deep Power-down and Read Electronic Signature command. This command can also be used when the device is not in Deep Power-down, to read the electronic signature out on the SO pin unless another command is being executed such as Erase, Program or Write STATUS register.

Release from Deep Power-Down mode and Read Electronic Signature is entered by driving $\overline{CS}$ low, followed by the `RDID` instruction code (Figure 3-12) and then a dummy address of 24 bits (A23-A0). After the last bit of the dummy address is clocked in, the 8-bit electronic signature is clocked out on the SO pin.

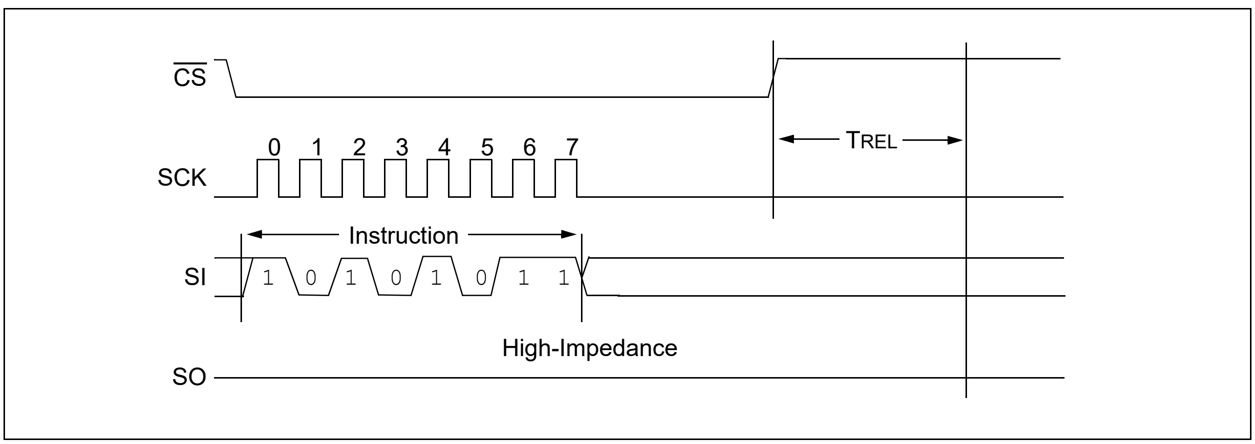
After the signature has been read out at least once, the sequence can be terminated by driving $\overline{CS}$ high. After a delay of TREL, the device will then return to Standby mode and will wait to be selected so it can be given new instructions. If additional clock cycles are sent after the electronic signature has been read once, it will continue to output the signature on the SO line until the sequence is terminated.

FIGURE 3-12: RELEASE FROM DEEP POWER-DOWN AND READ ELECTRONIC SIGNATURE



Driving $\overline{CS}$ high after the 8-bit RDID command, but before the electronic signature has been transmitted, will still ensure the device will be taken out of Deep Power-Down mode, as shown in Figure 3-13.

FIGURE 3-13: RELEASE FROM DEEP POWER-DOWN AND READ ELECTRONIC SIGNATURE



4.0 DATA PROTECTION

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or STATUS register write, the write enable latch is reset
- $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

5.0 POWER-ON STATE

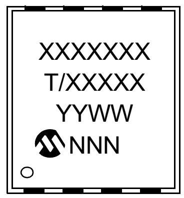
The 25AA1024 powers on in the following state:

- The device is in low-power Standby mode ($\overline{CS}$ = 1)
- The write enable latch is reset
- SO is in high-impedance state
- A high-to-low-level transition on $\overline{CS}$ is required to enter active state

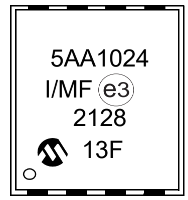
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

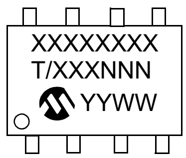
8-Lead DFN



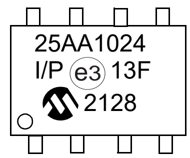
Example:



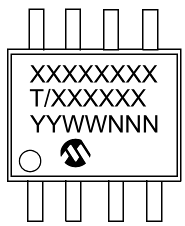
8-Lead PDIP



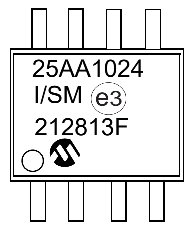
Example:



8-Lead SOIJ



Example:



1st Line Marking Codes			
Device	**DFN-S**	**PDIP**	**SOIJ**
25AA1024	25AA1024	25AA1024	25AA1024

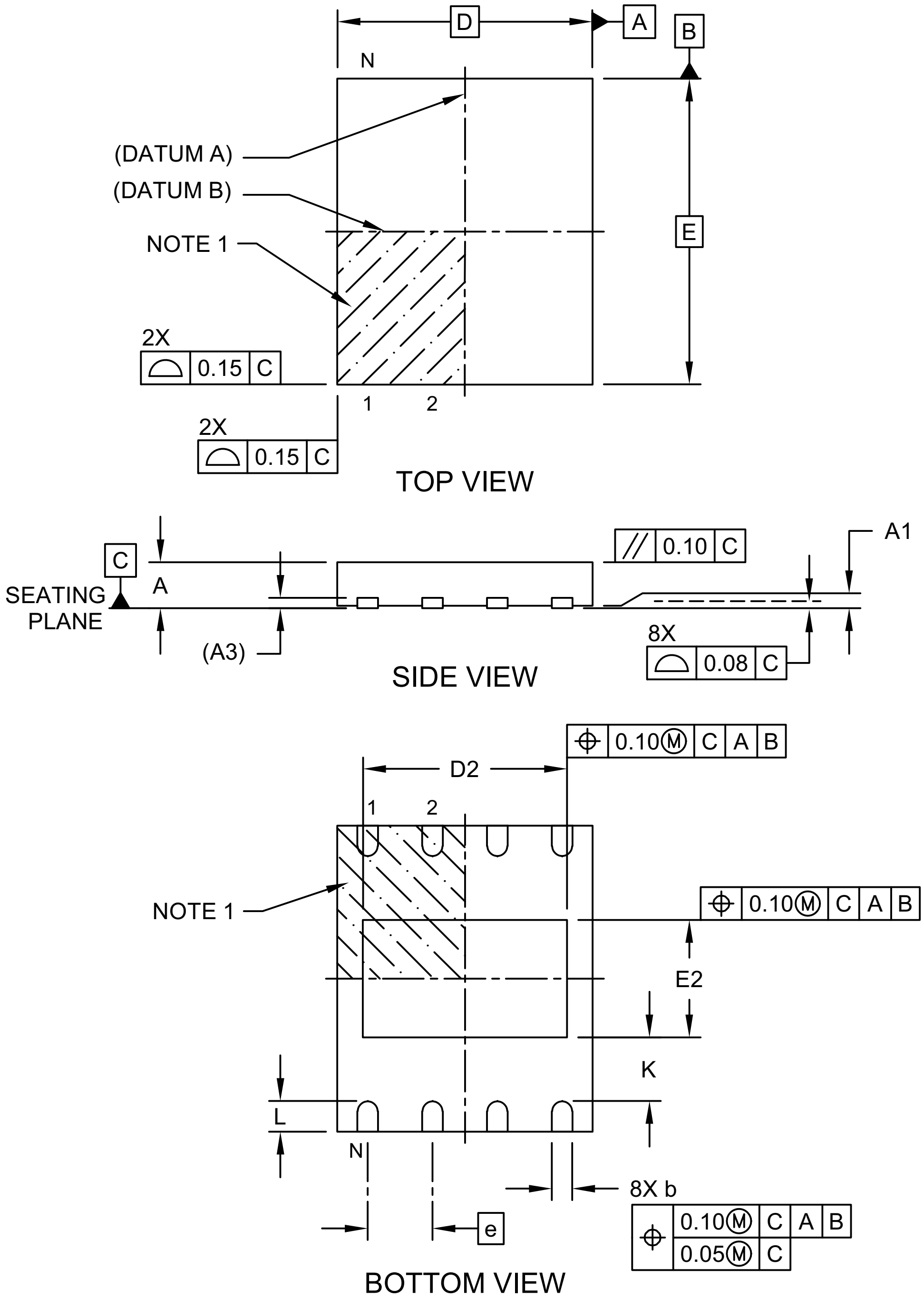
Legend:		
	XX...X	Part number or part number code
	T	Temperature (I)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	RoHS compliant JEDEC designator for Matte Tin (Sn)

Note: For very small packages with no room for the RoHS compliant JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

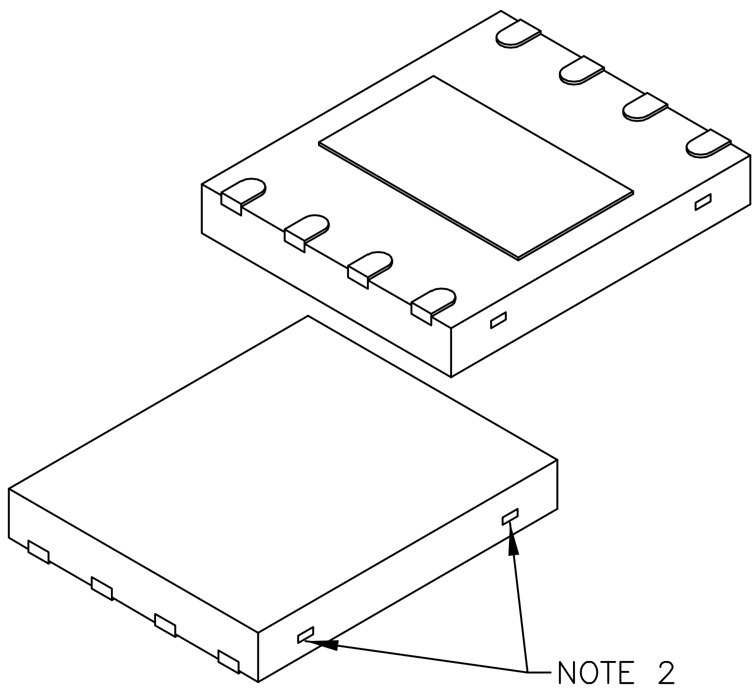
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-122 Rev C Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	0.80	0.85	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.90	4.00	4.10
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	2.20	2.30	2.40
Terminal Width	b	0.30	0.40	0.50
Terminal Length	L	0.50	0.60	0.75
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one ore more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

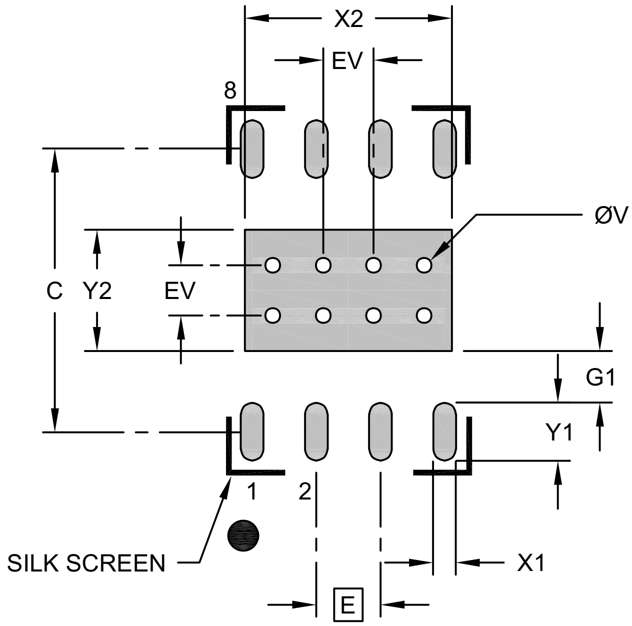
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-122 Rev C Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Optional Center Pad Width	X2			2.40
Optional Center Pad Length	Y2			4.10
Contact Pad Spacing	C		5.60	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.15
Contact Pad to Center Pad (X20)	G1	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

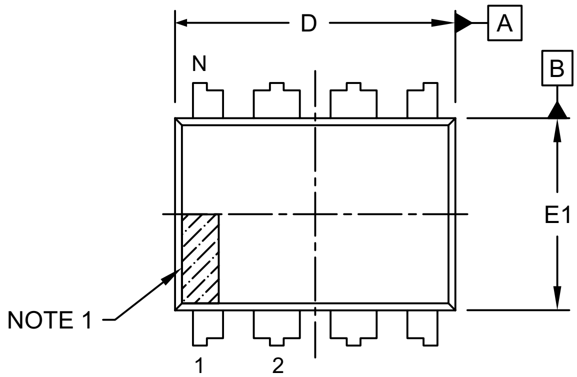
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

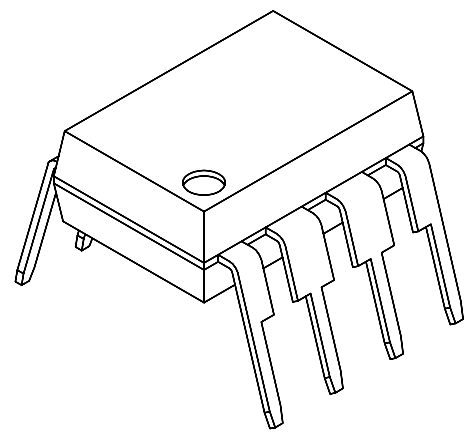
Microchip Technology Drawing C04-2122 Rev C

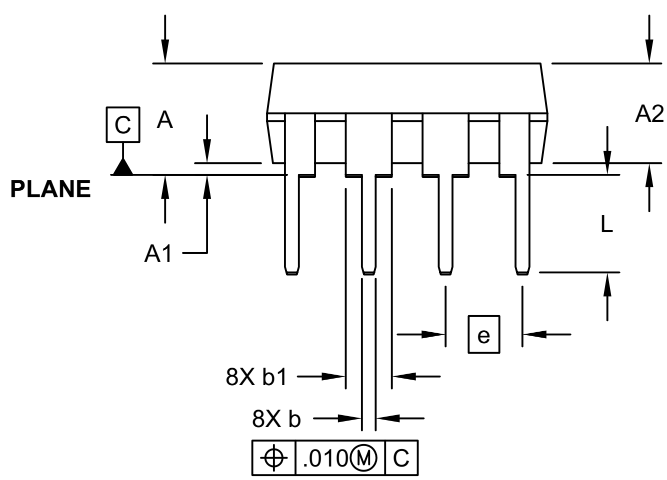
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

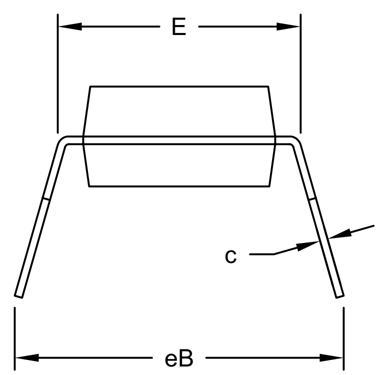


TOP VIEW





SIDE VIEW

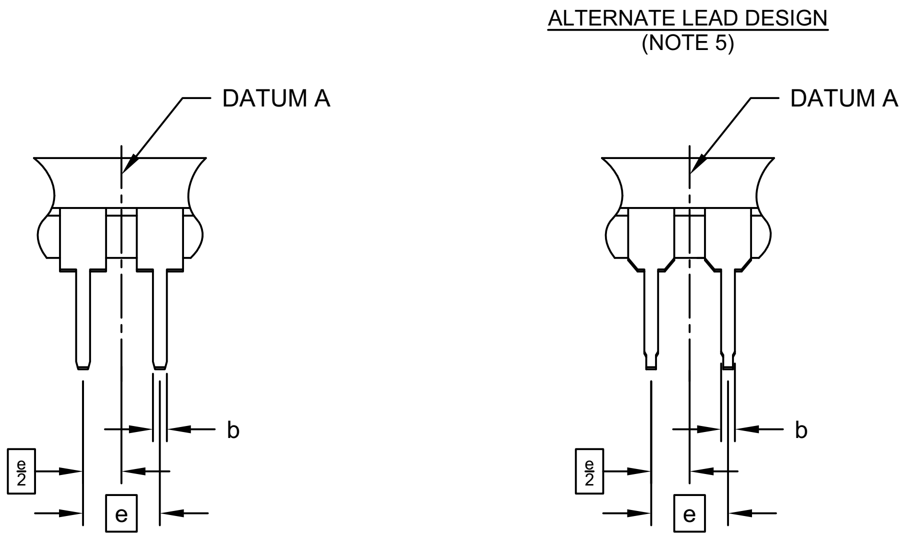


END VIEW

Microchip Technology Drawing No. C04-018-P Rev E Sheet 1 of 2

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

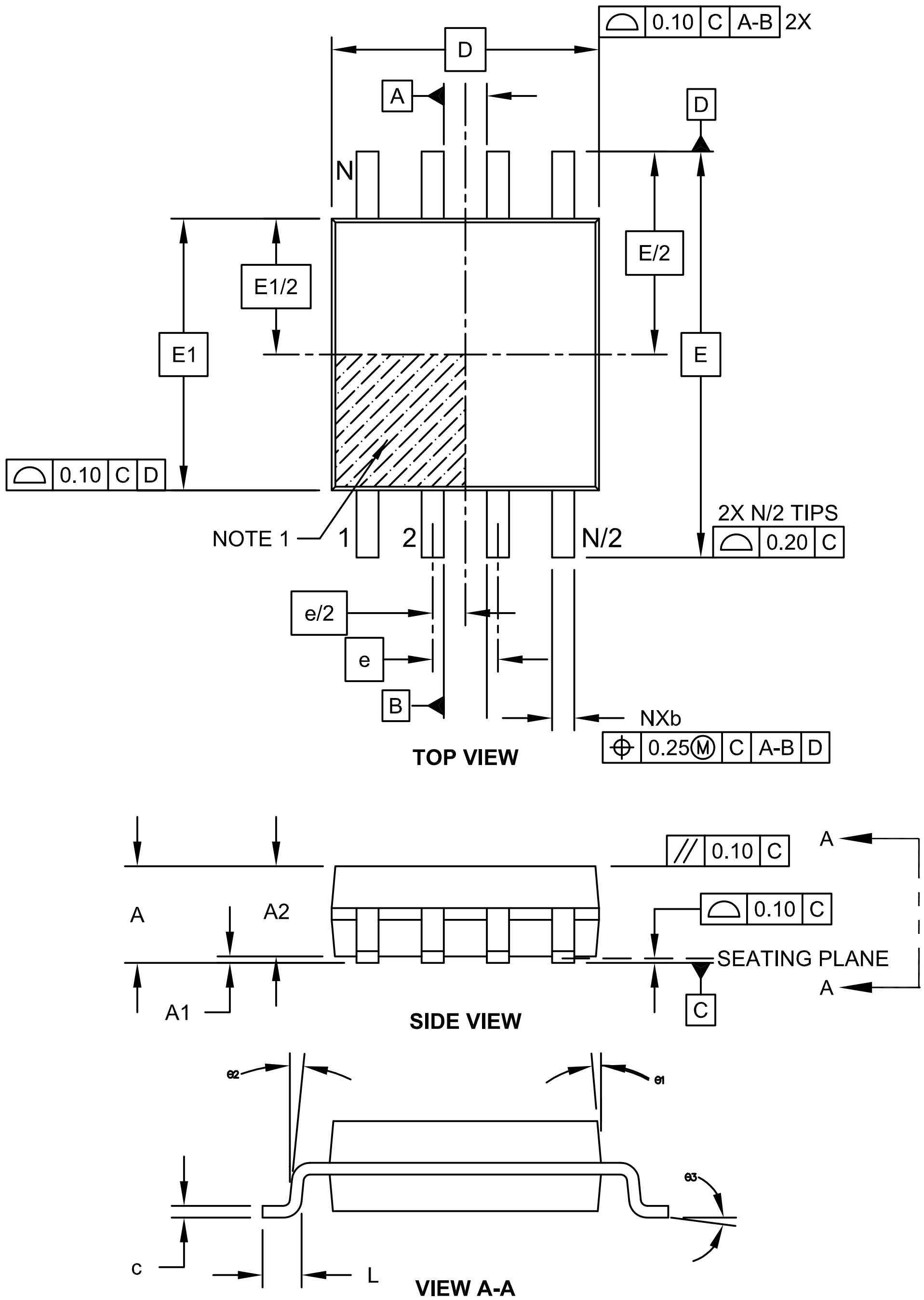
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev E Sheet 2 of 2

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

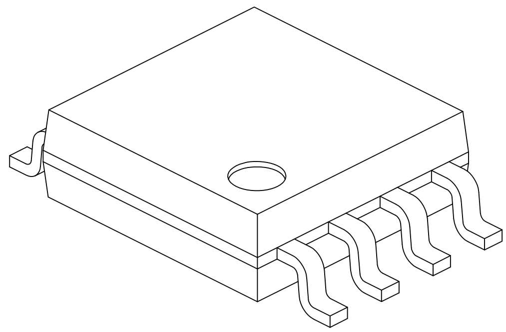
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-056C Sheet 1 of 2

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	1.77	-	2.03
Standoff §	A1	0.05		0.25
Molded Package Thickness	A2	1.75	-	1.98
Overall Width	E	7.94 BSC		
Molded Package Width	E1	5.25 BSC		
Overall Length	D	5.26 BSC		
Foot Length	L	0.51	-	0.76
Lead Thickness	c	0.15	-	0.25
Lead Width	b	0.36	-	0.51
Mold Draft Angle	Θ1	-	-	15°
Lead Angle	Θ2	0°	-	8°
Foot Angle	Θ3	0°	-	8°

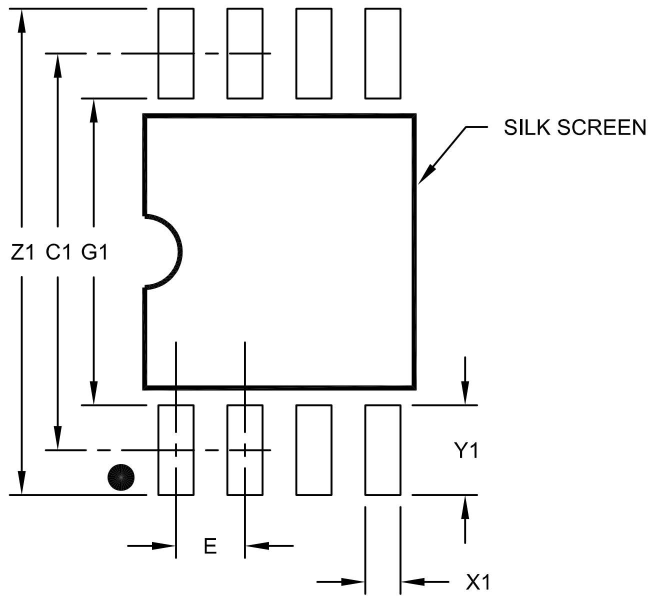
Notes:

1. SOIJ, JEITA/EIAJ Standard, Formerly called SOIC
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.

Microchip Technology Drawing No. C04-056C Sheet 2 of 2

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Overall Width	Z1			9.00
Contact Pad Spacing	C1		7.30	
Contact Pad Width (X8)	X1			0.65
Contact Pad Length (X8)	Y1			1.70
Distance Between Pads	G1	5.60		
Distance Between Pads	G	0.62		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2056C

APPENDIX A: REVISION HISTORY

Revision K (10/2021)

Updated Pin Description section; Updated Figure 1-3; Updated Package Drawings; Added Product Identification System for Automotive; Replaced terminology “Master” and “Slave” with “Host” and “Client”, respectively. Reformatted some sections for better readability.

Revision J (04/2015)

Corrected Features section; Revised Table 1-2, updated ‘Conditions’; Revised Figure 3-12, added parameter TREL; Revised Section 2-12, clarified condition for existing Deep Power-Down mode.

Revision H (05/2010)

Revised Table 1-2, Param. No 25 Conditions; Revised Section 2.2; Added note.

Revision G (01/2010)

Added 8-Lead (MF) DFN-S Land Pattern; Replaced 8-Lead (SM) SOIJ Land Pattern.

Revision F (05/2008)

Modified parameter D006 in Table 1-1; Revised Package Marking Information; Replaced Package Drawings.

Revision E (10/2007)

Removed 25LC1024 part number; New data sheet created for 25LC1024 (DS22064); Revised Tables; Updates throughout.

Revision D (07/2007)

Revised Features; Revised Tables 1-1 and 1-2 (added Industrial temp. and revised parameters 22-23); Replaced Package Drawings (Rev. AP); Revised Product ID System; Changed Flash to EEPROM.

Revision C (02/2007)

Revised Features Section (Self-timed Erase and Write Cycles); Revised Table 1-1 (parameters D012 and D13); Table 1-2 (parameters 20-24); Revised Package Marking Information; Replaced Package Drawings; Revised Product ID System Section (SM package); Changed PICmicro to PIC.

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PRODUCT IDENTIFICATION SYSTEM (NON-AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X][1]	X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	25AA1024		1 Mbit, 1.8V, 256-Byte Page SPI Serial EEPROM
Tape and Reel Option:	Blank	=	Standard packaging (tube or tray)
	T	=	Tape and Reel [1]
Temperature Range:	I	=	-40°C to+85°C (Industrial)
Package:	MF	=	Plastic Dual Flat, No Lead Package – 5x6x0.85 mm Body, 8-lead (DFN-S)
	P	=	Plastic Dual In-Line - 300 mil Body, 8-lead (PDIP)
	SM	=	Plastic Small Outline - Medium, 5.28 mm Body, 8-lead (SOIJ)

Examples:

a) 25AA1024T-I/SM = 1 Mbit, 1.8V Serial EEPROM, Industrial temp., Tape and Reel, SOIJ package

b) 25AA1024T-I/MF = 1 Mbit, 1.8V Serial EEPROM, Industrial temp., Tape and Reel, DFN package

c) 25AA1024-I/P = 1 Mbit, 1.8V Serial EEPROM, Industrial temp., PDIP package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X][1]	–X	/XX	XXX
Device	Tape and Reel Option	Temperature Range	Package	Variant

Device:	25AA1024		1 Mbit, 1.8V, 256-Byte Page SPI Serial EEPROM
Tape and Reel Option:	Blank T	= =	Standard packaging (tube or tray) Tape and Reel [1]
Temperature Range:	I	=	-40°C to+85°C (Automotive Grade 3)
Package:	SM	=	Plastic Small Outline - Medium, 5.28 mm Body, 8-lead (SOIJ)
Variant[2,3]:	16KVAO= 16KVXX=		Standard Automotive, 16K Process Customer-Specific Automotive, 16K Process

Examples:

a) 25AA1024-I/SM16KVAO = 1 Mbit, 1.8V Serial EEPROM, Automotive Grade 3, SOIJ package

b) 25AA1024T-I/SM16KVAO = 1 Mbit, 1.8V Serial EEPROM, Automotive Grade 3, Tape and Reel, SOIJ package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: The VAO/VXX automotive variants have been designed, manufactured, tested and qualified in accordance with AEC-Q100 requirements for automotive applications.

3: For customers requesting a PPAP, a customer-specific part number will be generated and provided. A PPAP is not provided for VAO part numbers.

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