LPC47N237

3.3v I/O Controller for Port Replicators and Docking Stations

Product Features

- 3.3 Volt Operation (5V Tolerant)
- 32 SMBus-Hosted General Purpose Input/Output Pins
  - SMBus Slave Controller Enables Read/Write Access to GPIO Ports
  - SMBus Runs on and GPIO Pins are Driven by Suspend Supply (VTR)
  - SMBus Interrupt Pin
  - SMBus Isolation Circuitry
- PC99a/PC2001 Compliant
- ACPI 1.0/2.0 Compliant
- Power Management Interface
- LPC Interface
  - Multiplexed Command, Address and Data Bus
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - nIO_PME pin for UART Ring Indicate
  - PCI Clock Run Support
- 4 LPC-Hosted General Purpose Input/Output Pins
- Serial Port
  - Full Function Serial Port
  - High Speed 16C550A Compatible UART with 16-Byte Send/Receive FIFOs
  - Programmable Baud Rate Generator supports 230k and 460k Baud
  - Modem Control Circuitry
  - 480 Address and 15 IRQ Options
  - Ring Indicator Wakeup Event
- Multi-Mode™ Parallel Port with ChiProtect™
  - Standard Mode IBM PC/XT®, PC/AT®, and PS/2™ Compatible Bidirectional Parallel Port
  - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
  - ChiProtect Circuitry for Protection
  - 480 Address, Up to 15 IRQ and Three DMA Options
- XNOR-Chain
- 100 pin TQFP RoHS Compliant Package

Description

The LPC47N237 is a 3.3V (5V Tolerant) PC99a/PC2001 compliant Docking I/O controller. The device, which implements the LPC interface, includes I/O functionality. LPC47N237's LPC interface supports LPC I/O and DMA cycles. There is also a SMBus hosted GPIO Block.

The LPC47N237 provides 4 LPC general purpose pins which offer flexibility to the system designer. The legacy I/O included in the LPC47N237 are: a 16C550A compatible UART; one Multi-Mode parallel port including ChiProtect circuitry plus EPP and ECP. The parallel port is compatible with IBM PC/AT architecture, as well as IEEE 1284 EPP and ECP. The LPC47N237 incorporates sophisticated power control circuitry (PCC) which includes support for PME. The PCC supports multiple low power-down modes. The LPC47N237 is ACPI 1.0b/2.0 compatible.

The I/O Address, DMA Channel and hardware IRQ of each logical device in the LPC47N237 may be reprogrammed through the internal configuration registers. There are up to 480 (960 for Parallel Port) I/O address location options, a Serialized IRQ interface, and three DMA channels.

The SMBus hosted GPIO Block includes 32 GPIOs that are powered by standby supply. The GPIOs can be used to assert an interrupt on a change in state of a GPIO. These events are indicated on the nSMBINT pin.

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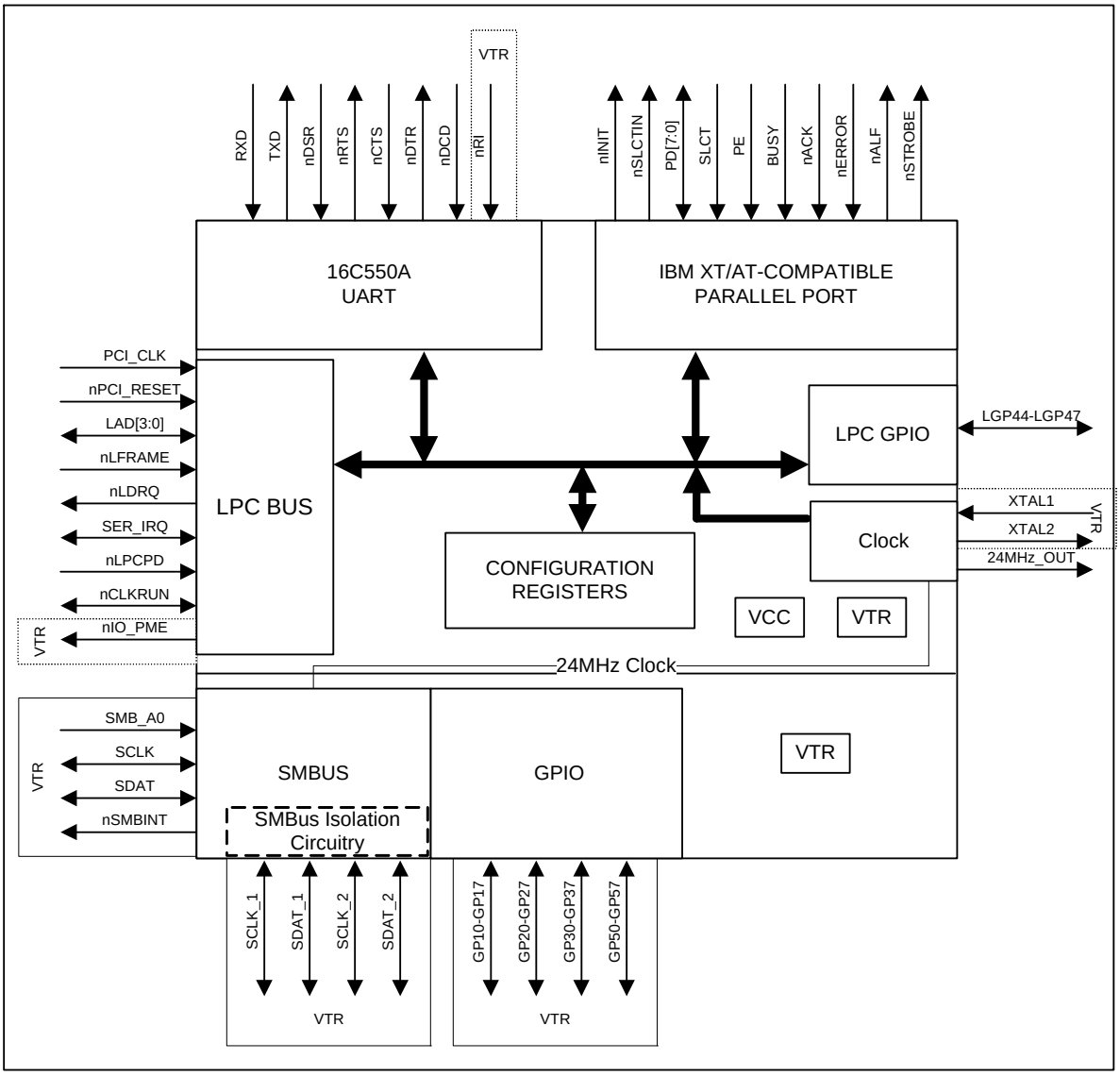
BLOCK DIAGRAM

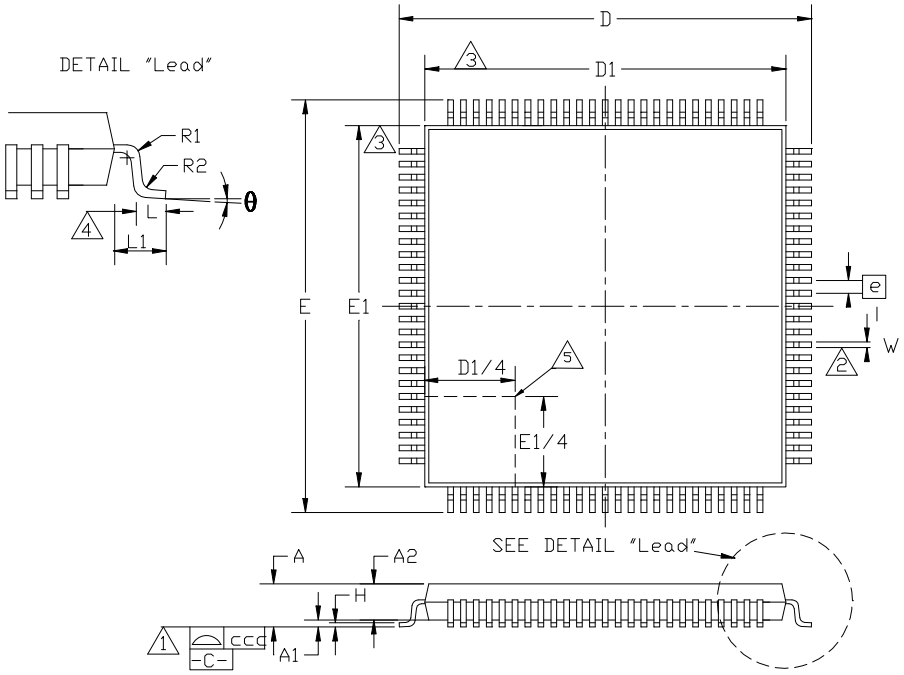
FIGURE 1: LPC47N237 BLOCK DIAGRAM



PACKAGE OUTLINE

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging.

FIGURE 2: LPC47N237 100-PIN TQFP PACKAGE



	Min	Nominal	Max	Remarks
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	~	1.45	Body Thickness
D	15.80	~	16.20	X Span
D1	13.90	~	14.10	X body Size
E	15.80	~	16.20	Y Span
E1	13.90	~	14.10	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e	0.50 Basic			Lead Pitch
θ	0°	~	7°	Lead Foot Angle
W	0.17	0.22	0.27	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

1. Controlling Unit: millimeter.
2. Tolerance on the position of the leads is ± 0.04 mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion.
   Maximum mold protrusion is 0.25 mm.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.

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APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00001811A (08-07-14)	Replaces previous SMSC version Rev. 0.3 (03-30-07)	

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To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.[1]	-	XXX[2]	-	[X][3]
Device		Package		Tape and Reel Option

Device:	LPC47N237 [1]	
Package:	MT	= 100-pin TQFP [2]
Tape and Reel Option:	Blank	= Tray packaging
	TR	= Tape and Reel [3]

Example:

LPC47N237-MT = 100-pin TQFP

Note 1: These products meet the halogen maximum concentration values per IEC61249-2-21.

Note 2: All package options are RoHS compliant. For RoHS compliance and environmental information, please visit http://www.microchip.com/pagehandler/en-us/aboutus/ehs.html .

Note 3: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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