

## **Features**

- Split Gate Trench MOSFET Technology
- · Excellent Package for Heat Dissipation
- High Density Cell Design for Low R<sub>DS(on)</sub>
- Epoxy Meets UL 94 V-0 Flammability Rating
- · Moisture Sensitivity Level 1
- Halogen Free Available Upon Request By Adding Suffix "-HF"
- Lead Free Finish/RoHS Compliant ("P" Suffix Designates RoHS Compliant. See Ordering Information)

## **Maximum Ratings**

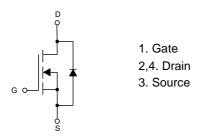
- Operating Junction Temperature Range : -55°C to +150°C
- Storage Temperature Range: -55°C to +150°C
- Thermal Resistance: 28°C/W Junction to Ambient<sup>(1)</sup>
- Thermal Resistance: 0.48°C/W Junction to Case

Parameter	Symbol	Rating	Unit	
Drain-Source Voltage	V <sub>DS</sub>	60	V	
Gate-Source Volltage		V <sub>GS</sub>	±20	V
Continuous Drain	T <sub>C</sub> =25°C	1	200	Α
Current <sup>(2)</sup>	T <sub>C</sub> =100°C	– I <sub>D</sub>	125	Α
Pulsed Drain Current (3)		I <sub>DM</sub>	600	Α
Avalanche Energy (4)		E <sub>AS</sub>	500	mJ
Total Power Dissipation (5)		P <sub>D</sub>	260	W

## Note:

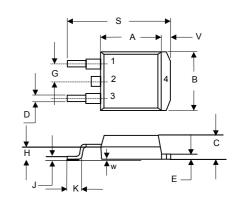
- 1. The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in  $^2$  FR-4 board with 2oz. copper, in a still air environment with  $T_A$ =25°C.
- 2. The maximum current rating is package limited.
- 3. Repetitive rating; pulse width limited by max. junction temperature.
- 4.  $V_{DD}$ =50V,  $R_G$ =25 $\Omega$ , L=0.5mH, starting  $T_J$ =25°C.
- 5. P<sub>D</sub> is based on max. junction temperature, using junction-case thermal resistance.

## **Internal Structure**



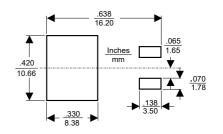
# N-CHANNEL MOSFET

## D2-PAK



DIMENSIONS					
DIM INCHES		MM		NOTE	
DIIVI	MIN	MAX	MIN	MAX	NOTE
Α	0.331	0.370	8.40	9.40	
В	0.378	0.417	9.60	10.60	
С	0.165	0.189	4.20	4.80	
D	0.027	0.037	0.68	0.94	
Е	0.045	0.055	1.14	1.40	
G	0.010		2.54		TYP.
Ι	0.096	0.134	2.43	3.40	
J	0.011	0.025	0.28	0.64	
K	0.071	0.131	1.80	3.32	
S	0.575	0.625	14.60	15.87	
V	0.042	0.058	1.07	1.47	
W	0.000	0.010	0.00	0.25	

## Suggested Solder Pad Layout



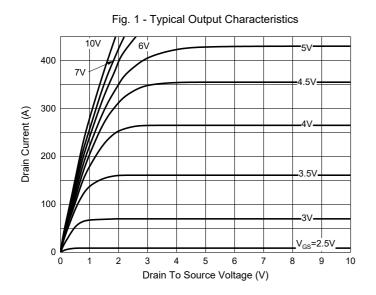


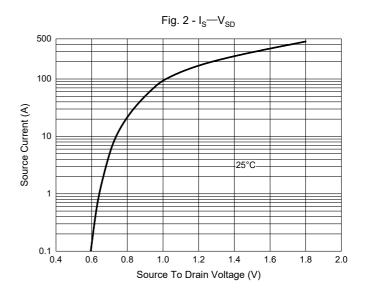
## Electrical Characteristics @ 25°C (Unless Otherwise Specified)

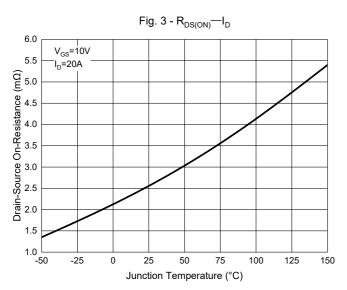
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static Characteristics			<u> </u>		1	I	
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60			V	
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			1	μA	
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.8	2.2	V	
Drain-Source On-Resistance	Б	V <sub>GS</sub> =10V, I <sub>D</sub> =20A		2.35	2.6	mΩ	
	$R_{DS(on)}$	V <sub>GS</sub> =4.5V, I <sub>D</sub> =15A		2.9	3.6	mΩ	
Diode Characteristics							
Continuous Body Diode Current	Is				200	Α	
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =20A			1.2	V	
Reverse Recovery Time	t <sub>rr</sub>	I <sub>S</sub> =25A,di/dt=100A/µs		68		ns	
Reverse Recovery Charge	Q <sub>rr</sub>	18-20A, al/al-100A/µ5		73		nC	
Dynamic Characteristics				•			
Input Capacitance	C <sub>iss</sub>			5950			
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> =25V,V <sub>GS</sub> =0V,f=100KHz		1250		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			85		1	
Total Gate Charge	Qg			93			
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> =50V,V <sub>GS</sub> =10V,I <sub>D</sub> =50A		17		nC	
Gate-Drain Charge	$Q_{gd}$			14			
Turn-On Delay Time	t <sub>d(on)</sub>			22.5			
Turn-On Rise Time	t <sub>r</sub>	V <sub>GS</sub> =10V,V <sub>DD</sub> =30V, I <sub>D</sub> =25A,		6.7		no	
Turn-Off Delay Time	t <sub>d(off)</sub>	R <sub>GEN</sub> =2Ω		80.3		ns	
Turn-Off Fall Time	t <sub>f</sub>			26.9			

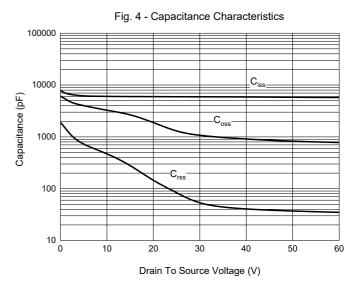


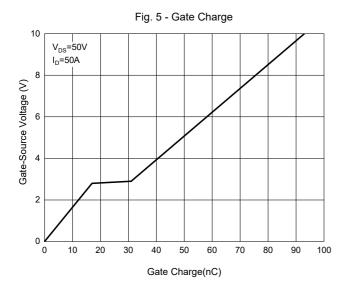
## **Curve Characteristics**

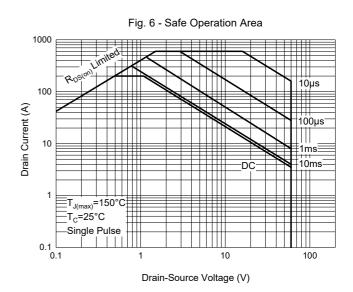














## **Ordering Information**

Device	Packing		
Part Number-TP	Tape&Reel: 800pcs/Reel		
Part Number-BP	Tube: 5Kpcs/Ctn		

Note: Adding "-HF" Suffix For Halogen Free, eg. Part Number-TP-HF

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