MAX11284

Dual 24-Bit, Low-Power, High-SNR, 4ksps Delta-Sigma ADCs with Integrated PGAs

General Description

The MAX11284 is a dual 24-bit delta sigma ADC that achieves excellent SNR while dissipating a low 3.6mW per ADC. Precision DC and AC measurements can be made at sample rates up to 4ksps. Integral nonlinearity is guaranteed to 4ppm maximum and the THD is -120dB. The MAX11284 communicates through an SPI-compatible serial interface and is available in a small, 40-pin TQFN package.

The PGAs can operate in either low-noise (9.1nV/$\sqrt{Hz}$) or low-power (13.6nV/$\sqrt{Hz}$) mode, and have selectable gain values ranging from 1x to 128x. Optional buffers are also included to provide isolation of the signal inputs from the switched capacitor sampling network. This allows the ADCs to be used with high-impedance sources without compromising available dynamic range.

The MAX11284 operates from a single 2.7V to 3.6V analog supply, or split ±1.8V analog supplies, allowing the analog input to be sampled below ground. The digital supply range is 2.0V to 3.6V, allowing communication with 2.5V, 3V, or 3.3V logic.

Applications

- Seismic Data Acquisition
- Scientific Instrumentation
- High-Precision Portable Sensors
- Medical Equipment
- ATE

Benefits and Features

- High Resolution for Instrumentation Applications That Require a Wide Dynamic Range
  - 131dB SNR at 31.25sps in Buffer Mode
  - 114dB SNR at 2000sps in Buffer Mode
- Low Power
  - Digital Current with FIR Filter, 1ksps: 500µA
  - Analog Current PGA Low-Power Mode: 2.1mA
  - Sleep Current: 1.2µA
- High Accuracy for DC Measurements
  - 1ppm INL (typ), 4ppm (max)
- Single/Split Analog Supplies Provide Input Voltage Range Flexibility
  - 2.7V to 3.6V (Single-Supply) or ±1.8V (Split Supplies)
- Digital Filters
  - Programmable SINC + FIR + IIR
  - Linear/Minimum Phase Response
  - Programmable High-Pass Filter
  - Selectable FIR Data Rates: 31.25sps to 4ksps
- Enables System Integration
  - Low-Noise and Low-Power mode PGA with Gains of 1, 2, 4, 8, 16, 32, 64, 128
  - Signal Buffer Optional
  - 2 General-Purpose I/Os
- Integrated Offset and Gain Self-Calibration and System Gain and Offset Calibration Registers
- Small 40-Pin TQFN Package

***Ordering Information* appears at end of data sheet.**

19-8268; Rev 0; 4/16

maxim integrated™

Absolute Maximum Ratings

AVDD_A/B to AVSS_A/B .....-0.3V to +3.9V
DVDD_A/B to DGND_A/B.....-0.3V to +3.9V
DVDD_A/B to AVSS_A/B .....-0.3V to +3.9V
AVSS_A/B to DGND_A/B .....-1.95V to +0.3V
Analog Inputs (AIN__, REF___, CAP___)
to AVSS__ ..... -0.3V to the lower of 3.9V or (V_{AVDD} + 0.3V)
Digital Inputs
(RSTB__, SYNC__, DIN__, SCLK__, CLK, GPIO__)
to DGND__.....-0.3V to the lower of 3.9V or (V_{DVDD} + 0.3V)
Digital Outputs (RDYB__, DOUT__, GPIO__)
to DGND__.....-0.3V to the lower of 3.9V or (V_{DVDD} + 0.3V)
Digital Inputs
(RSTB__, SYNC__, DIN, SCLK, CSB__, GPIO__) to
AVSS__ .....-0.3V to +3.9V
Digital Outputs
(RDYB__, DOUT__, GPIO__) to AVSS__.....-0.3V to +3.9V
CAPREG__ to DGND__.....-0.3V to +2.2V
CAPREG__ to AVSS__ .....-0.3V to +3.9V
Continuous Power Dissipation (T_A = +70°C, multi-layer board)
TQFN (derate 37mW/ºC above +70°C).....2963mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature (continuous).....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Package Thermal Characteristics (Note 1)

TQFN 6 x 6 x 0.75mm
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....37°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{AVDD} = V_{AVDD_A} = V_{AVDD_B} = 2.7V, V_{AVSS} = V_{AVSS_A} = V_{AVSS_B} = 0V, V_{DVDD} = V_{DVDD_A} = V_{DVDD_B} = 2.0V, V_{REFP_A} = V_{REFP} = V_{REFP_B} = 2.5V, V_{REFN} = V_{REFN_A} = V_{REFN_B} = 0V; f_{DATA} = 1000sps, External Clock = 2.048MHz; Continuous conversion mode (SCYCLE = 0); PGA maximum output is 300mV below AVDD and minimum output is 300mV above AVSS, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Integral Nonlinearity (Sample Rate = 250sps)	INL	Bypass, buffer		1	4	ppm
		PGA = 1, 2		1		
		PGA = 4		1	6	
		PGA > 4		2		
Offset Error	V_{OS}	After system offset calibration		10		nV
Offset Drift	$V_{OS\ DRIFT}$			50		nV/°C
Gain Error	G_{ERR}	After system gain calibration		2		ppm
Gain Drift	G_{ERR_DRIFT}			0.05		ppm/°C
DC Common-Mode Rejection (Note 4)	CMR_{DC}	Bypass and Buffer mode		130		dB
		PGA gain = 4		130		

Electrical Characteristics (continued)

(V_{AVDD} = V_{AVDD_A} = V_{AVDD_B} = 2.7V, V_{AVSS} = V_{AVSS_A} = V_{AVSS_B} = 0V, V_{DVDD} = V_{DVDD_A} = V_{DVDD_B} = 2.0V, V_{REFP_A} = V_{REFP} = V_{REFP_B} = 2.5V, V_{REFN} = V_{REFN_A} = V_{REFN_B} = 0V; f_{DATA} = 1000sps, External Clock = 2.048MHz; Continuous conversion mode (SCYCLE = 0); PGA maximum output is 300mV below AVDD and minimum output is 300mV above AVSS, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AVDD, AVSS DC Supply Rejection Ratio	PSRRA	Bypass and buffer mode		105		dB
		PGA gain = 4		105		
DVDD DC Supply Rejection Ratio	PSRRD	Bypass and buffer mode		125		dB
		PGA gain = 4		125		
DYNAMIC PERFORMANCE						
Signal-to-Noise Ratio (Notes 4, 6)	SNR	Bypass, buffer, V_{AVDD} = V_{REF} = 3.6V (see Tables 1 to 6)	113.6	118		dB
		PGA gain = 4, V_{AVDD} = V_{REF} = 3.6V (see Tables 1 to 6)	113.3	117.5		
Signal-to-Noise Ratio (Notes 4, 6)	SNR	Bypass, buffer, V_{REF} = 2.5V (see Tables 1 to 6)	110.5	114.5		dB
		PGA gain = 4, V_{REF} = 2.5V (see Tables 1 to 6)	110	114		
Total Harmonic Distortion (f_{SIGNAL} = 31.25Hz)	THD	Bypass, buffer		-120	-115	dB
		PGA = 1, 2		-119		
		PGA = 4		-119	-112	
		PGA = 8		-119		
		PGA = 16, 32, 64		-114		
		PGA = 128		-110		
Spurious-Free Dynamic Range (f_{SIGNAL} = 31.25Hz)	SFDR	Bypass, buffer		120		dB
		PGA = 4		120		
ANALOG INPUTS/REFERENCE INPUTS						
AIN Voltage Range	V_{RNG}	Unipolar	0		V_{REF}	V
		Bipolar	-V_{REF}		V_{REF}	
Absolute Input Voltage	$VABS_{RNG}$	Bypass mode	V_{AVSS} + 0.05		V_{AVDD} - 0.05	V
		PGA mode	V_{AVSS} + 0.3		V_{AVDD} - 1.3	
		Buffer mode	V_{AVSS} + 0.1		V_{AVDD} -0.1	
AIN DC Input Leakage (Note 4)	IIN_{LEAK}		-10		+10	nA
AIN Common-Mode Input Conductance	G_{AINCM}	Bypass		±2		nA/V

Electrical Characteristics (continued)

(V_{AVDD} = V_{AVDD_A} = V_{AVDD_B} = 2.7V, V_{AVSS} = V_{AVSS_A} = V_{AVSS_B} = 0V, V_{DVDD} = V_{DVDD_A} = V_{DVDD_B} = 2.0V, V_{REFP_A} = V_{REFP} = V_{REFP_B} = 2.5V, V_{REFN} = V_{REFN_A} = V_{REFN_B} = 0V; f_{DATA} = 1000sps, External Clock = 2.048MHz; Continuous conversion mode (SCYCLE = 0); PGA maximum output is 300mV below AVDD and minimum output is 300mV above AVSS, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AIN Common-Mode Input Current		Buffer		±125		nA
		PGA		±5		
AIN Differential Mode Input Conductance	$G_{AINDIFF}$	Bypass		±6		µA/V
AIN Differential Mode Input Current		Buffer		±5		nA
		PGA		±0.1		
REF Differential Input Conductance	$G_{REFDIFF}$	Active conversion state		±46.5		µA/V
REF Input Current at Power Down	I_{REF_PD}	Sleep and standby states		±2.5		µA
AIN Input Capacitance	C_{IN}	Buffer disabled		3		pF
REF Input Capacitance	C_{REF}	Buffer disabled		4.5		pF
Input and REF Sampling Rate	f_S			1.024		MHz
V_{REFP} – V_{REFN} Voltage Range	$VRABS_{RNG}$	(Note 5)			V_{AVDD}	V
REF Voltage Range	V_{REF}		2.0		V_{AVDD}	V
DIGITAL FILTER RESPONSE (Note 3)						
SINC FILTER						
Bandwidth (-3dB)	BW_{SINC}			0.203		f_{DATA}
Settling Time (Latency)				5		$1/f_{DATA}$
FIR FILTER						
Passband Ripple			-0.003		+0.003	dB
Passband (-0.01dB)			0.375		0.375	f_{DATA}
Bandwidth (-3dB)	BW_{FIR}		0.413		0.413	f_{DATA}
High-Pass Filter Corner	f_{HP}	IIR filter; CTRL3 FILT bits = 11	0.000375		0.1	f_{DATA}
Stopband Attenuation			135			dB
Stopband	f_{STOP}			0.5		f_{DATA}
Group Delay		Minimum phase filter		5		$1/f_{DATA}$
		Linear phase filter		31		
Settling Time (Latency)		Minimum phase filter		10		$1/f_{DATA}$
		Linear phase filter		62		

Electrical Characteristics (continued)

(V_{AVDD} = V_{AVDD_A} = V_{AVDD_B} = 2.7V, V_{AVSS} = V_{AVSS_A} = V_{AVSS_B} = 0V, V_{DVDD} = V_{DVDD_A} = V_{DVDD_B} = 2.0V, V_{REFP_A} = V_{REFP} = V_{REFP_B} = 2.5V, V_{REFN} = V_{REFN_A} = V_{REFN_B} = 0V; f_{DATA} = 1000sps, External Clock = 2.048MHz; Continuous conversion mode (SCYCLE = 0); PGA maximum output is 300mV below AVDD and minimum output is 300mV above AVSS, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
Input Current	I_{LEAK_DIG}	Leakage current only	-1		+1	µA
Input Low Voltage	V_{IL}				0.3x V_{DVDD}	V
Input High Voltage	V_{IH}		0.7x V_{DVDD}			V
Input Hysteresis	V_{HYS}			200		mV
GPIO Input Low Voltage	V_{IL_GPIO}				0.4	V
GPIO Input High Voltage	V_{IH_GPIO}		1.0			V
GPIO Input Hysteresis	V_{HYS_GPIO}			20		mV
LOGIC OUTPUTS						
Output Low Level	V_{OL}	I_{OL} = 1mA			0.4	V
Output High Level	V_{OH}	I_{OH} = 1mA	0.9x V_{DVDD}			V
Floating State Leakage Current	I_{DIGO_LEAK}		-10		+10	µA
Floating State Output Capacitance	C_{DIGO}			9		pF
POWER REQUIREMENTS						
Analog Negative Supply	V_{AVSS}	For split supplies, $V_{AVSS\_\_}$ = - $V_{AVDD\_\_}$	-1.8		0	V
Analog Positive Supply	V_{AVDD}	For split supplies, $V_{AVDD\_\_}$ = - $V_{AVSS\_\_}$	V_{AVSS}+ 2.7		V_{AVSS}+ 3.6	V
Digital Supply	V_{DVDD}		2.0		3.6	V
AVDD Sleep Current	I_{AVDD_SLEEP}	Per ADC channel		0.35	3	µA
AVDD Standby Current	I_{AVDD_STBY}	Per ADC channel		0.5	3	µA
DVDD Sleep Current	I_{DVDD_SLEEP}	Per ADC channel		0.25	1	µA
DVDD Standby Current	I_{DVDD_STBY}	Per ADC channel		21	200	µA

Electrical Characteristics (continued)

(V_{AVDD} = V_{AVDD_A} = V_{AVDD_B} = 2.7V, V_{AVSS} = V_{AVSS_A} = V_{AVSS_B} = 0V, V_{DVDD} = V_{DVDD_A} = V_{DVDD_B} = 2.0V, V_{REFP_A} = V_{REFP} = V_{REFP_B} = 2.5V, V_{REFN} = V_{REFN_A} = V_{REFN_B} = 0V; f_{DATA} = 1000sps, External Clock = 2.048MHz; Continuous conversion mode (SCYCLE = 0); PGA maximum output is 300mV below AVDD and minimum output is 300mV above AVSS, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Supply Current	I_{AVDD}	Bypass mode, each ADC		0.55	1.15	mA
		Buffers mode, each ADC		0.65	1.2	
		PGA low-power mode, each ADC		1.05	1.7	
		PGA low-noise mode, each ADC		1.55	2.3	
DVDD Operating Current		SINC filter, each ADC		0.2	0.3	mA
		FIR filter, 1ksps, each ADC		0.25	0.5	
		FIR filter, 4ksps, each ADC		0.86	1.1	
SPI TIMING REQUIREMENTS (SEE FIGURE 14–17)						
SCLK Frequency	f_{SCLK}				5	MHz
SCLK Clock Period	t_{CP}		200			ns
SCLK Pulse-Width High	t_{CH}	Allow 40% duty cycle	80			ns
SCLK Pulse-Width Low	t_{CL}	Allow 40% duty cycle	80			ns
CSB Low Setup	t_{CSS0}	CSB low to 1st SCLK rise setup	40			ns
CSB High Setup	t_{CSS1}	Required to prevent a 17th SCLK RE from being recognized by the device in a free-running application	40			ns
CSB Hold	t_{CSH1}	SCLK falling-edge to CSB rising-edge, CSB hold time	3			ns
CSB Pulse Width	t_{CSW}	Minimum CSB pulse-width high	40			ns
DIN Setup	t_{DS}	DIN setup to SCLK rising-edge	40			ns
DIN Hold	t_{DH}	DIN hold after SCLK rising-edge	0			ns
DOUT Transition	t_{DOT}	DOUT transition valid after SCLK fall			40	ns
DOUT Hold	t_{DOH}	Output hold time remains valid after SCLK fall	3			ns
DOUT Disable	t_{DOD}	CSB rise to DOUT disable, C_{LOAD} = 20pF			25	ns
CSB Fall to DOUT Valid	t_{DOE}	Default value of DOUT is ‘1’ for minimum specification, max specification for valid ‘0’ on RDYB	0		40	ns

Electrical Characteristics (continued)

(V_{AVDD} = V_{AVDD_A} = V_{AVDD_B} = 2.7V, V_{AVSS} = V_{AVSS_A} = V_{AVSS_B} = 0V, V_{DVDD} = V_{DVDD_A} = V_{DVDD_B} = 2.0V, V_{REFP_A} = V_{REFP} = V_{REFP_B} = 2.5V, V_{REFN} = V_{REFN_A} = V_{REFN_B} = 0V; f_{DATA} = 1000sps, External Clock = 2.048MHz; Continuous conversion mode (SCYCLE = 0); PGA maximum output is 300mV below AVDD and minimum output is 300mV above AVSS, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Fall to RDYB '1'	t_{R1}	RDYB transitions from '0' to '1' on falling-edge of SCLK after LSB of DATA is shifted onto DOUT	0		40	ns
RSTB Fall or SYNC Rise to RDYB '1'	t_{R2}	RDYB transitions from '0' to '1' on falling-edge of RSTB or rising-edge of SYNC after 2 f_{CLK} cycles			2	$1/f_{CLK}$
Minimum SYNC High Pulse Width	t_{SYNC1}		2			$1/f_{CLK}$
Minimum RSTB Low Pulse Width	t_{RSTB0}		2			$1/f_{CLK}$

Note 2: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and device characterization.

Note 3: These specifications are not fully tested and are guaranteed by design and/or characterization

Note 4: Tested with input shorted ($V_{AINP\_\_}$ - $V_{AINN\_\_}$ = 0V). SNR = 20 x log10((V_{REF})/($\sqrt{2}$ x V_{NOISE_RMS})). SNR is calculated for either a 3.6V reference or a 2.5V reference, as specified in the Conditions.

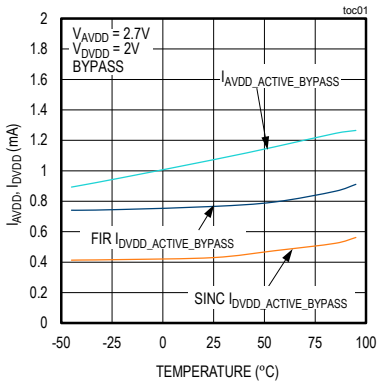
Note 5: Reference common mode (V_{AVSS} + 1V) ≤ (V_{REFP} + V_{REFN})/2 ≤ (V_{AVDD} + V_{ASS})/2 + 0.1V

Note 6: Typical values tested with 150mV supply headroom, V_{AVSS} + 150mV ≤ PGA Output Voltage ≤ V_{AVDD} - 150mV.

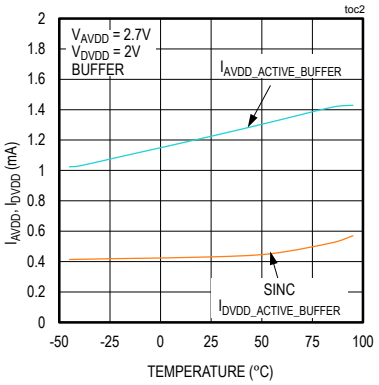
Typical Operating Characteristics

(V_{AVDD} = V_{AVDD_A} = V_{AVDD_B} = 2.7V, V_{AVSS} = V_{AVSS_A} = V_{AVSS_B} = 0V, V_{DVDD} = V_{DVDD_A} = V_{DVDD_B} =2.0V, V_{REFP_A} = V_{REFP} = V_{REFP_B} = 2.5V, V_{REFN} = V_{REFN_A} = V_{REFN_B} = 0V; f_{DATA} = 1000sps, External Clock = 2.048MHz; Continuous conversion mode; (S_{CYCLE} = 0); PGA maximum output is 300mV below AVDD and minimum output is 300mV above AVSS, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

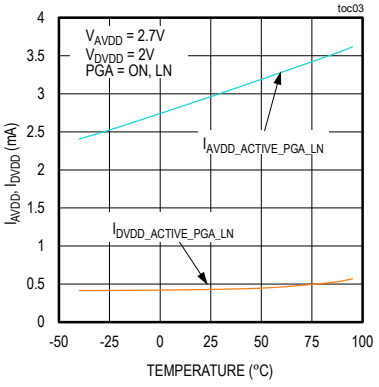
I_{AVDD_ACTIVE} AND I_{DVDD_ACTIVE} vs. TEMPERATURE (BOTH CHANNELS)



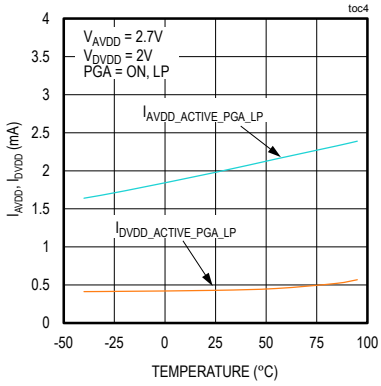
I_{AVDD_ACTIVE} AND I_{DVDD_ACTIVE} vs. TEMPERATURE (BOTH CHANNELS)



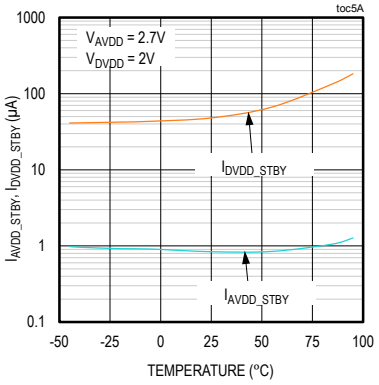
I_{AVDD_ACTIVE} AND I_{DVDD_ACTIVE} vs. TEMPERATURE (BOTH CHANNELS)



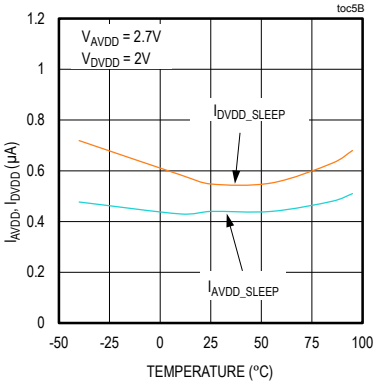
I_{AVDD_ACTIVE} AND I_{DVDD_ACTIVE} vs. TEMPERATURE (BOTH CHANNELS)



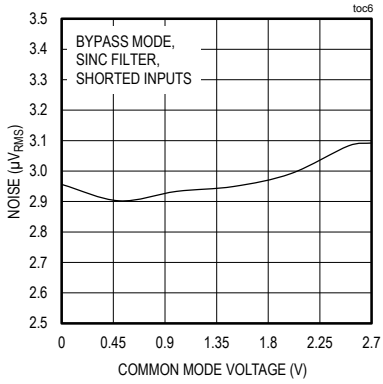
I_{AVDD_STBY} AND I_{DVDD_STBY} vs. TEMPERATURE (BOTH CHANNELS)



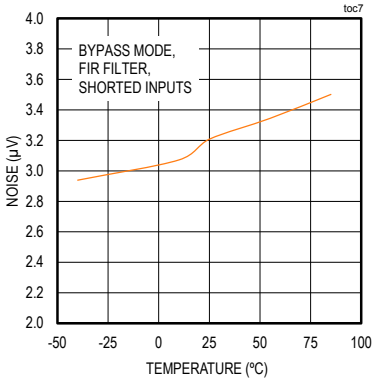
I_{AVDD_SLEEP} AND I_{DVDD_SLEEP} vs. TEMPERATURE (BOTH CHANNELS)



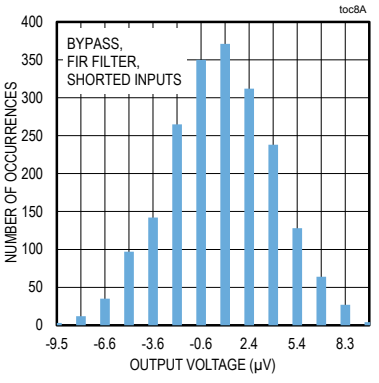
NOISE vs. COMMON MODE VOLTAGE



NOISE vs. TEMPERATURE

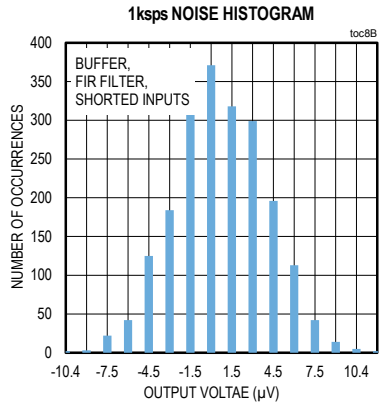


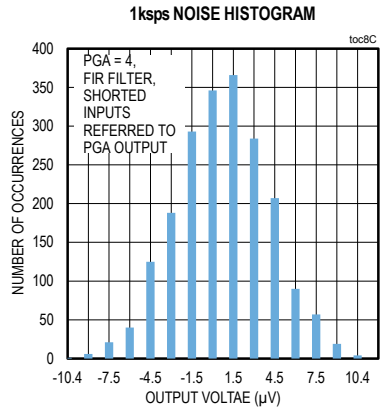
1ksps NOISE HISTOGRAM

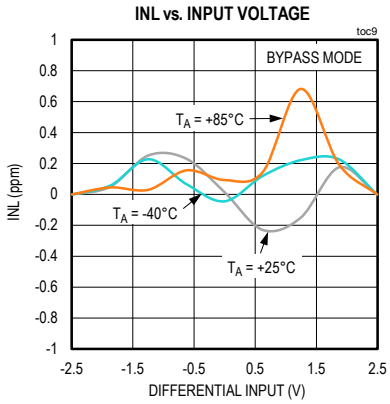


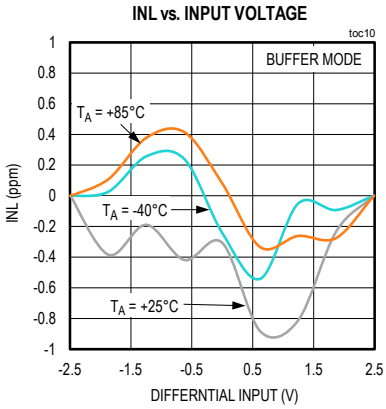
Typical Operating Characteristics (continued)

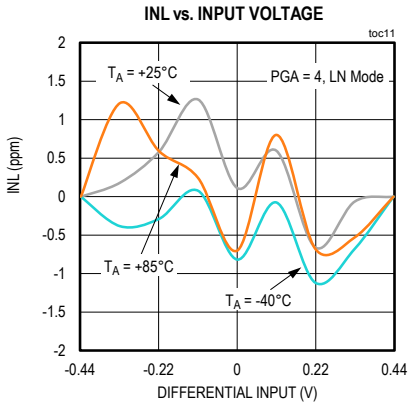
(V_{AVDD} = V_{AVDD_A} = V_{AVDD_B} = 2.7V, V_{AVSS} = V_{AVSS_A} = V_{AVSS_B} = 0V, V_{DVDD} = V_{DVDD_A} = V_{DVDD_B} =2.0V, V_{REFP_A} = V_{REFP} = V_{REFP_B} = 2.5V, V_{REFN} = V_{REFN_A} = V_{REFN_B} = 0V; f_{DATA} = 1000sps, External Clock = 2.048MHz; Continuous conversion mode; (S_{CYCLE} = 0); PGA maximum output is 300mV below AVDD and minimum output is 300mV above AVSS, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

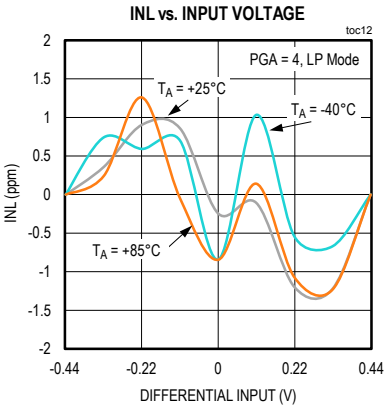


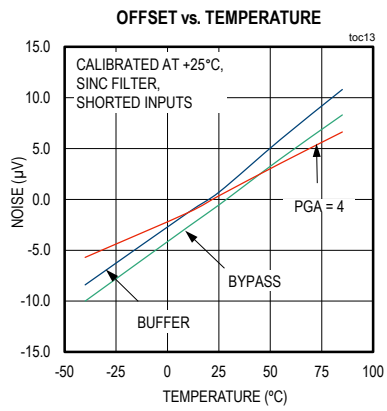


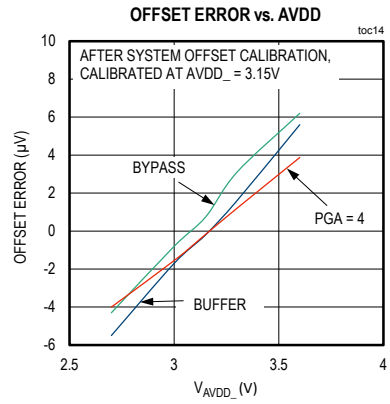


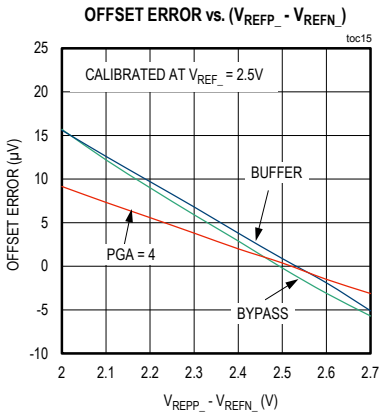








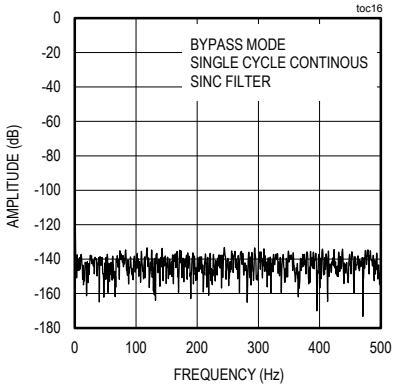




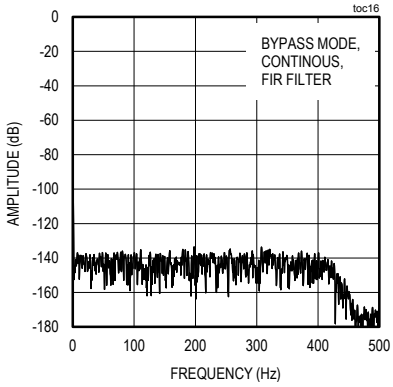
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{AVDD_A} = V_{AVDD_B} = 2.7V, V_{AVSS} = V_{AVSS_A} = V_{AVSS_B} = 0V, V_{DVDD} = V_{DVDD_A} = V_{DVDD_B} =2.0V, V_{REFP_A} = V_{REFP} = V_{REFP_B} = 2.5V, V_{REFN} = V_{REFN_A} = V_{REFN_B} = 0V; f_{DATA} = 1000sps, External Clock = 2.048MHz; Continuous conversion mode; (S_{CYCLE} = 0); PGA maximum output is 300mV below AVDD and minimum output is 300mV above AVSS, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

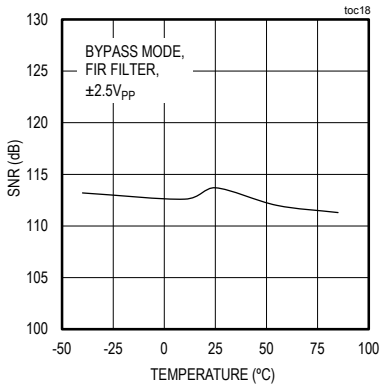
OUTPUT SPECTRUM
SHORTED INPUTS



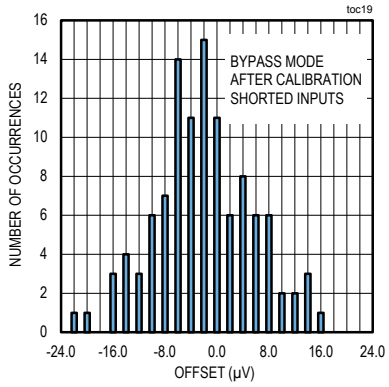
OUTPUT SPECTRUM
SHORTED INPUTS



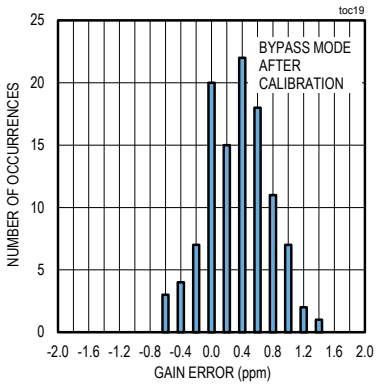
SNR vs. TEMPERATURE



OFFSET HISTOGRAM OF 100 UNITS



POSITIVE FULL SCALE
GAIN ERROR HISTOGRAM > 100 UNITS



NEGATIVE FULL SCALE
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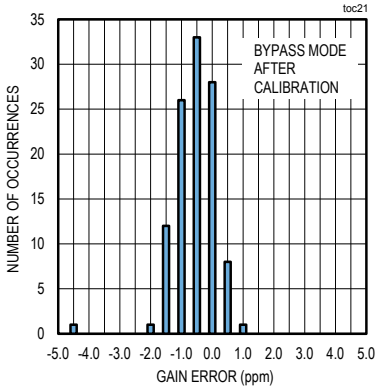
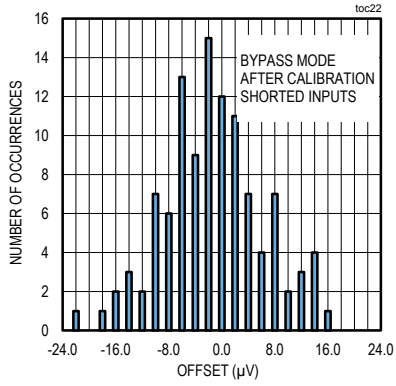
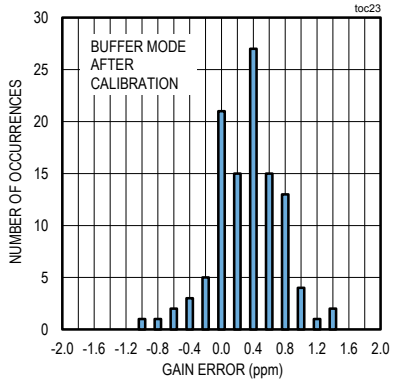


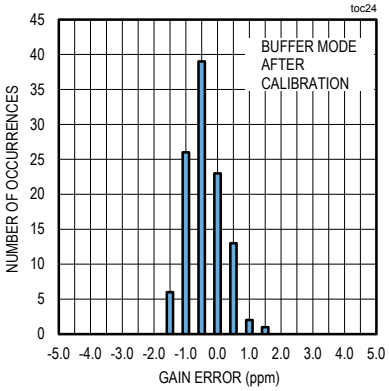
OFFSET HISTOGRAM OF 100 UNITS



POSITIVE FULL SCALE
GAIN ERROR HISTOGRAM > 100 UNITS



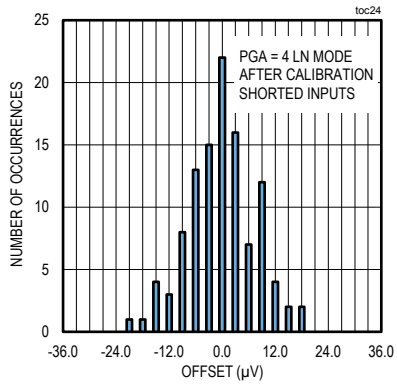
NEGATIVE FULL SCALE
GAIN ERROR HISTOGRAM > 100 UNITS



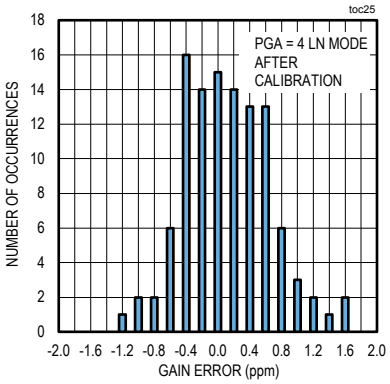
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{AVDD_A} = V_{AVDD_B} = 2.7V, V_{AVSS} = V_{AVSS_A} = V_{AVSS_B} = 0V, V_{DVDD} = V_{DVDD_A} = V_{DVDD_B} =2.0V, V_{REFP_A} = V_{REFP} = V_{REFP_B} = 2.5V, V_{REFN} = V_{REFN_A} = V_{REFN_B} = 0V; f_{DATA} = 1000sps, External Clock = 2.048MHz; Continuous conversion mode; (S_{CYCLE} = 0); PGA maximum output is 300mV below AVDD and minimum output is 300mV above AVSS, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

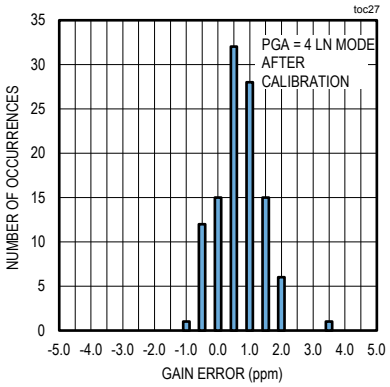
OFFSET HISTOGRAM OF 100 UNITS



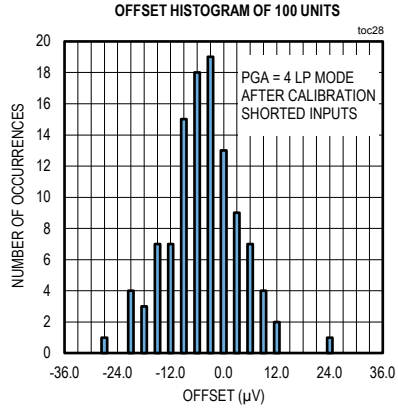
POSITIVE FULL SCALE
GAIN ERROR HISTOGRAM > 100 UNITS



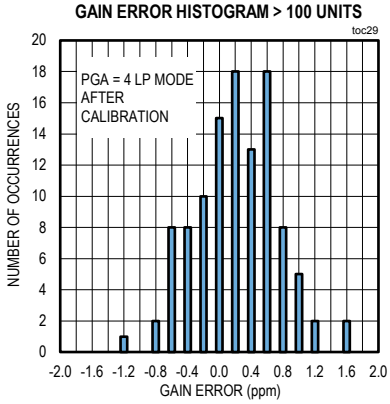
NEGATIVE FULL SCALE
GAIN ERROR HISTOGRAM > 100 UNITS



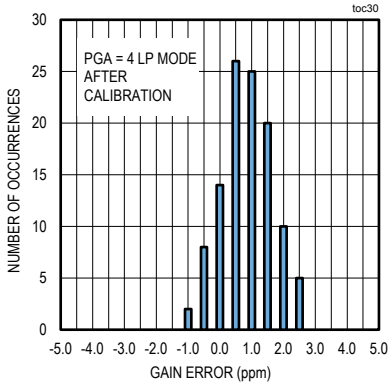
OFFSET HISTOGRAM OF 100 UNITS



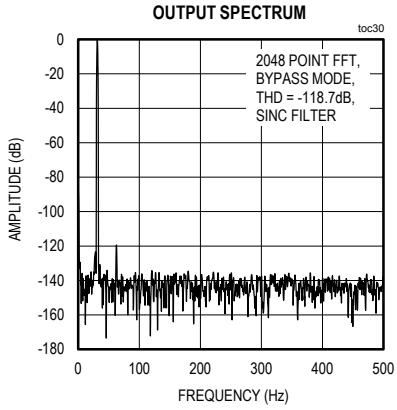
POSITIVE FULL SCALE
GAIN ERROR HISTOGRAM > 100 UNITS



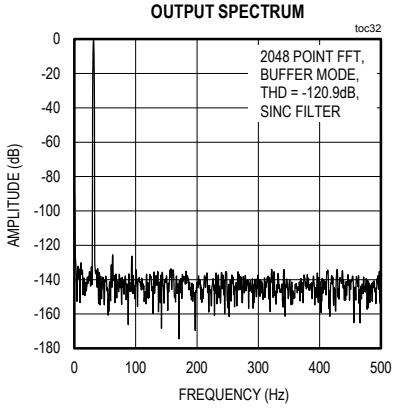
NEGATIVE FULL SCALE
GAIN ERROR HISTOGRAM > 100 UNITS



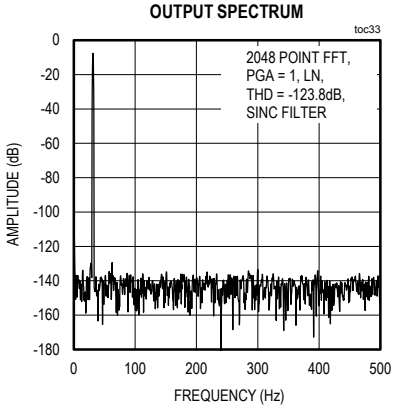
OUTPUT SPECTRUM



OUTPUT SPECTRUM

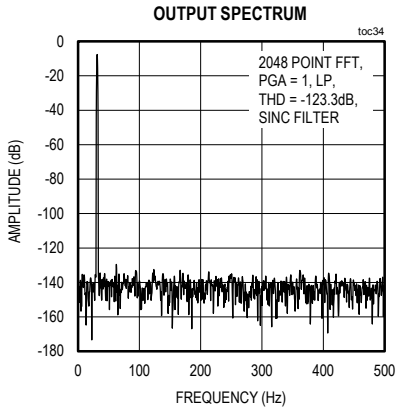


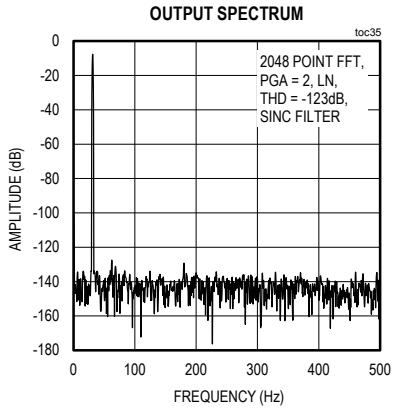
OUTPUT SPECTRUM

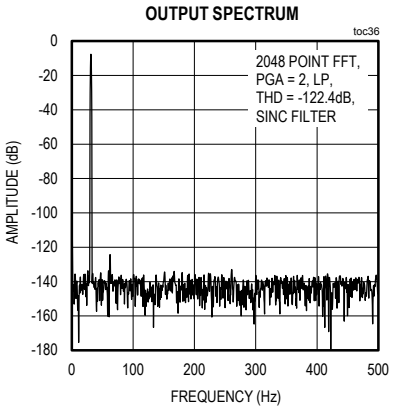


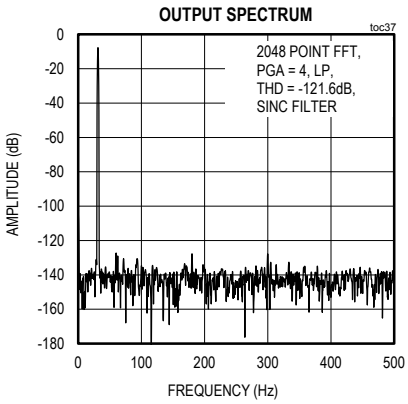
Typical Operating Characteristics (continued)

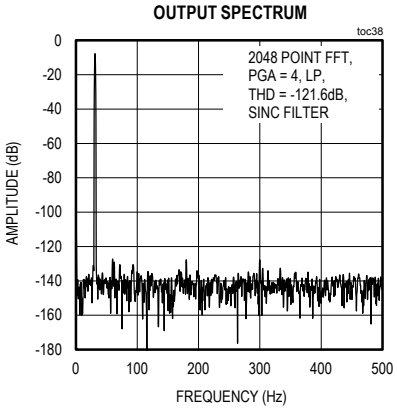
(V_{AVDD} = V_{AVDD_A} = V_{AVDD_B} = 2.7V, V_{AVSS} = V_{AVSS_A} = V_{AVSS_B} = 0V, V_{DVDD} = V_{DVDD_A} = V_{DVDD_B} =2.0V, V_{REFP_A} = V_{REFP} = V_{REFP_B} = 2.5V, V_{REFN} = V_{REFN_A} = V_{REFN_B} = 0V; f_{DATA} = 1000sps, External Clock = 2.048MHz; Continuous conversion mode; (S_{CYCLE} = 0); PGA maximum output is 300mV below AVDD and minimum output is 300mV above AVSS, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

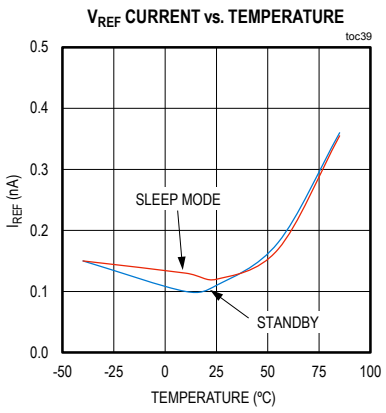


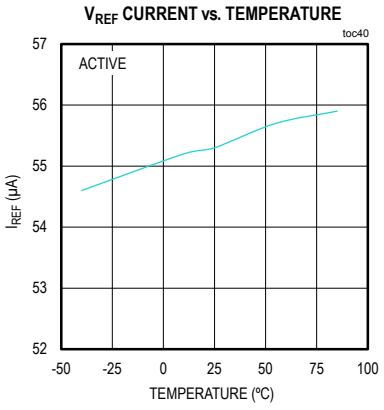




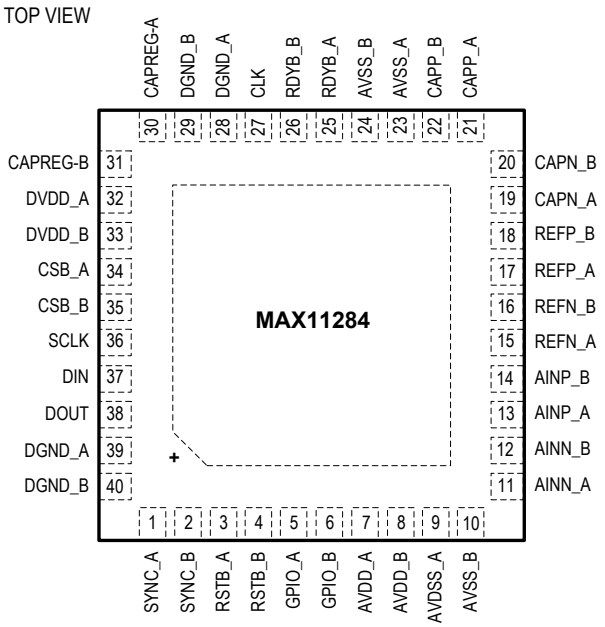








Pin Configuration



TQFN
(6mm x 6mm x 0.5mm)

Pin Description

PIN	NAME	FUNCTION
1	SYNC_A	SYNC Reset A. SYNC_A resets both the digital filter and the modulator of ADC A. Connect SYNC__ from multiple MAX11284 ADCs in parallel to synchronize more than one ADC to an external trigger. This is a digital input pin and is not internally pulled down. For normal operation, drive or pull this pin low.
2	SYNC_B	SYNC Reset B. SYNC_B resets both the digital filter and the modulator of ADC B. Connect SYNC__ from multiple MAX11284 ADCs in parallel to synchronize more than one ADC to an external trigger. This is a digital input pin and is not internally pulled down. For normal operation, drive or pull this pin low.
3	RSTB_A	Reset input for ADC A. RSTB_A causes a complete reset of all digital functions in ADC A, resulting in a power-on reset default state. This is a digital input and is not internally pulled up. For normal operation, drive or pull this pin high.
4	RSTB_B	Reset input for ADC B. RSTB_B causes a complete reset of all digital functions in ADC B, resulting in a power-on reset default state. This is a digital input and is not internally pulled up. For normal operation, drive or pull this pin high.
5	GPIO_A	General-Purpose I/O or Modulator Sync Output for ADC A. GPIO_A is configurable as a digital input or output. GPIO pins have weak pull ups and do not require external bias if unused. For lowest power operation, do not connect or drive high with GPIO configured as input (default).

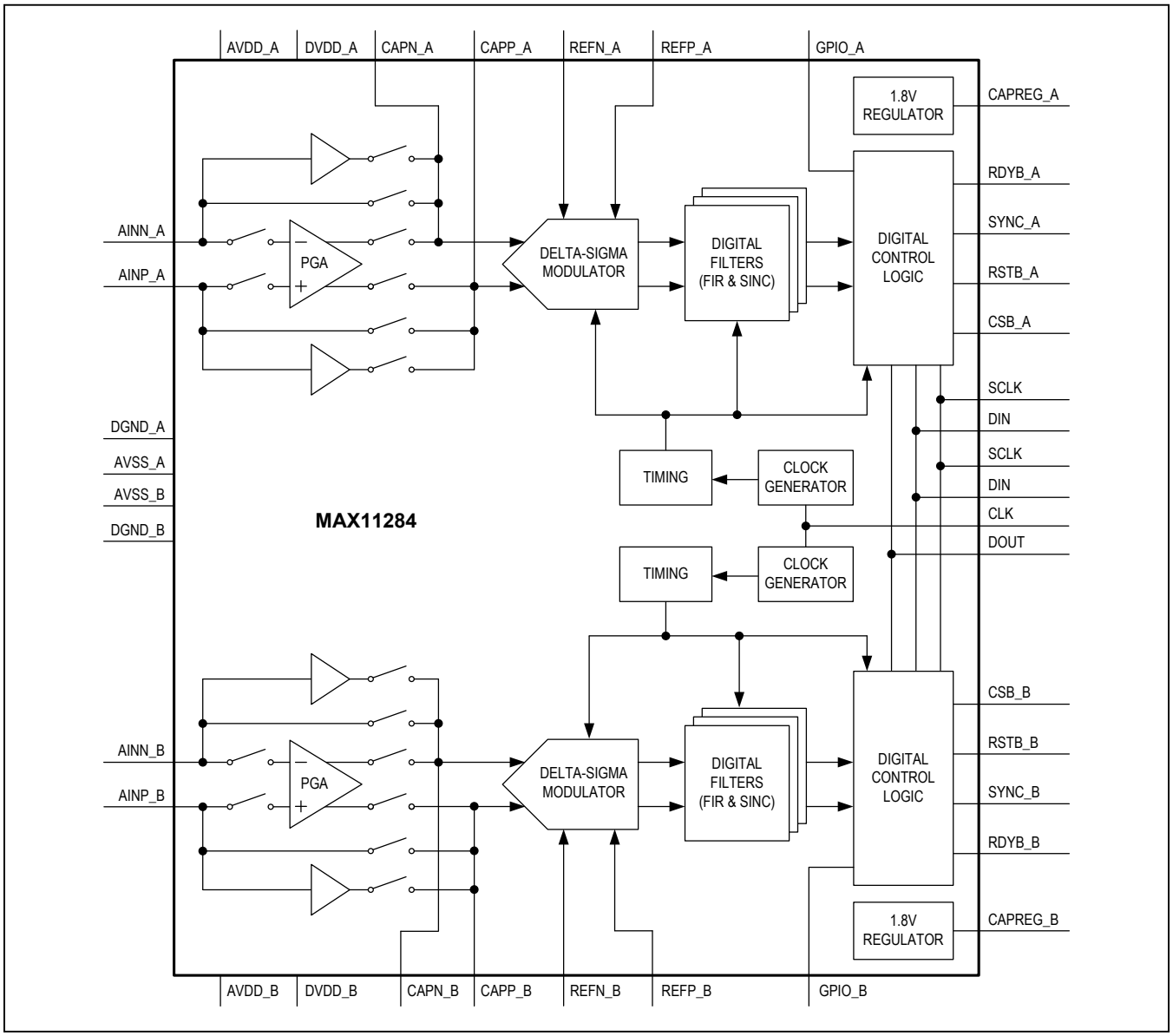
Pin Description (continued)

PIN	NAME	FUNCTION
6	GPIO_B	General-Purpose I/O or Modulator Sync Output for ADC B. GPIO_B is configurable as a digital input or output. GPIO pins have weak pullups and do not require external bias if unused. For lowest power operation, do not connect or drive high with GPIO configured as input (default).
7	AVDD_A	Analog Positive Supply Voltage for ADC A. In single-supply mode, V_{AVDD_A} = 2.7V to 3.6V with V_{AVSS_A} = 0V. In dual-supply mode, AVDD_A and AVSS_A can range from ±1.35V to ±1.8V.
8	AVDD_B	Analog Positive Supply Voltage for ADC B. In single-supply mode, V_{AVDD_B} = 2.7V to 3.6V with V_{AVSS_B} = 0V. In dual-supply mode, AVDD_B and AVSS_B can range from ±1.35V to ±1.8V.
9, 23	AVSS_A	Analog Negative Supply Voltage for ADC A. Connect A_{VSS_A} to the most negative supply. Connect V_{AVSS_A} = 0V in single-supply mode. Connect AVSS_A between -1.8V and 0V for dual-supply mode.
10, 24	AVSS_B	Analog Negative Supply Voltage for ADC B. Connect A_{VSS_B} to the most negative supply. Connect V_{AVSS_B} = 0V in single-supply mode. Connect AVSS_B between -1.8V and 0V for dual-supply mode.
11	AINN_A	Negative Analog Input for ADC A. The analog inputs can measure both unipolar and bipolar ranges, depending on the AVDD_A and AVSS_A voltages.
12	AINN_B	Negative Analog Input for ADC B. The analog inputs can measure both unipolar and bipolar ranges, depending on the AVDD_B and AVSS_B voltages.
13	AINP_A	Positive Analog Input for ADC A. The analog inputs can measure both unipolar and bipolar ranges, depending on the AVDD_A and AVSS_A voltages.
14	AINP_B	Positive Analog Input for ADC B. The analog inputs can measure both unipolar and bipolar ranges, depending on the AVDD_B and AVSS_B voltages.
15	REFN_A	Negative Reference Input for ADC A. REFN_A must be less than REFP_A. REFN_A voltage must be between AVDD_A and AVSS_A.
16	REFN_B	Negative Reference Input for ADC B. REFN_B must be less than REFP_B. REFN_B voltage must be between AVDD_B and AVSS_B.
17	REFP_A	Positive Reference Input for ADC A. REFP_A must be greater than REFN_A. REFP_A voltage must be between AVDD_A and AVSS_A.
18	REFP_B	Positive Reference Input for ADC B. REFP_B must be greater than REFN_B. REFP_B voltage must be between AVDD_B and AVSS_B.
19	CAPN_A	PGA Filter Negative Capacitor Output for ADC_A. Connect a 10nF C0G capacitor between CAPN_A and CAPP_A.
20	CAPN_B	PGA Filter Negative Capacitor Output for ADC_B. Connect a 10nF C0G capacitor between CAPN_B and CAPP_B.
21	CAPP_A	PGA Filter Positive Capacitor Output for ADC_A. Connect a 10nF C0G capacitor between CAPN_A and CAPP_A.
22	CAPP_B	PGA Filter Positive Capacitor Output for ADC_B. Connect a 10nF C0G capacitor between CAPN_B and CAPP_B.
25	RDYB_A	Active-Low Data Ready Output or Internal Clock Output for ADC A. RDYB_A asserts low when the data is ready. When in continuous conversion mode, a SYNC or POR event inhibits output of the first 4 data values to allow for filter settling when the SINC filter is selected. A SYNC or POR event inhibits output of the first 63 data values to allow for filter settling when using the FIR filters.

Pin Description (continued)

PIN	NAME	FUNCTION
26	RDYB_B	Active-Low Data Ready Output or Internal Clock Output for ADC B. RDYB_B asserts low when the data is ready. When in continuous conversion mode, a SYNC or POR event inhibits output of the first 4 data values to allow for filter settling when the SINC filter is selected. A SYNC/POR event inhibits output of the first 63 data values to allow for filter settling when using the FIR filters.
27	CLK	External Clock Input for both ADCs. For external clock mode, set the EXTCLK bit = 1 and provide a digital clock signal at CLK. The MAX11284 is specified with a clock frequency of 2.048MHz. Other clock frequencies may be used, but the data rate and digital filter notch frequencies will scale accordingly. This is a digital input pin and is not internally pulled down. When external clock is disabled, drive this pin low.
28, 39	DGND_A	Digital Ground for ADC_A
29, 40	DGND_B	Digital Ground for ADC_B
30	CAPREG_A	Internal 1.8V Subregulator Reservoir Output for ADC A. Bypass with a 10µF capacitor to DGND. Minimum capacitor value required for stability is 220nF.
31	CAPREG_B	Internal 1.8V Subregulator Reservoir Output for ADC B. Bypass with a 10µF capacitor to DGND. Minimum capacitor value required for stability is 220nF.
32	DVDD_A	Digital Supply Voltage for ADC_A. Supply DVDD with 2.0V to 3.6V, with respect to DGND.
33	DVDD_B	Digital Supply Voltage for ADC_B. Supply DVDD with 2.0V to 3.6V, with respect to DGND.
34	CSB_A	Active-Low Chip-Select Input for ADC_A. Set CSB low to access the serial interface. CSB is used for frame synchronization for communications when SCLK is continuous. Drive CSB high to reset the SPI interface.
35	CSB_B	Active-Low Chip-Select Input for ADC_B. Set CSB low to access the serial interface. CSB is used for frame synchronization for communications when SCLK is continuous. Drive CSB high to reset the SPI interface.
36	SCLK	Serial Clock Input for ADCs A and B. Apply an external serial clock at SCLK to issue commands or access data from the MAX11284.
37	DIN	Serial Data Input. Data is clocked into DIN on the rising edge of SCLK. DIN configures the internal register writes or a command operation.
38	DOUT	Serial Data Output. DOUT outputs 24 bits of filtered data. DOUT transitions on the falling-edge of SCLK.

Functional Diagram



Detailed Description

The MAX11284 is a dual, low-power ADC that resolves a very high dynamic range. Consisting of two identical delta-sigma ADCs, this IC is capable of resolving microvolt-level changes to the analog inputs, making it a good fit for seismic, instrumentation, and ATE applications. Input sources can connect directly to an ADC's delta sigma sampling network, a unity-gain buffer, or to a programmable gain amplifier.

Each ADC includes a high-accuracy internal oscillator that requires no external components. The serial interface outputs data at sample rates up to 4ksps with the FIR filter and 16ksps with the SINC filter. The MAX11284 has three digital filters: SINC, FIR, and IIR. The fifth-order SINC filter is always enabled. The FIR filter can be enabled to get a very flat passband response with extremely sharp cut-off and high stopband rejection. A programmable IIR high-pass filter is also available for rejecting DC and low-frequency signals.

Each ADC is highly configurable through the internal registers, which can be accessed through the SPI interface. This includes PGA gain selection, digital filter selection, offset and gain calibration, and a scalable sample rate to optimize performance.

System Clock

Each ADC incorporates a highly stable internal oscillator that provides the system clock, which is trimmed to 2.048MHz and is divided further down to run the digital and analog timing.

Switch Control

When EN is high, WP1 is connected to MST1, while WP2 is connected to MST2. When EN is low, both switches are open and the device enters a low-current shutdown mode.

Voltage Reference Inputs

Each ADC has a pair of differential inputs (REFP__ and REFN__) for an external reference voltage. Connect the external reference directly across the REFP__ and REFN__ pins to define the differential reference voltage. The $V_{REFP\_\_}$ should always be greater than $V_{REFN\_\_}$ and the common-mode voltage range is between 0.75V and $V_{AVDD\_\_}$ - 0.75V.

Analog Inputs

Each ADC has a pair of differential analog inputs (AINP__ and AINN__) that may be connected in one of three ways: direct connection, buffered connection, and PGA. See the *Control 2 Register (Read/Write)* section for information on programming and enabling the PGA, buffers, or direct connection. The default configuration is direct connect, with both PGA and input buffers powered down.

Input Buffers

The input buffer isolates the inputs from the capacitive load presented by the modulator, allowing for high source-impedance transducers.

Bypass/Direct Connect

The buffers and the PGA may be bypassed and the analog inputs routed directly to the modulator. This option lowers power dissipation since both buffers and PGA are shut off.

Programmable Gain Amplifier (PGA)

The integrated PGAs provide gain settings from 1x to 128x. See the *Control 2 Register (Read/Write)* section for information on controlling the PGAs. Figure 1 shows the PGA structure. The PGA's absolute input voltage range is $VABS_{RNG}$ as specified in the *Electrical Characteristics* table. The PGA output voltage range is from AVSS__+300mV to AVDD__-300mV. The PGA output common-mode voltage is the same as the input common-mode voltage.

Note that linearity and performance degrade when the usable input common-mode voltage of the PGA is exceeded. The usable input and output common-mode ranges are shown in Figure 2. The following equations describe the relationship between the analog inputs and PGA output.

$$V_{CM} = (V_{AINP} + V_{AINN})/2$$

$$V_{CAPP} = V_{CM} + GAIN \times (V_{AINP} - V_{CM})$$

$$V_{CAPN} = V_{CM} - GAIN \times (V_{CM} - V_{AINN})$$

where,

AINP = Positive input to the PGA

AINN = Negative input to the PGA

CAPP__ = Positive output of PGA

CAPN__ = Negative output of PGA

V_{CM} = Input common mode voltage

GAIN = PGA gain

V_{REF} = ADC reference input voltage

$V_{IN} = V_{AINP} - V_{AINN}$

Note: Input voltage range is limited by the reference voltage as described by $V_{IN} \le \pm V_{REF}/GAIN$.

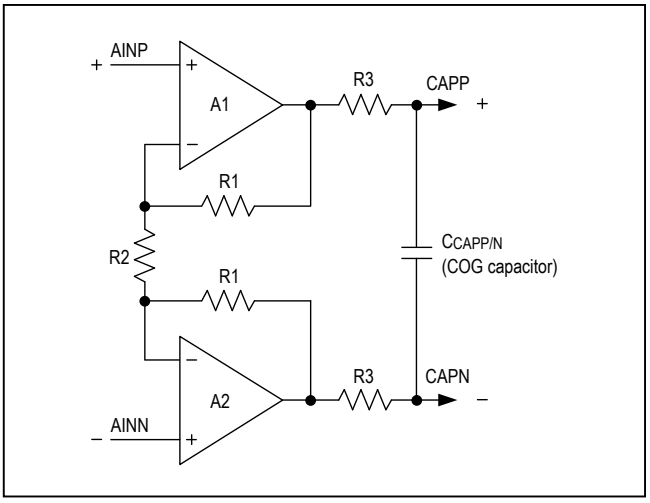


Figure 1. PGA Structure

Input Voltage Range

The ADC input range is programmable for bipolar ($-V_{REF}$ to $+V_{REF}$) or unipolar (0 to V_{REF}) ranges. The U/B bit in the CTRL1 register configures the ADCs for unipolar/bipolar transfer functions. See Figure 2.

Noise Performance vs. Data Rate

The ADCs offer software-selectable output data rates in order to optimize data rate and noise. The RATE bits in the command bytes determine the ADCs' output data rates. The single-cycle conversion mode provides zero latency. Set SCYCLE = 0 in the CTRL1 register to run in continuous conversion mode and SCYCLE = 1 for single-cycle conversion mode.

Single-cycle conversion mode gives an output result with no data latency for up to 3200sps. In continuous conversion mode, the maximum output data rate is 16ksps with the SINC filter and 4ksps with FIR filter.

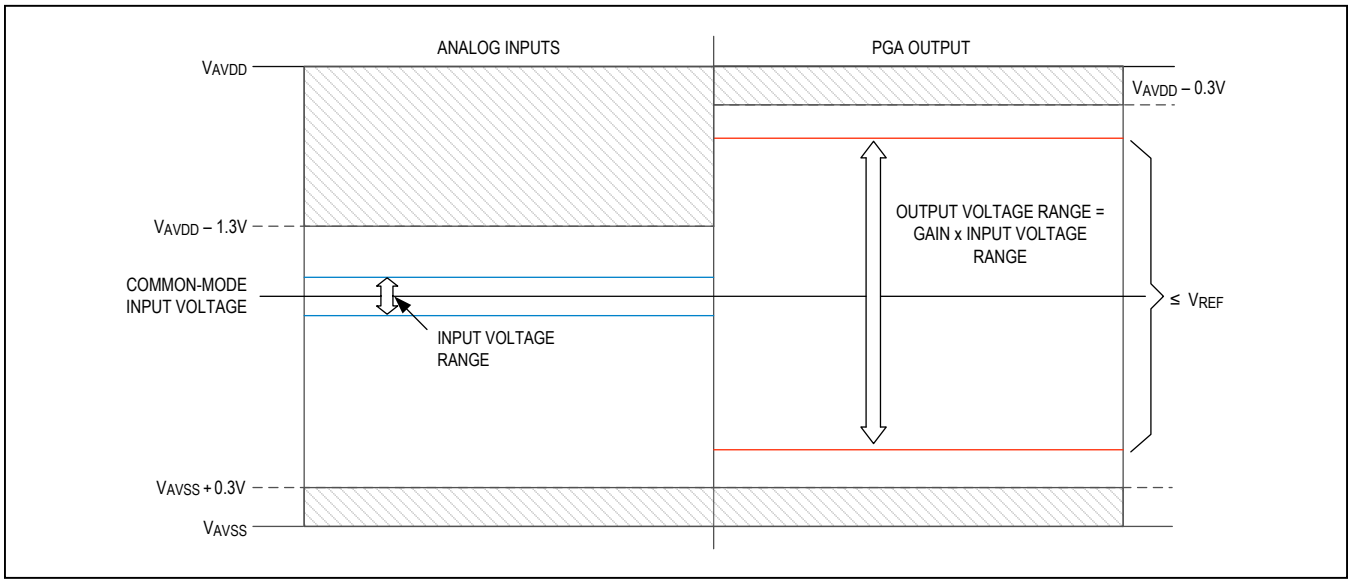


Figure 2. Usable Input and Output Common-Mode Range

Table 1. Continuous Mode SNR (dB) vs. Data Rate and PGA Gain with FIR Filter, AVDD = 2.7V*

DATA RATE (sps)	BYPASS	BUFFER	PGA GAIN SETTING															
			1		2		4		8		16		32		64		128	
			LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP
31.25	128.7	128.3	123.0	123.2	124.6	124.5	126.6	126.8	126.8	126.2	125.6	123.9	122.8	119.9	118.5	114.7	112.8	109.1
62.5	125.9	125.6	120.4	120.4	121.7	121.8	124.0	124.0	124.1	123.6	122.9	120.9	119.9	117.2	115.5	111.9	109.7	105.9
125	123.3	122.9	117.6	117.6	119.0	119.0	121.2	121.0	121.4	120.7	120.2	118.1	117.0	114.3	112.3	108.8	106.9	103.1
250	120.5	120.0	114.6	114.8	116.1	115.9	118.0	117.9	117.9	117.4	116.0	114.8	112.4	110.2	107.1	104.8	101.3	98.7
500	117.5	116.9	111.6	111.7	113.0	112.8	115.3	115.0	115.0	114.4	113.2	111.7	109.5	107.4	104.6	101.8	98.8	96.2
1000	114.4	114.0	108.5	108.6	110.3	110.1	112.4	112.1	112.2	111.6	110.7	108.8	107.2	105.0	102.3	99.5	96.6	93.6
2000	111.4	111.1	105.7	105.8	107.1	107.2	109.1	109.0	109.4	108.6	108.0	106.3	104.7	102.1	99.8	96.9	94.1	90.8
4000	108.3	108.0	102.4	102.7	104.1	104.0	106.4	105.9	106.5	105.5	104.9	103.2	101.8	99.2	96.9	93.8	91.5	88.1

**V_{IN} = 0V. V_{AVDD} = 2.7V, V_{AVSS} = 0V, V_{REF} = 2.5V, T_A = +25°C, external clock. Data taken with PGA output 150mV from AVDD__ and AVSS__. This table is not production tested and is based on characterization data.*

Table 2. Continuous Mode Input Referred Noise (μV_{RMS}) vs. Data Rate and PGA Gain with FIR Filter, AVDD = 2.7V*

DATA RATE (sps)	BYPASS	BUFFER	PGA GAIN SETTING															
			1		2		4		8		16		32		64		128	
			LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP
31.25	0.620	0.628	0.628	0.612	0.311	0.315	0.166	0.162	0.089	0.095	0.053	0.065	0.039	0.054	0.032	0.049	0.030	0.046
62.5	0.865	0.855	0.842	0.848	0.435	0.430	0.224	0.222	0.121	0.128	0.073	0.091	0.054	0.073	0.045	0.067	0.044	0.067
125	1.165	1.165	1.172	1.171	0.592	0.598	0.308	0.316	0.165	0.180	0.100	0.127	0.075	0.102	0.065	0.096	0.060	0.092
250	1.606	1.630	1.637	1.607	0.834	0.846	0.444	0.448	0.249	0.264	0.161	0.186	0.127	0.164	0.117	0.153	0.114	0.153
500	2.259	2.315	2.330	2.310	1.181	1.208	0.609	0.630	0.345	0.369	0.224	0.263	0.177	0.226	0.157	0.216	0.152	0.206
1000	3.229	3.241	3.319	3.267	1.617	1.662	0.844	0.882	0.475	0.513	0.297	0.371	0.232	0.299	0.203	0.282	0.195	0.277
2000	4.565	4.537	4.585	4.525	2.342	2.310	1.234	1.249	0.659	0.719	0.406	0.490	0.308	0.419	0.273	0.379	0.261	0.382
4000	6.522	6.460	6.686	6.449	3.325	3.358	1.697	1.789	0.923	1.033	0.579	0.707	0.431	0.581	0.380	0.539	0.352	0.522

V_{IN} = 0V. V_{AVDD} = 2.7V, V_{AVSS} = 0V, V_{REF} = 2.5V, T_A = +25°C, external clock. This table is not production tested and is based on characterization data.

Table 3. Continuous Mode SNR (dB) vs. Data Rate and PGA Gain with FIR Filter, AVDD = 3.6V*

DATA RATE (sps)	BYPASS	BUFFER	PGA GAIN SETTING															
			1		2		4		8		16		32		64		128	
			LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP
31.25	131.5	130.9	126.9	127.0	127.8	128.3	130.4	130.5	130.0	129.0	128.3	126.7	125.6	122.7	121.1	117.7	115.6	112.0
62.5	129.1	128.6	124.5	124.6	125.4	125.6	128.5	127.8	127.6	126.6	125.9	124.0	122.9	119.8	118.2	114.7	112.7	109.1
125	126.7	126.0	121.9	121.6	122.8	122.8	125.5	125.2	124.7	123.9	123.2	121.1	120.0	117.1	115.3	111.6	109.7	105.9
250	123.7	123.2	119.0	118.9	120.1	120.1	122.3	122.0	121.3	120.7	119.0	117.8	114.9	112.9	110.1	107.5	104.3	101.6
500	120.7	120.4	116.0	116.2	117.1	117.0	119.6	119.2	118.6	117.8	116.4	115.1	112.3	110.2	107.3	104.6	101.7	98.8
1000	117.9	117.3	113.3	113.1	114.2	114.1	116.6	116.1	115.7	115.0	113.8	112.1	110.2	107.8	105.1	102.2	99.7	96.2
2000	114.9	114.4	110.2	110.1	110.9	110.8	113.7	113.4	112.5	112.3	110.8	109.3	107.6	104.7	102.7	99.6	97.0	93.5
4000	111.9	111.4	106.8	107.2	108.2	108.0	110.5	110.3	109.7	108.9	108.2	106.5	104.7	101.9	99.8	96.7	94.2	90.9

V_{IN} = 0V. V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{REF} = 3.6V, T_A = +25°C, external clock. Data taken with PGA output 150mV from AVDD__ and AVSS__. This table is not production tested and is based on characterization data.

Table 4. Continuous Mode Input Referred Noise (μV_{RMS}) vs. Data Rate and PGA Gain with FIR Filter, AVDD = 3.6V*

DATA RATE (sps)	BYPASS	BUFFER	PGA GAIN SETTING															
			1		2		4		8		16		32		64		128	
			LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP
31.25	0.675	0.683	0.674	0.665	0.345	0.326	0.177	0.174	0.092	0.103	0.056	0.067	0.038	0.054	0.032	0.047	0.030	0.046
62.5	0.890	0.895	0.888	0.872	0.457	0.444	0.219	0.237	0.122	0.136	0.074	0.092	0.052	0.074	0.045	0.067	0.042	0.064
125	1.177	1.206	1.189	1.229	0.616	0.614	0.310	0.321	0.169	0.186	0.100	0.129	0.073	0.102	0.062	0.096	0.060	0.093
250	1.664	1.667	1.673	1.688	0.837	0.843	0.446	0.462	0.250	0.269	0.164	0.189	0.131	0.166	0.113	0.153	0.111	0.152
500	2.343	2.300	2.353	2.290	1.190	1.200	0.613	0.639	0.344	0.377	0.220	0.258	0.176	0.225	0.158	0.214	0.150	0.210
1000	3.247	3.271	3.222	3.269	1.656	1.678	0.863	0.910	0.479	0.516	0.298	0.364	0.226	0.299	0.202	0.283	0.189	0.283
2000	4.555	4.600	4.592	4.648	2.409	2.442	1.204	1.248	0.688	0.705	0.423	0.501	0.305	0.423	0.268	0.381	0.257	0.386
4000	6.476	6.468	6.788	6.458	3.286	3.379	1.747	1.790	0.960	1.041	0.569	0.692	0.424	0.588	0.371	0.535	0.356	0.520

V_{IN} = 0V. V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{REF} = 3.6V, T_A = +25°C, external clock. This table is not production tested and is based on characterization data.

Table 5. Continuous Mode SNR (dB) vs. Data Rate and PGA Gain with Sinc Filter*

DATA RATE (sps)	BYPASS	BUFFER	PGA GAIN SETTING															
			1		2		4		8		16		32		64		128	
			LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP
0.4875	139.1	139.0	133.7	135.4	136.5	135.8	138.9	138.3	139.2	136.8	137.6	136.2	136.2	134.0	130.1	130.1	127.0	123.5
0.975	139.5	138.7	135.1	135.2	135.7	135.7	138.9	138.4	138.4	136.8	136.4	135.5	135.2	133.7	131.6	129.4	126.7	123.6
1.95	137.8	138.4	135.0	134.2	135.6	135.2	137.9	136.8	136.7	136.1	135.8	135.5	134.0	132.5	130.0	127.7	124.2	121.4
3.9	137.4	137.0	133.0	132.7	134.0	133.4	136.1	135.8	135.8	134.8	134.0	133.5	132.1	130.2	128.2	125.0	122.9	119.2
7.8	135.5	134.8	131.1	131.1	132.0	131.5	134.3	133.9	133.7	133.4	132.1	131.5	129.6	127.8	125.9	122.5	120.4	116.9
15.625	133.5	132.6	129.0	128.9	130.0	130.1	132.4	132.1	132.1	131.4	130.1	128.8	127.5	125.0	122.9	119.7	117.6	114.0
31.25	131.3	130.4	126.9	126.3	127.6	127.5	130.2	129.8	129.6	128.8	127.8	126.2	124.8	122.2	120.5	116.8	114.9	111.0
62.5	128.7	128.0	124.1	124.0	125.1	125.0	127.4	127.1	126.7	126.0	125.0	123.5	122.3	119.1	117.5	113.9	111.7	107.9
125	126.1	125.3	121.4	121.1	122.2	122.2	124.5	124.5	123.7	123.1	121.7	120.0	117.8	115.3	112.5	110.1	106.9	104.2
250	123.3	122.6	118.6	118.5	119.3	119.4	121.8	121.6	120.7	120.0	118.5	117.2	114.8	112.5	112.4	107.2	104.1	101.0
500	120.2	119.9	115.7	115.6	116.7	116.6	118.8	118.9	118.1	117.4	116.2	114.4	112.1	110.0	109.8	104.3	101.5	98.7
1,000	117.7	117.2	113.1	112.9	113.9	113.8	116.5	116.5	115.7	115.1	113.6	112.3	110.2	107.6	107.6	102.1	99.3	96.3
2,000	115.7	115.2	111.0	110.7	111.9	111.9	114.3	114.5	113.7	113.1	111.8	110.1	108.1	105.7	106.0	100.2	97.7	94.5
4,000	114.6	114.1	110.0	109.9	111.0	110.9	113.7	113.6	112.5	112.0	111.2	109.3	106.8	105.0	104.7	99.0	97.1	93.6
8,000	111.6	111.2	106.9	107.0	107.7	107.8	110.4	110.2	109.5	108.8	107.7	106.3	104.4	101.9	102.0	96.3	94.3	90.6
16,000	108.1	107.4	103.4	103.1	104.3	104.3	107.0	106.9	106.2	105.4	104.4	102.9	101.9	98.8	99.1	93.6	91.5	87.7

V_{IN} = 0V. V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{REF} = 3.6V, T_A = +25°C, external clock. This table is not production tested and is based on characterization data.

Table 6. Continuous Mode Input-Referred Noise (μV_{RMS}) vs. Data Rate and PGA Gain with Sinc Filter*

DATA RATE (sps)	BYPASS	BUFFER	PGA GAIN SETTING															
			1		2		4		8		16		32		64		128	
			LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP
0.4875	0.283	0.270	0.307	0.251	0.127	0.137	0.066	0.071	0.032	0.042	0.019	0.023	0.011	0.015	0.011	0.011	0.008	0.012
0.975	0.271	0.280	0.261	0.259	0.139	0.139	0.066	0.070	0.035	0.042	0.022	0.025	0.013	0.015	0.010	0.012	0.008	0.012
1.95	0.328	0.288	0.265	0.290	0.140	0.148	0.074	0.084	0.043	0.046	0.024	0.024	0.015	0.017	0.011	0.015	0.011	0.016
3.9	0.342	0.339	0.332	0.346	0.168	0.182	0.092	0.094	0.047	0.053	0.029	0.031	0.018	0.023	0.014	0.020	0.013	0.020
7.8	0.429	0.435	0.416	0.415	0.213	0.227	0.112	0.117	0.060	0.062	0.036	0.039	0.024	0.030	0.018	0.027	0.018	0.026
15.625	0.539	0.563	0.528	0.532	0.268	0.264	0.140	0.145	0.072	0.079	0.046	0.053	0.031	0.041	0.026	0.038	0.024	0.036
31.25	0.696	0.724	0.669	0.723	0.354	0.359	0.179	0.189	0.097	0.106	0.059	0.072	0.042	0.057	0.034	0.053	0.033	0.051
62.5	0.930	0.961	0.928	0.940	0.472	0.479	0.248	0.258	0.135	0.146	0.082	0.097	0.056	0.081	0.049	0.074	0.047	0.074
125	1.266	1.299	1.258	1.301	0.657	0.660	0.349	0.349	0.191	0.204	0.120	0.145	0.094	0.125	0.086	0.115	0.083	0.112
250	1.751	1.777	1.754	1.767	0.917	0.911	0.476	0.483	0.268	0.292	0.172	0.201	0.132	0.172	0.088	0.159	0.114	0.163
500	2.475	2.430	2.440	2.460	1.236	1.260	0.672	0.663	0.363	0.392	0.227	0.276	0.181	0.229	0.118	0.222	0.154	0.213
1,000	3.323	3.320	3.304	3.348	1.712	1.727	0.872	0.877	0.481	0.511	0.306	0.355	0.227	0.305	0.151	0.286	0.197	0.279
2,000	4.160	4.189	4.193	4.307	2.160	2.161	1.121	1.105	0.603	0.645	0.373	0.454	0.285	0.378	0.183	0.356	0.236	0.345
4,000	4.716	4.716	4.694	4.769	2.381	2.431	1.210	1.214	0.688	0.729	0.404	0.499	0.333	0.409	0.211	0.408	0.253	0.381
8,000	6.700	6.612	6.688	6.650	3.513	3.451	1.754	1.811	0.974	1.056	0.604	0.709	0.441	0.586	0.288	0.560	0.352	0.541
16,000	10.010	10.256	10.038	10.395	5.154	5.157	2.603	2.635	1.428	1.566	0.880	1.048	0.585	0.842	0.406	0.761	0.482	0.751

V_{IN} = 0V. V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{REF} = 3.6V, T_A = +25°C, external clock. This table is not production tested and is based on characterization data.

Power-On Reset

The ADCs contain power-on reset (POR) supply-monitoring circuitry on both the digital supply (DVDD) and the positive analog supply (AVDD). The POR circuitry ensures proper device default conditions after either a digital or analog power-sequencing event.

The digital POR trigger threshold is typically 1.2V with respect to V_{DGND} and has 100mV of hysteresis. The analog POR trigger threshold is typically 1.25V with respect to V_{AVSS} and has 100mV of hysteresis. Both POR circuits have low-pass filters that prevent high-frequency supply glitches from triggering the POR.

Power-Down Modes

The ADCs can be powered down through the IMPD bit in the command byte (see Table 10). The PD[1:0] bits of the CTRL1 register are used to select the power-down state. The SPI interface remains fully functional in all power-down states.

Sleep Mode: Sleep mode can be set by writing 01 to the PD[1:0] bits. In this state, the internal subregulator that powers the digital core is powered off. This is the lowest power state for the device.

Standby Mode: Standby mode is set by writing 10 to the PD[1:0] bits. In this mode the device is not active, but the internal subregulator is still powered on. This allows conversions to start immediately after receiving a start conversion command (see Table 10).

Table 7. MAX11284 Command Behavior from Pin (RSTB__, SYNC__) and SPI (RESET, SYNC_SPI)

COMMAND ISSUED	COMMAND-ISSUED VIA	STATE BEFORE COMMAND	STATE AFTER COMMAND	TRANSITION TIME (MAX)	COMMAND INTERPRETATION AND RESULTING CHIP STATE
RESET SPI or PIN	SPI,PIN	STBY	STBY	—	Chip POR
		SLEEP	STBY	5ms	Chip POR
		Calibration	STBY	—	Calibration stops, chip POR
		Conversion	STBY	—	Conversion stops, chip POR
IMPD CTRL1:PD = ’01’ SLEEP Mode	SPI	STBY	SLEEP	—	Chip changes from STBY to SLEEP
		SLEEP	SLEEP	—	Chip remains in SLEEP
		Calibration	SLEEP	—	Calibrations stop
		Conversion	SLEEP	—	Conversion stop
IMPD CTRL1:PD = ’10’ STBY Mode	SPI	STBY	STBY	—	Chip remains in standby
		SLEEP	STBY	—	Chip changes from SLEEP to standby
		Calibration	STBY	—	Calibrations stop, chip changes to standby
		Conversion	STBY	—	Conversions stop, chip changes to standby
SYNC	SPI, PIN	STBY	STBY	—	SYNC ignored, chip remains in STBY mode
		Calibration	Calibration	—	SYNC ignored
		Conversion	Conversion	—	Pulse SYNC mode, conversions restart
		Conversion	Conversion	—	Continuous SYNC mode, 1st SYNC rising edge sets clock counter, subsequent rising edges are compared against clock counter. If count is off by more than ±1 clock counts, restart conversions; otherwise, do nothing and continue conversions in progress. If a SYNC rising edge occurs before the first RDYB__ asserts after conversions are started, SYNC__ is ignored. Once the first RDYB__ asserts, all subsequent SYNC__ rising edges are evaluated.
CMD Register Write	SPI	STBY	STBY	—	Chip remains in standby
		SLEEP	SLEEP	—	Chip remains in SLEEP
		Calibration	STBY	—	Calibration stops, chip goes to STBY mode
		Conversion	STBY	—	Conversion stops, chip goes to STBY mode
Convert Command Write	SPI	STBY	Conversion	—	Exit standby, conversion starts
		SLEEP (SPI)	Conversion	—	Exit SLEEP mode, conversion starts
		Calibration	Conversion	—	Calibration stops then a new conversion starts
		Conversion	Conversion	—	Conversion stops and a new conversion starts

Digital Filter

The digital filter is a mode-configurable digital filter and decimator that processes a one-bit data stream from the fourth order delta-sigma modulator and implements a fifth order SINC function with an averaging function to produce a 24-bit wide data stream. The internal state machine runs synchronous with the system clock of 2.048MHz.

SINC Filter

The SINC filter allows the ADCs to achieve very high SNR. One feature of the fifth-order SINC filter is a bandwidth that is about twenty percent of the data rate. The following example shows a -3dB BW of about 830Hz for 4ksps data rate.

FIR Filter

Selecting the built-in FIR filter expands the -3dB bandwidth of the ADCs to 0.413 times the data rate, thus achieving a very low ripple passband with extremely sharp rolloff and high stopband rejection. This is done by selecting the FILT bits in the CTRL 3 register to enable the FIR filter. There are two different forms of FIR filter available, selectable between linear phase response or minimum phase response by setting the PHASE bit in the CTRL 3 register.

The magnitude response for the FIR filter with linear phase and minimum phase at 4ksps data rate is shown below. The passband ripple is comparable in linear phase and minimum phase responses and is less than 5mdB.

The linear response FIR filter should be selected if the application requires a linear phase relationship; otherwise for faster settling use the minimum phase FIR filter. This is shown in the following phase response and step response plots. Note all plots are taken for a 4ksps data rate.

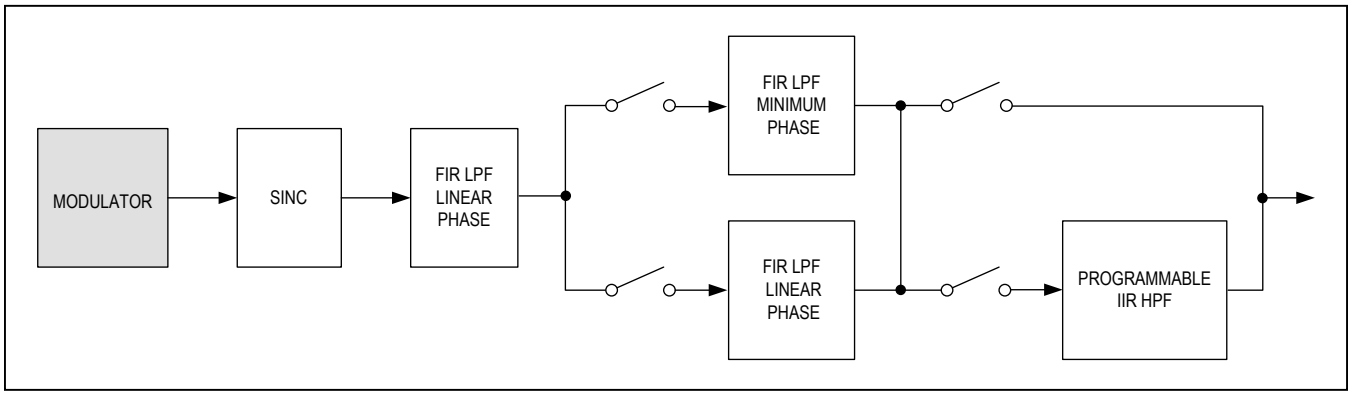


Figure 3. Digital Filter Path

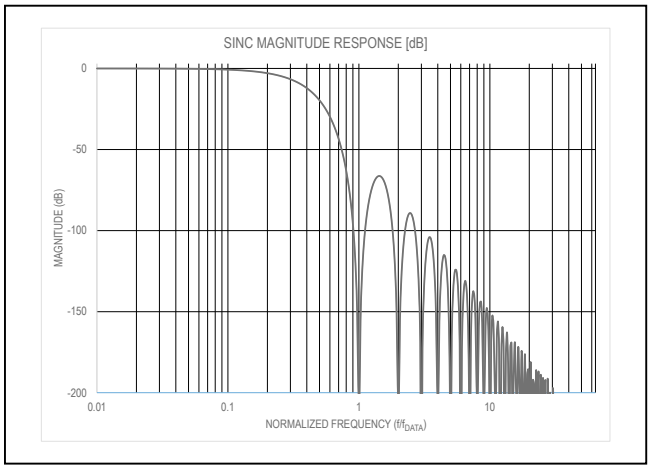


Figure 4a. SINC Magnitude Response

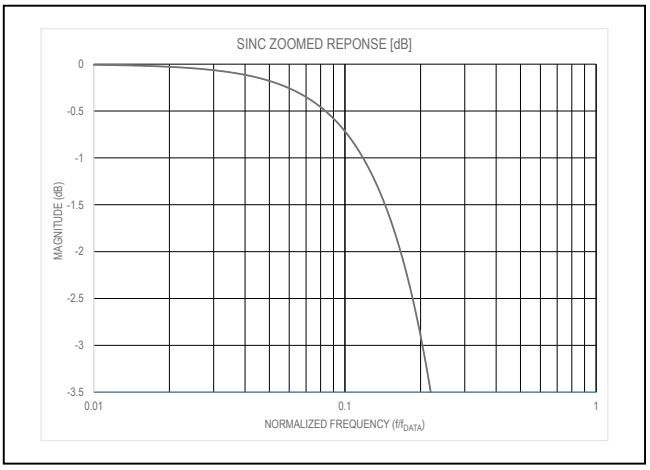


Figure 4b. SINC Magnitude Response Zoomed In

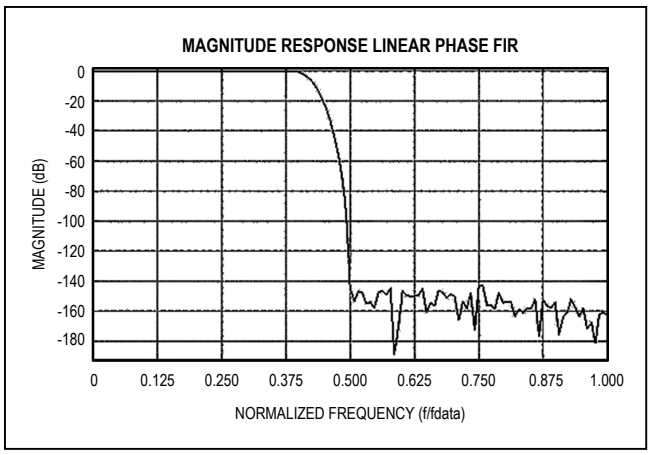


Figure 5. Magnitude Response, Linear Phase FIR, 4ksps Data Rate

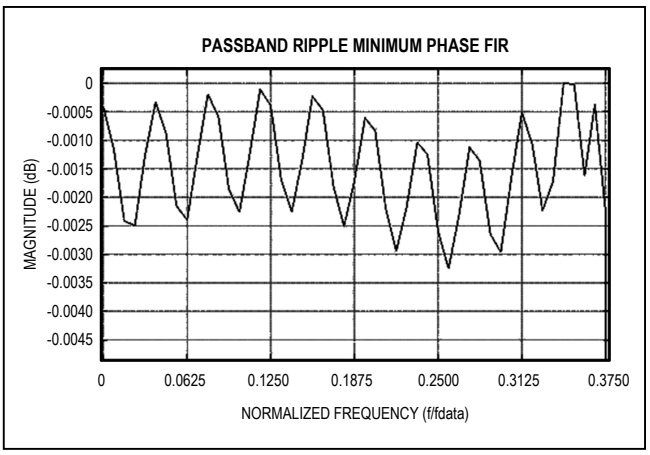


Figure 8. Passband Ripple, Minimum Phase FIR, 4ksps Data Rate

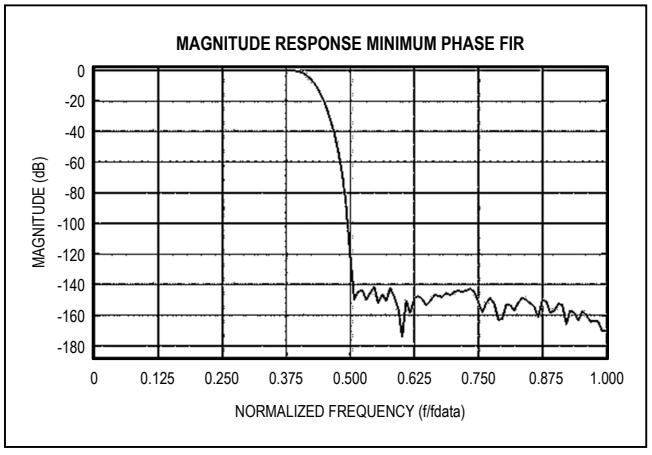


Figure 6. Magnitude Response, Minimum Phase FIR, 4ksps Data Rate

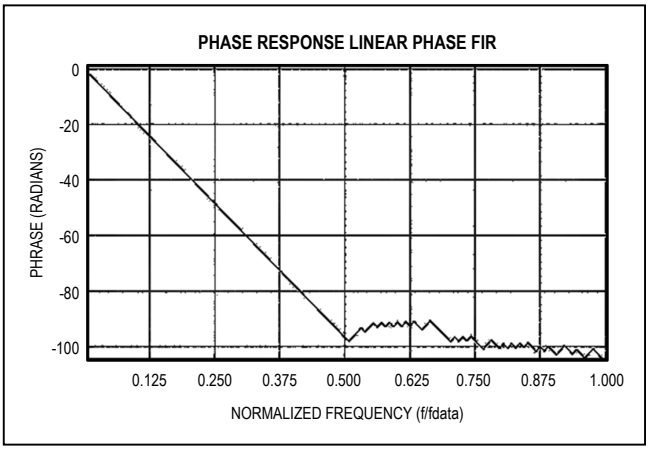


Figure 9. Phase Response, Linear Phase FIR, 4ksps Data Rate

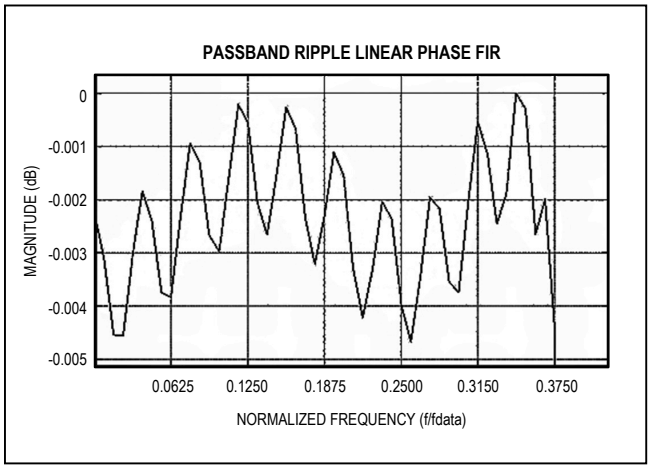


Figure 7. Passband Ripple, Linear Phase FIR, 4ksps Data Rate

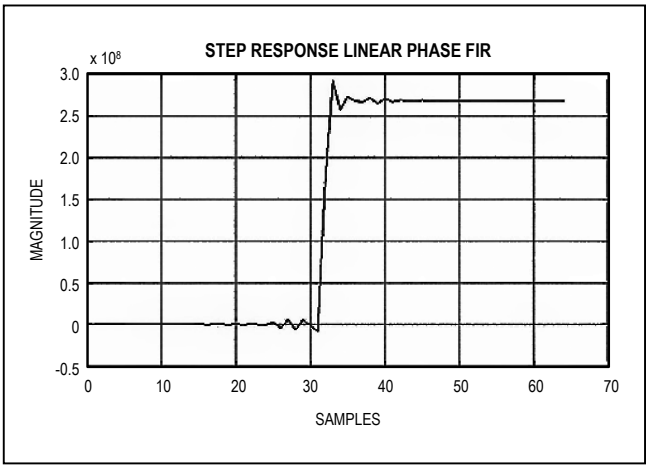


Figure 10. Step Response, Linear Phase FIR

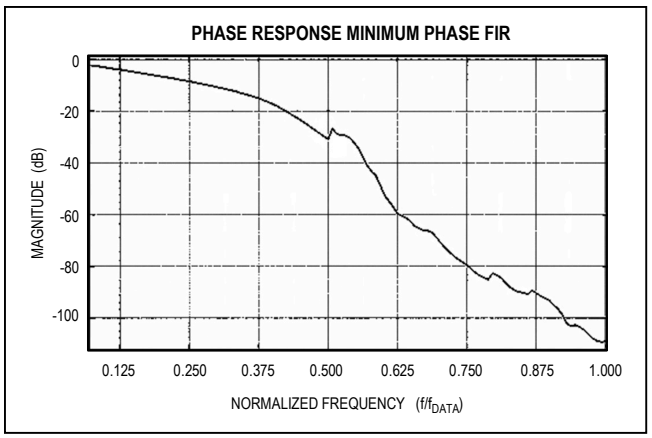


Figure 11. Phase Response, Minimum Phase FIR, 4ksps Data Rate

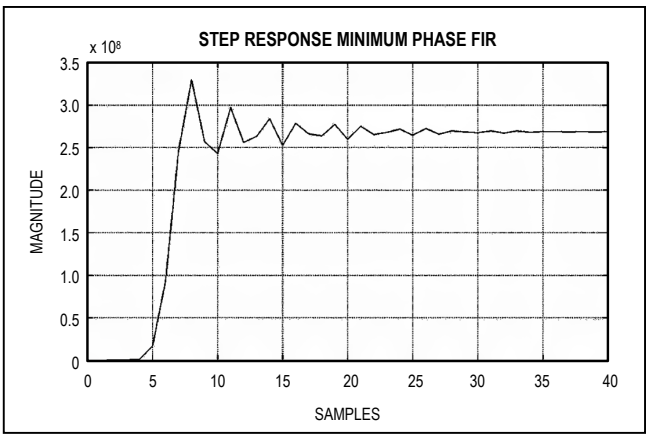


Figure 12. Step Response, Minimum Phase FIR

High-Pass Filter

The high-pass filter in each ADC has a selectable cutoff frequency and is used to reject DC/low-frequency components from the output. The IIR option is enabled by setting the FILT bits to '11' in the CTRL3 register (see Table 12). The 16-bit high-pass filter configuration register HPF configures the corner frequency of the IIR (infinite impulse response) digital filter. The transfer function for the IIR filter in z-domain is given by:

$$HPF(z) = \frac{2-a}{2} \times \frac{1-z^{-1}}{1-bz^{-1}}$$

where b is calculated from

$$b = \frac{1+(1-a)^2}{2}$$

The ideal HPF gain response is:

$$|HPF| = \frac{1+\sqrt{1-2\left(\frac{\cos\omega_N + \sin\omega_N - 1}{\cos_N}\right)}}{2-\left(\frac{\cos\omega_N + \sin\omega_N - 1}{\cos\omega_N}\right)}$$

where the normalized -3dB corner frequency is given by:

$$\omega_N = 2\pi\frac{f_{HP}}{f_S}$$

f_{HP} is the highest cutoff frequency and f_S is the data rate. To solve for the programmable register HPF value, use:

$$HPFR_{[15:0]} = 65536 \times \left(1-\sqrt{1-2\left(\frac{\cos\omega_N + \sin\omega_N - 1}{\cos\omega_N}\right)}\right)$$

Using the maximum High-pass Filter Register value typically gives a -3dB roll-off frequency equivalent to one tenth of the data rate. Note that not all values are allowed. Table 8 shows what maximum values HPF[15:0] can take for different data rates.

Table 9 shows a few examples of calculations for 3dB corner frequency.

Table 8. Max HPF[15:0] Register Values for Different Data Rates

CASE	FHP	DATA RATE	HPF[15:0] MAX VALUE
1	25	250	56492
2	102	1000	61787
3	204	2000	61787
4	409	4000	63164

Table 9. Examples of HPF [15:0] Register Values and Cutoff Frequencies

CASE	-3dB CORNER FREQUENCY (Hz)	HPF[15:0] (decimal)
1	$0.002f_S$	823
2	$0.001f_S$	410
3	$0.0005f_S$	203

Serial Interface

The serial interface for each ADC is fully compatible with SPI, QSPI™, and MICROWIRE-standard serial interfaces. The SPI interface provides access to on-chip registers that are 8 bits to 24 bits wide.

Chip-Select (CSB__)

CSB__ is an active-low, chip-select input to communicate with the ADC. CSB__ transitioning from low to high is used to reset the SPI interface. When CSB__ is low, data is clocked into the device from DIN on the rising-edge of SCLK. Data is clocked out of DOUT on the falling-edge of SCLK. When CSB__ is high, SCLK and DIN are ignored and DOUT is high impedance, allowing DOUT to be shared with other devices.

SCLK (Serial Clock)

The serial clock (SCLK) is shared by the two ADCs and is used to synchronize data communication between the host device and the ADCs. Data is shifted in on the rising-edge of SCLK and data is shifted out on the falling-edge of SCLK. SCLK remains low when not active.

DIN (Serial Data Input)

Data present on DIN (shared by the two ADCs) is clocked into internal registers on the rising edge of SCLK.

DOUT (Serial Data Output)

The DOUT pin is shared by the two ADCs and is actively driven when CSB__ is low and high impedance when CSB__ is high. Data are shifted out on DOUT on the falling-edge of SCLK.

Data Ready (RDYB__)

The RDYB__ outputs display the conversion status. RDYB__ is forced low when a conversion result is ready for readout and remains low until the conversion result has been read. RDYB__ returns high after SCLK is pulled high, following a complete read of the data register. RDYB__ also resets high for 4 master clock cycles prior to a DATA register update. (See Figure 13).

When the modulator is in one of the continuous conversion modes and the ADC has experienced either a RESET, SYNC, or POR event, the RDYB__ pin will remain high until the selected filter is settled. If the SINC filter is selected, RDYB__ remains high for five t_{CNV} times and, afterwards, data appears at each t_{CNV}.

The conversion status can also be determined by reading the MSTAT bit in the STAT1 register.

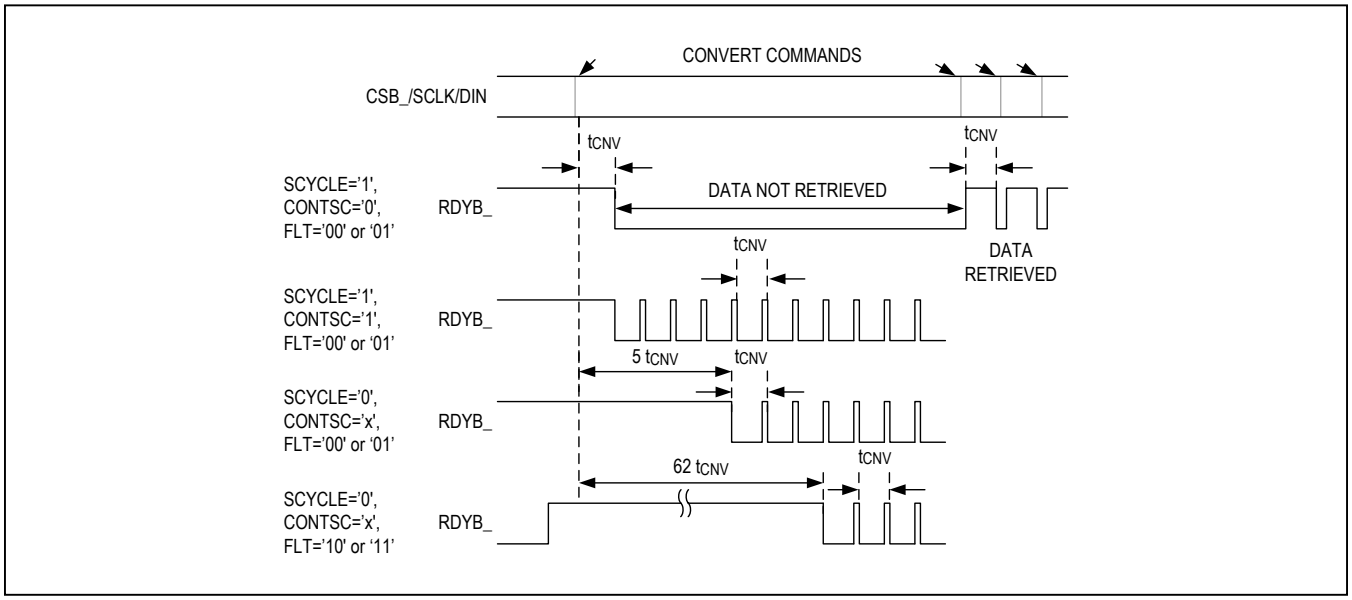


Figure 13. DATA Ready Timing for All Conversion Modes

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SPI Incomplete Write Command Termination

During register writes, the register values get updated every 8th clock cycle with a byte of data starting from the MSB. A minimum of 16 SCLKs are needed to write an 8-bit register or the first byte of data in a multibyte register. For example, a 24-bit register write requires 8 SCLKs for the register access byte and 24 SCLKs for the data bits to be written. If only 15 SCLKs are issued out of the 32 expected, the register value will not be updated. At least 16 SCLKs are required to update the MSB byte. For example, when a write command is issued for a 24-bit register write, but the transaction terminates after 16 SCLKs, only the MSB byte, (bits 23 to 16 of the register) is updated. Bits 15 to 0 retain the previous register values.

SPI Incomplete Read Command Termination

The SPI interface stays in read mode for as long as CSB stays low independent of the number of SCLKs issued. The CSB pin must be toggled high to remove the device from the bus and reset the internal SPI controller. Any activity on the DIN pin is ignored while in register read mode. The read operation is terminated if the CSB pin is toggled high before the maximum number of SCLK is issued.

When reading from DATA registers, the behavior of RDYB will depend on how many bits are read. If at least 23 bits are read, the read operation is complete and RDYB resets to high. If less than 23 bits are read, the internal logic considers the read incomplete and RDYB stays low. A new read can be initiated within the same conversion cycle and the new 24-bit read must complete before the next DATA register update.

SPI Timing Characteristics

The SPI timing diagrams illustrating command byte and register access operations are shown in Figure 14 through Figure 17. Input data is clocked in on rising-edges of SCLK. The timing allows for the input data to be changed by the user at both rising and falling-edges of SCLK. The data read out by the device on SCLK falling-edges can be sampled by the user on subsequent rising or falling-edges.

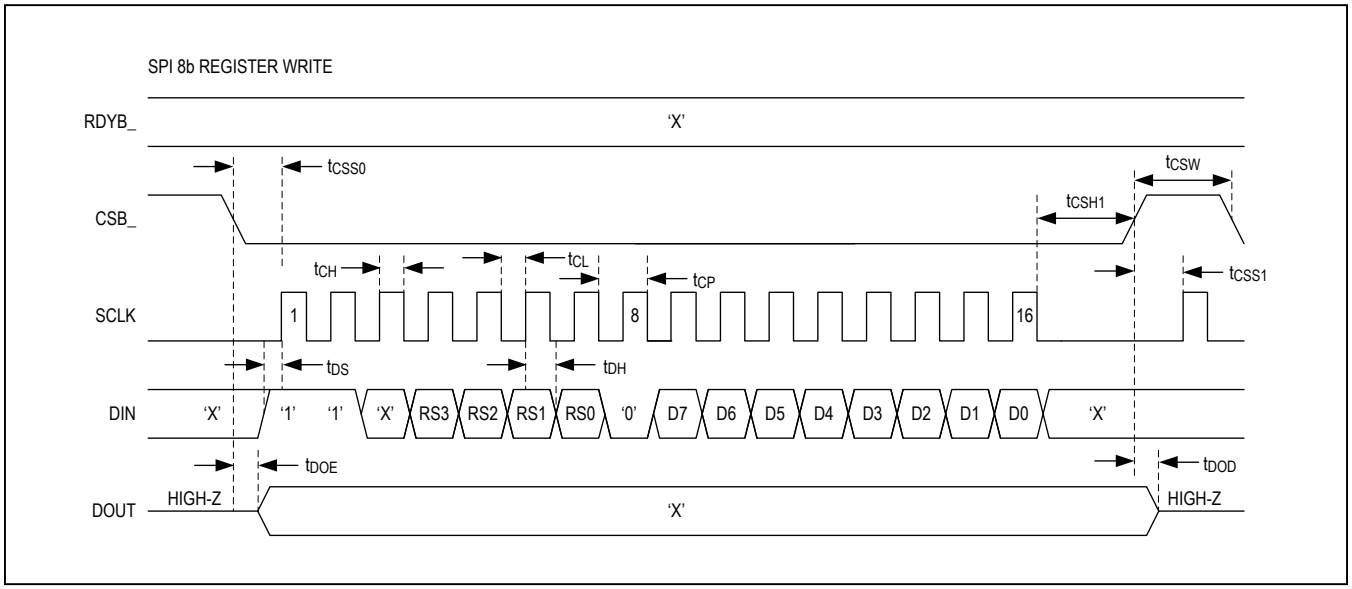


Figure 14. SPI Register Write Timing Diagram

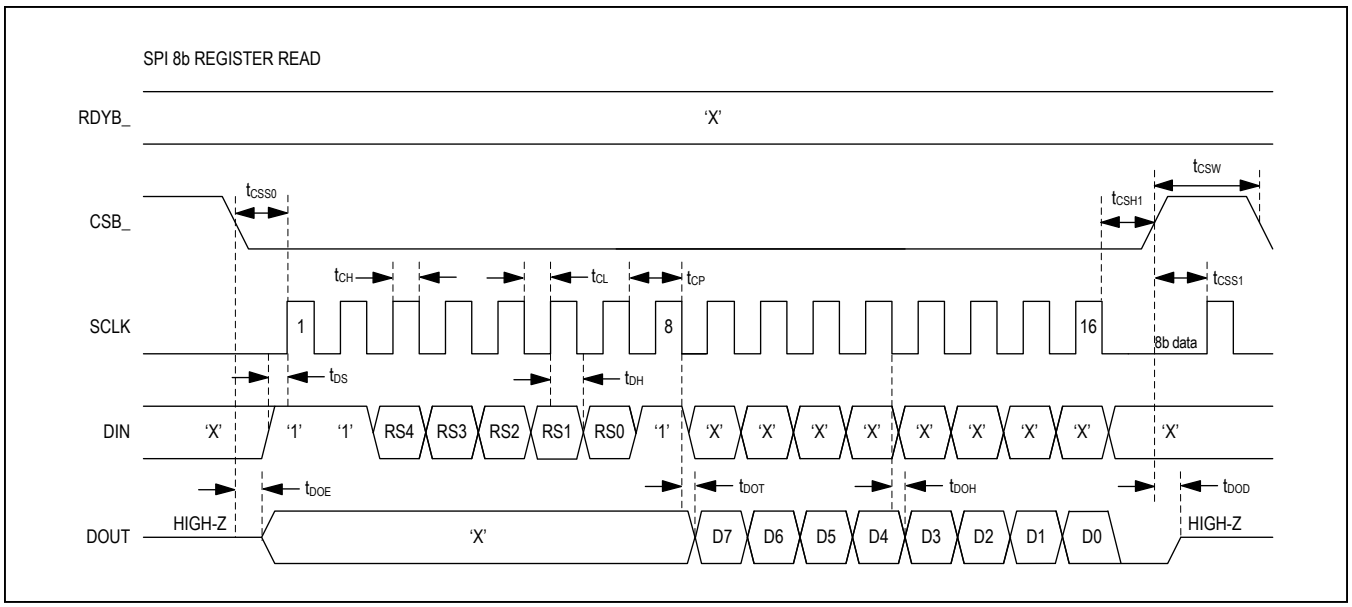


Figure 15. SPI Register Read Timing Diagram

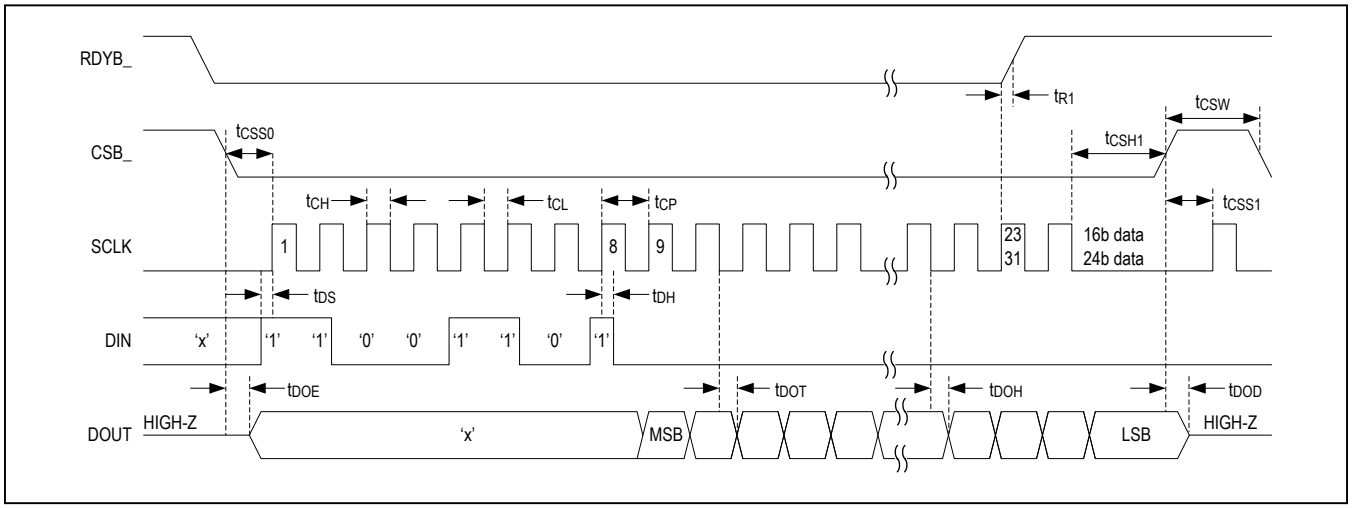


Figure 16. SPI Data Readout Timing Diagram

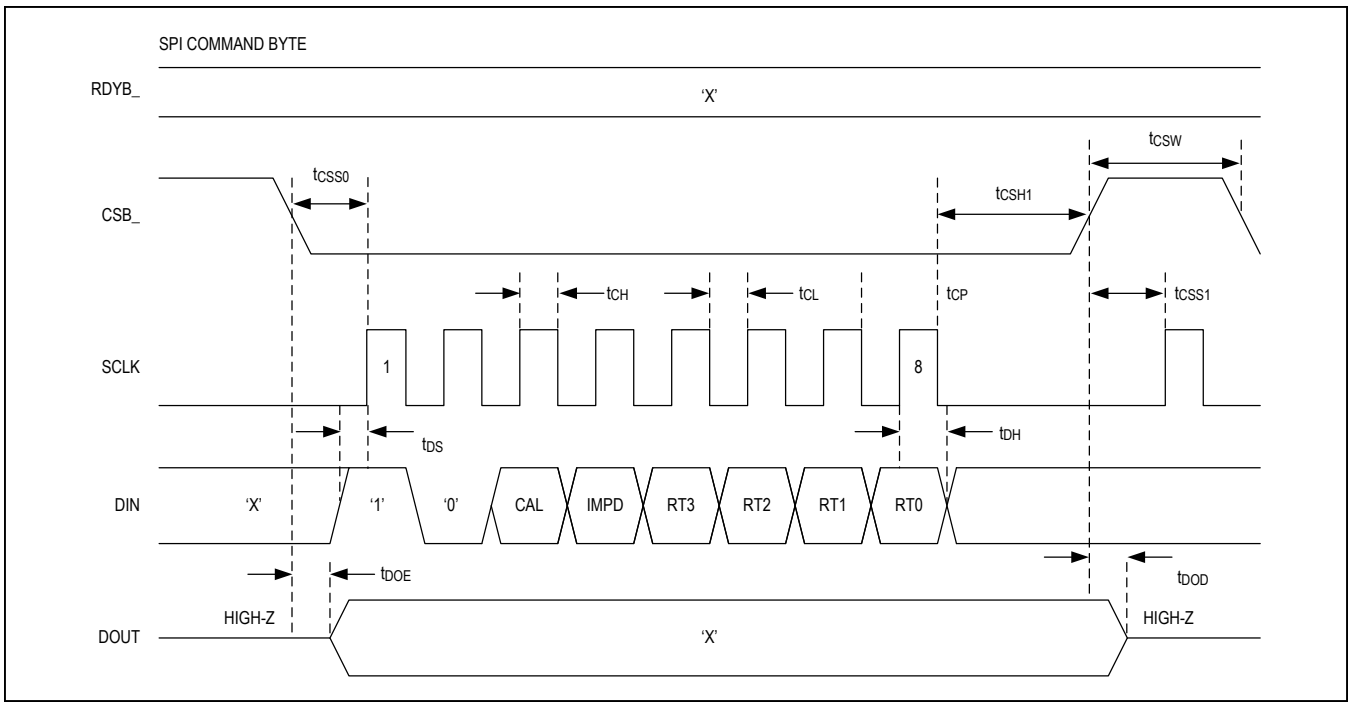


Figure 17. SPI Command Byte Timing Diagram

Modes and Registers

The SPI interface operates in two modes, conversion mode or register access mode, as selected by the command byte. Each ADC has its own independent set of control registers. Every SPI transaction to an ADC starts with a command byte. The command byte begins with a START bit (B7), which must be set to 1. The next bit is the MODE bit (B6), which selects between conversion mode or register access mode. Based on the mode selection, the remaining bits in the command byte get decoded accordingly.

If the command byte is for a register read/write request, hold CSB_ low for the entire read or write operation and pull CSB_ high at the end of the command. For example, if the command is to read a 24-bit data register; hold CSB_ low for 32 SCLK cycles (8 cycles of command plus 24 cycles of data). CSB transitions must not occur near the rising-edge of SCLK and must conform to the setup and hold timing detailed in the timing section.

Pulling CSB_ from low to high ends the current SPI transaction. If CSB_ is pulled high in the middle of an 8-bit register write command, the register will retain any previously written data. 24-bit registers are updated after each byte, so pulling CSB_ high after 12 clocks of a 24-bit write will update only the first 8 bits written.

Conversion Mode (MODE = 0)

Set the MODE bit to 0 to: start a conversion with a rate defined by RATE[3:0], immediately power down the ADC or perform a calibration.

The CAL bit (B5) determines if a calibration is to be performed. Set CAL = 1 to perform a calibration; for all other opera- tions set CAL = 0. The calibration is done based on the setting of the calibration bits in register CTRL 5. Also see discussion on calibration in the following sections. Do not set IMPD = 1 and CAL = 1 in the same command.

The IMPD bit (B4) controls the software power-down. Set IMPD = 1 to power down the MAX11284 and enter sleep mode or standby mode, based on the setting of the PD Bits in CTRL1, once the command byte is complete. The power-down status does not change until another command byte is received that is interpreted as a conversion byte (MODE = 0, IMPD = 0). Set IMPD = 0 for normal operation.

The data rate bits RATE[3:0] determine the conversion speed. Sample rates from 0.4875sps to 16ksps are programmable through the RATE bits. Table 13 shows available conversion rates.

Register Access Mode (MODE = 1)

MODE 1 or Register Access Mode is used for reading from and writing to the registers of the ADCs. Set the MODE bit (B6) = 1 to configure the command byte for Register Access Modes. The bits RS[4:0] determine the register that is addressed as shown in Table 11. The R/W bit enables either a read or a write of the register. Set R/W = 0 to write to the selected register and R/W = 1 to read from the selected register.

Register Map

There are 14 registers that can be accessed in each of the ADCs. The majority of registers can be both written to and read from, but the STAT and DATA registers are read only. RAM and SYNC are not physical registers, but addresses to enable special operating modes.

Table 10. Command Byte for Conversion Modes (MODE = 0)

BIT	B7 (MSB)	B6	B5	B4	B3	B2	B1	B0
BIT NAME	START = 1	MODE = 0	CAL	IMPD	RATE3	RATE2	RATE1	RATE0

Table 11. Command Byte for Register Access Mode (MODE = 1)

BIT	B7 (MSB)	B6	B5	B4	B3	B2	B1	B0
BIT NAME	START =1	MODE = 1	RS4	RS3	RS2	RS1	RS0	R/W

Table 12. Register Map

REGISTER NAME	R/W	ADDRESS SELECT RS[3:0]	B7	B6	B5	B4	B3	B2	B1	B0
STAT	R	0x0	INRESET	ERROR	—	—	PDSTAT1	PDSTAT0	RDERR	AOR
			RATE3	RATE2	RATE1	RATE0	SYSGOR	DOR	MSTAT	RDY
CTRL1	R/W	0x1	EXTCK	SYNC MODE	PD1	PD0	U/~B	FORMAT	SCYCLE	CONTSC
CTRL2	R/W	0x2	DGAIN1	DGAIN0	BUFEN	LPMODE	PGAEN	PGAG2	PGAG1	PGAG0
CTRL3	R/W	0x3	—	—	—	—	—	PHASE	FILT1	FILT0
CTRL4	R/W	0x4	—	DIR3	DIR2	DIR1	—	DIO3	DIO2	DIO1
CTRL5	R/W	0x5	CAL1	CAL0	—	—	NOSYSG	NOSYSO	NOSCG	NOSCO
DATA	R	0x6	D[23:0]							
SOC_SPI	R/W	0x7	B[23:0]							
SGC_SPI	R/W	0x8	B[23:0]							
SCOC_SPI	R/W	0x9	B[23:0]							
SCGC_SPI	R/W	0xA	B[23:0]							
HPF	R/W	0xB	B[15:0]							
RAM	R/W	0xC	Address Space Only, Not a Physical Register. Please contact factory for instructions on using internal RAM function.							
SYNC_SPI	W	0xD	Address Space Only, Not a Physical Register. Please contact factory for instructions on using internal RAM function.							
SOC_ADC	R	0x15	B[23:0]							
SGC_ADC	R	0x16	B[23:0]							
SCOC_ADC	R	0x17	B[23:0]							
SCGC_ADC	R	0x18	B[23:0]							

Status Register (Read Only)

The 16-bit STAT register is a read-only register that indicates the following: power-down status, modulator reset or overload, data rate, over-range condition, measurement in progress, and measurement complete.

BIT	B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
BIT NAME	INRESET	ERROR	—	—	PDSTAT1	PDSTAT0	RDERR	AOR	RATE3	RATE2	RATE1	RATE0	SYSGOR	DOR	MSTAT	RDY
DEFAULT	0	0	1	1	1	0	0	0	1	0	0	1	0	0	0	0

BIT	DEFAULT	LABEL	FUNCTION
00	0	RDY	Ready Bit. RDY = 1 when a new conversion result is available. A read of the DATA register resets RDY = 0. The function of the RDY bit is redundant and is duplicated by RDYB pin.
01	0	MSTAT	Measurement Status Bit. MSTAT = 1 indicates that a conversion, self-calibration, or system calibration is in progress and that the modulator is busy. When the modulator is not converting, MSTAT = 0.
02	0	DOR	Data Overrange Bit. DOR = 1 indicates that the conversion result has exceeded the maximum or minimum value and that the result has been clipped or limited to the maximum value. DOR = 0 when the conversion result is within the full-scale range.
03	0	SYSGOR	System Gain Overrange Bit. SYSGOR = 1 indicates that a system gain calibration was overranged. The SGC calibration coefficient maximum value is 1.9999999.
04	1	RATE0	Data Rate Bits. See Table 13. The RATE bits indicate the conversion rate that corresponds to the result in the DATA register or the rate that was used for calibration coefficient calculation. **Note:** RATE bits always show the rate of previous conversion and not the rate of the conversion in progress.
05	0	RATE1	
06	0	RATE2	
07	1	RATE3	
08	0	AOR	Analog Overrange Bit. AOR = 1 when the modulator detects that the analog input voltage exceeds 1.3 x full-scale range.
09	0	RDERR	Data Read Error Bit. RDERR = 1 when new result is being written to the DATA register while user is reading from the DATA register. RDERR = 0 otherwise.
10	0	PDSTAT0	00: ADC is converting 01: Device is fully powered down 10: In standby mode with modulator powered off but subregulator powered ON. 11: Reserved.
11	1	PDSTAT1	
12	1	—	—
13	1	—	—
14	0	ERROR	Error Bit. ERROR = 1 when CAL[1:0] bits are set to invalid setting of 11.
15	0	INRESET	In Reset Bit. INRESET = 1 when software reset is initiated until the ADC exits reset mode.

Table 13. Programmable Conversion Rates

RATE[3:0]	CONTINUOUS DATA RATE, SCYCLE = 0		SCYCLE = 1 SINGLE-CYCLE CONTINUOUS DATA RATE (sps)
	SINC FILTER (sps)	FIR FILTER (sps)	
0000	0.4875	—	12.5
0001	0.975	—	15.7
0010	1.95	—	25
0011	3.9	—	31.2
0100	7.8	—	50
0101	15.6	—	62
0110	31.3	31.25	100
0111	62.5	62.5	125
1000	125	125	200
1001	250	250	250
1010	500	500	400
1011	1000	1000	500
1100	2000	2000	400
1101	4000	4000	1000
1110	8000	—	1480
1111	16000	—	2767

**Continuous data rate with SCYCLE = 0, single cycle with CONTSC = 1, SCYCLE = 1. The FIR filter can operate only in continuous conversion mode.*

Control Registers

These registers configure the operation of the two ADCs.

Control 1 Register (Read/Write)

The CTRL1 register is an 8-bit read/write register. The byte written to the CTRL1 register determines the clock setting, synchronization mode, power-down or reset state, input range (unipolar or bipolar), data output format (two's complement

BIT	B07	B06	B05	B04	B03	B02	B01	B00
BIT NAME	EXTCK	SYNC	PD1	PD0	U/B	FORMAT	SCYCLE	CONTSC
DEFAULT	0	0	0	0	0	0	1	0

BIT	DEFAULT	LABEL	FUNCTION	
00	0	CONTSC	Continuous/Single Conversion Bit. Set CONTSC = 1 to select continuous conversions. Continuous conversion mode has a latency of 5 conversion cycles with a SINC filter and 62 conversion cycles with SINC + FIR filter whenever it restarts from a RESET, RSTB, SYNC, or POR state. The latency is due to the digital filter and the RDYB pin is held high until valid data is available. Set CONTSC = 0 to select single-cycle, no-latency conversions.	
01	1	SCYCLE	Single-Cycle Control Bit. Controls whether single-cycle conversions (selected by CONTSC = 0) will occur once or repeat continuously. Set SCYCLE = 1 to select single-conversion mode, in which the ADC completes one no-latency conversion and then powers down into a leakage-only state. Set SCYCLE = 0 to select continuous single-cycle conversions. No effect when CONTSC = 1.	
02	0	FORMAT	Bipolar Range Format Bit. When reading bipolar data, set FORMAT = 0 to select two's complement and FORMAT = 1 to select offset binary. When unipolar range is selected through the U/B bit, the data is always formatted in offset binary format.	
03	0	U/B	U/B: Unipolar/Bipolar Bit. Set U/B = 1 to select the unipolar input range (0 to V_{REF}). Set U/B = 0 to select the bipolar input range ($\pm V_{REF}$).	
04	0	PD0	00	Normal Power-Up State. This is the default state.
			01	Sleep Mode: Powers down the internal subregulator and the digital circuitry. Upon resumption of power to the digital the PD[1:0] reverts to the default state of '00'.
05	0	PD1	10	Standby Power: Powers down the analog blocks, leaving the subregulator powered up.
			11	Resets all registers to the POR state, leaving the subregulator powered, then resets the PD[1:0] bits to '00'. The operation of this state is identical to the RSTB pin.
06	0	SYNC	Set SYNC = 1 to select continuous synchronization mode. Set SYNC = 0 to select pulse synchronization mode.	
07	0	EXTCK	External Clock Bit. Set EXTCLK = 1 to select the external clock as the system clock. Set EXTCLK = 0 to select the internal oscillator as the system clock.	

Control 2 Register (Read/Write)

The CTRL2 register is an 8-bit read/write register. The byte written to the CTRL2 register determines the digital and analog gain settings, and enables/disables the buffers and the PGA.

BIT	B07	B06	B05	B04	B03	B02	B01	B00
BIT NAME	DGAIN1	DGAIN0	BUFEN	LPMODE	PGAEN	PGAG2	PGAG1	PGAG0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DEFAULT	LABEL	FUNCTION	
00	0	PGA0	000 001 010 011 100 101 110 111	X1 PGA Gain-Setting bits X2 X4 X8 X16 X32 X64 X128
01	0	PGA1		
02	0	PGA2		
03	0	PGAEN	PGA Enable Bit. Set PGAEN = 1 to enable the PGA. Set PGAEN = 0 to disable the PGA.	
04	0	LPMODE	PGA Low Power. Set LPMODE = 1 for lower power. Set LPMODE = 0 for standard power.	
05	0	DGAIN0	Analog Input Buffer Enable Bit. Set BUFEN = 1 to enable the analog input buffers. Set BUFEN = 0 to disable the analog input buffers. Buffer is always disabled when PGA is enabled.	
06	0	DGAIN0	Modulator Digital Gain Bits. These left-shift the conversion data to provide “digital gain”.	
			00	x1
			01	x2
07	0	DGAIN1	10	x4
			11	x8

Control 3 Register (Read/Write)

The CTRL3 register is an 8-bit read/write register. The byte written to the CTRL3 register determines the FIR filter phase and selected filters.

BIT	B07	B06	B05	B04	B03	B02	B01	B00
BIT NAME	—	—	—	—	—	PHASE	FILT1	FILT0
DEFAULT	0	1	1	0	0	0	0	1

BIT	DEFAULT	LABEL	FUNCTION	
00	1	FILT0	Filter Control Bits. When SCYCLE = 1 (CTRL1 register), only the SINC filter is enabled regardless of the values of FILT0 and FILT1.	
01	0	FILT1	0x	SINC
			10	FIR
			11	FIR + IIR
02	0	PHASE	PHASE: FIR Filter Phase Bit. Set PHASE = 1 to select minimum phase. Set PHASE = 0 to select linear phase.	
03	0	—	Reserved Bit	
04	0	—	Reserved Bit	
05	1	—	Reserved Bit	
06	1	—	Reserved Bit	
07	0	—	Reserved Bit	

Control 4 Register (Read/Write)

The CTRL4 register is an 8-bit read/write register. The byte written to an ADC's CTRL4 register determines whether the associated GPIO__ is an input or an output, and allows its state to be set or read.

BIT	B07	B06	B05	B04	B03	B02	B01	B00
BIT NAME	—	—	—	DIR	—	—	—	DIO
DEFAULT	0	0	0	0	1	1	1	1

BIT	DEFAULT	LABEL	FUNCTION
00	1	DIO	GPIO Bit Value. When GPIO is configured as an output, set DIO to select the GPIO output state. When GPIO is configured as an input, this bit indicates the pin status.
01	1	—	Reserved Bit
02	1	—	Reserved Bit
03	1	—	Reserved Bit
04	0	DIR	GPIO Direction Bit. Set DIR = 0 to configure GPIO as an input. The value returned by a read of the DIO bit is the value being driven on the GPIO pin. Set DIR = 1 to configure GPIO as an output. GPIO is driven to the logic value of the DIO bit.
05	0	—	Reserved Bit
06	0	—	Reserved Bit
07	0	—	Reserved Bit

Control 5 Register (Read/Write)

The CTRL5 register is an 8-bit read/write register. The byte written to the CTRL5 register determines the ADC's reset, data overflow, and calibration modes.

BIT	B07	B06	B05	B04	B03	B02	B01	B00
BIT NAME	CAL1	CAL0	—	—	NOSYSG	NOSYSO	NOSCG	NOSCO
DEFAULT	0	0	0	0	1	1	0	0

BIT	DEFAULT	LABEL	FUNCTION	
00	0	NOSCO	No Self-Calibration Offset Bit. Set NOSCO = 1 to disable the use of the self-calibration offset value when computing the final offset and gain-corrected data value. Set NOSCO = 0 to enable the use of the self-calibration offset value when computing the final offset and gain-corrected data value. Setting NOSCO = 1 has no effect on the calibration process.	
01	0	NOSCG	No Self-Calibration Gain Bit. Set NOSCG = 1 to disable the use of the self-calibration gain value when computing the final offset and gain-corrected data value. Set NOSCG = 0 to enable the use of the self-calibration gain value when computing the final offset and gain-corrected data value. Setting NOSCG = 1 has no effect on the calibration process.	
02	1	NOSYSO	No System Offset Bit. Set NOSYSO = 1 to disable the use of the system offset value when computing the final offset and gain-corrected data value. Set NOSYSO = 0 to enable the use of the system offset value when computing the final offset-corrected data value. Setting NOSYSO = 1 has no effect on the calibration process.	
03	1	NOSYSG	No System Gain Bit. Set NOSYSG = 1 to disable the use of the system gain value when computing the final offset and gain-corrected data value. Set NOSYSG = 0 to enable the use of the system gain value when computing the final gain-corrected data value. Setting NOSYSG = 1 has no effect on the calibration process.	
04	0	—	Reserved Bit.	
05	0	—	Reserved Bit	
06	0	CAL0	00	Perform Self-Calibration
			01	Perform System-Level Offset Calibration
07	0	CAL1	10	Perform System-Level Full-Scale Calibration
			11	Reserved

Data Register (Read-Only)

The data register is a 24-bit read-only register. Any attempt to write data to the data register has no effect. The data from this register is clocked out MSB first. The data register holds the conversion result. The result is stored in either two's complement or offset binary format, depending on the FORMAT bit in CTRL1 register.

The data format in unipolar mode is always offset binary. In bipolar mode, set the FORMAT bit = 1 for offset binary or FORMAT = 0 for two's compliment. Any input exceeding the available input range is limited to the minimum or maximum data value.

BIT	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 14. ADC Output Code Data Format

CODE DESCRIPTION	INPUT VOLTAGE (VAINP-VAINN)	DIGITAL OUTPUT CODE	
		OFFSET BINARY	2's COMPLEMENT
Positive Full Scale	≥V_{REF}	0xFFFFFF	0x7FFFFF
Positive FS – 1LSB	$V_{REF}(1-1/(2^{23}-1))$	0xFFFFFE	0x7FFFFE
Positive Mid-Scale	$V_{REF}(1+1/(2^{23}-1))/2$	0xC00000	0x400000
Positive 1 LSB	$V_{REF}/(2^{23}-1)$	0x800001	0x000001
Zero	0V	0x800000	0x000000
Negative 1 LSB	$-V_{REF}/(2^{23}-1)$	0x7FFFFF	0xFFFFFF
Negative FS + 1LSB	$-V_{REF}$	0x000001	0x800001
Negative FS	$-V_{REF}(1+1/(2^{23}-1))$	0x000000	0x800000

$V_{REF} = V_{REFP\_\_} - V_{REFN\_\_}$.

Calibration

Two types of calibration are available: self-calibration and system calibration. Self-calibration is used to reduce the ADC gain and offset errors after changes in operating conditions such as supply voltages, ambient temperature, and time. System calibration is used to reduce the gain and offset of the entire signal path. This enables calibration of board level components and the integrated PGA. System calibration requires the ADC inputs to be reconfigured for zero-scale and full-scale during calibration. See Figure 18 for details of the calibration signal flow.

The on-chip calibration registers are enabled or disabled by programming the NOSYSG, NOSYSO, NOSCG, and NOSCO bits in the CTRL5 register. See Table 12.

Self-Calibration

Self-calibration is an internal operation and does not disturb the analog inputs. Self-calibration is accomplished in two independent phases, offset and gain. The first phase disconnects the inputs to the modulator and shorts them together internally to develop a zero-scale input. A conversion is then completed and the results are post-processed to generate an offset coefficient which cancels all internally generated offsets. The second phase connects the inputs to the reference to develop a full-scale signal. A conversion is then completed and the results are post-processed to generate a full-scale coefficient, which scales the converter's full-scale analog range to the full-scale digital range.

The entire self-calibration sequence requires two independent conversions, one for offset and one for full-scale.

The conversion rate for self-calibration is 50sps which provides the lowest noise and most accurate calibrations. The self-calibration operation excludes the PGA. A system-level calibration is available in order to calibrate the PGA signal path.

The calibration operations are controlled with the CAL bit in the command byte. Request a self-calibration by setting the CAL bit to 1, with the CTRL5:CAL[1:0] = 00. A self-calibration requires 200ms to complete, and both the SCOC and SCGC registers contain the values that correct the chip output for zero scale and full scale.

System Calibration

This mode is used when board level components and the integrated PGA calibration is desired. A system calibration requires the user to configure the input to the proper level for the calibration operation. The offset and full-scale system calibrations are performed using separate command bytes by configuring the CTRL5:CAL [1:0] bits. The system offset and system full scale require setting these CAL bits appropriately before issuing the calibration command byte.

Request a system zero-scale calibration by setting the CAL bit to 1 and CTRL5:CAL[1:0] = 01, and connecting a system zero-level signal to the input pins. The system zero calibration requires 100ms to complete, and the SOC register contains values that correct the chip zero-scale.

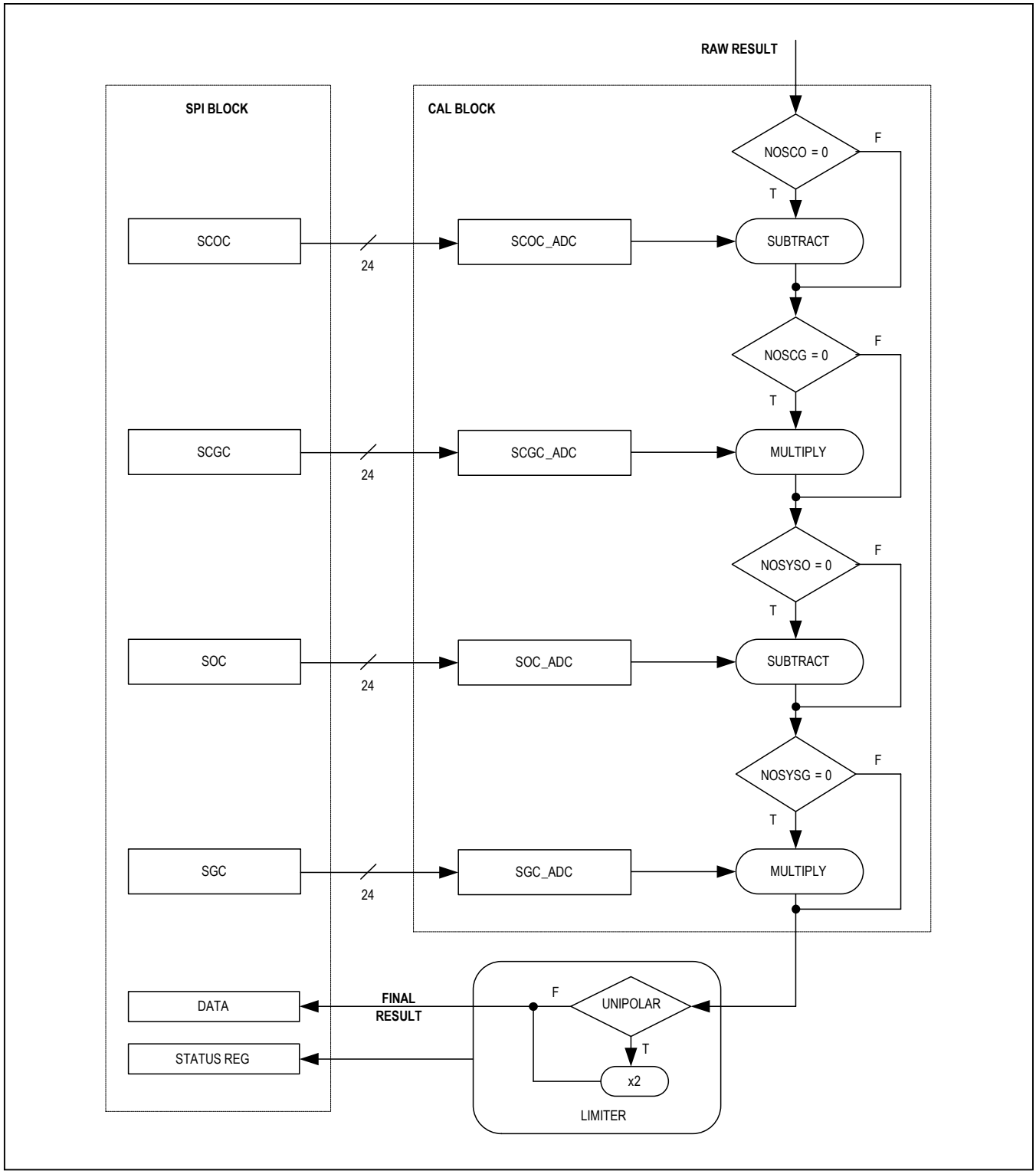


Figure 18. Calibration Flow Diagram

Request a system full-scale calibration by setting the CAL bit to 1 and CTRL5:CAL[1:0] = 10 and connect a system full-scale signal level to the input pins. The system full-scale calibration requires 100ms to complete, and the SGC register contains values that correct for the chip full-scale value.

A third level of calibration allows a write to the internal calibration registers through the SPI interface to achieve any digital offset or scaling with the following restrictions. The range of digital offset correction is $\pm V_{REF}/4$. The resolution of offset correction is 0.5 LSB. The range of digital gain correction is from 0.75 to 2. The resolution of gain is less than 1ppm.

SPI System Offset Calibration Register (SOC_SPI)

The system offset calibration register is a 24-bit read/write register. The data written/read to/from this register is clocked in/out MSB first. The format is always in two's complement. This register temporarily holds the system offset calibration value from the user. This value gets copied into the SOC_ADC register. The value written to this register remains until it is overwritten. This value gets invalidated for calibration after a system-calibration operation is requested. Any attempt to write to this register during an active calibration operation will be ignored.

ADC System Offset Calibration Register (SOC_ADC)

This is 24-bit read-only register. There are two ways this register value is updated. One way is if a system offset calibra- tion operation is requested. Another way is if a user writes a value to SOC_SPI register, the value will then get copied into SOC_ADC from SOC_SPI.

The system offset calibration value is subtracted from each conversion result if NOSYSO = 0 in the CTRL5 register. The system offset calibration value is subtracted from the conversion result after self-calibration, but before system gain correction. It is also applied prior to the 1x or 2x scale factor associated with bipolar and unipolar modes.

SPI System Gain Calibration Register (SGC_SPI)

The system gain calibration register is a 24-bit read/write register. The data written/read to/from this register is clocked in/out MSB first. The format is always in two's complement format. This register temporarily holds the system gain calibration value from the user. Once a conversion command is requested, this value gets copied into SGC_ADC register. The value written to this register remains until it is overwritten. This value gets invalidated for calibration after a system-calibration operation is requested. Any attempt to write to this register during an active calibration operation will be ignored.

ADC System Gain Calibration Register (SGC_ADC)

This is 24-bit read-only register. There are two ways this register value is updated. One way is if a system offset calibration operation is requested. Another way is if a user writes a value to SGC_SPI register, the value will then get copied into SGC_ADC from SGC_SPI.

The system gain calibration value is used to scale the offset-corrected conversion result if NOSYSG = 0 in the CTRL5 register. The system gain calibration value scales the gain corrected result by up to 2x or can correct a gain error of approximately -50%. The amount of positive gain error that can be corrected is determined by modulator overload characteristics which may be as much as +25%. The gain will be corrected to within 1ppm.

SPI Self-Cal Offset Calibration Register (SCOC_SPI)

The self-cal offset register is a 24-bit read/write register. The data written/read to/from this register is clocked in/out MSB first. The format is always in two's complement format. This register temporarily holds the self-cal offset calibration value from the user. This value gets copied into SCOC_ADC register. The value written to this register remains until it is overwritten. This value gets invalidated for calibration after a system-calibration operation is requested. Any attempt to write to this register during an active calibration operation will be ignored.

ADC Self-Cal Offset Calibration Register (SCOC_ADC)

This is a 24-bit read-only register. There are two ways this register value is updated. One way is if a self-cal operation is requested. Another way is if a user writes a value to SCOC_SPI register, the value will then get copied into SCOC_ADC from SCOC_SPI.

The self-cal offset value is a 24-bit two's complement value. It is subtracted from each conversion result if NOSCO = 0 in the CTRL5 register. The self-cal offset value is subtracted from the conversion result before the self-calibration gain correction and before the system offset and gain correction. It is also applied prior to the 2x scale factor associated with unipolar mode.

SPI Self-Cal Gain Calibration Register (SCGC_SPI)

The self-cal gain calibration register is a 24-bit read/write register. The data written/read to/from this register is clocked in/ out MSB first. The format is always in two's complement format. This register temporarily holds the self-cal offset calibration value from the user. This value

gets copied into SCOC_ADC register. The value written to this register remains until it is overwritten. This value gets invalidated for calibration after a system-calibration operation is requested. Any attempt to write to this register during an active calibration operation will be ignored.

ADC Self-Cal Gain Calibration Register (SCGC_ADC)

This is a 24-bit read-only register. There are two ways this register value is updated. One way is if a self-cal operation is requested. Another way is if a user writes a value to SCGC_SPI register, the value will then get copied into SCGC_ADC from SCGC_SPI.

The self-cal gain calibration value is used to scale the self-cal offset corrected conversion result before the system offset and gain calibration values have been applied—provided NOSCG = 0 in the CTRL5 register. The self-cal gain calibration value scales the self-cal offset corrected conversion result by up to 2x or can correct a gain error of approximately -50%. The value in the gain calibration register is an unsigned number as follows:

FFFFFF = 1.99999

800000 = 1.00000

3FFFFF = 0.50000

1FFFFF = 0.25000

Entering a gain calibration value less than 0.75 should be avoided, as this could lead to modulator overload for a full-scale output.

High-Pass Filter Configuration Register (Read/Write)

The high-pass filter configuration register programs the corner frequency of the IIR high-pass filter. Any attempt to write to this register during an active conversion operation will be ignored. This register should be updated during standby or sleep modes only. See the *High-Pass Filter* section for information on selecting values.

BIT	B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
DEFAULT	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	0

GPIOs

Each ADC provides a general-purpose input/output port that can be programmed through the CTRL4 register. Set the DIR bit in the CTRL4 register to configure GPIO__ as an input or an output. GPIO__ pins are inputs by default. When programmed as an output, set the DIO bit in the CTRL4 register to set pin state to 0 or 1.

Conversion Synchronization Using SYNC__ Pins or SYNC_SPI Function

Each ADC's SYNC__ pin can be used to synchronize the data conversions to external events. This can be done either by either pulling the SYNC__ pin high or by addressing the SYNC_SPI register in a SPI command byte. There are two methods available to synchronize conversion results using external signals on the SYNC__ pins: continuous mode or pulse mode.

Continuous Mode

In continuous synchronization mode, conversions are synchronized to a continuous series of synchronization pulses with a period greater than the data period. The ADC compares the number of device master clocks (either internally generated or from the CLK input) between the RDYB__ assertion to the rising edge of the SYNC__ pin. The relative edges of RDYB__ and SYNC__ should stay aligned within 1 master clock period of the initial SYNC__ pulse and remain within integer multiples of the data rate. If the rising-edge of the SYNC__ pin occurs after an integer multiple of the data rate, and is greater than plus or minus 1 master clock period from the initial SYNC__ rising edge, the chip resets the conversion in progress, flushes the digital filter contents, and starts a new conversion. The conversion reset process incurs the full digital filter latency before valid results are available.

See Figure 19 for timing waveform relationships between the chip master clock and the SYNC pin. Due to startup delays, any SYNC__ pin assertions before the first RDYB__ assertion are ignored. The first SYNC__ pin assertion after a RDYB__ assertion establishes the relationship between the SYNC__ pin and the conversion ready signal, timed in master clock units. This relationship is defined as n, which constitutes the number of clocks that occur between the assertion of RDYB__ and the rising-edge of the SYNC__ pin.

Pulse Mode

Pulse or single-event synchronization mode starts a new conversion upon the rising-edge of the SYNC__ pin. When the SYNC__ pin is asserted, the chip begins conversions using the speed settings from the previous convert command. If no previous convert command was issued prior to the SYNC__ pin asserting, then the default conversion speed of 1ksps is used. Note that the convert start command and the SYNC__ pin rising edge cannot be applied at the same time. Any activity on the SYNC__ pin is ignored until after the first RDYB__ assertion following a convert start. This is required due to convert start overhead, which delays the first conversion result by 32 master clocks.

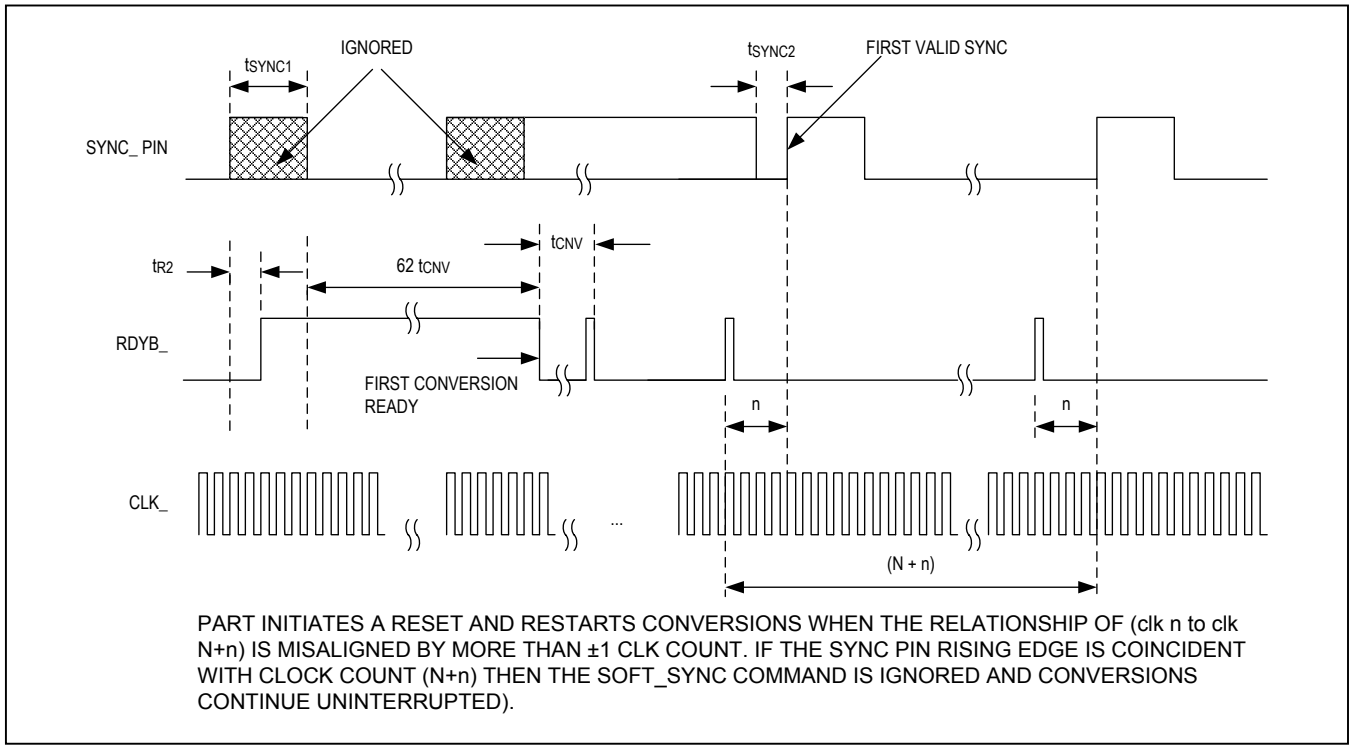


Figure 19. Synchronization Using Continuous Sync Mode Showing Relationship Between SYNC Pin and CLK Pin

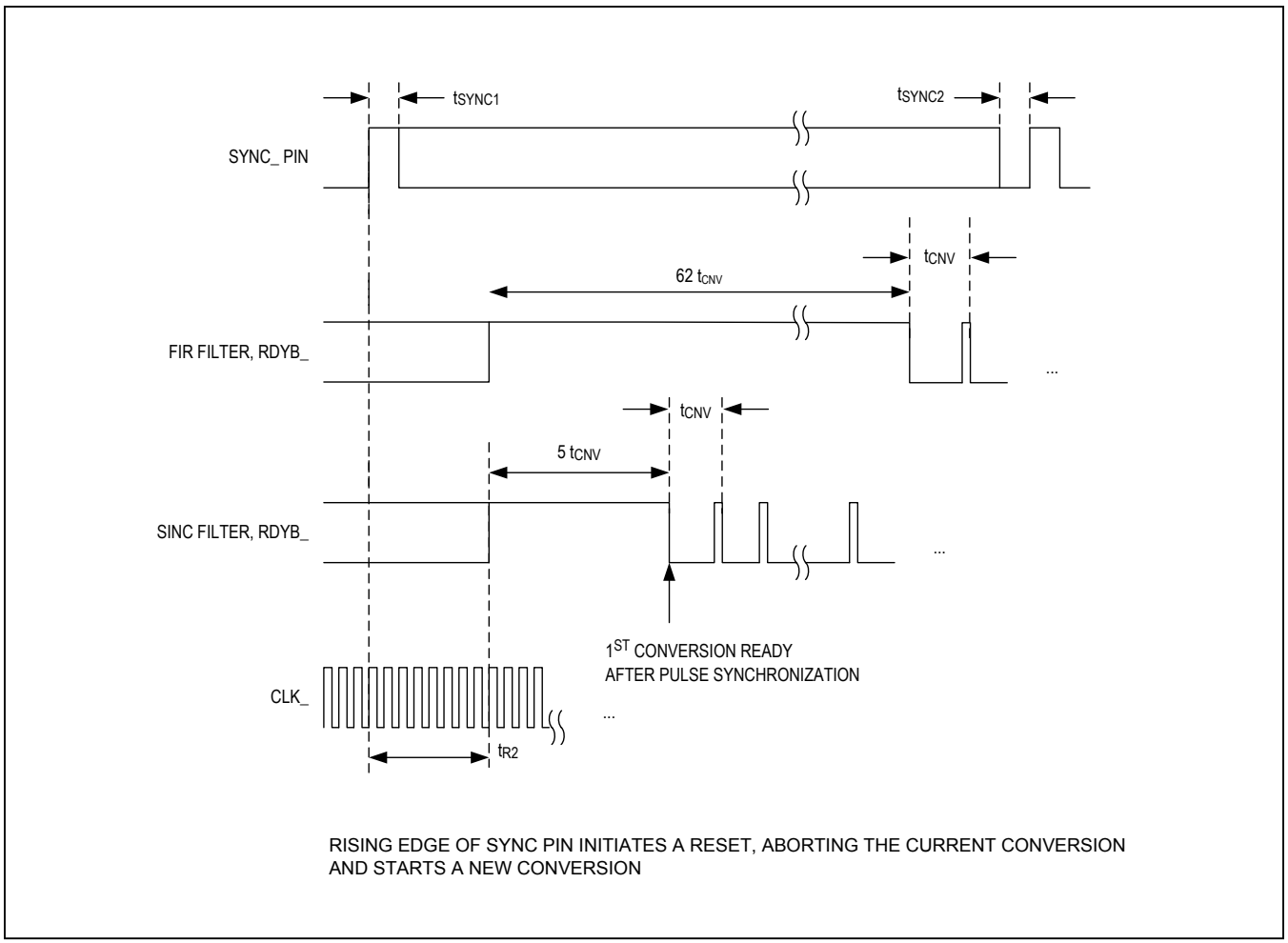
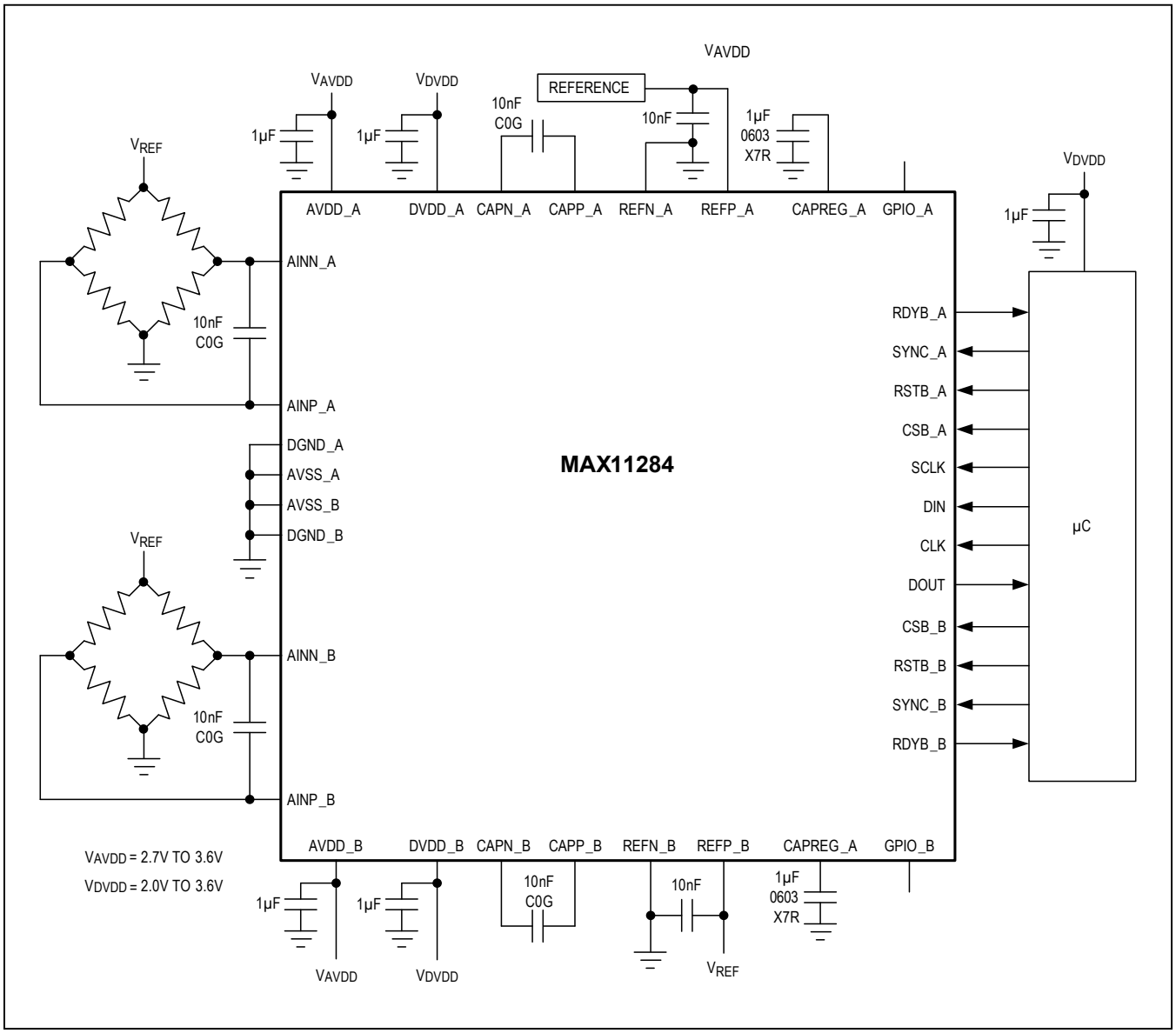


Figure 20. Synchronization Using Pulse Sync Mode Showing Relationship Between SYNC, RDYB, and CLK Pins

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX11284ETL+	-40°C to +85°C	40 TQFN

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
40 TQFN	T4066MK+5	21-0141	90-0055

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/16	Initial release	—

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