19-1050; Rev 6; 5/12

EVALUATION KIT AVAILABLE

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

General Description

The MAX16046/MAX16048 EEPROM-configurable system managers monitor, sequence, track, and margin multiple system voltages. The MAX16046 manages up to twelve system voltages simultaneously, and the MAX16048 manages up to eight supply voltages. These devices integrate an analog-to-digital converter (ADC) for monitoring supply voltages, digital-to-analog converters (DAC) for adjusting supply voltages, and configurable outputs for sequencing and tracking supplies (during power-up and power-down). Nonvolatile EEPROM registers are configurable for storing upper and lower voltage limits, setting timing and sequencing requirements, and for storing critical fault data for readback following failures.

An internal 1% accurate 10-bit ADC measures each input and compares the result to one upper, one lower, and one selectable upper or lower limit. A fault signal asserts when a monitored voltage falls outside the set limits. Up to three independent fault output signals are configurable to assert under various fault conditions.

The integrated sequencer/tracker allows precise control over the power-up and power-down order of up to twelve (MAX16046) or up to eight (MAX16048) power supplies. Four channels (EN_OUT1–EN_OUT4) support closed-loop tracking using external series MOSFETs. Six outputs (EN_OUT1–EN_OUT6) are configurable with charge-pump outputs to directly drive MOSFETs without closed-loop tracking.

The MAX16046/MAX16048 include twelve/eight integrated 8-bit DAC outputs for margining power supplies when connected to the trim input of a point-of-load (POL) module.

The MAX16046/MAX16048 include six programmable general-purpose inputs/outputs (GPIOs). GPIOs are EEPROM configurable as dedicated fault outputs, as a watchdog input or output (WDI/WDO), as a manual reset ($\overline{MR}$), or as margin control inputs.

The MAX16046/MAX16048 feature two methods of fault management for recording information during system shutdown events. The fault logger records a failure in the internal EEPROM and sets a lock bit protecting the stored fault data from accidental erasure.

An I^2C or a JTAG serial interface configures the MAX16046/MAX16048. These devices are offered in a 56-pin 8mm x 8mm TQFN package or a 64-pin 10mm x 10mm TQFP package and are fully specified from -40°C to +85°C.

Features

- **Operates from 3V to 14V**
- **1% Accurate 10-Bit ADC Monitors 12/8 Inputs**
- **12/8 Monitored Inputs with 1 Overvoltage/ 1 Undervoltage/1 Selectable Limit**
- **12/8 8-Bit DAC Outputs for Margining or Voltage Adjustments**
- **Nonvolatile Fault Event Logger**
- **Power-Up and Power-Down Sequencing Capability**
- **12/8 Outputs for Sequencing/Power-Good Indicators**
- **Closed-Loop Tracking for Up to Four Channels**
- **Two Programmable Fault Outputs and One Reset Output**
- **Six General-Purpose Input/Outputs Configurable as:**
  - **Dedicated Fault Output**
  - **Watchdog Timer Function**
  - **Manual Reset**
  - **Margin Enable Input**
- **I^2C (with Timeout) and JTAG Interface**
- **EEPROM-Configurable Time Delays, Thresholds, and DAC Outputs**
- **100 Bytes of Internal User EEPROM**
- **-40°C to +85°C Operating Temperature Range**

Applications

Servers

Workstations

Storage Systems

Networking/Telecom

Ordering Information

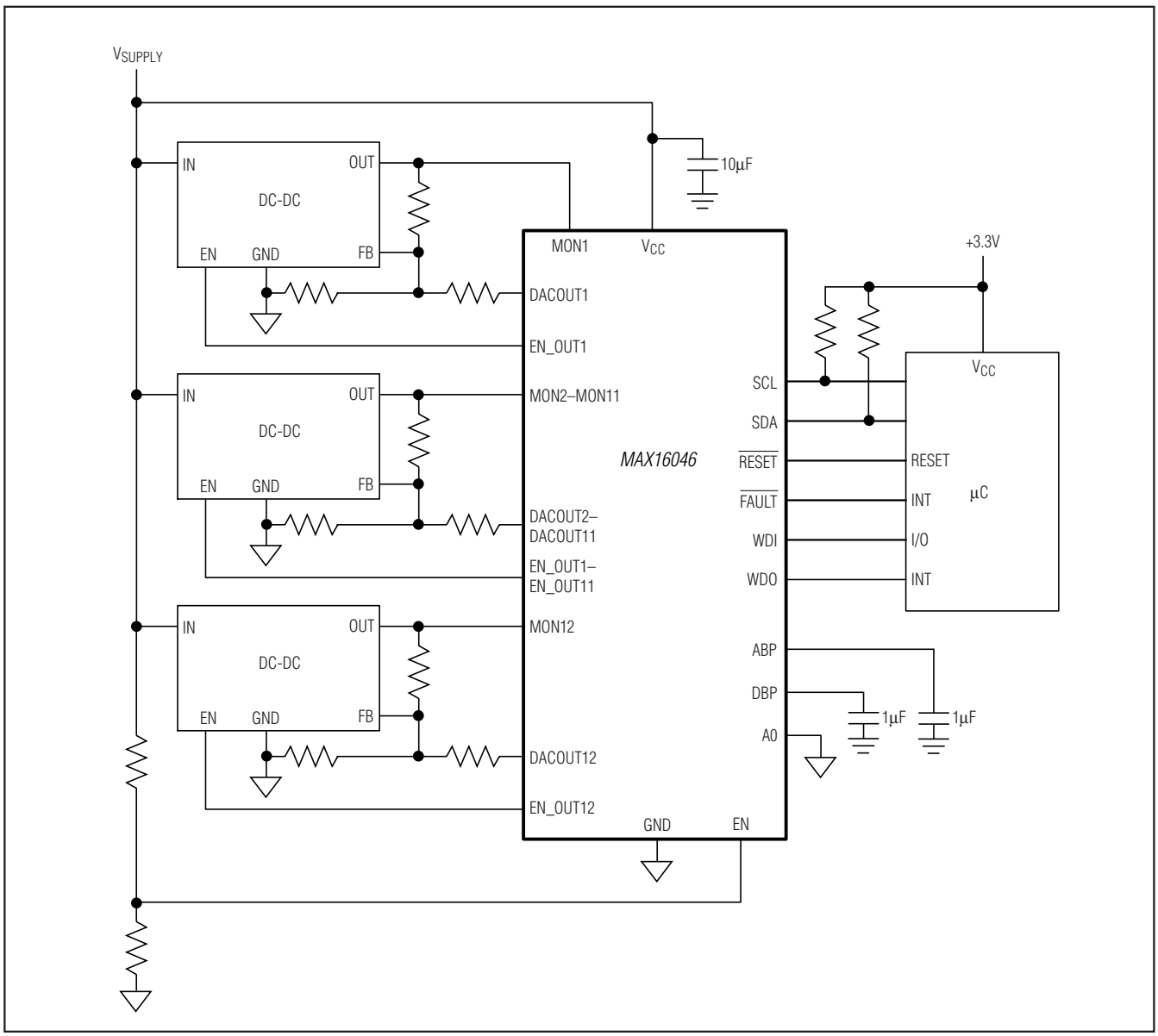
PART	TEMP RANGE	PIN-PACKAGE
MAX16046ECB+	-40°C to +85°C	64 TQFP-EP*
MAX16046ETN+	-40°C to +85°C	56 TQFN-EP*
MAX16048ECB+	-40°C to +85°C	64 TQFP-EP*
MAX16048ETN+	-40°C to +85°C	56 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configurations appear at end of data sheet.

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Typical Operating Circuit



Selector Guide

PART	VOLTAGE-DETECTOR INPUTS	DAC OUTPUTS	GENERAL-PURPOSE INPUTS/OUTPUTS	SEQUENCING OUTPUTS
MAX16046	12	12	6	12
MAX16048	8	8	6	8

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +15V
EN, MON_, SCL, SDA, A0 to GND .....-0.3V to +6V
GPIO_, $\overline{RESET}$ (configured as open drain) to GND.....-0.3V to +6V
EN_OUT1–EN_OUT6 (configured as open drain) to GND.....-0.3V to +12V
EN_OUT7–EN_OUT12 (configured as open drain) to GND.....-0.3V to +6V
GPIO_, EN_OUT_, $\overline{RESET}$ (configured as push-pull) to GND .....-0.3V to (V_{DBP} + 0.3V)
DBP, ABP to GND .....-0.3V to the lower of 3V or (V_{CC} + 0.3V)
TCK, TMS, TDI to GND.....-0.3V to +3.6V
TDO to GND .....-0.3V to (V_{DBP} + 0.3V)
DACOUT_ to GND.....-0.3V to (V_{ABP} + 0.3V)
EN_OUT1–EN_OUT6 (configured as charge pump) to GND ....-0.3V to ($V_{MON1–6}$ + 6V)
Continuous Current (all pins).....±20mA
TQFN (derate 47.6mW/°C above +70°C) 3810mW
TQFP (derate 43.5mW/°C above +70°C).....3478.3mW
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

56 TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....21°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....1°C/W

64 TQFP
Junction-to-Ambient Thermal Resistance (θ_{JA}).....23°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	$\overline{RESET}$ output asserted low	1.4			V
			3		14	
Undervoltage Lockout	V_{UVLO}				2.85	V
Undervoltage-Lockout Hysteresis	$UVLO_{HYS}$	(Note 3)		50		mV
Supply Current	I_{CC}	V_{CC} = 14V, V_{EN} = 3.3V, no load on any output		4.8	6.5	mA
DBP Regulator Voltage	V_{DBP}	C_{DBP} = 1µF, no load on any output	2.6	2.7	2.8	V
ABP Regulator Voltage	V_{ABP}	C_{ABP} = 1µF, no load on any DACOUT_	2.78	2.88	2.96	V
Boot Time	t_{BOOT}	V_{CC} > V_{UVLO}		0.8	1.5	ms
Internal Timing Accuracy		(Note 4)	-5		+5	%
ADC						
ADC Resolution				10		Bits
ADC Total Unadjusted Error (Note 5)	ADC_{ERR}	MON_ range set to '00' in r0Fh–r11h			0.65	%FSR
		MON_ range set to '01' in r0Fh–r11h			0.75	
		MON_ range set to '10' in r0Fh–r11h			0.95	
ADC Integral Nonlinearity	ADC_{INL}				0.8	LSB
ADC Differential Nonlinearity	ADC_{DNL}				0.8	LSB
ADC Total Monitoring Cycle Time	t_{CYCLE}	MAX16046, all channels monitored, no MON_ fault detected (Note 6)		80	100	µs
MON_ Input Impedance	R_{IN}	MON1–MON4	46		100	kΩ
		MON5–MON12	65		140	
ADC MON_ Ranges	ADC_{RNG}	MON_ range set to '00' in r0Fh–r11h		5.6		V
		MON_ range set to '01' in r0Fh–r11h		2.8		
		MON_ range set to '10' in r0Fh–r11h		1.4		

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC LSB Step Size	ADC_{LSB}	MON_ range set to '00' in r0Fh–r11h		5.46		mV
		MON_ range set to '01' in r0Fh–r11h		2.73		
		MON_ range set to '10' in r0Fh–r11h		1.36		
EN Input-Voltage Threshold	$V_{TH\_EN\_R}$	EN voltage rising		0.525		V
	$V_{TH\_EN\_F}$	EN voltage falling	0.487	0.500	0.512	
EN Input Current	I_{EN}		-0.5		+0.5	µA
EN Input Voltage Range			0		5.5	V
CLOSED-LOOP TRACKING						
Tracking Differential Voltage Stop Ramp	V_{TRK}	$V_{INS\_} > V_{TH\_PL}$, $V_{INS\_} < V_{TH\_PG}$		150		mV
Tracking Differential Voltage Hysteresis				20		$\%V_{TRK}$
Tracking Differential Fault Voltage	V_{TRK_F}	$V_{INS\_} > V_{TH\_PL}$, $V_{INS\_} < V_{TH\_PG}$	285	330	375	mV
Track/Sequence Slew-Rate Rising or Falling	TRK_{SLEW}	Slew-rate register set to '00'	640	800	960	V/s
		Slew-rate register set to '01'	320	400	480	
		Slew-rate register set to '10'	160	200	240	
		Slew-rate register set to '11'	80	100	120	
INS_ Power-Good Threshold	V_{TH_PG}	Power-good register set to '00', $V_{MON\_}$ = 3.5V	94	95	96	$\%V_{MON\_}$
		Power-good register set to '01', $V_{MON\_}$ = 3.5V	91.5	92.5	93.5	
		Power-good register set to '10', $V_{MON\_}$ = 3.5V	89	90	91	
		Power-good register set to '11', $V_{MON\_}$ = 3.5V	86.5	87.5	88.5	
Power-Good Threshold Hysteresis	V_{PG_HYS}			0.5		$\%V_{TH\_PG}$
Power-Low Threshold	V_{TH_PL}	INS_ falling	125	142	160	mV
Power-Low Hysteresis	$V_{TH\_PL\_HYS}$			10		mV
GPIO_ Input Impedance	$GPIO_{INR}$	GPIO_ configured as INS_	75	100	145	kΩ
INS_ to GND Pulldown Impedance when Enabled	INS_{RPD}	$V_{INS\_}$ = 2V		100		Ω
DAC						
DAC Resolution				8		Bits
DAC Output Voltage Range	DAC_{RNG}	DACOUT_ range set to '11'		0.8		V
		DACOUT_ range set to '10'		0.6		
		DACOUT_ range set to '01'		0.4		
DAC LSB Step Size		DACOUT_ range set to '11'		3.137		mV
		DACOUT_ range set to '10'		2.353		
		DACOUT_ range set to '01'		1.568		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DAC Center Code Absolute Accuracy	DAC_{ACC}	I_{DACOUT} = ±50µA, mid code, DACOUT_ range set to '11'	T_A = +25°C	1.1960	1.2016	1.2060	V
			T_A = -40°C to +85°C	1.1900	1.2016	1.2130	
		I_{DACOUT} = ±50µA, mid code, DACOUT_ range set to '10'	T_A = +25°C	0.897	0.901	0.905	
			T_A = -40°C to +85°C	0.890	0.901	0.912	
		I_{DACOUT} = ±50µA, mid code, DACOUT_ range set to '01'	T_A = +25°C	0.597	0.601	0.605	
			T_A = -40°C to +85°C	0.592	0.601	0.612	
Gain Error		Any range		-0.8		+0.8	%
DAC Output Sink Capability	DAC_{SINK}	Sinking current, $I_{DACOUTMAX}$ = 0.5mA				+8	mV
DAC Output Source Capability	DAC_{SOURCE}	Sourcing current, $I_{DACOUTMAX}$ = -0.5mA		-8			mV
DAC Output Switch Leakage		DACOUT_ switch off		-150		+150	nA
DAC Output Capacitive Load		(Note 6)				50	pF
DAC Output Settling Time					50		µs
DAC Power-Supply Rejection Ratio	DAC_{PSRR}	DC			60		dB
		100mV step in 20ns with 50pF load			40		
DAC Differential Nonlinearity	DAC_{DNL}	DACOUT_ code from 07h to F8h, any range		-0.6		+0.6	LSB
DAC Integral Nonlinearity	DAC_{INL}	DACOUT_ code from 07h to F8h, any range		-0.9		+0.9	LSB
OUTPUTS (EN_OUT_, $\overline{RESET}$, GPIO_)							
Output-Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
Output-Voltage High (Push-Pull)		I_{SOURCE} =100µA		2.4			V
Output Leakage (Open Drain)	I_{OUT_LKG}					1	µA
		GPIO1–GPIO4, $V_{GPIO\_}$ = 3.3V			1		
		GPIO1–GPIO4, $V_{GPIO\_}$ = 5.0V				22	
EN_OUT_ Overdrive (Charge Pump) (EN_OUT1 to EN_OUT6 Only) Volts above $V_{MON\_}$	V_{OV}	$I_{GATE\_}$ = 0.5µA		4.6	5.1	5.6	V
EN_OUT_ Pullup Current (Charge Pump)	I_{CHG_UP}	During power-up/power-down, $V_{GATE\_}$ = 1V		4.5	6		µA
EN_OUT_ Pulldown Current (Charge Pump)	I_{CHG_DOWN}	During power-up/power-down, $V_{GATE\_}$ = 5V			10		µA
INPUTS (A0, GPIO_)							
Logic-Input Low Voltage	V_{IL}					0.8	V
Logic-Input High Voltage	V_{IH}			2.0			V
SMBus INTERFACE							
Logic-Input Low Voltage	V_{IL}	Input voltage falling				0.8	V
Logic-Input High Voltage	V_{IH}	Input voltage rising		2.0			V

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current		V_{CC} shorted to GND, SCL/SDA at 0V or 3.3V	-1		+1	µA
			-1		+1	
Output-Voltage Low	V_{OL}	I_{SINK} = 3mA			0.4	V
Input Capacitance	C_{IN}			5		pF
SMBus TIMING						
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Condition Setup Time	$t_{SU:STA}$		0.6			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU:DAT}$		200			ns
Output Fall Time	t_{OF}	10pF ≤ C_{BUS} ≤ 400pF			250	ns
Data Hold Time	$t_{HD:DAT}$	Receive	0			µs
		Transmit	0.3		0.9	
Pulse Width of Spike Suppressed	t_{SP}			30		ns
JTAG INTERFACE						
TDI, TMS, TCK Logic-Low Input Voltage	V_{IL}	Input voltage falling			0.55	V
TDI, TMS, TCK Logic-High Input Voltage	V_{IH}	Input voltage rising	2			V
TDO Logic-Output Low Voltage	V_{OL_TDO}	V_{DBP} ≥ 2.5V, I_{SINK} = 2mA			0.4	V
TDO Logic-Output High Voltage	V_{OH_TDO}	V_{DBP} ≥ 2.5V, I_{SOURCE} = 200mA	2.4			V
TDO Leakage Current		TDO high impedance	-1		+1	µA
TDI, TMS Pullup Resistors	R_{JPU}	Pullup to V_{DBP}	7	10	13	kΩ
Input/Output Capacitance	$C_{I/O}$			5		pF
JTAG TIMING						
TCK Clock Period	t_1				1000	ns
TCK High/Low Time	t_2, t_3		50	500		ns
TCK to TMS, TDI Setup Time	t_4		15			ns
TCK to TMS, TDI Hold Time	t_5		15			ns
TCK to TDO Delay	t_6				500	ns
TCK to TDO High-Impedance Delay	t_7				500	ns
EEPROM TIMING						
EEPROM Byte Write Cycle Time	t_{WR}	(Note 7)		10.5	12	ms

Note 2: Specifications are guaranteed for the stated global conditions, unless otherwise noted. 100% production tested at T_A = +25°C and T_A = +85°C. Specifications at T_A = -40°C are guaranteed by design.
Note 3: V_{UVLO} is the minimum voltage on V_{CC} to ensure the device is EEPROM configured.
Note 4: Applies to $\overline{RESET}$, fault, delay, and watchdog timeouts.
Note 5: Total unadjusted error is a combination of gain, offset, and quantization error.
Note 6: Guaranteed by design.
Note 7: An additional cycle is required when writing to configuration memory for the first time.

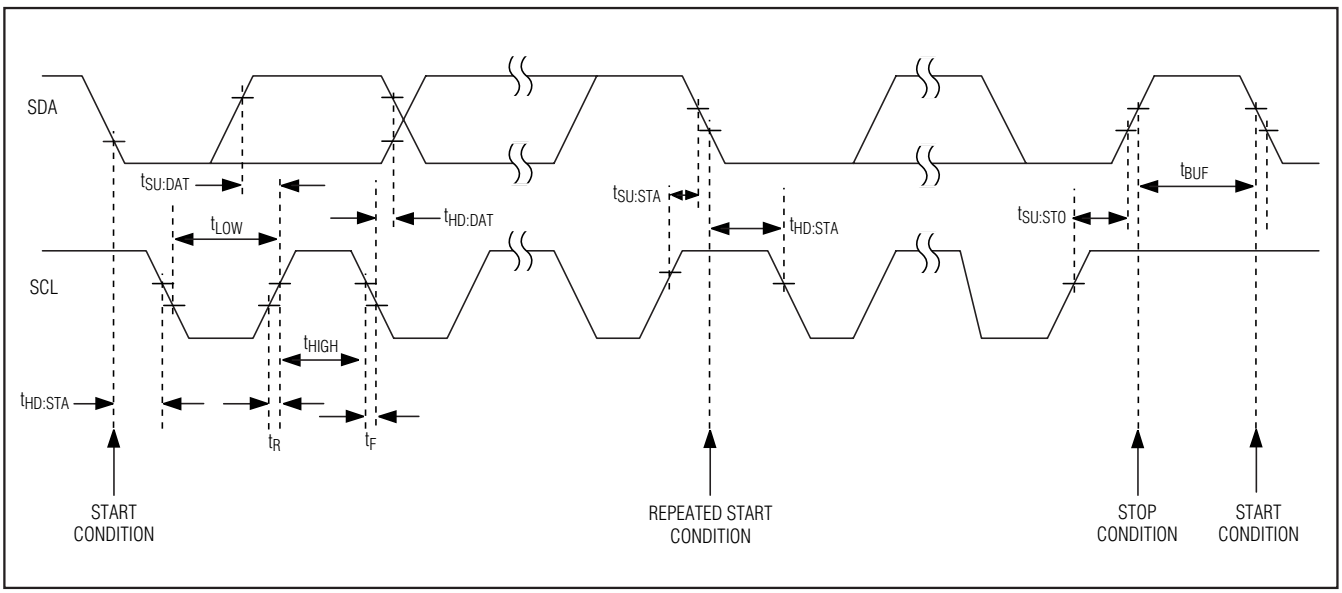


Figure 1. I²C/SMBus Timing Diagram

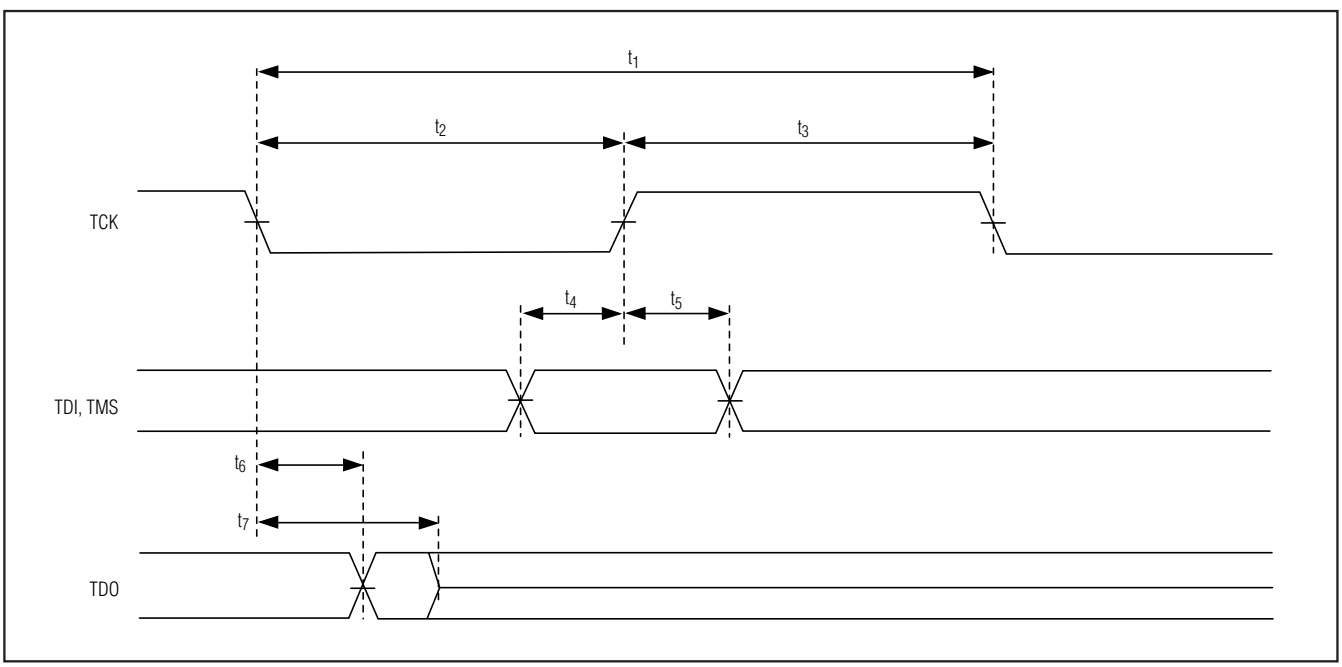


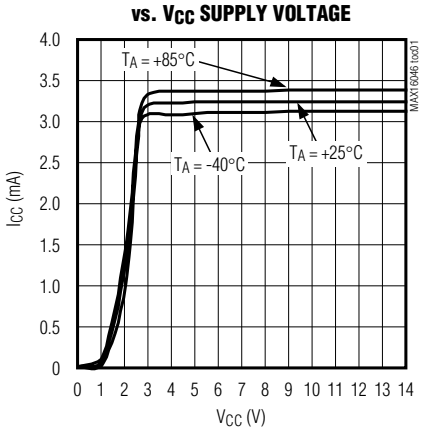
Figure 2. JTAG Timing Diagram

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

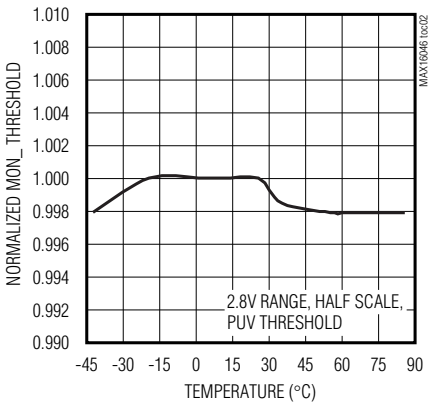
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

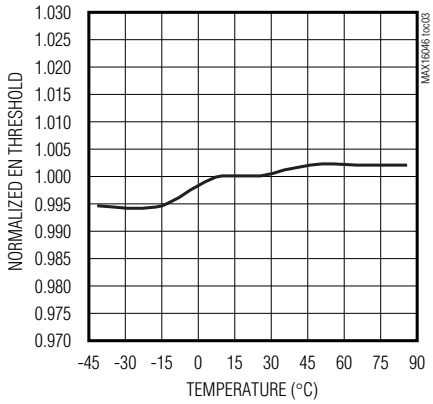
V_{CC} SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE



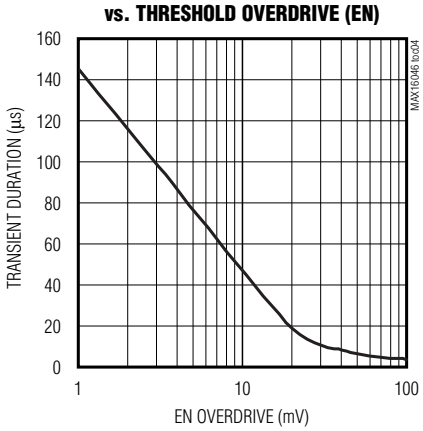
NORMALIZED MON_ THRESHOLD vs. TEMPERATURE



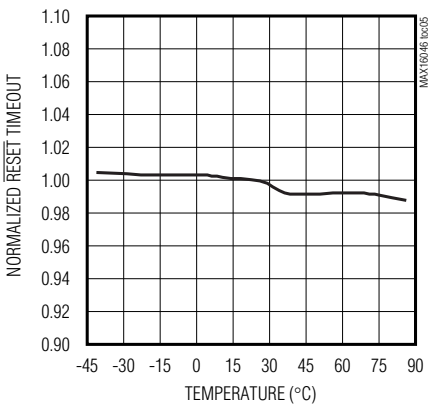
NORMALIZED EN THRESHOLD vs. TEMPERATURE



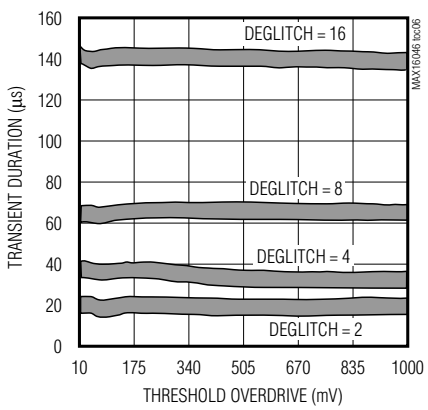
TRANSIENT DURATION vs. THRESHOLD OVERDRIVE (EN)



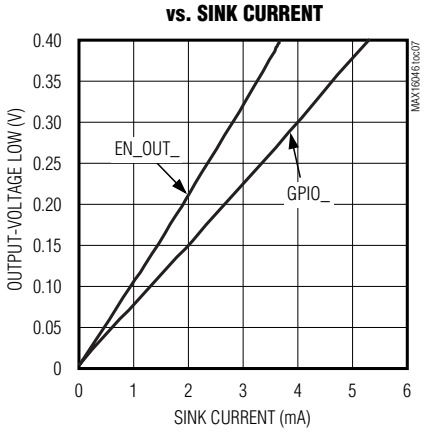
NORMALIZED $\overline{RESET}$ TIMEOUT PERIOD vs. TEMPERATURE



MON_ PUV THRESHOLD OVERDRIVE vs. TRANSIENT DURATION



OUTPUT-VOLTAGE LOW vs. SINK CURRENT

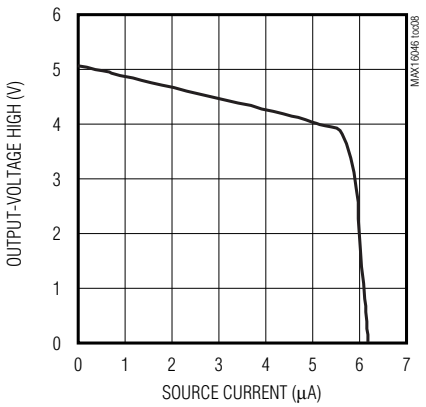


12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

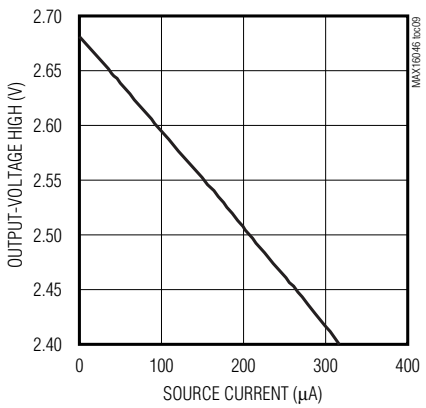
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

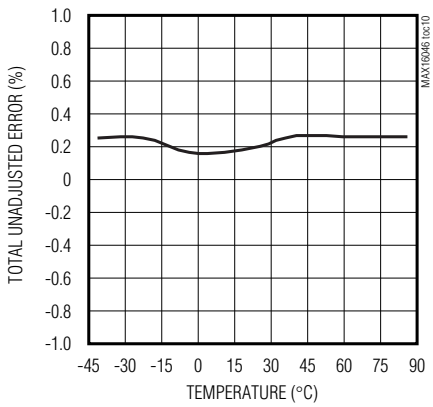
OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT (CHARGE-PUMP OUTPUT)



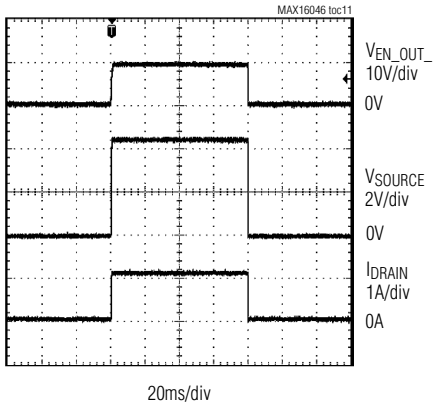
OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT (PUSH-PULL OUTPUT)



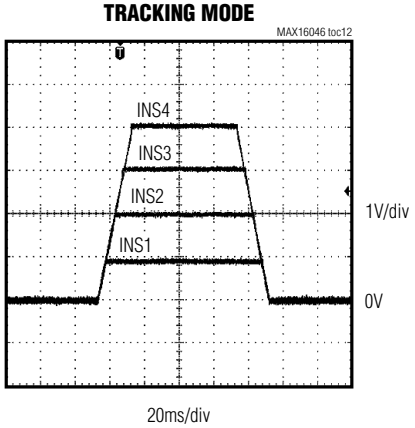
ADC ACCURACY vs. TEMPERATURE



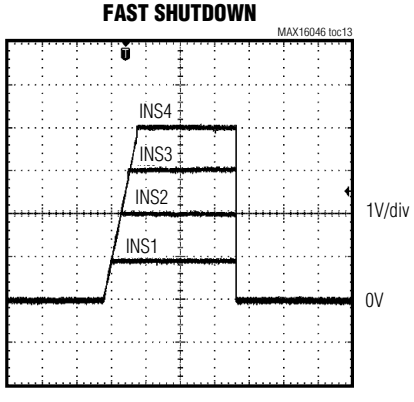
FET TURN-ON WITH CHARGE PUMP



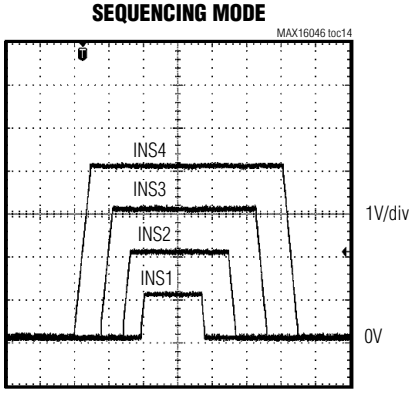
TRACKING MODE



TRACKING MODE WITH FAST SHUTDOWN



SEQUENCING MODE

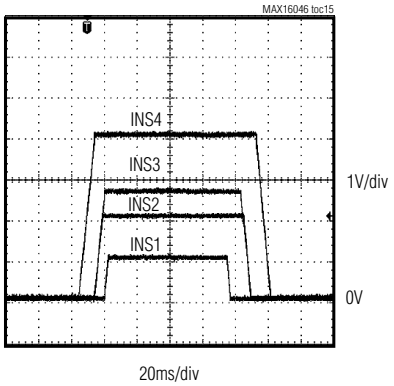


12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

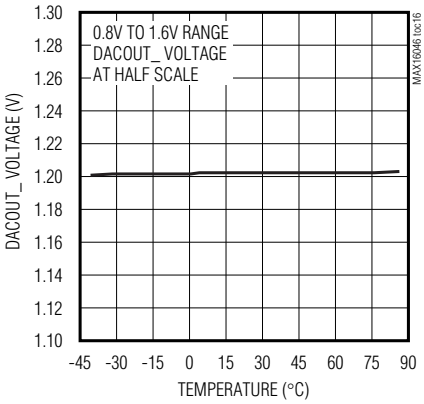
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

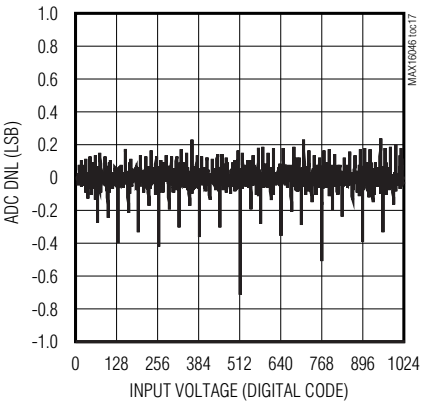
MIXED MODE



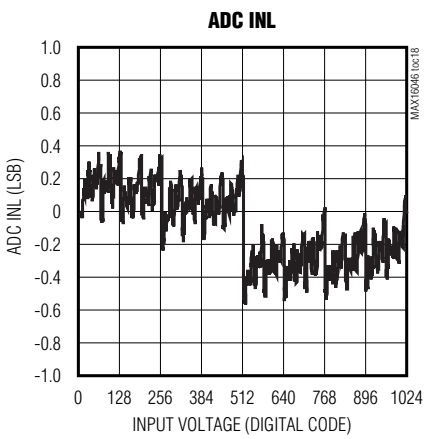
DACOUT_ VOLTAGE vs. TEMPERATURE



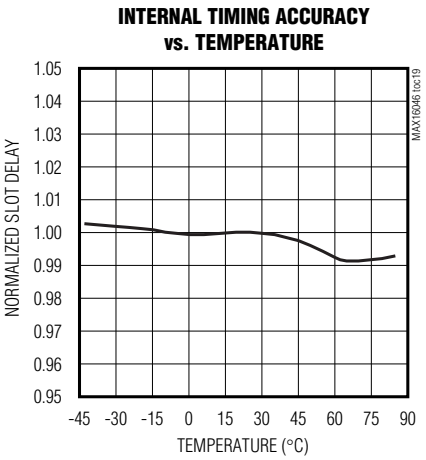
ADC DNL



ADC INL



INTERNAL TIMING ACCURACY vs. TEMPERATURE



12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Pin Descriptions

PIN		NAME	FUNCTION
THIN QFN			
MAX16046	MAX16048		
1–8	1–8	MON1–MON8	ADC Monitored Voltage Inputs. Set ADC input range for each MON_ through configuration registers. Measured values are written to ADC registers and can be read back through the I^2C or JTAG interface.
9–12	—	MON9–MON12	ADC Monitored Voltage Inputs. Set ADC input range through configuration registers. Measured values are written to ADC registers and can be read back through the I^2C or JTAG interface.
—	9–12, 33–36, 53–56	N.C.	No Connection. Must be left unconnected.
13	13	$\overline{\text{RESET}}$	Configurable Reset Output
14	14	A0	Four-State SMBus Address. Address sampled upon POR. Connect A0 to ground, DBP, SCL, or SDA to program an individual address when connecting multiple devices. See the *I^2C/SMBus-Compatible Serial Interface* section.
15	15	SCL	SMBus Serial Clock Input
16	16	SDA	SMBus Serial Data Open-Drain Input/Output
17	17	TMS	JTAG Test Mode Select
18	18	TDI	JTAG Test Data In
19	19	TCK	JTAG Test Clock
20	20	TDO	JTAG Test Data Out
21, 40	21, 40	GND	Ground. Connect all GND connections together.
22	22	GPIO6	General-Purpose Input/Output. GPIO6 and GPIO5 are configurable as open-drain or push-pull outputs, dedicated fault outputs, or for watchdog functionality. GPIO5 is configurable as a watchdog input (WDI). GPIO6 is configurable as a watchdog output (WDO). These inputs/outputs are also configurable for margining. Use the EEPROM to configure GPIO5 and GPIO6. See the *General-Purpose Inputs/Outputs* section.
23	23	GPIO5	
24	24	EN	Analog Enable Input. Apply a voltage greater than the 0.525V (typ) threshold to enable all outputs. The power-down sequence is triggered when EN falls below 0.5V (typ) and all outputs are deasserted.
25–32	25–32	DACOUT1–DACOUT8	DAC Outputs. DACOUT1–DACOUT8 are the outputs of an internal 8-bit DAC. Set DACOUT1–DACOUT8 ranges through configuration registers. Connect a DACOUT_ to an external DC-DC converter for margining. Leave DACOUT_ outputs unconnected, if unused.
33–36	—	DACOUT9–DACOUT12	DAC Outputs. DACOUT9–DACOUT12 are the outputs of an internal 8-bit DAC. Set DACOUT9–DACOUT12 ranges through configuration registers. Connect a DACOUT_ to an external DC-DC converter for margining. Leave DACOUT_ outputs unconnected, if unused.

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Pin Descriptions (continued)

PIN		NAME	FUNCTION
THIN QFN			
MAX16046	MAX16048		
37	37	ABP	Internal Analog Voltage Bypass. Bypass ABP to GND with a 1µF ceramic capacitor. ABP powers the internal circuitry of the MAX16046/MAX16048. Do not use ABP to power any external circuitry.
38	38	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with a 10µF ceramic capacitor.
39	39	DBP	Internal Digital Voltage Bypass. Bypass DBP to GND with a 1µF ceramic capacitor. DBP supplies power to the EEPROM memory, to the internal logic circuitry, and to the internal charge pumps when the programmable outputs are configured as charge pumps. All push-pull outputs are referenced to DBP. Do not use DBP to power any external circuitry.
41	41	GPIO1	General-Purpose Input/Output 1. Configure GPIO1 as a logic input, a return sense line for closed-loop tracking, an open-drain/push-pull fault output, or an open-drain/push-pull output port. Use the EEPROM to configure GPIO1. See the *General-Purpose Inputs/Outputs* section.
42	42	GPIO2	General-Purpose Input/Output 2. GPIO2 is configurable as a logic input, a return sense line for closed-loop tracking, an open-drain/push-pull fault output, or an open-drain/push-pull output port. GPIO2 is also configurable as a dedicated $\overline{\text{MARGINUP}}$ input. Use the EEPROM to configure GPIO2. See the *General-Purpose Inputs/Outputs* section.
43	43	GPIO3	General-Purpose Input/Output 3. GPIO3 is configurable as a logic input, a return sense line for closed-loop tracking, an open-drain/push-pull fault output, or an open-drain/push-pull output port. GPIO3 is also configurable as a dedicated $\overline{\text{MARGINDN}}$ input. Use the EEPROM to configure GPIO3. See the *General-Purpose Inputs/Outputs* section.
44	44	GPIO4	General-Purpose Input/Output 4. GPIO4 is configurable as a logic input, a return sense line for closed-loop tracking, an open-drain/push-pull fault output, or an open-drain/push-pull output port. GPIO4 is also configurable as an active-low manual reset, $\overline{\text{MR}}$. Use the EEPROM to configure GPIO4. See the *General-Purpose Inputs/Outputs* section.
45–50	45–50	EN_OUT1–EN_OUT6	Output. EN_OUT1–EN_OUT6 are configurable with active-high/active-low logic and with an open-drain or push-pull configuration. Program the EEPROM to configure EN_OUT1–EN_OUT6 as a charge-pump output 5V greater than the monitored input voltage ($V_{MON\_}$ + 5V). EN_OUT1–EN_OUT4 can also be used for closed-loop tracking.
51, 52	51, 52	EN_OUT7–EN_OUT8	Output. Configure EN_OUT_ with active-low/active-high logic and with an open-drain or push-pull configuration.
53–56	—	EN_OUT9–EN_OUT12	Output. Configure EN_OUT_ with active-low/active-high logic and with an open-drain or push-pull configuration.
—	—	EP	Exposed Pad. Internally connected to GND. Connect to GND. EP also functions as a heatsink to maximize thermal dissipation. Do not use as the main ground connection.

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Pin Descriptions (continued)

PIN		NAME	FUNCTION
TQFP			
MAX16046	MAX16048		
1–7, 10	1–7, 10	MON1–MON8	ADC Monitored Voltage Inputs. Set ADC input range for each IN_ through configuration registers. Measured values are written to ADC registers and can be read back through the I^2C or JTAG interface.
11–14	—	MON9–MON12	ADC Monitored Voltage Inputs. Set ADC input range through configuration registers. Measured values are written to ADC registers and can be read back through the I^2C or JTAG interface.
8, 9, 15, 25, 33, 48, 49, 64	8, 9, 11–15, 25, 33, 38–41, 48, 49, 60–64	N.C.	No Connection. Must leave unconnected.
16	16	$\overline{\text{RESET}}$	Configurable Reset Output
17	17	A0	Four-State SMBus Address. Address sampled upon POR. Connect A0 to ground, DBP, SCL, or SDA to program an individual address when connecting multiple devices. See the *I^2C/SMBus-Compatible Serial Interface* section.
18	18	SCL	SMBus Serial Clock Input
19	19	SDA	SMBus Serial Data Open-Drain Input/Output
20	20	TMS	JTAG Test Mode Select
21	21	TDI	JTAG Test Data In
22	22	TCK	JTAG Test Clock
23	23	TDO	JTAG Test Data Out
24, 45	24, 45	GND	Ground
26, 27	26, 27	GPIO6, GPIO5	General-Purpose Input/Output. GPIO6 and GPIO5 are configurable as open-drain or push-pull outputs, dedicated fault outputs, or for watchdog functionality. GPIO5 is configurable as a watchdog input (WDI). GPIO6 is configurable as a watchdog output (WDO). These inputs/outputs are also configurable for margining. Use the EEPROM to GPIO5 and GPIO6. See the *General-Purpose Inputs/Outputs* section.
28	28	EN	Analog Enable Input. Apply a voltage greater than the 0.525V (typ) threshold to enable all outputs. Power-down sequence triggered when EN falls below 0.5V (typ) and all outputs are deasserted.
29–32, 34–37	29–32, 34–37	DACOUT1–DACOUT8	DAC Outputs. DACOUT1–DACOUT8 are the outputs of an internal 8-bit DAC. Set DACOUT_ ranges through configuration registers. Connect a DACOUT_ to an external DC-DC converter for margining. Leave DACOUT_ outputs unconnected, if unused.
38–41	—	DACOUT9–DACOUT12	DAC Outputs. DACOUT9–DACOUT12 are the outputs of an internal 8-bit DAC. Set DACOUT_ ranges range through configuration registers. Connect a DACOUT_ to an external DC-DC converter for margining. Leave DACOUT_ outputs unconnected, if unused.

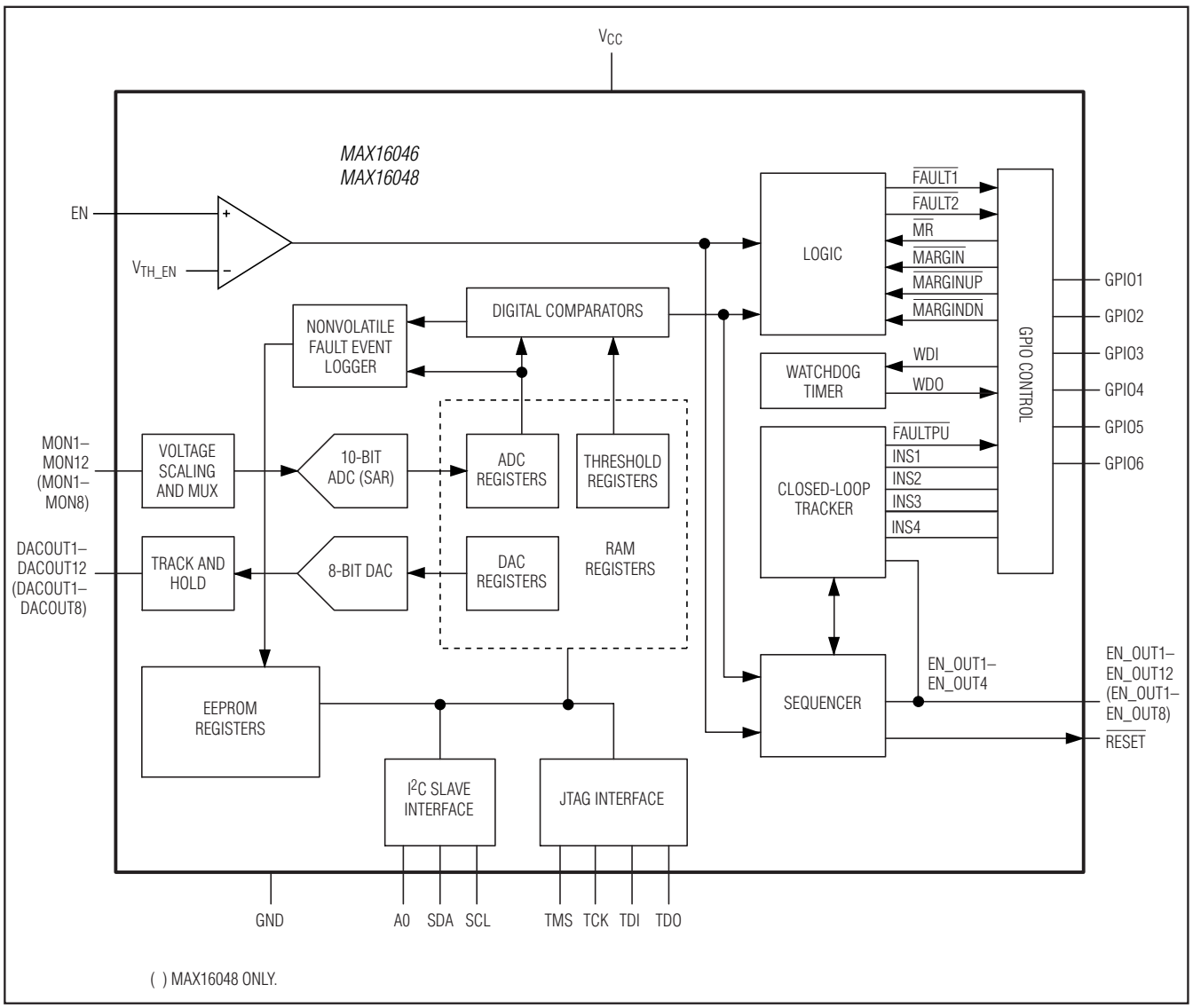
12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Pin Descriptions (continued)

PIN		NAME	FUNCTION
TQFP			
MAX16046	MAX16048		
42	42	ABP	Internal Analog Voltage Regulator Output. Bypass ABP to GND with a 1µF ceramic capacitor. ABP powers the internal circuitry of the MAX16046/MAX16048 and supplies power to the internal charge pumps when the programmable outputs are configured as charge pumps. Do not use ABP to power any external circuitry.
43	43	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with a 10µF ceramic capacitor.
44	44	DBP	Internal Digital Voltage Regulator Output. Bypass DBP to GND with a 1µF ceramic capacitor. DBP supplies power to the EEPROM memory and the internal logic circuitry. All push-pull outputs are referenced to DBP. Do not use DBP to power any external circuitry.
46	46	GPIO1	General-Purpose Input/Output 1. Configure GPIO1 as a TTL input, a return sense line for closed-loop tracking, an open-drain/push-pull fault output, or an open-drain/push-pull output port. Use the EEPROM to configure GPIO1. See the *General-Purpose Inputs/Outputs* section.
47	47	GPIO2	General-Purpose Input/Output 2. GPIO2 is configurable as a TTL input, a return sense line for closed-loop tracking, an open-drain/push-pull fault output, or an open-drain/push-pull output port. GPIO2 is also configurable as a dedicated $\overline{\text{MARGINUP}}$ input. Use the EEPROM to configure GPIO2. See the *General-Purpose Inputs/Outputs* section.
50	50	GPIO3	General-Purpose Input/Output 3. GPIO3 is configurable as a TTL input, a return sense line for closed-loop tracking, an open-drain/push-pull fault output, or an open-drain/push-pull output port. GPIO3 is also configurable as a dedicated $\overline{\text{MARGINDN}}$ input. Use the EEPROM to configure GPIO3. See the *General-Purpose Inputs/Outputs* section.
51	51	GPIO4	General-Purpose Input/Output 4. GPIO4 is configurable as a TTL input, a return sense line for closed loop tracking, an open-drain/push-pull fault output, or an open-drain/push-pull output port. GPIO4 is also configurable as an active-low manual reset, $\overline{\text{MR}}$. Use the EEPROM to configure GPIO4. See the *General-Purpose Inputs/Outputs* section.
52–57	52–57	EN_OUT1–EN_OUT6	Output. EN_OUT1–EN_OUT6 are configurable with active-high/active-low logic and with open-drain or push-pull configurations. Program the EEPROM to configure EN_OUT_ with a charge-pump output 5V greater than the monitored input voltage ($V_{IN\_}$ + 5V). EN_OUT1–EN_OUT4 can also be used for closed-loop tracking.
58, 59	58, 59	EN_OUT7, EN_OUT8	Output. Configure EN_OUT_ with active-low/active-high logic and with an open-drain or push-pull configuration.
60–63	—	EN_OUT9–EN_OUT12	Output. Configure EN_OUT_ with active-low/active-high logic and with an open-drain or push-pull configuration.
—	—	EP	Exposed Pad. Internally connected to GND. Connect to GND. EP also functions as a heatsink to maximize thermal dissipation. Do not use as the main ground connection.

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Functional Diagram



12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Register Summary (All Registers 8-Bits Wide)

Note: *This data sheet uses a specific convention for referring to bits within a particular address location. As an example, r0Fh[3:0] refers to bit 3 to bit 0 in register with address 15 decimal.*

PAGE	REGISTER	DESCRIPTION
Extended	ADC Conversion Results (Registers r00h to r17h)	Input ADC conversion results. ADC writes directly to these registers during normal operation. ADC input ranges (MON1–MON12) are selected with registers r0Fh to r11h.
	Failed Line Flags (Registers r18h to r19h)	Voltage fault flag bits. Flags for each input signal when undervoltage or overvoltage threshold is exceeded.
	GPIO Data (Registers r1Ah to r1Bh)	GPIO state data. Used to read back and control the state of each GPIO.
	DAC Enables (Registers r1Ch to r1Dh)	DAC output control. Controls whether DAC outputs are high impedance or connected to the DAC.
Default	DAC Registers (Registers r00h to r0Bh)	DAC code registers. Sets the output voltage of each DAC output.
Default and EEPROM	ADC Range Selections (Registers r0Fh to r11h)	ADC input voltage range. Selects the voltage range of the monitored inputs.
	DAC Range (Registers r12h to r14h)	DAC range registers. Sets the voltage output range of each DAC output.
	$\overline{\text{RESET}}$ and Fault Outputs (Registers r15h to r1Bh)	$\overline{\text{RESET}}$ and $\overline{\text{FAULT1}}$–$\overline{\text{FAULT2}}$ output configuration. Programs the functionality of the $\overline{\text{RESET}}$, $\overline{\text{FAULT1}}$, and $\overline{\text{FAULT2}}$ outputs, as well as which inputs they depend on.
	GPIO Configuration (Registers r1Ch to r1Eh)	General-purpose input/output configuration registers. GPIOs are configurable as a manual-reset input, a margin disable input, margin-up/margin-down control inputs, a watchdog timer input and output, logic inputs/outputs, fault-dependent outputs, or as the feedback/pulldown inputs (INS_) for closed-loop tracking.
	Programmable Output Configuration (Registers r1Fh to r22h)	Programmable output configurations. Selectable output configurations include: active-low or active-high, open-drain or push-pull outputs. EN_OUT1–EN_OUT6 are configurable as charge-pump outputs, and EN_OUT1–EN_OUT4 can be configured for closed-loop tracking.
	Overvoltage and Undervoltage Thresholds (Registers r23h to r46h)	Input overvoltage and undervoltage thresholds. ADC conversion results are compared to overvoltage and undervoltage threshold values stored here. MON_ voltages exceeding threshold values trigger a fault event.
	Fault Behavior (Registers r47h to r4Ch)	Selects how the device should operate during faults. Options include latch-off or autoretry after fault. The autoretry delay is selectable (r4Fh). Use registers r48h through r4Ch to select fault conditions that trigger a critical fault event.
	$\overline{\text{Software Enable}}$ and Margin (Register r4Dh)	Use register r4Dh to set the $\overline{\text{Software Enable}}$ bit, to select early warning thresholds and undervoltage/overvoltage, to enable/disable margining, and to enable/disable the watchdog for independent/dependent mode.
	Sequencing-Mode Configuration (Registers r50h to r5Bh and r5Eh to r63h)	Assign inputs and outputs for sequencing. Select sequence delays (20µs to 1.6s) with registers r50h through r54h. Use register r54h to enable/disable the reverse sequence bit for power-down operation.
	Watchdog Functionality (Register r55h)	Configure watchdog functionality for GPIO5 and GPIO6.
	DAC Output Margin Levels (Registers r66h to r7Dh)	DAC output levels depend on GPIO2 and GPIO3 when configured for margining functionality. Set registers r66h to r71h for margin up. Set registers r72h to r7Dh for margin down.
EEPROM	Fault Log Results (Registers r00h to r0Eh)	ADC conversion results and failed-line flags at the time of a fault. These values are recorded by the fault event logger at the time of a critical fault.
	User EEPROM (Registers r9Ch to rFFh)	User-available EEPROM

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Detailed Description

Getting Started

The MAX16046 is capable of managing up to twelve system voltages simultaneously, and the MAX16048 can manage up to eight system voltages. After boot-up, if EN is high and the Software Enable bit is set to '0,' an internal multiplexer cycles through each input. At each multiplexer stop, the 10-bit ADC converts the monitored analog voltage to a digital result and stores the result in a register. Each time the multiplexer finishes a conversion (8.3µs max), internal logic circuitry compares the conversion results to the overvoltage and undervoltage thresholds stored in memory. When a conversion violates a programmed threshold, the conversion can be configured to generate a fault. Logic outputs can be programmed to depend on many combinations of faults. Additionally, faults are programmable to trigger the nonvolatile fault logger, which writes all fault information automatically to the EEPROM and write-protects the data to prevent accidental erasure.

The MAX16046/MAX16048 contain both I²C/SMBus and JTAG serial interfaces for accessing registers and EEPROM. Use only one interface at any given time. For more information on how to access the internal memory through these interfaces, see the *I²C/SMBus-Compatible Serial Interface* and *JTAG Serial Interface* sections. Registers are divided into three pages with access controlled by special I²C and JTAG commands.

The factory-default values at POR (power-on reset) for all RAM registers are '0's. POR occurs when V_{CC} reaches the undervoltage-lockout threshold (UVLO) of 2.85V (max). At POR, the device begins a boot-up sequence. During the boot-up sequence, all monitored inputs are masked from initiating faults and EEPROM contents are copied to the respective register locations. During boot-up, the MAX16046/MAX16048 are not accessible through the serial interface. The boot-up sequence can take up to 1.5ms, after which the device is ready for normal operation. $\overline{RESET}$ is low during boot-up and asserts after boot-up for its programmed timeout period once all monitored channels are within their respective thresholds. During boot-up, the GPIOs, DACOUTs, and EN_OUTs are high impedance.

Accessing the EEPROM

The MAX16046/MAX16048 memory is divided into three separate pages. The default page, selected by default at POR, contains configuration bits for all functions of the part. The extended page contains the ADC conversion results, GPIO input and output registers, and DAC enable bits. Finally, the EEPROM page contains all stored configuration information as well as saved fault data and user-defined data. See the *Register Map* table for more information on the function of each register.

During the boot-up sequence, the contents of the EEPROM (r0Fh to r7Dh) are copied into the default page (r0Fh to r7Dh). Registers r00h to r0Bh of the default page contain the DAC output voltage registers and are reset to '0's at POR. Registers r00h to r0Eh of the EEPROM page contain saved fault data.

The JTAG and I²C interfaces provide access to all three pages. Each interface provides commands to select and deselect a particular page:

- 98h(I²C)/09h(JTAG)—Switches to the extended page. Switch back to the default page with 99h(I²C)/0Ah(JTAG).
- 9Ah(I²C)/0Bh(JTAG)—Switches to the EEPROM page. Switch back to the default page with 9Bh(I²C)/0Ch(JTAG).

See the *I²C/SMBus-Compatible Serial Interface* or the *JTAG Serial Interface* section.

Power

Apply 3V to 14V to V_{CC} to power the MAX16046/MAX16048. Bypass V_{CC} to ground with a 10µF capacitor. Two internal voltage regulators, ABP and DBP, supply power to the analog and digital circuitry within the device. Do not use ABP or DBP to power external circuitry.

ABP is a 2.85V (typ) voltage regulator that powers the internal analog circuitry and supplies power to the DAC outputs. Bypass the ABP output to GND with a 1µF ceramic capacitor installed as close to the device as possible.

DBP is an internal 2.7V (typ) voltage regulator. EEPROM and digital circuitry are powered by DBP. All push-pull outputs are referenced to DBP. DBP supplies the input voltage to the internal charge pumps when the programmable outputs are configured as charge-pump outputs. Bypass the DBP output to GND with a 1µF ceramic capacitor installed as close as possible to the device.

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Enable

To initiate sequencing/tracking and enable monitoring, the voltage at EN must be above 0.525V and the Software Enable bit in r4Dh[0] must be set to '0.' To power down and disable monitoring, either pull EN below 0.5V or set the Software Enable bit to '1.' See Table 1 for the software enable bit configurations. Connect EN to ABP if not used.

If a fault condition occurs during the power-up cycle, the EN_OUT_ outputs are powered down immediately, independent of the state of EN. If operating in latch-on fault mode, toggle EN or toggle the Software Enable bit to clear the latch condition and restart the device once the fault condition has been removed.

Table 1. EEPROM Software Enable Configurations

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
4Dh	0	**Software Enable bit** 0 = Enabled. EN must also be high to begin sequencing. 1 = Disabled (factory default)
	1	**Margin bit** 1 = Margin functionality is enabled 0 = Margin disabled
	2	**Early Warning Selection bit** 0 = Early warning thresholds are undervoltage thresholds 1 = Early warning thresholds are overvoltage thresholds
	3	**Watchdog Mode Selection bit** 0 = Watchdog timer is in dependent mode 1 = Watchdog timer is in independent mode
	[7:4]	Not used

Voltage Monitoring

The MAX16046/MAX16048 feature an internal 10-bit ADC that monitors the MON_ voltage inputs. An internal multiplexer cycles through each of the twelve inputs, taking 100µs (typ) for a complete monitoring cycle. Each acquisition takes approximately 8.3µs. At each multiplexer stop, the 10-bit ADC converts the analog input to a digital result and stores the result in a register. ADC conversion results are stored in registers r00h to r17h in the extended page. Use the I^2C or JTAG serial interface to read ADC conversion results. See the *I^2C/SMBus-Compatible Serial Interface* or the *JTAG Serial Interface* section for more information on accessing the extended page.

The MAX16046 provides twelve inputs, MON1–MON12, for voltage monitoring. The MAX16048 provides eight inputs, MON1–MON8, for voltage monitoring. Each input voltage range is programmable in registers r0Fh to r11h (see Table 2). When MON_ configuration registers are set to '11,' MON_ voltages are not monitored or converted, and the multiplexer does not stop at these inputs, decreasing the total cycle time. These inputs cannot be configured to trigger fault conditions.

The three programmable thresholds for each monitored voltage include an overvoltage, an undervoltage, and an early warning threshold that can be set in r4Dh[2] to be either an undervoltage or overvoltage threshold. See the *Faults* section for more information on setting overvoltage and undervoltage thresholds. All voltage thresholds are 8 bits wide. The 8 MSBs of the 10-bit ADC conversion result are compared to these overvoltage and undervoltage thresholds.

For any undervoltage or overvoltage condition to be monitored and any faults detected, the MON_ input must be assigned to a particular sequence order. See the *Sequencing* section for more details on assigning MON_ inputs.

Table 2. Input Monitor Ranges and Enables

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
0Fh	[1:0]	**MON1 Voltage Range Selection:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON1 is not converted or monitored
	[3:2]	**MON2 Voltage Range Selection:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON2 is not converted or monitored
	[5:4]	**MON3 Voltage Range Selection:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON3 is not converted or monitored
	[7:6]	**MON4 Voltage Range Selection:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON4 is not converted or monitored
10h	[1:0]	**MON5 Voltage Range Selection:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON5 is not converted or monitored
	[3:2]	**MON6 Voltage Range Selection:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON6 is not converted or monitored
	[5:4]	**MON7 Voltage Range Selection:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON7 is not converted or monitored
	[7:6]	**MON8 Voltage Range Selection:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON8 is not converted or monitored

Table 2. Input Monitor Ranges and Enables (continued)

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
11h	[1:0]	**MON9 Voltage Range Selection*:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON9 is not converted or monitored
	[3:2]	**MON10 Voltage Range Selection*:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON10 is not converted or monitored
	[5:4]	**MON11 Voltage Range Selection*:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON11 is not converted or monitored
	[7:6]	**MON12 Voltage Range Selection*:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON12 is not converted or monitored

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The extended memory page contains the ADC conversion result registers (see Table 3). These registers are also used internally for fault threshold comparison. Voltage-monitoring thresholds are compared with the 8 MSBs of the conversion results. Inputs that are not enabled are not converted by the ADC; they contain the last value acquired before that channel was disabled.

The ADC conversion result registers are reset to 00h at boot-up. These registers are not reset when a reboot command is executed.

Table 3. ADC Conversion Registers

EXTENDED PAGE ADDRESS	BIT RANGE	DESCRIPTION
00h	[7:0]	MON1 ADC Conversion Result (MSB)
01h	[7:6]	MON1 ADC Conversion Result (LSB)
	[5:0]	Reserved
02h	[7:0]	MON2 ADC Conversion Result (MSB)
03h	[7:6]	MON2 ADC Conversion Result (LSB)
	[5:0]	Reserved
04h	[7:0]	MON3 ADC Conversion Result (MSB)
05h	[7:6]	MON3 ADC Conversion Result (LSB)
	[5:0]	Reserved
06h	[7:0]	MON4 ADC Conversion Result (MSB)
07h	[7:6]	MON4 ADC Conversion Result (LSB)
	[5:0]	Reserved
08h	[7:0]	MON5 ADC Conversion Result (MSB)
09h	[7:6]	MON5 ADC Conversion Result (LSB)
	[5:0]	Reserved
0Ah	[7:0]	MON6 ADC Conversion Result (MSB)
0Bh	[7:6]	MON6 ADC Conversion Result (LSB)
	[5:0]	Reserved
0Ch	[7:0]	MON7 ADC Conversion Result (MSB)
0Dh	[7:6]	MON7 ADC Conversion Result (LSB)
	[5:0]	Reserved
0Eh	[7:0]	MON8 ADC Conversion Result (MSB)
0Fh	[7:6]	MON8 ADC Conversion Result (LSB)
	[5:0]	Reserved
10h	[7:0]	MON9 ADC Conversion Result (MSB)*
11h	[7:6]	MON9 ADC Conversion Result (LSB)*
	[5:0]	Reserved
12h	[7:0]	MON10 ADC Conversion Result (MSB)*
13h	[7:6]	MON10 ADC Conversion Result (LSB)*
	[5:0]	Reserved
14h	[7:0]	MON11 ADC Conversion Result (MSB)*
15h	[7:6]	MON11 ADC Conversion Result (LSB)*
	[5:0]	Reserved
16h	[7:0]	MON12 ADC Conversion Result (MSB)*
17h	[7:6]	MON12 ADC Conversion Result (LSB)*
	[5:0]	Reserved

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12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

General-Purpose Inputs/Outputs

GPIO1–GPIO6 are programmable general-purpose inputs/outputs. GPIO1–GPIO6 are configurable as a manual reset input, a margin disable input, margin-up/margin-down control inputs, a watchdog timer input and output, logic inputs/outputs, fault-dependent outputs, or as the feedback inputs (INS_) for closed-loop tracking. When programmed as outputs, GPIOs are open drain or push-pull. See registers r1Ch to r1Eh in Tables 4 and 5 for more detailed information on configuring GPIO1–GPIO6.

Table 4. General-Purpose IO Configuration Registers

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
1Ch	[2:0]	GPIO1 Configuration Register
	[5:3]	GPIO2 Configuration Register
	[7:6]	GPIO3 Configuration Register (LSB)
1Dh	[0]	GPIO3 Configuration Register (MSB)
	[3:1]	GPIO4 Configuration Register
	[6:4]	GPIO5 Configuration Register
	[7]	GPIO6 Configuration Register (LSB)
1Eh	[1:0]	GPIO6 Configuration Register (MSB)
	[7:2]	Reserved

Table 5. GPIO Mode Selection

CONFIGURATION BITS	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO6
000	INS1	INS2	INS3	INS4	—	$\overline{\text{MARGIN}}$ input
001	Push-pull logic input/output	Push-pull logic input/output	Push-pull logic input/output	Push-pull logic input/output	Push-pull logic input/output	Push-pull logic input/output
010	Open-drain logic input/output	Open-drain logic input/output	Open-drain logic input/output	Open-drain logic input/output	Open-drain logic input/ output	Open-drain logic input/ output
011	Push-pull Any_Fault output	Push-pull Any_Fault output	Push-pull Any_Fault output	Push-pull Any_Fault output	Push-pull $\overline{\text{FAULT1}}$ output	Push-pull $\overline{\text{FAULT2}}$ output
100	Open-drain Any_Fault output	Open-drain Any_Fault output	Open-drain Any_Fault output	Open-drain Any_Fault output	Open-drain $\overline{\text{FAULT1}}$ output	Open-drain $\overline{\text{FAULT2}}$ output
101	Logic input	Logic input	Logic input	Logic input	Logic input	Logic input
110	—	—	—	—	—	Open-drain, WDO output
111	—	$\overline{\text{MARGINUP}}$ input	$\overline{\text{MARGINDN}}$ input	$\overline{\text{MR}}$ input	WDI input	Open-drain, $\overline{\text{FAULTPU}}$ output

Note: *The dash "—" represents a reserved GPIO configuration. Do not set any GPIO to these values.*

Voltage Tracking Sense (INS_) Inputs

GPIO1–GPIO4 are configurable as feedback sense return inputs (INS_) for closed-loop tracking. Connect the gate of an external n-channel MOSFET to each EN_OUT_ configured for closed-loop tracking. Connect INS_ inputs to the source of the MOSFETs for tracking feedback.

Internal comparators monitor INS_ with respect to a control tracking ramp voltage for power-up/power-down and control each EN_OUT_ voltage. Under normal conditions each INS_ voltage tracks the ramp voltage until the power-good voltage threshold has been reached. The slew rate for the ramp voltage and the INS_ to MON_ power-good threshold are programmable. See the *Closed-Loop Tracking* section.

INS_ connections can also act as 100Ω pulldowns for closed-loop tracking channels or for other power supplies, if INS_ are connected to the outputs of the supplies. Set the appropriate bits in r4Eh[7:4] to enable pulldown functionality. See Table 13.

General-Purpose Logic Inputs/Outputs

Configure GPIO1–GPIO6 to be used as general-purpose inputs/outputs. Write values to GPIOs through r1Ah when operating as outputs, and read values from r1Bh when operating as inputs. Register r1Bh is read-only. See Table 6 for more information on reading and writing to the GPIOs as logic inputs/outputs. Both registers r1Ah and r1Bh are located in the extended page and are therefore not loaded from EEPROM on boot-up.

Table 6. GPIO Data-In/Data-Out Data

EXTENDED PAGE ADDRESS	BIT RANGE	DESCRIPTION
1Ah	[0]	**GPIO Logic Output Data** 0 = GPIO1 is a logic-low output 1 = GPIO1 is a logic-high output
	[1]	0 = GPIO2 is a logic-low output 1 = GPIO2 is a logic-high output
	[2]	0 = GPIO3 is a logic-low output 1 = GPIO3 is a logic-high output
	[3]	0 = GPIO4 is a logic-low output 1 = GPIO4 is a logic-high output
	[4]	0 = GPIO5 is a logic-low output 1 = GPIO5 is a logic-high output
	[5]	0 = GPIO6 is a logic-low output 1 = GPIO6 is a logic-high output
	[7:6]	Not used
1Bh	[0]	**GPIO Logic Input Data** GPIO1 logic-input state
	[1]	GPIO2 logic-input state
	[2]	GPIO3 logic-input state
	[3]	GPIO4 logic-input state
	[4]	GPIO5 logic-input state
	[5]	GPIO6 logic-input state
	[7:6]	Not used

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Any_Fault Outputs

GPIO1–GPIO4 are configurable as active-low push-pull or open-drain fault-dependent outputs. These outputs assert when any monitored input exceeds an overvoltage, undervoltage, or early warning threshold.

$\overline{FAULT1}$ and $\overline{FAULT2}$

GPIO5 and GPIO6 are configurable as dedicated fault outputs, $\overline{FAULT1}$ and $\overline{FAULT2}$, respectively. Fault outputs can assert on one or more overvoltage, undervoltage, or early warning conditions for selected inputs. $\overline{FAULT1}$ and $\overline{FAULT2}$ dependencies are set using registers r15h to r18h. See Table 7.

If a fault output depends on more than one MON_, the fault output will assert if one or more MON_ exceeds a programmed threshold voltage.

Table 7. $\overline{FAULT1}$ and $\overline{FAULT2}$ Output Configuration and Dependencies

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
15h	[0]	1 = $\overline{FAULT1}$ is a digital output dependent on MON1
	[1]	1 = $\overline{FAULT1}$ is a digital output dependent on MON2
	[2]	1 = $\overline{FAULT1}$ is a digital output dependent on MON3
	[3]	1 = $\overline{FAULT1}$ is a digital output dependent on MON4
	[4]	1 = $\overline{FAULT1}$ is a digital output dependent on MON5
	[5]	1 = $\overline{FAULT1}$ is a digital output dependent on MON6
	[6]	1 = $\overline{FAULT1}$ is a digital output dependent on MON7
	[7]	1 = $\overline{FAULT1}$ is a digital output dependent on MON8
16h	[0]	1 = $\overline{FAULT1}$ is a digital output dependent on MON9*
	[1]	1 = $\overline{FAULT1}$ is a digital output dependent on MON10*
	[2]	1 = $\overline{FAULT1}$ is a digital output dependent on MON11*
	[3]	1 = $\overline{FAULT1}$ is a digital output dependent on MON12*
	[4]	1 = $\overline{FAULT1}$ is a digital output that depends on the overvoltage thresholds at the input selected by r15h and r16h[3:0]
	[5]	1 = $\overline{FAULT1}$ is a digital output that depends on the undervoltage thresholds at the input selected by r15h and r16h[3:0]
	[6]	1 = $\overline{FAULT1}$ is a digital output that depends on the early warning thresholds at the input selected by r15h and r16h[3:0]
	[7]	0 = $\overline{FAULT1}$ is an active-low digital output 1 = $\overline{FAULT1}$ is an active-high digital output
17h	[0]	1 = $\overline{FAULT2}$ is a digital output dependent on MON1
	[1]	1 = $\overline{FAULT2}$ is a digital output dependent on MON2
	[2]	1 = $\overline{FAULT2}$ is a digital output dependent on MON3
	[3]	1 = $\overline{FAULT2}$ is a digital output dependent on MON4
	[4]	1 = $\overline{FAULT2}$ is a digital output dependent on MON5
	[5]	1 = $\overline{FAULT2}$ is a digital output dependent on MON6
	[6]	1 = $\overline{FAULT2}$ is a digital output dependent on MON7
	[7]	1 = $\overline{FAULT2}$ is a digital output dependent on MON8

Table 7. $\overline{\text{FAULT1}}$ and $\overline{\text{FAULT2}}$ Output Configuration and Dependencies (continued)

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
18h	[0]	1 = $\overline{\text{FAULT2}}$ is a digital output dependent on MON9*
	[1]	1 = $\overline{\text{FAULT2}}$ is a digital output dependent on MON10*
	[2]	1 = $\overline{\text{FAULT2}}$ is a digital output dependent on MON11*
	[3]	1 = $\overline{\text{FAULT2}}$ is a digital output dependent on MON12*
	[4]	1 = $\overline{\text{FAULT2}}$ is a digital output that depends on the overvoltage thresholds at the input selected by r17h and r18h[3:0]
	[5]	1 = $\overline{\text{FAULT2}}$ is a digital output that depends on the undervoltage thresholds at the input selected by r17h and 18h[3:0]
	[6]	1 = $\overline{\text{FAULT2}}$ is a digital output that depends on the early warning thresholds at the input selected by r17h and r18h[3:0]
	[7]	0 = $\overline{\text{FAULT2}}$ is an active-low digital output 1 = $\overline{\text{FAULT2}}$ is an active-high digital output

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Fault-On Power-Up ($\overline{\text{FAULTPU}}$)

GPIO6 indicates a fault during power-up or power-down when configured as a "fault-on power-up" output. Under these conditions, all EN_OUT_ voltages are pulled low and fault data is saved to nonvolatile EEPROM. See the *Faults* section.

$\overline{\text{MARGINUP}}$ and $\overline{\text{MARGINDN}}$

Configure GPIO2 and GPIO3 as margin-up ($\overline{\text{MARGINUP}}$) and margin-down ($\overline{\text{MARGINDN}}$) inputs, respectively, for margining functionality. Pull $\overline{\text{MARGINUP}}$ low and pull $\overline{\text{MARGINDN}}$ high to select DACOUT_ voltage values set in registers r66h to r71h. Pull $\overline{\text{MARGINDN}}$ low and pull $\overline{\text{MARGINUP}}$ high to select DACOUT_ values set in registers r72h to r7Dh. Pull both $\overline{\text{MARGINUP}}$ and $\overline{\text{MARGINDN}}$ high or low to select DACOUT_ values set in registers r00h to r0Bh. See the *Voltage Margining* section for more information on setting DACOUT_ outputs for margining.

Margin-up and margin-down functionality is controlled by GPIO2 and GPIO3 when configured for margining (see Table 8). When $\overline{\text{MARGINUP}}$ or $\overline{\text{MARGINDN}}$ are asserted, the DAC output switches are automatically closed and the margin function is enabled. Writing to the DAC-enabled registers (r1Ch and r1Dh) is not required to close the DAC switches. See the *MARGIN* section for an explanation of the margin function.

Table 8. $\overline{\text{MARGINUP}}$ and $\overline{\text{MARGINDN}}$ FUNCTION

$\overline{\text{MARGINUP}}$ (GPIO2)	$\overline{\text{MARGINDN}}$ (GPIO3)	DACOUT REGISTER USED	DACOUT SWITCH STATE
1	1	DACOUT registers r00h to r0Bh	Depends on r1Ch, r1Dh*
1	0	$\overline{\text{MARGINDN}}$ registers r72h to r7Dh	Closed
0	1	$\overline{\text{MARGINUP}}$ registers r66h to r71h	Closed
0	0	DACOUT registers r00h to r0Bh	Depends on r1Ch, r1Dh*

*****Note:*** *r1Ch and r1Dh are located in the extended page.*

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MARGIN

GPIO6 is configurable as an active-low MARGIN input. Drive MARGIN low before varying system voltages above or below the thresholds to avoid signaling an error. Drive MARGIN high for normal operation.

When MARGIN is pulled low or r4Dh[1] is a '1,' the margin function is enabled. FAULT1, FAULT2, Any_Fault, and RESET are latched in their current state. Threshold violations will be ignored, and faults will not be logged.

Manual Reset (MR)

GPIO4 is configurable to act as an active-low manual reset input, MR. Drive MR low to assert RESET. RESET remains low for the selected reset timeout period after MR transitions from low to high. See the *RESET* section for more information on selecting a reset timeout period.

Watchdog Input (WDI) and Output (WDO)

Set r1Eh[1:0] and register r1Dh[7] to '110' to configure GPIO6 as WDO. Set r1Dh[6:4] to '111' to configure GPIO5 as WDI. WDO is an open-drain active-low output. See the *Watchdog Timer* section for more information about the operation of the watchdog timer.

Programmable Outputs (EN_OUT1–EN_OUT12)

The MAX16046 includes twelve programmable outputs, and the MAX16048 includes eight programmable outputs. These outputs are capable of connecting to either the enable (EN) inputs of a DC-DC or LDO power supply or to the gates of series-pass MOSFETs for closed-loop tracking mode, or for charge-pump mode. Selectable output configurations include: active-low or active-high, open-drain or push-pull. EN_OUT1–EN_OUT4 are also configurable for closed-loop tracking, and EN_OUT1–EN_OUT6 can act as charge-pump outputs with no closed-loop tracking. Use the registers r1Fh to r22h to configure outputs. See Table 9 for detailed information on configuring EN_OUT1–EN_OUT12.

Table 9. EN_OUT1–EN_OUT12 Configuration

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
1Fh	[2:0]	**EN_OUT1 Configuration:** 000 = EN_OUT1 is an open-drain active-low output 001 = EN_OUT1 is an open-drain active-high output 010 = EN_OUT1 is a push-pull active-low output 011 = EN_OUT1 is a push-pull active-high output 100 = EN_OUT1 is used in closed-loop tracking 101 = EN_OUT1 is configured with a charge-pump output (MON1 + 5V) capable of driving an external n-channel MOSFET 110 = Reserved 111 = Reserved
	[5:3]	**EN_OUT2 Configuration:** 000 = EN_OUT2 is an open-drain active-low output 001 = EN_OUT2 is an open-drain active-high output 010 = EN_OUT2 is a push-pull active-low output 011 = EN_OUT2 is a push-pull active-high output 100 = EN_OUT2 is used in closed-loop tracking 101 = EN_OUT2 is configured with a charge-pump output (MON2 + 5V) capable of driving an external n-channel MOSFET 110 = Reserved 111 = Reserved
	[7:6]	**EN_OUT3 Configuration (LSBs):** 000 = EN_OUT3 is an open-drain active-low output 001 = EN_OUT3 is an open-drain active-high output 010 = EN_OUT3 is a push-pull active-low output 011 = EN_OUT3 is a push-pull active-high output 100 = EN_OUT3 is used in closed-loop tracking 101 = EN_OUT3 is configured with a charge-pump output (MON3 + 5V) capable of driving an external n-channel MOSFET 110 = Reserved 111 = Reserved

Table 9. EN_OUT1–EN_OUT12 Configuration (continued)

REGISTER/EEPROM ADDRESS	BIT RANGE	DESCRIPTION
20h	[0]	**EN_OUT3 Configuration (MSB)**—see r1Fh[7:6]
	[3:1]	**EN_OUT4 Configuration:** 000 = EN_OUT4 is an open-drain active-low output 001 = EN_OUT4 is an open-drain active-high output 010 = EN_OUT4 is a push-pull active-low output 011 = EN_OUT4 is a push-pull active-high output 100 = EN_OUT4 is used in closed-loop tracking 101 = EN_OUT4 is configured with a charge-pump output (MON4 + 5V) capable of driving an external n-channel MOSFET 110 = Reserved 111 = Reserved
	[6:4]	**EN_OUT5 Configuration:** 000 = EN_OUT5 is an open-drain active-low output 001 = EN_OUT5 is an open-drain active-high output 010 = EN_OUT5 is a push-pull active low output 011 = EN_OUT5 is a push-pull active-high output 100 = Reserved. EN_OUT5 is not usable for closed-loop tracking. 101 = EN_OUT5 is configured with a charge-pump output (MON5 + 5V) capable of driving an external n-channel MOSFET 110 = Reserved 111 = Reserved
	[7]	**EN_OUT6 Configuration (LSB)**—see r21h[1:0]
21h	[1:0]	**EN_OUT6 Configuration (MSBs):** 000 = EN_OUT6 is an open-drain active-low output 001 = EN_OUT6 is an open-drain active-high output 010 = EN_OUT6 is a push-pull active-low output 011 = EN_OUT6 is a push-pull active-high output 100 = Reserved. EN_OUT6 is not useable for closed-loop tracking. 101 = EN_OUT6 is configured with a charge-pump output (MON6 + 5V) capable of driving an external n-channel MOSFET 110 = Reserved 111 = Reserved
	[3:2]	**EN_OUT7 Configuration:** 00 = EN_OUT7 is an open-drain active-low output 01 = EN_OUT7 is an open-drain active-high output 10 = EN_OUT7 is a push-pull active-low output 11 = EN_OUT7 is a push-pull active-high output
	[5:4]	**EN_OUT8 Configuration:** 00 = EN_OUT8 is an open-drain active-low output 01 = EN_OUT8 is an open-drain active-high output 10 = EN_OUT8 is a push-pull active-low output 11 = EN_OUT8 is a push-pull active-high output
	[7:6]	**EN_OUT9 Configuration*:** 00 = EN_OUT9 is an open-drain active-low output 01 = EN_OUT9 is an open-drain active-high output 10 = EN_OUT9 is a push-pull active-low output 11 = EN_OUT9 is a push-pull active-high output

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Table 9. EN_OUT1–EN_OUT12 Configuration (continued)

REGISTER/EEPROM ADDRESS	BIT RANGE	DESCRIPTION
22h	[1:0]	**EN_OUT10 Configuration*:** 00 = EN_OUT10 is an open-drain active-low output 01 = EN_OUT10 is an open-drain active-high output 10 = EN_OUT10 is a push-pull active-low output 11 = EN_OUT10 is a push-pull active-high output
	[3:2]	**EN_OUT11 Configuration*:** 00 = EN_OUT11 is an open-drain active-low output 01 = EN_OUT11 is an open-drain active-high output 10 = EN_OUT11 is a push-pull active-low output 11 = EN_OUT11 is a push-pull active-high output
	[5:4]	**EN_OUT12 Configuration*:** 00 = EN_OUT12 is an open-drain active-low output 01 = EN_OUT12 is an open-drain active high output 10 = EN_OUT12 is a push-pull active-low output 11 = EN_OUT12 is a push-pull active-high output
	[7:6]	Reserved

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Charge-Pump Configuration

EN_OUT1–EN_OUT6 can act as high-voltage charge-pump outputs to drive up to six external n-channel MOSFETs. During sequencing, an EN_OUT_ output configured this way drives 6µA until the voltage reaches 5V above the corresponding MON_ to fully enhance the external n-channel MOSFET. For example, EN_OUT2 will rise to 5V above MON2. See the *Sequencing* section for more detailed information on power-supply sequencing.

Closed-Loop Tracking Operation

EN_OUT1–EN_OUT4 can operate in closed-loop tracking mode. When configured for closed-loop tracking, EN_OUT1–EN_OUT4 are capable of driving the gates of up to four external n-channel MOSFETs. For closed-loop tracking, configure GPIO1–GPIO4 as return-sense line inputs (INS_) to be used in conjunction with EN_OUT1–EN_OUT4 and MON1–MON4. See the *Closed-Loop Tracking* section.

Open-Drain Output Configuration

Connect an external pullup resistor from the output to an external voltage up to 6V (abs max, EN_OUT7 to EN_OUT12) or 12V (abs max, EN_OUT1 to EN_OUT6) when configured as an open-drain output. Choose the pullup resistor depending on the number of devices connected to the open-drain output and the allowable current consumption. The open-drain output configuration allows wire-ORed connection.

Push-Pull Output Configuration

The MAX16046/MAX16048s' programmable outputs sink 2mA and source 100µA when configured as push-pull outputs.

EN_OUT_ State During Power-Up

When V_{CC} is ramped from 0V to the operating supply voltage, the EN_OUT_ output is high impedance until V_{CC} is approximately 2.4V and then EN_OUT_ will be in its configured deasserted state. See Figures 3 and 4. $\overline{RESET}$ is configured as an active-low open-drain output pulled up to V_{CC} through a 10kΩ resistor for Figures 3 and 4.

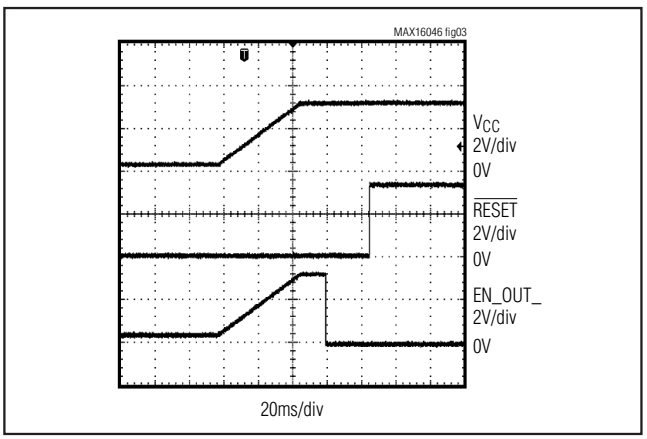

Figure 3. $\overline{RESET}$ and EN_OUT_ During Power-Up, EN_OUT_ Is in Open-Drain Active-Low Configuration

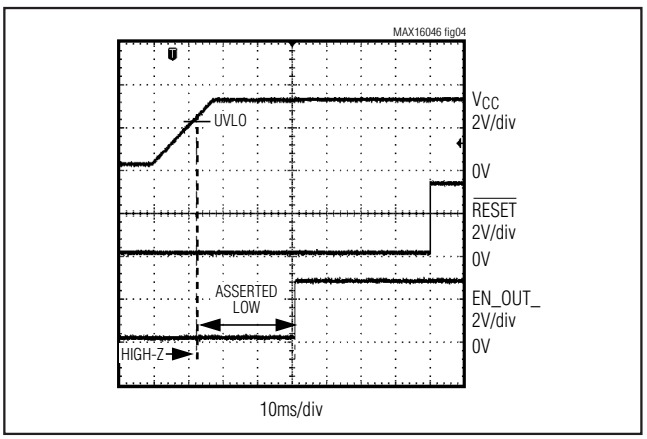

Figure 4. $\overline{RESET}$ and EN_OUT_ During Power-Up, EN_OUT_ Is in Push-Pull Active-High Configuration

Sequencing

Each EN_OUT_ has one or more associated MON_ inputs, facilitating the voltage monitoring of multiple power supplies. To sequence a system of power supplies safely, the output voltage of a power supply must be good before the next power supply may turn on. Connect EN_OUT_ outputs to the enable input of an external power supply and connect MON_ inputs to the output of the power supply for voltage monitoring. More than one MON_ may be used if the power supply has multiple outputs.

Sequence Order

The MAX16046/MAX16048 utilize a system of ordered slots to sequence multiple power supplies. To determine the sequence order, assign each EN_OUT_ to a slot ranging from Slot 0 to Slot 11. EN_OUT_(s) assigned to Slot 0 are turned on first, followed by outputs assigned to Slot 1, and so on through Slot 11. Multiple EN_OUT_s assigned to the same slot turn on at the same time.

Each slot has a built-in configurable sequence delay (registers r50h to r54h) ranging from 20µs to 1.6s. During a reverse sequence, slots are turned off in reverse order starting from Slot 11. The MAX16046/MAX16048 may be configured to power-down in simultaneous mode or in reverse sequence mode as set in r54h[4]. See Tables 10, 11, and 12 for the EN_OUT_ slot assignment bits and Tables 13 and 14 for the sequence delays.

Monitoring Inputs While Sequencing

An enabled MON_ input may be assigned to a slot ranging from Slot 1 to Slot 12. Monitoring inputs are always checked at the beginning of a slot. The inputs are given the power-up fault delay within which they must satisfy the programmed undervoltage limit; otherwise a fault condition will occur. The fault occurs regardless of the critical fault enable bits. This undervoltage limit cannot be disabled during power-up and power-down. EN_OUT_s configured for open-drain, push-pull, or charge-pump operation are always asserted at the end of a slot, following the sequence delay. See Tables 10, 11, and 12 for the MON_ slot assignment bits.

Slot 0 does not monitor any MON_ input. Instead, Slot 0 waits for the $\overline{Software\ Enable}$ bit r4Dh[0] to be a logic '0' and for the voltage on EN to rise above 0.525V before asserting any assigned outputs. Outputs assigned to Slot 0 are asserted before the Slot 0 sequence delay. Generally, Slot 0 controls the enable inputs of power supplies that are first in the sequence.

Similarly, Slot 12 does not control any EN_OUT_ outputs. Rather, Slot 12 monitors assigned MON_ inputs and then enters the power-on state. Generally, Slot 12 monitors the last power supplies in the sequence. The power-up sequence is complete when any MON_ inputs assigned to Slot 12 exceed their undervoltage thresholds and the sequence delay is expired. If no MON_ inputs are assigned to Slot 12, the power-up sequence is complete after the slot sequence delay is expired.

The output rail(s) of a power supply should be monitored by one or more MON_ inputs placed in the succeeding slot, ensuring that the output of the supply is not checked until it has first been turned on. For example, if a power supply uses EN_OUT1 located in Slot 3 and has two monitoring inputs, MON1 and MON2, they must both be assigned to Slot 4. In this example, EN_OUT1 turns on at the end of Slot 3. At the start of Slot 4, MON1 and MON2 must exceed the undervoltage threshold before the programmed power-up fault delay; otherwise a fault triggers.

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$\overline{\text{RESET}}$ Deassertion

After any MON_ inputs assigned to Slot 12 exceed their undervoltage thresholds, the reset timeouts begin. When the reset timeout completes, $\overline{\text{RESET}}$ deasserts. The reset timeout period is set in r19h[6:4] (see Table 27).

Power-Down

Power-down starts when EN is pulled low or the Software Enable bit is set to '1.' $\overline{\text{RESET}}$ asserts as soon as power-down begins regardless of the reset output dependencies. Power down EN_OUT_s simultaneously or in reverse sequence mode by setting the Reverse Sequence bit (r54h[4]) appropriately. In reverse sequence mode (r54h[4] set to '1'), the EN_OUT_s assigned to Slot 11 deassert, the MAX16046/MAX16048 wait for the Slot 11 sequence delay and then proceed to Slot 10, and so on until the EN_OUT_s assigned to Slot 0 turn off. When simultaneous power-down is selected (r54h[4] set to '0'), all EN_OUT_s turn off at the same time.

Table 10. MON_ and EN_OUT_ Slot Assignment Registers

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
56h	[3:0]	MON1 Slot Assignment Register
	[7:4]	MON2 Slot Assignment Register
57h	[3:0]	MON3 Slot Assignment Register
	[7:4]	MON4 Slot Assignment Register
58h	[3:0]	MON5 Slot Assignment Register
	[7:4]	MON6 Slot Assignment Register
59h	[3:0]	MON7 Slot Assignment Register
	[7:4]	MON8 Slot Assignment Register
5Ah	[3:0]	MON9 Slot Assignment Register*
	[7:4]	MON10 Slot Assignment Register*
5Bh	[3:0]	MON11 Slot Assignment Register*
	[7:4]	MON12 Slot Assignment Register*
5Eh	[3:0]	EN_OUT1 Slot Assignment Register
	[7:4]	EN_OUT2 Slot Assignment Register
5Fh	[3:0]	EN_OUT3 Slot Assignment Register
	[7:4]	EN_OUT4 Slot Assignment Register
60h	[3:0]	EN_OUT5 Slot Assignment Register
	[7:4]	EN_OUT6 Slot Assignment Register
61h	[3:0]	EN_OUT7 Slot Assignment Register
	[7:4]	EN_OUT8 Slot Assignment Register
62h	[3:0]	EN_OUT9 Slot Assignment Register*
	[7:4]	EN_OUT10 Slot Assignment Register*
63h	[3:0]	EN_OUT11 Slot Assignment Register*
	[7:4]	EN_OUT12 Slot Assignment Register *

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Table 11. MON_ Slot Assignment

CONFIGURATION BITS	DESCRIPTION
0000	MON_ is not assigned to a slot
0001	MON_ is assigned to Slot 1
0010	MON_ is assigned to Slot 2
0011	MON_ is assigned to Slot 3
0100	MON_ is assigned to Slot 4
0101	MON_ is assigned to Slot 5
0110	MON_ is assigned to Slot 6
0111	MON_ is assigned to Slot 7
1000	MON_ is assigned to Slot 8
1001	MON_ is assigned to Slot 9
1010	MON_ is assigned to Slot 10
1011	MON_ is assigned to Slot 11
1100	MON_ is assigned to Slot 12
1101	Not used
1110	Not used
1111	Not used

Table 12. EN_OUT_ Slot Assignment

CONFIGURATION BITS	DESCRIPTION
0000	EN_OUT_ is not assigned to a slot
0001	EN_OUT_ is assigned to Slot 0
0010	EN_OUT_ is assigned to Slot 1
0011	EN_OUT_ is assigned to Slot 2
0100	EN_OUT_ is assigned to Slot 3
0101	EN_OUT_ is assigned to Slot 4
0110	EN_OUT_ is assigned to Slot 5
0111	EN_OUT_ is assigned to Slot 6
1000	EN_OUT_ is assigned to Slot 7
1001	EN_OUT_ is assigned to Slot 8
1010	EN_OUT_ is assigned to Slot 9
1011	EN_OUT_ is assigned to Slot 10
1100	EN_OUT_ is assigned to Slot 11
1101	Not used
1110	Not used
1111	Not used

Table 13. Sequence Delays and Fault Recovery

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
4Eh	[1:0]	**Power-Up Fault Timeout** 00 = 25ms 01 = 50ms 10 = 100ms 11 = 200ms
	[3:2]	**Power-Down Fault Timeout** 00 = 25ms 01 = 50ms 10 = 100ms 11 = 200ms
	[4]	**INS1 Pulldown Resistor Enable** 0 = Pulldown resistor for INS1 is disabled 1 = Pulldown resistor for INS1 is enabled
	[5]	**INS2 Pulldown Resistor Enable** 0 = Pulldown resistor for INS2 is disabled 1 = Pulldown resistor for INS2 is enabled
	[6]	**INS3 Pulldown Resistor Enable** 0 = Pulldown resistor for INS3 is disabled 1 = Pulldown resistor for INS3 is enabled
	[7]	**INS4 Pulldown Resistor Enable** 0 = Pulldown resistor for INS4 is disabled 1 = Pulldown resistor for INS4 is enabled
4Fh	[2:0]	**Autoretry Timeout** 000 = 20µs 001 = 12.5ms 010 = 25ms 011 = 50ms 100 = 100ms 101 = 200ms 110 = 400ms 111 = 1.6s
	[3]	**Fault Recovery Mode** 0 = Autoretry procedure is performed following a fault event 1 = Latch-off on fault
	[5:4]	**Slew Rate** 00 = 800V/s 01 = 400V/s 10 = 200V/s 11 = 100V/s
	[7:6]	**Fault Deglitch** 00 = 2 conversions 01 = 4 conversions 10 = 8 conversions 11 = 16 conversions

Table 13. Sequence Delays and Fault Recovery (continued)

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
50h	[2:0]	Slot 0 Sequence Delay
	[5:3]	Slot 1 Sequence Delay
	[7:6]	Slot 2 Sequence Delay (LSBs)
51h	[0]	Slot 2 Sequence Delay (MSB)—see r50h[7:6]
	[3:1]	Slot 3 Sequence Delay
	[6:4]	Slot 4 Sequence Delay
	[7]	Slot 5 Sequence Delay (LSB)—see r52h[1:0]
52h	[1:0]	Slot 5 Sequence Delay
	[4:2]	Slot 6 Sequence Delay
	[7:5]	Slot 7 Sequence Delay
53h	[2:0]	Slot 8 Sequence Delay
	[5:3]	Slot 9 Sequence Delay
	[7:6]	Slot 10 Sequence Delay (LSBs)
54h	[0]	Slot 10 Sequence Delay (MSB)—see r53h[7:6]
	[3:1]	Slot 11 Sequence Delay
	[4]	**Reverse Sequence** 0 = Power down all EN_OUT_s at the same time (simultaneously) 1 = Controlled power-down will be reverse of power-up sequence
	[7:5]	Not used

Table 14. Slot Sequence Delay Selection

CONFIGURATION BITS	SLOT SEQUENCE DELAY
000	20µs
001	12.5ms
010	25ms
011	50ms
100	100ms
101	200ms
110	400ms
111	1.6s

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Closed-Loop Tracking

The MAX16046/MAX16048 track up to four voltages during any time slot except Slot 0 and Slot 12. Configure GPIO1–GPIO4 as sense line inputs (INS_) to monitor tracking voltages. Configure GPIO6 as FAULTPU to indicate tracking faults, if desired. See the *General-Purpose Inputs/Outputs* section for information on configuring GPIOs.

For closed-loop tracking, use MON1, EN_OUT1, and INS1 together to form a complete channel. Use MON2, EN_OUT2, and INS2 to form a second complete channel. Use MON3, EN_OUT3, and INS3 together to form a third channel. Use MON4, EN_OUT4, and INS4 to form a fourth channel.

When configured for closed-loop tracking, assign each EN_OUT_ to the same slot as its associated single monitoring input (MON_). For example, if EN_OUT2 is assigned to Slot 3, the monitoring input is MON2 and must be assigned to Slot 3. This is because the MON_ input, checked at the start of the slot, must be valid before tracking can begin. Tracking begins immediately and must finish before the power-up fault timeout expires, or a fault will trigger. EN_OUT_ configured for closed-loop tracking cannot be assigned to Slot 0.

The tracking control circuitry includes a ramp generator and a comparator control block for each tracked voltage (see the *Functional Diagram* and Figure 5). The comparator control block compares each INS_ voltage with a control voltage ramp. If INS_ voltages vary from the control ramp by more than 150mV (typ), the comparator control block signals an alert that dynamically stops the ramp until the slow INS_ voltage rises to within the allowed voltage window. The total tracking time is extended under these conditions, but must still complete within the selected power-up/power-down fault timeout. The power-up/power-down tracking fault timeout period is adjustable through r4Eh[3:0].

A voltage difference between any two tracking INS_ voltages exceeding 330mV generates a tracking fault, forcing all EN_OUT_ voltages low and generating a fault log. If configured as FAULTPU, GPIO6 asserts when a tracking fault occurs.

The comparator control blocks also monitor INS_ voltages with respect to input (MON_) voltages. Under normal conditions each INS_ tracks the control ramp until the INS_ voltages reach the configured power-good (PG) thresholds, set as a programmable percentage of the MON_ voltage. Use register r64h to set the PG thresholds (Table 15). Once PG is detected, the external n-channel FET saturates with 5V (typ) applied between gate and source. The slew rate for the control ramp is programmable from 100V/s to 800V/s in r4Fh[5:4] (see Table 13).

Power-down initiates when EN is forced low or when the Software Enable bit in r4Dh[0] is set to '1.' If the Reverse Sequence bit is set (r54h[4]) INS_ voltages follow a falling reference ramp to ground as long as MON_ voltages remain high enough to supply the required voltage/current. If a monitored voltage drops faster than the control ramp voltage or the corresponding MON_ voltage falls too quickly, power-down tracking operation is terminated and all EN_OUT_ voltages are immediately forced to ground. If the Reverse Sequence bit is set to '0,' all EN_OUT_ voltages are forced low simultaneously.

The MAX16046/MAX16048 include selectable internal 100Ω pulldown resistors to ensure that tracked voltages are not held high by large external capacitors during a fault event. The pulldowns help to ensure that monitored INS_ voltages are fully discharged before the next power-up cycle is initiated. These pulldowns are high impedance during normal operation. Set r4Eh[7:4] to '1' to enable the pulldown resistors (Table 13). These pulldown resistors may also be used with EN_OUT1–EN_OUT4 channels not configured for closed-loop tracking, which is useful to discharge the output capacitors of a DC-DC converter during shutdown. For this case, configure the GPIO as an INS_ input and set the 100Ω pulldown bit, but do not enable closed-loop tracking. Connect the INS_ input to the output of the power supply.

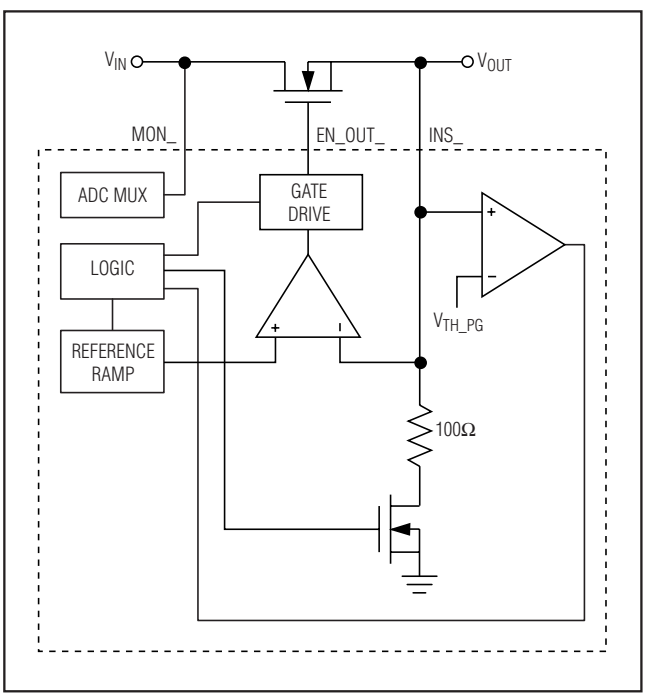

Figure 5. Closed-Loop Tracking

Table 15. Power-Good (PG) Thresholds

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
64h	[1:0]	00 = PG is asserted when monitored V_{MON1} is 95% of V_{INS1} 01 = PG is asserted when monitored V_{MON1} is 92.5% of V_{INS1} 10 = PG is asserted when monitored V_{MON1} is 90% of V_{INS1} 11 = PG is asserted when monitored V_{MON1} is 87.5% of V_{INS1}
	[3:2]	00 = PG is asserted when monitored V_{MON2} is 95% of V_{INS2} 01 = PG is asserted when monitored V_{MON2} is 92.5% of V_{INS2} 10 = PG is asserted when monitored V_{MON2} is 90% of V_{INS2} 11 = PG is asserted when monitored V_{MON2} is 87.5% of V_{INS2}
	[5:4]	00 = PG is asserted when monitored V_{MON3} is 95% of V_{INS3} 01 = PG is asserted when monitored V_{MON3} is 92.5% of V_{INS3} 10 = PG is asserted when monitored V_{MON3} is 90% of V_{INS3} 11 = PG is asserted when monitored V_{MON3} is 87.5% of V_{INS3}
	[7:6]	00 = PG is asserted when monitored V_{MON4} is 95% of V_{INS4} 01 = PG is asserted when monitored V_{MON4} is 92.5% of V_{INS4} 10 = PG is asserted when monitored V_{MON4} is 90% of V_{INS4} 11 = PG is asserted when monitored V_{MON4} is 87.5% of V_{INS4}

DAC Outputs

The MAX16046/MAX16048 feature an 8-bit DAC with 12 outputs (MAX16046) or 8 outputs (MAX16048) for voltage margining. Program the voltage on the DAC outputs (DACOUT1–DACOUT12) to trim external power-supply voltages, by connecting through a series resistor to the feedback node or to the trim input. DAC outputs are high impedance during power-up to prevent improper operation of the external power supplies and must be explicitly enabled by setting the appropriate DACOUT_ enable bits.

Each DACOUT output has three voltage ranges: 0.4V to 0.8V, 0.6V to 1.2V, and 0.8V to 1.6V. Configure DAC outputs using registers r12h to r14h (see Table 16). Calculate DACOUT_ voltages, $V_{DACOUT\_}$, using the following equation:

$$V_{DACOUT\_} = DAC_{ACC}\ (V) + ((DAC_n - 80h) \times (DAC_{RNG})/255)\ (V)$$

where DAC_{ACC} is the DAC center code absolute accuracy and DAC_{RNG} is the DAC output voltage range as listed in the *Electrical Characteristics* table and 07h < DAC_n < F8h.

Set any DACOUT_ range configuration register to 00h to switch off the DACOUT buffer. Set the DACOUT_ enable bit to '0' to leave the DAC output as high impedance. See Table 16 for the registers associated with the DAC output ranges.

The DAC enable bits are not copied from EEPROM during the boot phase; therefore each DACOUT_ output must be enabled in the r1Ch and r1Dh registers, located in the extended page, following power-up. See Table 17 for the DAC enable bits.

To control the voltage on a particular DAC output, write the 8-bit binary value to the appropriate output register; see Table 18 for the register locations. Although these registers are located in the default page, they are not stored in nonvolatile EEPROM and are set to '0' after a POR.

Table 16. DACOUT Ranges

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
12h	[1:0]	**DACOUT1 Range Selection:** 00 = DACOUT1 is OFF 01 = 0.4V (min) to 0.8V (max) 10 = 0.6V (min) to 1.2V (max) 11 = 0.8V (min) to 1.6V (max)
	[3:2]	**DACOUT2 Range Selection:** 00 = DACOUT2 is OFF 01 = 0.4V (min) to 0.8V (max) 10 = 0.6V (min) to 1.2V (max) 11 = 0.8V (min) to 1.6V (max)
	[5:4]	**DACOUT3 Range Selection:** 00 = DACOUT3 is OFF 01 = 0.4V (min) to 0.8V (max) 10 = 0.6V (min) to 1.2V (max) 11 = 0.8V (min) to 1.6V (max)
	[7:6]	**DACOUT4 Range Selection:** 00 = DACOUT4 is OFF 01 = 0.4V (min) to 0.8V (max) 10 = 0.6V (min) to 1.2V (max) 11 = 0.8V (min) to 1.6V (max)
13h	[1:0]	**DACOUT5 Range Selection:** 00 = DACOUT5 is OFF 01 = 0.4V (min) to 0.8V (max) 10 = 0.6V (min) to 1.2V (max) 11 = 0.8V (min) to 1.6V (max)
	[3:2]	**DACOUT6 Range Selection:** 00 = DACOUT6 is OFF 01 = 0.4V (min) to 0.8V (max) 10 = 0.6V (min) to 1.2V (max) 11 = 0.8V (min) to 1.6V (max)
	[5:4]	**DACOUT7 Range Selection:** 00 = DACOUT7 is OFF 01 = 0.4V (min) to 0.8V (max) 10 = 0.6V (min) to 1.2V (max) 11 = 0.8V (min) to 1.6V (max)
	[7:6]	**DACOUT8 Range Selection:** 00 = DACOUT8 is OFF 01 = 0.4V (min) to 0.8V (max) 10 = 0.6V (min) to 1.2V (max) 11 = 0.8V (min) to 1.6V (max)

Table 16. DACOUT Ranges (continued)

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
14h	[1:0]	**DACOUT9 Range Selection*:** 00 = DACOUT9 is OFF 01 = 0.4V (min) to 0.8V (max) 10 = 0.6V (min) to 1.2V (max) 11 = 0.8V (min) to 1.6V (max)
	[3:2]	**DACOUT10 Range Selection*:** 00 = DACOUT10 is OFF 01 = 0.4V (min) to 0.8V (max) 10 = 0.6V (min) to 1.2V (max) 11 = 0.8V (min) to 1.6V (max)
	[5:4]	**DACOUT11 Range Selection*:** 00 = DACOUT11 is OFF 01 = 0.4V (min) to 0.8V (max) 10 = 0.6V (min) to 1.2V (max) 11 = 0.8V (min) to 1.6V (max)
	[7:6]	**DACOUT12 Range Selection*:** 00 = DACOUT12 is OFF 01 = 0.4V (min) to 0.8V (max) 10 = 0.6V (min) to 1.2V (max) 11 = 0.8V (min) to 1.6V (max)

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Table 17. DACOUT Enables

EXTENDED PAGE ADDRESS	DACOUT ENABLES	
1Ch	[0]	1 = DACOUT1 is enabled
	[1]	1 = DACOUT2 is enabled
	[2]	1 = DACOUT3 is enabled
	[3]	1 = DACOUT4 is enabled
	[4]	1 = DACOUT5 is enabled
	[5]	1 = DACOUT6 is enabled
	[6]	1 = DACOUT7 is enabled
	[7]	1 = DACOUT8 is enabled
1Dh	[0]	1 = DACOUT9 is enabled*
	[1]	1 = DACOUT10 is enabled*
	[2]	1 = DACOUT11 is enabled*
	[3]	1 = DACOUT12 is enabled*
	[7:4]	Reserved

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Table 18. DACOUT Voltages

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
00h	[7:0]	DACOUT1 Data
01h	[7:0]	DACOUT2 Data
02h	[7:0]	DACOUT3 Data
03h	[7:0]	DACOUT4 Data
04h	[7:0]	DACOUT5 Data
05h	[7:0]	DACOUT6 Data
06h	[7:0]	DACOUT7 Data
07h	[7:0]	DACOUT8 Data
08h	[7:0]	DACOUT9 Data*
09h	[7:0]	DACOUT10 Data*
0Ah	[7:0]	DACOUT11 Data*
0Bh	[7:0]	DACOUT12 Data*

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Voltage Margining

Margining is commonly performed while a system is under development, but margining can also be performed during the manufacturing process. The supply voltages of external DC-DC regulators can be adjusted by trimming the regulator's reference input (for voltage-regulator modules), altering the voltage regulator's feedback node, or adjusting a "brick" power supply's trim input. See the *Applications Information* section for sample circuits.

Margining can be controlled over the serial interface or by using GPIO2 and GPIO3. Before adjusting the voltages using the DAC outputs, enable voltage margining functionality by setting the Margin bit at r4Dh[1] to '1' (see Table 1) or configure GPIO6 as $\overline{\text{MARGIN}}$ (see Tables 4 and 5). Set DACOUT_ voltages to the appropriate values and then enable the appropriate DAC outputs.

To control margining with external circuitry, configure GPIO2 and GPIO3 as $\overline{\text{MARGINUP}}$ and $\overline{\text{MARGINDN}}$ inputs, respectively. Pull $\overline{\text{MARGINUP}}$ low and pull $\overline{\text{MARGINDN}}$ high to select DACOUT_ voltage values set in registers r66h to r71h. Pull $\overline{\text{MARGINDN}}$ low and pull $\overline{\text{MARGINUP}}$ high to select DACOUT_ values set in registers r72h to r7Dh (see Tables 19 and 20). Pull both $\overline{\text{MARGINUP}}$ and $\overline{\text{MARGINDN}}$ high or low to select DACOUT_ values set in registers r00h to r0Bh.

See Table 16 for more information on setting the voltage ranges for the DACOUT_ outputs. Table 20 shows which register values are used for the DAC outputs for each state of $\overline{\text{MARGINUP}}$ and $\overline{\text{MARGINDN}}$.

Table 19. DACOUT1–DACOUT12 Margin Data

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
66h	[7:0]	DACOUT1 Margin-Up Data
67h	[7:0]	DACOUT2 Margin-Up Data
68h	[7:0]	DACOUT3 Margin-Up Data
69h	[7:0]	DACOUT4 Margin-Up Data
6Ah	[7:0]	DACOUT5 Margin-Up Data
6Bh	[7:0]	DACOUT6 Margin-Up Data
6Ch	[7:0]	DACOUT7 Margin-Up Data
6Dh	[7:0]	DACOUT8 Margin-Up Data
6Eh	[7:0]	DACOUT9 Margin-Up Data*
6Fh	[7:0]	DACOUT10 Margin-Up Data*
70h	[7:0]	DACOUT11 Margin-Up Data*
71h	[7:0]	DACOUT12 Margin-Up Data*

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
72h	[7:0]	DACOUT1 Margin-Down Data
73h	[7:0]	DACOUT2 Margin-Down Data
74h	[7:0]	DACOUT3 Margin-Down Data
75h	[7:0]	DACOUT4 Margin-Down Data
76h	[7:0]	DACOUT5 Margin-Down Data
77h	[7:0]	DACOUT6 Margin-Down Data
78h	[7:0]	DACOUT7 Margin-Down Data
79h	[7:0]	DACOUT8 Margin-Down Data
7Ah	[7:0]	DACOUT9 Margin-Down Data*
7Bh	[7:0]	DACOUT10 Margin-Down Data*
7Ch	[7:0]	DACOUT11 Margin-Down Data*
7Dh	[7:0]	DACOUT12 Margin-Down Data*

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Table 20. DACOUT Margining Output Dependencies

$\overline{\text{MARGINUP}}$ (GPIO2)	$\overline{\text{MARGINDN}}$ (GPIO3)	DACOUT REGISTER USED	DACOUT SWITCH STATE
1	1	DACOUT registers r00h to r0Bh	Depends on r1Ch, r1Dh
1	0	MARGIN DN registers r72h to r7Dh	Closed
0	1	MARGIN UP registers r66h to r71h	Closed
0	0	DACOUT registers r00h to r0Bh	Depends on r1Ch, r1Dh

Faults

The MAX16046/MAX16048 monitor the input (MON_) channels and compare the results with an overvoltage threshold, an undervoltage threshold, and a selectable overvoltage or undervoltage early warning threshold. Based on these conditions, the MAX16046/MAX16048 can assert various fault outputs and save specific information about the channel conditions and voltages into the nonvolatile EEPROM. Once a critical fault event occurs, the failing channel condition, ADC conversions at the time of the fault, or both may be saved by configuring the event logger. The event logger records a single failure in the internal EEPROM and sets a lock bit which protects the stored fault data from accidental erasure on a subsequent power-up.

The MAX16046/MAX16048 are capable of measuring overvoltage and undervoltage fault events. Fault conditions are detected at the end of each ADC conversion. An overvoltage event occurs when the voltage at a monitored input exceeds the overvoltage threshold for that input. An undervoltage fault occurs when the voltage at a monitored input falls below the undervoltage threshold. Fault thresholds are set in registers r23h to r46h as shown in Table 21. Disabled inputs are not monitored for fault conditions and are skipped over by the input multiplexer. Only the upper 8 bits of a conversion result are compared with the programmed fault thresholds. Inputs not assigned to a sequencing slot are not monitored for fault conditions but are still recorded in the ADC results registers.

The general-purpose inputs/outputs (GPIO1–GPIO6) can be configured as Any_Fault outputs or dedicated $\overline{\text{FAULT1}}$ and $\overline{\text{FAULT2}}$ outputs to indicate fault conditions. These fault outputs are not masked by the critical fault enable bits shown in Table 23. See the *General-Purpose Inputs/Outputs* section for more information on configuring GPIOs as fault outputs.

Table 21. Fault Thresholds

REGISTER/ EEPROM ADDRESS	DESCRIPTION
23h	MON1 Early Warning Threshold
24h	MON1 Overvoltage Threshold
25h	MON1 Undervoltage Threshold
26h	MON2 Early Warning Threshold
27h	MON2 Overvoltage Threshold
28h	MON2 Undervoltage Threshold
29h	MON3 Early Warning Threshold
2Ah	MON3 Overvoltage Threshold
2Bh	MON3 Undervoltage Threshold
2Ch	MON4 Early Warning Threshold
2Dh	MON4 Overvoltage Threshold
2Eh	MON4 Undervoltage Threshold
2Fh	MON5 Early Warning Threshold
30h	MON5 Overvoltage Threshold
31h	MON5 Undervoltage Threshold
32h	MON6 Early Warning Threshold
33h	MON6 Overvoltage Threshold
34h	MON6 Undervoltage Threshold
35h	MON7 Early Warning Threshold
36h	MON7 Overvoltage Threshold
37h	MON7 Undervoltage Threshold
38h	MON8 Early Warning Threshold
39h	MON8 Overvoltage Threshold
3Ah	MON8 Undervoltage Threshold
3Bh	MON9 Early Warning Threshold*
3Ch	MON9 Overvoltage Threshold*
3Dh	MON9 Undervoltage Threshold*
3Eh	MON10 Early Warning Threshold*
3Fh	MON10 Overvoltage Threshold*
40h	MON10 Undervoltage Threshold*
41h	MON11 Early Warning Threshold*
42h	MON11 Overvoltage Threshold*
43h	MON11 Undervoltage Threshold*
44h	MON12 Early Warning Threshold*
45h	MON12 Overvoltage Threshold*
46h	MON12 Undervoltage Threshold*

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Deglitch

Fault conditions are detected at the end of each conversion. If the voltage on an input falls outside a monitored threshold for one acquisition, the input multiplexer remains on that channel and performs several successive conversions. To trigger a fault, the input must stay outside the threshold for a certain number of acquisitions as determined by the deglitch setting in r4Fh[7:6] (see Table 25).

Fault Flags

Fault flags indicate the fault status of a particular input. The fault flag of any monitored input in the device can be read at any time from registers r18h and r19h in the extended page, as shown in Table 22. Clear a fault flag by writing a '1' to the appropriate bit in the flag register. Unlike the fault signals sent to the fault outputs, these bits are masked by the critical fault enable bits (see Table 23). The fault flag will only be set if the matching enable bit in the critical fault enable register is also set.

Critical Faults

If a specific input threshold is critical to the operation of the system, an automatic fault log can be configured to shut down all the EN_OUT_s and trigger a transfer of fault information to EEPROM. For a fault condition to trigger a critical fault, set the appropriate enable bit in registers r48h to r4Ch (see Table 23).

Logged fault information is stored in EEPROM registers r00h to r0Eh (see Table 24). Once a fault log event occurs, the EEPROM is locked and must be unlocked to enable a new fault log to be stored. Write a '1' to r5Dh[1] to unlock the EEPROM. Fault information can be configured to store ADC conversion results and/or fault flags in registers r01h and r02h. Select the critical fault configuration in r47h[1:0]. Set r47h[1:0] to '11' to turn off the fault logger. All stored ADC results are 8 bits wide.

Table 22. Fault Flags

EXTENDED PAGE ADDRESS	BIT RANGE	DESCRIPTION
18h	[0]	1 = MON1 conversion exceeds overvoltage or undervoltage thresholds
	[1]	1 = MON2 conversion exceeds overvoltage or undervoltage thresholds
	[2]	1 = MON3 conversion exceeds overvoltage or undervoltage thresholds
	[3]	1 = MON4 conversion exceeds overvoltage or undervoltage thresholds
	[4]	1 = MON5 conversion exceeds overvoltage or undervoltage thresholds
	[5]	1 = MON6 conversion exceeds overvoltage or undervoltage thresholds
	[6]	1 = MON7 conversion exceeds overvoltage or undervoltage thresholds
	[7]	1 = MON8 conversion exceeds overvoltage or undervoltage thresholds
19h	[0]	1 = MON9 conversion exceeds overvoltage or undervoltage thresholds*
	[1]	1 = MON10 conversion exceeds overvoltage or undervoltage thresholds*
	[2]	1 = MON11 conversion exceeds overvoltage or undervoltage thresholds*
	[3]	1 = MON12 conversion exceeds overvoltage or undervoltage thresholds*
	[7:4]	Not used

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Table 23. Critical Fault Configuration and Enable Bits

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
47h	[1:0]	**Critical Fault Log Control** 00 = Failed lines and ADC conversion values save to EEPROM upon critical fault 01 = Failed line flags only saved to EEPROM upon critical fault 10 = ADC conversion values only saved to EEPROM upon critical fault 11 = No information saved upon critical fault
	[7:2]	Not used
48h	[0]	1 = Fault log triggered when MON1 is below its undervoltage threshold
	[1]	1 = Fault log triggered when MON2 is below its undervoltage threshold
	[2]	1 = Fault log triggered when MON3 is below its undervoltage threshold
	[3]	1 = Fault log triggered when MON4 is below its undervoltage threshold
	[4]	1 = Fault log triggered when MON5 is below its undervoltage threshold
	[5]	1 = Fault log triggered when MON6 is below its undervoltage threshold
	[6]	1 = Fault log triggered when MON6 is below its undervoltage threshold
	[7]	1 = Fault log triggered when MON8 is below its undervoltage threshold
49h	[0]	1 = Fault log triggered when MON9 is below its undervoltage threshold*
	[1]	1 = Fault log triggered when MON10 is below its undervoltage threshold*
	[2]	1 = Fault log triggered when MON11 is below its undervoltage threshold*
	[3]	1 = Fault log triggered when MON12 is below its undervoltage threshold*
	[4]	1 = Fault log triggered when MON1 is above its overvoltage threshold
	[5]	1 = Fault log triggered when MON2 is above its overvoltage threshold
	[6]	1 = Fault log triggered when MON3 is above its overvoltage threshold
	[7]	1 = Fault log triggered when MON3 is above its overvoltage threshold
4Ah	[0]	1 = Fault log triggered when MON5 is above its overvoltage threshold
	[1]	1 = Fault log triggered when MON6 is above its overvoltage threshold
	[2]	1 = Fault log triggered when MON7 is above its overvoltage threshold
	[3]	1 = Fault log triggered when MON8 is above its overvoltage threshold
	[4]	1 = Fault log triggered when MON9 is above its overvoltage threshold*
	[5]	1 = Fault log triggered when MON10 is above its overvoltage threshold*
	[6]	1 = Fault log triggered when MON11 is above its overvoltage threshold*
	[7]	1 = Fault log triggered when MON12 is above its overvoltage threshold*
4Bh	[0]	1 = Fault log triggered when MON1 is above/below its early earning threshold
	[1]	1 = Fault log triggered when MON2 is above/below its early warning threshold
	[2]	1 = Fault log triggered when MON3 is above/below its early warning threshold
	[3]	1 = Fault log triggered when MON4 is above/below its early warning threshold
	[4]	1 = Fault log triggered when MON5 is above/below its early warning threshold
	[5]	1 = Fault log triggered when MON6 is above/below its early warning threshold
	[6]	1 = Fault log triggered when MON7 is above/below its early warning threshold
	[7]	1 = Fault log triggered when MON8 is above/below its early warning threshold

Table 23. Critical Fault Configuration and Enable Bits (continued)

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
4Ch	[0]	1 = Fault log triggered when MON9 is above/below its early warning threshold*
	[1]	1 = Fault log triggered when MON10 is above/below its early warning threshold*
	[2]	1 = Fault log triggered when MON11 is above/below its early warning threshold*
	[3]	1 = Fault log triggered when MON12 is above/below its early warning threshold*
	[7:4]	Not used

**MAX16046 only*

Table 24. Fault Log EEPROM

EEPROM ADDRESS	BIT RANGE	DESCRIPTION
00h	[3:0]	**Power-Up/Power-Down Fault Register** Slot where power-up/power-down fault is detected
	[4]	**Tracking Fault Bits** If '0,' tracking fault occurred on MON1/EN_OUT1/INS1
	[5]	If '0,' tracking fault occurred on MON2/EN_OUT2/INS2
	[6]	If '0,' tracking fault occurred on MON3/EN_OUT3/INS3
	[7]	If '0,' tracking fault occurred on MON4/EN_OUT4/INS4
01h	[0]	If '1,' fault occurred on MON1
	[1]	If '1,' fault occurred on MON2
	[2]	If '1,' fault occurred on MON3
	[3]	If '1,' fault occurred on MON4
	[4]	If '1,' fault occurred on MON5
	[5]	If '1,' fault occurred on MON6
	[6]	If '1,' fault occurred on MON7
	[7]	If '1,' fault occurred on MON8
02h	[0]	If '1,' fault occurred on MON9*
	[1]	If '1,' fault occurred on MON10*
	[2]	If '1,' fault occurred on MON11*
	[3]	If '1,' fault occurred on MON12*
	[7:4]	Not used
03h	[7:0]	**MON_ ADC Fault Information (only the 8 MSBs of converted channels are saved following a fault event)** MON1 conversion result at the time the fault log was triggered
04h	[7:0]	MON2 conversion result at the time the fault log was triggered
05h	[7:0]	MON3 conversion result at the time the fault log was triggered
06h	[7:0]	MON4 conversion result at the time the fault log was triggered
07h	[7:0]	MON5 conversion result at the time the fault log was triggered
08h	[7:0]	MON6 conversion result at the time the fault log was triggered
09h	[7:0]	MON7 conversion result at the time the fault log was triggered
0Ah	[7:0]	MON8 conversion result at the time the fault log was triggered
0Bh	[7:0]	MON9 conversion result at the time the fault log was triggered*
0Ch	[7:0]	MON10 conversion result at the time the fault log was triggered*
0Dh	[7:0]	MON11 conversion result at the time the fault log was triggered*
0Eh	[7:0]	MON12 conversion result at the time the fault log was triggered*

**MAX16046 only*

Power-Up/Power-Down Faults

All EN_OUTs are deasserted if an overvoltage or undervoltage fault is detected during power-up/power-down (regardless of the critical fault enable bits). Under these conditions, information of the failing slot is stored in EEPROM r00h[3:0] unless r47h[1:0] is set to '11' (see Table 23).

If there is a tracking fault on a channel configured for closed-loop tracking, a fault log operation occurs and the bits representing the failed tracking channels are set to '0' unless r47h[1:0] is set to '11' (see Table 24).

Autoretry/Latch Mode

For critical faults, the MAX16046/MAX16048 can be configured for one of two fault management methods: autoretry or latch-on-fault. Set r4Fh[3] to '0' to select autoretry mode. In this configuration, the device will shut down after a critical fault event and then restart following a configurable delay. Use r4Fh[2:0] to select an autoretry delay from 20µs to 1.6s. See Table 25 for more information on setting the autoretry delay.

Set r4Fh[3] to '1' to select the latch-on-fault mode. In this configuration EN_OUT_s are deasserted after a critical fault event. The device does not re-initiate the power-up sequence until EN is toggled or the Software Enable bit is reset to '0.' See the *Enable* section for more information on setting the Software Enable bit.

If fault information is stored in EEPROM (see the *Critical Faults* section) and autoretry mode is selected, set an autoretry delay greater than the time required for the storing operation. If fault information is stored in EEPROM and latch-on-fault mode is chosen, toggle EN or reset the Software Enable bit only after the completion of the storing operation. If saving information about the failed lines only, ensure a delay of at least 60ms before the restart procedure. Otherwise, ensure a minimum 204ms timeout. This ensures that ADC conversions are completed and values are stored correctly in EEPROM. See Table 26 for more information about required fault log operation periods.

Table 25. Fault Recovery Configuration

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
4Fh	[2:0]	**Autoretry Delay** 000 = 20µs 001 = 12.5ms 010 = 25ms 011 = 50ms 100 = 100ms 101 = 200ms 110 = 400ms 111 = 1.6s
	[3]	**Fault Recovery Mode** 0 = Autoretry procedure is performed following a fault event 1 = Latchoff on fault
	[5:4]	**Slew Rate** 00 = 800V/s 01 = 400V/s 10 = 200V/s 11 = 100V/s
	[7:6]	**Fault Deglitch** 00 = 2 conversions 01 = 4 conversions 10 = 8 conversions 11 = 16 conversions

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Table 26. EEPROM Fault Log Operation Period

FAULT CONTROL REGISTER r47h[1:0]	DESCRIPTION	MINIMUM REQUIRED SHUTDOWN PERIOD (ms)
00	Failed lines and ADC values saved	204
01	Failed lines saved	60
10	ADC values saved	168
11	No information saved	N/A

$\overline{RESET}$

The reset output, $\overline{RESET}$, is asserted during power-up/power-down and deasserts following the reset time-out period once the power-up sequence is complete. The power-up sequence is complete when any MON_ inputs assigned to Slot 12 exceed their undervoltage thresholds. If no MON_ inputs are assigned to Slot 12, the power-up sequence is complete after the slot sequence delay is expired.

$\overline{RESET}$ is a configurable output that monitors selected MON_ voltages during normal operation. $\overline{RESET}$ also depends on any monitoring input that has one or more critical fault enable bits set. Use r19h[1:0] to configure $\overline{RESET}$ to assert on an overvoltage fault, undervoltage fault, or both. Use r19h[3:2] to configure $\overline{RESET}$ as an active-high/active-low push-pull/open-drain output. If desired, configure GPIO4 as a manual reset input, $\overline{MR}$, and pull $\overline{MR}$ low to assert $\overline{RESET}$. $\overline{RESET}$ includes a programmable timeout. See Table 27 for $\overline{RESET}$ dependencies and configuration registers.

Table 27. $\overline{RESET}$ Configuration and Dependencies

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
19h	[1:0]	**$\overline{RESET}$ OUTPUT CONFIGURATION** 00 = $\overline{RESET}$ is asserted if at least one of the selected inputs exceeds its undervoltage threshold 01 = $\overline{RESET}$ is asserted if at least one of the selected inputs exceeds its early warning threshold 10 = $\overline{RESET}$ is asserted if at least one of the selected inputs exceeds its overvoltage threshold 11 = $\overline{RESET}$ is asserted if any of the selected inputs exceeds undervoltage or overvoltage thresholds
	[2]	0 = $\overline{RESET}$ is an active-low output 1 = $\overline{RESET}$ is an active-high output
	[3]	0 = $\overline{RESET}$ is a push-pull output 1 = $\overline{RESET}$ is an open-drain output
	[6:4]	**$\overline{RESET}$ TIMEOUT** 000 = 25µs 001 = 2ms 010 = 25ms 011 = 100ms 100 = 200ms 101 = 400ms 110 = 800ms 111 = 1600ms
	[7]	Reserved

Table 27. $\overline{\text{RESET}}$ Configuration and Dependencies (continued)

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
1Ah	[0]	**$\overline{\text{RESET}}$ DEPENDENCIES** 1 = $\overline{\text{RESET}}$ is dependent on MON1
	[1]	1 = $\overline{\text{RESET}}$ is dependent on MON2
	[2]	1 = $\overline{\text{RESET}}$ is dependent on MON3
	[3]	1 = $\overline{\text{RESET}}$ is dependent on MON4
	[4]	1 = $\overline{\text{RESET}}$ is dependent on MON5
	[5]	1 = $\overline{\text{RESET}}$ is dependent on MON6
	[6]	1 = $\overline{\text{RESET}}$ is dependent on MON7
	[7]	1 = $\overline{\text{RESET}}$ is dependent on MON8
1Bh	[0]	1 = $\overline{\text{RESET}}$ is dependent on MON9*
	[1]	1 = $\overline{\text{RESET}}$ is dependent on MON10*
	[2]	1 = $\overline{\text{RESET}}$ is dependent on MON11*
	[3]	1 = $\overline{\text{RESET}}$ is dependent on MON12*
	[7:4]	Reserved

**MAX16046 only*

Watchdog Timer

The watchdog timer can operate together with or independently of the MAX16046/MAX16048. When operating in dependent mode, the watchdog is not activated until the sequencing is complete and $\overline{\text{RESET}}$ is deasserted. When operating in independent mode, the watchdog timer is independent of the sequencing operation and activates immediately after V_{CC} exceeds the UVLO threshold and the boot phase is complete. Set r4Dh[3] to '0' to configure the watchdog in dependent mode. Set r4Dh[3] to '1' to configure the watchdog in independent mode. See Table 28 for more information on configuring the watchdog timer in dependent or independent mode.

Dependent Watchdog Timer Operation

The watchdog timer can be used to monitor µP activity in two modes. Flexible timeout architecture provides an adjustable watchdog startup delay of up to 128s, allowing complicated systems to complete lengthy boot-up routines. An adjustable watchdog timeout allows the supervisor to provide quick alerts when processor activity fails. After each reset event (V_{CC} drops below UVLO then returns above UVLO, software reboot, manual reset ($\overline{\text{MR}}$), EN input going low then high, or watchdog reset) and once sequencing is complete, the watchdog startup delay provides an extended time for the system to power up and fully initialize all µP and system components before assuming responsibility for routine watchdog updates. Set r55h[6] to '1' to enable the watchdog startup delay. Set r55h[6] to '0' to disable the watchdog startup delay.

The normal watchdog timeout period, t_{WDI}, begins after the first transition on WDI before the conclusion of the long startup watchdog period, $t_{WDI\_STARTUP}$ (Figures 6 and 7). During the normal operating mode, WDO asserts if the µP does not toggle WDI with a valid transition (high-to-low or low-to-high) within the standard timeout period, t_{WDI}. WDO remains asserted until WDI is toggled or $\overline{\text{RESET}}$ is asserted (Figure 7).

While EN is low, or r55h[7] is a '0,' the watchdog timer is in reset. The watchdog timer does not begin counting until the power-on mode is reached and $\overline{\text{RESET}}$ is deasserted. The watchdog timer is reset and WDO deasserts any time $\overline{\text{RESET}}$ is asserted (Figure 8). The watchdog timer will be held in reset while $\overline{\text{RESET}}$ is asserted.

The watchdog can be configured to control the $\overline{\text{RESET}}$ output as well as the WDO output. $\overline{\text{RESET}}$ is pulsed low for the reset timeout, t_{RP}, when the watchdog timer expires and the Watchdog Reset Output Enable bit (r55h[7]) is set to '1.' Therefore, WDO pulses low for a short time (approximately 1µs) when the watchdog timer expires. $\overline{\text{RESET}}$ is not affected by the watchdog timer when the Watchdog Reset Output Enable bit (r55h[7]) is set to '0.'

See Table 29 for more information on configuring watchdog functionality.

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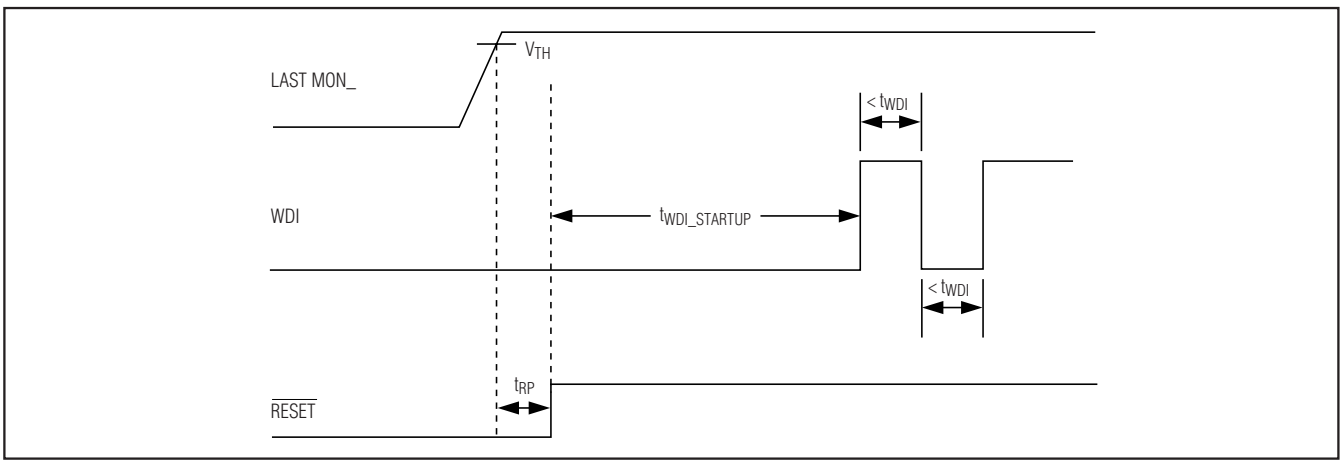

Figure 6. Normal Watchdog Startup Sequence

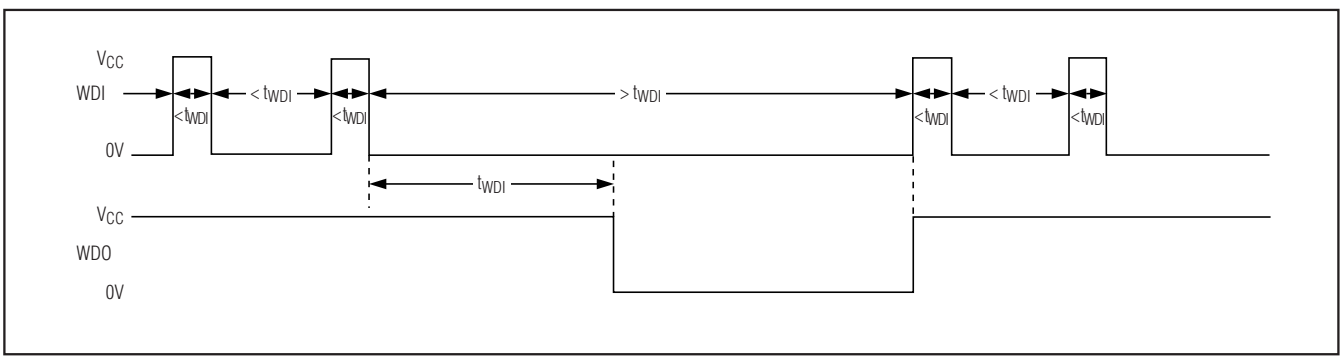

Figure 7. Watchdog Timer Operation

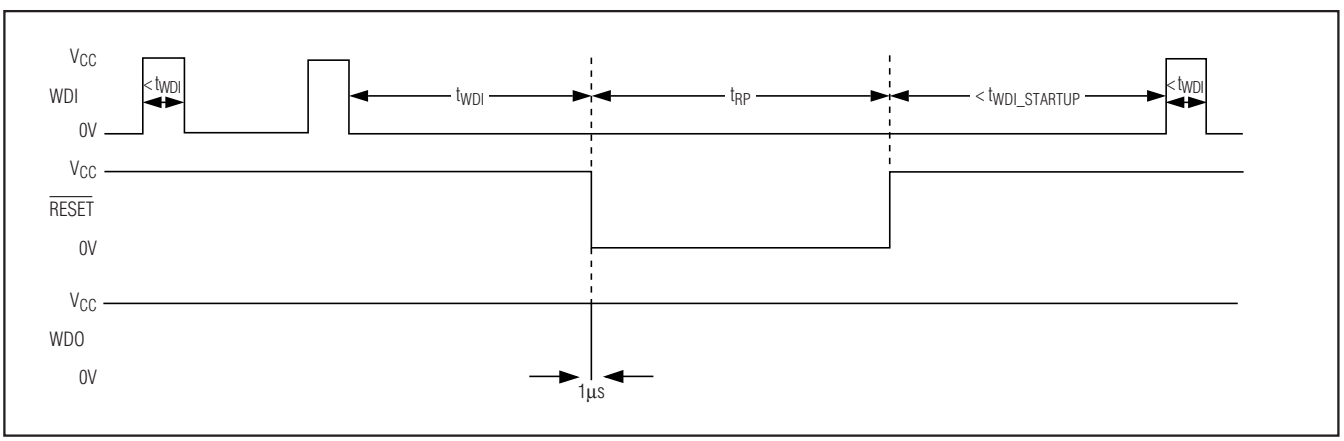

Figure 8. Watchdog Startup Sequence with Watchdog Reset Output Enable Bit (r55h[7]) Set to '1'

Table 28. Watchdog Mode Selection

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
4Dh	0	**$\overline{\text{Software Enable}}$ Bit** 0 = Enabled. EN must also be high to begin sequencing. 1 = Disabled (factory default)
	1	**Margin Bit** 1 = Margin functionality is enabled 0 = Margin disabled
	2	**Early Warning Selection Bit** 0 = Early warning thresholds are undervoltage thresholds 1 = Early warning thresholds are overvoltage thresholds
	3	**Watchdog Mode Selection Bit** 0 = Watchdog timer is in dependent mode 1 = Watchdog timer is in independent mode
	[7:4]	Not used

Table 29. Watchdog Enables and Configuration

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
55h	[2:0]	**Watchdog Timeout** 000 = 1ms 001 = 4ms 010 = 12.5ms 011 = 50ms 100 = 200ms 101 = 800ms 110 = 1.6s 111 = 3.2s
	[4:3]	**Watchdog Startup Delay** 00 = 25.6s 01 = 51.2s 10 = 102.4s 11 = 128s
	[5]	**Watchdog Enable** 1 = Watchdog enabled 0 = Watchdog disabled
	[6]	**Watchdog Startup Delay Enable** 1 = Watchdog startup delay enabled 0 = Watchdog startup delay disabled
	[7]	**Watchdog Reset Output Enable** 1 = Watchdog timeout asserts $\overline{\text{RESET}}$ output 0 = Watchdog timeout does not assert $\overline{\text{RESET}}$ output

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Independent Watchdog Timer Operation

When r4Dh[3] is '1' the watchdog timer operates in the independent mode. In the independent mode, the watchdog timer operates as if it were a separate chip. The watchdog timer is activated immediately upon V_{CC} exceeding UVLO and once the boot-up sequence is finished. If $\overline{RESET}$ is asserted by the sequencer state machine, the watchdog timer and WDO will not be affected.

There will be a long startup delay if r55h[6] is a '1.' If r55h[6] is a '0,' there will not be a long startup delay.

In independent mode, if the Watchdog Reset Output Enable bit r55h[7] is set to '1,' when the watchdog timer expires, WDO will be asserted, then $\overline{RESET}$ will be asserted. WDO will then be deasserted. WDO will be low for 3 system clock cycles or approximately 1µs. If the Watchdog Reset Output Enable bit (r55h[7]) is set to '0,' when the WDT expires, WDO will be asserted but $\overline{RESET}$ will not be affected.

Miscellaneous

Table 30 lists several miscellaneous programmable items. Register r5Ch provides storage space for a user-defined configuration or firmware version number. Bit r5Dh[0] locks and unlocks the configuration registers. Bit r5Dh[1] locks and unlocks EEPROM addresses 00h to 11h. Write data to EEPROM r5Dh as normally done; however, to toggle a bit in register r5Dh, write a '1' to that bit. The r65h[2:0] bits contain a read-only manufacturing revision code.

Table 30. Miscellaneous Settings

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
5Ch	[7:0]	User identification. Eight bits of memory for user-defined identification.
5Dh	[0]	**Configuration Lock** 0 = Configuration registers and EEPROM writable. 1 = Configuration registers and EEPROM [except r5Dh] locked.
	[1]	**EEPROM Fault Data Lock Flag (set automatically after fault log is triggered):** 0 = EEPROM is not locked. A triggered fault log stores fault information to EEPROM. 1 = EEPROM addresses 00h to 11h are locked. Write a '1' to this bit to toggle the flag.
	[7:2]	Not used
65h	[2:0]	Manufacturing revision code. This register is read only. Not stored in EEPROM.
	[7:3]	Not used

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I²C/SMBus-Compatible Serial Interface

The MAX16046/MAX16048 feature an I²C/SMBus-compatible 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX16046/MAX16048 and the master device at clock rates up to 400kHz. Figure 1 shows the 2-wire interface timing diagram. The MAX16046/MAX16048 are transmit/receive slave-only devices, relying upon a master device to generate a clock signal. The master device (typically a microcontroller) initiates a data transfer on the bus and generates SCL to permit that transfer.

A master device communicates to the MAX16046/MAX16048 by transmitting the proper address followed by command and/or data words. The slave address input, A0, is capable of detecting four different states, allowing multiple identical devices to share the same serial bus. The slave address is described further in the *Slave Address* section. Each transmit sequence is framed by a START (S) or REPEATED START (SR) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse. SCL is a logic input, while SDA is an open-drain input/output. SCL and SDA both require external pullup resistors to generate the logic-high voltage. Use 4.7kΩ for most applications.

Bit Transfer

Each clock pulse transfers one data bit. The data on SDA must remain stable while SCL is high (Figure 9); otherwise the MAX16046/MAX16048 registers a START or STOP condition (Figure 10) from the master. SDA and SCL idle high when the bus is not busy.

START and STOP Conditions

Both SCL and SDA idle high when the bus is not busy. A master device signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. The master device issues a STOP condition by transitioning SDA from low to high while SCL is high. A STOP condition frees the bus for another transmission. The bus remains active if a REPEATED START condition is generated, such as in the block read protocol (see Figure 1).

Early STOP Conditions

The MAX16046/MAX16048 recognize a STOP condition at any point during transmission except if a STOP condition occurs in the same high pulse as a START condition. This condition is not a legal I²C format; at least one clock pulse must separate any START and STOP condition.

REPEATED START Conditions

A REPEATED START may be sent instead of a STOP condition to maintain control of the bus during a read operation. The START and REPEATED START conditions are functionally identical.

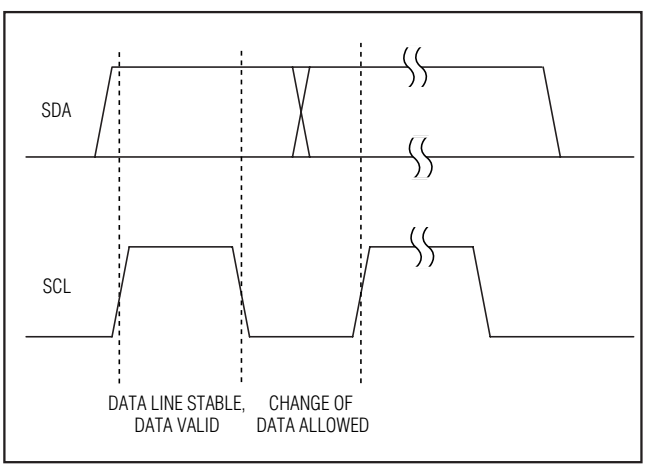

Figure 9. Bit Transfer

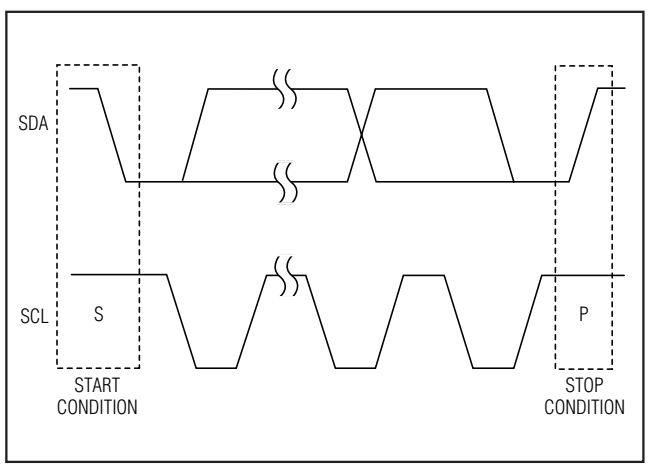

Figure 10. START and STOP Conditions

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Acknowledge

The acknowledge bit (ACK) is the 9th bit attached to any 8-bit data word. The receiving device always generates an ACK. The MAX16046/MAX16048 generate an ACK when receiving an address or data by pulling SDA low during the 9th clock period (Figure 11). When transmitting data, such as when the master device reads data back from the MAX16046/MAX16048, the device waits for the master device to generate an ACK. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if the receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time. The MAX16046/MAX16048 generate a NACK after the command byte received during a software reboot, while writing to the EEPROM, or when receiving an illegal memory address.

Slave Address

Use the slave address input, A0, to allow multiple identical devices to share the same serial bus. Connect A0 to GND, DBP (or an external supply voltage greater than 2V), SCL, or SDA to set the device address on the bus. See Table 31 for a listing of all possible 7-bit addresses.

Table 31. Setting the I²C/SMBus Slave Address

A0	SLAVE ADDRESS
0	1010 00XR
1	1010 01XR
SCL	1010 10XR
SDA	1010 11XR

X = Don't care, R = Read/write select bit

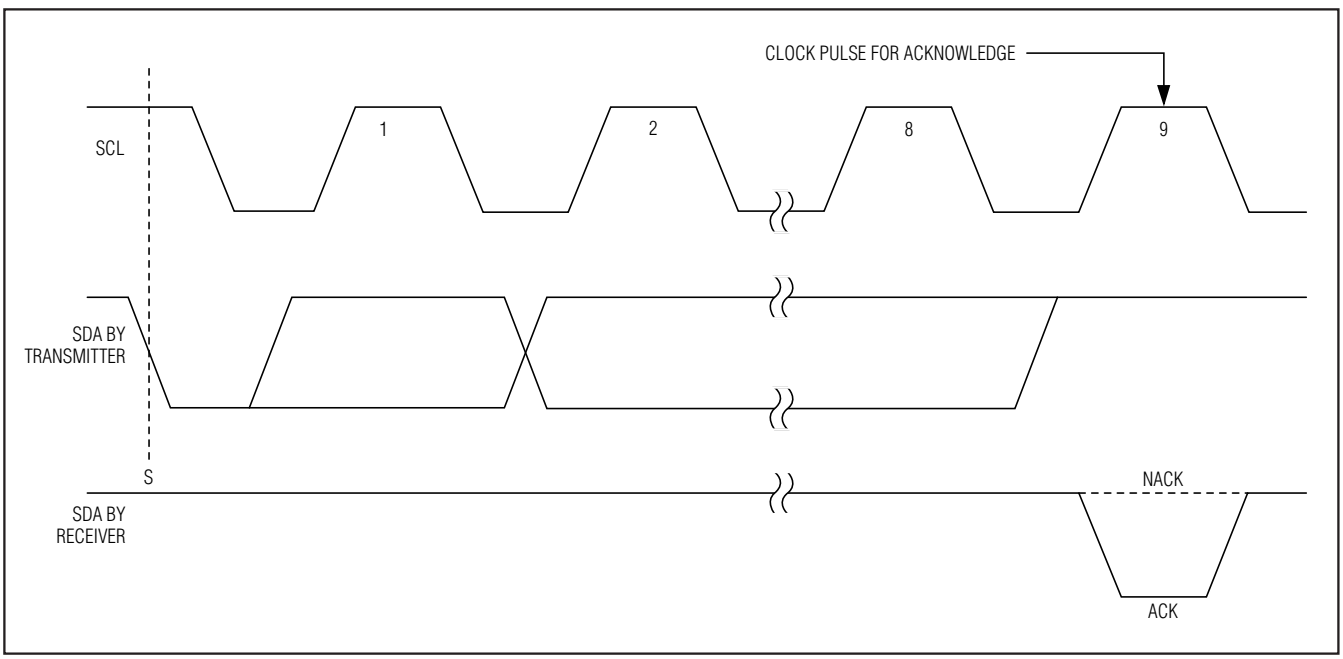

Figure 11. Acknowledge

Send Byte

The send byte protocol allows the master device to send one byte of data to the slave device (see Figure 12). The send byte presets a register pointer address for a subsequent read or write. The slave sends a NACK instead of an ACK if the master tries to send a memory address or command code that is not allowed. If the master sends 94h or 95h, the data is ACK, because this could be the start of the write block or read block. If the master sends a STOP condition before the slave asserts an ACK, the internal address pointer does not change. If the master sends 96h, this signifies a software reboot. The send byte procedure is the following:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends an 8-bit memory address or command code.
5) The addressed slave asserts an ACK (or NACK) on SDA.
6) The master sends a STOP condition.

Receive Byte

The receive byte protocol allows the master device to read the register content of the MAX16046/MAX16048 (see Figure 12). The EEPROM or register address must be preset with a send byte or write word protocol first. Once the read is complete, the internal pointer increases by one. Repeating the receive byte protocol reads the contents of the next address. The receive byte procedure follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a read bit (high).
3) The addressed slave asserts an ACK on SDA.
4) The slave sends 8 data bits.
5) The master asserts a NACK on SDA.
6) The master generates a STOP condition.

Write Byte

The write byte protocol (see Figure 12) allows the master device to write a single byte in the default page, extended page, or EEPROM page, depending on which page is currently selected. The write byte procedure is the following:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends an 8-bit memory address.
5) The addressed slave asserts an ACK on SDA.
6) The master sends an 8-bit data byte.
7) The addressed slave asserts an ACK on SDA.
8) The master sends a STOP condition.

To write a single byte, only the 8-bit memory address and a single 8-bit data byte are sent. The data byte is written to the addressed location if the memory address is valid. The slave will assert a NACK at step 5 if the memory address is not valid.

Read Byte

The read byte protocol (see Figure 12) allows the master device to read a single byte located in the default page, extended page, or EEPROM page depending on which page is currently selected. The read byte procedure is the following:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends an 8-bit memory address.
5) The addressed slave asserts an ACK on SDA.
6) The master sends a REPEATED START condition.
7) The master sends the 7-bit slave address and a read bit (high).
8) The addressed slave asserts an ACK on SDA.
9) The slave sends an 8-bit data byte.
10) The master asserts a NACK on SDA.
11) The master sends a STOP condition.

If the memory address is not valid, it is NACKed by the slave at step 5 and the address pointer is not modified.

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Command Codes

The MAX16046/MAX16048 use eight command codes for block read, block write, and other commands. See Table 32 for a list of command codes.

To initiate a software reboot, send 96h using the send byte format. A software-initiated reboot is functionally the same as a hardware-initiated power-on reset. During boot-up, EEPROM configuration data in the range of 0Fh to 7Dh is copied to the same register addresses in the default page.

Send command code 97h to trigger a fault store to EEPROM. Configure the Critical Fault Log Control register (r47h) to store ADC conversion results and/or fault flags in registers once the command code has been sent.

Using command code 98h allows access to the extended page, which contains registers for ADC conversion results, DACOUT enables, and GPIO input/output data. Use command code 99h to return to the default page.

Send command code 9Ah to access the EEPROM page. Once command code 9Ah has been sent, all addresses are recognized as EEPROM addresses only. Send command code 9Bh to return to the default page.

When accessing any EEPROM location using a read byte or block read protocol, set the address to the desired location, send a dummy read byte protocol, and then set the address to the desired location again. This primes the device for subsequent read operations.

Table 32. Command Codes

COMMAND CODE	ACTION
94h	Write block
95h	Read block
96h	Reboot EEPROM in register file
97h	Trigger fault store to EEPROM
98h	Extended page access on
99h	Extended page access off
9Ah	EEPROM page access on
9Bh	EEPROM page access off

Block Write

The block write protocol (see Figure 12) allows the master device to write a block of data (1 byte to 16 bytes) to memory. The destination address should be preloaded by a previous send byte command; otherwise the block write command begins to write at the current address pointer. After the last byte is written, the address pointer remains preset to the next valid address. If the number of bytes to be written causes the address pointer to exceed FFh for EEPROM or 7Dh for configuration registers, the address pointer stays at FFh or 7Dh, overwriting this memory address with the remaining bytes of data. The last data byte sent is stored at register address FFh. The slave generates a NACK at step 5 if the command code is invalid or if the device is busy, and the address pointer is not altered. The block write procedure is the following:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends the 8-bit command code for block write (94h).
5) The addressed slave asserts an ACK on SDA.
6) The master sends the 8-bit byte count (1 byte to 16 bytes), *n*.
7) The addressed slave asserts an ACK on SDA.
8) The master sends 8 bits of data.
9) The addressed slave asserts an ACK on SDA.
10) Repeat steps 8 and 9 *n* - 1 times.
11) The master sends a STOP condition.

Block Read

The block read protocol (see Figure 12) allows the master device to read a block of up to 16 bytes from memory. Read fewer than 16 bytes of data by issuing an early STOP condition from the master or by generating a NACK with the master. The destination address should be preloaded by a previous send byte command; otherwise the block read command begins to read at the current address pointer. If the number of bytes to be read causes the address pointer to exceed FFh for the configuration register or EEPROM, the address pointer stays at FFh and the last data byte read is from register rFFh. The block read procedure is the following:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends 8 bits of the block read command (95h).
5) The slave asserts an ACK on SDA, unless busy.
6) The master generates a REPEATED START condition.
7) The master sends the 7-bit slave address and a read bit (high).

8) The slave asserts an ACK on SDA.
9) The slave sends the 8-bit byte count (16).
10) The master asserts an ACK on SDA.
11) The slave sends 8 bits of data.
12) The master asserts an ACK on SDA.
13) Repeat steps 11 and 12 up to fifteen times.
14) The master asserts a NACK on SDA.
15) The master sends a STOP condition.

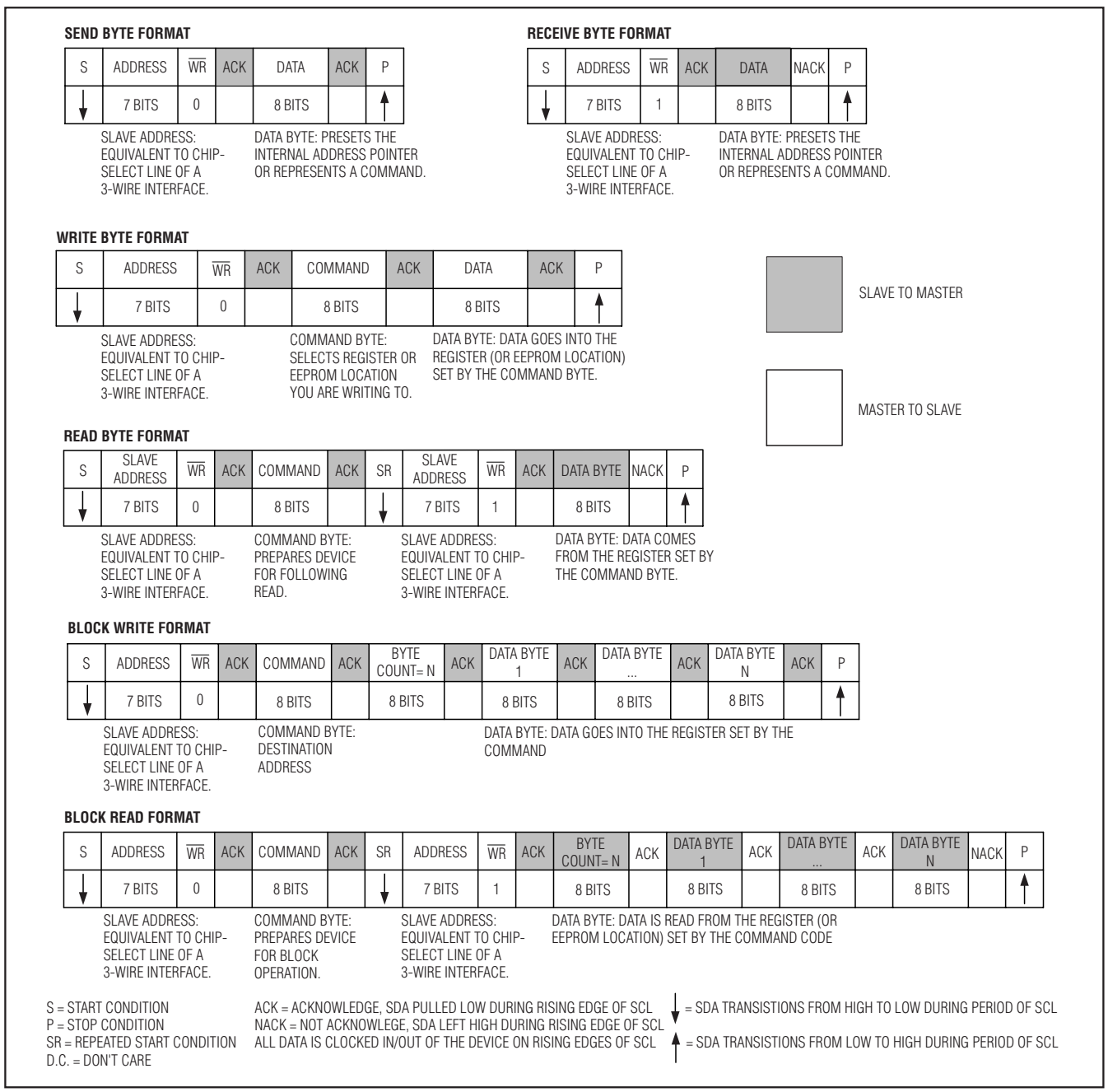

Figure 12. I²C/SMBus Protocols

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JTAG Serial Interface

The MAX16046/MAX16048 contain a JTAG port that complies with a subset of the IEEE® 1149.1 specification. Either the I²C or the JTAG interface may be used to access internal memory; however, only one interface is allowed to run at a time. The MAX16046/MAX16048 do not support IEEE 1149.1 boundary-scan functionality. The MAX16046/MAX16048 contain extra JTAG instructions and registers not included in the JTAG specification that provide access to internal memory. The extra instructions include LOAD ADDRESS, WRITE DATA, READ DATA, REBOOT, SAVE, and USERCODE.

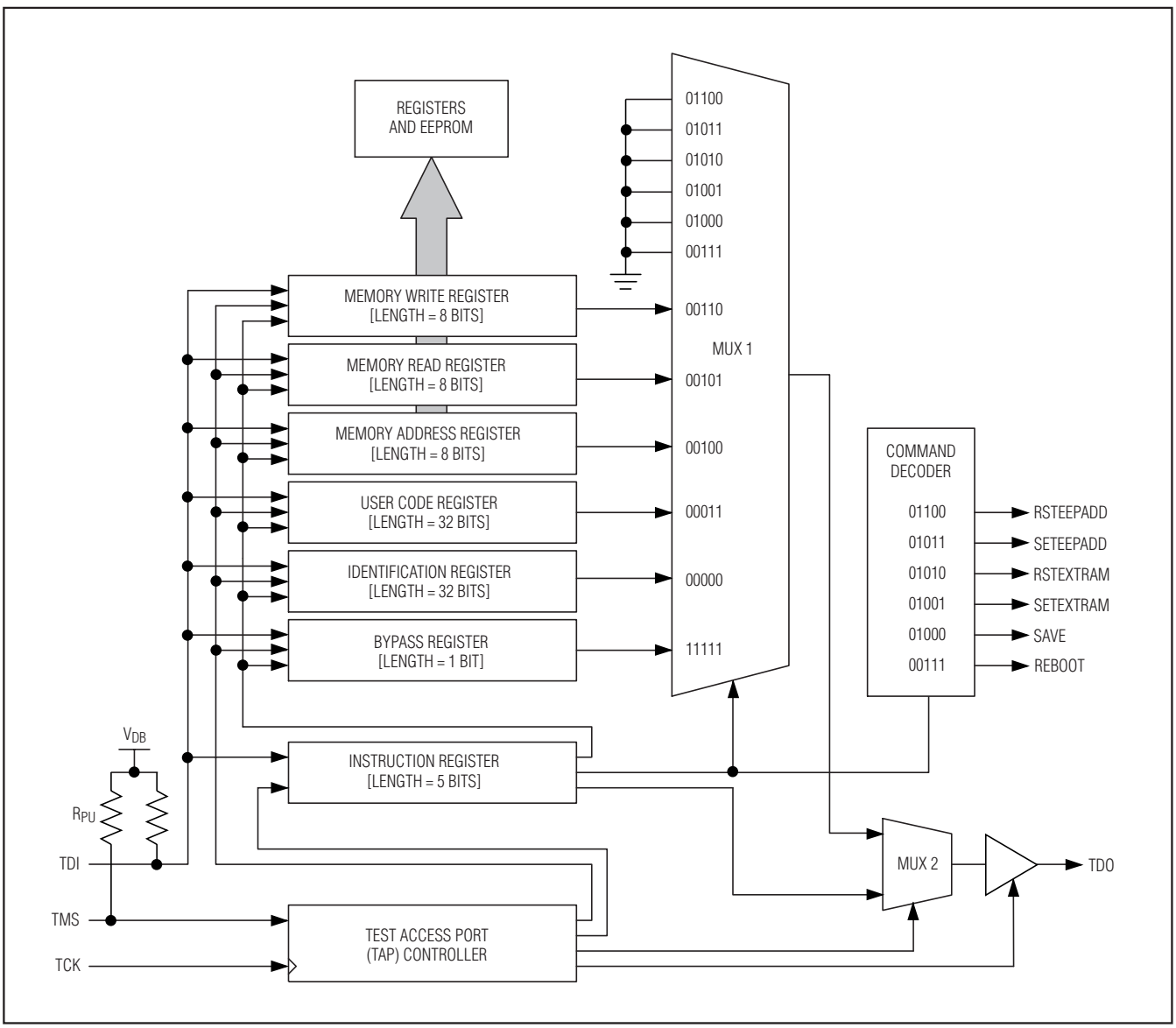

Figure 13. JTAG Block Diagram

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Test Access Port (TAP) Controller State Machine

The TAP controller is a finite state machine that responds to the logic level at TMS on the rising edge of TCK. See Figure 14 for a diagram of the finite state machine. The possible states are described below:

Test-Logic-Reset: At power-up, the TAP controller is in the test-logic-reset state. The instruction register contains the IDCODE instruction. All system logic of the device operates normally. This state can be reached from any state by driving TMS high for five clock cycles.

Run-Test/Idle: The run-test/idle state is used between scan operations or during specific tests. The instruction register and test data registers remain idle.

Select-DR-Scan: All test data registers retain their previous state. With TMS low, a rising edge of TCK moves the controller into the capture-DR state and initiates a scan sequence. TMS high during a rising edge on TCK moves the controller to the select-IR-scan state.

Capture-DR: Data can be parallel-loaded into the test data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected test data register does not allow parallel loads, the test data register remains at its current value. On the rising edge of TCK, the controller goes to the shift-DR state if TMS is low or it goes to the exit1-DR state if TMS is high.

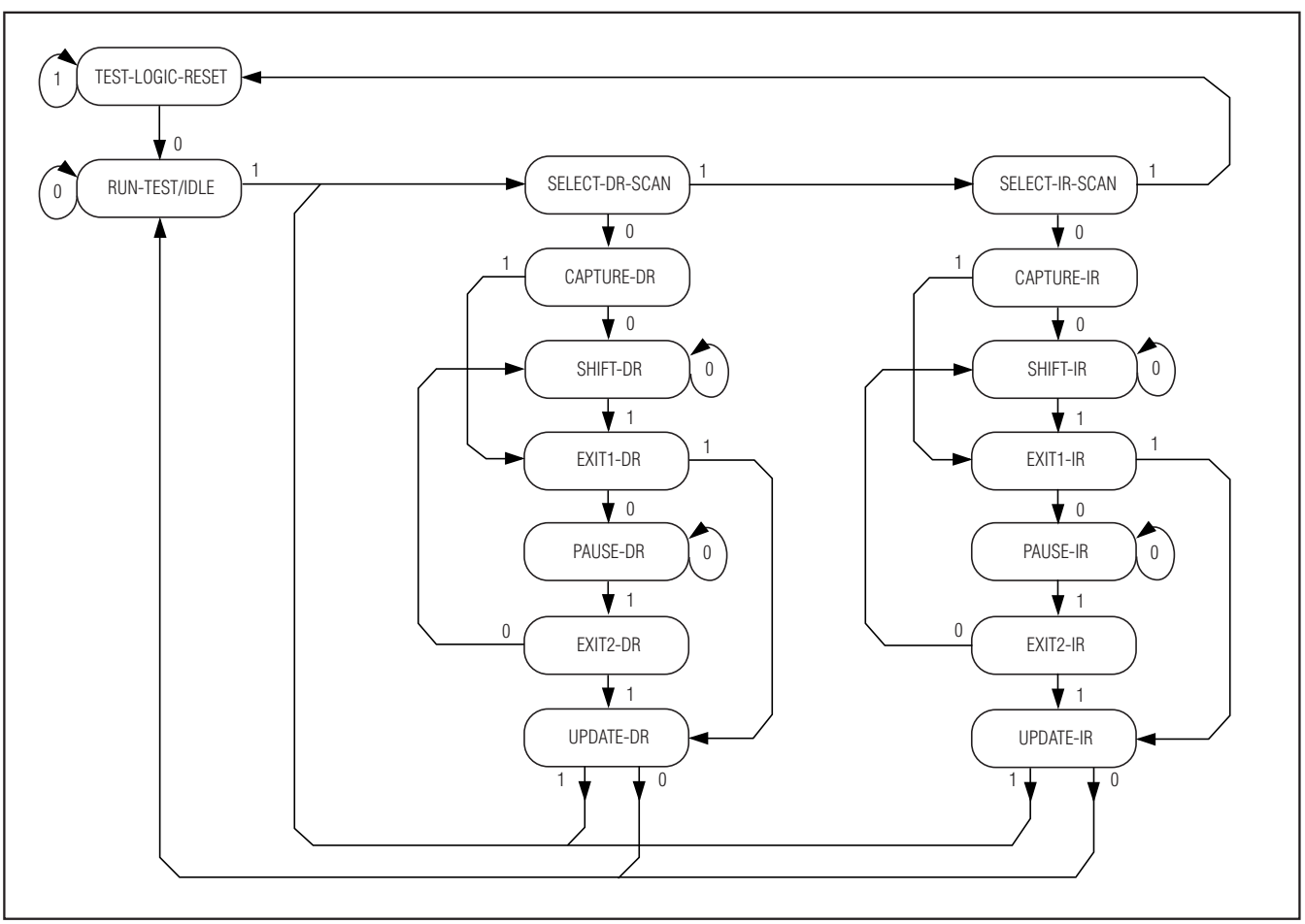

Figure 14. TAP Controller State Diagram

Shift-DR: The test data register selected by the current instruction connects between TDI and TDO and shifts data one stage toward its serial output on each rising edge of TCK while TMS is low. On the rising edge of TCK, the controller goes to the exit1-DR state if TMS is high.

Exit1-DR: While in this state, a rising edge on TCK puts the controller in the update-DR state. A rising edge on TCK with TMS low puts the controller in the pause-DR state.

Pause-DR: Shifting of the test data registers halts while in this state. All test data registers retain their previous state. The controller remains in this state while TMS is low. A rising edge on TCK with TMS high puts the controller in the exit2-DR state.

Exit2-DR: A rising edge on TCK with TMS high while in this state puts the controller in the update-DR state. A rising edge on TCK with TMS low enters the shift-DR state.

Update-DR: A falling edge on TCK while in the update-DR state latches the data from the shift register path of the test data registers into a set of output latches. This prevents changes at the parallel output because of changes in the shift register. On the rising edge of TCK, the controller goes to the run-test/idle state if TMS is low or goes to the select-DR-scan state if TMS is high.

Select-IR-Scan: All test data registers retain their previous states. The instruction register remains unchanged during this state. With TMS low, a rising edge on TCK moves the controller into the capture-IR state. TMS high during a rising edge on TCK puts the controller back into the test-logic-reset state.

Capture-IR: Use the capture-IR state to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of TCK. If TMS is high on the rising edge of TCK, the controller enters the exit1-IR state. If TMS is low on the rising edge of TCK, the controller enters the shift-IR state.

Shift-IR: In this state, the shift register in the instruction register connects between TDI and TDO and shifts data one stage for every rising edge of TCK toward the TDO serial output while TMS is low. The parallel outputs of the instruction register as well as all test data registers remain at their previous states. A rising edge on TCK with TMS high moves the controller to the exit1-IR state. A rising edge on TCK with TMS low keeps the controller in the shift-IR state while moving data one stage through the instruction shift register.

Exit1-IR: A rising edge on TCK with TMS low puts the controller in the pause-IR state. If TMS is high on the rising edge of TCK, the controller enters the update-IR state.

Pause-IR: Shifting of the instruction shift register halts temporarily. With TMS high, a rising edge on TCK puts the controller in the exit2-IR state. The controller remains in the pause-IR state if TMS is low during a rising edge on TCK.

Exit2-IR: A rising edge on TCK with TMS high puts the controller in the update-IR state. The controller loops back to shift-IR if TMS is low during a rising edge of TCK in this state.

Update-IR: The instruction code that has been shifted into the instruction shift register latches to the parallel outputs of the instruction register on the falling edge of TCK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on TCK with TMS low puts the controller in the run-test/idle state. With TMS high, the controller enters the select-DR-scan state.

Instruction Register

The instruction register contains a shift register as well as a latched parallel output and is 5 bits in length. When the TAP controller enters the shift-IR state, the instruction shift register connects between TDI and TDO. While in the shift-IR state, a rising edge on TCK with TMS low shifts the data one stage toward the serial output at TDO. A rising edge on TCK in the exit1-IR state or the exit2-IR state with TMS high moves the controller to the update-IR state. The falling edge of that same TCK latches the data in the instruction shift register to the instruction register parallel output. Instructions supported by the MAX16046/MAX16048 and the respective operational binary codes are shown in Table 33.

Table 33. JTAG Instruction Set

INSTRUCTION	HEX CODE	SELECTED REGISTER/ACTION
BYPASS	1Fh	Bypass. Mandatory instruction code.
IDCODE	00h	Manufacturer ID code and part number
USERCODE	03h	User code (user-defined ID)
LOAD ADDRESS	04h	Load address register content
READ DATA	05h	Memory read
WRITE DATA	06h	Memory write
REBOOT	07h	Resets the device
SAVE	08h	Stores current fault information in EEPROM
SETEXTRAM	09h	Extended page access on
RSTEXTRAM	0Ah	Extended page access off
SETEEPADD	0Bh	EEPROM page access on
RSTEEPADD	0Ch	EEPROM page access off

BYPASS: When the BYPASS instruction is latched into the instruction register, TDI connects to TDO through the 1-bit bypass test data register. This allows data to pass from TDI to TDO without affecting the device's normal operation.

IDCODE: When the IDCODE instruction is latched into the parallel instruction register, the identification data register is selected. The device identification code is loaded into the identification data register on the rising edge of TCK following entry into the capture-DR state. Shift-DR can be used to shift the identification code out serially through TDO. During test-logic-reset, the IDCODE instruction is forced into the instruction register. The identification code always has a '1' in the LSB position. The next 11 bits identify the manufacturer's JEDEC number and number of continuation bytes followed by 16 bits for the device and 4 bits for the version. See Table 34.

Table 34. 32-Bit Identification Code

MSB			LSB
Version (4 bits)	Device ID (16 bits)	Manufacturer ID (11 bits)	Fixed value (1 bit)
0000	0000000000000001	00011001011	1

USERCODE: When the USERCODE instruction latches into the parallel instruction register, the user-code data register is selected. The device user-code loads into the user-code data register on the rising edge of TCK following entry into the capture-DR state. Shift-DR can be used to shift the user-code out serially through TDO. See Table 35. This instruction may be used to help identify multiple MAX16046/MAX16048 devices connected in a JTAG chain.

Table 35. 32-Bit User-Code Data

MSB		LSB
D.C. (don't cares)	I^2C/SMBus slave address	User identification (firmware version)
00000000000000000	See Table 31	r5Ch[7:0] contents

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LOAD ADDRESS: This is an extension to the standard IEEE 1149.1 instruction set to support access to the memory in the MAX16046/MAX16048. When the LOAD ADDRESS instruction latches into the instruction register, TDI connects to TDO through the 8-bit memory address test data register during the shift-DR state.

READ DATA: This is an extension to the standard IEEE 1149.1 instruction set to support access to the memory in the MAX16046/MAX16048. When the READ DATA instruction latches into the instruction register, TDI connects to TDO through the 8-bit memory read test data register during the shift-DR state.

WRITE DATA: This is an extension to the standard IEEE 1149.1 instruction set to support access to the memory in the MAX16046/MAX16048. When the WRITE DATA instruction latches into the instruction register, TDI connects to TDO through the 8-bit memory write test data register during the shift-DR state.

REBOOT: This is an extension to the standard IEEE 1149.1 instruction set to initiate a software controlled reset to the MAX16046/MAX16048. When the REBOOT instruction latches into the instruction register, the MAX16046/MAX16048 resets and immediately begins the boot-up sequence.

SAVE: This is an extension to the standard IEEE 1149.1 instruction set that triggers a fault log. The current ADC conversion results along with fault information are saved to EEPROM depending on the configuration of the Critical Fault Log Control register (r47h).

SETEXTRAM: This is an extension to the standard IEEE 1149.1 instruction set that allows access to the extended page. Extended registers include ADC conversion results, DACOUT enables, and GPIO input/output data.

RSTEXTRAM: This is an extension to the standard IEEE 1149.1 instruction set. Use RSTEXTRAM to return to the default page and disable access to the extended page.

SETEEPADD: This is an extension to the standard IEEE 1149.1 instruction set that allows access to the EEPROM page. Once the SETEEPADD command has been sent, all addresses are recognized as EEPROM addresses only. When accessing any EEPROM location, set the address to the desired location, perform a dummy READ DATA operation, and then set the address back to the desired location. This primes the device for a subsequent series of READ DATA operations.

RSTEEPADD: This is an extension to the standard IEEE 1149.1 instruction set. Use RSTEEPADD to return to the default page and disable access to the EEPROM.

Applications Information

Unprogrammed Device Behavior

When the EEPROM has not been programmed using the JTAG or I^2C interface, the default configuration of the EN_OUT_ outputs is open-drain active-low. If it is necessary to hold an EN_OUT_ high or low to prevent premature startup of a power supply before the EEPROM is programmed, connect a resistor to ground or the supply voltage. Avoid connecting a resistor to ground if the output is to be configured as open-drain with a separate pullup resistor.

Device Behavior at Power-Up

When V_{CC} is ramped from 0V, the $\overline{RESET}$ output is high impedance until V_{CC} reaches 1.4V, at which point it is driven low. All other outputs are high impedance until V_{CC} reaches 2.85V, when the EEPROM contents are copied into register memory, and after which the outputs assume their programmed states.

Margining Power Supplies

The MAX16046/MAX16048 can margin or shift the voltages on external power supplies to facilitate prototyping or manufacturing tests. There are several different ways to margin power supplies: One method feeds a current into the feedback node of a DC-DC converter or LDO, and another method feeds a current into the trim input on a DC-DC module.

Feedback Method

See Figure 15 for the connections of the MAX16046/MAX16048 to a power supply using the feedback node method. The output voltage, V_{OUT}, can be calculated using the following formula:

$$V_{OUT} = V_{REF}\left(1+\frac{R_1}{R_3}+\frac{R_1}{R_2}\right)-\frac{R_1}{R_3}V_{DACOUT\_}$$

where V_{REF} is the internal reference voltage of the power supply and $V_{DACOUT\_}$ is the output voltage of the MAX16046/MAX16048 DACOUT_ output.

Select R_1 and R_2 to obtain the desired output voltage with no trim in effect ($V_{DACOUT\_} = V_{REF}$). Set the DAC range bits such that V_{REF} falls approximately halfway within the DACOUT_ output range (see the *DAC Outputs* section). The resistor, R_3, varies the amount of control that the DACOUT_ voltage has on the output voltage of the power supply. Large values of R_3 correspond to a higher degree of resolution control over the output voltage, and small values of R_3 correspond to a lesser degree of resolution control.

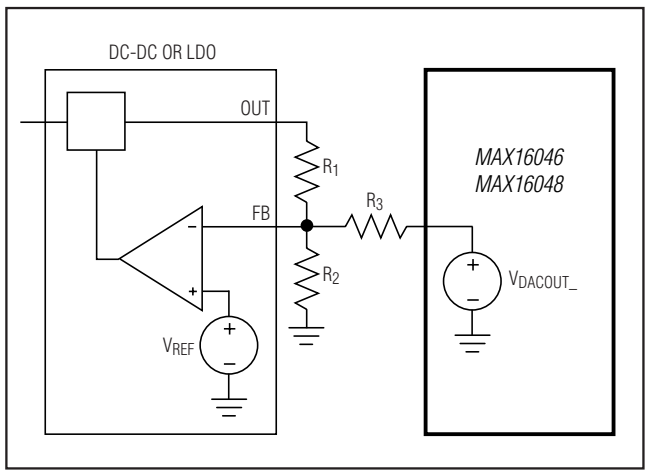

Figure 15. Connections for Margining Using Feedback Method

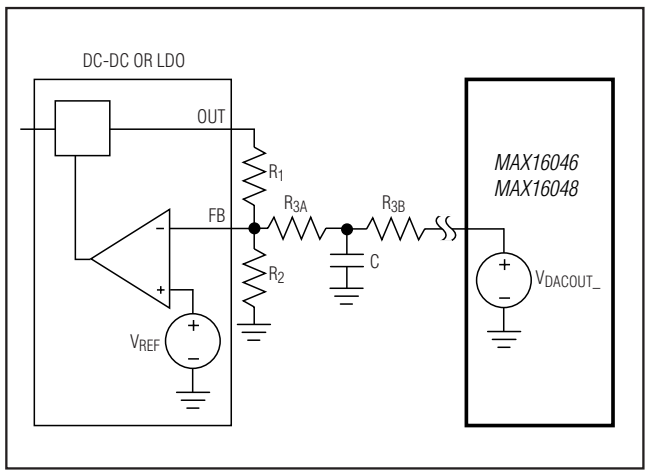

Figure 16. DACOUT Filter

Filtering the DAC Outputs

Some applications require filtering of the DAC outputs. This is especially necessary in applications that require a large distance between the power supplies to be margined and the MAX16046/MAX16048, or those that require immunity to noise. A simple RC filter may be inserted (see Figure 16).

The calculations change slightly for this configuration. For DC margining calculations, $R_3 = R_{3A} + R_{3B}$. To calculate the lowpass cutoff frequency, use the following formula:

$$f = \frac{1}{2\pi R_{3B} C}$$

Place resistor R_{3A} and the capacitor, C, as close as possible to the feedback node.

Trim Input Method

To connect the MAX16046/MAX16048 to a power supply using the trim input method, see Figure 17. Calculate the output voltage, V_{OUT}, as follows:

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right)\left(\frac{R_3 V_{DACOUT\_} + (R_4 + R_5)V_{REF}}{R_3 + R_4 + R_5}\right)$$

where V_{REF} is the reference voltage of the power supply; R_1, R_2, R_3, and R_4 are resistors internal to the power supply; R_5 is an optional series resistor connecting the trim input to the DACOUT_ output; and $V_{DACOUT\_}$ is the output voltage of the DACOUT_ output.

Calculate the ratio of R_1 and R_2 using the following formula:

$$\left(1 + \frac{R_1}{R_2}\right) = \frac{V_{OUT\_NOM}}{V_{REF}}$$

Resistors R_3 and R_4 and the reference voltage, V_{REF}, may be derived from the formulas given in the DC-DC converter data sheet where trim input functionality is discussed. DC-DC module data sheets usually include trim-up and trim-down formulas in the following form:

$$\text{TRIM DOWN:} R_{ADJ\_DOWN}(k\Omega) = \left(\frac{1-\Delta}{\Delta}\right) R_3(k\Omega) - R_4(k\Omega)$$

$$\text{TRIM UP:} R_{ADJ\_UP}(k\Omega) = \left(\frac{V_{OUT\_NOM}}{V_{REF}} - 1\right)\left(\frac{1-\Delta}{\Delta}\right) R_3(k\Omega) - R_4(k\Omega)$$

where Δ is the fraction of the total correction.

Another form of trim-up and trim-down formulas may appear as follows:

$$\text{TRIM DOWN:} R_{ADJ\_DOWN}(k\Omega) = \left(\frac{R_3(k\Omega) \times 100}{\Delta\%} - \left(R_4(k\Omega) + R_3(k\Omega)\right)\right)$$

$$\text{TRIM UP:} R_{ADJ\_UP}(k\Omega) = \left(\frac{V_{OUT\_NOM}\left(R_3(k\Omega) \times (100 + \Delta\%)\right)}{V_{REF}\Delta\%}\right) - \left(\frac{R_3(k\Omega) \times 100 + \left(R_4(k\Omega) + R_3(k\Omega)\right)\Delta\%}{\Delta\%}\right)$$

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Set the DACOUT_ range bits (see the *DAC Outputs* section) such that V_{REF} falls approximately halfway within the DACOUT range. Set R_5 to vary the amount of control the DAC has on the output voltage of the power supply. Large values of R_5 correspond to higher degree of resolution control over the output voltage, and small values of R_5 correspond to lesser degree of resolution control. Be sure to respect the minimum and maximum output voltages that the DC-DC converter is capable of generating.

The following is an example that illustrates the use of the formulas for calculating the margin up and margin down values. This example uses a generic 3.3V DC-DC converter with a trim input. Below are the margin up and margin down formulas taken from the data sheet for the power supply:

$$\text{TRIM DOWN:} R_{ADJ\_DOWN} = \left(\frac{100}{\Delta\%} - 2\right)(k\Omega)$$

$$\text{TRIM UP:} R_{ADJ\_UP} = \left(\frac{V_{OUT\_NOM}\,(100 + \Delta\%)}{1.225\Delta\%} - \frac{100 + 2\Delta\%}{\Delta\%}\right)(k\Omega)$$

By inspecting these formulas, V_{REF} = 1.225V, R_3 = 1kΩ, and R_4 = 1kΩ. Set the DACOUT_ range from 0.8V to 1.6V to fit the reference voltage. The output voltage of the DC-DC converter is 3.3V; therefore the ratio (1 + R_1/R_2) = V_{OUT}/V_{REF} = 3.3/1.225 = 2.69.

Set R_5 to zero to use the widest trim range possible (increase R_5 to decrease the trim range). Insert these values into the equations for the output voltage:

$$V_{OUT} = (2.69)\left(\frac{1k\Omega \times V_{DACOUT} + 1k\Omega \times 1.225}{2k\Omega}\right) = (2.69)\frac{\left(V_{DACOUT\_} + 1.225\right)}{2}$$

For $V_{DACOUT\_}$ = 0.8V, V_{OUT} = 2.72V, and for $V_{DACOUT\_}$ = 1.6V, V_{OUT} = 3.80V. These output voltages correspond with a margin down limit of -17.6% and a margin up limit of 15.2%. Since the reference voltage is not exactly in the center of the DACOUT_ range, the margin limits are not symmetrical. To decrease the margin limits, increase the value of R_5.

Maintaining Power During a Fault Condition

Power to the MAX16046/MAX16048 must be maintained for a specific period of time to ensure a successful EEPROM fault log operation during a fault that removes power to the circuit. The amount of time required depends on the settings in the fault control register (r47h[1:0]) according to Table 36.

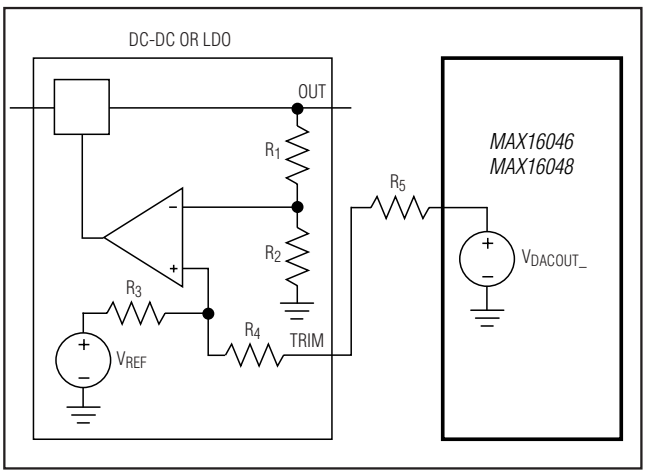

Figure 17. Connections for Margining Using Trim Input Method

Table 36. EEPROM Fault Log Operation Period

FAULT CONTROL REGISTER VALUE r47h[1:0]	DESCRIPTION	REQUIRED PERIOD t_{FAULT_SAVE} (ms)
00	Failed lines and ADC values saved	204
01	Failed lines saved	60
10	ADC values saved	168
11	No information saved	—

Maintain power for shutdown during fault conditions in applications where the always-on power supply cannot be relied upon by placing a diode and a large capacitor between the voltage source, V_{IN}, and V_{CC} (Figure 18). The capacitor value depends on V_{IN} and the time delay required, t_{FAULT_SAVE}. Use the following formula to calculate the capacitor size:

$$C = \frac{t_{FAULT\_SAVE} \times I_{CC(MAX)}}{V_{IN} - V_{DIODE} - V_{UVLO}}$$

where the capacitance is in Farads and t_{FAULT_SAVE} is in seconds. $I_{CC(MAX)}$ is 6.5mA, V_{DIODE} is the voltage drop across the diode, and V_{UVLO} is 2.85V. For example, with a V_{IN} of 14V, a diode drop of 0.7V, and a t_{FAULT_SAVE} of 0.204s, the minimum required capacitance is 127µF.

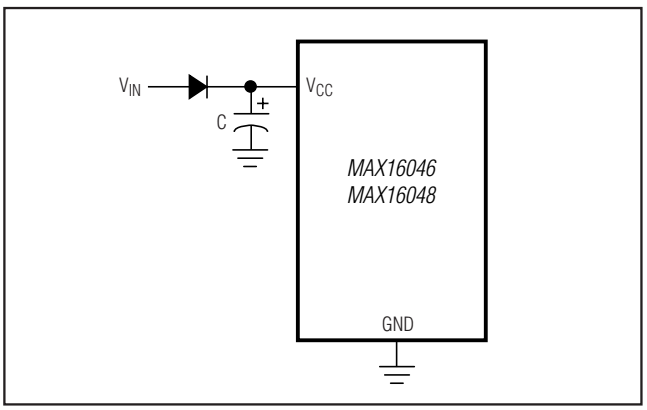

Figure 18. Power Circuit for Shutdown During Fault Conditions

Driving High-Side MOSFET Switches

The MAX16046/MAX16048 use external n-channel MOSFET switches for voltage tracking applications. To configure the part for closed-loop voltage tracking using series-pass MOSFETs, configure up to four of the programmable outputs (EN_OUT1–EN_OUT4) of the MAX16046/MAX16048 as closed-loop tracking outputs and configure up to four of the GPIOs as sense-return inputs (INS1–INS4). Connect the EN_OUT_ output to the gate of an n-channel MOSFET, connect the source of the MOSFET to the INS_ feedback input, and monitor the drain side of the MOSFET with the corresponding MON_ input (see Figure 19). Both the input and the output must be assigned to the same slot (see the *Closed–Loop Tracking* section). Configure the power-up and power-down slew rates in the configuration registers. To provide additional control over power-down, enable the internal 100Ω pulldown resistors on the INS_ connections.

Up to six of the programmable outputs (EN_OUT1–EN_OUT6) of the MAX16046/MAX16048 may be configured as charge-pump outputs. In this case, they can drive the gates of series-pass n-channel MOSFETs without closed-loop tracking functionality. When configured in this way, these outputs act as simple power switches to turn on the voltage supply rails. Approximate the slew rate, SR, using the following formula:

$$SR = \frac{I_{CP}}{(C_{GATE} + C_{EXT})}$$

where I_{CP} is the 6µA (typ) charge-pump source current, C_{GATE} is the gate capacitance of the MOSFET, and C_{EXT} is the capacitance connected from the gate to ground. Power-down is not well controlled due to the absence of the 100Ω pulldowns.

If more than six series-pass MOSFETs are required for an application, additional series-pass p-channel MOSFETS may be connected to outputs configured as active-low open drain (Figure 20). Connect a pullup resistor from the gate to the source of the MOSFET and ensure the absolute maximum ratings of the MAX16046/MAX16048 are not exceeded.

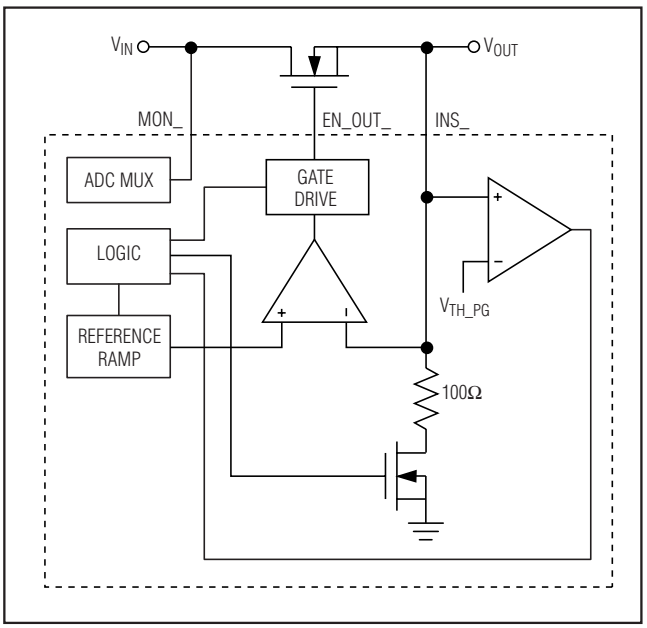

Figure 19. Closed-Loop Tracking

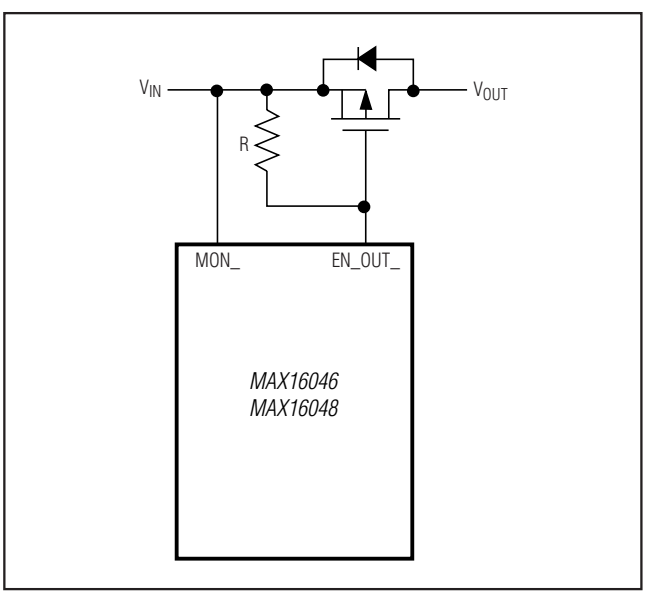

Figure 20. Connection for a p-Channel Series-Pass MOSFET

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Simple slew-rate control is accomplished by adding a capacitor from the gate to ground. The slew rate is approximated by the RC charge curve of the pullup resistor acting with the capacitor from gate to ground. Note that the power-off is not well controlled due to the absence of the 100Ω pulldowns.

Ensure that MOSFETs have a low gate-to-source threshold (V_{GS_TH}) and $R_{DS(ON)}$. See Table 37 for recommended n-channel MOSFETs.

Layout and Bypassing

Bypass DBP and ABP each with a 1µF ceramic capacitor to GND. Bypass V_{CC} with a 10µF capacitor to ground. Avoid routing digital return currents through a sensitive analog area, such as an analog supply input return path or ABP's bypass capacitor ground connection. Use dedicated analog and digital ground planes. Connect the capacitors as close as possible to the device.

Table 37. Recommended MOSFETs

MANUFACTURER	PART	MAX V_{DS} (V)	V_{GS_TH} (V)	$R_{DS(ON)}$ AT V_{GS} = 4.5V (mΩ)	I_{MAX} AT 50mV VOLTAGE DROP (A)	Q_g (typ) (nC)	PACKAGE
Fairchild	FDC633N	30	0.67	42	1.19	11	Super SOT-6
	FDP8030L FDB8030L	30	1.5	4.5	11.11	120	TO-220 TO-263AB
	FDD6672A	30	1.2	9.5	5.26	33	TO-252
	FDS8876	30	2.5	10.2	2.94	15	SO-8
Vishay	Si7136DP	20	3	4.5	11.11	24.5	SO-8
	Si4872DY	30	1	10	5	27	SO-8
	SUD50N02-09P	20	3	17	2.94	10.5	TO-252
	Si1488DH	20	0.95	49	1.02	6	SOT-363 SC70-6
International Rectifier	IRL3716	20	3	4.8	10.4	53	TO220AB D^2PAK TO-262
	IRL3402	20	0.7	10	5	78 (max)	TO220AB
	IRL3715Z	20	2.1	15.5	3.22	7	TO220AB D^2PAK TO-262
	IRLM2502	20	1.2	45	1.11	8	SOT23-3 Micro3

Register Map

PAGE	ADDRESS	READ/WRITE	DESCRIPTION
Ext	00h	R	MON1 ADC Result Register (MSB)
Ext	01h	R	MON1 ADC Result Register (LSB)
Ext	02h	R	MON2 ADC Result Register (MSB)
Ext	03h	R	MON2 ADC Result Register (LSB)
Ext	04h	R	MON3 ADC Result Register (MSB)
Ext	05h	R	MON3 ADC Result Register (LSB)
Ext	06h	R	MON4 ADC Result Register (MSB)
Ext	07h	R	MON4 ADC Result Register (LSB)
Ext	08h	R	MON5 ADC Result Register (MSB)
Ext	09h	R	MON5 ADC Result Register (LSB)
Ext	0Ah	R	MON6 ADC Result Register (MSB)
Ext	0Bh	R	MON6 ADC Result Register (LSB)
Ext	0Ch	R	MON7 ADC Result Register (MSB)
Ext	0Dh	R	MON7 ADC Result Register (LSB)
Ext	0Eh	R	MON8 ADC Result Register (MSB)
Ext	0Fh	R	MON8 ADC Result Register (LSB)
Ext	10h	R	MON9 ADC Result Register (MSB)*
Ext	11h	R	MON9 ADC Result Register (LSB)*
Ext	12h	R	MON10 ADC Result Register (MSB)*
Ext	13h	R	MON10 ADC Result Register (LSB)*
Ext	14h	R	MON11 ADC Result Register (MSB)*
Ext	15h	R	MON11 ADC Result Register (LSB)*
Ext	16h	R	MON12 ADC Result Register (MSB)*
Ext	17h	R	MON12 ADC Result Register (LSB)*
Ext	18h	R/W	Fault Register—Failed Line Flags
Ext	19h	R/W	Fault Register—Failed Line Flags
Ext	1Ah	R/W	GPIO Data Out
Ext	1Bh	R	GPIO Data In
Ext	1Ch	R/W	DAC Enables
Ext	1Dh	R/W	DAC Enables
Default	00h	R/W	DACOUT1
Default	01h	R/W	DACOUT2
Default	02h	R/W	DACOUT3
Default	03h	R/W	DACOUT4
Default	04h	R/W	DACOUT5
Default	05h	R/W	DACOUT6
Default	06h	R/W	DACOUT7
Default	07h	R/W	DACOUT8
Default	08h	R/W	DACOUT9*
Default	09h	R/W	DACOUT10*

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Register Map (continued)

PAGE	ADDRESS	READ/WRITE	DESCRIPTION
Default	0Ah	R/W	DACOUT11*
Default	0Bh	R/W	DACOUT12*
EEPROM	00h	R/W	Power-Up Fault Registers
EEPROM	01h	R/W	Failed Line Flags (Fault Registers)
EEPROM	02h	R/W	Failed Line Flags (Fault Registers)
EEPROM	03h	R/W	MON1 Conversion Result at Time of Fault
EEPROM	04h	R/W	MON2 Conversion Result at Time of Fault
EEPROM	05h	R/W	MON3 Conversion Result at Time of Fault
EEPROM	06h	R/W	MON4 Conversion Result at Time of Fault
EEPROM	07h	R/W	MON5 Conversion Result at Time of Fault
EEPROM	08h	R/W	MON6 Conversion Result at Time of Fault
EEPROM	09h	R/W	MON7 Conversion Result at Time of Fault
EEPROM	0Ah	R/W	MON8 Conversion Result at Time of Fault
EEPROM	0Bh	R/W	MON9 Conversion Result at Time of Fault*
EEPROM	0Ch	R/W	MON10 Conversion Result at Time of Fault*
EEPROM	0Dh	R/W	MON11 Conversion Result at Time of Fault*
EEPROM	0Eh	R/W	MON12 Conversion Result at Time of Fault*
Def/EE	0Fh	R/W	ADC MON4–MON1 Voltage Ranges
Def/EE	10h	R/W	ADC MON8–MON5 Voltage Ranges
Def/EE	11h	R/W	ADC MON12–MON9 Voltage Ranges*
Def/EE	12h	R/W	DACOUT4–DACOUT1 Voltage Ranges
Def/EE	13h	R/W	DACOUT8–DACOUT5 Voltage Ranges
Def/EE	14h	R/W	DACOUT12–DACOUT9 Voltage Ranges*
Def/EE	15h	R/W	$\overline{\text{FAULT1}}$ Dependencies
Def/EE	16h	R/W	$\overline{\text{FAULT1}}$ Dependencies
Def/EE	17h	R/W	$\overline{\text{FAULT2}}$ Dependencies
Def/EE	18h	R/W	$\overline{\text{FAULT2}}$ Dependencies
Def/EE	19h	R/W	$\overline{\text{RESET}}$ Output Configuration
Def/EE	1Ah	R/W	$\overline{\text{RESET}}$ Output Dependencies
Def/EE	1Bh	R/W	$\overline{\text{RESET}}$ Output Dependencies
Def/EE	1Ch	R/W	GPIO Configuration
Def/EE	1Dh	R/W	GPIO Configuration
Def/EE	1Eh	R/W	GPIO Configuration
Def/EE	1Fh	R/W	EN_OUT1–EN_OUT3 Output Configuration
Def/EE	20h	R/W	EN_OUT3–EN_OUT6 Output Configuration
Def/EE	21h	R/W	EN_OUT6–EN_OUT9 Output Configuration*
Def/EE	22h	R/W	EN_OUT10–EN_OUT12 Output Configuration*
Def/EE	23h	R/W	MON1 Early Warning Threshold
Def/EE	24h	R/W	MON1 Overvoltage Threshold
Def/EE	25h	R/W	MON1 Undervoltage Threshold

Register Map (continued)

PAGE	ADDRESS	READ/WRITE	DESCRIPTION
Def/EE	26h	R/W	MON2 Early Warning Threshold
Def/EE	27h	R/W	MON2 Overvoltage Threshold
Def/EE	28h	R/W	MON2 Undervoltage Threshold
Def/EE	29h	R/W	MON3 Early Warning Threshold
Def/EE	2Ah	R/W	MON3 Overvoltage Threshold
Def/EE	2Bh	R/W	MON3 Undervoltage Threshold
Def/EE	2Ch	R/W	MON4 Early Warning Threshold
Def/EE	2Dh	R/W	MON4 Overvoltage Threshold
Def/EE	2Eh	R/W	MON4 Undervoltage Threshold
Def/EE	2Fh	R/W	MON5 Early Warning Threshold
Def/EE	30h	R/W	MON5 Overvoltage Threshold
Def/EE	31h	R/W	MON5 Undervoltage Threshold
Def/EE	32h	R/W	MON6 Early Warning Threshold
Def/EE	33h	R/W	MON6 Overvoltage Threshold
Def/EE	34h	R/W	MON6 Undervoltage Threshold
Def/EE	35h	R/W	MON7 Early Warning Threshold
Def/EE	36h	R/W	MON7 Overvoltage Threshold
Def/EE	37h	R/W	MON7 Undervoltage Threshold
Def/EE	38h	R/W	MON8 Early Warning Threshold
Def/EE	39h	R/W	MON8 Overvoltage Threshold
Def/EE	3Ah	R/W	MON8 Undervoltage Threshold
Def/EE	3Bh	R/W	MON9 Early Warning Threshold*
Def/EE	3Ch	R/W	MON9 Overvoltage Threshold*
Def/EE	3Dh	R/W	MON9 Undervoltage Threshold*
Def/EE	3Eh	R/W	MON10 Early Warning Threshold*
Def/EE	3Fh	R/W	MON10 Overvoltage Threshold*
Def/EE	40h	R/W	MON10 Undervoltage Threshold*
Def/EE	41h	R/W	MON11 Early Warning Threshold*
Def/EE	42h	R/W	MON11 Overvoltage Threshold*
Def/EE	43h	R/W	MON11 Undervoltage Threshold*
Def/EE	44h	R/W	MON12 Early Warning Threshold*
Def/EE	45h	R/W	MON12 Overvoltage Threshold*
Def/EE	46h	R/W	MON12 Undervoltage Threshold*
Def/EE	47h	R/W	Fault Control
Def/EE	48h	R/W	Faults Causing Emergency EEPROM Save
Def/EE	49h	R/W	Faults Causing Emergency EEPROM Save
Def/EE	4Ah	R/W	Faults Causing Emergency EEPROM Save
Def/EE	4Bh	R/W	Faults Causing Emergency EEPROM Save
Def/EE	4Ch	R/W	Faults Causing Emergency EEPROM Save
Def/EE	4Dh	R/W	$\overline{\text{Software Enable}}$/MARGIN

Register Map (continued)

PAGE	ADDRESS	READ/WRITE	DESCRIPTION
Def/EE	4Eh	R/W	Power-Up/Power-Down Pulldown Resistors
Def/EE	4Fh	R/W	Autoretry, Slew Rate, and ADC Fault Deglitch
Def/EE	50h	R/W	Sequence Delays
Def/EE	51h	R/W	Sequence Delays
Def/EE	52h	R/W	Sequence Delays
Def/EE	53h	R/W	Sequence Delays
Def/EE	54h	R/W	Sequence Delays/Reverse Sequence Bit
Def/EE	55h	R/W	Watchdog Timer Setup
Def/EE	56h	R/W	MON2–MON1 Slot Assignment from Slot 1 to Slot 12
Def/EE	57h	R/W	MON4–MON3 Slot Assignment from Slot 1 to Slot 12
Def/EE	58h	R/W	MON6–MON5 Slot Assignment from Slot 1 to Slot 12
Def/EE	59h	R/W	MON8–MON7 Slot Assignment from Slot 1 to Slot 12
Def/EE	5Ah	R/W	MON10–MON9 Slot Assignment from Slot 1 to Slot 12*
Def/EE	5Bh	R/W	MON12–MON11 Slot Assignment from Slot 1 to Slot 12*
Def/EE	5Ch	R/W	Customer Firmware Version
Def/EE	5Dh	R/W	EEPROM and Configuration Lock
Def/EE	5Eh	R/W	EN_OUT2–EN_OUT1 Slot Assignment from Slot 0 to Slot 11
Def/EE	5Fh	R/W	EN_OUT4–EN_OUT2 Slot Assignment from Slot 0 to Slot 11
Def/EE	60h	R/W	EN_OUT6–EN_OUT5 Slot Assignment from Slot 0 to Slot 11
Def/EE	61h	R/W	EN_OUT8–EN_OUT7 Slot Assignment from Slot 0 to Slot 11
Def/EE	62h	R/W	EN_OUT10–EN_OUT9 Slot Assignment from Slot 0 to Slot 11*
Def/EE	63h	R/W	EN_OUT12–EN_OUT11 Slot Assignment from Slot 0 to Slot 11*
Def/EE	64h	R/W	INS Power-Good (PG) Thresholds
Def/EE	65h	R	Manufacturing Revision Code
Def/EE	66h	R/W	DACOUT1—MARGIN UP
Def/EE	67h	R/W	DACOUT2—MARGIN UP
Def/EE	68h	R/W	DACOUT3—MARGIN UP
Def/EE	69h	R/W	DACOUT4—MARGIN UP
Def/EE	6Ah	R/W	DACOUT5—MARGIN UP
Def/EE	6Bh	R/W	DACOUT6—MARGIN UP
Def/EE	6Ch	R/W	DACOUT7—MARGIN UP
Def/EE	6Dh	R/W	DACOUT8—MARGIN UP
Def/EE	6Eh	R/W	DACOUT9—MARGIN UP*
Def/EE	6Fh	R/W	DACOUT10—MARGIN UP*
Def/EE	70h	R/W	DACOUT11—MARGIN UP*
Def/EE	71h	R/W	DACOUT12—MARGIN UP*
Def/EE	72h	R/W	DACOUT1—MARGIN DN
Def/EE	73h	R/W	DACOUT2—MARGIN DN
Def/EE	74h	R/W	DACOUT3—MARGIN DN
Def/EE	75h	R/W	DACOUT4—MARGIN DN

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Register Map (continued)

PAGE	ADDRESS	READ/WRITE	DESCRIPTION
Def/EE	76h	R/W	DACOUT5—MARGIN DN
Def/EE	77h	R/W	DACOUT6—MARGIN DN
Def/EE	78h	R/W	DACOUT7—MARGIN DN
Def/EE	79h	R/W	DACOUT8—MARGIN DN
Def/EE	7Ah	R/W	DACOUT9—MARGIN DN*
Def/EE	7Bh	R/W	DACOUT10—MARGIN DN*
Def/EE	7Ch	R/W	DACOUT11—MARGIN DN*
Def/EE	7Dh	R/W	DACOUT12—MARGIN DN*
Def/EE	7Eh–93h	—	Reserved
EEPROM	9Ch–FFh	R/W	User EEPROM

**MAX16046 only*

Note: *Ext refers to registers contained in the extended page, Default refers to registers contained in the default page, EEPROM refers to EEPROM memory locations, and Def/EE refers to locations that are stored in EEPROM and loaded into the same addresses in the default page on boot-up.*

Chip Information

PROCESS: BiCMOS

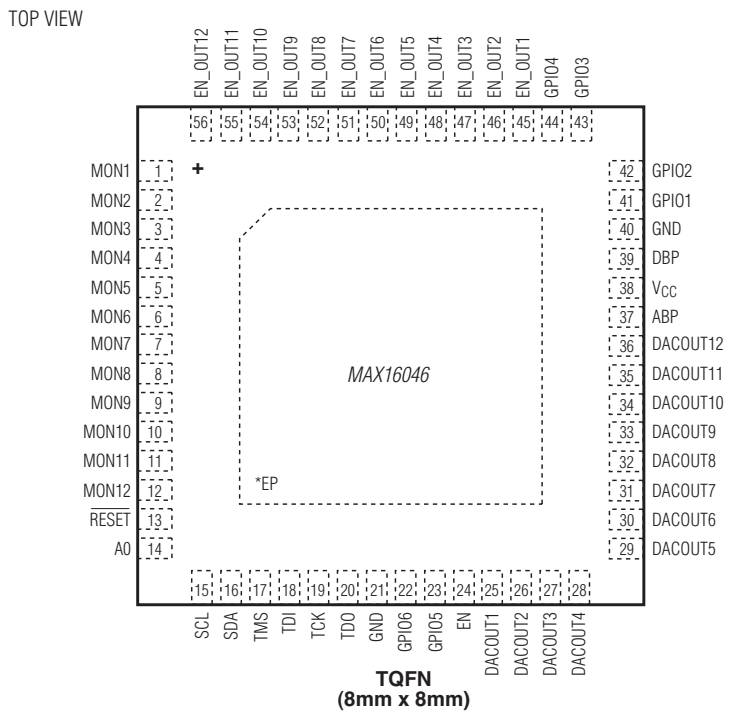
Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

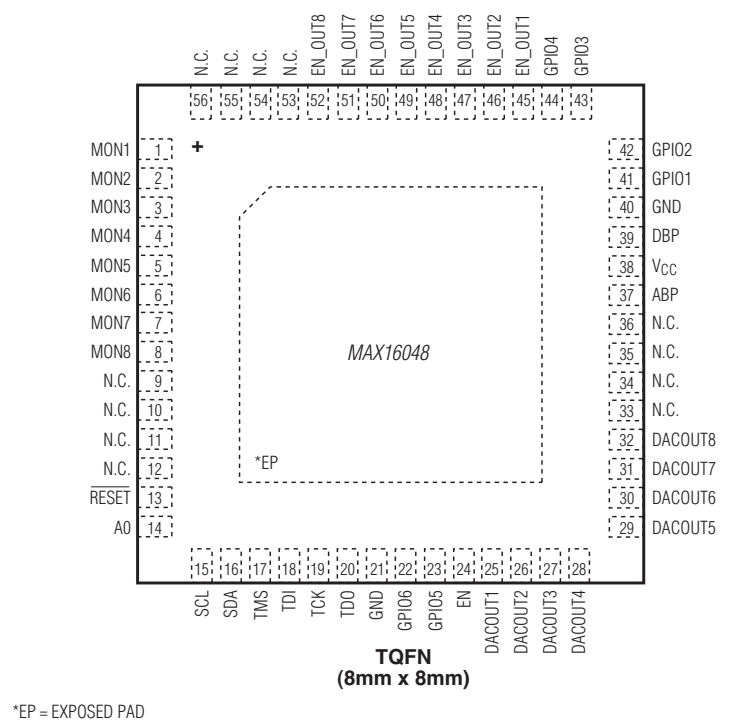
PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
56 TQFN	T5688-3	21-0135	90-0047
64 TQFP	C64E+6	21-0084	90-0328

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Pin Configurations



TQFN
(8mm x 8mm)

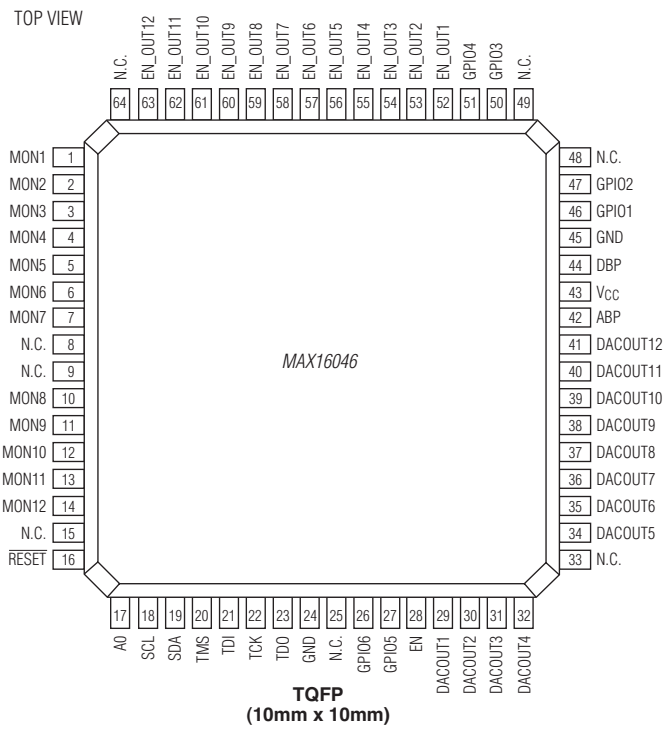


TQFN
(8mm x 8mm)

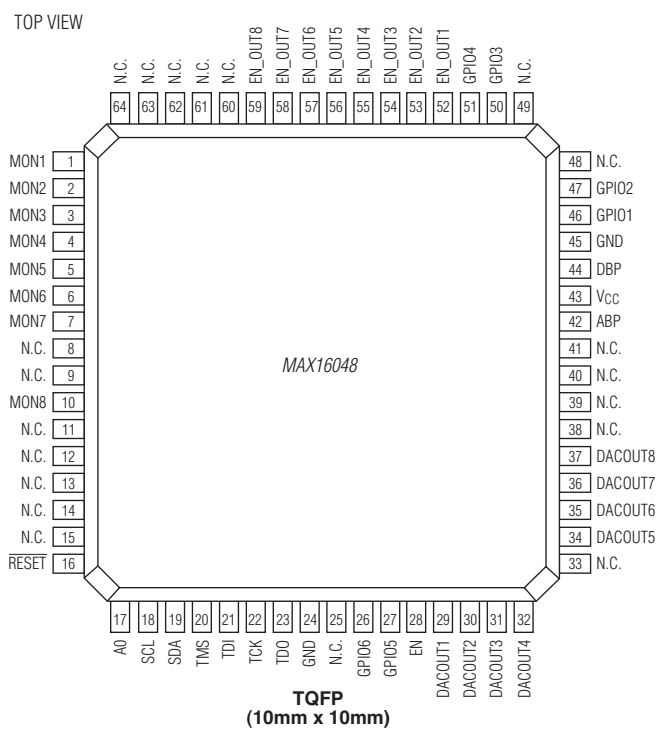
*EP = EXPOSED PAD

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Pin Configurations (continued)



TQFP
(10mm x 10mm)



TQFP
(10mm x 10mm)

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/07	Initial release	—
1	2/08	Removed future product designation in the *Ordering Information* table and updated *Package Information*	1, 67, 68
2	4/08	Added TQFP package to the data sheet and updated the *General Description*, *Ordering Information*, *Features*, *Absolute Maximum Ratings*, *Pin Description*, *Pin Configuration*, and *Selector Guide*	1, 2, 11, 12, 65, 66, 67
3	12/08	Updated *Pin Descriptions*, *Register Summary (All Registers 8-Bits Wide)* section, and *Revision History*	14, 16, 70
4	3/09	Updated *Detailed Description*, Table 30 and Table 31	17, 29, 30, 39, 43, 44, 48, 50
5	9/10	Updated *Electrical Characteristics* table, added text to the *Command Codes* and *Instruction Register* sections, style edits, updated *Package Information*	3, 6, 14, 52, 53, 58, 67
6	5/12	Updated *Electrical Characteristics* table	5

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