# **General Description**

The MAX9389 is a fully differential, high-speed, low-jitter, 8-to-1 ECL/PECL multiplexer (mux) with dual output buffers. The device is designed for clock and data distribution applications, and features extremely low propagation delay (310ps typ) and output-to-output skew (30ps max).

Three single-ended select inputs, SEL0, SEL1, and SEL2, control the mux function. The mux select inputs are compatible with ECL/PECL logic, and are internally referenced to the on-chip reference output (V<sub>BB1</sub>, V<sub>BB2</sub>), nominally V<sub>CC</sub> - 1.425V. The select inputs accept signals between V<sub>CC</sub> and V<sub>EE</sub>. Internal pulldowns to V<sub>EE</sub> ensure a low default condition if the select inputs are left open.

The differential inputs D\_,  $\overline{D}$  can be configured to accept a single-ended signal when the unused complementary input is connected to the on-chip reference output (V<sub>BB1</sub>, V<sub>BB2</sub>). All the differential inputs have internal bias and clamping circuits that ensure a low output state when the inputs are left open.

The MAX9389 operates with a wide supply range V<sub>CC</sub> - V<sub>EE</sub> of 2.375V to 5.5V. The device is offered in 32-pin TQFP and thin QFN packages, and operates over the -40°C to +85°C extended temperature range.

### Applications

High-Speed Telecom and Datacom Applications Central-Office Backplane Clock Distribution DSLAM/DLC



### Pin Configurations

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\_\_Features

- ♦ 310ps Propagation Delay
- Guaranteed 2.7GHz Operating Frequency
- 0.3ps<sub>RMS</sub> Random Jitter
- <30ps Output-to-Output Skew</p>
- -2.375V to -5.5V Supplies for Differential LVECL/ECL
- +2.375V to +5.5V Supplies for Differential LVPECL/PECL
- Outputs Low for Open Inputs
- Dual Output Buffers
- >2kV ESD Protection (Human Body Model)

## **\_Ordering Information**

PART	TEMP RANGE	PIN-PACKAGE
MAX9389EHJ	-40°C to +85°C	32 TQFP
MAX9389ETJ*	-40°C to +85°C	32 Thin QFN

\*Future product—contact factory for availability.

# \_Functional Diagram



\_\_\_\_\_ Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

### **ABSOLUTE MAXIMUM RATINGS**

	$0.2$ \/ to $1.6.0$ \/
VCC - VEE	0.3V 10 +0.0V
Inputs (D_, D_, SEL_) to V <sub>EE</sub>	-0.3V to (V <sub>CC</sub> + 0.3V)
D_ to D	±3.0V
Continuous Output Current	50mA
Surge Output Current	100mA
VBB_ Sink/Source Current	±600µA
Continuous Power Dissipation (T <sub>A</sub> = +70°C	;) ;)
32-Lead TQFP (derate 13.1mW/°C abov	/e +70°C)1047mW
θ <sub>JA</sub> in Still Air	+76°C/W
өјс	+25°C/W

32-Lead QFN (derate 21.3mW/°C above	e +70°C)1702mW
θ. <sub>IA</sub> in Still Air	+47°C/W
θJC	+2°C/W
Operating Temperature Range	40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
ESD Protection	
Human Body Model (D_, D_, Q_, Q_, SEL_, Soldering Temperature (10s)	V <sub>BB</sub> _)≥2kV +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# DC ELECTRICAL CHARACTERISTICS

 $(V_{CC} - V_{EE} = 2.375V \text{ to } 5.5V, \text{ outputs loaded with } 50\Omega \pm 1\% \text{ to } V_{CC} - 2V. \text{ Typical values are at } V_{CC} - V_{EE} = 3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, \text{ unless otherwise noted.})$  (Notes 1–4)

		CONDITIONS			-40°C			+25°C			+85°C		
PARAMETER	STNDUL	CON	DITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	ТҮР	MAX	
INPUT (D_, D_, SE	EL_)												
Single-Ended Input High Voltage	VIH	V <sub>BB</sub> _ con unused in	nected to the put, Figure 1	V <sub>CC</sub> - 1.225		V <sub>CC</sub> - 0.880	V <sub>CC</sub> - 1.225		V <sub>CC</sub> - 0.880	V <sub>CC</sub> - 1.225		V <sub>CC</sub> - 0.880	V
Single-Ended Input Low Voltage	VIL	V <sub>BB</sub> _ con unused in	nected to the put, Figure 1	V <sub>CC</sub> - 1.945		V <sub>CC</sub> - 1.625	V <sub>CC</sub> - 1.945		V <sub>CC</sub> - 1.625	V <sub>CC</sub> - 1.945		V <sub>CC</sub> - 1.625	V
Differential Input High Voltage	VIHD	Figure 1		V <sub>EE</sub> + 1.2		V <sub>CC</sub>	V <sub>EE</sub> + 1.2		V <sub>CC</sub>	V <sub>EE</sub> + 1.2		V <sub>CC</sub>	V
Differential Input Low Voltage	V <sub>ILD</sub>	Figure 1		$V_{EE}$		V <sub>CC</sub> - 0.095	$V_{EE}$		V <sub>CC</sub> - 0.095	VEE		V <sub>CC</sub> - 0.095	V
Differential Input	V <sub>IHD</sub> -	Eiguro 1	V <sub>CC</sub> - V <sub>EE</sub> < 3.0V	0.095		V <sub>CC</sub> - V <sub>EE</sub>	0.095		V <sub>CC</sub> - V <sub>EE</sub>	0.095		V <sub>CC</sub> - V <sub>EE</sub>	V
Voltage	VILD	LD Figure 1	V <sub>CC</sub> - V <sub>EE</sub> ≥ 3.0V	0.095		3.000	0.095		3.000	0.095		3.000	V
Input Current	lin	VIH, VIL, V	ihd, Vild	-60		+60	-60		+60	-60		+60	μΑ
OUTPUT ( $Q_{,} \overline{Q_{}}$ )													
Single-Ended Output High Voltage	Vон	Figure 2		V <sub>CC</sub> - 1.145		V <sub>CC</sub> - 0.895	V <sub>CC</sub> - 1.145		V <sub>CC</sub> - 0.895	V <sub>CC</sub> - 1.145		V <sub>CC</sub> - 0.895	V

MAX9389

# DC ELECTRICAL CHARACTERISTICS (continued)

 $(V_{CC} - V_{EE} = 2.375V \text{ to } 5.5V, \text{ outputs loaded with } 50\Omega \pm 1\% \text{ to } V_{CC} - 2V. \text{ Typical values are at } V_{CC} - V_{EE} = 3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, \text{ unless otherwise noted.}) (Notes 1–4)$ 

				-40°C			+25°C			+85°C		
FARAMETER	STMBOL	CONDITIONS	MIN	ТҮР	MAX	MIN	ТҮР	MAX	MIN	ТҮР	MAX	
Single-Ended Output Low Voltage	V <sub>OL</sub>	Figure 2	V <sub>CC</sub> - 1.945		V <sub>CC</sub> - 1.695	V <sub>CC</sub> - 1.945		V <sub>CC</sub> - 1.695	V <sub>CC</sub> - 1.945		V <sub>CC</sub> - 1.695	V
Differential Output Voltage	V <sub>OH</sub> - V <sub>OL</sub>	Figure 2	650	830		650	840		650	840		mV
REFERENCE OUT	TPUT (V <sub>BB</sub>	_)										
Reference Voltage Output	V <sub>BB1</sub> V <sub>BB2</sub>	I <sub>BB1</sub> + I <sub>BB2</sub> = ±0.5mA (Note 5)	V <sub>CC</sub> - 1.525	V <sub>CC</sub> - 1.425	V <sub>CC</sub> - 1.325	V <sub>CC</sub> - 1.525	V <sub>CC</sub> - 1.425	V <sub>CC</sub> - 1.325	V <sub>CC</sub> - 1.525	V <sub>CC</sub> - 1.425	V <sub>CC</sub> - 1.325	V
POWER SUPPLY												
Supply Current	IEE	(Note 6)		50	70		53	70		55	70	mA

# **AC ELECTRICAL CHARACTERISTICS**

 $(V_{CC} - V_{EE} = 2.375V \text{ to } 5.5V, \text{ outputs loaded with } 50\Omega \pm 1\% \text{ to } V_{CC} - 2V, V_{IHD} - V_{ILD} = 0.15V \text{ to } 1V, f_{IN} \le 2.5GHz$ , input duty cycle = 50%, input transition time = 125ps (20% to 80%). Typical values are at V<sub>CC</sub> - V<sub>EE</sub> = 3.3V, V<sub>IHD</sub> = V<sub>CC</sub> - 1V, V<sub>ILD</sub> = V<sub>CC</sub> - 1.5V, f\_{IN} = 622 \text{ MHz}, input duty cycle = 50%, input transition time = 125ps (20% to 80%.)) (Note 7)

DADAMETED	SYMBOL				-40°C			+25°C			+85°C		
PARAMETER	STMBUL		INDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Differential Input- to-Output Delay	tplhd, tphld	Figure 2	2	216	301	370	237	310	416	255	329	456	ps
SELto-Output Delay	tpLH2, tpHL2	Figure 4 transitic (20% to	4, input n time = 500ps 80%) (Note 8)		1.34	2		1.25	2		1.44	2	ns
Output-to-Output Skew	tskoo	Figure 5	5 (Note 9)			15			15			30	ps
Input-to-Output Skew	tskio	Figure 6	6 (Note 10)			50			50			55	ps
Part-to-Part Skew	<sup>t</sup> SKPP	(Note 1	1)			125			150			160	ps
A data at Dava dava			$f_{IN} = 156MHz$		0.3	1.15		0.3	1.15		0.3	1.15	
Added Random Jitter (Note 12)	t <sub>RJ</sub>	CIOCK	$f_{IN} = 622 MHz$		0.3	1.15		0.3	1.15		0.3	1.15	psrms
		pattern	$f_{IN} = 2.5 GHz$		0.3	1.15		0.3	1.15		0.3	1.15	
Added Deterministic Jitter (Note 12)	Tol	PRBS	f <sub>IN</sub> = 156Mbps		33	95		33	95		33	95	
	١DJ	2 <sup>23</sup> - 1	f <sub>IN</sub> = 622Mbps		21	61		21	61		21	61	h9h-h

# AC ELECTRICAL CHARACTERISTICS (continued)

 $(V_{CC} - V_{EE} = 2.375V \text{ to } 5.5V, \text{ outputs loaded with } 50\Omega \pm 1\% \text{ to } V_{CC} - 2V, V_{IHD} - V_{ILD} = 0.15V \text{ to } 1V, f_{IN} \le 2.5GHz$ , input duty cycle = 50%, input transition time = 125ps (20% to 80%). Typical values are at V<sub>CC</sub> - V<sub>EE</sub> = 3.3V, V<sub>IHD</sub> = V<sub>CC</sub> - 1V, V<sub>ILD</sub> = V<sub>CC</sub> - 1.5V, f<sub>IN</sub> = 622 MHz, input duty cycle = 50%, input transition time = 125ps (20% to 80%.)) (Note 7)

			-40°C		+25°C			+85°C				
PARAMETER	STMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Switching Frequency	fMAX	$V_{OH}$ - $V_{OL} ≥ 300mV$ , Figure 2	2.7			2.7			2.7			GHz
Select Toggle Frequency	fSEL	V <sub>OH</sub> - V <sub>OL</sub> ≥ 300mV, Figure 4	100			100			100			MHz
Output Rise and Fall Time (20% to 80%)	t <sub>R</sub> , t <sub>F</sub>	Figure 2	67	105	138	74	117	155	81	128	165	ps

Note 1: Measurements are made with the device in thermal equilibrium.

Note 2: Current into an I/O pin is defined as positive. Current out of an I/O pin is defined as negative.

Note 3: DC parameters production tested at  $T_A = +25^{\circ}C$  and guaranteed by design over the full operating temperature range.

**Note 4:** Single-ended data input operation using  $V_{BB_{-}}$  is limited to  $(V_{CC} - V_{EE}) \ge 3.0V$ .

Note 5: Use V<sub>BB</sub> only for inputs that are on the same device as the V<sub>BB</sub> reference.

Note 6: All pins open except V<sub>CC</sub> and V<sub>EE</sub>.

Note 7: Guaranteed by design and characterization. Limits are set at ±6 sigma.

Note 8: Measured from the 50% point of the input signal with the 50% point equal to VBB, to the 50% point of the output signal.

Note 9: Measured between outputs of the same part at the signal crossing points for a same-edge transition.

Note 10: Measured between input-to-output paths of the same part at the signal crossing points for a same-edge transition of the differential input signal.

Note 11: Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.

Note 12: Device jitter added to the differential input signal.

# **Typical Operating Characteristics**

 $(V_{CC} - V_{EE} = 3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V$ , outputs loaded with  $50\Omega \pm 1\%$  to  $V_{CC} - 2V$ ,  $f_{IN} = 622MHz$ , input duty cycle = 50\%, input transition time = 125ps (20% to 80%), unless otherwise noted.)



# **Typical Operating Characteristics (continued)**

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t<sub>PLH</sub>

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 $(V_{CC} - V_{EE} = 3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V$ , outputs loaded with  $50\Omega \pm 1\%$  to  $V_{CC} - 2V$ ,  $f_{IN} = 622MHz$ , input duty cycle = 50\%, input transition time = 125ps (20% to 80%), unless otherwise noted.)



# **Pin Description**

PIN	NAME	FUNCTION
1, 8, 22, 26, 29	Vcc	Positive Supply Input. Bypass each V <sub>CC</sub> to V <sub>EE</sub> with 0.1 $\mu$ F and 0.01 $\mu$ F ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
2	V <sub>BB2</sub>	Reference Output Voltage 2. Connect to the inverting or noninverting data input to provide a reference for single-ended operation. When used, bypass $V_{BB2}$ to $V_{CC}$ with a 0.01µF ceramic capacitor. Otherwise leave open.
3	V <sub>BB1</sub>	Reference Output Voltage 1. Connect to the inverting or noninverting data input to provide a reference for single-ended operation. When used, bypass $V_{BB1}$ to $V_{CC}$ with a 0.01µF ceramic capacitor. Otherwise leave open.
4	D0	Noninverting Differential Input 0. Internal 232k $\Omega$ to V <sub>CC</sub> and 180k $\Omega$ to V <sub>EE</sub> .
5	DO	Inverting Differential Input 0. Internal 180k $\Omega$ to V <sub>CC</sub> and 180k $\Omega$ to V <sub>EE</sub> .
6	D1	Noninverting Differential Input 1. Internal 232k $\Omega$ to V <sub>CC</sub> and 180k $\Omega$ to V <sub>EE</sub> .
7	D1	Inverting Differential Input 1. Internal 180k $\Omega$ to V <sub>CC</sub> and 180k $\Omega$ to V <sub>EE</sub> .
9	D2	Noninverting Differential Input 2. Internal 232k $\Omega$ to V <sub>CC</sub> and 180k $\Omega$ to V <sub>EE</sub> .
10	D2	Inverting Differential Input 2. Internal 180k $\Omega$ to V <sub>CC</sub> and 180k $\Omega$ to V <sub>EE</sub> .
11	D3	Noninverting Differential Input 3. Internal 232k $\Omega$ to V <sub>CC</sub> and 180k $\Omega$ to V <sub>EE</sub> .
12	D3	Inverting Differential Input 3. Internal 180k $\Omega$ to V <sub>CC</sub> and 180k $\Omega$ to V <sub>EE</sub> .
13	D4	Noninverting Differential Input 4. Internal 232k $\Omega$ to V <sub>CC</sub> and 180k $\Omega$ to V <sub>EE</sub> .
14	D4	Inverting Differential Input 4. Internal 180k $\Omega$ to V <sub>CC</sub> and 180k $\Omega$ to V <sub>EE</sub> .
15	D5	Noninverting Differential Input 5. Internal 232k $\Omega$ to V <sub>CC</sub> and 180k $\Omega$ to V <sub>EE</sub> .
16	D5	Inverting Differential Input 5. Internal 180k $\Omega$ to V <sub>CC</sub> and 180k $\Omega$ to V <sub>EE</sub> .
17, 32	VEE	Negative Supply Input
18	D6	Noninverting Differential Input 6. Internal 232k $\Omega$ to V <sub>CC</sub> and 180k $\Omega$ to V <sub>EE</sub> .
19	D6	Inverting Differential Input 6. Internal 180k $\Omega$ to V <sub>CC</sub> and 180k $\Omega$ to V <sub>EE</sub> .

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**MAX9389** 

	<b>Pin Descri</b>	ption	(continued)
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PIN	NAME	FUNCTION
20	D7	Noninverting Differential Input 7. Internal 232k $\Omega$ to V_{CC} and 180k $\Omega$ to V_{EE}.
21	D7	Inverting Differential Input 7. Internal 180k $\Omega$ to V <sub>CC</sub> and 180k $\Omega$ to V <sub>EE</sub> .
23	SEL0	Select Logic Input 0. Internal 165k $\Omega$ pulldown to V <sub>EE</sub> .
24	SEL1	Select Logic Input 1. Internal 165k $\Omega$ pulldown to V <sub>EE</sub> .
25	SEL2	Select Logic Input 2. Internal 165k $\Omega$ pulldown to V <sub>EE</sub> .
27	Q1	Inverting Output 1. Typically terminate with 50 $\Omega$ resistor to V <sub>CC</sub> - 2V.
28	Q1	Noninverting Output 1. Typically terminate with 50 $\Omega$ resistor to V <sub>CC</sub> - 2V.
30	QO	Inverting Output 0. Typically terminate with 50 $\Omega$ resistor to V <sub>CC</sub> - 2V.
31	QO	Noninverting Output 0. Typically terminate with 50 $\Omega$ resistor to V <sub>CC</sub> - 2V.
_	EP	Exposed Pad (QFN Package Only). Connect to VEE.



Figure 1. Input Definitions



Figure 3. Single-Ended Input-to-Output Propagation Delay Timing Diagram



Figure 2. Differential Input-to-Output Propagation Delay Timing Diagram



Figure 4. Select Input (SEL0) to Output ( $Q_{-}, \overline{Q}_{-}$ ) Delay Timing Diagram





Figure 5. Output-to-Output Skew (tSKOO) Definition

### \_Detailed Description

The MAX9389 is a fully differential, high-speed, low-jitter 8-to-1 ECL/PECL mux with dual output buffers. The device is designed for clock and data distribution applications, and features extremely low propagation delay (310ps typ) and output-to-output skew (30ps max).

Three single-ended select inputs, SEL0, SEL1, and SEL2, control the mux function (see Table 1). The mux select inputs are compatible with ECL/PECL logic, and are internally referenced to the on-chip reference output (VBB1, VBB2), nominally V<sub>CC</sub> - 1.425V. The select inputs accept signals between V<sub>CC</sub> and V<sub>EE</sub>. Internal 165k $\Omega$  pulldowns to V<sub>EE</sub> ensure a low default condition if the select inputs are left open. Leaving SEL0, SEL1, and SEL2 open selects the D0, D0 inputs by default.

The differential inputs D\_,  $\overline{D}$  can be configured to accept a single-ended signal when the unused complementary input is connected to the on-chip reference voltage (VBB1, VBB2). Voltage reference outputs VBB1 and VBB2 provide the reference voltage needed for single-ended operations. A single-ended input of at least VBB\_ ±100mV or a differential input of at least 100mV switches the outputs to the VOH and VOL levels specified in the *DC Electrical Characteristics* table. The maximum magnitude of the differential input from D\_ to  $\overline{D}_$  is ±3.0V. This limit also applies to the difference between a single-ended input and any reference voltage input.



Figure 6. Input-to-Output Skew (t<sub>SKIO</sub>) Definition

### Table 1. Mux Select Input Truth Table

DATA OUTPUT	SEL0	SEL1	SEL2
D0*	L or open	L or open	L or open
D1	Н	L or open	L or open
D2	L or open	Н	L or open
D3	Н	Н	L or open
D4	L or open	L or open	Н
D5	Н	L or open	Н
D6	L or open	Н	Н
D7	Н	Н	Н

\*Default output when SEL0, SEL1, and SEL2 are left open.

### **Single-Ended Operation**

The recommended supply voltage for single-ended operation is 3.0V to 3.8V. The differential inputs (D\_,  $\overline{D}_{-}$ ) can be configured to accept single-ended inputs when operating at supply voltages greater than 2.725V. In single-ended mode operation, the unused complementary input needs to be connected to the on-chip reference voltage, V<sub>BB1</sub> or V<sub>BB2</sub>, as a reference. For example, the differential D\_,  $\overline{D}_{-}$  inputs are converted to a noninverting, single-ended input by connecting V<sub>BB1</sub> or V<sub>BB2</sub> to  $\overline{D}_{-}$  and connecting the single-ended input to D\_. Similarly, an inverting input is obtained by connecting V<sub>BB1</sub> or V<sub>BB2</sub> to  $\overline{D}_{-}$  and connecting the single-ended input to D\_. The single-ended input can be driven to V<sub>CC</sub> or V<sub>EE</sub> or with a single-ended LVPECL/LVECL signal.

# **MAX9389**

M/X/M

### Traces

In single-ended operation, ensure that the supply voltage (V<sub>CC</sub> -V<sub>EE</sub>) is greater than 2.725V. The input high minimum level must be at least (VEE + 1.2V) or higher for proper operation. The reference voltage VBB must be at least (VEE + 1.2V) because it becomes the highlevel input when a single-ended input swings below it. The minimum VBB output for the MAX9389 is (VCC -1.525V). Substituting the minimum VBB output for (VBB = VEE + 1.2V) results in a minimum supply (VCC - VEE) of 2.725V. Rounding up to standard supplies gives the recommended single-ended operating supply ranges (VCC - VFF) of 3.0V to 5.5V.

When using the VBB reference output, bypass it with a 0.01µF ceramic capacitor to V<sub>CC</sub>. If V<sub>BB</sub> is not being used, leave it unconnected. The VBB reference can source or sink a total of 0.5mA (shared between VBB1 and VBB2), which is sufficient to drive eight inputs.

## **Applications Information**

### **Output Termination**

Terminate each output with a 50 $\Omega$  to V<sub>CC</sub> - 2V or use an equivalent Thevenin termination. Terminate each Q and  $\overline{Q}$  output with identical termination for minimal distortion. When a single-ended signal is taken from the differential output, terminate both Q\_ and  $\overline{Q}_{-}$ .

Ensure that the output current does not exceed the current limits specified in the Absolute Maximum Ratings table. Under all operating conditions, the device's total thermal limits should not be exceeded.

### **Supply Bypassing**

Bypass each V<sub>CC</sub> to V<sub>EE</sub> with high-frequency surfacemount ceramic 0.1µF and 0.01µF capacitors. For PECL, bypass each V<sub>CC</sub> to V<sub>EE</sub>. For ECL, bypass each V<sub>EE</sub> to VCC. Place the capacitors as close to the device as possible with the 0.01µF capacitor closest to the device pins.

Use multiple vias when connecting the bypass capacitors to ground. When using the VBB1 or VBB2 reference outputs, bypass each one with a 0.01µF ceramic capacitor to V<sub>CC</sub>. If the V<sub>BB1</sub> or V<sub>BB2</sub> reference outputs are not used, they can be left open.

Circuit board trace layout is very important to maintain the signal integrity of high-speed differential signals. Maintaining integrity is accomplished in part by reducing signal reflections and skew, and increasing commonmode noise immunity.

Signal reflections are caused by discontinuities in the  $50\Omega$  characteristic impedance of the traces. Avoid discontinuities by maintaining the distance between differential traces, not using sharp corners or using vias. Maintaining distance between the traces also increases common-mode noise immunity. Reducing signal skew is accomplished by matching the electrical length of the differential traces.



**Pin Configurations (continued)** 

# **Chip Information**

**TRANSISTOR COUNT: 716 PROCESS: Bipolar** 

**MAX9389** 

# Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



# **MAX9389**

# **Package Information (continued)**

THIN.EPS

ZLO

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



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10

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