19-3973; Rev 1; 8/08

EVALUATION KIT AVAILABLE

# 4.5V to 28V Input Current-Mode Step-Down Controller with Adjustable Frequency



## General Description

The MAX8650 synchronous PWM buck controller operates from a 4.5V to 28V input and generates an adjustable 0.7V to 5.5V output voltage at loads up to 25A.

The MAX8650 uses a peak current-mode control architecture with an adjustable (200kHz to 1.2MHz) constant switching frequency and is externally synchronizable. The IC's current limit uses the inductor's DC resistance to improve efficiency or an external sense resistor for high accuracy. The current-limit threshold is adjusted with an external resistor. Foldback-type current limit can be implemented to reduce the power dissipation in overload or short-circuit conditions. Short-circuit protection is provided based on sensing the current in the low-side MOSFET. A reference input is provided for use with a high-accuracy external reference or for double-data-rate (DDR)-tracking applications.

Monotonic prebiased startup is available for a safe-start in applications where the output capacitor may have an initial charge. This feature prevents the output from pulling low during startup, which is a common characteristic of conventional buck regulators.

A 180° out-of–phase synchronization output is available for synchronizing with another converter.

## Applications

Base Stations
Network and Telecom
Storage
Servers
DDR
Power Modules
IBA Applications

***Pin Configuration appears at end of data sheet.***

## Features

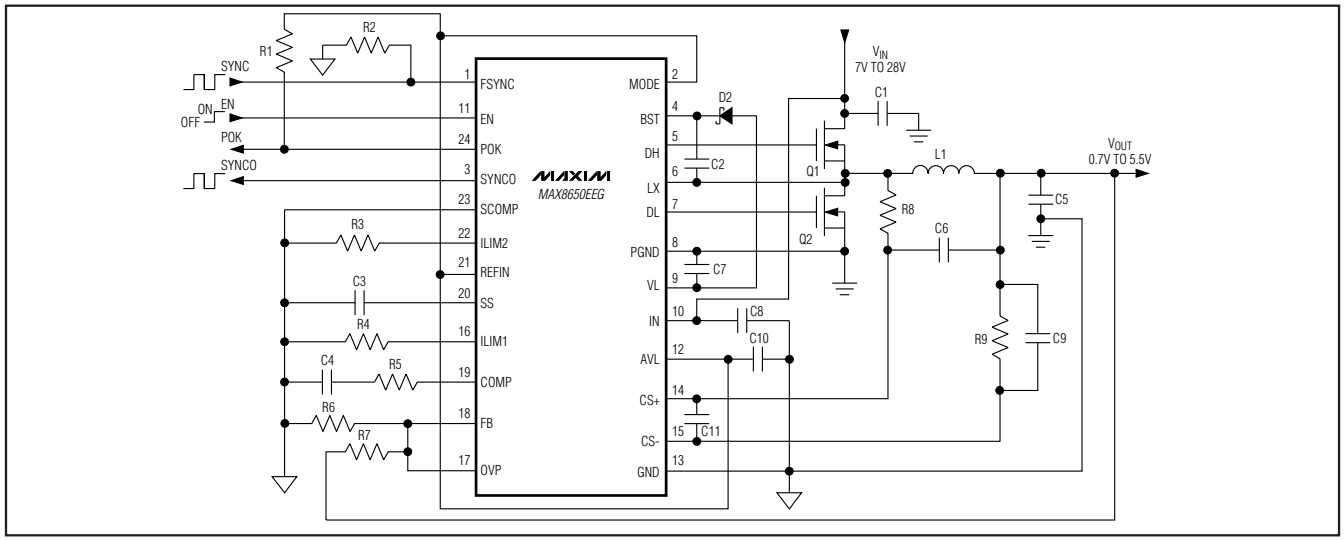
- **Operates from 4.5V to 28V Supply**
- **1% FB Voltage Accuracy Over Temperature**
- **Adjustable Output Voltage Down to 0.7V or REFIN**
- **Adjustable Switching Frequency or External Synchronization from 200kHz to 1.2MHz**
- **180° Phase-Shifted Clock Output**
- **Adjustable Overcurrent Limit**
- **Adjustable Foldback Current Limit**
- **Adjustable Slope Compensation**
- **Selectable Current-Limit Mode: Latch-Off or Automatic Recovery**
- **Monotonic Output-Voltage Rise at Startup**
- **Output Sources and Sinks Current**
- **Enable Input**
- **Power-OK (POK) Output**
- **Adjustable Soft-Start**
- **Independently Adjustable Overvoltage Protection**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX8650EEG+ | -40°C to +85°C | 24 QSOP |

*+Denotes a lead-free/RoHS-compliant package.*

## Typical Operating Circuit



# 4.5V to 28V Input Current-Mode Step-Down Controller with Adjustable Frequency

## ABSOLUTE MAXIMUM RATINGS

IN, EN to GND .....-0.3V to +30V
BST to LX.....-0.3V to +7.5V
DH to LX.....-0.3V to ($V_{BST}$ + 0.3V)
LX to GND ..... -1V (-2.5V for < 50ns transient) to +30V
DL to PGND.....-0.3V to ($V_{VL}$ + 0.3V)
ILIM2, ILIM1, SYNCO, FSYNC, OVP, SCOMP to GND .....-0.3V to ($V_{AVL}$ + 0.3V)
VL to PGND .....-0.3V to +7.5V
AVL, FB, POK, COMP, SS, MODE, REFIN to GND .....-0.3V to +6V
CS+, CS- to GND .....-0.3V to +6V
PGND to GND .....-0.3V to +0.3V
Continuous Power Dissipation ($T_A$ = +70°C)
24-Pin QSOP (derate 9.5mW/°C above +70°C).....762mW
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{IN}$ = 12V, $V_{BST}$ - $V_{LX}$ = 6.5V, $T_A$ = -40°C to +85°C. Typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Operating Input Voltage Range | VL = IN for $V_{IN}$ < 7V | 4.5 | | 28.0 | V |
| Quiescent Supply Current | $V_{FB}$ = 0.75V, no switching | | 2 | 3 | mA |
| Shutdown Supply Current $I_{IN}$ + $I_{VL}$ + $I_{AVL}$ | EN = GND, $V_{IN}$ ≤ 28V | | | 10 | µA |
| | EN = GND, $V_{AVL}$ = $V_{VL}$ = $V_{IN}$ = 5V | | | 32 | |
| AVL Undervoltage-Lockout Trip Level | $V_{AVL}$ rising, 3% typ hysteresis | 3.90 | 4.15 | 4.40 | V |
| Output Voltage Adjust Range | Minimum output voltage is limited by minimum duty cycle and external components | 0.7 | | 5.5 | V |
| VL Regulation Voltage | 7V < $V_{IN}$ < 28V, 1mA < $I_{LOAD}$ < 40mA | 6.0 | 6.5 | 7.0 | V |
| VL Output Current | | 40 | | | mA |
| AVL Regulation Voltage | 5.5V < $V_{VL}$ < 7V, 1mA < $I_{LOAD}$ < 10mA | 4.900 | 4.975 | 5.050 | V |
| AVL Output Current | | 10 | | | mA |
| **SOFT-START** | | | | | |
| SS Shutdown Resistance | From SS to GND, $V_{EN}$ = 0V | | 20 | 100 | Ω |
| SS Soft-Start Current | $V_{SS}$ = 0.625V | 18 | 23 | 28 | µA |
| **REFIN INPUT** | | | | | |
| REFIN Dual Mode™ Threshold | | $V_{AVL}$ - 1.0V | | $V_{AVL}$ | V |
| REFIN Input Bias Current | $V_{REFIN}$ = 0.7V to 1.5V | -250 | | +250 | nA |
| REFIN Input Voltage Range | | 0 | | 1.5 | V |

*Dual Mode is a trademark of Maxim Integrated Products, Inc.*

## ELECTRICAL CHARACTERISTICS (continued)

($V_{IN}$ = 12V, $V_{BST}$ - $V_{LX}$ = 6.5V, $T_A$ = -40°C to +85°C. Typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **ERROR AMPLIFIER** | | | | | |
| FB Regulation Voltage | REFIN = AVL | 0.693 | 0.7 | 0.707 | V |
| | $V_{REFIN}$ = 0.7V to 1.5V | $V_{REFIN}$ - 0.00375 | $V_{REFIN}$ | $V_{REFIN}$ + 0.00375 | |
| Transconductance | | 70 | 110 | 160 | µS |
| COMP Shutdown Resistance | From COMP to GND, $V_{EN}$ = 0V | | 20 | 100 | Ω |
| FB Input Leakage Current | $V_{FB}$ = 0.7V | | 5 | 50 | nA |
| FB Input Common-Mode Range | | -0.1 | | +1.5 | V |
| **CURRENT-SENSE AMPLIFIER** | | | | | |
| Voltage Gain | $V_{OUT}$ = 0 to 5.5V, $V_{CS+}$ - $V_{CS-}$ = 30mV | | 12 | | V/V |
| **CURRENT LIMIT** | | | | | |
| Peak Current-Limit Threshold ($V_{CS+}$ - $V_{CS-}$) | $R_{ILIM1}$ = 24kΩ | 27.2 | 32.0 | 36.8 | mV |
| | ILIM1 = AVL | 68.0 | 80.0 | 92.0 | |
| Valley Current-Limit Threshold ($V_{LX}$ - $V_{PGND}$) | $R_{ILIM2}$ = 50kΩ | -42.5 | -50.0 | -57.5 | mV |
| | $R_{ILIM2}$ = 200kΩ | -170 | -200 | -230 | |
| Negative Current-Limit Threshold | % of (typ) positive direction current limit ($V_{LX}$ - $V_{PGND}$) | -90 | -120 | -150 | % |
| CS+, CS- Input Current | $V_{CS+}$ = $V_{CS-}$ = 0V or 5.5V | -25 | | +25 | µA |
| CS+, CS- Input Common-Mode Range | | 0 | | 5.5 | V |
| **SLOPE COMPENSATION** | | | | | |
| Slope Compensation at Maximum Duty Cycle | $V_{SCOMP}$ = 2.5V | 231.25 | 250.00 | 268.75 | mV |
| | $V_{SCOMP}$ = 1.25V | 113.77 | 123.00 | 132.23 | |
| | SCOMP = AVL | 231.25 | 250.00 | 268.75 | |
| | SCOMP = GND, $T_A$ = 0°C to +85°C | 113.77 | 123.00 | 132.23 | |
| | $T_A$ = -40°C to +85°C | 110.70 | 123.00 | 132.23 | |
| SCOMP High Threshold | | | | $V_{AVL}$ - 0.5 | V |
| SCOMP Low Threshold | | 0.5 | | | V |
| SCOMP Adjustment Range | | 1.25 | | 2.5 | V |
| SCOMP Input Leakage Current | $V_{SCOMP}$ = 1.25V to 2.5V | | 5 | 200 | nA |
| **OSCILLATOR** | | | | | |
| Switching Frequency | $R_{FSYNC}$ = 21.0kΩ | 800 | 1000 | 1200 | kHz |
| | $R_{FSYNC}$ = 143kΩ | 160 | 200 | 240 | |
| Minimum Off-Time | Measured at DH | | 235 | | ns |
| Minimum On-Time | Measured at DH | | 75 | 100 | ns |

# 4.5V to 28V Input Current-Mode Step-Down Controller with Adjustable Frequency

## ELECTRICAL CHARACTERISTICS (continued)

($V_{IN}$ = 12V, $V_{BST}$ - $V_{LX}$ = 6.5V, $T_A$ = -40°C to +85°C. Typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| FSYNC Synchronization Range | | 160 | | 1200 | kHz |
| FSYNC Input-High Pulse Width | | 100 | | | ns |
| FSYNC Input-Low Pulse Width | | 100 | | | ns |
| FSYNC Rise/Fall Time | | | | 100 | ns |
| SYNCO Phase Shift | | | 180 | | Degrees |
| SYNCO Output Low Level | $I_{SYNCO}$ = 5mA | | | 0.4 | V |
| SYNCO Output High Level | $I_{SYNCO}$ = 5mA | $V_{AVL}$ - 1V | | | V |
| FSYNC Pin Threshold for SYNC Mode | | 1.7 | | 2.5 | V |
| FSYNC Input Low | | | | 0.4 | V |
| FSYNC Input High | | 2.5 | | | V |
| **FET DRIVERS** | | | | | |
| DH On-Resistance, High State | $V_{BST}$ - $V_{LX}$ = 6.5V | | 1.13 | 1.8 | Ω |
| | $V_{BST}$ - $V_{LX}$ = 5V | | 1.4 | 2.2 | |
| DH On-Resistance, Low State | $V_{BST}$ - $V_{LX}$ = 6.5V | | 1.0 | 2 | Ω |
| | $V_{BST}$ - $V_{LX}$ = 5V | | 1.3 | 2.2 | |
| DL On-Resistance, High State | $V_{VL}$ = 6.5V | | 1.6 | 2.5 | Ω |
| | $V_{VL}$ = 5V | | 1.7 | 2.8 | |
| DL On-Resistance, Low State | $V_{VL}$ = 6.5V | | 0.8 | 1.5 | Ω |
| | $V_{VL}$ = 5V | | 0.85 | 1.5 | |
| Break-Before-Make Dead Time | Low side off to high side on, high side off to low side on | | 20 | 30 | ns |
| LX, BST Leakage Current | $V_{BST}$ = 35V, $V_{LX}$ = 28V, $V_{IN}$ = 28V | | | 5 | µA |
| **THERMAL PROTECTION** | | | | | |
| Thermal Shutdown | Rising temperature | | +160 | | °C |
| Thermal-Shutdown Hysteresis | | | 15 | | °C |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{IN}$ = 12V, $V_{BST}$ - $V_{LX}$ = 6.5V, $T_A$ = -40°C to +85°C. Typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **POK** | | | | | |
| Power-OK Threshold | REFIN = AVL, $V_{FB}$ rising, typical hysteresis is 3% | 629.0 | 650.0 | 671.0 | mV |
| | $V_{REFIN}$ = 0.7V to 1.5V, $V_{FB}$ rising, typical hysteresis is 3% | 88.7 | 91.7 | 94.7 | % of |
| POK Output Voltage, Low | $V_{FB}$ = 0.6V, $I_{POK}$ = 2mA | | 25 | 200 | mV |
| POK Leakage Current, High | $V_{POK}$ = 5.5V | | | 1 | µA |
| **OVP** | | | | | |
| OVP Threshold Voltage | REFIN = AVL | 770 | 800 | 840 | mV |
| | $V_{REFIN}$ = 0.7V to 1.5V | 110 | 115 | 120 | % of $V_{REFIN}$ |
| OVP Leakage Current, High | $V_{OVP}$ = 0.8V | | | 500 | nA |
| **MODE CONTROL** | | | | | |
| MODE Logic-Level Low | 4.5V ≤ $V_{AVL}$ ≤ 5.5V | | | 0.4 | V |
| MODE Logic-Level High | 4.5V ≤ $V_{AVL}$ ≤ 5.5V | 1.8 | | | V |
| MODE Input Current | $V_{MODE}$ = 0 to $V_{AVL}$ | -1 | | +1 | µA |
| **SHUTDOWN CONTROL** | | | | | |
| EN Logic-Level Low | 4.5V ≤ $V_{AVL}$ ≤ 5.5V | | | 0.45 | V |
| EN Logic-Level High | 4.5V ≤ $V_{AVL}$ ≤ 5.5V | 2 | | | V |
| EN Input Current | $V_{EN}$ = 0V | -1 | | +1 | µA |
| | $V_{EN}$ = 28V | | 1.5 | 6.0 | |

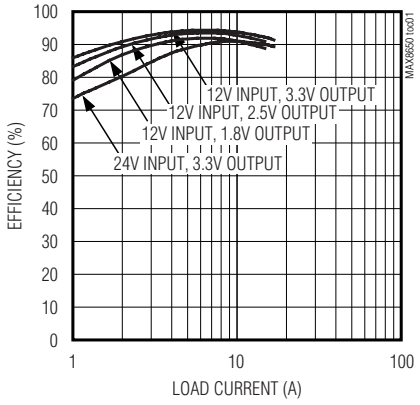
**Note 1:** Specifications are 100% production tested at $T_A$ = +85°C. Limits over the operating temperature range are guaranteed by design.

# 4.5V to 28V Input Current-Mode Step-Down Controller with Adjustable Frequency

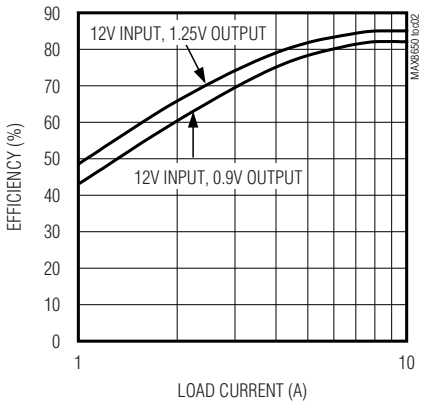
## Typical Operating Characteristics

(Circuit of Figure 3, 500kHz switching, $V_{IN}$ = 17V, $V_{OUT}$ = 3.3V, $T_A$ = +25°C, unless otherwise noted.)

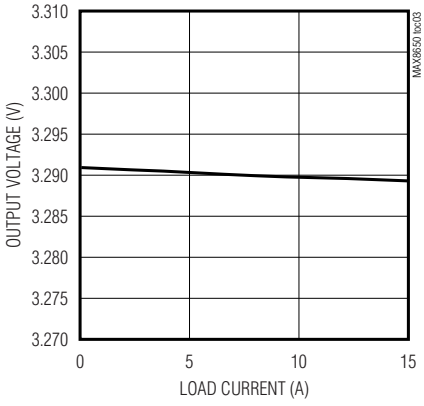
**EFFICIENCY vs. LOAD CURRENT**



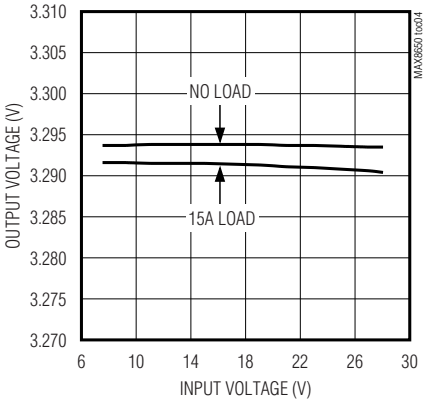

**EFFICIENCY vs. LOAD CURRENT (CIRCUIT OF FIGURE 4)**



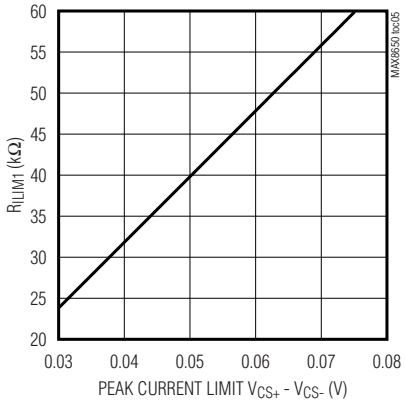

**LOAD REGULATION**



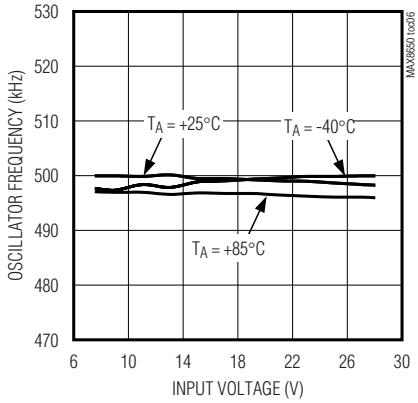

**LINE REGULATION**



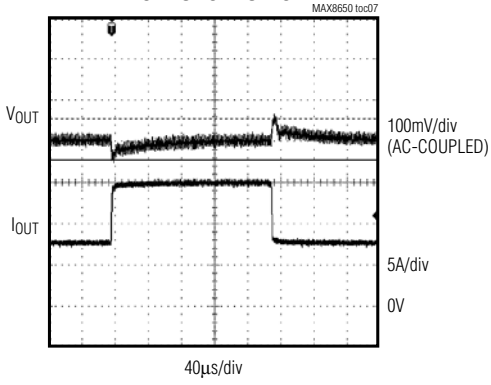

**$R_{ILIM1}$ vs. PEAK CURRENT LIMIT**



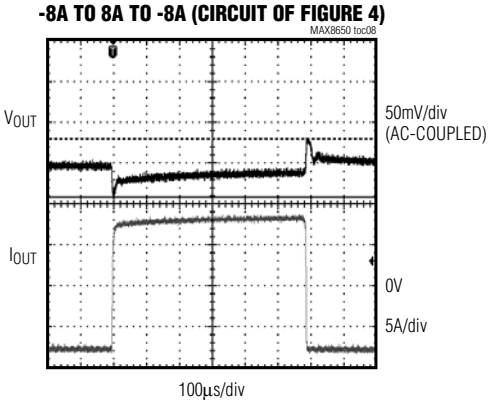

**OSCILLATOR FREQUENCY vs. INPUT VOLTAGE**




**STEP-LOAD RESPONSE 7.5A TO 15A TO 7.5A**



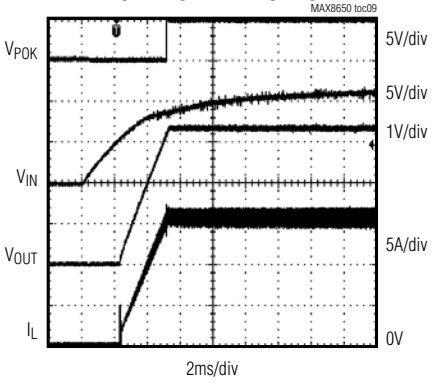

**STEP-LOAD RESPONSE -8A TO 8A TO -8A (CIRCUIT OF FIGURE 4)**



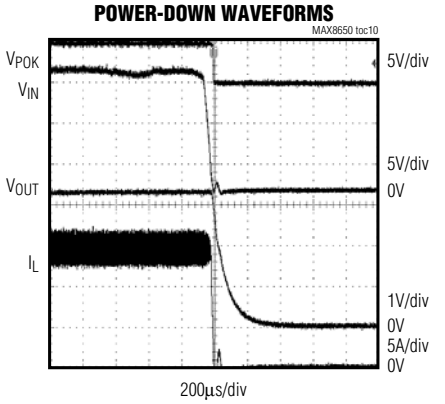
## Typical Operating Characteristics (continued)

(Circuit of Figure 3, 500kHz switching, $V_{IN}$ = 17V, $V_{OUT}$ = 3.3V, $T_A$ = +25°C, unless otherwise noted.)

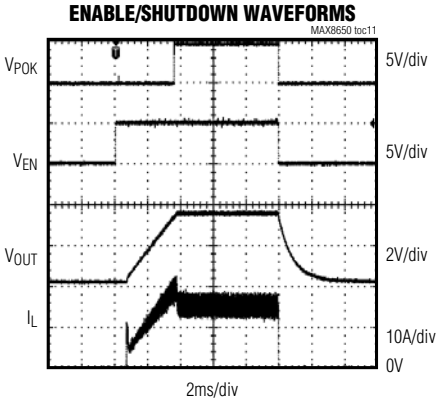
**POWER-UP WAVEFORMS**



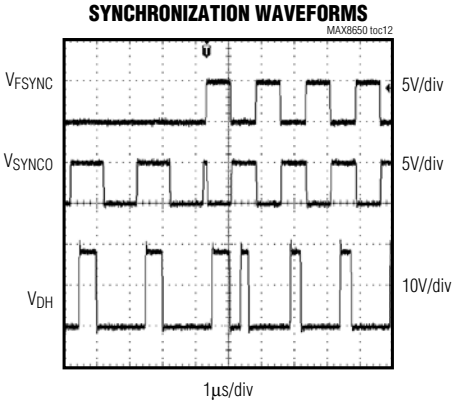

**POWER-DOWN WAVEFORMS**



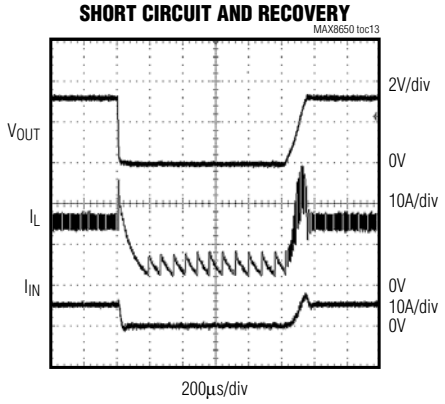

**ENABLE/SHUTDOWN WAVEFORMS**



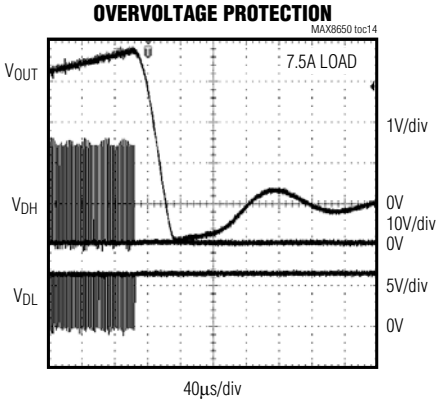

**SYNCHRONIZATION WAVEFORMS**



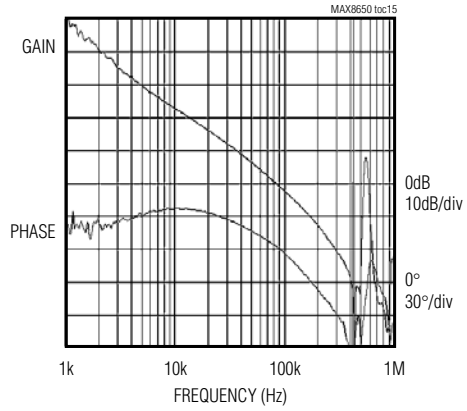

**SHORT CIRCUIT AND RECOVERY**



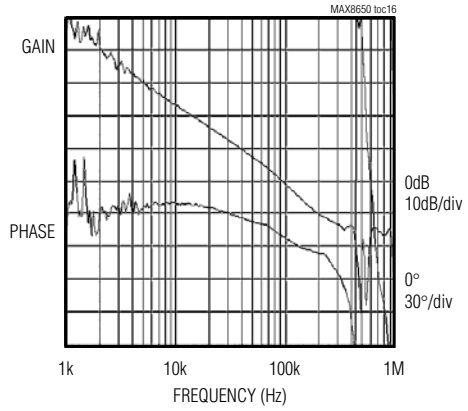

**OVERVOLTAGE PROTECTION**




**CLOSED-LOOP BODE PLOT WITH NO LOAD**




**CLOSED-LOOP BODE PLOT WITH 15A LOAD**



# 4.5V to 28V Input Current-Mode Step-Down Controller with Adjustable Frequency

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | FSYNC | Frequency Set and Synchronization. Connect a resistor from FSYNC to GND to set the switching frequency, or drive with an external clock signal between 160kHz and 1.2MHz. See the *Switching Frequency and Synchronization* section. |
| 2 | MODE | Current-Limit Operating-Mode Selection. Connect MODE to AVL for latch-off current limit or connect MODE to GND for automatic-recovery current limit. |
| 3 | SYNCO | Synchronization Output. Provides a clock output that is 180° out-of-phase with the internal oscillator for synchronizing another MAX8650. |
| 4 | BST | Boost Capacitor Connection. Connect a 0.1µF ceramic capacitor from BST to LX. |
| 5 | DH | High-Side n-Channel MOSFET Gate-Driver Output. Connect DH to the gate of the high-side MOSFET. DH is internally pulled low in shutdown. |
| 6 | LX | External Inductor Connection |
| 7 | DL | Low-Side n-Channel MOSFET Gate-Driver Output. Connect DL to the gate of the low-side MOSFET (synchronous rectifier). DL is internally pulled low in shutdown. |
| 8 | PGND | Power Ground. Connect PGND to the power ground plane and to the source of the low-side external MOSFET. The return path for both gate drivers is through PGND. |
| 9 | VL | Internal 6.5V Linear-Regulator Output. Connect a 1µF to 10µF ceramic capacitor from VL to ground. For $V_{IN}$ < 7V, connect VL directly to IN. VL powers both gate drivers. VL is the input to the AVL linear regulator. |
| 10 | IN | Input Supply Voltage. IN is the input to the VL linear regulator. Connect VL to IN for $V_{IN}$ < 7V. |
| 11 | EN | Enable. Apply logic-high to enable the output, or logic-low to put the controller in low-power shutdown mode. Connect EN to IN for always-on operation. |
| 12 | AVL | Internal 5V Linear-Regulator Output. Connect a 1µF ceramic capacitor from AVL to ground. AVL powers the MAX8650's internal circuits. |
| 13 | GND | Ground. Connect GND to the analog ground plane. Connect the analog ground and power ground planes at a single point near the IC. Low-current signals return to GND. |
| 14 | CS+ | Positive Differential Current-Sense Input |
| 15 | CS- | Negative Differential Current-Sense Input |
| 16 | ILIM1 | Programmable Current-Limit Input for Inductor Current. Connect a resistor from ILIM1 to GND to set the peak current-limit threshold. ILIM1 sources 10µA through the resistor, and the voltage at ILIM1 is attenuated 7.5:1 to set the final current limit. For example, a 60kΩ resistor results in 600mV at ILIM1. This results in a current-limit threshold ($V_{CS+}$ - $V_{CS-}$) of 80mV. The ILIM1 resistor range is 24kΩ to 60kΩ. Connect ILIM1 to AVL to set the default current-limit threshold of 80mV. |

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 17 | OVP | Output Voltage Sensing for Overvoltage Protection. Connect OVP to the center of a resistor-divider from OUT to GND to set the FB independent output overvoltage trip point. Connect OVP to FB if this independence is not desired. The OVP threshold is 115% of the nominal FB regulation voltage. |
| 18 | FB | Feedback Input. Connect FB to the center of a resistor voltage-divider between the output and GND to set the output voltage. The FB threshold regulates at 0.7V or $V_{REFIN}$. |
| 19 | COMP | Loop Compensation. Connect COMP to an external RC network to compensate the loop. COMP is internally pulled to GND through 20Ω during shutdown. |
| 20 | SS | Soft-Start. Connect a 0.1µF to 1µF ceramic capacitor from SS to GND. This capacitor sets the soft-start period during startup. SS is internally pulled to GND through 20Ω during shutdown. |
| 21 | REFIN | External Reference Input. Connect REFIN to AVL to use the internal 0.7V reference for the feedback threshold. |
| 22 | ILIM2 | Programmable Current-Limit Input for the Low-Side MOSFET (LX-PGND). Connect a resistor from ILIM2 to GND to set the valley current-limit threshold. ILIM2 sources 5µA through the resistor, and the voltage at ILIM2 is attenuated 5:1 to set the final current limit. For example, a 50kΩ resistor results in 250mV at ILIM2. This results in a current-limit threshold ($V_{LX}$ - $V_{PGND}$) of 50mV. $V_{ILIM2}$ must not exceed 1V. |
| 23 | SCOMP | Programmable Slope-Compensation Input. The slope-compensation voltage rate is the voltage at SCOMP times 0.1 divided by the oscillator period (T). Connect SCOMP to AVL or GND to set to the default of 250mV/T or 125mV/T, respectively. |
| 24 | POK | Open-Drain Output that Is High Impedance when the Output Voltage Rises Above 92% of the Nominal Regulation Value. POK pulls low during shutdown and when the output drops below 88% of the nominal regulation value. |

# 4.5V to 28V Input Current-Mode Step-Down Controller with Adjustable Frequency

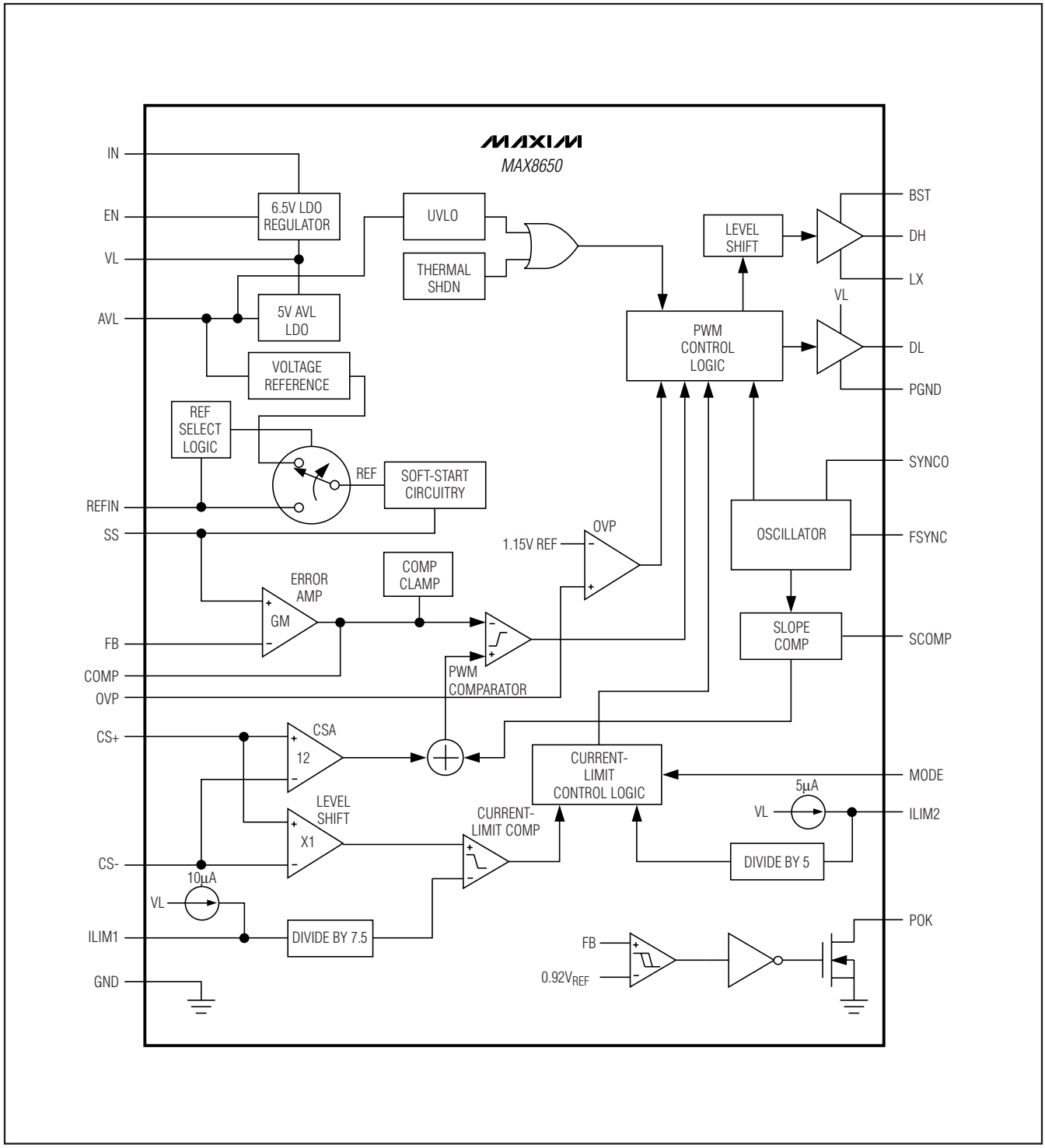



*Figure 1. Functional Diagram*

# 4.5V to 28V Input Current-Mode Step-Down Controller with Adjustable Frequency

## Detailed Description

### DC-DC Converter Control Architecture

The MAX8650 step-down controller uses a PWM, current-mode control scheme. An internal transconductance amplifier establishes an integrated error voltage. The heart of the PWM controller is an open-loop comparator that compares the integrated voltage-feedback signal against the amplified current-sense signal plus the adjustable slope-compensation ramp, which are summed into the main PWM comparator to preserve inner-loop stability. At each rising edge of the internal clock, the high-side MOSFET turns on until the PWM comparator trips or the maximum duty cycle is reached. During this on-time, current ramps up through the inductor, storing energy in a magnetic field and sourcing current to the output. The current-mode feedback system regulates the peak inductor current as a function of the output-voltage error signal. The circuit acts as a switch-mode transconductance amplifier and pushes the output LC filter pole normally found in a voltage-mode PWM to a higher frequency.

During the second half of the cycle, the high-side MOSFET turns off and the low-side MOSFET turns on. The inductor releases the stored energy as the current ramps down, providing current to the output. The output capacitor stores charge when the inductor current exceeds the required load current and discharges when the inductor current is lower, smoothing the voltage across the load. Under soft-overload conditions, when the peak inductor current exceeds the selected current limit (see the *Current-Limit Circuit* section), the high-side MOSFET is turned off immediately and the low-side MOSFET is turned on and remains on to let the inductor current ramp down until the next clock cycle. Under heavy-overload or short-circuit conditions, the valley foldback current limit is enabled to reduce power dissipation of external components.

The MAX8650 operates in a forced-PWM mode. As a result, the controller maintains a constant switching frequency, regardless of load, to allow for easier filtering of the switching noise.

### Internal Linear Regulators

The MAX8650 contains two internal LDO regulators. The AVL regulator provides 5V for the IC's internal circuitry, and the VL regulator provides 6.5V for the MOSFET gate drivers. Connect a 4.7µF ceramic capacitor from VL to PGND, and connect a 1µF ceramic capacitor from AVL to GND. For applications where the input voltage is between 4.5V and 7V, connect VL directly to IN and connect a 10Ω resistor from VL to AVL.

### Undervoltage Lockout

When AVL drops below 4.03V, the MAX8650 assumes that the supply voltage is too low for proper operation, so the undervoltage-lockout (UVLO) circuitry inhibits switching and forces the DL and DH gate drivers low. When AVL rises above 4.15V, the controller enters the startup sequence and then resumes normal operation.

### Startup and Soft-Start

The internal soft-start circuitry gradually ramps up the reference voltage to control the rate of rise of the step-down controller's output and reduce input surge currents during startup. The soft-start period is determined by the value of the capacitor from SS to GND. The soft-start time is approximately (30.4ms/µF) x $C_{SS}$. The MAX8650 also features monotonic output-voltage rise; therefore, both external power MOSFETs are kept off if the voltage at FB is higher than the voltage at SS. This allows the MAX8650 to start up into a prebiased output without pulling the output voltage down.

Before the MAX8650 can begin the soft-start and power-up sequence, the following conditions must be met:

- $V_{AVL}$ exceeds the 4.15V UVLO threshold.
- EN is at logic-high.
- The thermal limit is not exceeded.

### Enable (EN)

The MAX8650 features a low-power shutdown mode. A logic-low at EN shuts down the controller. During shutdown, the output is high impedance, and both DH and DL are low. Shutdown reduces the quiescent current ($I_Q$) to less than 10µA. A logic-high at EN enables the controller.

### Synchronous-Rectifier Driver (DL)

Synchronous rectification reduces conduction losses in the rectifier by replacing the normal Schottky catch diode with a low-resistance MOSFET switch. The MAX8650 also uses the synchronous rectifier to ensure proper startup of the boost gate-driver circuit and to provide the current-limit signal. The low-side gate driver (DL) swings from 0 to the 6.5V provided from VL. The DL waveform is always the complement of the DH high-side gate-drive waveform (with controlled dead time to prevent cross-conduction or shoot-through). An adaptive dead-time circuit monitors the DL voltage and prevents the high-side MOSFET from turning on until DL is fully off. For the dead-time circuit to work properly, there must be a low-resistance, low-inductance path from the DL driver to the MOSFET gate. Otherwise, the sense circuitry in the MAX8650 can interpret the MOSFET gate as off when gate charge actually remains. Use very short, wide traces, approximately 10

# 4.5V to 28V Input Current-Mode Step-Down Controller with Adjustable Frequency

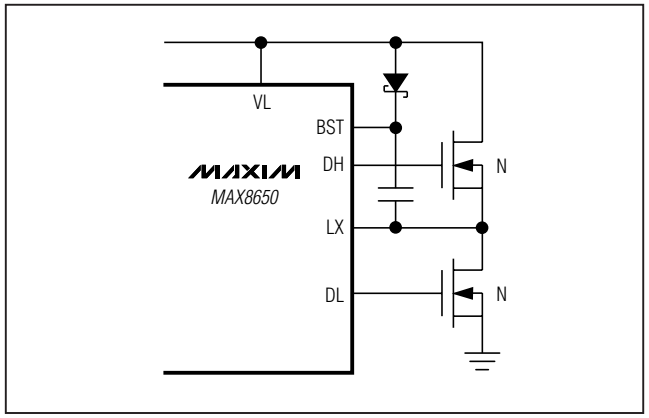



*Figure 2. DH Boost Circuit*

to 20 squares (50 mils to 100 mils wide if the MOSFET is 1in from the device) for the gate drive. The dead time at the other edge (DH turning off) also has an adaptive dead-time circuit operating in a similar manner. For both edges, there is an additional 20ns fixed dead time after the adaptive dead time expires.

### High-Side Gate-Drive Supply (BST)

A flying capacitor boost circuit (Figure 2) generates the gate-drive voltage for the high-side n-channel MOSFET. The capacitor between BST and LX is charged from VL to 6.5V minus the diode forward-voltage drop while the low-side MOSFET is on. When the low-side MOSFET is switched off, the stored voltage of the capacitor is stacked above LX to provide the necessary turn-on voltage ($V_{GS}$) for the high-side MOSFET. The controller then closes an internal switch between BST and DH to turn the high-side MOSFET on.

### Current-Sense Amplifier

The current-sense circuit amplifies the differential current-sense voltage ($V_{CS+}$ - $V_{CS-}$). This amplified current-sense signal and the internal slope-compensation signal are summed ($V_{SUM}$) together and fed into the PWM comparator's inverting input. The PWM comparator shuts off the high-side MOSFET when $V_{SUM}$ exceeds the integrated feedback voltage ($V_{COMP}$).

The differential current sense is also used to provide peak inductor current limiting. This current limit is more accurate than the valley current limit, which is measured across the low-side MOSFET's on-resistance.

### Current-Limit Circuit

The MAX8650 uses both foldback and peak current limiting (Figure 5). The valley foldback current limit is used to reduce power dissipation of external components, mainly inductor and power MOSFETs, and upstream power source, when output is severely overloaded or short circuited and POK is low. Thus, the circuit can withstand short-circuit conditions continuously without causing overheating of any component. The peak constant-current limit sets the current-limit point more accurately since it does not have to suffer the wide variation of the low-side power MOSFET's on-resistance due to tolerance and temperature.

The valley current is sensed across the on-resistance of the low-side MOSFET ($V_{PGND}$ - $V_{LX}$). The valley current limit trips when the sensed voltage exceeds the valley current-limit threshold. The valley current limit recovers when the sensed voltage drops below the valley current-limit threshold (except when using the latch-off option).

Set the minimum valley current-limit threshold, when the output voltage is at the nominal regulated value, higher than the maximum peak current-limit setting. With this method, the current-limit point accuracy is controlled by the peak current limit and is not interfered with by the wide variation of MOSFET on-resistance. See the *Setting the Current Limit* section for how to set these limits.

The MAX8650 can be configured for either an adjustable valley current-limit threshold with adjustable foldback ratio, or a fixed valley current limit that latches the converter off. When latch-off is used (MODE is connected to AVL), set the current-limit threshold by only one resistor from ILIM2 to GND and make sure this threshold is higher than the maximum output current required by at least a 20% margin. Cycle EN or input power to reset the current-limit latch.

The peak current limit is used to sense the inductor current, and is more accurate than the valley current limit since it does not depend upon the on-resistance of the low-side MOSFET. The peak current can be measured across the resistance of the inductor for the highest efficiency, or alternatively, a current-sense resistor can be used for more accurate current sensing. A resistor connected from ILIM1 to GND sets the peak current-limit threshold.

For more information on the current limit, see the *Setting the Current Limit* section.

### Switching Frequency and Synchronization

The MAX8650 has an adjustable internal oscillator that can be set to any frequency from 200kHz to 1.2MHz. To set the switching frequency, connect a resistor from FSYNC to GND. Calculate the resistor value from the following equation:

$$R_{FSYNC} = \left(\frac{1}{2f_S} - 162ns\right)\left(\frac{1k\Omega}{16.34ns}\right)$$

The MAX8650 can also be synchronized to an external clock by connecting the clock signal to FSYNC. In addition, SYNCO is provided to synchronize a second MAX8650 controller 180° out-of-phase with the first by connecting SYNCO of the first controller to FSYNC of the second. When the first controller is synchronized to an external clock, the external clock is inverted to generate SYNCO. Therefore, to get 180° out-of-phase operation, the clock input to the first controller should have a 50% duty cycle.

### Power-Good Signal (POK)

POK is an open-drain output on the MAX8650 that monitors the output voltage. When the output is above 92% of its nominal regulation voltage, POK is high impedance. When the output drops below 89% of its nominal regulation voltage, POK is internally pulled low. POK is also internally pulled low when the MAX8650 is shut down. To use POK as a logic-level signal, connect a pullup resistor from POK to the logic supply rail.

### Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX8650. When the junction temperature exceeds +160°C, an internal thermal sensor shuts down the device, allowing the IC to cool. The thermal sensor turns the IC on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous thermal-overload conditions.

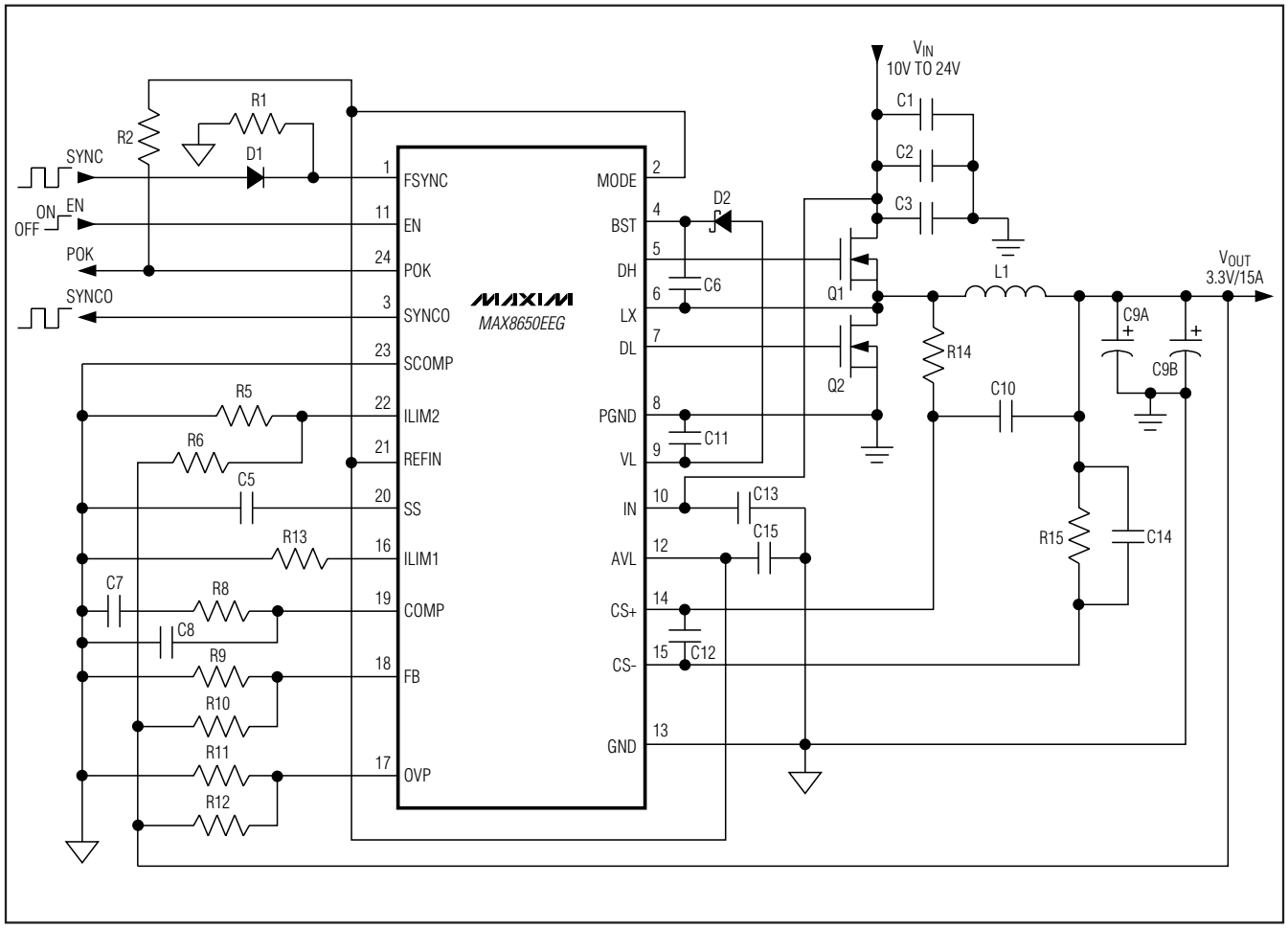



*Figure 3. Applications Circuit with 500kHz Switching, 10V to 24V Input, and 3.3V/15A Output*

# 4.5V to 28V Input Current-Mode Step-Down Controller with Adjustable Frequency

## Table 1. Component List for Figure 3

| COMPONENT | DESCRIPTION | VENDOR/PART | QUANTITY |
|---|---|---|---|
| C1, C2, C3 | 10µF, 25V X5R ceramic capacitors | TDK C3225X5R1E106M (1210) | 3 |
| C5, C6 | 0.1µF, 10V X7R ceramic capacitors | Kemet C0603C104M9RAC (0603) | 2 |
| C7 | 220pF, 50V X7R ceramic capacitor | TDK C1608X7R1H271K | 1 |
| C8 | Not installed | — | 0 |
| C9A, C9B | 150µF ±20%, 4V, 7mΩ ESR polymer aluminum electrolytic capacitors | Panasonic EEFSDOG151R | 2 |
| C10, C14 | 0.47µF ±10%, 10V X5R ceramic capacitors | Taiyo Yuden LMK107BJ474KA (0603) | 2 |
| C11 | 4.7µF, 10V X5R ceramic capacitor | TDK C2012X5R1A475M (0805) | 1 |
| C12 | 100pF, 25V C0G ceramic capacitor | Kemet C603C101K3GAC (0603) | 1 |
| C13, C15 | 1µF, 16V X5R ceramic capacitors | TDK C1608X7R1C105M (0603) | 2 |
| D1 | 100V, 200mA switching diode | Central CMPD914 (SOT23) | 1 |
| D2 | 30V, 100mA Schottky diode | Central CMPSH-3 (SOT23) | 1 |
| L1 | 1.2µH, 18.2A, 2.6mΩ max, 2.16mΩ typ inductor | TOKO FDA1254-1R2M | 1 |
| Q1 | 30V n-channel MOSFET | Fairchild FDS7296N3 | 1 |
| Q2 | 30V n-channel MOSFET | Fairchild FDS7088SN3 | 1 |
| R1 | 51.1kΩ ±1% resistor (0603) | — | 1 |
| R2 | 100kΩ ±5% resistor (0603) | — | 1 |
| R3 | 0Ω resistor | — | 1 |
| R4 | Not installed | — | 0 |
| R5 | 17.4kΩ ±1% resistor (0603) | — | 1 |
| R6 | 130kΩ ±1% resistor (0603) | — | 1 |
| R8 | 220kΩ ±5% resistor (0603) | — | 1 |
| R9, R11 | 7.5kΩ ±1% resistors (0603) | — | 2 |
| R10, R12 | 28.0kΩ ±1% resistors (0603) | — | 2 |
| R13 | 39.2kΩ ±1% resistor (0603) | — | 1 |
| R14 | 2.4kΩ ±5% resistor (0603) | — | 1 |
| R15 | 39.2kΩ ±5% resistor (0603) | — | 1 |

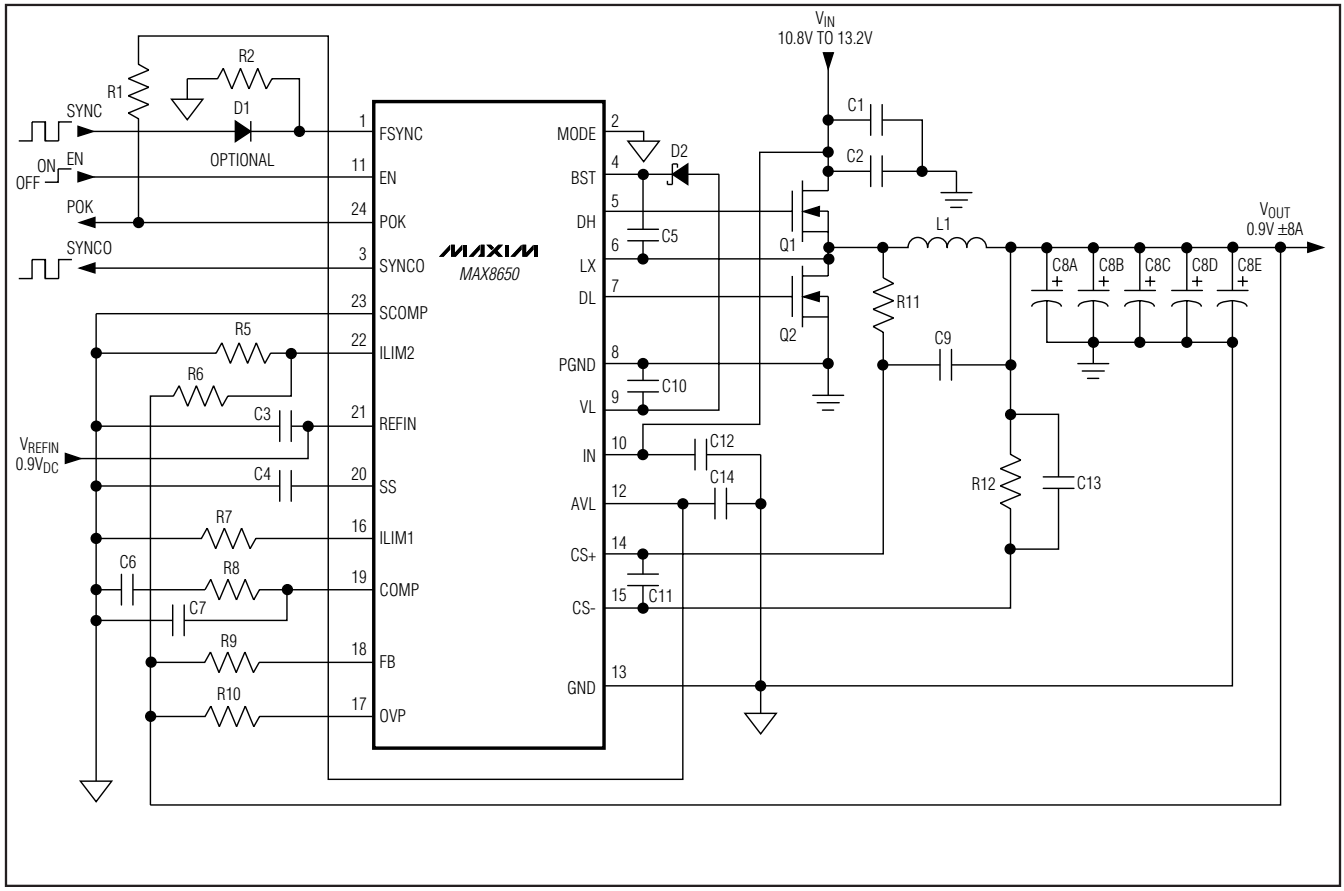



*Figure 4. Applications Circuit with 400kHz Switching, 12V Input, and 0.9V ±8A Output*

# 4.5V to 28V Input Current-Mode Step-Down Controller with Adjustable Frequency

## Table 2. Component List for Figure 4

| COMPONENT | DESCRIPTION | VENDOR / PART | QUANTITY |
|---|---|---|---|
| C1, C2 | 10µF, 16V X5R ceramic capacitors (1210) | Taiyo Yuden EMK325BJ106MN | 2 |
| C3 | 0.01µF, 10V X7R ceramic capacitor (0603) | Kemet C0603C103M9RAC | 1 |
| C4, C5 | 0.1µF, 10V X7R ceramic capacitors | Kemet C0603C104M9RAC | 2 |
| C6 | 1800pF, 50V X7R ceramic capacitor | TDK C1608X7R1H182K | 1 |
| C7 | X7% 22pF, 50V ceramic capacitor | TDK C1608C0G1H220K | 1 |
| C8A–C8E | 680µF/20%, 2.5V, 6mΩ ESR capacitors, POS Al Lytic | Sanyo 2R5TPD680M6 | 5 |
| C9, C13 | 10V ±10%, 0.47µF X5R ceramic capacitors (0603) | Taiyo Yuden LMK107BJ474KA | 2 |
| C10 | 4.7µF, 10V X5R ceramic capacitor (0805) | TDK C2012X5R1A475M | 1 |
| C11 | 100pF, 25V ceramic capacitor (C0G) | Kemet C0402C101K3GAC | 1 |
| C12, C14 | 1µF, 16V X5R ceramic capacitors (0603) | TDK C1608X7R1C105M | 2 |
| D1 | Diode, switching, 100V, 200mA | Central/CMPD914 | 1 |
| D2 | 30V, 100mA diode Schottky | Central/CMPSH-3 | 1 |
| L1 | 0.56µH, 15A, 1.7mΩ inductor | Panasonic ETQPLR56WFC | 1 |
| Q1 | 30V n-MOSFET, 8-pin SO | Vishay Si4346DY | 1 |
| Q2 | 30V n-MOSFET, 8-pin SO | Vishay Si4362DY | 1 |
| R1 | 100kΩ ±5% resistor (0603) | — | 1 |
| R2 | 66.5kΩ ±1% resistor (0603) | — | 1 |
| R3 | 0Ω resistor | — | 1 |
| R4 | Resistor, open | — | 0 |
| R5 | 16.2kΩ ±1% resistor (0603) | — | 1 |
| R6 | 35.7 kΩ ±1% resistor (0603) | — | 1 |
| R7 | 15.8kΩ ±1% resistor (0603) | — | 1 |
| R8 | 160kΩ ±5% resistor (0603) | — | 1 |
| R9, R10 | 10kΩ ±5% resistors (0603) | — | 2 |
| R11 | 1.5kΩ ±5% resistor (0603) | — | 1 |
| R12 | 1.1kΩ ±5% resistor (0603) | — | 1 |

## Table 3. Suggested Components Manufacturers

| MANUFACTURER | COMPONENTS | PHONE | WEBSITE |
|---|---|---|---|
| Central Semiconductor | Diodes | 631-435-1110 | www.centralsemi.com |
| Fairchild Semiconductor | MOSFETs | 972-910-8000 | www.fairchildsemi.com |
| Panasonic | Capacitors | 714-373-7939 | www.panasonic.com |
| Sumida | Inductors | 847-545-6700 | www.sumida.com |
| Taiyo Yuden | Capacitors | 408-573-4150 | www.t-yuden.com |
| TDK | Capacitors | 847-803-6100 | www.component.tdk.com |
| Vishay | MOSFETs | 402-564-3131 | www.vishay.com |

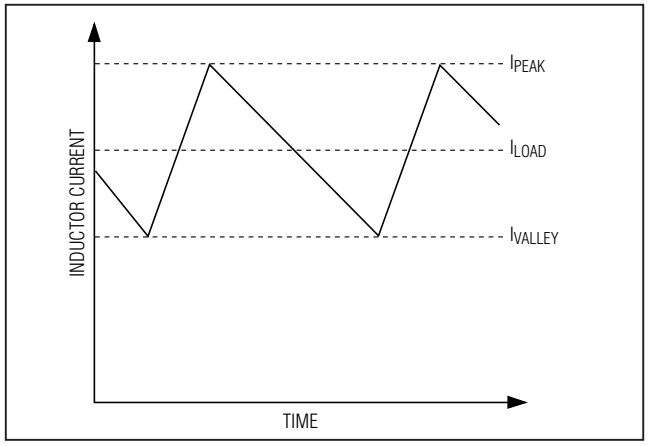



*Figure 5. Inductor-Current Waveform*

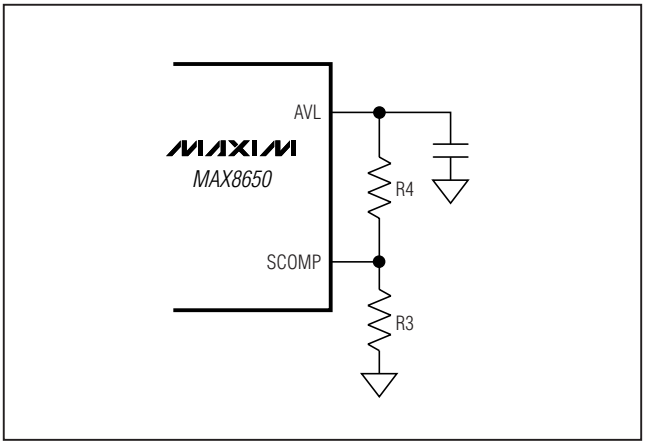



*Figure 6. Resistor-Divider for Setting the Slope Compensation*

## Design Procedure

### Setting the Output Voltage

To set the output voltage for the MAX8650, connect FB to the center of an external resistor-divider from the output to GND (R9 and R10 of Figure 3). Select R9 between 8kΩ and 24kΩ, and then calculate R10 with the following equation:

$$R10 = R9 \times \left( \frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where $V_{FB}$ = 0.7V. R9 and R10 should be placed as close to the IC as possible.

### Setting the Output Overvoltage Protection Threshold

To set the overvoltage threshold voltage for the MAX8650, connect OVP to the center of an external resistor-divider from the output to GND (R11 and R12 of Figure 3). Select R11 between 8kΩ and 24kΩ, then calculate R12 with the following equation:

$$R12 = R11 \times \left( \frac{V_{OUT}}{V_{OVP}} - 1 \right)$$

where $V_{OVP}$ = 0.8V when using the internal reference. When using an external reference, $V_{OVP}$ is 115% of $V_{REFIN}$.

### Setting the Slope Compensation

For most applications where the duty cycle is less than 50%, connect SCOMP to GND to set the slope compensation to the default of 125mV/T, where T is the oscillator period (T = 1 / $f_S$).

For a slope compensation of 250mV/T, connect SCOMP to AVL.

For applications with a duty cycle greater than 50%, set the SCOMP voltage with a resistor voltage-divider from AVL to GND (R3 and R4 in Figure 6). First, use the following equation to find the SCOMP voltage:

$$V_{SCOMP} = \frac{V_{OUT} \times 60 \times R_L}{f_S \times L}$$

where $R_L$ is the DC resistance of the inductor, and $f_S$ is the switching frequency.

Next, select a value for R3, typically 10kΩ, and solve for R4 as follows:

$$R4 = \frac{\left(5V - V_{SCOMP}\right) \times R3}{V_{SCOMP}}$$

This sets the slope-compensation voltage rate to $V_{SCOMP}$ / (10 x T).

### Inductor Selection

There are several parameters that must be examined when determining which inductor is to be used. Input voltage, output voltage, load current, switching frequency, and LIR. LIR is the ratio of inductor-current ripple to maximum DC load current. A higher LIR value allows for a smaller inductor, but results in higher losses and higher output ripple. A good compromise between size and efficiency is an LIR of 0.3. Once all the parameters are chosen, the inductor value is determined as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_S \times I_{LOAD(MAX)} \times LIR}$$

# 4.5V to 28V Input Current-Mode Step-Down Controller with Adjustable Frequency

where $f_S$ is the switching frequency. Choose a standard-value inductor close to the calculated value. The exact inductor value is not critical and can be adjusted to make trade-offs between size, cost, and efficiency. Lower inductor values minimize size and cost, but they also increase the output ripple and reduce the efficiency due to higher peak currents. On the other hand, higher inductor values increase efficiency, but eventually resistive losses due to extra turns of wire exceed the benefit gained from lower AC current levels. This is especially true if the inductance is increased without also increasing the physical size of the inductor. Find a low-loss inductor with the lowest possible DC resistance that fits the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 300kHz. The chosen inductor's saturation current rating must exceed the peak inductor current determined as:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{LIR}{2} \times I_{LOAD(MAX)}$$

## Setting the Current Limit

### Valley Current Limit

The MAX8650 has an adjustable valley current limit, configurable for foldback with automatic recovery, or a constant-current limit with latchup. To set the current limit for foldback mode, connect a resistor from ILIM2 to the output ($R_{FOBK}$), and another resistor from ILIM2 to GND ($R_{ILIM2}$). See Figure 7. The values of $R_{FOBK}$ and $R_{ILIM2}$ are calculated as follows:

1) First, select the percentage of foldback ($P_{FB}$). This percentage corresponds to the current limit when $V_{OUT}$ equals zero, divided by the current limit when $V_{OUT}$ equals its nominal voltage. A typical value of $P_{FB}$ is in the 15% to 40% range. A lower value of $P_{FB}$ yields lower short-circuit current. The following equations are used to calculate $R_{FOBK}$ and $R_{ILIM2}$:

$$R_{FOBK} = \frac{P_{FB} \times V_{OUT}}{5\mu A \times \left(1 - P_{FB}\right)}$$

$$R_{ILIM2} = \frac{5 \times R_{DS(ON)} \times I_{VALLEY} \times \left(1 - P_{FB}\right) \times R_{FOBK}}{V_{OUT} - \left[5 \times R_{DS(ON)} \times I_{VALLEY} \times \left(1 - P_{FB}\right)\right]}$$

where $I_{VALLEY}$ is the value of the inductor valley current at maximum load ($I_{LOAD(MAX)}$ - 1/2 x $I_{P-P}$), and $R_{DS(ON)}$ is the maximum on-resistance of the low-side MOSFET at the highest operating junction temperature.

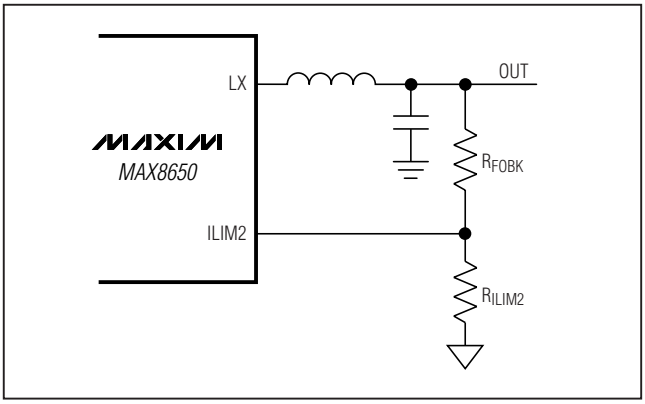



*Figure 7. ILIM2 Resistor Connections*

2) If the resulting value of $R_{ILIM2}$ is negative, either increase $P_{FB}$ or choose a low-side MOSFET with a lower $R_{DS(ON)}$. The latter is preferred as it increases the efficiency and results in a lower short-circuit current.

   To set the constant-current limit for the latchup mode, only $R_{ILIM2}$ is used. The equation for $R_{ILIM2}$ below sets the current-limit threshold at 1.2 times the maximum rated output current:

$$R_{ILIM2} = \frac{1.2 \times I_{VALLEY} \times R_{DS(ON)}}{1\mu A}$$

   Similarly, $I_{VALLEY}$ is the value of the inductor valley current at maximum load and $R_{DS(ON)}$ is the maximum on-resistance of the low-side MOSFET at the highest operating junction temperature.

### Peak Current Limit

The peak current-limit threshold ($V_{TH}$) is set by a resistor connected from ILIM1 to GND. $V_{TH}$ corresponds to the peak voltage across the sensing element (inductor or current-sense resistor), $R_{LIM1}$. $R_{LIM1}$ is calculated as follows:

$$R_{ILIM1} = \frac{8 \times V_{TH}}{10\mu A}$$

This allows a maximum DC output current ($I_{LIM}$) of:

$$I_{LIM} = \frac{V_{TH}}{R_{DC}} - \frac{I_{P-P}}{2}$$

where $R_{DC}$ is either the DC resistance of the inductor or the value of the optional current-sense resistor.

To ensure maximum output current, use the minimum value of $V_{TH}$ from each setting, and the maximum $R_{DC}$ values at the highest expected operating temperature.

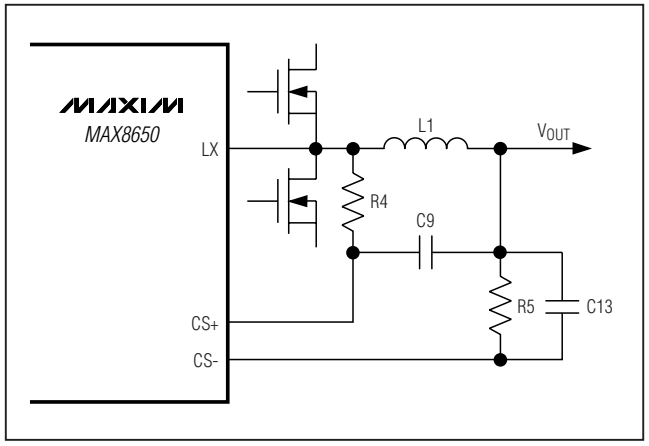



*Figure 8. Current Sense Using the Inductor's DC Resistance*

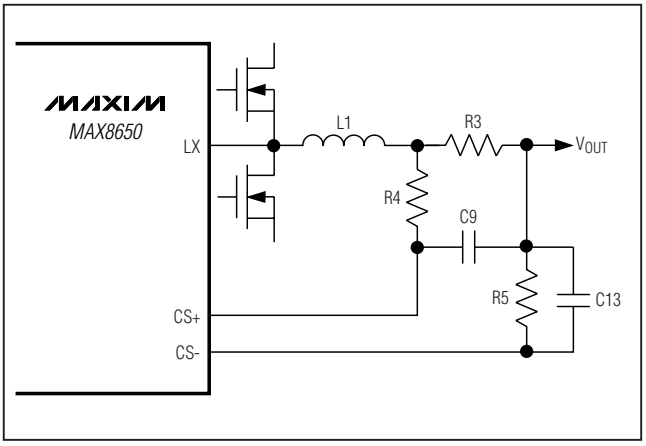



*Figure 9. Using a Current-Sense Resistor for Improved Current-Sense Accuracy*

The DC resistance of the inductor's copper wire has a +0.22%/°C temperature coefficient.

To use the DC resistance of the output inductor for current sensing, an RC circuit is added (see Figure 8). The RC time constant is set at twice the inductor ($L/R_{DC}$) time constant. Pick the value of C9 (typically 0.47µF), then calculate the resistor value from $R4 = 2L / (R_{DC} \times C9)$.

Add a resistor (R5 in Figure 8) to the CS- connection to minimize input offset error. Calculate the value of R5 as follows:

1) When $V_{OUT} \geq 2.4V$:

$$R5 = \frac{\left(20\mu A + \frac{R_{ILIM1} \times 10\mu A}{32k\Omega}\right) \times R4}{20\mu A}$$

2) When $V_{OUT} < 2.4V$:

$$R5 = \frac{15\mu A \times R4}{\left(15\mu A + \frac{R_{ILIM1} \times 10\mu A}{32k\Omega}\right)}$$

Capacitor C13 is connected in parallel with R5 and is equal in value to C9.

The equivalent current-sense resistance when using an inductor for current sensing is equal to the DC resistance of the inductor ($R_{DC}$).

### MOSFET Selection

The MAX8650 drives two or four external, logic-level, n-channel MOSFETs as the circuit switch elements. The key selection parameters are:

1) On-resistance ($R_{DS(ON)}$): the lower, the better.
2) Maximum drain-to-source voltage ($V_{DSS}$): should be at least 20% higher than the input supply rail at the high-side MOSFET's drain.
3) Gate charges ($Q_G$, $Q_{GD}$, $Q_{GS}$): the lower, the better.

For a 5V input application, choose the MOSFETs with rated $R_{DS(ON)}$ at $V_{GS} \leq 4.5V$. With higher input voltages, the internal VL regulator provides 6.5V for gate drive to minimize the on-resistance for a wide range of MOSFETs.

For a good compromise between efficiency and cost, choose the high-side MOSFET (N1, N2) that has conduction losses equal to switching losses at nominal input voltage and output current. The selected low-side MOSFET (N3, N4) must have an $R_{DS(ON)}$ that satisfies the current-limit-setting condition above. Make sure that the low-side MOSFET does not spuriously turn on due to dV/dt caused by the high-side MOSFET turning on, as this would result in shoot-through current and degrade the efficiency. MOSFETs with a lower $Q_{GD}/Q_{GS}$ ratio have higher immunity to dV/dt. For high-current applications, it is often preferable to parallel two MOSFETs rather than to use a single large MOSFET.

For proper thermal-management design, the power dissipation must be calculated at the desired maximum operating junction temperature, maximum output current, and worst-case input voltage (for the low-side MOSFET, worst case is at $V_{IN(MAX)}$; for the high-side MOSFET, it could be either at $V_{IN(MAX)}$ or $V_{IN(MIN)}$). The high-side and low-side MOSFETs have different loss components due to the circuit operation. The low-side MOSFET operates as a zero voltage switch; therefore, major losses are the channel-conduction loss ($P_{LSCC}$) and the body-diode conduction loss ($P_{LSDC}$).

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$$P_{LSCC} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times I_{LOAD}^2 \times R_{DS(ON)}$$

Use $R_{DS(ON)}$ at $T_{J(MAX)}$:

$$P_{LSDC} = 2 \times I_{LOAD} \times V_F \times t_{DT} \times f_S$$

where $V_F$ is the body-diode forward-voltage drop, $t_{DT}$ is the dead time between high-side and low-side switching transitions (30ns typ), and $f_S$ is the switching frequency.

The high-side MOSFET operates as a duty-cycle control switch and has the following major losses: the channel-conduction loss ($P_{HSCC}$), the VL overlapping switching loss ($P_{HSSW}$), and the drive loss ($P_{HSDR}$). The high-side MOSFET does not have body-diode conduction loss, unless the converter is sinking current, when the loss due to body-diode conduction is calculated as $P_{HSDC} = 2 \times I_{LOAD} \times V_F \times t_{DT} \times f_S$:

$$P_{HSCC} = \frac{V_{OUT}}{V_{IN}} \times I_{LOAD}^2 \times R_{DS(ON)}$$

Use $R_{DS(ON)}$ at $T_{J(MAX)}$:

$$P_{HSSW} = V_{IN} \times I_{LOAD} \times \frac{Q_{GS} + Q_{GD}}{I_{GATE}} \times f_S$$

where $I_{GATE}$ is the average DH driver output-current capability determined by:

$$I_{GATE} \cong \frac{0.5 \times V_{VL}}{R_{DS(ON)(DR)} + R_{GATE}}$$

where $R_{DS(ON)(DR)}$ is the high-side MOSFET driver's on-resistance (1.5Ω typ) and $R_{GATE}$ is the internal gate resistance of the MOSFET (~2Ω):

$$P_{HSDR} = Q_G \times V_{GS} \times f_S \times \frac{R_{GATE}}{R_{GATE} + R_{DS(ON)(DR)}}$$

where $V_{GS} \approx V_{VL}$.

In addition to the losses above, allow approximately 20% more for additional losses due to MOSFET output capacitances and low-side MOSFET body-diode reverse-recovery charge dissipated in the high-side MOSFET, but is not well defined in the MOSFET data sheet. Refer to the MOSFET data sheet for thermal-resistance specifications to calculate the PCB area needed to maintain the desired maximum operating junction temperature with the above calculated power dissipations.

To reduce EMI caused by switching noise, add a 0.1µF ceramic capacitor from the high-side switch drain to the low-side switch source or add resistors in series with DH and DL to slow down the switching transitions. However, adding series resistors increases the power dissipation of the MOSFET, so ensure this does not overheat the MOSFET.

### Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor must meet the ripple-current requirement ($I_{RMS}$) imposed by the switching currents defined by the following equation:

$$I_{RMS} = \frac{I_{LOAD}\sqrt{V_{OUT} \times \left(V_{IN} - V_{OUT}\right)}}{V_{IN}}$$

$I_{RMS}$ has a maximum value when the input voltage equals twice the output voltage ($V_{IN}$ = 2 x $V_{OUT}$), so $I_{RMS(MAX)} = I_{LOAD} / 2$. Ceramic capacitors are recommended due to their low ESR and ESL at high frequency with relatively low cost. Choose a capacitor that exhibits less than 10°C temperature rise at the maximum operating RMS current for optimum long-term reliability. Ceramic capacitors with X5R or better temperature characteristics are recommended.

### Output Capacitor

The key selection parameters for the output capacitor are the actual capacitance value, the equivalent series resistance (ESR), the equivalent series inductance (ESL), and the voltage-rating requirements. These parameters affect the overall stability, output voltage ripple, and transient response. The output ripple has three components: variations in the charge stored in the output capacitor, the voltage drop across the capacitor's ESR and ESL caused by the current into and out of the capacitor. The maximum output voltage ripple is estimated as follows:

$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)} + V_{RIPPLE(ESL)}$

The output voltage ripple as a consequence of the ESR, ESL, and output capacitance is:

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(ESL)} = \frac{V_{IN}}{L + ESL} \times ESL$$

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_S}$$

where $I_{P-P}$ is the peak-to-peak inductor current:

$$I_{P-P} = \frac{V_{IN} - V_{OUT}}{f_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

These equations are suitable for initial capacitor selection, but final values should be chosen based on a prototype or evaluation circuit. As a general rule, a smaller current ripple results in less output-voltage ripple. Since the inductor ripple current is a factor of the inductor value and input voltage, the output-voltage ripple decreases with larger inductance, and increases with higher input voltages. Ceramic, tantalum, or aluminum polymer electrolytic capacitors are recommended. The aluminum electrolytic capacitor is the least expensive; however, it has higher ESR. To compensate for this, use a ceramic capacitor in parallel to reduce the switching ripple and noise. For reliable and safe operation, ensure that the capacitor's voltage and ripple-current ratings exceed the calculated values.

The response to a load transient depends on the selected output capacitors. After a load transient, the output voltage instantly changes by ESR x $\Delta I_{LOAD}$. Before the controller can respond, the output voltage deviates further, depending on the inductor and output-capacitor values. After a short period (see the *Typical Operating Characteristics*), the controller responds by regulating the output voltage back to its nominal state. The controller response time depends on its closed-loop bandwidth. With a higher bandwidth, the response time is faster, thus preventing the output voltage from further deviation from its regulating value.

### Compensation Design

The MAX8650 uses an internal transconductance error amplifier whose output compensates the control loop. The external inductor, output capacitor, compensation resistor, and compensation capacitors determine the loop stability. The inductor and output capacitor are chosen based on performance, size, and cost. Additionally, the compensation resistor and capacitors are selected to optimize control-loop stability. The component values, shown in the circuits of Figures 3 and 4, yield stable operation over the given range of input-to-output voltages.

The controller uses a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor, so the MAX8650 uses the voltage drop across the DC resistance of the inductor or the alternate series current-sense resistor to measure the inductor current. Current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor resulting in a smaller phase shift and requiring a less elaborate error-amplifier compensation than voltage-mode control. A simple single-series $R_C$ and $C_C$ is all that is needed to have a stable, high-bandwidth loop in applications where ceramic capacitors are used for output filtering. For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed-loop crossover frequency. To stabilize a nonceramic output capacitor loop, add another compensation capacitor from COMP to GND to cancel this ESR zero.

The basic regulator loop is modeled as a power modulator, an output feedback-divider, and an error amplifier. The power modulator has DC gain set by $g_{mc}$ x $R_{LOAD}$, with a pole and zero pair set by $R_{LOAD}$, the output capacitor ($C_{OUT}$), and its ESR. Below are equations that define the power modulator:

$$G_{MOD(dc)} = g_{mc} \times \frac{R_{LOAD} \times f_S \times L}{R_{LOAD} + f_S \times L}$$

where $R_{LOAD} = V_{OUT} / I_{OUT(MAX)}$, $f_S$ is the switching frequency, L is the output inductance, and $g_{mc} = 1 / (A_{VCS} \times R_{DC})$, where $A_{VCS}$ is the gain of the current-sense amplifier (12 typ), and $R_{DC}$ is the DC resistance of the inductor.

Find the pole and zero frequencies created by the power modulator as follows:

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times \left( \frac{R_{LOAD} \times f_S \times L}{R_{LOAD} + f_S \times L} + ESR \right)}$$

$$f_{zMOD} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

When $C_{OUT}$ comprises "n" identical capacitors in parallel, the resulting $C_{OUT} = n \times C_{OUT(EACH)}$, and $ESR = ESR_{(EACH)} / n$. Note that the capacitor zero for a parallel combination of like capacitors is the same as for an individual capacitor. See Figures 10 and 11 for illustrations of the pole and zero locations.

The feedback voltage-divider has a gain of $G_{FB} = V_{FB} / V_{OUT}$, where $V_{FB}$ is equal to 0.75V.

# 4.5V to 28V Input Current-Mode Step-Down Controller with Adjustable Frequency

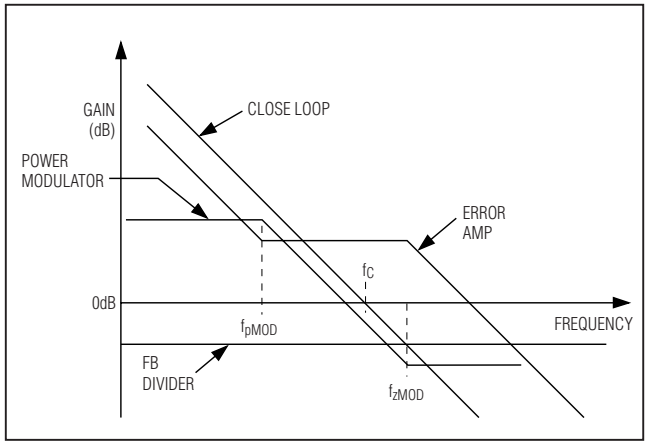



*Figure 10. Simplified Gain Plot for the $f_{ZMOD} > f_C$ Case*

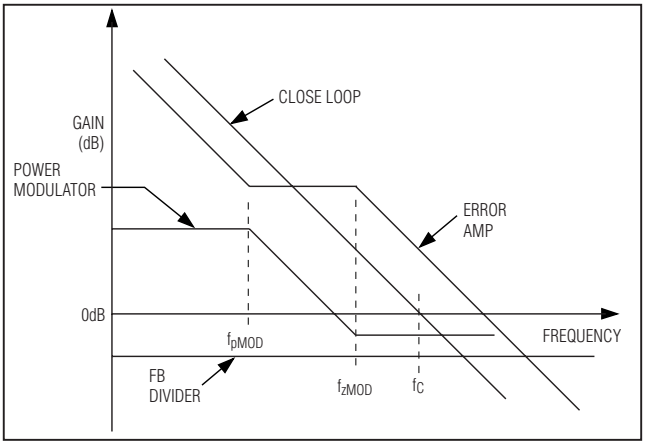



*Figure 11. Simplified Gain Plot for the $f_{ZMOD} < f_C$ Case*

The transconductance error amplifier has a DC gain, $G_{EA(DC)} = g_{mEA} \times R_O$, where $g_{mEA}$ is the error-amplifier transconductance, which is equal to 110µS, $R_O$ is the output resistance of the error amplifier, which is 30MΩ. A dominant pole is set by the compensation capacitor ($C_C$), the amplifier output resistance ($R_O$), and the compensation resistor ($R_C$), and a zero is set by the compensation resistor ($R_C$) and the compensation capacitor ($C_C$). There is an optional pole set by $C_F$ and $R_C$ to cancel the output-capacitor ESR zero if it occurs near the crossover frequency ($f_C$). Thus:

$$f_{pdEA} = \frac{1}{2\pi \times C_C \times (R_O + R_C)}$$

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C}$$

$$f_{pEA} = \frac{1}{2\pi \times C_F \times R_C}$$

The crossover frequency, $f_C$, should be much higher than the power-modulator pole $fp_{MOD}$. Also, $f_C$ should be less than or equal to 1/5 the switching frequency. Select a value for $f_C$ in the range:

$$f_{pMOD} << f_C \le \frac{f_S}{5}$$

At the crossover frequency, the total loop gain must equal 1, and is expressed as:

$$G_{EA(fc)} \times G_{MOD(fc)} \times \frac{V_{FB}}{V_{OUT}} = 1$$

**For the case where $f_{zMOD}$ is greater than $f_C$:**

$$G_{EA(fc)} = g_{mEA} \times R_C$$

$$G_{MOD(fc)} = G_{MOD(dc)} \times \frac{f_{pMOD}}{f_C}$$

Then $R_C$ can be calculated as:

$$R_C = \frac{V_{OUT}}{g_{mEA} \times V_{FB} \times G_{MOD(fc)}}$$

where $g_{mEA}$ = 110µS.

The error-amplifier compensation zero formed by $R_C$ and $C_C$ should be set at the modulator pole $fp_{MOD}$. Calculate the value of $C_C$ as follows:

$$C_C = \frac{R_{LOAD} \times f_S \times L \times C_{OUT}}{\left(R_{LOAD} + f_S \times L\right) \times R_C}$$

If $f_{zMOD}$ is less than 5 x $f_C$, add a second capacitor, $C_F$, from COMP to GND. The value of $C_F$ is:

$$C_F = \frac{1}{2\pi \times R_C \times f_{zMOD}}$$

As the load current decreases, the modulator pole also decreases; however, the modulator gain increases accordingly and the crossover frequency remains the same.

**For the case where $f_{zMOD}$ is less than $f_C$:**

The power modulator gain at $f_C$ is:

$$G_{MOD(fc)} = G_{MOD(dc)} \times \frac{f_{pMOD}}{f_{zMOD}}$$

The error-amplifier gain at $f_C$ is:

$$G_{EA(fc)} = g_{mEA} \times R_C \times \frac{f_{zMOD}}{f_C}$$

$R_C$ is calculated as:

$$R_C = \frac{V_{OUT}}{V_{FB}} \times \frac{f_C}{g_{mEA} \times G_{MOD(fc)} \times f_{zMOD}}$$

where $g_{mEA}$ = 110µS.

$C_C$ is calculated from:

$$C_C = \frac{R_{LOAD} \times f_S \times L \times C_{OUT}}{\left(R_{LOAD} + f_S \times L\right) \times R_C}$$

$C_F$ is calculated from:

$$C_F = \frac{1}{2\pi \times R_C \times f_{zMOD}}$$

Below is a numerical example to calculate $R_C$ and $C_C$ values of the typical operating circuit of Figure 3:

$A_{VCS}$ = 12

L = 1.2µH

$R_{DC}$ = 2.16mΩ

$f_S$ = 500kHz

$g_{mc}$ = 1 / ($A_{VCS}$ x $R_{DC}$) = 1 / (12 x 0.00216) = 38.6S

$V_{OUT}$ = 3.3V

$I_{OUT(MAX)}$ = 15A

$R_{LOAD}$ = $V_{OUT}$ / $I_{OUT(MAX)}$ = 3.3 / 15 = 0.22Ω

$C_{OUT}$ = 300µF

ESR = 3.5mΩ

$$G_{MOD(dc)} = g_{mc} \times \frac{R_{LOAD} \times f_S \times L}{R_{LOAD} + f_S \times L}$$

$$= 38.6 \times \frac{0.22 \times (500 \times 10^3) \times \left(1.2 \times 10^{-6}\right)}{0.22 + (500 \times 10^3) \times \left(1.2 \times 10^{-6}\right)} = 6.22$$

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times \left(\frac{R_{LOAD} \times f_S \times L}{R_{LOAD} + f_S \times L} + ESR\right)}$$

$$= \frac{1}{2\pi \times (300 \times 10^{-6}) \times \left(\frac{0.22 \times (500 \times 10^3) \times \left(1.2 \times 10^{-6}\right)}{0.22 + (500 \times 10^3) \times \left(1.2 \times 10^{-6}\right)} + 0.0035\right)}$$

$$= 3.23kHz$$

$$f_{pMOD} << f_C \le \frac{f_S}{5}$$

3.23kHz << $f_C$ ≤ 100kHz, select $f_C$ = 100kHz:

$$f_{zMOD} = \frac{1}{2\pi \times C_{OUT} \times ESR} = \frac{1}{2\pi \times (300 \times 10^{-6}) \times 0.0035} = 152kHz$$

Since $f_{zMOD}$ > $f_C$:

$$G_{MOD(fc)} = G_{MOD(dc)} \times \frac{f_{pMOD}}{f_C} = 6.22 \times \frac{3230}{100 \times 10^3} = 0.201$$

$$R_C = \frac{V_{OUT}}{g_{mEA} \times V_{FB} \times G_{MOD(fc)}}$$

$$= \frac{3.3}{\left(110 \times 10^{-6}\right) \times 0.7 \times 0.201} = 199k\Omega$$

Select the nearest standard value: $R_C$ = 200kΩ:

$$C_C = \frac{R_{LOAD} \times f_S \times L \times C_{OUT}}{\left(R_{LOAD} + f_S \times L\right) \times R_C}$$

$$= \frac{0.22(500 \times 10^3) \times (1.2 \times 10^{-6}) \times (300 \times 10^{-6})}{\left(0.22 + (500 \times 10^3) \times (1.2 \times 10^{-6})\right) \times (200 \times 10^3)} = 241p$$

Select the nearest standard value: $C_C$ = 270pF:

$$C_F = \frac{1}{2\pi \times R_C \times f_{zMOD}} = \frac{1}{2\pi \times (200 \times 10^3) \times (152 \times 10^3)} = 5.2pF$$

Since the calculated value for $C_F$ is very small (close to the parasitic capacitance present at COMP), it is not necessary:

R8 = $R_C$ = 200kΩ

C7 = $C_C$ = 270pF

C8 = $C_F$ = Not installed

# 4.5V to 28V Input Current-Mode Step-Down Controller with Adjustable Frequency

## Applications Information

### PCB Layout Guidelines

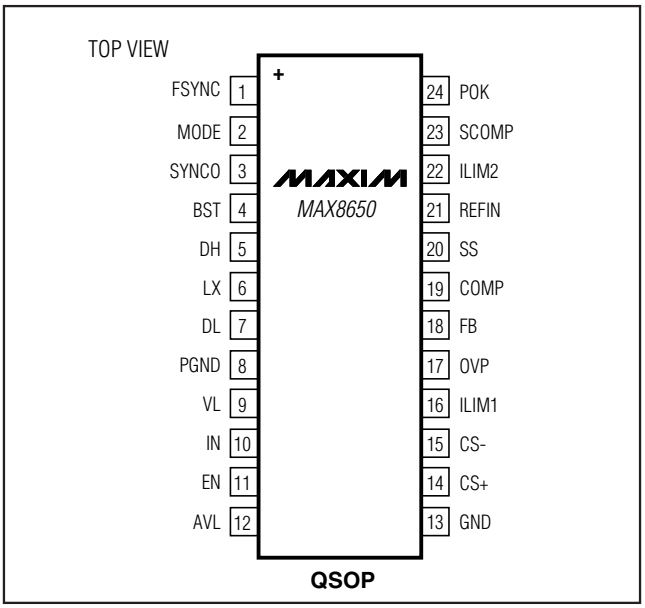
Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. Follow these guidelines for good PCB layout:

1) Place IC decoupling capacitors as close to IC pins as possible. Keep the power ground plane and signal ground plane separate. Place the input ceramic decoupling capacitor directly across and as close as possible to the high-side MOSFET's drain and the low-side MOSFET's source. This is to help contain the high switching current within this small loop.
2) For output current greater than 10A, a multilayer PCB is recommended. Pour a signal ground plane in the second layer underneath the IC to minimize noise coupling.
3) Connect input, output, and VL capacitors to the power ground plane; connect all other capacitors to the signal ground plane.
4) Place the inductor current-sense resistor and capacitor as close to the inductor as possible. Make a Kelvin connection to minimize the effect of PCB trace resistance. Place the input-bias balance resistor (R5 in Figures 8 and 9) near CS-. Run two closely parallel traces from across the capacitor (C9 in Figures 8 and 9) to CS+ and CS-.
5) Place the MOSFET as close as possible to the IC to minimize trace inductance of the gate-drive loop. If parallel MOSFETs are used, keep the trace lengths to both gates equal.
6) Connect the drain leads of the power MOSFET to a large copper area to help cool the device. Refer to the power MOSFET data sheet for recommended copper area.
7) Place the feedback and compensation components as close to the IC pins as possible. Connect the feedback resistor-divider from FB to the output as close as possible to the farthest output capacitor.
8) Refer to the MAX8650 evaluation kit for an example layout.

## Chip Information

PROCESS: BiCMOS

## Pin Configuration




## Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 24 QSOP | E24-1 | **21-0055** |

# 4.5V to 28V Input Current-Mode Step-Down Controller with Adjustable Frequency

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 1/06 | Initial release | — |
| 1 | 8/08 | Updated Table 1 and added *Package Information* table. | 14, 19, 25 |

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