*Click **here** to ask about the production status of specific part numbers.*

MAX77975/MAX77976 19VIN, 3.5/5.5A 1-Cell Li+ Battery Charger with Smart Power Selector and OTG for USBC PD

General Description

The MAX77975/MAX77976 is a high-performance high-input 3.5/5.5A fast charger with Smart Power Selector™. The IC can operate as a reverse boost without an additional inductor, allowing the battery to share its power through the charging port and is voltage programmable from 5V to 12V. The device features fully integrated low-loss power switches to provide small solution size and high-efficiency, even at high input voltage and high charging current. Its high switching frequency allows the use of a smaller sized inductor. The IC features true load disconnection in reverse boost mode and has an adjustable output current protection limit. The device is highly flexible and programmable through I^2C configuration.

The battery charger includes a Smart Power Selector to accommodate a wide range of battery sizes and system loads. The Smart Power Selector allows the system to start-up gracefully as soon as an input source is available, even when the battery is deeply discharged (dead battery) or missing. It can be configured so that when power is applied to the charger input, the battery charging can automatically start.

Applications

- Gaming Devices
- VR Applications
- mPOS
- Tablet PCs

Benefits and Features

- High-Efficiency Single-Cell Switching Charger
  - Up to 5.5A Charging with MAX77976
  - 91.2% Buck Efficiency at 4A, 12V Input
  - 90.5% Charging Efficiency at 3.5A, 9V Input
  - Optimized for High Voltage Input Operation
  - Accelerate Charge Time by Monitoring Kelvin Sensing Battery Voltage
  - Up to 3.2A Input Current Limit with AICL
- +28V Absolute Maximum Input Voltage Rating
- 4.7V to 19V Input Operating Voltage Range
- Reverse Boost with Programmable Output Voltage Options up to 12V
  - Up to 18W for MAX77976
  - Up to 12W for MAX77975
- Integrated Battery True-Disconnect FET
  - R_{DSON} = 7.7mΩ
  - Discharge Current up to 10A
  - Support Shipping Mode and Low Battery Leakage Current
  - 1.3MHz/2.6MHz Switching Frequency with 1µH/0.47µH Inductor
  - Disconnect Input (DISQBAT)
- Safety
  - Battery Temperature Sensing and Charge Safety Timer
  - JEITA Guideline Compliant
  - Thermal Regulation and Thermal Shutdown
  - System Voltage OVLO/UVLO
- Charge Status Output for LED
- Push-Button Input for Exiting from Ship Mode
- External Discharge FET Enable Output
- Dedicated Input for Suspend Mode (SUSPND)
- I^2C Interface
- 4mm x 4mm FC2QFN

***Ordering Information** appears at end of data sheet.*

19-100876; Rev 2; 7/21

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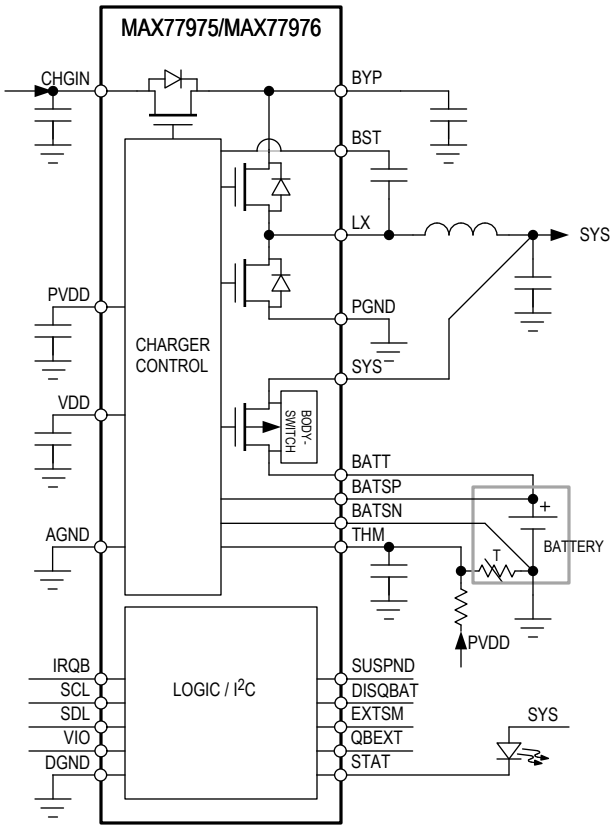
Simplified Block Diagram



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BYP to LX ..... -0.3V to +28V
LX to PGND ..... -0.3V to +22V
BST to PVDD ..... -0.3V to +22V
BST to LX ..... -0.3V to +2.2V
SYS to AGND ..... -0.3V to +6.0V
BATT to AGND ..... -0.3V to +6.0V
BATSP to AGND ..... -0.3V to V_{BATT} +0.3V
BATSP to BATT ..... -0.3V to +0.3V
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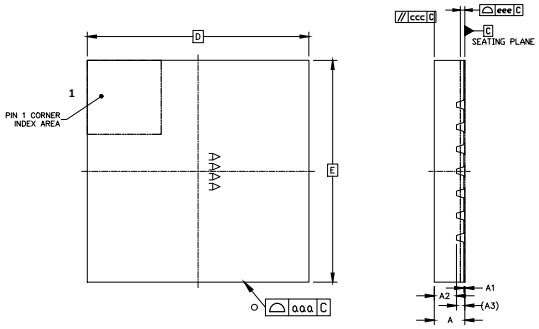
DISQBAT, SUSPEND, QBEXT to AGND ..... -0.3V to +6.0V
EXTSM to AGND ..... -0.3V to V_{BATT} +0.3V
IRQB, STAT to AGND ..... -0.3V to +6.0V
THM to AGND ..... -0.3V to V_{PVDD}+0.3V
SDA, SCL to AGND ..... -0.3V to +6.0V
CHGIN, BYP Continuous Current ..... 3.4A_{RMS}
LX, PGND Continuous Current ..... 5.7A_{RMS}
SYS, BATT Continuous Current ..... 10.0A_{RMS}
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, deration is 35.34mW/°C above +70°C) ..... mW to 2826.86mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

FCQFN

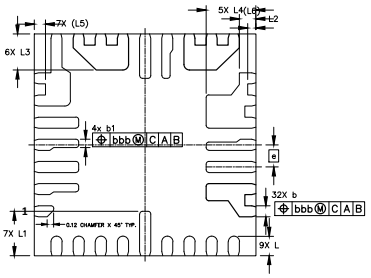
Package Code	F234A4F+1
Outline Number	21-100411
Land Pattern Number	90-100145
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	28.30°C/W
Junction to Case (θ_{JC})	6.65°C/W



TOP VIEW

SIDE VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b1	0.15	0.2	0.25
		b2	0.1	0.15	0.2
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
LEAD LENGTH		L	0.25	0.35	0.45
		L1	0.7	0.8	0.9
		L2	0.2	0.3	0.4
		L3	0.55	0.65	0.75
		L4	0.8	0.9	1
LEAD EDGE TO PKG EDGE		L5		0.2 REF	
		L6		0.15 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	



BOTTOM VIEW

NOTES
1. REFER TO JEDEC MO-220;
2. COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET SPECS;
4. FINISH: Cu/EP· Sn8~20s
5. MAXIM PKG CODE : F234A4F-1
6. MATERIAL MUST BE COMPLIANT WITH MAXIM SPECIFICATION 10-0131 FOR SUBSTANCE CONTENT, MUST BE Eu ROHS COMPLIANT WITHOUT EXEMPTION AND PB-FREE.

-DRAWING NOT TO SCALE-

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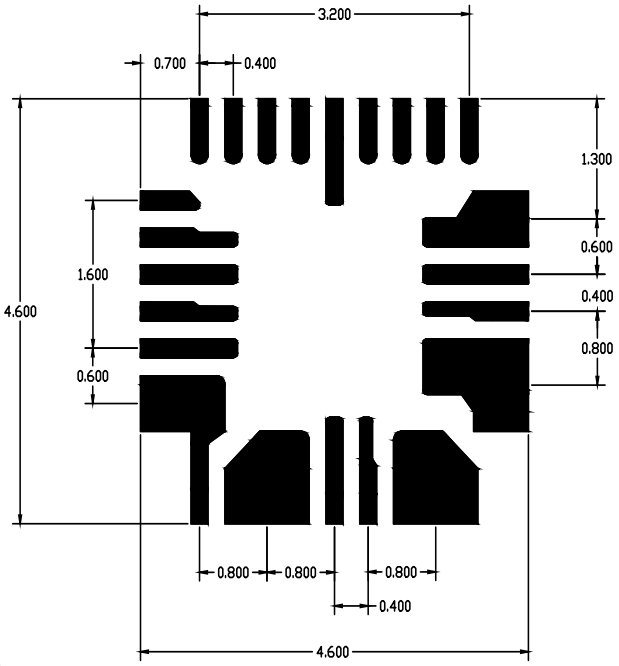
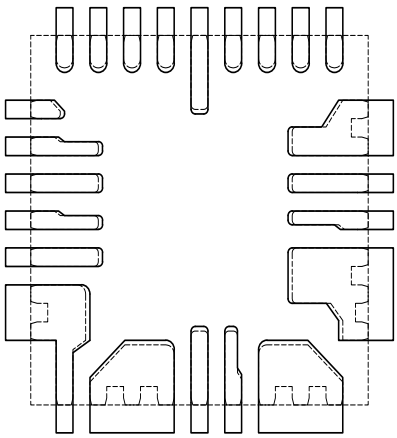
TITLE:
PACKAGE OUTLINE, 23L FC2QFN
4x4x0.55mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
ZHEN LI	21-100411	C	1/1

RECOMMENDED LAND PATTERN



PACKAGE OVERLAY



NOTES:
1. REFERENCE PKG. OUTLINE: 21-100411
2. LAND PATTERN COMPLIES TO: IPC7351A.
3. TOLERANCE: +/- 0.02 MM.
4. ALL DIMENSIONS APPLY TO LEADED, PbFREE PACKAGES.
5. ALL DIMENSIONS IN MM.

—DRAWING NOT TO SCALE—

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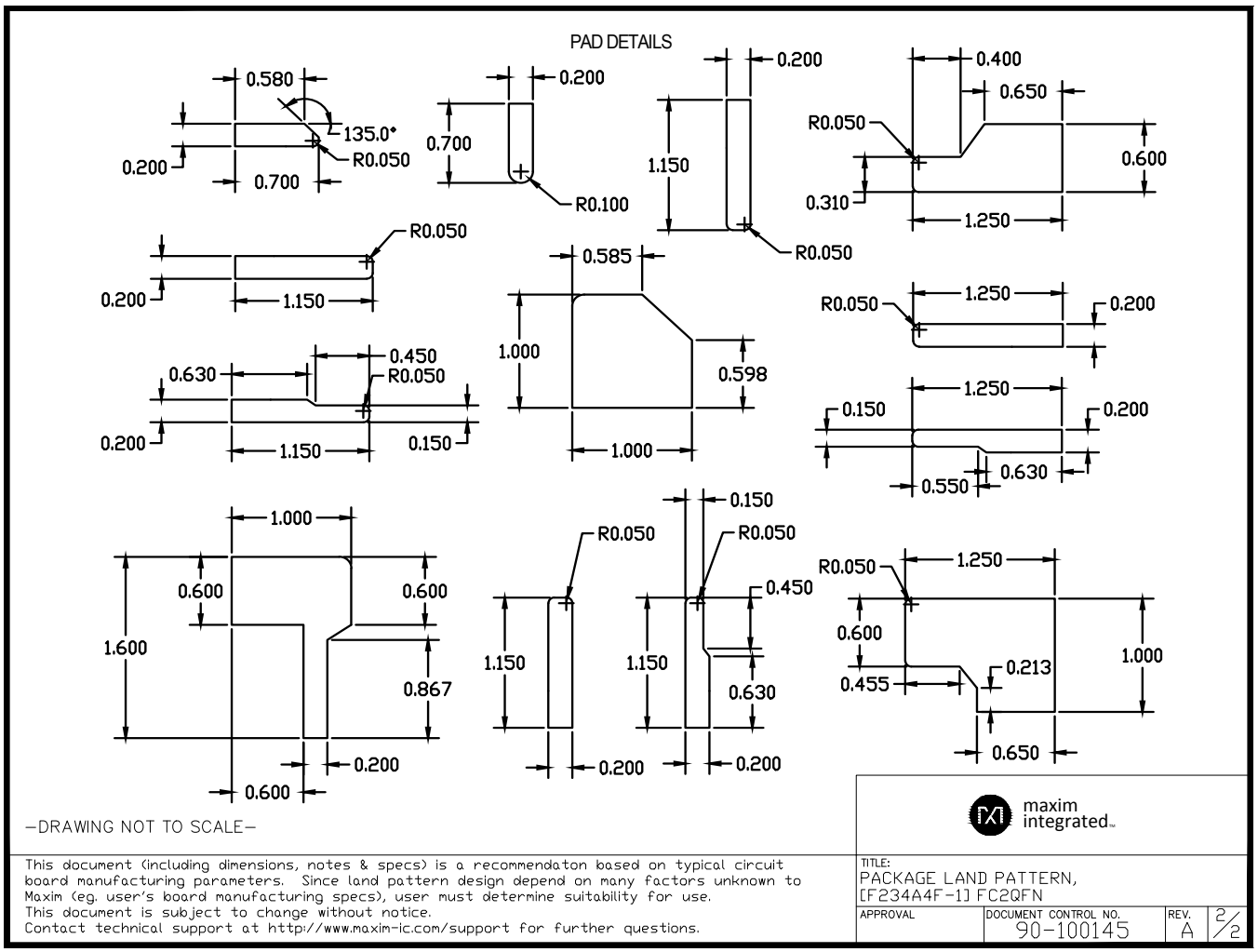
This document (including dimensions, notes & specs) is a recommendaton based on typical circuit board manufacturing parameters. Since land pattern design depend on many factors unknown to Maxim (eg. user's board manufacturing specs), user must determine suitability for use.
This document is subject to change without notice.
Contact technical support at http://www.maxim-ic.com/support for further questions.

TITLE:
PACKAGE LAND PATTERN,
[F234A4F-1] FC2QFN

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	90-100145	A	1/2



For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V, unless otherwise specified. Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL ELECTRICAL CHARACTERISTICS						
CHGIN Quiescent Current	I_{CHGIN}	V_{CHGIN} = 5.0V, SUSPEND pin digital high or MODE = 0, DEEP_SUSP_DIS = 1		0.19	0.38	mA
		V_{CHGIN} = 5.0V, SUSPEND pin digital high or MODE = 0, DEEP_SUSP_DIS = 0		85		µA
		V_{CHGIN} = 5.0V, V_{BATT} = 4.2V, MODE = 5, DONE state (V_{SYS} = 4.35V), I_{SYS} = 0A		2.35		mA
Input Undervoltage Supply Current	I_{IN}	V_{CHGIN} = 2.4V, the input is undervoltage		0.035		mA
BAT Quiescent Current	I_{BAT}	V_{CHGIN} = 0V, V_{BATT} = 3.6V, Q_{BATT} FET is on, LPM = 0, I_{SYS} = 0A		29		µA
BAT Quiescent Current in Low-Power Mode	I_{BAT}	V_{CHGIN} = 0V, V_{BATT} = 3.6V, Q_{BATT} FET is on, LPM = 1, I_{SYS} = 0A		22		µA
BAT Quiescent Current in Factory-Ship Mode	I_{BAT}	V_{CHGIN} = 0V, V_{BATT} = 3.6V, Q_{BATT} FET is off, V_{SYS} = V_{VDD} = 0V, factory-ship mode		3		µA
BAT Quiescent Current in Done State	I_{MBDN}	V_{CHGIN} = 5V, I_{BYP} = 0A, V_{BATT} = 4.2V, I_{SYS} = 0A, Q_{BATT} FET is off, MODE = 5, done state		7.5	10.5	µA
SYS Operating Voltage	V_{SYS}	Guaranteed by $V_{SYS\_UVLO\_R}$ and $V_{SYS\_OVLO\_R}$	$V_{SYS\_UVLO\_R}$		$V_{SYS\_OVLO\_R}$	V
VIO Voltage Range	V_{VIO}		1.62		5.5	V
SCL, SDA Input Low Level	$V_{SCL\_SDA\_IN\_L}$	T_A = +25°C			0.3 x V_{VIO}	V
SCL, SDA Input High Level	$V_{SCL\_SDA\_IN\_H}$	T_A = +25°C	0.7 x V_{VIO}			V
SCL, SDA Input Hysteresis	$V_{SCL\_SDA\_HYS}$	T_A = +25°C		0.05 x V_{VIO}		V
SCL, SDA Logic Input Current	I_{SCL_SDA}	V_{SCL} = V_{SDA} = V_{VIO} = 1.9V	-10		+10	µA
SDA Output Low Voltage	$V_{SDA\_OUT\_L}$	I_{SDA} = 20mA sinking			0.4	V
IRQB Output Low Voltage	$V_{IRQB\_OUT\_L}$	I_{IRQB} = 1mA sinking			0.4	V
IRQB Output High Leakage	I_{IRQB_H}	V_{IRQB} = 5.5V, T_A = 2+5°C	-1	0	+1	µA
		V_{IRQB} = 5.5V, T_A = +85°C		0.1		
CHGIN INPUT LIMITER						
CHGIN Operating Voltage Range	V_{CHGIN}	V_{CHGIN} must be less than V_{CHGIN_OVLO} and greater than both V_{CHGIN_UVLO} and (V_{SYS} + $V_{CHGIN2SYS\_TH}$) for the charger to turn-on	V_{CHGIN_UVLO}		V_{CHGIN_OVLO}	V
CHGIN Overvoltage Threshold	V_{CHGIN_OVLO}	V_{CHGIN} rising	19	19.5	20	V
CHGIN Overvoltage Threshold Hysteresis	$V_{CHGIN\_OVLO\_HYS}$			500		mV

Electrical Characteristics (continued)

(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V, unless otherwise specified. Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHGIN Undervoltage Threshold Setting Range	V_{CHGIN_UVLO}	V_{CHGIN} rising, 20% hysteresis, programmable at 4.7V, 4.8V, 4.9V, 5.05V	4.7		5.05	V
CHGIN Undervoltage Threshold Accuracy	$V_{CHGIN\_UVLO\_ACC}$	V_{CHGIN} rising, 4.7V setting	4.6	4.7	4.8	V
CHGIN to SYS Undervoltage Threshold Rising	$V_{CHGIN2SYS\_TH}$	V_{CHGIN} - V_{SYS}, rising	0.12	0.20	0.28	V
CHGIN Turn-On Threshold Validation Delay	t_{D-UVLO}	Delay from V_{CHGIN} > V_{CHGIN_UVLO} to Q_{CHGIN} FET enable		8		ms
CHGIN Switching Start Delay	t_{START}	Delay from Input Validation to LX switching (if charge or buck mode is selected and charger is not suspended); see the *Input Validation* section for input validation conditions		150		ms
CHGIN Adaptive Voltage Regulation Threshold Setting Range	V_{CHGIN_REG}	Programmable at 4.5V, 4.6V, 4.7V, 4.85V. The input voltage regulation loop decreases the input current to regulate V_{CHGIN} at V_{CHGIN_REG} under weak input source conditions. If the input current is decreased to I_{IULO_DET} and the input voltage is equal or below V_{CHGIN_REG}, then the charger input is turned off.	4.5		4.85	V
CHGIN Adaptive Voltage Regulation Threshold Accuracy	$V_{CHGIN\_REG\_ACC}$	4.5V setting	4.4	4.5	4.6	V
CHGIN Input Current Limit Setting Range	$I_{INLIMIT}$	Programmable, 500mA default, 50mA step, production tested at 100mA, 500mA, 1000mA, 1800mA, and 3200mA settings only	0.1		3.2	A
CHGIN Input Current Limit Accuracy	$I_{INLIMIT}$	Charger enabled, 500mA input current limit setting	440	470	500	mA
		Charger enabled, 1000mA input current limit setting	880	940	1000	
		Charger enabled, 1800mA input current limit setting	1584	1692	1800	
		Charger enabled, 3200mA input current limit setting	2816	3008	3200	
CHGIN Input Current Low Threshold	I_{IULO_DET}	Charger enabled, 3200mA input current limit setting		60		mA
SYSTEM BUCK						
Buck Output Voltage Setting Range (Tracking Disabled)	V_{SYSREG}	Programmable 4.15V to 4.46V in 10mV steps (5-bits). Production tested at 4.2V only.	4.15		4.46	V

Electrical Characteristics (continued)

(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V, unless otherwise specified. Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Buck Output Voltage Accuracy (Tracking Disabled)	V_{SYSREG_ACC}	Buck only, charging disabled	-3		+3	%
Buck Output Voltage (Tracking Enabled)	$V_{SYSREG\_TRK\_MIN}$	MODE = 4, SYS Tracking mode enabled, $V_{BATT} < V_{SYS\_MIN}/1.04$	3.48	3.60	3.72	V
	V_{SYSREG_TRK}	MODE = 4, SYS Tracking mode enabled, $V_{BATT} \geq V_{SYS\_MIN}/1.04$, V_{SYSREG_TRK} represented as a percentage of V_{BATT}		104		%
Buck Inductor Current Limit	I_{HSILIM}	For MAX77976	8.5	9.5	10.5	A
	I_{HSILIM}	For MAX77975	5.95	7.00	8.05	
Buck Minimum On Time	t_{ON-MIN}	Measured on LX		100		ns
Buck Minimum Off Time	$t_{OFF-MIN}$	Measured on LX		100		ns
System Power-Up Current (from BYP)	I_{SYSPU_BYP}	Charger present, $V_{SYS} < V_{SYS\_UVLO\_R}$	50	75	100	mA
System Power-Up Time-Out (from BYP)	t_{SYSPU_BYP}			150		ms
CHARGER						
Precharge Charge Current	I_{PRECHG}	$V_{BATT} < V_{PRECHG}$	40	55	80	mA
Precharge Voltage Threshold	V_{PRECHG}	V_{BATT} rising	2.4	2.5	2.6	V
Precharge Voltage Threshold Hysteresis	V_{PRECHG_HYS}			500		mV
Trickle Charge Current	$I_{TRICKLE}$	TKEN = 1 by default, $V_{PRECHG} < V_{BATT} < V_{TRICKLE}$	270	300	330	mA
Trickle Charge Voltage Threshold	$V_{TRICKLE}$	V_{BATT} rising, TKEN = 1 by default	3.0	3.1	3.2	V
Trickle Charge Voltage Threshold Hysteresis	$V_{TRICKLE\_HYS}$	TKEN = 1 by default		100		mV
Prequalification Time	t_{PQ}	Applies to the total time of precharge and trickle charge mode		30		min
Fast-Charge Current Setting Range	I_{FC}	100mA to 5500mA in 50mA steps; production tested at 500mA, 1000mA, 3000mA, and 5000mA settings (MAX77976 only)	0.1		5.5	A
		100mA to 3500mA in 50mA steps; production tested at 500mA, 1000mA, and 3000mA settings (MAX77975 only)	0.1		3.5	
Fast-Charge Current Accuracy	I_{FC_ACC}	Programmed $I_{FC} \geq 500mA$, $V_{BATT} > V_{SYSMIN}$, T_A = +25°C	-3.5		+3.5	%
		Programmed $I_{FC} \geq 500mA$, $V_{BATT} > V_{SYSMIN}$, T_A = 0°C to +85°C	-6		+6	
		Programmed $I_{FC} \geq 500mA$, $V_{TRICKLE} < V_{BATT} < V_{SYSMIN}$ (LDO mode), T_A = -5°C to +85°C	-10		+10	

Electrical Characteristics (continued)

(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V, unless otherwise specified. Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fast-Charge Current Thermal Regulation Setting Range	T_{REG}	Junction temperature when charge current starts to reduce for thermal regulation; programmable from +85°C to +130°C in 5°C steps; default value is +115°C	85		130	°C
Fast-Charge Current Thermal Regulation Gain	A_{TJREG}	The charge current is decreased 5.73% of the fast-charge current full-scale for every degree that the junction temperature exceeds the thermal regulation temperature. This slope ensures that the full-scale current of 5.5A is reduced to 0A by the time the junction temperature is +17.5°C above the programmed loop set point. For lower programmed charge currents such as 480mA, this slope is valid for charge current reductions down to 80mA; below 100mA the slope becomes shallower but the charge current is reduced to 0A if the junction temperature is +20°C above the programmed loop set point.		-315		mA/°C
Fast-Charge Termination Voltage Setting Range	$V_{BATTREG}$	Programmable from 4.15V to 4.46V in 10mV steps (5-bits); production tested at 4.2V and 4.35V only	4.15		4.46	V
Fast-Charge Termination Voltage Accuracy at Room Temp	$V_{BATTREG\_ACC}$	$V_{BATTREG}$ = 4.35V setting, represented as percentage of $V_{BATTREG}$; T_A = +25°C	-0.6	-0.3	+0.0	%
Fast-Charge Termination Voltage Accuracy	$V_{BATTREG\_ACC}$	$V_{BATTREG}$ = 4.35V setting, represented as percentage of $V_{BATTREG}$; T_A = -5°C to +85°C	-0.8	-0.3	+0.2	%
Fast-Charge Termination Debounce Time	t_{TERM}			30		ms
Fast-Charge Constant Current + Constant Voltage Safety Time	t_{FC}	Adjustable from 3hrs, 4hrs, 5hrs, 6hrs, 7hrs, 8hrs including a disable setting; 5hrs default		5		hrs
Top-Off Current Setting Range	I_{TO}	Programmable from 150mA to 850mA with 50mA in 16 steps; production tested at 150mA, 200mA, 500mA, and 850mA settings	150		850	mA
Top-Off Current Accuracy	I_{TO_ACC}	150mA setting	122.5		177.5	mA
		200mA setting	170		230	
		500mA setting	455		545	
		850mA setting	787.5		912.5	
Top-Off Time	t_{TO}	Adjustable from 30sec to 70min in 10min steps; default setting is 30min		30		min

Electrical Characteristics (continued)

(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V, unless otherwise specified. Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Charge Restart Threshold Setting Range	V_{RSTRT}	Adjustable at 100mV, 150mV, and 200mV; it can also be disabled	100	150	200	mV
Charge Restart Debounce Time	t_{CRDG}			130		ms
Charge State Change Interrupt Debounce Time	t_{SCIDG}	Excludes transition to timer fault state, watchdog timer state		30		ms
Charge Watchdog Time	t_{WD}			80		s
Charge Timers Accuracy	t_{ACC}		-20		+20	%
Charge-Overvoltage Threshold	V_{COV}	V_{BAT_SP} - V_{BAT_SN}, relative to $V_{CHG\_CV\_PRM}$		200		mV
Remote Sense BAT_SP Input Current in Charging Mode	$I_{BAT\_SP\_CHG}$	V_{BATT_SP} = V_{BATT} = 3.8V, MODE = 5, T_A = +25°C		14		µA
Remote Sense BAT_SN Input Current in Charging Mode	$I_{BAT\_SN\_CHG}$	V_{BATT_SN} = 0, MODE = 5, T_A = +25°C		10		µA
SMART POWER SELECTOR						
System Regulation Voltage (Charging Enabled, Low Battery)	V_{SYSMIN}	Charging enabled, V_{BATT} < V_{SYSMIN} - V_{SYSTRK}	3.492	3.600	3.708	V
	V_{SYSTRK}	Charging enabled, V_{SYSMIN} - V_{SYSTRK} < V_{BATT} < V_{SYSMIN}, measure of V_{SYS} - V_{BATT}		0.45		
BATT to SYS Reverse Regulation Voltage	V_{BSREG}	Measure of V_{SYS} - V_{BATT}; production tested at 10mA and 2A		-100		mV
SYS Self-Discharge Resistor	R_{SYSSD}	Switching is disabled, Q_{BATT} FET is off, V_{SYS} < $V_{SYSUVLO\_F}$		600		Ω
SYSTEM POWER-UP						
System Power-Up Current (from BATT)	I_{SYSPU_BAT}	V_{CHGIN} = 0V	35	50	80	mA
System Power-Up Voltage (from BATT)	V_{SYSPU_BAT}	V_{SYS} rising, 100mV hysteresis	1.9	2.0	2.1	V
System Power-Up Time-Out (from BATT)	t_{SYSPU_BAT}			150		ms
REVERSE BOOST						
Reverse Boost Quiescent Current		V_{BYP} = 5.1V, V_{BATT} = 3.8V, MODE = 0x0A, V_{BYPSET} = 0x1		2.5		mA
Reverse Boost Output Voltage Setting Range	V_{BYP_OTG}	Measured on BYP pin, 2.5V < V_{BATT} < 4.5V; adjustable from 5V to 12V with 0.1V step; production tested at 5V and 12V	5		12	V
Reverse Boost Output Voltage Accuracy	V_{BYP_ACC}	Measured on BYP, MODE = 0x0A, V_{BYPSET} = 0x1	4.95	5.10	5.25	V

Electrical Characteristics (continued)

(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V, unless otherwise specified. Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Boost Inductor Current Limit	I_{LSILIM}	For MAX77976	8.5	9.5	10.5	A
	I_{LSILIM}	For MAX77975	5.95	7.00	8.05	
CHGIN OUTPUT LIMITER						
OTG Output Current Limit Setting Range (MAX77975)	$I_{CHGIN\_OTG\_LIM}$	Configurable from 500mA to 2400mA in 100mA steps. Clamped to 12W power limit	500		2400	mA
OTG Output Current Limit Setting Range (MAX77976)	$I_{CHGIN\_OTG\_LIM}$	Configurable from 500mA to 3100mA in 100mA steps. Clamped to 18W power limit	500		3100	mA
OTG Output Current Limit	$I_{CHGIN\_OTG\_LIM}$	3.4V < V_{BATT} < 4.5V, OTG_ILIM = 0x00	500	537	575	mA
		3.4V < V_{BATT} < 4.5V, OTG_ILIM = 0x04	900	967	1035	
		3.4V < V_{BATT} < 4.5V, OTG_ILIM = 0x0A	1500	1612	1725	
		3.4V < V_{BATT} < 4.5V, OTG_ILIM = 0x19 (MAX77975 only)	2400	2580	2760	
		3.4V < V_{BATT} < 4.5V, OTG_ILIM = 0x19 (MAX77976 only)	3000	3225	3450	
OTG Output Current Limit Alarm Time	t_{OTG_ALARM}	Delay from OTG overcurrent event to BYP_I interrupt generated		20		ms
OTG Output Current Limit Fault Time	t_{OTG_FAULT}	Delay from OTG overcurrent event to Q_{CHGIN} FET opening		30		ms
OTG Output Current Limit Retry Time	t_{OTG_RETRY}	Delay from Q_{CHGIN} FET opening to Q_{CHGIN} FET closing again (OTG_REC_EN = 1)		300		ms
SWITCHE IMPEDANCES AND LEAKAGE CURRENTS						
CHGIN to BYP On Resistance at Room Temp	$R_{CHGIN2BYP\_ROOM}$	CHGIN pin to BYP pin, T_A = +25°C		13.0	16.9	mΩ
CHGIN to BYP On Resistance	$R_{CHGIN2BYP}$	CHGIN pin to BYP pin, T_A = -40°C to +85°C		13.0	20.0	mΩ
LX High-Side On Resistance at Room Temp	R_{HS_ROOM}	BYP pin to LX pin, T_A = +25°C		31.0	43.4	mΩ
LX High-Side On Resistance	R_{HS}	BYP pin to LX pin, T_A = -40°C to +85°C		31.0	54.3	mΩ
LX Low-Side On Resistance at Room Temp	R_{LS_ROOM}	LX pin to PGND pin, T_A = +25°C		16.0	22.4	mΩ
LX Low-Side On Resistance	R_{LS}	LX pin to PGND pin, T_A = -40°C to +85°C		16.0	28.0	mΩ
BATT to SYS On Resistance at Room Temp	$R_{BAT2SYS\_ROOM}$	BATT pin to SYS pin, V_{BATT} = 4.4V, T_A = +25°C		7.70	11.05	mΩ
BATT to SYS On Resistance	$R_{BAT2SYS}$	BATT pin to SYS pin, V_{BATT} = 4.4V, T_A = -40°C to +85°C		7.70	12.75	mΩ

Electrical Characteristics (continued)

(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V, unless otherwise specified. Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LX Leakage Current	I_{LX_LEAK}	V_{LX} = V_{PGND} or V_{BYP}, T_A = +25°C		0.01	10	µA
		V_{LX} = V_{PGND} or V_{BYP}, T_A = +85°C		1		
BST Leakage Current	I_{BST_LEAK}	V_{BST} - V_{LX} = 1.8V, T_A = +25°C		0.01	10	µA
		V_{BST} - V_{LX} = 1.8V, T_A = +85°C		1		
BYP Leakage Current	I_{BYP_LEAK}	V_{BYP} = 5.5V, V_{CHGIN} = 0V, V_{LX} = 0V, charger disabled, T_A = +25°C		0.01	10	µA
		V_{BYP} = 5.5V, V_{CHGIN} = 0V, V_{LX} = 0V, charger disabled, T_A = +85°C		1		
BATSP Input Current Leakage	I_{BATSP}	Charger disabled, V_{BATSP} = V_{BATT}, T_A = +25°C		±1		µA
BATSN Input Current Leakage	I_{BATSN}	Charger disabled, V_{BATSN} = V_{AGND}, T_A = +25°C		±1		µA
LOGIC AND CONTROL I/Os						
Input Low Level	V_{IL}	SUSPND, DISQBAT, T_A = +25°C			0.4	V
		EXTSM, T_A = +25°C			0.3 x V_{BATT}	
Input High Level	V_{IH}	SUSPND, DISQBAT, T_A = +25°C	1.4			V
		EXTSM, T_A = +25°C	0.7 x V_{BATT}			
Input Leakage Current	I_{LK}	SUSPND, DISQBAT, EXTSM pin, at 5.5V (including current through pulldown resistor)		24	60	µA
Output Low Voltage QBEXT	$V_{OLQBEXT}$	Sourcing 1mA, T_A = +25°C			0.4	V
Output High Leakage QBEXT	I_{LQBEXT}	V_{SYS} = 5.5V, T_A = +25°C	-1	0	+1	µA
		V_{SYS} = 5.5V, T_A = +85°C		0.1		
SUSPND Internal Pulldown Resistor	R_{SUSPND}			235		kΩ
DISQBAT Internal Pulldown Resistor	$R_{DISQBAT}$			235		kΩ
EXTSM Internal Pulldown Resistor	R_{EXTSM}			235		kΩ
EXTSM Debounce Time	t_{EXTSM_DEB}	V_{BATT} in 3.3V to 4.5V range, EXTSM_T = 0		10		ms
		V_{BATT} in 3.3V to 4.5V range, EXTSM_T = 1		0.1		
CHARGE STATUS INDICATOR						
Charge Status Current Setting Range	I_{STAT_RNG}	5mA to 20mA in 5mA steps; production tested at V_{STAT} - V_{AGND} = 1.0V and 5.0V	5		20	mA
Charge Status Current Accuracy	I_{STAT_ACC}	Production tested at 5mA and 20mA	-30		+30	%

Electrical Characteristics (continued)

(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V, unless otherwise specified. Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THERMISTOR MONITOR						
THM Threshold, COLD	THM_COLD	V_{THM}/V_{PVDD} rising, 1% hysteresis (thermistor temperature falling)	73.8	75.0	76.2	%
THM Threshold, COOL	THM_COOL	V_{THM}/V_{PVDD} rising, 1% hysteresis (thermistor temperature falling)	64.3	65.5	66.7	%
THM Threshold, WARM	THM_WARM	V_{THM}/V_{PVDD} falling, 1% hysteresis (thermistor temperature rising)	30.8	32.0	33.2	%
THM Threshold, HOT	THM_HOT	V_{THM}/V_{PVDD} falling, 1% hysteresis (thermistor temperature rising)	20.8	22.0	23.2	%
THM Threshold, Disabled	THM_DIS	V_{THM}/V_{PVDD} falling, 1% hysteresis, THM function is disabled below this voltage	4.8	6.0	7.2	%
THM Threshold, Battery Removal Detection	THM_RM	V_{THM}/V_{PVDD} rising, 1% hysteresis, battery removal	85	87	89	%
THM Input Leakage Current	I_{LKTHM}	V_{THM} = V_{AGND} or V_{PVDD}, charger disabled, T_A = +25°C		0.1	1	µA
		V_{THM} = V_{AGND} or V_{PVDD}, charger disabled, T_A = +85°C		0.1		
SUPPLIES AND MONITORING						
VDD Output Voltage	V_{VDD_1P8}	V_{SYS} or V_{BATT} = 3.8V, I_{VDD} = 20mA	1.71	1.80	1.89	V
SYS Undervoltage-Lockout Threshold (SYS Rising)	$V_{SYS\_UVLO\_R}$		2.74	2.80	2.86	V
SYS Undervoltage-Lockout Threshold (SYS Falling)	$V_{SYS\_UVLO\_F}$		2.55	2.60	2.65	V
SYS Undervoltage-Lockout Hysteresis	$V_{SYS\_UVLO\_H}$			200		mV
SYS Overvoltage-Lockout Threshold (SYS Rising)	$V_{SYS\_OVLO\_R}$	SYS rising	5.2	5.35	5.5	V
SYS Overvoltage-Lockout Threshold (SYS Falling)	$V_{SYS\_OVLO\_F}$	SYS falling	5	5.15	5.3	V
SYS Overvoltage-Lockout Hysteresis	$V_{SYS\_OVLO\_H}$			200		mV
Thermal Shutdown Threshold	T_{SHDN_R}	T_j rising		155		°C
Thermal Shutdown Threshold Hysteresis	T_{SHDN_H}			15		°C
PVDD Output Voltage	V_{PVDD_1P8}	V_{SYS} = 3.8V, I_{PVDD} = 20mA	1.71	1.80	1.89	V
I²C-COMPATIBLE INTERFACE TIMING FOR STANDARD, FAST, AND FAST-MODE PLUS						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		0.26			µs
CLK Low Period	t_{LOW}		0.5			µs

Electrical Characteristics (continued)

(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V, unless otherwise specified. Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK High Period	t_{HIGH}		0.26			µs
Set-Up Time Repeated START Condition	$t_{SU;STA}$		0.26			µs
DATA Hold Time	$t_{HD:DAT}$		0			µs
DATA Valid Time	$t_{VD:DAT}$				0.45	µs
DATA Valid Acknowledge Time	$t_{VD:ACK}$				0.45	µs
DATA Set-Up time	$t_{SU;DAT}$		50			ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		0.26			µs
Bus-Free Time Between STOP and START	t_{BUF}		0.5			µs
Pulse Width of Spikes that must be Suppressed by the Input Filter	t_{SP}			50		ns
I²C-COMPATIBLE INTERFACE TIMING FOR HS-MODE (CB = 100pF)						
Clock Frequency	f_{SCL}				3.4	MHz
Set-Up Time Repeated START Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		160			ns
CLK High Period	t_{HIGH}		60			ns
DATA Set-Up time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that must be Suppressed by the Input Filter	t_{SP}			10		ns
I²C-COMPATIBLE INTERFACE TIMING FOR HS-MODE (CB = 400pF)						
Clock Frequency	f_{SCL}				1.7	MHz
Set-Up Time Repeated START Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		320			ns
CLK High Period	t_{HIGH}		120			ns
DATA Set-Up time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns

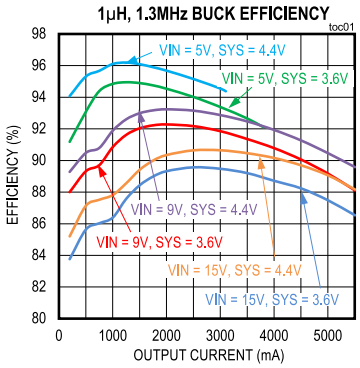
Electrical Characteristics (continued)

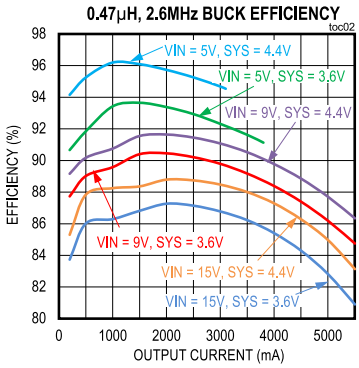
(V_{SYS} = 3.8V, V_{BATT} = 3.8V, V_{VIO} = 1.8V, V_{CHGIN} = 5V, unless otherwise specified. Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

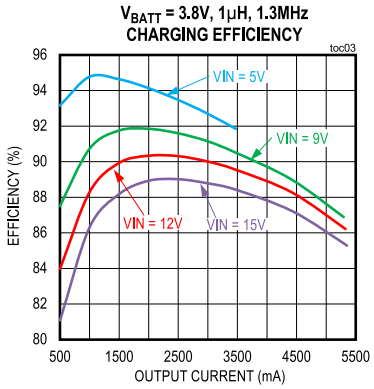
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Set-Up Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that must be Suppressed by the Input Filter	t_{SP}			10		ns

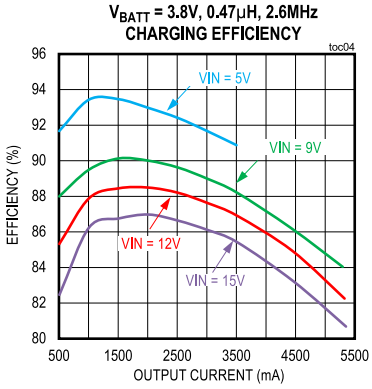
Typical Operating Characteristics

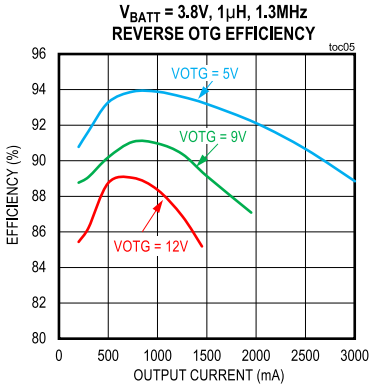
(T_A = +25°C, unless otherwise noted.)

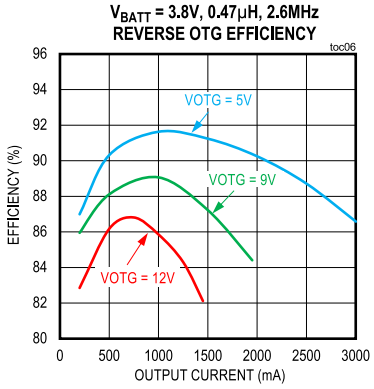






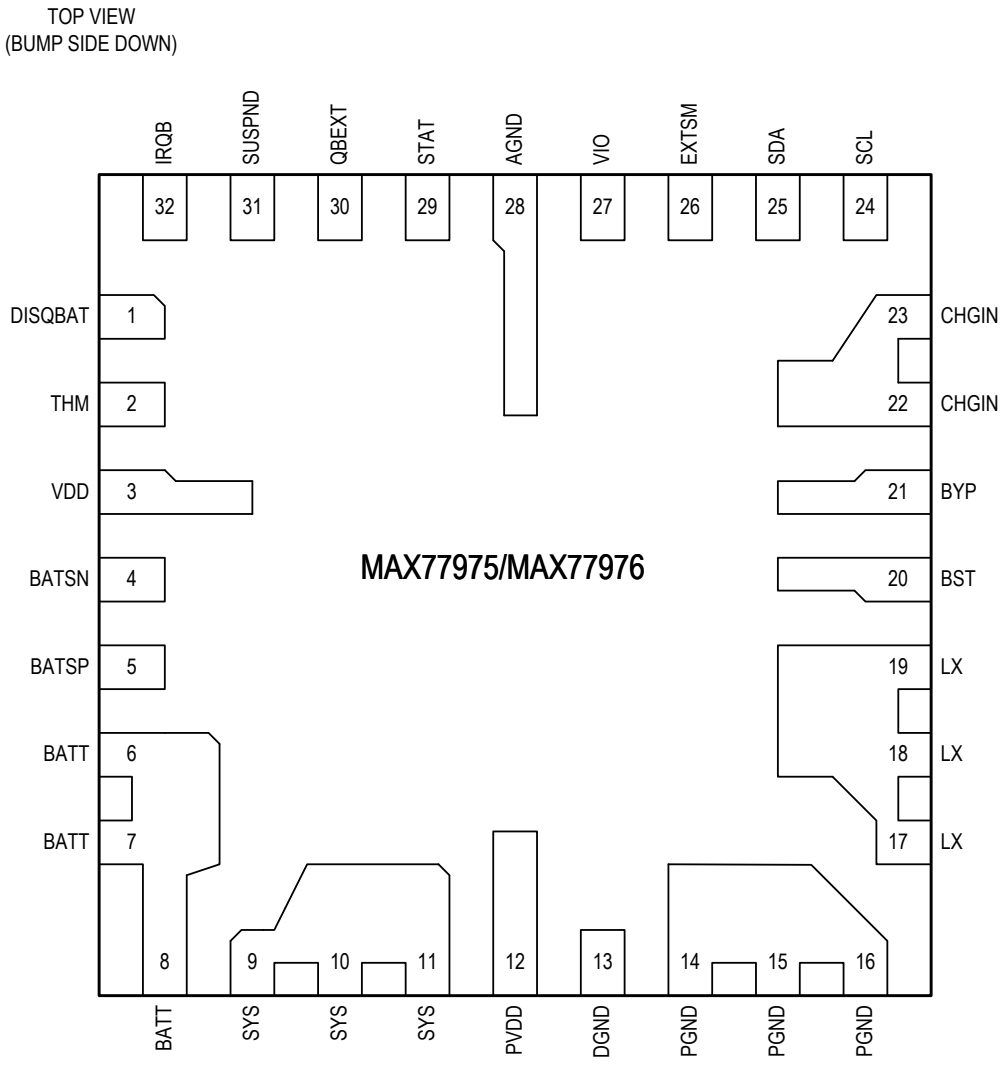






Pin Configuration

FC2QFN



FC2QFN
(4mm x 4mm)

Pin Description

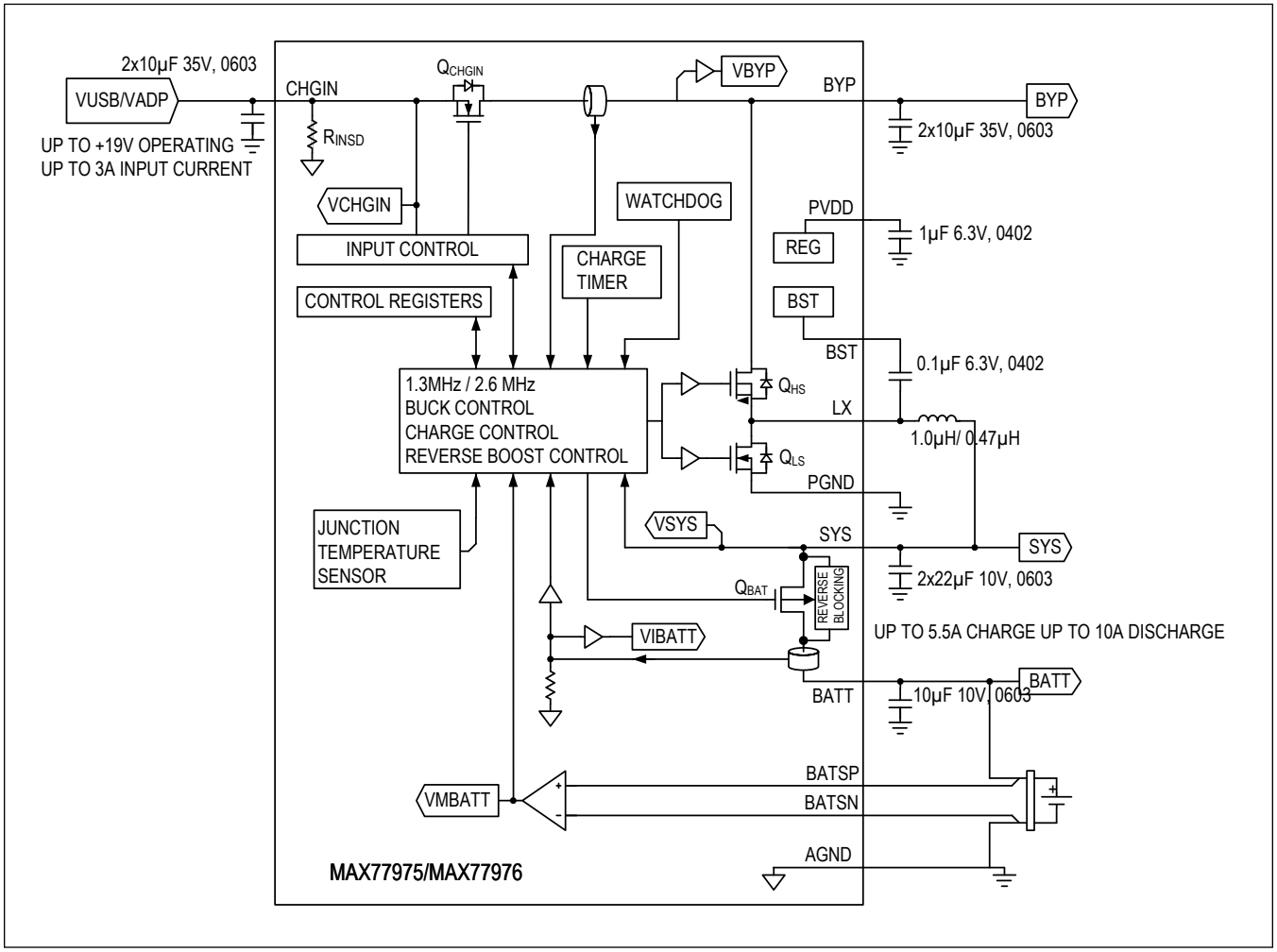
PIN	NAME	FUNCTION	TYPE
1	DISQBAT	Active-high to disable internal Q_{BATT} FET between SYS and BATT.	DI
2	THM	Thermistor Connection. Connect an external thermistor between THM and AGND.	A

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
3	VDD	Analog Voltage Level. The output of on-chip low voltage LDO used to power on-chip, low-noise circuits. Bypass with a 0.1µF (6.3V) ceramic capacitor to AGND. Powering external loads from VDD is not recommended, other than pullup resistors.	A
4	BATSN	Battery Negative Differential Sense Connection. Connect to the negative or ground terminal as close as possible.	A
5	BATSP	Battery Positive Differential Sense Pin. Connect to battery positive terminal as close as possible to eliminate errors due to trace/connector voltage drops.	A
6, 7, 8	BATT	Connection with Battery. Connect to the positive terminal of a single-cell Li-ion battery. Bypass with a 10µF (6.3V) ceramic capacitor from BATT to PGND.	P
9, 10, 11	SYS	Connection with System. Bypass with at least 2x 22µF (6.3V) ceramic capacitors from SYS to PGND. This ensures that the minimum effective capacitance on the SYS node is 12µF (effective), for stability purposes. For application purposes, SYS node capacitance can increase up to 350µF total (effective).	P
12	PVDD	Internal Bias Regulator High Current Output Bypass Pin. Supplies internal noisy and high current gate drive loads. Bypass with 1x 1µF (6.3V) and 1x 100nF (6.3V) from PVDD to PGND. Powering external loads from PVDD is not recommended, other than pullup resistors.	P
13	DGND	Digital Ground	A
14, 15 ,16	PGND	Charger Power Ground	P
17, 18, 19	LX	Charger Switching Node. Connect the inductor between LX and SYS.	P
20	BST	High-Side FET Driver Supply. Bypass BST to LX with a 1x 100nF (6.3V) ceramic capacitor.	A
21	BYP	CHGIN Bypass Pin. This pin is the input for the switching charger and the output for the boost converter when the charger is operating in 'reverse-boost' mode. Bypass with 2x 10µF (35V) ceramic capacitor from BYP to PGND.	P
22, 23	CHGIN	Charger Input. Connect 2x 10µF (35V) between CHGIN and PGND. Connect a Schottky diode with anode at CHGIN and cathode at BYP if required. See the *Design Considerations to Protect Against Hot Plug Event* section.	P
24	SCL	I^2C Interface Clock Input	DI
25	SDA	I^2C Interface Data Input	DI
26	EXTSM	Exit Ship Mode Input by Push-Button. Active-high input.	DI
27	VIO	I^2C Supply Voltage Input. Bypass to AGND with a 0.1µF (6.3V) capacitor.	P
28	AGND	Analog Ground	A
29	STAT	LED Low-Side Driver Output for Indicating Charging Status	A
30	QBEXT	External Battery FET Control Output. Connect a pullup resistor to VIO, SYS, or BATT supply.	DO
31	SUSPND	Active-High Input to Disable the DC-DC Between CHGIN Input and SYS Output	DI
32	IRQB	Interrupt Output. Connect a 100kΩ pullup resistor between IRQB and VIO.	DO

Functional Diagram

Functional Diagram



Detailed Description

Switching Mode Charger

Features

- Complete Li+/LiPoly Battery Charger
  - Prequalification, Constant Current, Constant Voltage
  - 55mA Precharge Current
  - 300mA Trickle Charge Current
  - Adjustable Constant Current Charge
    - 100mA to 5.5A in 50mA steps
  - Adjustable Charge-Termination Threshold
    - 150mA to 850mA in 50mA Steps
  - Adjustable Battery Regulation Voltage
    - 4.15V to 4.46V in 10mV Steps
    - -0.8/+0.2% accuracy from 0°C to +85°C
    - Remote Differential Sensing
- Synchronous Switch-Mode Based Design
- Smart Power Selector
  - Optimally distributes power between the charge adapter, system, and battery.
  - When powered by a charge adapter, the battery can provide supplemental current to the system.
  - The charge adapter can support the system with a dead battery or without a battery.
- No External MOSFETs Required for Switcher
- CHGIN Input
  - Adjustable Input Current Limit
    - 100mA to 3.20A in 50mA steps (CHGIN_ILIM)
    - Default is set to 500mA
  - Supports AC-to-DC Wall Adapters
  - V_{CHGIN_OVLO} = 19V
  - Reverse-Leakage Protection Prevents the Battery Leaking Current to the Inputs
- Charge Safety Watchdog Timer
  - Selectable: 3hr to 10hr, plus a Disable Setting
- Die Temperature Monitor with Thermal Foldback Loop
  - Selectable Die-Temperature Thresholds (°C): +85°C to +130°C in +5°C steps
- Input Voltage Dropout Control Allows Operation from High-Impedance Sources (AICL)
- BATT to SYS Switch is 7.7mΩ Typical
  - Capable of 10A Steady-State Operation from BATT to SYS
- Short-Circuit Protection
  - DISIBS Bit Allows the Host to Disable the Battery to System Discharge Path to Protect Against a Short-Circuit
  - SYS Short to Ground
    - Buck current is limited by switcher current limit and disabling of the synchronous rectifier.

Detailed Description

The MAX77975/MAX77976 includes a full-featured switch-mode charger for a one-cell lithium-ion (Li+) or lithium-polymer (Li-polymer) battery. The current limit for CHGIN input is independently programmable from 100mA to 3.2A in 50mA steps allowing the flexibility for connection to either an AC-to-DC wall charger or a USB port.

The synchronous switch-mode DC-DC converter utilizes a high 1.3MHz/2.6MHz switching frequency which is ideal for portable devices because it allows the use of small components while eliminating excessive heat generation. The DC-DC has both a buck and a boost mode of operation. When charging the main-battery the converter operates as a buck. The DC-DC buck operates from a 4.3V to 19.5V source. The battery charge current is programmable from 100mA to 5.5A.

As a boost converter, the DC-DC uses energy from the main-battery to boost the voltage at BYP. The BYP supplies the USB OTG voltage (5.1V) and USB Type-C® PD Source Voltages (5V to 12V). The programmable boost output current limit range is from 0.5A to 3.1A with a 0.1A step.

Maxim's Smart Power Selector architecture makes the best use of the limited adapter power and the battery's power at all times to supply up to buck current limit from the buck to the system. (Additionally, supplement mode provides additional current from the battery to the system.) Adapter power that is not used for the system goes to charging the battery. All power switches for charging and switching the system load between the battery and adapter power are included on-chip—no external MOSFETs are required.

A multitude of safety features ensures reliable charging. Features include a charge timer, watchdog, junction thermal regulation, over/under voltage protection, and short circuit protection.

Smart Power Selector (SPS)

The SPS architecture is a network of internal switches and control loops that distribute energy between external power sources CHGIN, BYP, SYS, and BATT.

The *Functional Diagram* shows a detailed arrangement of the Smart Power Selector switches and gives them the following names: Q_{CHGIN}, Q_{HS}, Q_{LS}, and Q_{BATT}.

Switch and Control Loop Descriptions

- CHGIN Input Switch: The input switch is either completely on or completely off. As shown in the *Functional Diagram*, there are SPS control loops that monitor the current through the input switches as well as the input voltage.
- DC-DC Switches: Q_{HS} and Q_{LS} are the DC-DC switches that can operate as a buck (step-down) or a boost (step-up). When operating as a buck, energy is moved from BYP to SYS. When operating as a boost, energy is moved from SYS to BYP. SPS control loops monitor the DC-DC switch current, the SYS voltage, and the BYP voltage.
- Battery-to-System Switch: Q_{BATT} controls the battery charging and discharging. Additionally, Q_{BATT} allows the battery to be isolated from the system (SYS). An SPS control loop monitors the Q_{BATT} current.

Control Bits

- MODE configures the Smart Power Selector
- V_{BYPSET} sets the BYP regulation voltage target

Energy Distribution Priority

- With a valid external power source:
  - The external power source is the primary source of energy
  - The main-battery is the secondary source of energy
  - Energy delivery to BYP is the highest priority
  - Energy delivery to SYS is the second priority
  - Any energy that is not required by BYP or SYS is available to the main-battery charger
- With no power source available at CHGIN:
  - The main-battery is the primary source of energy
  - Energy delivery to BYP (if boost mode is selected) and SYS share the same priority
    - BYP includes CHGIN if boost OTG mode is selected, itself limited by OTG_ILIM threshold

BYP Regulation Voltage

- When the DC-DC is off or in one of its buck modes and there is a valid power source at CHGIN, $V_{BYP} = V_{CHGIN} - I_{CHGIN} \times RCHGIN2BYP$.
- When the DC-DC is off and there is no valid power source at CHGIN, BYP is connected to LX through the high-side switch's body diode.

SYS Regulation Voltage

- When the DC-DC is enabled as a buck and the charger is disabled, Q_{BATT} is off and V_{SYS} is regulated to $V_{SYSREG\_TRK\_MIN}$ when the $V_{BATT} < V_{SYSMIN}$ or V_{SYSREG_TRK} when the $V_{BATT} \geq V_{SYSMIN}$.
- When the DC-DC is enabled as a buck and the charger is enabled but in a non-charging state such as done, thermistor suspend, watchdog suspend or timer fault, Q_{BATT} is off and V_{SYS} is regulated to $V_{SYSREG\_TRK\_MIN}$ when the $V_{BATT} < V_{SYSMIN}$ or V_{SYSREG_TRK} when the $V_{BATT} \geq V_{SYSMIN}$.
- When the DC-DC is enabled as a buck and charging in prequalification, fast-charge, or top-off modes, V_{SYS} is regulated to V_{SYSMIN} when the $V_{BATT} < V_{SYSMIN}$; in this mode, the Q_{BATT} switch acts as a linear regulator and dissipates power [$P = (V_{SYSMIN} - V_{BATT}) \times I_{BATT}$]. When $V_{BATT} > V_{SYSMIN}$, then $V_{SYS} = V_{BATT} + I_{BATT} \times R_{BAT2SYS}$; in this mode, the Q_{BATT} switch is closed.
- In all of the above modes, if the combined SYS and BYP loading exceeds the input current limit, then V_{SYS} drops to $V_{BATT} - V_{BSREG}$ and the battery provides supplemental current.
- When the DC-DC is enabled as a boost, then the Q_{BATT} switch is closed, and $V_{SYS} = V_{BATT} - I_{BATT} \times R_{BAT2SYS}$.

Input Validation

The charger input is compared with several voltage thresholds to determine if it is valid. A charger input must meet the following four characteristics to be valid:

- CHGIN must be above V_{CHGIN_UVLO} to be valid. Once CHGIN is above the UVLO threshold, the information (together with IN2SYS, described below) is latched and can only be reset when the charger is in adaptive input current loop (AICL) and input current is lower than the IULO_DET threshold.
- CHGIN must be below its overvoltage-lockout threshold (V_{CHGIN_OVLO}).
- CHGIN must be above the system voltage by IN2SYS drop out.
- CHGIN input generates a CHGIN_I interrupt when its status changes. The input status can be read with CHGIN_OK and CHGIN_DTLS. Interrupts can be masked with CHGIN_M.

Input Current Limit

The default settings of the CHGIN_ILIM and MODE control bits are such that when a charge source is applied to CHGIN, the IC turns its DC-DC converter on in BUCK mode, limits V_{SYS} to V_{SYSREG_TRK}, and limits the charge source current to $I_{INLIMIT}$. All control bits are reset on global shutdown.

Input Voltage Regulation Loop

An input voltage regulation loop allows the charger to be well behaved when it is attached to a poor quality charge source. The loop improves performance with relatively high resistance charge sources that exist when long cables are used or devices are charged with non-compliant USB hub configurations. Additionally, this input voltage regulation loop improves performance with current limited adapters. If the ICs input current limit is programmed above the current-limit threshold of a given adapter, the input voltage loop allows the IC to regulate at the current limit of the adapter. Finally, the input-voltage regulation loop allows the IC to perform well with adapters that have poor transient load response times.

The input voltage regulation loop automatically reduces the inductor average current to keep the input voltage at V_{CHGIN_REG}. If the input current is reduced to I_{ULO_DET} and the input voltage is below V_{CHGIN_REG}, then the charger input is turned off. V_{CHGIN_REG} is programmable with V_{CHGIN_REG}[1:0].

After operating with the input voltage regulation loop active, a AICL_I interrupt is generated, AICL_OK sets to 0. To optimize input power when working with a current limited charge source, monitor the AICL_OK status while decreasing the input current limit. When the input current limit is set below the limit of the adapter, the input voltage rises. Although the input current limit is lowered, more power can be extracted from the input source when the input voltage is allowed to rise.

Example 1. Optimum use of the Input Voltage Regulation Loop along with a current limited adapter.

Sequence of Events:

1. V_{BATT} = 3.2V, the system is operating normally.
2. MODE = 0x04, CHGIN_ILIM = 100mA, CHG_CV_PRM = 4.2V, V_{CHGIN_REG} = 4.5V, CHG_CC_TOT = 2.0A.
3. A 5.0V 1.2A current limited dedicated USB charger is applied to CHGIN.
4. The DC-DC buck regulator turns on, V_{SYS} is regulated to $V_{BATTREG}$ (4.2V) and the input is allowed to provide 100mA to the system.
5. The system detects that the charge source is a dedicated USB charger and enables the battery charger (MODE = 0x05) and programs an input current limit to 1.8A (CHGIN_ILIM = 1.8A).
6. The input current limit starts to ramp up from 100mA to 1.8A, but at the input current limit of the adapter (1.2A), the adapter voltage collapses. The ICs input voltage regulation loop prevents the adapter voltage from falling below 4.5V (V_{CHGIN_REG} = 4.5V). A AICL_I interrupt is generated and AICL_OK sets to 0.
7. With the input-voltage regulation loop active, the adapter provides 1.2A at 4.5V which is a total of 5.4W being delivered to the system.
8. The system software detects that the input voltage regulation loop is active and it begins to ramp down the programmed input current limit. When the current limit ramps down to 1.175A, the adapter is no longer in current limit, and the adapter voltage increases from 4.5V to 5.0V.
9. With the adapter operating just below its current limit, it provides 1.175A at 5.0V which is a total of 5.88W to the system. This is 440mW more than when the adapter was in current limit.

System Self-Discharge with No Power

To ensure a timely, complete, repeatable, and reliable reset behavior when the system has no power, the ICs actively discharge the SYS nodes when Q_{BATT} and switcher are disabled and V_{SYS} is less than $V_{SYSUVLO}$. As shown in Figure 1, the SYS discharge resistor is 600Ω.

Example 1. Basic System Self-Discharge

Initial Conditions: No charger adapter is present at CHGIN, the BAT-to-SYS switch is closed, C_{BAT} = 100µF, C_{SYS} = 200µF, V_{BATT} = 3.6V, and $V_{SYSUVLO}$ falling is SYS_UVLOB_F.

Sequence of Events:

1. With the system in its normal operating mode it is drawing 1A.
2. The main battery is removed.
3. The system continues to draw 1A until V_{SYS} falls below $V_{SYSUVLO}$. This takes 480µs ((3.6V-2.0V)/1A x 300µF).
4. When the system voltage falls below $V_{SYSUVLO}$, the system turns off leakage current. To facilitate discharging C_{BAT} and C_{SYS} the IC engages its 600Ω discharge resistors.

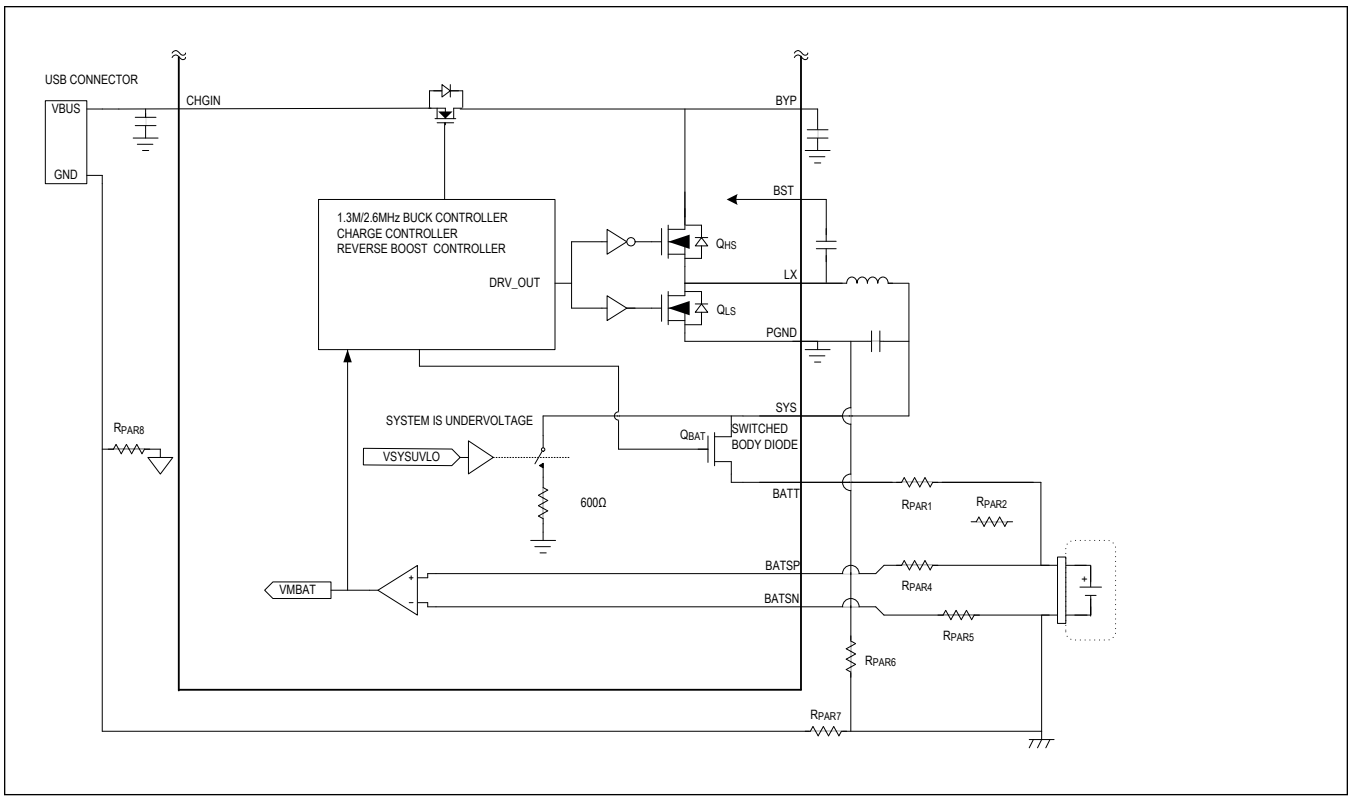


Figure 1. System Self-Discharge Circuit

Power States

The MAX77975/MAX77976 transitions between power states as input/battery and load conditions dictate; see Figure 2.

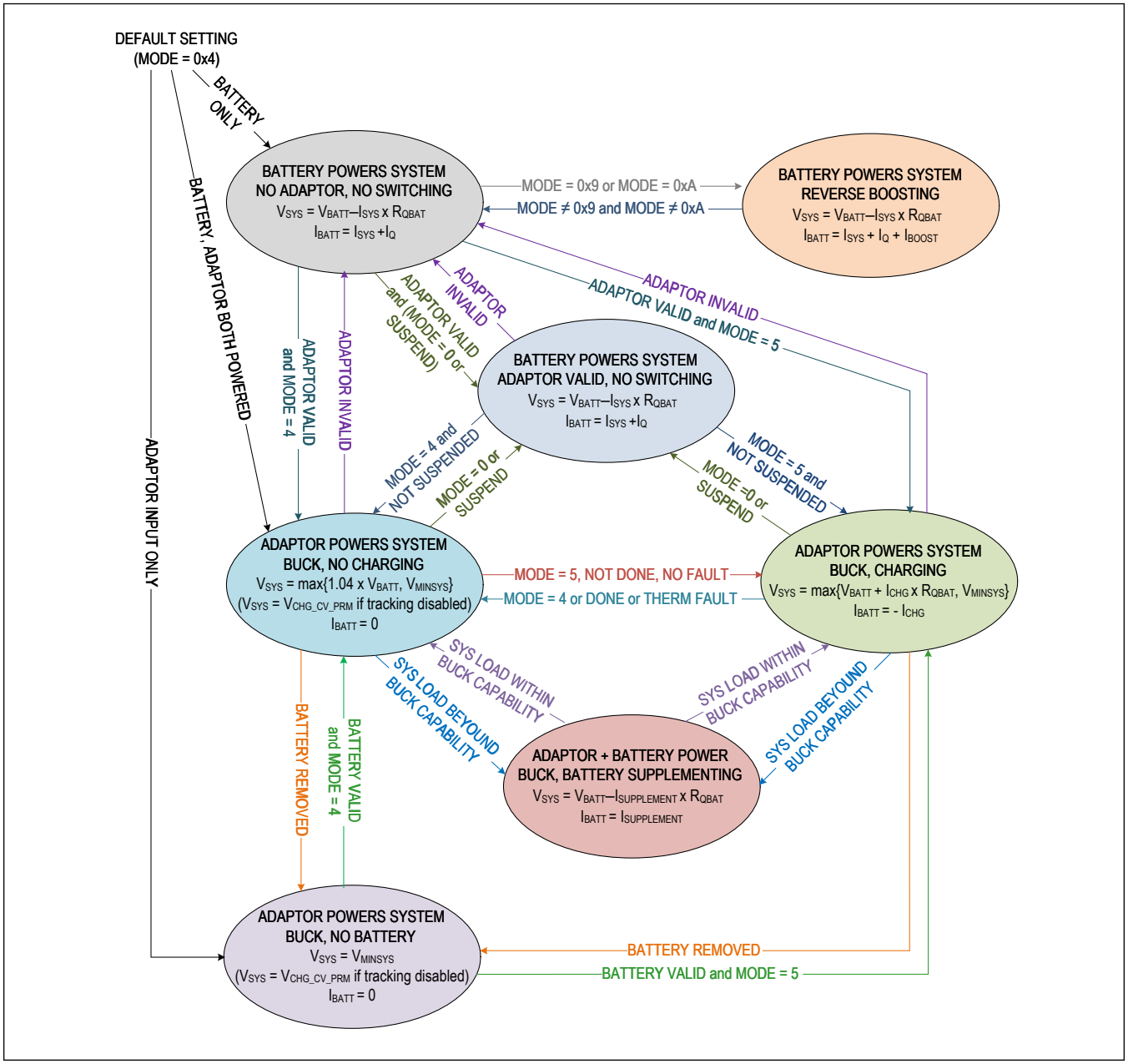


Figure 2. Power State Diagram

The IC provides five (5) power modes and one (1) no power mode (MODE detailed description is at register CHG_CNFG_00 [3:0]). Under power limited conditions, the PowerPath™ feature maintains SYS load at the expense of battery charge current. Also, the battery supplements the input power when required. As shown, transitions between power states are initiated by detection/removal of valid power sources, OTG events, and undervoltage conditions. Details of the SYS voltage and BATT current are provided for each state. There are six main usage modes:

1. NO INPUT POWER, *MODE = undefined*: No input adapter or battery is detected. The charger and system are off. The battery is disconnected and the charger is off.

2. BATTERY-ONLY, *MODE = any modes*: Adapter is invalid and outside the input voltage operating range (Q_{CHGIN} = OFF). The battery is connected to power the SYS load (Q_{BATT} = ON).

3. NO CHARGE-BUCK, *MODE = 0x04*: Adapter is valid, buck supplies power to SYS. The battery is disconnected (Q_{BATT} = OFF) when SYS load is less than the power that buck can supply.

When SYS load is larger than the power that buck can supply, the battery is reconnected (Q_{BATT} = ON) and supplements extra SYS load.

4. CHARGE-BUCK, *MODE = 0x05*: Adapter is valid, buck supplies power to SYS, and charges battery with I_{BATT}.

5. BATTERY-BOOST (FLASH), *MODE = 0x09*: OTG is inactive (Q_{CHGIN} = OFF). Battery is connected to support SYS and BYP loads (Q_{BATT} = ON), and charger is operating in boost mode (Boost = ON).

6. BATTERY-BOOST (OTG), *MODE = 0x0A*: OTG is active (Q_{CHGIN} = ON). Battery is connected to support SYS and OTG loads (Q_{BATT} = ON), and charger is operating in boost mode (Boost = ON).

Charger States

The ICs utilize several charging states to safely and quickly charge batteries as shown in Figure 3. The figure shows an exaggerated view of a Li+/Li-Poly battery progressing through the following charge states when there is no system load and the die and battery are close to room temperature. It shows a complete charging state transition process with four states: prequalification, fast-charge, top-off, and done.

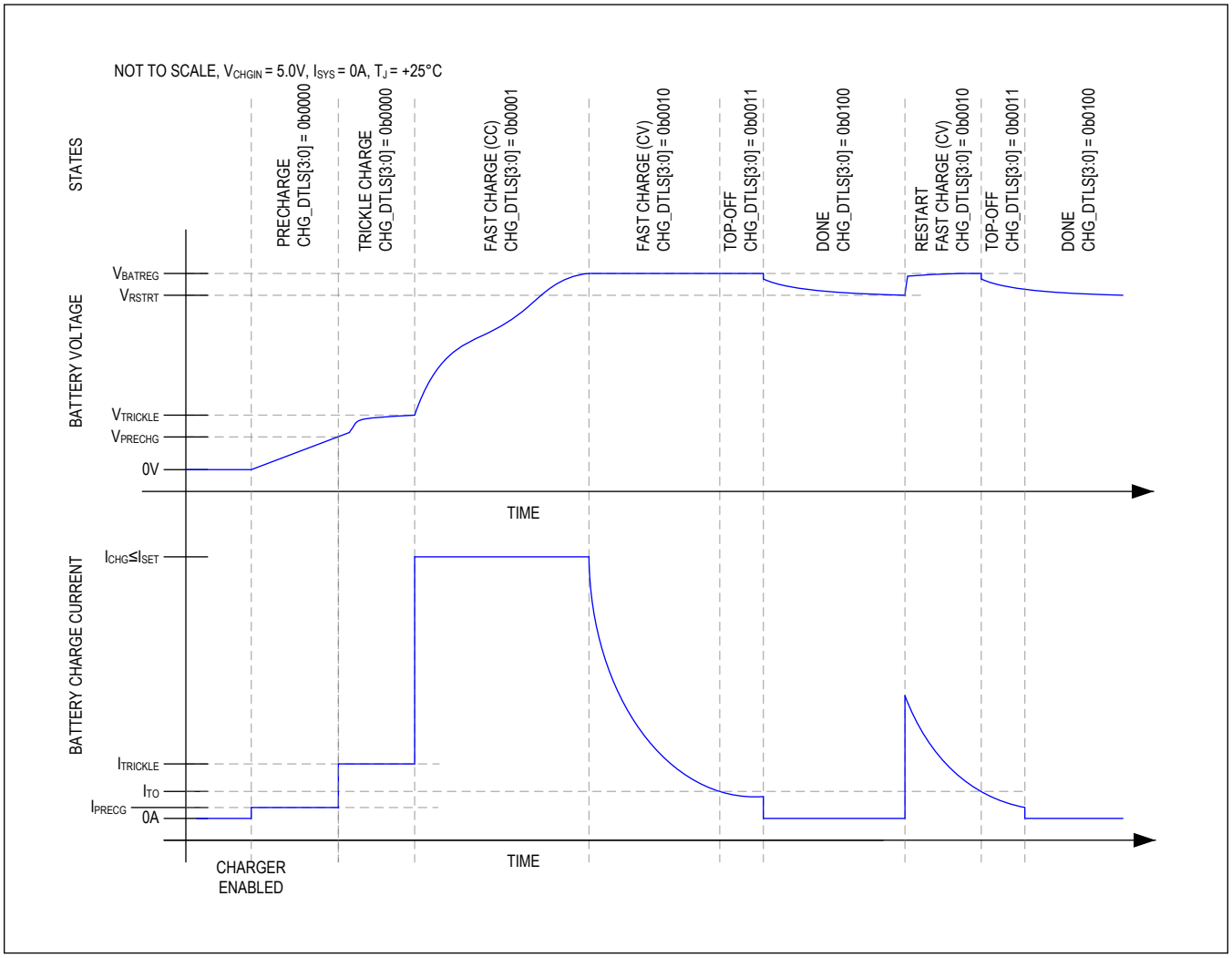


Figure 3. Li+/Li-Poly Charge Profile

No Input Power or Charge Idle State

While in the “no input power or charger idle” state, the charge current is 0mA, the watchdog and charge timers are forced to 0, and the power to the system is provided by either the battery or the adapter. When both battery and adapter power is available, the adapter provides primary power to the system and the battery contributes supplemental energy to the system if necessary.

To exit the “no input power or charger idle” state, the charger input must be valid and the charger has to be enabled.

Precharge State

As shown in Figure 3, the precharge state occurs when the main-battery voltage is less than V_{PRECHG}. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated only if CHG_OK was 0 previously, CHG_OK is set to 1, and CHG_DTLS is set to 0x00. In the precharge state, charge current into the battery is I_{PRECHG}.

The following events cause the state machine to exit this state:

- Main battery voltage rises above V_{PRECHG} and the charger enters the next state in the charging cycle: “Trickle Charge”.
- If the battery charger remains in this state for longer than t_{PQ}, the charger state machine transitions to the “Timer Fault” state.
- If the watchdog timer is not serviced (see the *Watchdog Timer* section), the charger state machine transitions to the “Watchdog Suspend” state.

Note that the precharge state works with battery voltages down to 0V. The low 0V operation typically allows this battery charger to recover batteries that have an “open” internal pack protector. Typically a pack internal protection circuit opens if the battery has seen an overcurrent, undervoltage, or overvoltage. When a battery with an “open” internal pack protector is used with this charger, the precharge mode current flows into the 0V battery—this current raises the pack’s terminal voltage to the pointer where the internal pack protection switch closes.

Note that a normal battery typically stays in the precharge state for several minutes or less. Therefore a battery that stays in the precharge for longer than t_{PQ} may be experiencing a problem.

Trickle Charge State

As shown in Figure 3, the trickle charge state occurs when $V_{BATT} > V_{PRECHG}$ and $V_{BATT} < V_{TRICKLE}$. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated only if CHG_OK was 0 previously, CHG_OK is set to 1, and CHG_DTLS = 0x00.

With TKEN = 1 and the IC is in its trickle charge state, the current in the battery is less than or equal to ITRICKLE. When TKEN = 0, the battery current is less than or equal to I_{FC}.

Charge current may be less than ITRICKLE/I_{FC} for any of the following reasons:

- The charger input is in input current limit
- The charger input voltage is low
- The charger is in thermal foldback
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

Typical systems operate with TKEN = 1. When operating with TKEN = 0, the system’s software usually sets I_{FC} to a low value such as 450mA and then monitors the battery voltage. When the battery exceeds a relatively low voltage such as 3.1V, then the system’s software usually increases I_{FC}.

The following events cause the state machine to exit this state:

- When the main battery voltage rises above VTRICKLE or the PQEN bit is cleared, the charger enters the next state in the charging cycle: “Fast Charge (CC)”.
- If the battery charger remains in this state for longer than t_{PQ}, the charger state machine transitions to the “Timer Fault” state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

Note that a normal battery typically stays in the trickle charge state for several minutes or less. Therefore a battery that stays in trickle charge for longer than t_{PQ} may be experiencing a problem.

Fast-Charge Constant Current (CC) State

As shown in Figure 3, the fast-charge CC state occurs when the main-battery voltage is greater than the low-battery prequalification threshold and less than the battery regulation threshold ($V_{TRICKLE} < V_{BATT} < V_{BATTREG}$). After being in the fast-charge CC state for t_{SCIDG}, a CHG_I interrupt is generated only if CHG_OK was 0 previously, CHG_OK is set to 1, and CHG_DTLS = 0x01.

In the fast-charge CC state, the current into the battery is less than or equal to I_{FC}. Charge current may be less than I_{FC} for any of the following reasons:

- The charger input is in input current limit
- The charger input voltage is low
- The charger is in thermal foldback
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events causes the state machine to exit this state:

- When the main battery voltage rises above $V_{BATTREG}$, the charger enters the next state in the charging cycle: “Fast Charge (CV)”.
- If the battery charger remains in this state for longer than t_{FC}, the charger state machine transitions to the “Timer Fault” state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

The battery charger dissipates the most power in the fast-charge constant current state. This power dissipation causes the internal die temperature to rise. If the die temperature exceeds T_{REG}, I_{FC} is reduced. See the *Thermal Foldback* section for more information.

Fast-Charge Constant Voltage (CV) State

As shown in Figure 3, the fast-charge CV state occurs when the battery voltage rises to $V_{BATTREG}$ from the fast-charge CC state. After being in the fast-charge CV state for t_{SCIDG}, a CHG_I interrupt is generated only if CHG_OK was 0 previously, CHG_OK is set to 1, and CHG_DTLS = 0x02.

In the fast-charge CV state, the battery charger maintains $V_{BATTREG}$ across the battery and the charge current is less than or equal to I_{FC}. As shown in Figure 3, charger current decreases exponentially in this state as the battery becomes fully charged.

The smart power selector control circuitry may reduce the charge current lower than the battery may otherwise consume for any of the following reasons:

- The charger input is in input current limit
- The charger input voltage is low
- The charger is in thermal foldback
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events causes the state machine to exit this state:

- When the charger current is below I_{TO} for t_{TERM}, the charger enters the next state in the charging cycle: “TOP OFF” state.
- If the battery charger remains in this state for longer than t_{FC}, the charger state machine transitions to the “Timer Fault” state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

Top-Off State

As shown in Figure 3, the top-off state can only be entered from the fast-charge CV state when the charger current decreases below I_{TO} for t_{TERM}. After being in the top-off state for t_{SCIDG}, a CHG_I interrupt is generated only if CHG_OK was 0 previously, CHG_OK is set to 1, and CHG_DTLS = 0x03. In the top-off state, the battery charger tries to maintain $V_{BATTREG}$ across the battery and typically the charge current is less than or equal to I_{TO}.

The smart power selector control circuitry may reduce the charge current lower than the battery may otherwise consume

for any of the following reasons:

- The charger input is in input current limit
- The charger input voltage is low
- The charger is in thermal foldback
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- After being in this state for the top-off time (t_{TO}), the charger enters the next state in the charging cycle: “DONE” state.
- If $V_{BATT} < V_{BATTREG} – V_{RSTRT}$, the charger goes back to the “FAST CHARGE (CC)” state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

Done State

As shown in Figure 3, the battery charger enters its done state after the charger has been in the top-off state for t_{TO}. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated only if CHG_OK was 0 previously, CHG_OK is set to 0, and CHG_DTLS = 0x04.

The following events cause the state machine to exit this state:

- If $V_{BATT} < V_{BATTREG} – V_{RSTRT}$, the charger goes back to the “FAST-CHARGE CC” state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

In the done state, the charge current into the battery (I_{CHG}) is 0A. In the done state, the charger presents a very low load (I_{MBDN}) to the battery. If the system load presented to the battery is low, then a typical system can remain in the done state for many days. If left in the done state long enough, the battery voltage decays below the restart threshold (V_{RSTRT}), and the charger state machine transitions back into the fast-charge CV state. There is no soft-start (di/dt limiting) during the done to fast-charge state transition.

Timer Fault State

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging. The charge timer prevents the battery from charging indefinitely. The time that the charger is allowed to remain in each of its prequalification states is t_{PQ}. The time that the charger is allowed to remain in the fast-charge CC & CV states is t_{FC} which is programmable with FCHGTIME. Finally, the time that the charger is in the top-off state is t_{TO} which is programmable with TO_TIME. Upon entering the timer fault state a CHG_I interrupt is generated without a delay, CHG_OK is cleared, and CHG_DTLS = 0x06.

In the timer fault state, the charger is off. The charger can exit the timer fault state by programming the charger to be off and then programming it to be on again through the MODE bits. Alternatively, the charger input can be removed and re-inserted to exit the timer fault state.

Watchdog Timer

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging. The watchdog timer protects the battery from charging indefinitely if the host hangs or otherwise cannot communicate correctly. The watchdog timer is disabled by default with WDTEN = 0. To use the watchdog timer feature enable the feature by setting WDTEN. While enabled, the system controller must reset the watchdog timer within the timer period (t_{WD}) for the charger to operate normally. Reset the watchdog timer by programming WDTCLR = 0x01.

If WD_QBATTOFF bit is set to 0 and the watchdog timer expires while the charger is in dead-battery prequalification, low-battery prequalification, fast-charge CC or CV, top-off, done, or timer fault, the charging stops, a CHG_I interrupt is generated only if CHG_OK was 1 previously, CHG_OK is cleared, and CHG_DTLS indicates that the charger is off because the watchdog timer expired. Once the watchdog timer has expired, the charger may be restarted by programming WDTCLR = 0x01. The SYS node can be supported by the battery and/or the adapter through the DC-DC buck while the watchdog timer is expired.

If WD_QBATTOFF bit is set to 1 and the watchdog timer expires, MAX77976 turns off the buck, charger, and Q_{BATT} switch for 150ms. And then V_{SYS} voltage collapses and it resets all I^2C registers. The IC restarts as initial power-up condition.

Thermal Shutdown State

The thermal shutdown state occurs when the battery charger is in any state and the junction temperature (T_J) exceeds the device's thermal-shutdown threshold (T_{SHDN}). When T_J is close to T_{SHDN} the charger folds back the charge current to 0A (see the *Thermal Foldback* section). Upon entering this state, CHG_I interrupt is generated if CHG_OK was 1 previously, CHG_OK is cleared, and CHG_DTLS = 0x0A.

In the thermal shutdown state, the charger is off. MODE register (CHG_CNFG_00[3:0]) is reset to its default value as well as all O type registers.

Charger Interrupt Debounce Time

Table 1. Charger Interrupt Debounce Time

	DEBOUNCE TIME RISING	DEBOUNCE TIME FALLING
INTERRUPT	**Typ (ms)**	**Typ (ms)**
AICL_I	30	30
CHGIN_I	7.5	—
INLIM_I	30	30
BAT_I (Overvoltage T_{BATOV})	7.5	—
BYP_I (T_{OTG_I})	20	—
BYP_I (BST_I_{LIM})	30	—
BYP_I (Buck Neg I_{LIM})	0.5	—

Accuracy of the timer is defined by T_{ACC}.

Battery Differential Voltage Sense

BATSP and BATSN are differential remote sense lines for the main-battery. To improve accuracy and decrease charging times, the battery charger voltage sense is based on the differential voltage between BATSP and BATSN. Similarly, the thermistor voltage is interpreted with respect to BATSN.

A Maxim battery charger without the remote sensing function would typically measure the battery voltage between BATT and GND. In case a charge current of 1A measuring from BATT to GND leads to a V_{BATT} that is 40mV higher than the real voltage because of R_{PAR1} and R_{PAR7} (I_{CHG} x (R_{PAR1} + R_{PAR7}) = 1A x 40mΩ = 40mV). Since the charger thinks the battery voltage is higher than it actually is, it enters its fast-charge CV state sooner and the effective charge time may be extended by 10 minutes (based on real lab measurements). This charger with differential remote sensing does not experience this type of problem because BATSP and BATSN sense the battery voltage directly. To get the maximum benefit from these sense lines, connect them as close as possible to the main-battery connector.

Reverse Boost Mode

The DC-DC converter topology of the IC allows it to operate as a forward buck converter or as a reverse boost converter. The modes of the DC-DC converter are controlled with MODE. When MODE = 0x09 or 0x0A, the DC-DC converter operates in reverse boost mode allowing it to source current to BYP. To allow current flow to CHGIN, set MODE = 0x0A. This mode allows current to be sourced from CHGIN and is commonly referred to as OTG mode.

When MODE = 0x0A, the DC-DC converter operates in reverse boost mode and regulates V_{BYP} to $V_{BYP.OTG}$ and the low ohmic ($R_{CHGIN2BYP}$) switch from BYP to CHGIN is closed. The current through the BYP to CHGIN switch is limited to the value programmed by OTG_ILIM. The programmable OTG_ILIM options allow for supplying from 500mA to 3100mA to an external load. When the OTG mode is selected, the unipolar CHGIN transfer function measures the current going out of CHGIN. When OTG mode is not selected, the unipolar CHGIN transfer function measures current going into CHGIN.

If the external OTG load at CHGIN exceeds ICHGIN.OTG.ILIM current during a minimum time of T_{OTG_I} ms, then a BYP_I interrupt is generated. BYP_OK = 0 and BYP_DTLS[0] = 1. In response to an overload at CHGIN during OTG mode operation, the BYP to CHGIN switch is latched off T_{OTG_fault} after entering OTG_ILIM condition. If the overload at CHGIN persists, BYP_DTLS keeps continuing to report OTG_ILIM fault through BYP_DTLS[0] = 1.

If OTG_REC_EN bit = '1: other functions remain unaffected, i.e., BYP is supplied by reverse boost and the BYP to CHGIN

switch automatically retries after T_{OTG_retry}. If the overload at CHGIN persists, then the CHGIN switch toggles ON and OFF with T_{OTG_fault} ON time and T_{OTG_retry} OFF time.

If OTG_REC_EN bit = '0: the BYP to CHGIN switch remains off and the switcher is turned off until MODE is toggled.

BYP_I exit interrupt is only generated on OTG load release such as IOTG < ICHGIN.OTG.ILIM or FET opening. At that time, BYP_I interrupt is generated. BYP_OK = 1 and BYP_DTLS[0] = 0.

Note: On OTG_ILIM debounce time out, BYP_DTLS[0] is latched until the BYP_DTLS register is read by AP. BYP_OK is matching BYP_DTLS[0] behavior.

Battery Overcurrent Protection

The IC is rated for a maximum discharge current of 10A. To protect against excessive battery discharge current, the IC must only be used with a battery pack with overcurrent protection circuit rated for 10A or less.

Battery to SYS Q_{BATT} Switch Control (DISIBS)

To protect the system from unexpected and critical events (e.g., excessive battery discharge current), the AP can control the MAX77975/MAX77976 Q_{BATT} switch by driving DISIBS bit to a logic-high.

There are different scenarios of how the IC responds to setting the DISIBS bit high depending on the available power source and the state of the charger:

1) The IC is only powered from BATT and DISIBS bit is set
    a. Q_{BATT} switch opens
    b. SYS collapses and is allowed to go to 0V
    c. If RECYCLE_EN = 1, the IC self-recovers and restarts after t_{OCP_RETRY}. If RECYCLE_EN = 0, after t_{OCP_RETRY}, the IC does not recycle until a valid charger input is inserted.
2) The IC is powered from BATT, CHGIN is present, the charger buck is not switching, and DISIBS bit is set:
    a. Q_{BATT} switch opens
    b. SYS collapses and is allowed to go to 0V
    a. Regardless of RECYCLE bit setting, the IC self-recovers and restarts after t_{OCP_RETRY}.
3) The IC is powered from CHGIN, buck is switching, charge is OFF, and DISIBS bit is set:
    a. Q_{BATT} stays OFF (opened)
    b. Turn off Buck
    c. SYS collapses and is allowed to go to 0V
    d. Regardless of RECYCLE bit setting, the IC self-recovers and restarts after t_{OCP_RETRY}.
4) The IC is powered from CHGIN, buck is switching, charge is ON, and DISIBS bit is set:
    a. Charge is disabled
    b. Q_{BATT} turns off (opened)
    c. Turn off Buck
    d. SYS collapses and is allowed to go to 0V
    e. Regardless of RECYCLE bit setting, the IC self-recovers and restarts after t_{OCP_RETRY}.

HW Control of Battery to SYS Q_{BATT} Switch—DISQBAT

To protect the system from unexpected and critical events (e.g., excessive battery discharge current), the AP can control the ICs Q_{BATT} switch by driving the DISQBAT hardware pin. This pin can also be driven during factory test modes.

On DISQBAT low-to-high assertion, Q_{BATT} FET opens and any ongoing charge is disabled but buck keeps switching (if allowed by MODE setting).

The IC supports factory-boost mode to enter in boost mode (through CHG_CNFG_00.MODE setting) and keep Q_{BATT} OFF even if boost mode is set.

This functionality is only enabled once functional register CHG_CNFG_07.FMBST bit is set 1.

DISQBAT is an input control signal for Q_{BATT} FET with an external logic signal. If DISQBAT is driven by high, Q_{BATT} FET is truly disconnected. It has an internal 470kΩ pulldown resistor.

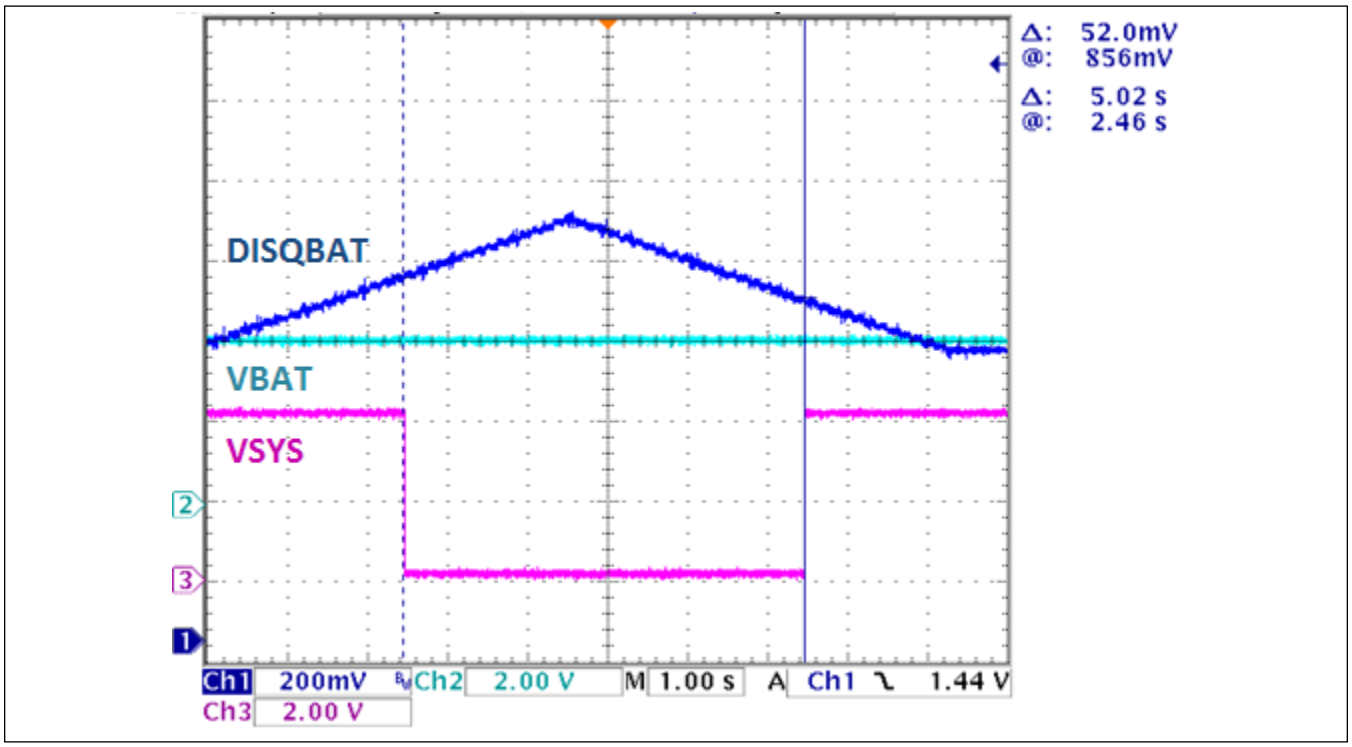


Figure 4. Hardware Control of Battery to SYS Switch

Thermal Management

The ICs charger uses several thermal management techniques to prevent excessive battery and die temperatures.

Thermal Foldback

Thermal foldback maximizes the battery charge current while regulating the ICs junction temperature. As shown in Figure 5, when the die temperature exceeds the value programmed by REGTEMP (T_{REG}), a thermal limiting circuit reduces the battery charger's target current by A_{TJREG}. The target charge current reduction is achieved with an analog control loop (i.e., not a digital reduction in the input current). When the thermal foldback loop changes state, a CHG_I interrupt is generated and the system's microprocessor may read the status of the thermal regulation loop through the T_{REG} status bit. Note that the thermal foldback loop being active is not considered to be abnormal operation and the thermal foldback loop status does not affect the CHG_OK bit (only information contained within CHG_DTLS affects CHG_OK).

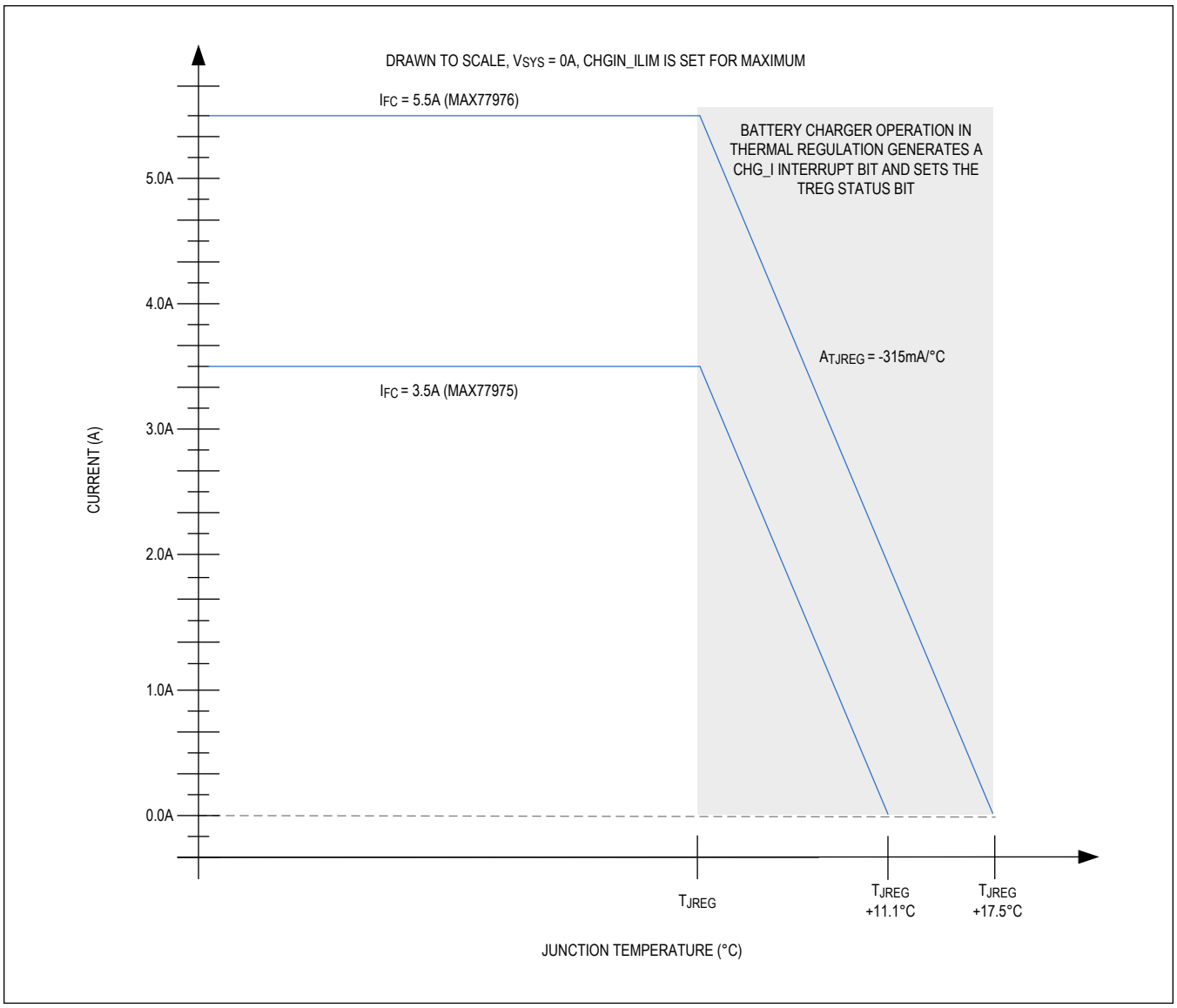


Figure 5. Charge Currents vs. Junction Temperature

Thermistor Input (THM)

The thermistor input can be utilized to achieve functions such as, charge suspension, JEITA compliant charging, and battery removal detection. The thermistor monitoring feature can be disabled by connecting the THM pin to ground.

The THM input connects to an external negative temperature coefficient (NTC) thermistor to monitor battery or system temperature.

JEITA Compliant Charging

JEITA compliant charging is available with JEITA_EN = 1.

Charging stops when the thermistor temperature is out of range ($T < T_{COLD}$ or $T > T_{HOT}$). The charge timers are reset and the CHG_DTLS[3:0], CHG_OK register bits report the charging suspension status, and CHG_I interrupt bit is set. When the thermistor comes back into range ($T_{COLD} < T < T_{HOT}$), charging resumes, and the charge timer restarts.

See the *JEITA Controlled Charging* section for more details.

Battery Removal Detection

With pullup connected between PVDD and THM, if battery is removed, the thermistor is disconnected from THM; this event is detected as THM is pulled up to PVDD. Battery removal event prevents charging.

Disable Thermistor Monitoring

Connecting THM to GND disables the thermistor monitoring function, and JEITA controlled charging is unavailable in this configuration. The IC detects an always-connected battery when THM is grounded, and charging starts automatically when a valid adapter is plugged in. In applications with removable batteries, do not connect THM to GND because the IC is not able to detect battery removal when THM is grounded. Instead, connecting THM to the thermistor pin in the battery pack is recommended.

Since the thermistor monitoring circuit employs an external bias resistor from THM to PVDD, the thermistor is not limited only to 10kΩ (at +25ºC). Any resistance thermistor can be used as long as the value is equivalent to the thermistors +25ºC resistance. For example, with a 10kΩ at RTB resistor, the charger enters a temperature suspend state when the thermistor resistance falls below 4.67kΩ (too hot) or rises above 30.3kΩ (too cold). This corresponds to 0ºC to +45ºC range when using a 10kΩ NTC thermistor with a beta of 3610. The general relation of thermistor resistance to temperature is defined by the following equation:

$$R_T = R_{25} \times e^{\left\{\beta\left\{\frac{1}{T+273^{\circ}C} - \frac{1}{298^{\circ}C}\right\}\right\}}$$

where:

R_T = The resistance in Ω of the thermistor at temperature T in Celsius

R_{25}= The resistance in Ω of the thermistor at +25ºC

β = The material constant of the thermistor, which typically ranges from 3000k to 5000k

T = The temperature of the thermistor in °C

Some designs might prefer other thermistor temperature limits. Threshold adjustment can be accommodated by changing R_{TB}, connecting a resistor in series and/or in parallel with the thermistor, or using a thermistor with different β. For example, a +45ºC hot threshold and 0°C cold threshold can be realized by using a thermistor with a β to 4250 and connecting 120kΩ in parallel. Since the thermistor resistance near 0ºC is much higher than it is near +50ºC, a large parallel resistance lowers the cold threshold while only slightly lowering the hot threshold. Conversely, a small series resistance raises the cold threshold, while only slightly raising the hot threshold. Raising R_{TB}, lowers both the hot and cold threshold, while lowering R_{TB} raises both thresholds.

Thermistor bias current flows whenever PVDD is enabled (CHGIN valid or BOOST enabled). When using a 10kΩ thermistor and a 10kΩ pullup to THM, this results in an additional 90µA load. This load can be reduced to 9µA by instead using a 100kΩ thermistor and 100kΩ pullup resistor.

Table 2. Trip Temperatures for Different Thermistors

Thermistor	R25 (Ω)	10000	10000	47000	100000
	Thermistor Beta (β)	3380	3610	4050	4250
	RTB (Ω)	10000	10000	47000	100000
	R15 (Ω)	14826	15223	75342	164083
	R45 (Ω)	4900	4671	19993	40781
Trip Temperatures	T_{COLD} (˚C)	-1.3	0.2	2.7	3.7
	T_{COOL} (˚C)	9.0	10.0	11.6	12.2
	T_{WARM} (˚C)	46.2	44.8	42.5	41.7
	T_{HOT} (˚C)	62.5	59.8	55.6	54.1

JEITA Controlled Charging

The MAX77976 safely charges Li+ batteries in accordance with JEITA specifications. The IC monitors the battery temperature with an NTC thermistor connected at THM pin and automatically adjusts the fast-charge current and/or charge termination voltage as the battery temperature varies. JEITA controlled charging can be disabled by setting JEITA_EN to '0; if JEITA_EN = '0, thermistor input is not taken into account to determine charge state or charge current and voltage levels.

CHG_DTLS and THM_DTLS registers report JEITA controlled charging status.

The JEITA controlled fast-charging current (I_{CHGCC_JEITA}) for $T_{WARM} < T < T_{HOT}$ is programmable with I^2C bit CHG_CC_WARM.

The JEITA controlled charge termination voltage (V_{CHGCV_JEITA}) for $T_{COLD} < T < T_{COOL}$ is programmable with I^2C bit CHG_CV_COOL.

The JEITA controlled fast-charging current for $T_{COLD} < T < T_{COOL}$ is halved (to CHG_CC x 0.5) and the charge termination voltage for $T_{WARM} < T < T_{HOT}$ is reduced to (CHG_CV_PRM - 150mV), as shown in the Figure 6.

The JEITA controlled charging is suspended when the battery temperature is too cold or too hot ($T < T_{COLD}$ or $T_{HOT} < T$).

Temperature thresholds T_{COLD}, T_{COOL}, T_{WARM}, T_{HOT} depend on the thermistor selection. See the *Thermistor Input (THM)* section for more details.

When JEITA controlled battery charge current is reduced by 50%, the charger timer is doubled.

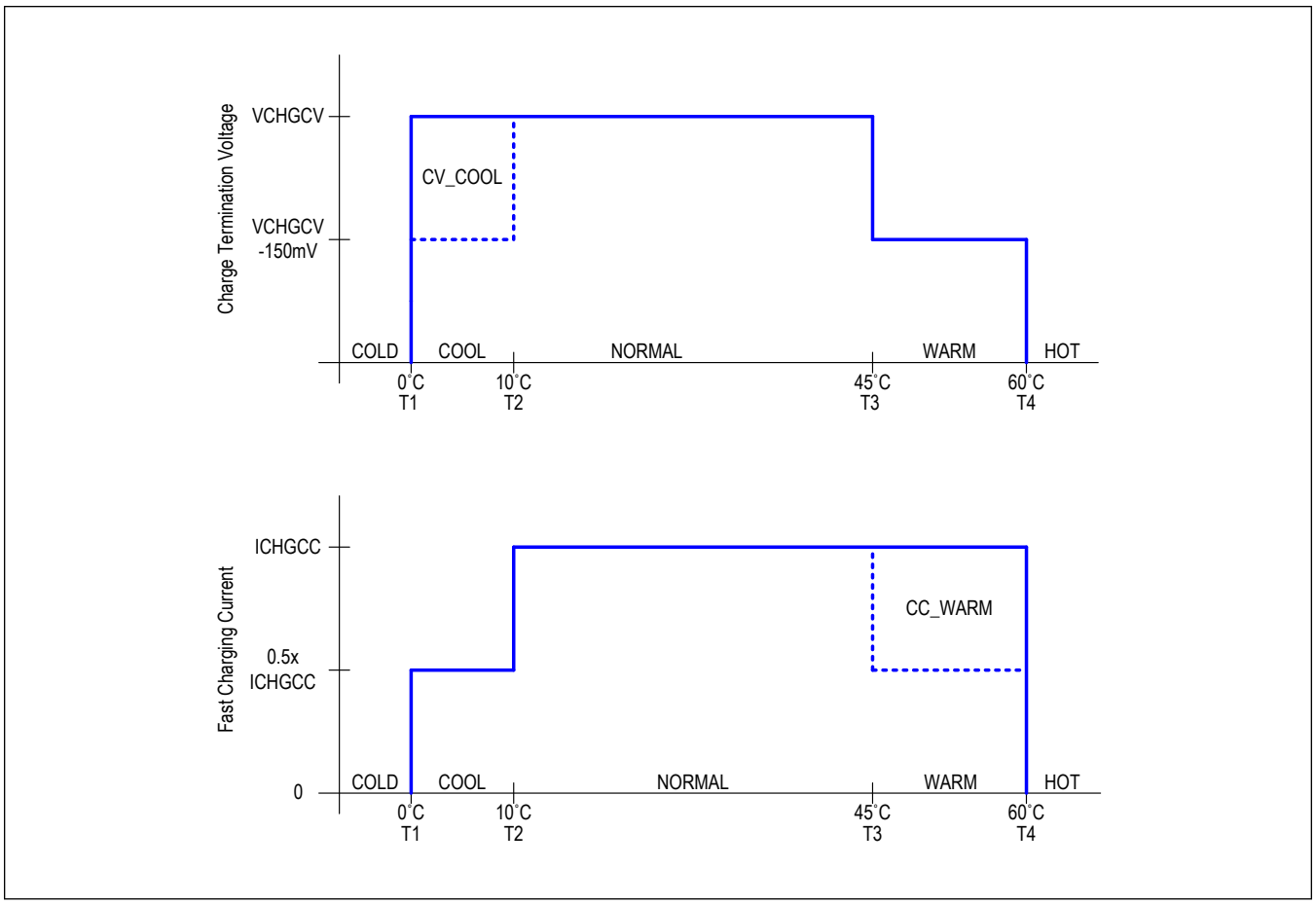


Figure 6. JEITA Controlled Charging

Analog Low-Noise Power PVDD and VDD

VDD is the 1.8V LDO output for the charger's analog circuitry. VDD takes its power from the higher voltage of CHGIN, BATT, and SYS. VDD has a bypass capacitance of 1µF.

PVDD is the 1.8V LDO output for internal power circuitry. PVDD has a bypass capacitance of 1µF.

Factory-Ship Mode

The ICs support factory-ship mode.

Charger's CHG_CNFG_07 bit 0: FSHIP_MODE bit controls this mode.

When this bit is set to 1, the IC goes into factory-ship mode.

This mode can be exited by battery removal or on a valid charger input plug or by pulling EXTSM high longer than t_{EXTSM_DEB} (programmable with EXTSM_T bit).

Factory-ship mode can not be entered when a valid charger is present.

This feature minimizes battery leakage current when factory ships battery connected devices.

External Q_{BATT} Control I/O

QBEXT is an open-drain output that is driven low in Battery mode and high-impedance (pulled-up externally) in non-battery mode.

The Q_{BATT} in MAX77976 has a very low R_{DSON} that equals to 8.5mΩ. If the application requires a lower resistive discharging path then this output can be utilized to drive an external Q_{BATT} FET driver in parallel with internal Q_{BATT}. This output can be enabled or disabled by the QBEXT_CTRL bit.

Table 3. QBEXT Output in Different System Modes

SYSTEM MODE	USE CASE DETAILS	QBEXT OUTPUT
Battery Mode	All use cases except non-battery mode	Low
Non-Battery Mode	Valid adapter is present, and buck is switching (whatever charge status is) or MODE = 0x09 (Boost) or MODE = 0x0A (Boost + OTG)	Hi-Z (pulled-up)

Charge Status LED Indication

STAT is the LED current sink shown in the following tables based on the STAT_MODE bit.

The LED driving current can be programmed through I^2C STAT_CURR from 5mA to 20mA with a 5mA step.

Table 4. STAT_MODE = 0x0

CHG STATUS	LED	DUTY (%)
No DC input or Suspend or Buck operation	Off	0
Any Charging Timeout, Off by JEITA feature, Off by thermal shutdown	Blink in 2Hz	50
DBAT, Pre-Q, CC, CV	Blink in 1Hz	50
Top-off, Done, Restart	Solid on	100

Table 5. STAT_MODE = 0x1

CHG STATUS	LED	DUTY (%)
No DC input or Suspend or Buck operation	Off	0
Any Charging Timeout, Off by JEITA feature, Off by thermal shutdown	Off	0
DBAT, Pre-Q, CC, CV	Blink in 1Hz	50
Top-off, Done, Restart	Solid on	100

Design Considerations to Protect Against Hot Plug Event

In USB Type-C compatible applications, the output slew rate of the travel adaptor when changing output levels is defined by the USB Type-C spec to be within 30mV/µs. However, non-compliant USB adapters or high fixed voltage sources ≥ 15V can cause high inrush current during a hot plug event. The amount of inrush current that can flow through the IC is defined by the following equation:

- I_inrush = dVIN/dt x C_BYP

With the recommended 2 x 10µF 0805 package capacitance at BYP node (effective capacitance of 4µF at 12V), the max inrush current can be as high as 4A if dVIN/dt is within 1V/µs. During this rising edge, the Q_{CHGIN} FET is off, so all the current goes through the body diode. To prevent damaging the IC when the application uses a voltage source that is already "hot" when connected, or with a high input slew rate, connect an external Schottky diode with anode at CHGIN and cathode at BYP. The Schottky diode must be selected as follows:

- Calculate I_inrush with dVIN/dt information and assume C_BYP = 4µF
- Select the Shottky so that when forward voltage at room temperature is 0.45V, the current is less than I_inrush x 1.5

Example: 1V/µs max slew rate, I_inrush = 4A. The Schottky is chosen to be rated at least 6A at 0.45V.

Top System Management

Overview

This section discusses the top system of the MAX77975/MAX77976 and how the IC manages its bias, system faults, and turn-on and off events.

Main Bias

The main bias includes voltage and current references for all circuitry that runs from the V_{SYS} node.

System Faults

V_{SYS} Fault

The system monitors the V_{SYS} node for undervoltage and overvoltage events. The following describes the IC behavior if any of these events is to occur.

V_{SYS} Undervoltage Lockout ($V_{SYSUVLO}$)

V_{SYS} undervoltage lockout prevents the regulators from being used when the input voltage is below the operating range. When the voltage from SYS to GND (V_{SYS}) is less than the undervoltage-lockout threshold ($V_{SYSUVLO}$), MAX77975/MAX77976 shuts down and resets "O" Type I^2C registers.

V_{SYS} Overvoltage Lockout ($V_{SYSOVLO}$)

V_{SYS} overvoltage lockout is a fail-safe mechanism and prevents the regulators from being used when the input voltage is above the operating range. The absolute maximum ratings state that the SYS node withstands up to 6V. The SYS OVLO threshold is set to 5.35V (typ)—ideally V_{SYS} should not exceed the battery charge termination threshold. Systems must be designed such that V_{SYS} never exceeds 5.2V (transient and steady-state). If the V_{SYS} exceeds $V_{SYS\_OVLO\_R}$, the ICs shuts down and resets "O" Type I^2C registers.

V_{SYS} Power-Up Failure ($P_{WRUPFAIL}$)

V_{SYS} power-up failure is a hardware diagnostic mechanism to detect failures affecting the system and preventing the platform from powering up. When a **valid** power source (battery V_{BATT} > SYS_UVLOB_R or charger with V_{CHGIN} > $V_{CHGIN\_UVLO\_R}$**)** is plugged, MAX77975/MAX77976 is expected to pull SYS node up by means of one of the system power-up current sources (I_{SYSPU_BAT} or I_{SYSPU_BYP} respectively). If V_{SYS} does not rise above V_{SYSPU} due to a fault in the application (external to MAX77976), after a time-out elapses (t_{SYSPU_BAT} or t_{SYSPU_BYP} respectively) a power-up fault is asserted and an interrupt (PWRUP_FAIL_INT) is generated. Because the SYS node is down, the application software may not be able to service the interrupt; the interrupt can only be observed by pulling VIO up externally and serviced by taking control of the I^2C interface.

Thermal Fault

The ICs have one centralized thermal circuit which senses temperature on the die. If temperature increases >155°C (T_{SHDN}) this constitutes a thermal shutdown event and the MAX77976 shuts down and resets "O" Type I^2C registers. There is a 15°C thermal hysteresis. After thermal shutdown, if the die temperature is reduced by 15°C, the thermal shutdown bus is deasserted and the IC can be enabled again. The main battery charger has an independent thermal control loop which does not cause a thermal shutdown event. In the event that a charger thermal overload occurs, only the charger turns off.

System Faults Debounce Time

Applicable in charge or buck mode.

Table 6. System Faults Debounce Time Summary

	EDGE TO I/T		I/T TO FAULT		ACTION ON FAULT
	t_{DEB} (Rising)	t_{DEB} (Falling)	t_{DEB} (Rising)	t_{DEB} (Falling)	
SYS UVLO	—	—	8ms	—	O-Type reset
SYS OVLO	*-/100µs by I²C	—	—	—	O-Type reset
TSHDN	175µs	—	—	—	O-Type reset
OTG OCP	t_{OTG_ALARM}	—	t_{OTG_FAULT} - t_{OTG_ALARM}	—	RBFET opens

(*) depending on I²C bit SYSOVLO_DEB_EN

I²C Interface Description

Main I²C Interface

The IC acts as a Slave Transmitter/Receiver and has the following slave addresses:

Slave Address (7 bit) 0x6B 110 1011

Slave Address (Write) 0xD6 1101 0110

Slave Address (Read) 0xD7 1101 0111

I²C Bit Transfer

One data bit is transferred for each clock pulse. The data on SDA must remain stable during the high portion of the clock pulse as changes in data during this time are interpreted as a control signal.

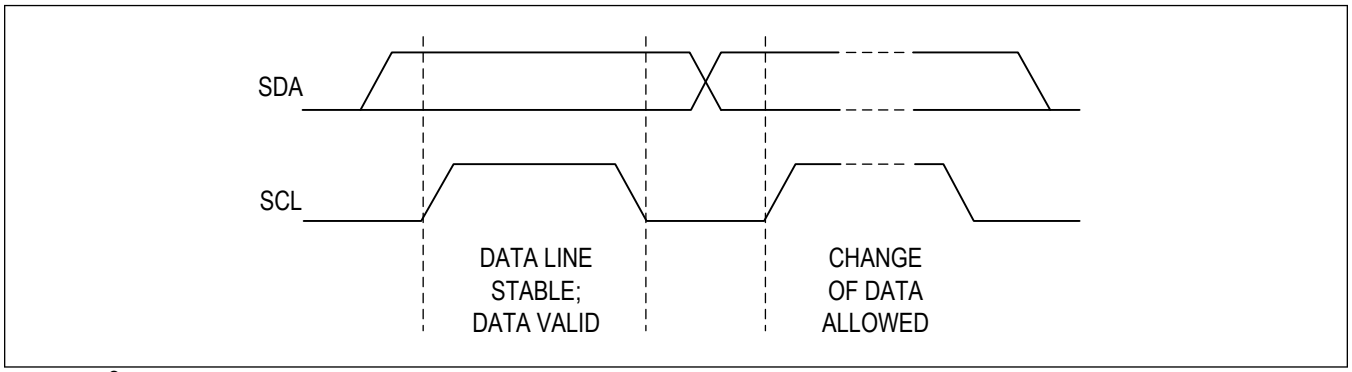


Figure 7. I²C Bit Transfer

I²C Start and Stop Conditions

Both SDA and SCL remain High when the bus is not busy. The Start (S) condition is defined as a high-to-low transition of the SDA while the SCL is high. The Stop (P) condition is defined as a low-to-high transition of the SDA while the SCL is high.

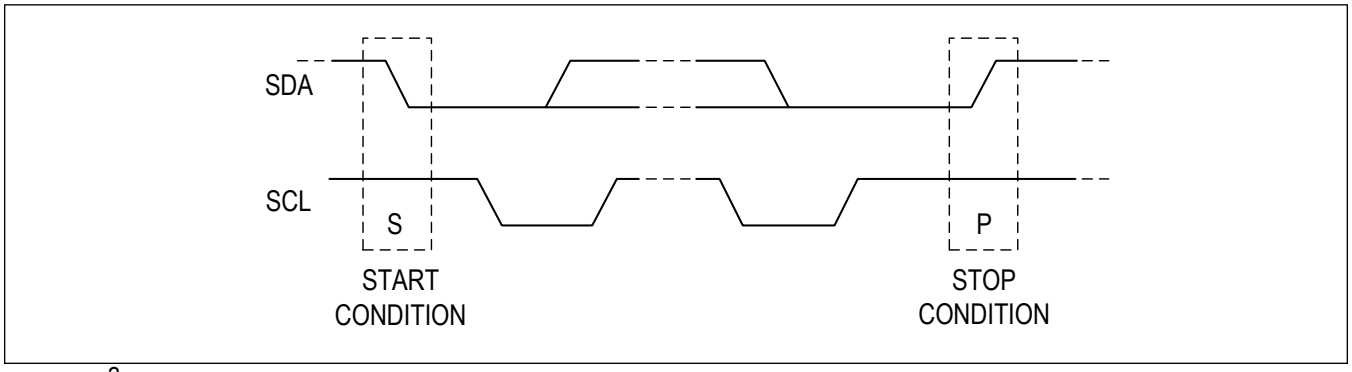


Figure 8. I²C Start and Stop

I²C System Configuration

A device on the I²C bus that generates a “message” is called a “Transmitter” and a device that receives the message is a “Receiver”. The device that controls the message is the “Master” and the devices that are controlled by the “Master” are called “Slaves”.

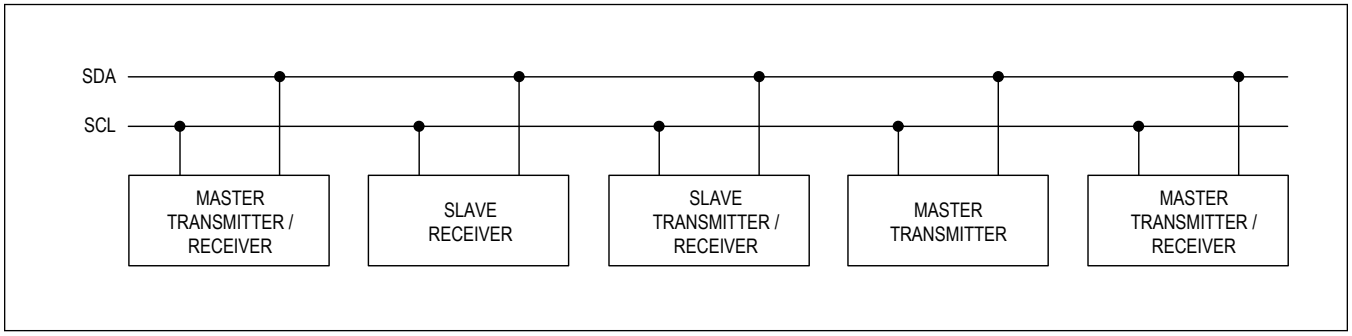


Figure 9. System Configurations

I²C Acknowledge

The number of data bytes between the start and stop conditions for the Transmitter and Receiver are unlimited.

Each 8-bit byte is followed by an Acknowledge bit. The Acknowledge bit is a high level signal put on SDA by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after each byte it receives. Also a master receiver must generate an acknowledge after each byte it receives that has been clocked out of the slave transmitter.

The device that acknowledges must pulldown the SDA line during the acknowledge-clock pulse, so that the SDA line is stable and low during the high period of the acknowledge-clock pulse (setup and hold times must also be met). A master receiver must signal the end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave SDA high to enable the master to generate a stop condition.

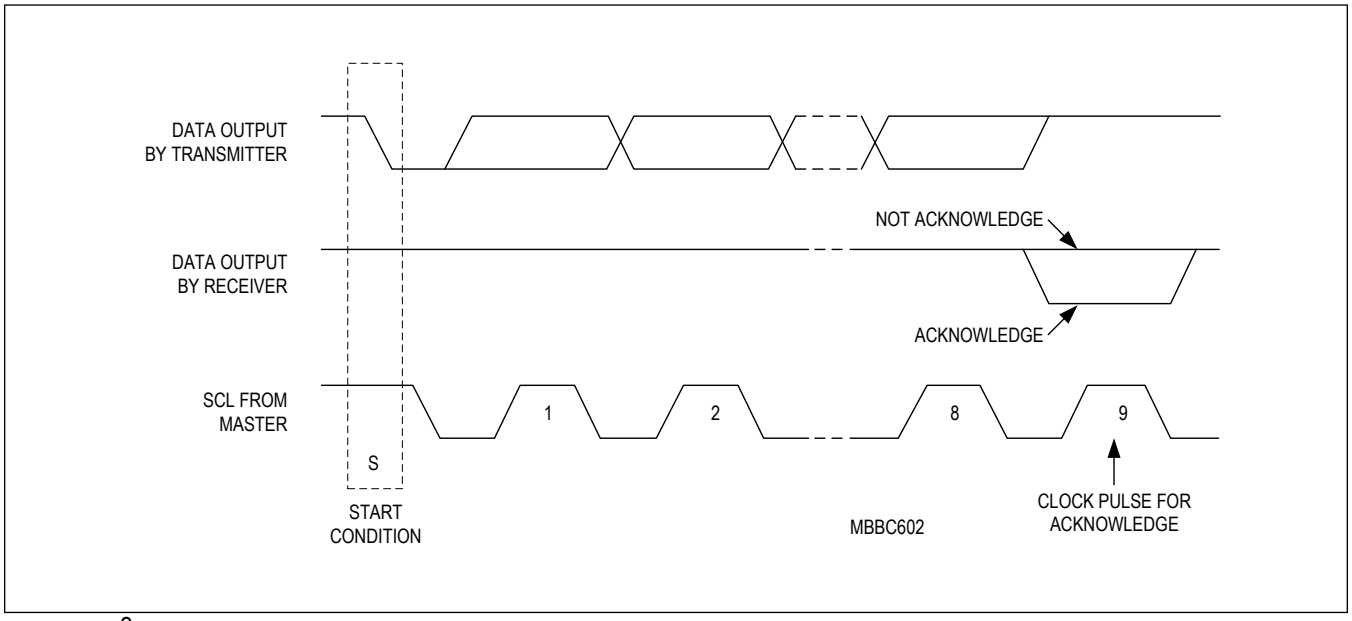


Figure 10. I²C Acknowledge

Master Transmits (Write Mode)

Use the following format when the master writes to the slave.

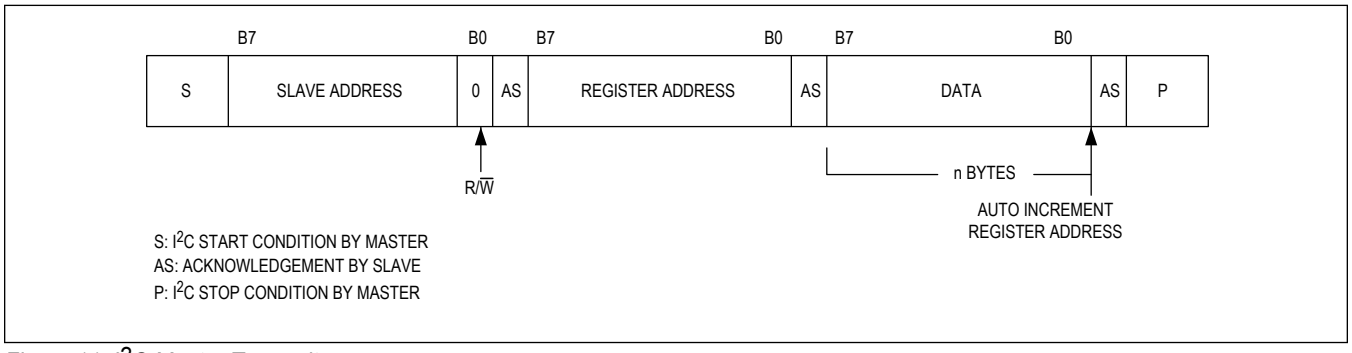


Figure 11. I²C Master Transmits

Master Reads after Setting Register Address (Write Register Address and Read Data)

Use the following format to read a specific register.

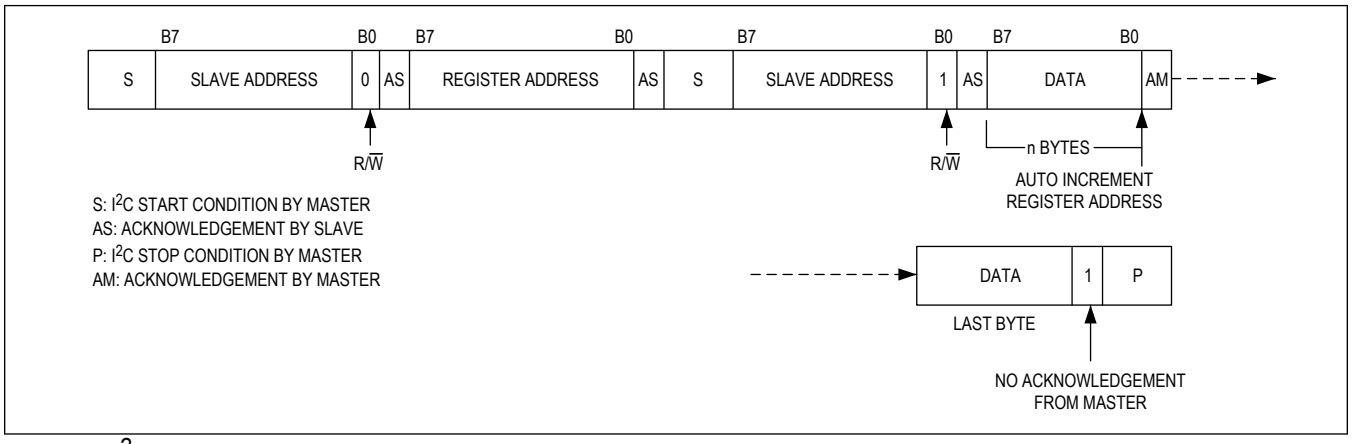


Figure 12. I2C Master Reads After Setting Register Address

Master Reads Register Data Without Setting Register Address (Read Mode)

Use the following format to read registers continuously starting from first address.

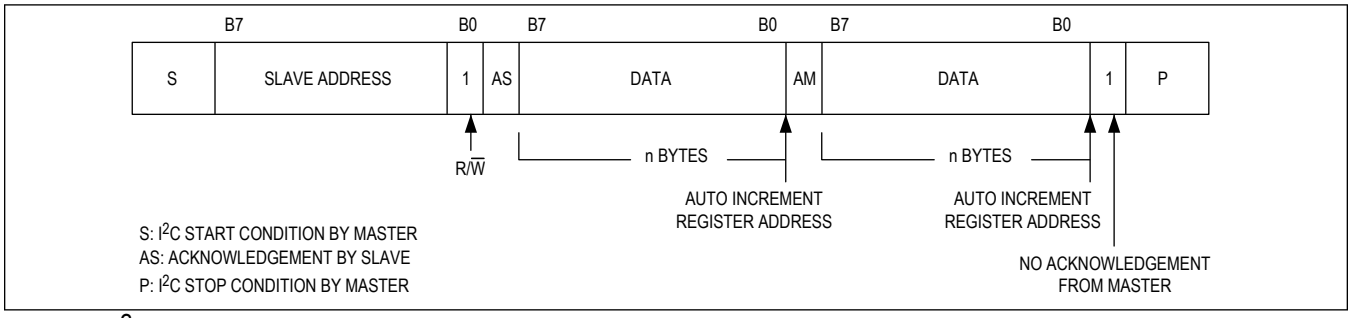


Figure 13. I2C Master Block Read

Register Map

TOP

I²C Slave Address

Slave Address (7 bit) 0x6B (7'b110 1011)

Slave Address (Write) 0xD6 (8'b1101 0110)

Slave Address (Read) 0xD7 (8'b1101 0111)

Functional Reset Conditions

The chip has different levels of reset as defined below:

• Type S: Registers are reset each time when: SYS < VDD (1.8V)

• Type O: Registers are reset each time when: SYS < VDD or SYS < SYS UVLO or SYS > SYS OVLO or die temp > T_{SHDN} or software reset (SW_RST)

ADDRESS	NAME	MSB							LSB
TOP_FUNC									
0x00	CHIP_ID[7:0]	ID[7:0]							
0x01	CHIP_REVISION[7:0]	VERSION[3:0]				REVISION[3:0]			
0x02	OTP_REVISION[7:0]	SPR_7_4[3:0]				OTP_REV[3:0]			
0x03	TOP_INT[7:0]	SPR_7	TSHDN_INT	SYSOVLO_INT	SYSUVLO_INT	SPR_3_1[2:0]			PWRUP_FAIL_INT
0x04	TOP_INT_MASK[7:0]	SPR_7	TSHDN_INT_M	SYSOVLO_INT_M	SYSUVLO_INT_M	SPR_3_1[2:0]			PWRUP_FAIL_INT_M
0x05	TOP_CTRL[7:0]	–	SPR_6_4[2:0]			LPM	SYSOVLO_DIS	SYSOVLO_DEB_EN	TSHDN_DIS
0x50	SW_RESET[7:0]	SWR_RST[7:0]							
0x51	SM_CTRL[7:0]	SPR_7_1[6:0]							EXTSM_T
I2C_FUNC									
0x40	I2C_CNFG[7:0]	SPR_7	RSVD[1:0]		PAIR	SPR_3_1[2:0]			HS_EXT_EN

Register Details

CHIP_ID (0x0)

PMIC ID

BIT	7	6	5	4	3	2	1	0
Field	ID[7:0]							
Reset	0x76							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ID	7:0	ID of MAX77976/MAX77975	0x76: MAX77976 0x75: MAX77975

CHIP_REVISION (0x1)

PMIC revision

BIT	7	6	5	4	3	2	1	0
Field	VERSION[3:0]				REVISION[3:0]			
Reset	0x0				0b010			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
VERSION	7:4	Version	
REVISION	3:0	Revision	0b001: PASS1 0b010: PASS2 0b011: PASS3 0b100: PASS4

OTP_REVISION (0x2)

BIT	7	6	5	4	3	2	1	0
Field	SPR_7_4[3:0]				OTP_REV[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
SPR_7_4	7:4	
OTP_REV	3:0	Revision

TOP_INT (0x3)

Top SYS Interrupts

BIT	7	6	5	4	3	2	1	0
Field	SPR_7	TSHDN_INT	SYSOVLO_INT	SYSUVLO_INT	SPR_3_1[2:0]			PWRUP_FAIL_INT
Reset	0b0	0b0	0b0	0b0	0x0			0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All			Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7	7		
TSHDN_INT	6	Thermal Shutdown Interrupt (entering fault condition)	0b0: No interrupt 0b1: Interrupt is detected
SYSOVLO_INT	5	SYSOVLO Interrupt (entering fault condition)	0b0: No interrupt 0b1: Interrupt is detected
SYSUVLO_INT	4	SYSUVLO Interrupt (entering fault condition)	0b0: No interrupt 0b1: Interrupt is detected
SPR_3_1	3:1		
PWRUP_FAIL_INT	0	PowerUp Fail Interrupt (entering fault condition)	0b0: No interrupt 0b1: Interrupt is detected

TOP_INT_MASK (0x4)

Top SYS Interrupt Mask

BIT	7	6	5	4	3	2	1	0
Field	SPR_7	TSHDN_INT_M	SYSOVLO_INT_M	SYSUVLO_INT_M	SPR_3_1[2:0]			PWRUP_FAIL_INT_M
Reset	0b1	0b1	0b1	0b1	0x7			0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7	7		
TSHDN_INT_M	6	Thermal Shutdown Interrupt Mask	0b0: Unmasked 0b1: Masked
SYSOVLO_INT_M	5	SYSOVLO Interrupt Mask	0b0: Unmasked 0b1: Masked
SYSUVLO_INT_M	4	SYSUVLO Interrupt Mask	0b0: Unmasked 0b1: Masked
SPR_3_1	3:1		
PWRUP_FAIL_INT_M	0	Powe-Up Fail Interrupt Mask	0b0: Unmasked 0b1: Masked

TOP_CTRL (0x5)

Main Control1

BIT	7	6	5	4	3	2	1	0
Field	–	SPR_6_4[2:0]			LPM	SYSOVLO_DIS	SYSOVLO_DEB_EN	TSHDN_DIS
Reset	–	0b000			0b0	0b0	0b0	0b1
Access Type	–	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_6_4	6:4		
LPM	3	Low-Power Mode Cycling mode is allowed for SYS UVLO, SYS OVLO, THERM comparators.	0: Low-power mode is disabled. SYSUVLO comparator is always ON. SYSOVLO comparator is controlled by SYSOVLO_DIS. THERM comparator is controlled by THRM_DIS. 1: Low-power mode is allowed. Comparators are periodically enabled (depending on SYSOVLO_DIS/THERM_DIS control)/disabled and cycling every 3ms.
SYSOVLO_DIS	2	SYSOVLO Disable	0: SYSOVLO comparator is enabled 1: SYSOVLO comparator is disabled
SYSOVLO_DEB_EN	1	SYSOVLO debounce (rising 100µs)	0: SYSOVLO debounce is disabled 1: SYSOVLO debounce is enabled
TSHDN_DIS	0	Internal Die Temperature Shutdown Disable Bit	1: T_{SHDN} comparator is disabled. 0: T_{SHDN} comparator is enabled.

SW_RESET (0x50)

SW-reset register

BIT	7	6	5	4	3	2	1	0
Field	SWR_RST[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SWR_RST	7:0	Software Reset.	0xA5: O-Type registers are reset.

SM_CTRL (0x51)

SW-reset register

BIT	7	6	5	4	3	2	1	0
Field	SPR_7_1[6:0]							EXTSM_T
Reset	0x00							0b0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7_1	7:1		
EXTSM_T	0	External Ship Mode Timer	0b0: 10ms 0b1: 0.1ms

I2C_CNFG (0x40)

BIT	7	6	5	4	3	2	1	0
Field	SPR_7	RSVD[1:0]		PAIR	SPR_3_1[2:0]			HS_EXT_EN
Reset	0b0	0b0		0b000	0b000			0b0
Access Type	Write, Read	Write, Read		Write, Read	Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7	7	Reserved	
RSVD	6:5	Reserved	
PAIR	4	Pair address mode option for register write burst operation.	1 = Pair address mode is enabled for the channel. 0 = Pair address mode is disabled and sequential mode is used.
SPR_3_1	3:1		
HS_EXT_EN	0	Enable HS-Mode Extension	0b0: HS-mode extension is disabled. (I^2C Rev. 4 Compliant) 0b1: HS-mode extension is enabled. HS-mode is enabled without HS-mode entrance code and keeps HS-mode during STOP condition.

CHARGER

ADDRESS	NAME	MSB							LSB
CHARGER_FUNC									
0x10	CHG_INT[7:0]	AICL_I	CHGIN_I	INLIM_I	CHG_I	BAT_I	RSVD_2	DISQBAT_I	BYP_I
0x11	CHG_INT_MASK[7:0]	AICL_M	CHGIN_M	INLIM_M	CHG_M	BAT_M	SPR_2	DISQBAT_M	BYP_M
0x12	CHG_INT_OK[7:0]	AICL_OK	CHGIN_OK	INLIM_OK	CHG_OK	BAT_OK	RSVD_2	DISQBAT_OK	BYP_OK
0x13	CHG_DETAILS_00[7:0]	RSVD_7	CHGIN_DTLS[1:0]		RSVD_4_3[1:0]		SPSN_DTLS[1:0]		RSVD_0
0x14	CHG_DETAILS_01[7:0]	TREG	BAT_DTLS[2:0]			CHG_DTLS[3:0]			
0x15	CHG_DETAILS_02[7:0]	RSVD_7	THM_DTLS[2:0]			BYP_DTLS[3:0]			
0x16	CHG_CNFG_00[7:0]	SPR_7_4[3:0]				MODE[3:0]			
0x17	CHG_CNFG_01[7:0]	TKEN	WDTEN	CHG_RSTRT[1:0]		SPR_3	FCHGTIME[2:0]		
0x18	CHG_CNFG_02[7:0]	SPR_7	CHG_CC[6:0]						
0x19	CHG_CNFG_03[7:0]	SPR_7	TO_TIME[2:0]			TO_ITH[3:0]			
0x1A	CHG_CNFG_04[7:0]	SYS_TRACK_DIS	RSVD_6_5[1:0]		CHG_CV_PRM[4:0]				
0x1B	CHG_CNFG_05[7:0]	Reserved	Reserved	Reserved	RECYCLE_EN	Reserved[3:0]			
0x1C	CHG_CNFG_06[7:0]	SPR_7_4[3:0]				CHGPROT[1:0]		WDTCLR[1:0]	
0x1D	CHG_CNFG_07[7:0]	WD_QBATOFF	SPR_6	DISIBS	SPSN_DET_EN	QBEXT_CTRL_EN	SPR_2_1[1:0]		FSHIP_MODE
0x1E	CHG_CNFG_08[7:0]	RSVD_7	SPR_6_5[1:0]		FMBST	SPR_3	SLOWLX	FSW	DISKIP
0x1F	CHG_CNFG_09[7:0]	INLIM_CLK[1:0]	CHGIN_ILIM[5:0]						
0x20	CHG_CNFG_10[7:0]	OTG_REC_EN	SPR_6_5[1:0]		OTG_ILIM[4:0]				
0x21	CHG_CNFG_11[7:0]	SPR_7	VBYPSET[6:0]						
0x22	CHG_CNFG_12[7:0]	BYPDISCHG_EN	DEEP_SUSP_DIS	VCHGIN_REG[1:0]		SPR_3_2[1:0]		BATRMV_MSK	DIS_AICL
0x23	CHG_CNFG_13[7:0]	JEITA_EN	SPR_6	CHG_CV_COOL	CHG_CC_WARM	REGTEMP[3:0]			
0x24	STAT_CNFG[7:0]	STAT_EN	SPR_6_4[2:0]			STAT_CURR[1:0]		SPR_1	STAT_MODE

Register Details

CHG_INT (0x10)

Interrupt status register for the charger block.

BIT	7	6	5	4	3	2	1	0
Field	AICL_I	CHGIN_I	INLIM_I	CHG_I	BAT_I	RSVD_2	DISQBAT_I	BYP_I
Reset						0x0		
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
AICL_I	7	AICL Interrupt	0b0: The AICL_OK bit has not changed since the last time this bit was read. 0b1: The AICL_OK bit has changed since the last time this bit was read.
CHGIN_I	6	CHGIN Interrupt	0b0: The CHGIN_OK bit has not changed since the last time this bit was read. 0b1: The CHGIN_OK bit has changed since the last time this bit was read.
INLIM_I	5	Input Current Limit Interrupt	0b0: The INLIM_OK bit has not changed since the last time this bit was read. 0b1: The INLIM_OK bit has changed since the last time this bit was read.
CHG_I	4	Charger Interrupt	0b0: The CHG_OK bit has not changed since the last time this bit was read. 0b1: The CHG_OK bit has changed since the last time this bit was read.
BAT_I	3	Battery Interrupt	0b0: The BAT_OK bit has not changed since the last time this bit was read. 0b1: The BAT_OK bit has changed since the last time this bit was read.
RSVD_2	2		
DISQBAT_I	1	DISQBAT Interrupt	0b0: The DISQBAT_OK bit has not changed since the last time this was read. 0b1: The DISQBAT_OK bit has changed since the last time this was read.
BYP_I	0	Bypass Node Interrupt	0b0: The BYP_OK bit has not changed since the last time this bit was read. 0b1: The BYP_OK bit has changed since the last time this bit was read.

CHG_INT_MASK (0x11)

Mask register to mask the corresponding charger interrupts.

BIT	7	6	5	4	3	2	1	0
Field	AICL_M	CHGIN_M	INLIM_M	CHG_M	BAT_M	SPR_2	DISQBAT_M	BYP_M
Reset	0b1	0b1	0b1	0b1	0b1	0x1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AICL_M	7	AICL Interrupt Mask	0b0: Unmasked 0b1: Masked
CHGIN_M	6	CHGIN Interrupt Mask	0b0: Unmasked 0b1: Masked
INLIM_M	5	Input Current Limit Interrupt Mask	0b0: Unmasked 0b1: Masked
CHG_M	4	Charger Interrupt Mask	0b0: Unmasked 0b1: Masked
BAT_M	3	Battery Interrupt Mask	0b0: Unmasked 0b1: Masked
SPR_2	2		

BITFIELD	BITS	DESCRIPTION	DECODE
DISQBAT_M	1	DISQBAT Interrupt Mask	0b0: Unmasked 0b1: Masked
BYP_M	0	Bypass Interrupt Mask	0b0: Unmasked 0b1: Masked

CHG_INT_OK (0x12)

BIT	7	6	5	4	3	2	1	0
Field	AICL_OK	CHGIN_OK	INLIM_OK	CHG_OK	BAT_OK	RSVD_2	DISQBAT_OK	BYP_OK
Reset	0x1	0x0	0x1	0x1	0x1	0x0	0x1	0x1
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
AICL_OK	7	AICL_OK Status	0b0: AICL mode 0b1: Not in AICL mode
CHGIN_OK	6	CHGIN Input Status Indicator	0b0: The CHGIN input is invalid. CHGIN_DTLS≠0x03 0b1: The CHGIN input is valid. CHGIN_DTLS=0x03
INLIM_OK	5	Input Current Limit Status Indicator	0b0: The CHGIN input current has been reaching the current limit for at least 30ms. 0b1: The CHGIN input current has not reached the current limit.
CHG_OK	4	Charger Status Indicator	0b0: The charger has suspended charging or T_{REG} = 1. 0b1: The charger is okay or the charger is off.
BAT_OK	3	Battery Status Indicator	0b0: The battery has an issue or the charger has been suspended. BAT_DTLS≠0x03, ≠0x04 and ≠0x07 0b1: The battery is okay. BAT_DTLS = 0x03,0x04 or 0x07
RSVD_2	2		
DISQBAT_OK	1	DISQBAT Status Indicator	0b0: DISQBAT is high and Q_{BATT} is disabled. 0b1: DISQBAT is low and Q_{BATT} is not disabled.
BYP_OK	0	Bypass Status Indicator.	0b0: Something powered by the bypass node has hit current limit. BYP_DTLS≠0x00 0b1: The bypass node is okay. BYP_DTLS=0x00

CHG_DETAILS_00 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	RSVD_7	CHGIN_DTLS[1:0]		RSVD_4_3[1:0]		SPSN_DTLS[1:0]		RSVD_0
Reset	0x0			0x0				0b0
Access Type	Read Only	Read Only		Read Only		Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD_7	7		

BITFIELD	BITS	DESCRIPTION	DECODE
CHGIN_DTLS	6:5	CHGIN Details	0b00: VBUS is invalid. V_{CHGIN} rising: $V_{CHGIN} < V_{CHGIN\_UVLO}$ V_{CHGIN} falling: $V_{CHGIN} < V_{CHGIN\_REG}$ (AICL) 0b01: VBUS is invalid. $V_{CHGIN} < V_{BATT} + V_{CHGIN2SYS}$ and $V_{CHGIN} > V_{CHGIN\_UVLO}$ 0b10: VBUS is invalid. $V_{CHGIN} > V_{CHGIN\_OVLO}$ 0b11: VBUS is valid. $V_{CHGIN} > V_{CHGIN\_UVLO}$ and $V_{CHGIN} > V_{BATT} + V_{CHGIN2SYS}$ and $V_{CHGIN} < V_{CHGIN\_OVLO}$
RSVD_4_3	4:3		
SPSN_DTLS	2:1	SP/SN Remonte Sense Battery Line Connection Status	0b00: SPSN remote sense line is connected. 0b01: SP remote sense line detected as opened. 0b10: SN remote sense line detected as opened. 0b11: SP and SN remote sense lines are both detected as opened.
RSVD_0	0	Spare Bit	

CHG_DETAILS_01 (0x14)

BIT	7	6	5	4	3	2	1	0
Field	TREG	BAT_DTLS[2:0]			CHG_DTLS[3:0]			
Reset								
Access Type	Read Only	Read Only			Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
TREG	7	Temperature Regulation Status	0b0: The junction temperature is less than the threshold set by REGTEMP and the full charge current limit is available. 0b1: The junction temperature is greater than the threshold set by REGTEMP and the charge current limit may be folding back to reduce power dissipation.

BITFIELD	BITS	DESCRIPTION	DECODE
BAT_DTLS	6:4	Battery Details	0b000: Battery Removal A valid adpater is present and the battery is detached, detected on THM pin. 0b001: Battery Prequalification Voltage A valid adapter is present and the battery voltage is low: $V_{BATT} < V_{TRICKLE}$. **Note:** This condition is also reported in the CHG_DTLS as 0x00. 0b010: Battery Timer Fault A valid adapter is present and the battery has taken longer than expected to charge (exceeded t_{FC}). This could be due to high system currents, an old battery, a damaged battery, or something else. Charging has suspended and the charger is in timer-fault mode. **Note:** This condition is also reported in the CHG_DTLS as 0x06. 0b011: Battery Regular Voltage A valid adapter is present and the battery voltage is greater than the minimum system regulation level but lower than overvoltage level: $V_{SYSMIN} < V_{BATT} < V_{BATTREG} + V_{COV}$ V_{SYS} is approximately equal to V_{BATT}. 0b100: Battery Low Voltage A valid adapter is present and the battery voltage is lower than the minimum system regulation level but higher than prequalification voltage: $V_{TRICKLE} < V_{BATT} < V_{SYSMIN}$ V_{SYS} is regulated at least equal to V_{SYSMIN}. 0b101: Battery Overvoltage A valid adapter is present and the battery voltage is greater than the battery-overvoltage threshold ($V_{BATTREG} + V_{COV}$) for the last 30ms. **Note:** This flag is only generated when there is a valid input. 0b110: Reserved 0b111: Battery Only No valid adapter is present The battery voltage and battery removal monitoring are not available. **Note:** In case of deep suspend, it is considered that no valid adapter is present.

BITFIELD	BITS	DESCRIPTION	DECODE
CHG_DTLS	3:0	Charger Details	0x00: Charger is in dead-battery prequalification or low-battery prequalification mode. CHG_OK = 1 and $V_{BATT} < V_{PQLB}$ and $T_J < T_{SHDN}$ 0x01: Charger is in fast-charge constant current mode. CHG_OK = 1 and $V_{BATT} < V_{BATTREG}$ and $T_J < T_{SHDN}$ 0x02: Charger is in fast-charge constant voltage mode. CHG_OK = 1 and $V_{BATT} = V_{BATTREG}$ and $T_J < T_{SHDN}$ 0x03: Charger is in top-off mode. CHG_OK = 1 and $V_{BATT} = V_{BATTREG}$ and $T_J < T_{SHDN}$ 0x04: Charger is in done mode. CHG_OK = 0 and $V_{BATT} > V_{BATTREG} - V_{RSTRT}$ and $T_J < T_{SHDN}$ 0x05: Reserved 0x06: Charger is in timer-fault mode. CHG_OK = 0 and if BAT_DTLS=0b001 then $V_{BATT} < V_{PQLB}$ or $V_{BATT} < V_{PQDB}$ and $T_J < T_{SHDN}$ 0x07: Charger is suspended because Q_{BATT} is disabled (DISQBAT = H or DISIBS = 1). CHG_OK = 0 0x08: Charger is off, charger input invalid and/or charger is disabled. CHG_OK = 1 0x09: Reserved 0x0A: Charger is off and the junction temperature is > T_{SHDN}. CHG_OK = 0 0x0B: Charger is off because the watchdog timer expired. CHG_OK = 0 0x0C: Charger is suspended or charge current or voltage is reduced based on JEITA control. This condition is also reported in THM_DTLS. CHG_OK = 0 0x0D: Charger is suspended because battery removal is detected on THM pin. This condition is also reported in THM_DTLS. CHG_OK = 0 0x0E: Charger is suspended because SUSPEND pin is high. CHG_OK = 0 0x0F: Reserved

CHG_DETAILS_02 (0x15)

BIT	7	6	5	4	3	2	1	0
Field	RSVD_7	THM_DTLS[2:0]			BYP_DTLS[3:0]			
Reset								
Access Type	Read Only	Read Only			Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD_7	7		
THM_DTLS	6:4	Thermistor Details	0b000: Low temperature and charging suspended (COLD) 0b001: Low temperature charging (COOL) 0b010: Normal temperature charging (NORMAL) 0b011: High temperature charging (WARM) 0b100: High temperaure and charging suspended (HOT) 0b101: Battery removal detected on THM pin 0b110: Thermistor monitoring is disabled 0b111: RSVD
BYP_DTLS	3:0	Bypass Node Details	0x0: The bypass node is okay. 0x1: OTG_ILIM when CHG_CNFG_00.MODE=0xA or 0xE or 0xF The BYP to CHGIN switch (OTG switch) current limit was reached within the last 37.5ms. BYP_DTLS[0] status bit is latched until CHG_DETAILS_02 register read access is performed by AP. 0x2: BSTILIM The BYP reverse boost converter has hit its current limit and condition persisted for 30ms. 0x4: BCKNegILIM The BYP buck converter has hit the max negative demand current limit BYP_DTLS[2] status bit is latched until CHG_DETAILS_02 register read access is performed by AP. 0x8: BST_SWON_DONE (This status bit is only available in CHG_CNFG_00.MODE=0x9) The BYP reverse boost converter switch-on is done and V_{BYP} reached the V_{BYPSET} target.

CHG_CNFG_00 (0x16)

Charger configuration 0

BIT	7	6	5	4	3	2	1	0
Field	SPR_7_4[3:0]				MODE[3:0]			
Reset	0x0				0x4			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7_4	7:4	Spare Bit	

BITFIELD	BITS	DESCRIPTION	DECODE
MODE	3:0	Smart Power Selector Configuration	0x0: Charger = off, OTG = off, buck = off, boost = off. The Q_{BATT} switch is on to allow the battery to support the system. BYP may or may not be biased based on the CHGIN availability. 0x1: Same as 0b0000 0x2: Same as 0b0000 0x3: Same as 0b0000 0x4: Charger = off, OTG = off, buck = on, boost = off. When there is a valid input, the buck converter regulates the system voltage to be the maximum of (Vminsys and V_{BATT} +4%). V_{BYP} is equal to V_{CHGIN} minus the resistive drops. 0x5: Charger = on, OTG = off, buck = on, boost = off. When there is a valid input, the battery is charging. V_{SYS} is the larger of V_{SYSMIN} and ~V_{BATT} + IBATT x RBAT2SYS. V_{BYP} is equal to V_{CHGIN} minus the resistive drops. 0x6: Same as 0b0101 0x7: Same as 0b0101 0x8: Reserved 0x9: Charger = off, OTG = off, buck = off, boost = on. The Q_{BATT} switch is on to allow the battery to support the system, the charger's DC-DC operates as a boost converter. BYP voltage is regulated to V_{BYPSET}. Q_{CHGIN} is off. 0xA: Charger = off, OTG = on, buck = off, boost = on. The Q_{BATT} switch is on to allow the battery to support the system, the charger's DC-DC operates as a boost converter. BYP voltage is regulated to V_{BYPSET}. Q_{CHGIN} is on allowing it to source current up to ICHGIN.OTG.LIM. 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved

CHG_CNFG_01 (0x17)

Charger configuration 1

BIT	7	6	5	4	3	2	1	0
Field	TKEN	WDTEN	CHG_RSTRT[1:0]		SPR_3	FCHGTIME[2:0]		
Reset	0b1	0b0	0b01		0b0	0b011		
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TKEN	7	Trickle Charge Enable	0b0: Trickle charge is disabled: When V_{BATT} is in trickle charge voltage range, charge current target level is I_{FC}. 0b1: Trickle charge is enabled: When V_{BATT} is in trickle charge voltage range, charge current target level is $I_{TRICKLE}$.

BITFIELD	BITS	DESCRIPTION	DECODE
WDTEN	6	Watchdog Timer Enable Bit	0b0: Watchdog timer disabled. 0b1: Watchdog timer enabled.
CHG_RSTRT	5:4	Charger-Restart Threshold	0b00: 100mV below the value programmed by CHG_CV_PRM. 0b01: 150mV below the value programmed by CHG_CV_PRM. 10: 200mV below the value programmed by CHG_CV_PRM. 11: Disabled
SPR_3	3	Spare Bit	
FCHGTIME	2:0	Fast-Charge Timer Setting (t_{FC}, hrs)	0b000: Disable 0b001: 3 0b010: 4 0b011: 5 0b100: 6 0b101: 7 0b110: 8 0b111: Do not configure

CHG_CNFG_02 (0x18)

Charger configuration 2

BIT	7	6	5	4	3	2	1	0
Field	SPR_7	CHG_CC[6:0]						
Reset	0b0	0x09						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7	7	Spare Bit	

BITFIELD	BITS	DESCRIPTION	DECODE
CHG_CC	6:0	Fast-Charge Current Selection (mA). When the charger is enabled, the charge current limit is set by these bits. These bits range from 0.10A (0x00) to 5.5A (0x6E) in 50mA step. Note that the first three codes are all 100mA. Note that the thermal-foldback loop can reduce the battery charger's target current by A_{TJREG}. Note that the fast-charge current is clamped at 3.5A from 0x46 to 0x7F in MAX77975.	Value: Decode 0x00: 100 0x01: 100 0x02: 100 0x03: 150 0x04: 200 0x05: 250 0x06: 300 0x07: 350 0x08: 400 0x09: 450 0x0A: 500 0x0B: 550 0x0C: 600 0x0D: 650 0x0E: 700 0x0F: 750 0x10: 800 0x11: 850 0x12: 900 0x13: 950 0x14: 1000 0x15: 1050 0x16: 1100 0x17: 1150 0x18: 1200 0x19: 1250 0x1A: 1300 0x1B: 1350 0x1C: 1400 0x1D: 1450 0x1E: 1500 0x1F: 1550 0x20: 1600 0x21: 1650 0x22: 1700 0x23: 1750 0x24: 1800 0x25: 1850 0x26: 1900 0x27: 1950 0x28: 2000 0x29: 2050 0x2A: 2100 0x2B: 2150 0x2C: 2200 0x2D: 2250 0x2E: 2300 0x2F: 2350 0x30: 2400 0x31: 2450 0x32: 2500 0x33: 2550 0x34: 2600 0x35: 2650 0x36: 2700 0x37: 2750 0x38: 2800 0x39: 2850

BITFIELD	BITS	DESCRIPTION	DECODE
			0x3A: 2900 0x3B: 2950 0x3C: 3000 0x3D: 3050 0x3E: 3100 0x3F: 3150 0x40: 3200 0x41: 3250 0x42: 3300 0x43: 3350 0x44: 3400 0x45: 3450 0x46: 3500 0x47: 3550 0x48: 3600 0x49: 3650 0x4A: 3700 0x4B: 3750 0x4C: 3800 0x4D: 3850 0x4E: 3900 0x4F: 3950 0x50: 4000 0x51: 4050 0x52: 4100 0x53: 4150 0x54: 4200 0x55: 4250 0x56: 4300 0x57: 4350 0x58: 4400 0x59: 4450 0x5A: 4500 0x5B: 4550 0x5C: 4600 0x5D: 4650 0x5E: 4700 0x5F: 4750 0x60: 4800 0x61: 4850 0x62: 4900 0x63: 4950 0x64: 5000 0x65: 5050 0x66: 5100 0x67: 5150 0x68: 5200 0x69: 5250 0x6A: 5300 0x6B: 5350 0x6C: 5400 0x6D: 5450 0x6E: 5500 0x6F: 5500 0x70: 5500 0x71: 5500 0x72: 5500 0x73: 5500 0x74: 5500

BITFIELD	BITS	DESCRIPTION	DECODE
			0x75: 5500 0x76: 5500 0x77: 5500 0x78: 5500 0x79: 5500 0x7A: 5500 0x7B: 5500 0x7C: 5500 0x7D: 5500 0x7E: 5500 0x7F: 5500

CHG_CNFG_03 (0x19)

Charger configuration 3

BIT	7	6	5	4	3	2	1	0
Field	SPR_7	TO_TIME[2:0]			TO_ITH[3:0]			
Reset	0b0	0b011			0b0010			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7	7	Spare Bit	
TO_TIME	6:4	Top-Off Timer Setting (min)	0b000: 30sec 0b001: 10 0b010: 20 0b011: 30 0b100: 40 0b101: 50 0b110: 60 0b111: 70
TO_ITH	3:0	Top-Off Current Threshold (mA). The charger transitions from its fast charge constant voltage mode to its top-off mode when the charger current decays to the value programmed by this register. This transition generates a CHG_I interrupt and causes the CHG_DTLS register to report top-off mode. This transition also starts the top-off time as programmed by TO_TIME.	0b0000: Disable 0b0001: 150mA 0b0010: 200mA 0b0011: 250mA 0b0100: 300mA 0b0101: 350mA 0b0110: 400mA 0b0111: 450mA 0b1000: 500mA 0b1001: 550mA 0b1010: 600mA 0b1011: 650mA 0b1100: 700mA 0b1101: 750mA 0b1110: 800mA 0b1111: 850mA

CHG_CNFG_04 (0x1A)

Charger configuration 4

BIT	7	6	5	4	3	2	1	0
Field	SYS_TRACK_DIS	RSVD_6_5[1:0]		CHG_CV_PRM[4:0]				
Reset	0b0	0b10		0x05				
Access Type	Write, Read	Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
SYS_TRACK_DIS	7	BUCK SYS tracking disable control.	0x0: SYS tracking is enabled. In Buck mode, SYS is regulated to MAX of (V_{BATT} +4% , V_{MINSYS}). This is also valid in charge Done state. 0x1: SYS tracking is disabled. In Buck mode, SYS is regulated to $V_{BATTERM}$.
RSVD_6_5	6:5	Spare Bit	
CHG_CV_PRM	4:0	Charge Termination Voltage Setting(V)	Value: Decode 0x00: 4.15 0x01: 4.16 0x02: 4.17 0x03: 4.18 0x04: 4.19 0x05: 4.20 0x06: 4.21 0x07: 4.22 0x08: 4.23 0x09: 4.24 0x0A: 4.25 0x0B: 4.26 0x0C: 4.27 0x0D: 4.28 0x0E: 4.29 0x0F: 4.30 0x10: 4.31 0x11: 4.32 0x12: 4.33 0x13: 4.34 0x14: 4.35 0x15: 4.36 0x16: 4.37 0x17: 4.38 0x18: 4.39 0x19: 4.40 0x1A: 4.41 0x1B: 4.42 0x1C: 4.43 0x1D: 4.44 0x1E: 4.45 0x1F: 4.46

CHG_CNFG_05 (0x1B)

Charger configuration 5

BIT	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	RECYCLE_EN	Reserved[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	7	Reserved	Reserved
Reserved	6	Reserved	Reserved
Reserved	5	Reserved	Reserved
RECYCLE_EN	4	DISIBS Event Recycle Option	0b0: In case of DISIBS events, buck is disabled (OFF) and Q_{BATT} FET is opened. System recycles after 150ms (min) only in case a valid charger is present. 0b1: In case of DISIBS events, buck is disabled (OFF) and Q_{BATT} FET is opened. System recycles after 150ms (min).
Reserved	3:0	Reserved	Reserved

CHG_CNFG_06 (0x1C)

Charger configuration 6

BIT	7	6	5	4	3	2	1	0
Field	SPR_7_4[3:0]				CHGPROT[1:0]		WDTCLR[1:0]	
Reset	0x0				0b00		0b00	
Access Type	Write, Read				Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_7_4	7:4	Spare Bit	
CHGPROT	3:2	Charger Settings Protection Bit Writing "11" to these bits unlocks the write capability for the registers who are "Protected with CHGPROT". Writing any value besides "11" locks these registers.	0b00: Write capability locked 0b01: Write capability locked 0b10: Write capability locked 0b11: Write capability unlocked
WDTCLR	1:0	Watchdog Timer Clear Bit. Writing "01" to these bits clears the watchdog timer when the watchdog timer is enabled.	0b00: The watchdog timer is not cleared. 0b01: The watchdog timer is cleared. 0b10: The watchdog timer is not cleared. 0b11: The watchdog timer is not cleared.

CHG_CNFG_07 (0x1D)

Charger configuration 7

BIT	7	6	5	4	3	2	1	0
Field	WD_QBAT OFF	SPR_6	DISIBS	SPSN_DET_EN	QBEXT_CTRL_EN	SPR_2_1[1:0]		FSHIP_MODE
Reset	0b0	0b0	0b0	0b0	0b0	0b00		0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WD_QBATOFF	7	Q_{BATT} FET Control Under Watchdog Condition	0b0: When watchdog timer expires, turn off only the charger. 0b1: When watchdog timer expires, turn off buck, charger, and Q_{BATT} switch for 150ms.
SPR_6	6	Spare Bit	
DISIBS	5	BATT to SYS FET Disable Control	0b0: BATT to SYS FET is controlled by the power-path state machine. 0b1: BATT to SYS FET is forced off.
SPSN_DET_EN	4	SPSN Remote Sense Line Detection Enable. Enable SPSN remote sense line detection only when MODE = 0x0 (*detection is discarded if not*). End of SPSN detction triggers a BAT_I interrupt. Detection result available in dedicated status bit field SPSN_DTLS[1:0].	0b0: SPSN remote sense line detection disabled. 0b1: SPSN remote sense line detection enabled.
QBEXT_CTRL_EN	3		0b0: External Q_{BATT} control is disabled. 0b1: External Q_{BATT} control is enabled.
SPR_2_1	2:1	Spare Bit	
FSHIP_MODE	0	Factory-Ship Mode. When asserted to "1", system enters into factory-ship mode. This bit can be reset by battery removal or on a valid charger input plug.	0b0: Not factory-ship mode. 0b1: Factory-ship mode.

CHG_CNFG_08 (0x1E)

Charger configuration 8

BIT	7	6	5	4	3	2	1	0
Field	RSVD_7	SPR_6_5[1:0]		FMBST	SPR_3	SLOWLX	FSW	DISKIP
Reset	0x0	0b0		0b0	0b0	0b0	0b1	0b0
Access Type	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD_7	7	Reserved Bit	
SPR_6_5	6:5	Spare Bit	
FMBST	4	Factory Mode Boost	0b0: When DISQBAT = high, any mode change is not possible. 0b1: When DISQBAT = high, this bit makes mode change (Boost mode) possible.
SPR_3	3	Spare Bit	
SLOWLX	2	LX Slope Control Options	0b0: Fastest LX slope without control. 0b1: Slowest LX slope.
FSW	1	Switching Frequency Options (MHz)	0b0: 2.6 0b1: 1.3
DISKIP	0	Charger Skip Mode Disable	0b0: Auto skip mode. 0b1: Disable skip mode.

CHG_CNFG_09 (0x1F)

Charger configuration 9

BIT	7	6	5	4	3	2	1	0
Field	INLIM_CLK[1:0]		CHGIN_ILIM[5:0]					
Reset	0b10		0x09					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
INLIM_CLK	7:6	Input Current Limit Soft Start Clock(µsec)	0b00: 8 0b01: 256 0b10: 1024 0b11: 4096

BITFIELD	BITS	DESCRIPTION	DECODE
CHGIN_ILIM	5:0	CHGIN Input Current Limit (mA) 6 Bit adjustment from100mA to 3.2A in 50mA steps. Note that the first two codes are all 100mA.	0x00: 100 0x01: 100 0x02: 150 0x03: 200 0x04: 250 0x05: 300 0x06: 350 0x07: 400 0x08: 450 0x09: 500 0x0A: 550 0x0B: 600 0x0C: 650 0x0D: 700 0x0E: 750 0x0F: 800 0x10: 850 0x11: 900 0x12: 950 0x13: 1000 0x14: 1050 0x15: 1100 0x16: 1150 0x17: 1200 0x18: 1250 0x19: 1300 0x1A: 1350 0x1B: 1400 0x1C: 1450 0x1D: 1500 0x1E: 1550 0x1F: 1600 0x20: 1650 0x21: 1700 0x22: 1750 0x23: 1800 0x24: 1850 0x25: 1900 0x26: 1950 0x27: 2000 0x28: 2050 0x29: 2100 0x2A: 2150 0x2B: 2200 0x2C: 2250 0x2D: 2300 0x2E: 2350 0x2F: 2400 0x30: 2450 0x31: 2500 0x32: 2550 0x33: 2600 0x34: 2650 0x35: 2700 0x36: 2750 0x37: 2800 0x38: 2850 0x39: 2900 0x3A: 2950

BITFIELD	BITS	DESCRIPTION	DECODE
			0x3B: 3000 0x3C: 3050 0x3D: 3100 0x3E: 3150 0x3F: 3200

CHG_CNFG_10 (0x20)

Charger configuration 10

BIT	7	6	5	4	3	2	1	0
Field	OTG_REC_EN	SPR_6_5[1:0]		OTG_ILIM[4:0]				
Reset	0b0	0b0		0x00				
Access Type	Write, Read	Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OTG_REC_EN	7	OTG OCP Event Recycle Option	1b0: In case of OTG OCP, OTG FET is disabled (OFF = opened). System does not recycle OTG output. 1b1: In case of OTG OCP, OTG FET is disabled (OFF = opened). OTG recycles after T_{OTG}, retry.
SPR_6_5	6:5	Spare Bit	

BITFIELD	BITS	DESCRIPTION	DECODE
OTG_ILIM	4:0	CHGIN OTG Output Current Limit (mA) When the boost-OTG mode (MODE = 0xA) is enabled, the OTG output current limit is set by these bits. These bits range from 0.50A (0x00) to 3.1A (0x1A) in 100mA steps. Note that the OTG output current limit is clamped at 2.4A from 0x13 to 0x1F in MAX77975.	Value: Decode 0x00: 500 0x01: 600 0x02: 700 0x03: 800 0x04: 900 0x05: 1000 0x06: 1100 0x07: 1200 0x08: 1300 0x09: 1400 0x0A: 1500 0x0B: 1600 0x0C: 1700 0x0D: 1800 0x0E: 1900 0x0F: 2000 0x10: 2100 0x11: 2200 0x12: 2300 0x13: 2400 0x14: 2500 0x15: 2600 0x16: 2700 0x17: 2800 0x18: 2900 0x19: 3000 0x1A: 3100 0x1B: 3100 0x1C: 3100 0x1D: 3100 0x1E: 3100 0x1F: 3100

CHG_CNFG_11 (0x21)

Charger configuration 11

BIT	7	6	5	4	3	2	1	0
Field	SPR_7	VBYPSET[6:0]						
Reset	0b0	0x1						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
SPR_7	7	Spare Bit
VBYPSET	6:0	V_{BYP} Target Output Voltage(V). Bypass target output voltage in boost mode. MODE = 0x9/0xA. 5.0V to 12.0V with 100mV step.

CHG_CNFG_12 (0x22)

Charger configuration 12

BIT	7	6	5	4	3	2	1	0
Field	BYPDISCHG_EN	DEEP_SUSP_DIS	VCHGIN_REG[1:0]		SPR_3_2[1:0]		BATRMV_MSK	DIS_AICL
Reset	0b0	0b0	0b01		0b00		0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BYPDISCHG_EN	7	Boost BYP Discharge after Overshoot When enabled, if BYP is seen to be above target, a soft pulldown is activated to discharge BYP back to target, even if auto-skip mode is active.	0b0: Disabled 0b1: Enabled
DEEP_SUSP_DIS	6	When SUSPND pin pulls high or in MODE 0, input FET is enabled or disabled by this bit.	0b0: Disabled 0b1: Enabled
VCHGIN_REG	5:4	CHGIN Voltage Regulation Threshold (V_{CHGIN_REG}) Adjustment. The CHGIN to GND minimum turn-on threshold (V_{CHGIN_UVLO}) also scales with this adjustment.	0b00: V_{CHGIN_REG} = 4.5V and V_{CHGIN_UVLO} = 4.7V 0b01: V_{CHGIN_REG} = 4.6V and V_{CHGIN_UVLO} = 4.8V 0b10: V_{CHGIN_REG} = 4.7V and V_{CHGIN_UVLO} = 4.9V 0b11: V_{CHGIN_REG} = 4.85V and V_{CHGIN_UVLO} = 5.05V
SPR_3_2	3:2	Spare Bit	
BATRMV_MSK	1	Battery Removal Detection Masking When masked, battery removal detection is ignored.	0b0: Unmasked 0b1: Masked
DIS_AICL	0	AICL Disable Feature	0b0: AICL feature is not disabled. 0b1: AICL feature is disabled.

CHG_CNFG_13 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	JEITA_EN	SPR_6	CHG_CV_COOL	CHG_CC_WARM	REGTEMP[3:0]			
Reset	0b0	0b0	0b0	0b0	0x6			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
JEITA_EN	7	JEITA Enable	0x0: JEITA disabled Fast charge current and charge termination voltage do not change based on thermistor temperature. 0x1: JEITA enabled Fast charge current and charge termination voltage change based on thermistor temperature.
SPR_6	6	Spare Bit	
CHG_CV_COOL	5	JEITA controlled battery termination voltage when thermistor temperature is between T_{COLD} and T_{COOL}.	0x0: Battery termination voltage is set by CHG_CV_PRM. 0x1: Battery termination voltage is set by (CHG_CV_PRM - 150mV).

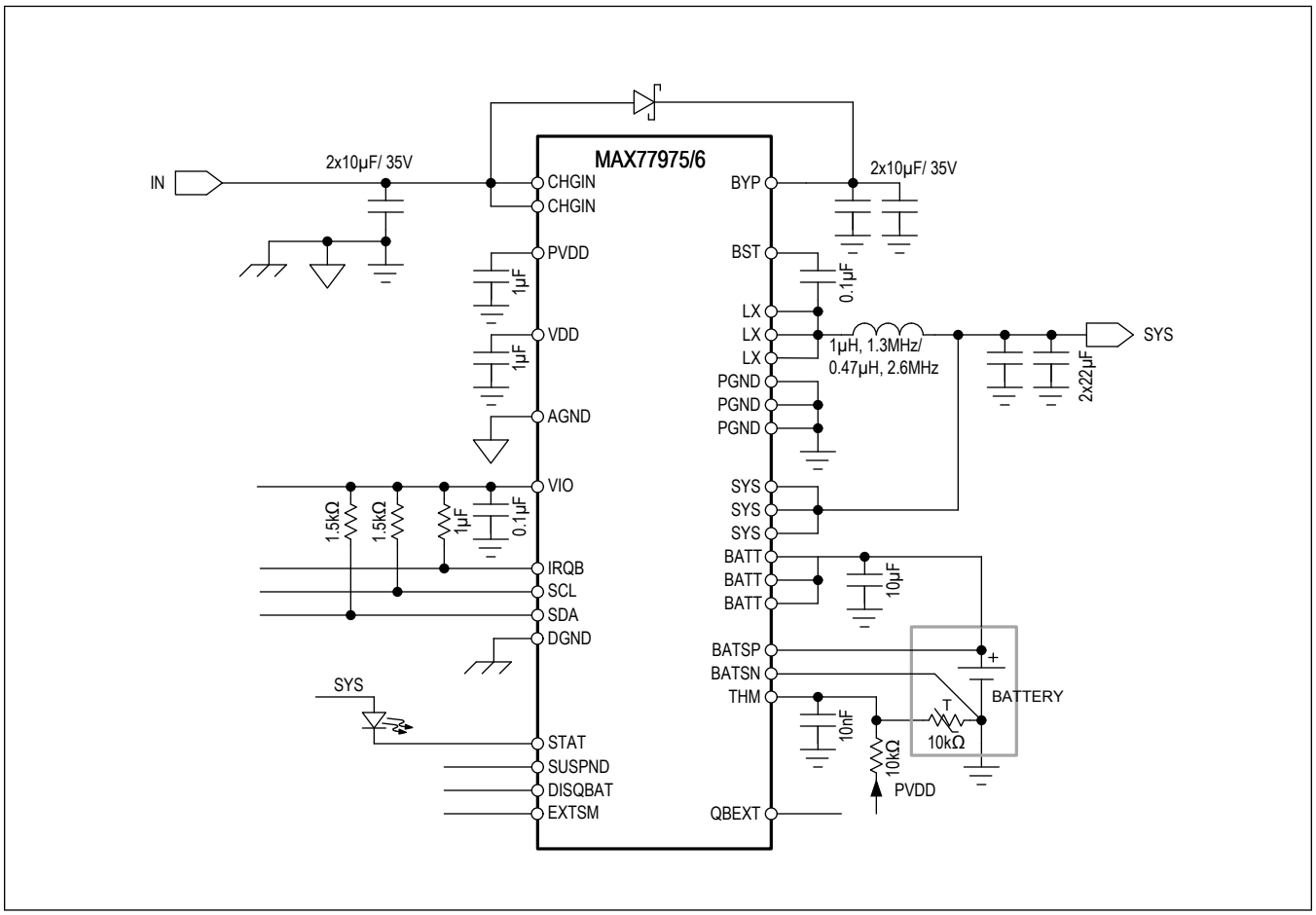
BITFIELD	BITS	DESCRIPTION	DECODE
CHG_CC_WARM	4	JEITA controlled battery fast charge current when thermistor temperature is between T_{WARM} and T_{HOT}.	0x0: Battery fast-charge current is set by CHG_CC. 0x1: Battery fast-charge current is to 50% of CHG_CC.
REGTEMP	3:0	Junction Temperature Thermal Regulation (ºC). The charger's target current limit starts to foldback and the T_{REG} bit is set if the junction temperature is greater than the REGTEMP setpoint.	0x0: 85 0x1: 90 0x2: 95 0x3: 100 0x4: 105 0x5: 110 0x6: 115 0x7: 120 0x8: 125 0x9: 130

STAT_CNFG (0x24)

BIT	7	6	5	4	3	2	1	0
Field	STAT_EN	SPR_6_4[2:0]			STAT_CURR[1:0]		SPR_1	STAT_MODE
Reset	0b1	0b0			0x00		0b0	0b0
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
STAT_EN	7	STAT Charging Status Indication LED Enable Bit	0x0: Disable 0x1: Enable
SPR_6_4	6:4	Spare Bit	
STAT_CURR	3:2	STAT LED Driving Current (mA)	0b00: 5 0b01: 10 0b10: 15 0b11: 20
SPR_1	1	Spare Bit	
STAT_MODE	0	STAT LED Behaviour Selection Bit	0b0: LED mode 1 0b1: LED mode 2

Typical Application Circuits



Note: The Schottky diode between CHGIN and BYP is required when using a fixed voltage adaptor higher than 15V. It is needed for USB Type-C PD high voltage applications in some cases. See the *Design Consideration to Protect Against Hot Plug Event* section for details.

Ordering Information

PART NUMBER	TEMP RANGE	MAX FAST CHARGE CURRENT(A)	BUCK INDUCTOR CURRENT LIMIT (A)	REVERSE BOOST INDUCTOR CURRENT LIMIT (A)	REVERSE BOOST POWER CEILING (W)	PIN-PACKAGE
MAX77975EFD+	-40°C to +85°C	3.5	7	7	12	32 FC2QFN
MAX77975EFD+T	-40°C to +85°C	3.5	7	7	12	32 FC2QFN
MAX77976EFD+	-40°C to +85°C	5.5	9.5	9.5	18	32 FC2QFN
MAX77976EFD+T	-40°C to +85°C	5.5	9.5	9.5	18	32 FC2QFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/20	Initial release	—
1	11/20	Updated *Pin Description* table, *Design Considerations to Protect Against Hot Plug Event* section, *Typical Applications Circuits* section, and *Ordering Information* table	23, 46, 77, 78
2	7/21	Updated *Benefits and Features, Absolute Maximum Ratings, Electrical Characteristics, Pin Description, Functional Diagram, Detailed Description, Battery Differential Voltage Sense,* and *Battery Overcurrent Protection*, removed *Main-Battery Overcurrent Protection Due to Fault* section, updated *External Q_{BATT} Control I/O*, Table 6, added *I^2C Start and Stop Conditions* and *I^2C System Configuration* sections, updated *I^2C Acknowledge, Master Reads after Setting Register Address (Write Register Address and Read Data), Master Reads Register Data Without Setting Register Address (Read Mode),* and *Register Map*	1, 7, 11, 15, 23–26, 36, 37, 43, 45, 47, 48, 53, 56, 61, 66

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