Click here to ask about the production status of specific part numbers.

MAX77827

5.5V Input, 1.8A/3.1A Switch Buck-Boost Converter with 6µA I_Q

General Description

The MAX77827 is a high-efficiency buck-boost regulator targeted for one-cell Li-ion powered applications with the lowest typical quiescent current in the industry of 6µA. It supports input voltages of 1.8V to 5.5V and an output voltage range of 2.3V to 5.3V. The IC provides two different switching current levels (1.8A and 3.1A) to optimize external component sizing based on given load current requirements. With the 1.8A switching current-limit option, the IC can support up to 1.0A load current in buck mode and 900mA in boost mode (V_{IN} = 3.0V, V_{OUT} = 3.3V).

The peak efficiency of 96% makes the IC one of the best solutions as a DC/DC converter to supply a rail for battery-powered portable applications.

The IC features an adjustable output voltage, which can be programmed from 2.3V to 5.3V through a single resistor. Two GPIO pins are available to support force PWM enable function and power-OK (POK) indicator. A unique control algorithm allows high-efficiency, outstanding line/load transient response, and seamless transition between buck and boost modes. These options provide design flexibility that allow the IC to cover a wide range of applications and use cases while minimizing board space.

The MAX77827 is available in a 1.61mm x 2.01mm, 12-bump wafer-level package (WLP), and a 2.5mm x 2.5mm, 14-lead FC2QFN package.

Applications

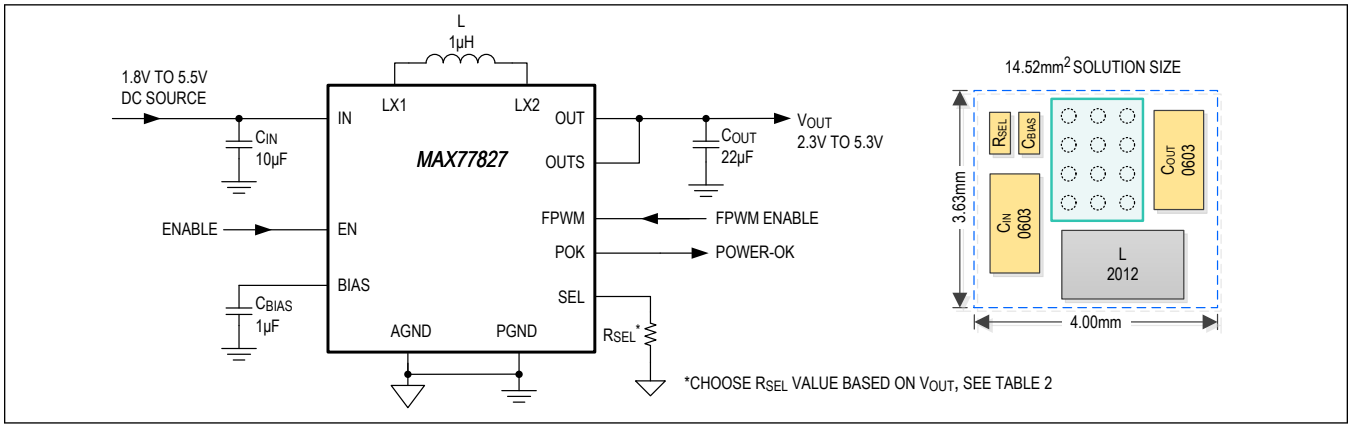
- 1-Cell Li+ Battery Powered Equipment
- Smartphones/Portable/Wearables
- Internet of Things (IoT) Devices
- LPWAN (LTE/NB-IoT, LTE/Cat-M1)

Benefits and Features

- 1.8V to 5.5V Input Voltage Range
- 2.3V to 5.3V Single Resistor Adjustable Output Voltage
- 1.6A Maximum Output Current (3.1A I_{LIM} Option, Buck Mode)
- 900mA Maximum Output Current (1.8A I_{LIM} Option, Boost Mode 3.0V_{IN}, 3.3V_{OUT})
- 96% Peak Efficiency (3.3V_{IN}, 3.3V_{OUT})
- SKIP Mode for Higher Light-Load Efficiency
- 6µA Ultra-Low Typical Quiescent Current (At T_J = +25°C)
- 2.5MHz Nominal Switching Frequency
- Enable Pin
- GPIO Pins for System Design Convenience
  - FPWM (Forced PWM) Mode Selection Pin
  - POK Indicator Pin
- UVLO, Soft-Start, Active-Output Discharge, Overcurrent, and Thermal Shutdown Protections
- 1.61mm x 2.01mm, 12-Bump WLP
- 2.5mm x 2.5mm, 14-Lead FC2QFN

***Ordering Information* appears at end of data sheet.**

Simplified Block Diagram



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Absolute Maximum Ratings

IN, OUT, BIAS to PGND ..... -0.3V to +6V
PGND to AGND ..... -0.3V to +0.3V
EN, SEL, FPWM, POK to AGND ..... -0.3V to V_{BIAS} + 0.3V
FB to AGND ..... -0.3V to V_{OUT} + 0.3V
LX1 to PGND ..... -0.3V to +6.0V
LX2 to PGND ..... -0.3V to +6.0V
IN, LX1, LX2, OUT Continuous RMS current 1.6A
Operating Junction Temperature Range ..... -40°C to +125°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C
Continuous Power Dissipation
WLP Package (T_A = +70°C, derate 13.73mW/°C above +70°C) 1098.4mW
FC2QFN Package (T_A = +70°C, derate 15.77mW/°C above +70°C) 1261.8mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12 WLP

Package Code	W121H2+1
Outline Number	21-100302
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	72.82 C°/W
Junction to Case (θ_{JC})	N/A

14 FC2QFN

Package Code	F142A2F+1
Outline Number	21-100382
Land Pattern Number	90-100127
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	63.4°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = 3.8V, V_{OUT} = 3.3V, typicals are at $T_A \approx T_J$ = +25°C. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Input Voltage Range	V_{IN}	For A and D options	1.8		5.5	V
		For B and C options	2.6		5.5	
Shutdown Supply Current	I_{SHDN}	EN = Low, T_J = +25°C		0.1	2	µA
		EN = Low, T_J = -40°C to +125°C (Note 2)		3	8	
Input Supply Current	I_{Q_SKIP}	SKIP mode, no switching		6	14	µA
	I_{Q_PWM}	FPWM mode, no load, no switching		2	6	mA
Active Discharge Resistance	R_{DISCHG}			100		Ω
Thermal Shutdown	T_{SHDN}	Rising, +20°C hysteresis		165		°C
H-BRIDGE						
Output Voltage Range	V_{OUT}	External resistor programmable	2.3		5.3	V
Output Voltage Accuracy	V_{OUT_ACC1}	PWM mode, T_J = +25°C	-1		+1	%
		PWM mode, T_J = -40°C to +125°C	-2		+2	
	V_{OUT_ACC2}	SKIP mode, no load, T_J = +25°C	-1		+4.5	
Line Regulation		V_{IN} = 1.8V to 5.5V (for A and D options)		0.4		%/V
		V_{IN} = 2.6V to 5.5V (for B and C options)		0.4		
Load Regulation		Note 1		0.25		%/A
Line Transient Response	V_{OS1}/V_{US1}	I_{OUT} = 0.5A, V_{IN} changes from 3.4V to 2.9V in 25µs (20mV/µs), L = 1µH, C_{OUT_NOM} = 8µF (Note 1)		50		mV
Load Transient Response	V_{OS2}/V_{US2}	I_{OUT} changes from 10mA to 0.5A in 15µs, L = 1µH, C_{OUT_NOM} = 8µF (Note 1)		250		mV
LX1/2 Current Limit	I_{LIM_LX}	T_J = -40°C to +125°C, for A and C options	2.5	3.1	3.7	A
		T_J = -40°C to +125°C, for B and D options	1.3	1.8	2.3	
High-Side PMOS On Resistance	R_{DSON_P}	I_{LX} = 100mA per switch	10		130	mΩ
Low-Side NMOS On Resistance	R_{DSON_N}	I_{LX} = 100mA per switch	15		110	mΩ
Switching Frequency	f_{SW}	PWM mode, T_J = +25°C	2.25	2.5	2.75	MHz
		PWM mode, T_J = -40°C to +125°C	2.2	2.5	2.8	
Turn-On Delay Time	t_{ON_DLY}	From EN asserting to SEL detection (Note 2)		100		µs
SEL Detection Time	t_{SEL}	After turn-on delay to LX switching (Note 2)		600		µs

Electrical Characteristics (continued)

(V_{IN} = 3.8V, V_{OUT} = 3.3V, typicals are at $T_A \approx T_J$ = +25°C. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Soft-Start Time	t_{SS}	After SEL detection to soft-start timer finish	I_{OUT} = 10mA (Note 1), for B and D options		1500		µs
			I_{OUT} = 10mA (Note 1), for A and C options		200		
Minimum Effective Output Capacitance	C_{EFF_MIN}	0A < I_{OUT} < 1A			8		µF
LX1, LX2 Leakage Current	I_{LK_85}	$V_{LX1/2}$ = 0V or 5.5V, V_{OUT} = 5.5V, V_{IN} = 5.5V, T_J = +85°C			0.1	2	µA
SYS Undervoltage-Lockout Threshold	V_{UVLO_R}	SYS rising, options B and C		2.4	2.5	2.6	V
		SYS rising, options A and D		1.70	1.75	1.80	
	V_{UVLO_F}	SYS falling, options B and C		1.9	2.05	2.2	
		SYS falling, options A and D		1.62	1.68	1.74	
ENABLE INPUT (EN)							
EN Logic-Low Threshold	V_{EN_L}					0.4	V
EN Logic-High Threshold	V_{EN_H}			1.3			V
FPWM INPUT							
FPWM Logic-Low Threshold	V_{IL}					0.4	V
FPWM Logic-High Threshold	V_{IH}			1.3			V
FPWM Internal Pulldown Resistance	R_{PD}	Pulldown resistor to GND		400	800	1600	kΩ
POK OUTPUT							
POK Output Low Voltage	V_{POK_L}	I_{SINK} = 1mA				0.4	V
POK Output High Leakage	I_{POK_25C}	T_J = +25°C		-1		+1	µA
POK Threshold	I_{POK_R}	V_{OUT} rising, expressed as a percentage of V_{OUT}			92.5		%
	I_{POK_F}	V_{OUT} falling, expressed as a percentage of V_{OUT}			90		

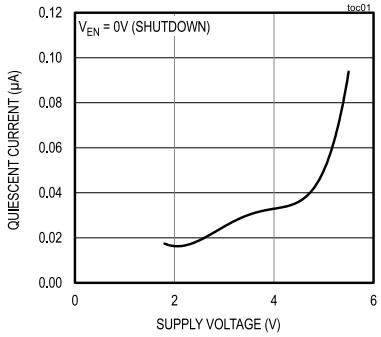
Note 1: Guaranteed by ATE characterization. Not directly tested in production.

Note 2: Guaranteed by design. Production tested through scan.

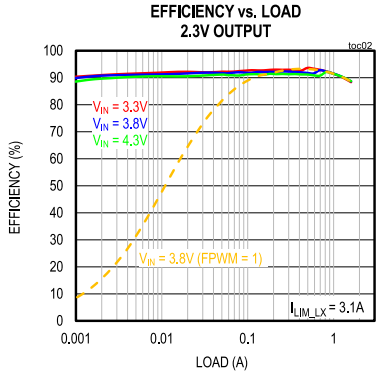
Typical Operating Characteristics

(V_{IN} = 3.8V, V_{OUT} = 3.3V, L = 1µH (Coilcraft XAL4020-102ME), Skip Mode, I_{LIM_LX} = 1.8A, T_A = +25°C, unless otherwise noted.)

SHUTDOWN CURRENT 3.3V OUTPUT



EFFICIENCY vs. LOAD 2.3V OUTPUT



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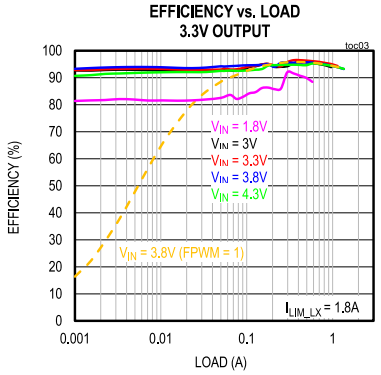
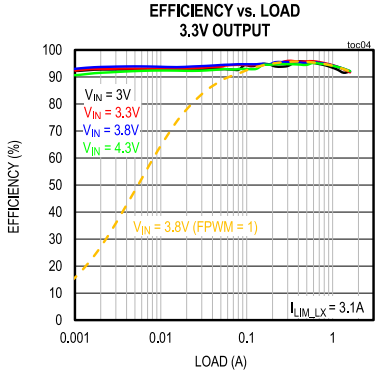
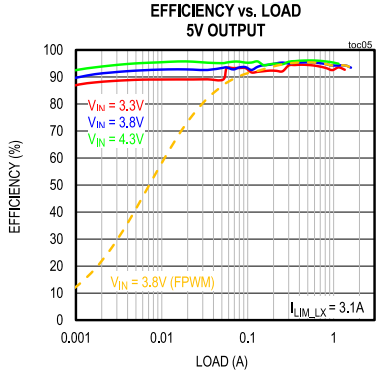


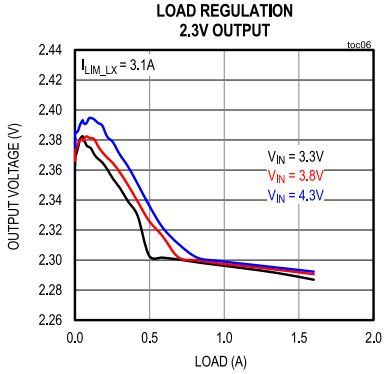
EFFICIENCY vs. LOAD 3.3V OUTPUT



EFFICIENCY vs. LOAD 5V OUTPUT



LOAD REGULATION 2.3V OUTPUT



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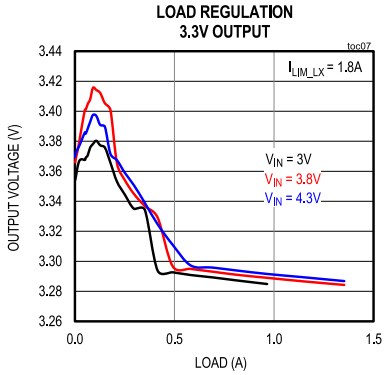

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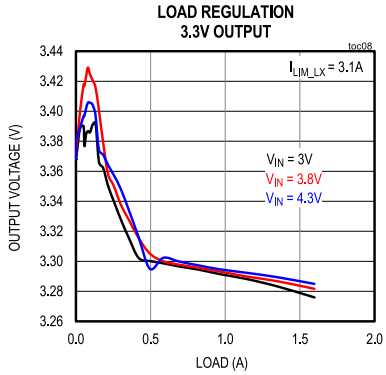

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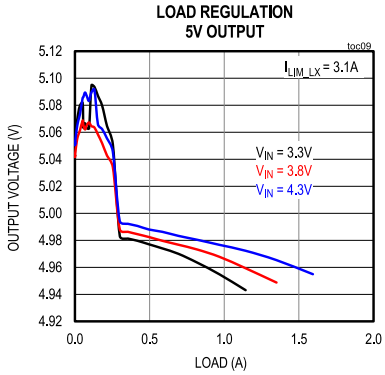
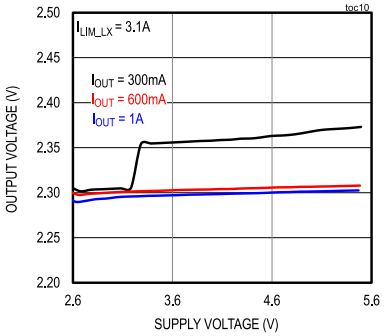


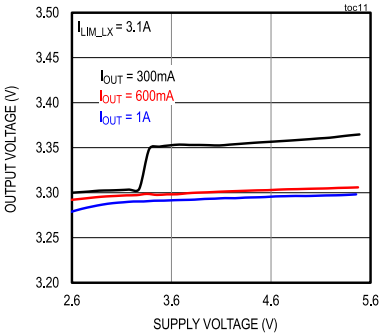
Typical Operating Characteristics (continued)

(V_{IN} = 3.8V, V_{OUT} = 3.3V, L = 1µH (Coilcraft XAL4020-102ME), Skip Mode, I_{LIM_LX} = 1.8A, T_A = +25°C, unless otherwise noted.)

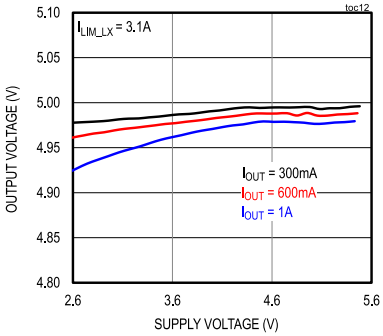
LINE REGULATION
2.3V OUTPUT



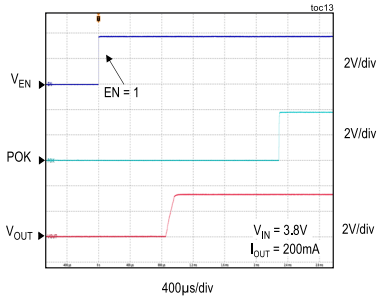
LINE REGULATION
3.3V OUTPUT



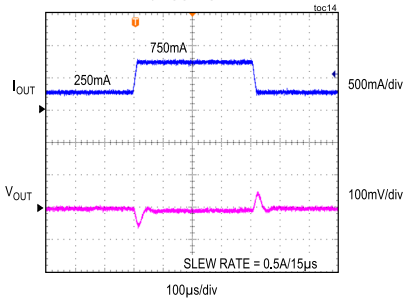
LINE REGULATION
5V OUTPUT



ENABLE STARTUP WAVEFORM
3.3V OUTPUT



LOAD TRANSIENT RESPONSE
2.3V OUTPUT



LOAD TRANSIENT RESPONSE
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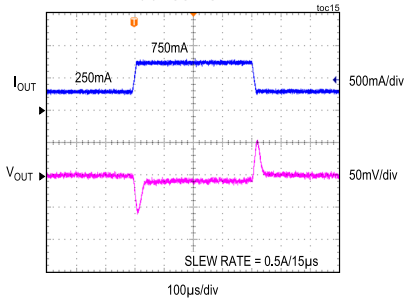

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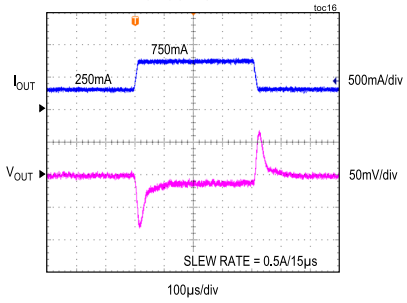
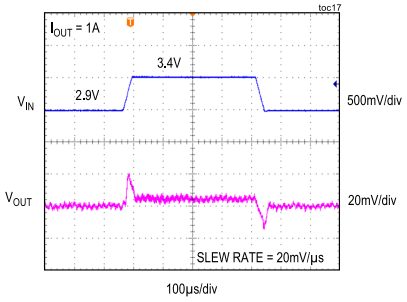
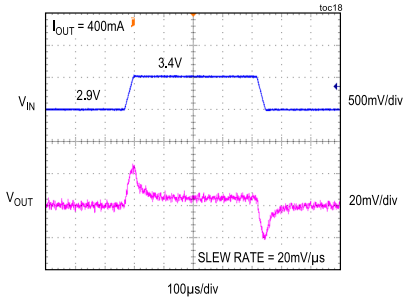


LINE TRANSIENT RESPONSE
2.3V OUTPUT



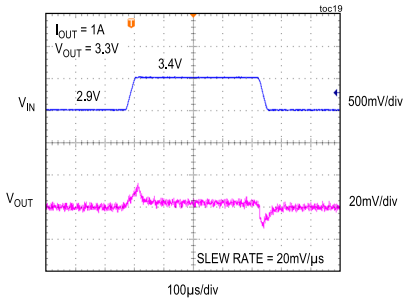
LINE TRANSIENT RESPONSE
5V OUTPUT



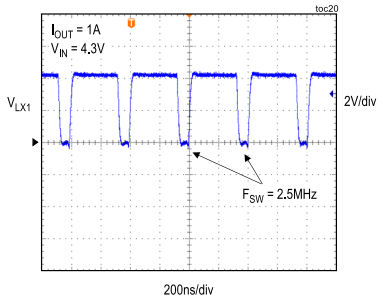
Typical Operating Characteristics (continued)

(V_{IN} = 3.8V, V_{OUT} = 3.3V, L = 1µH (Coilcraft XAL4020-102ME), Skip Mode, I_{LIM_LX} = 1.8A, T_A = +25°C, unless otherwise noted.)

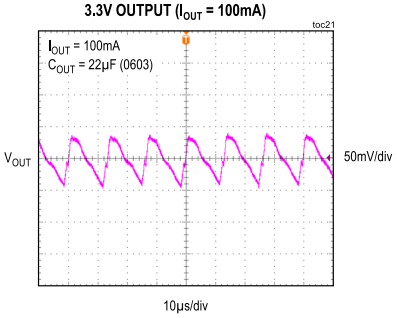
BOOST TO BUCK
LINE TRANSIENT RESPONSE



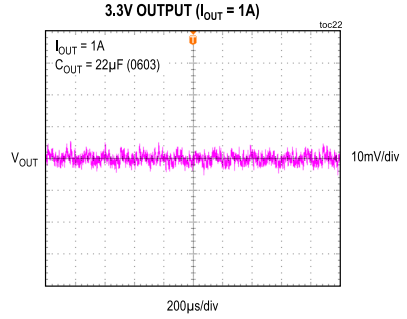
SWITCHING WAVEFORM
3.3V OUTPUT



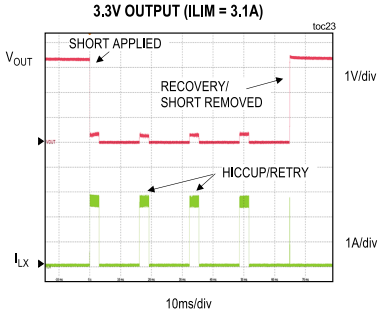
OUTPUT RIPPLE IN SKIP MODE
3.3V OUTPUT (I_{OUT} = 100mA)



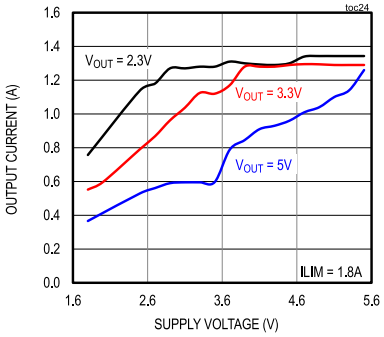
OUTPUT RIPPLE IN PWM
3.3V OUTPUT (I_{OUT} = 1A)



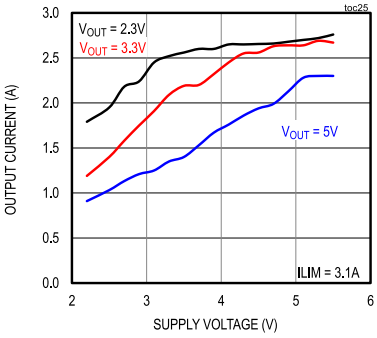
SHORT-CIRCUIT HICCUP AND RECOVERY
3.3V OUTPUT (ILIM = 3.1A)



MAXIMUM OUTPUT CURRENT vs.
SUPPLY VOLTAGE

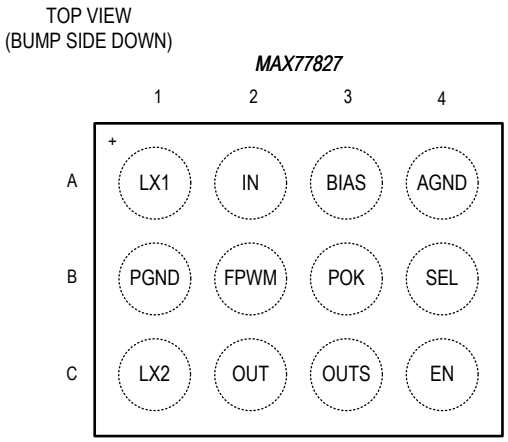


MAXIMUM OUTPUT CURRENT vs.
SUPPLY VOLTAGE



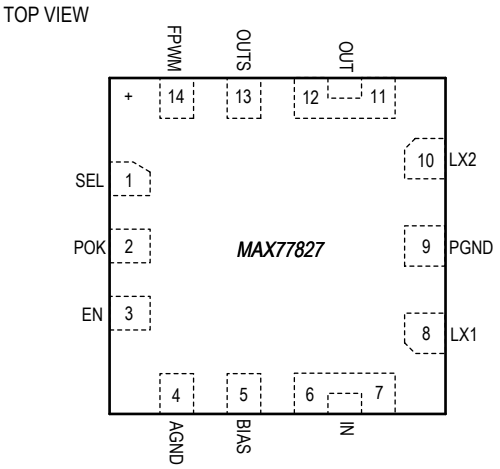
Pin Configurations

12 WLP



12 WLP
(1.61mm x 2.01mm, 0.4mm PITCH)

14 FC2QFN



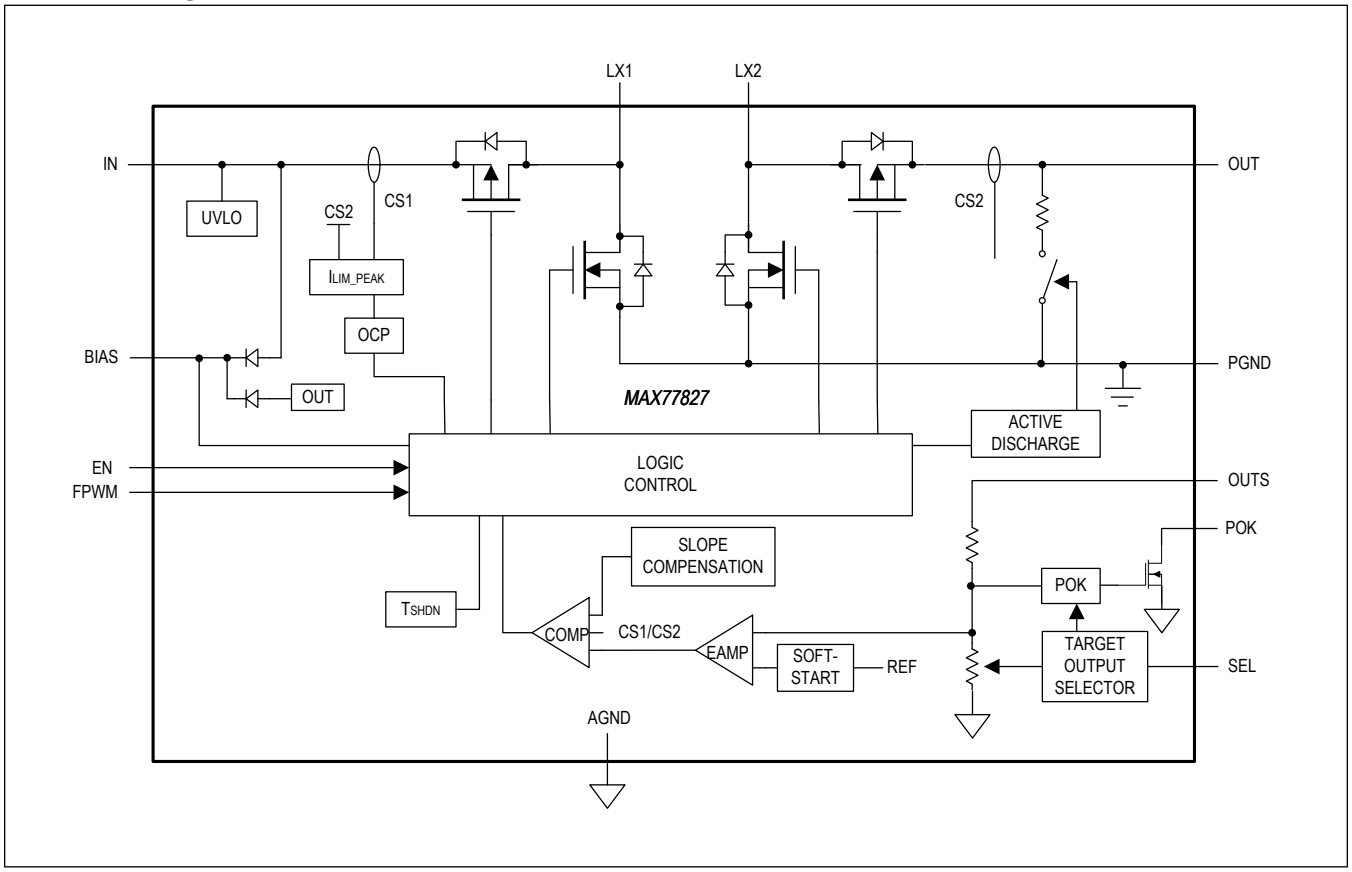
14 FC2QFN
(2.5mm x 2.5mm x 0.55mm PITCH)

Pin Description

PIN		NAME	FUNCTION	TYPE
12 WLP	14 FC2QFN			
A1	8	LX1	Switching Node 1	Power
A2	6, 7	IN	Input. Bypass to PGND with a 10V 10µF capacitor.	Power
A3	5	BIAS	Internal Bias. Bypass to PGND with a 10V 1µF capacitor.	Analog
A4	4	AGND	Analog Ground	Ground
B1	9	PGND	Power Ground	Ground
B2	14	FPWM	FPWM Mode Selection (active-high)	Digital Input
B3	2	POK	Power-OK Open-Drain Output (active-high)	Digital Output
B4	1	SEL	Select the output voltage with resistor (see *Table 2*).	Analog
C1	10	LX2	Switching Node 2	Power
C2	11, 12	OUT	Output. Bypass to PGND with a 10V 22µF capacitor.	Power
C3	13	OUTS	Output Sense	Analog
C4	3	EN	Enable Pin	Digital Input

Functional Diagrams

Function Diagram



Detailed Description

Start Up

When the EN pin is set to high, the IC turns on the internal bias circuitry which takes typically 100µs (t_{ON_DLY}) to settle. After the internal bias circuitry is settled, the controller senses the SEL pin resistance to set the reference voltage. The R_{SEL} reading takes about 600µs (typ). After the IC reads the R_{SEL} value, it begins the soft-start process. During the soft-start process, the IC lowers the I_{LIM} level from normal I_{LIM} level and ramps the output voltage. This prevents the buck-boost from drawing too much current from the input supply during start up. The soft-start process takes 1.5ms (typ) for options B and D, and takes 200µs (typ) for options A and C.

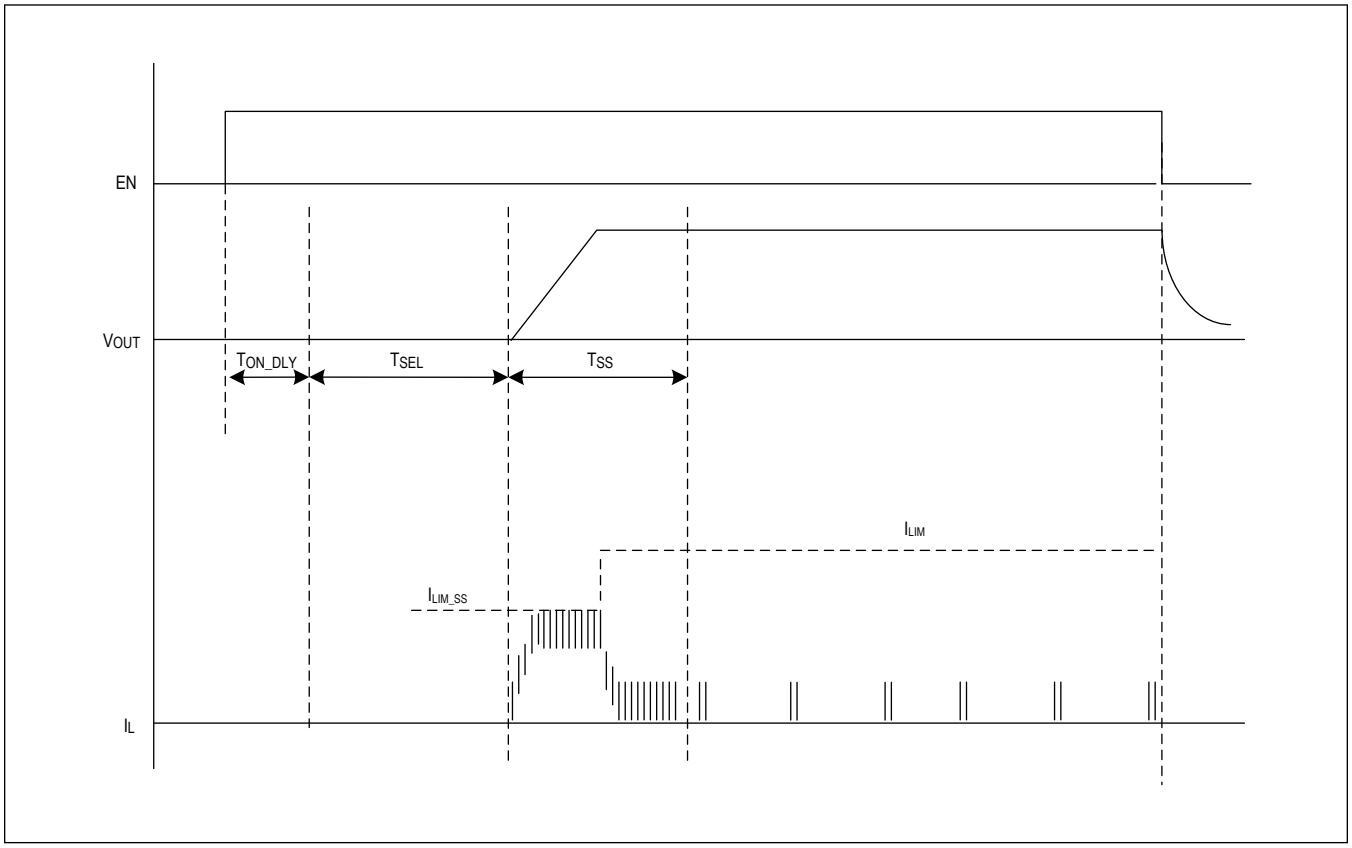


Figure 1. Start-Up Waveform

The buck-boost is in FPWM mode for the entire duration of T_{SS}. Current limit during soft-start (I_{LIM_SS}) increases to I_{LIM} after approximately half of T_{SS}. See Table 1 for a list of parts with their respective soft-start and normal operation I_{LIM} levels.

Table 1. I_{LIM} Levels

PART NUMBER	I_{LIM_SS} (A)	I_{LIM} (A)
MAX77827BEWC+T, MAX77827BEFD+T, MAX77827DEWC+T, MAX77827DEFD+T	1.15	1.8
MAX77827AEWC+T, MAX77827AEFD+T, MAX77827CEWC+T, MAX77827CEFD+T	1.8	3.1

Immediate Shutdown Conditions

The following events immediately shutdown the buck-boost:

- Thermal Protection (T_J > +165°C)
- V_{SYS} < SYS UVLO Falling Threshold (V_{UVLO_F})

The events in this category shutdown the output until fault conditions are removed from the system.

Power Down

When EN pin is set to low, the IC stops switching and turns on the discharge switches until the output is discharged.

Buck-Boost Regulator

The IC buck-boost regulator utilizes a four-switch H-bridge configuration to realize buck and boost operating modes. This topology maintains output voltage regulation when the input voltage is greater than, equal to, or less than the output voltage. The buck-boost is ideal in one-cell Li-ion battery powered applications and two-cell Alkaline battery powered applications, providing 2.3V to 5.3V of output voltage range. High-switching frequency and a unique control algorithm allow for the smallest solution size, low output noise, and the highest-efficiency across a wide input voltage and output current range.

Buck-Boost Control Scheme

The buck-boost converter operates using a 2.5MHz fixed-frequency pulse-width modulated (PWM) control scheme with current-mode compensation. The buck-boost utilizes an H-bridge topology using a single inductor and output capacitor.

The H-bridge topology has three switching phases. See Figure 2 for details.

- Φ1 Switch period (Phase 1: HS1 = ON, LS2 = ON) stores energy in the inductor. Inductor current ramps up at a rate proportional to the input voltage divided by inductance: V_{IN}/L.
- Φ2 Switch period (Phase 2: HS1 = ON, HS2 = ON) ramps inductor current up or down depending on the differential voltage across the inductor: $(V_{IN} – V_{OUT})/L$.
- Φ3 Switch period (Phase 3: LS1 = ON, HS2 = ON) ramps inductor current down at a rate proportional to the output voltage divided by inductance: $(-V_{OUT}/L)$.

Boost operation (V_{IN} < V_{OUT}) utilizes phase 1 and phase 2 within a single clock period. See the representation of inductor current waveform for boost mode operation in Figure 2.

Buck operation (V_{IN} > V_{OUT}) utilizes phase 2 and phase 3 within a single clock period. See the representation of inductor current waveform for buck mode operation in Figure 2.

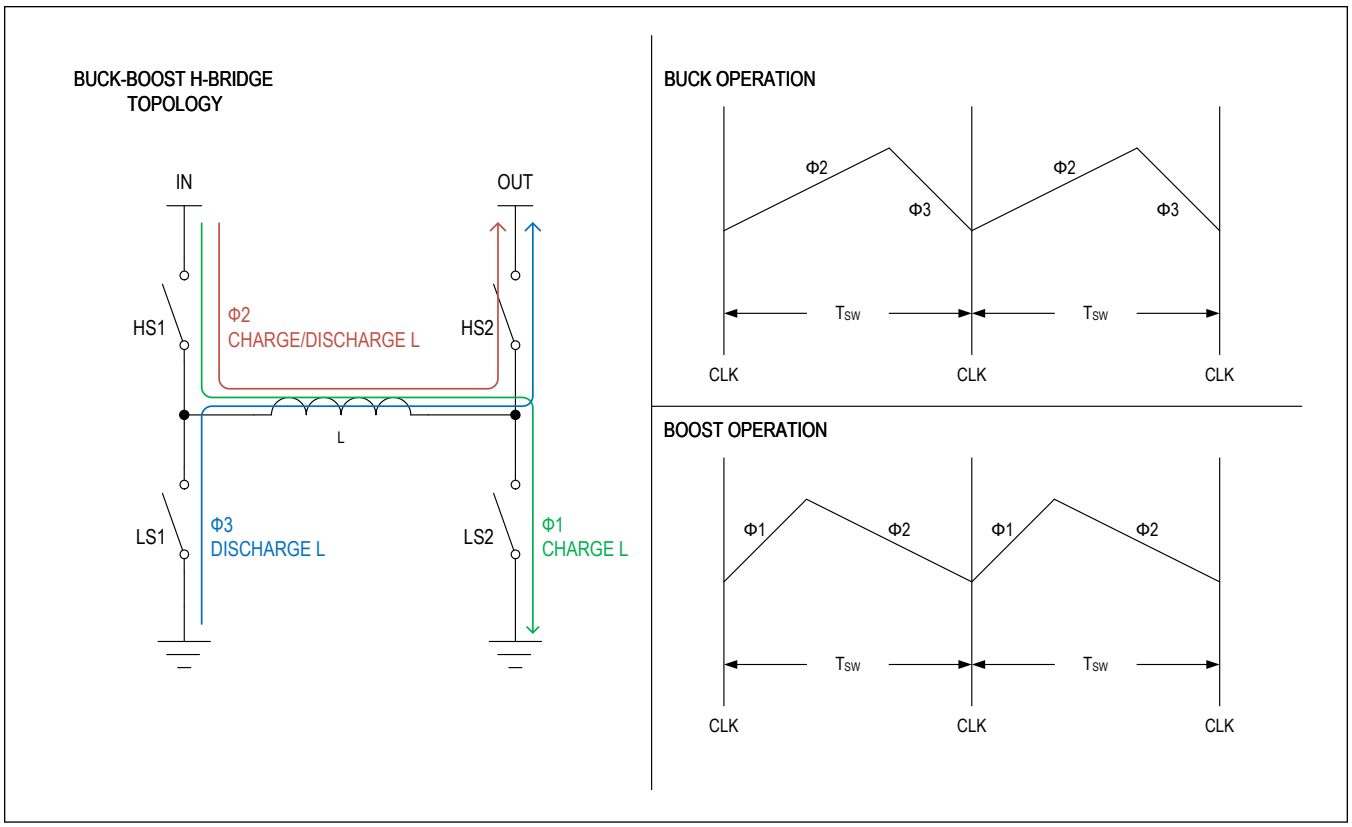


Figure 2. Buck-Boost H-Bridge Topology

Output Voltage Configuration

The IC allows a SEL pin to configure the output voltage. Resistors with 1% tolerance (or better) should be chosen, with nominal values specified in Table 2.

Table 2. R_{SEL} Selection Table

R_{SEL} (kΩ)	V_{OUT} (V)
909	2.3
768	2.4
634	2.5
536	2.6
452	2.7
383	2.8
324	2.8
267	2.85
191	2.9
133	3
113	3
95.3	3.1
80.6	3.15
66.5	3.15

Table 2. R_{SEL} Selection Table (continued)

R_{SEL} (kΩ)	V_{OUT} (V)
56.2	3.2
Open	3.3
Short to GND	3.3
47.5	3.4
40.2	3.45
34	3.5
28	3.6
23.7	3.7
20	3.75
16.9	3.8
14	3.9
11.8	4
10	4.1
8.45	4.2
7.15	4.4
5.9	4.5
4.99	5
226	5.2
162	5.3

FPWM Mode Enable

The IC automatically defaults to SKIP mode operation at no load and light load conditions. Transition from skip mode to PWM occurs when load current increases past a certain threshold. Another way to enable PWM operation is by connecting the FPWM pin to logic HIGH level. This forces PWM mode (FPWM) regardless of load current at the output. FPWM mode benefits applications where the lowest output ripple is required, whereas skip mode helps maximize the buck-boost regulator's efficiency at light loads.

Power-OK (POK) Indicator

The device features an open-drain POK output to monitor the output voltage. The POK pin requires an external pull-up resistor and goes high (high-impedance) after the output increases above 92.5% (typ) of the target output voltage (V_{OUT_TARGET}). The POK pin goes low when the regulator output drops below 90% (typ) of V_{OUT_TARGET}.

Protection Features

Undervoltage Lockout (UVLO)

The device supports a UVLO feature that prevents operation in abnormal input voltage conditions when V_{IN} falls below the $V_{IN\_UVLO\_F}$ threshold. Regardless of the EN pin status, the device disables until the input voltage V_{IN} rises above the $V_{IN\_UVLO\_R}$ threshold.

Soft-Start

The IC is equipped with a soft-start feature to limit large input-current draw from the system supply during device start-up. During the soft-start time, the IC lowers the switching current-limit level from normal level and operates in FPWM mode. See Table 1 for the I_{LIM} levels of each part number.

Output Active Discharge

The buck-boost provides an internal 100Ω switch for output active discharge function. The internal switch provides a path to discharge the energy stored in the output capacitor to PGND whenever the regulator is disabled. While the regulator remains enabled, the internal switch is disconnected from the output.

Overcurrent Protection (OCP)

The device features a robust switching current-limit scheme that protects the device and the inductor during overload and fast transient conditions. The current-sense circuit takes current information from the high-side MOSFETs to determine the peak-switching current ($R_{DS(ON)}$ x I_L).

The IC provides two different cycle-by-cycle current limit levels (1.8A (typ) and 3.1A (typ)) for the high-side MOSFET. If the switching current (I_{LIM}) hits current limit for about 3ms, the IC shuts off the output for about 12ms, retries, and repeats this cycle until the over-current condition is removed from the system.

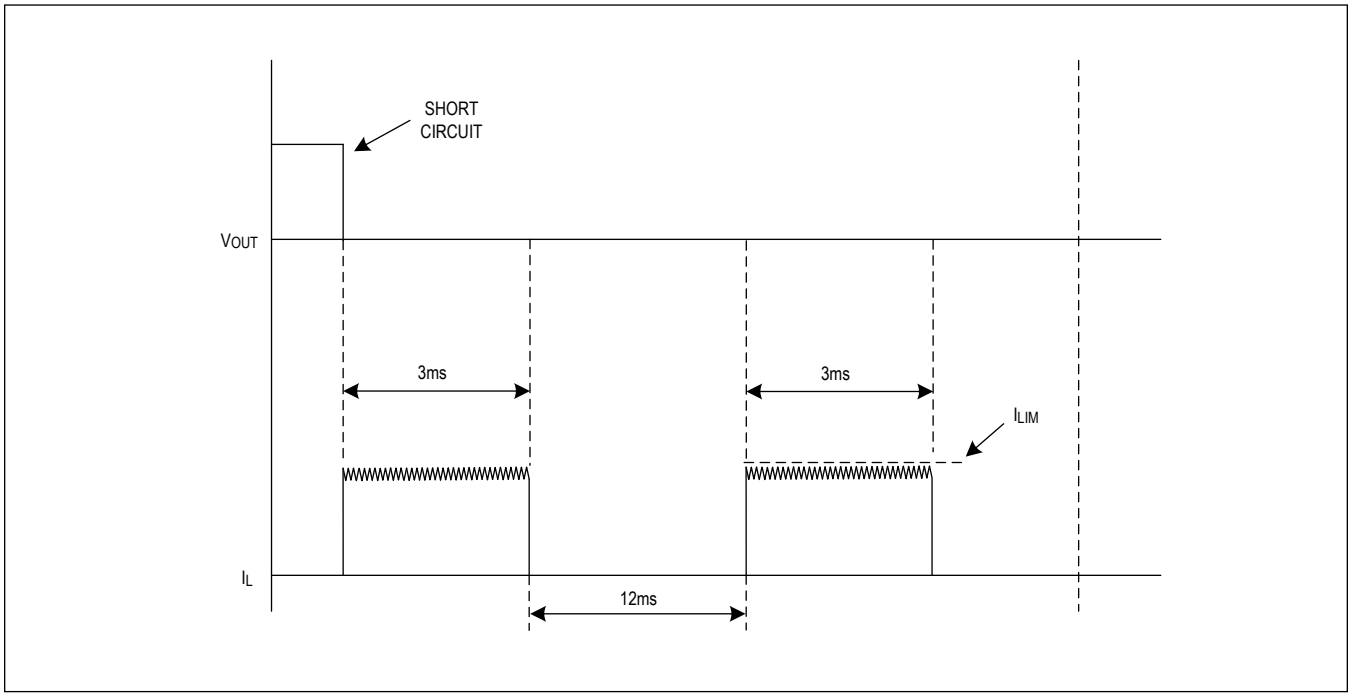


Figure 3. Short-Circuit Waveform

Thermal Shutdown

The device has an internal thermal-protection circuit which monitors die temperature. The buck-boost disables if the die temperature exceeds T_{SHDN} (+165°C typ). The buck-boost enables again after the die temperature cools by approximately +20°C.

Applications Information

Inductor Selection

Buck-boost is optimized for a 1µH inductance. The lower the inductor DCR, the higher the buck-boost efficiency. Users need to trade off inductor size with DCR value and choose a suitable inductor for the buck-boost.

The saturation current of the inductor should be higher than the maximum switching current limit to avoid inductor saturation during operation. See the *Electrical Characteristics* table specifications for the maximum I_{LIM} of each IC option.

Table 3 lists recommended inductors for the IC. Always choose the inductor carefully by consulting the manufacturer's latest released data sheet.

Table 3. Inductor Recommendations

MFGR.	SERIES	NOMINAL INDUCTANCE (µH)	TYPICAL DC RESISTANCE (mΩ)	CURRENT RATING (A) -30 (ΔL/L)	CURRENT RATING (A) ΔT = 40°C RISE	DIMENSIONS L x W x H (mm)	OPTIONS
Murata	DFE18SBN1R0ME0	1.0	120	3.1	2.4	1.6 x 0.8 x 0.8	B, D
Samsung	CIGT201610EH1R0MNE	1.0	38	4.5	4.3	2.0 x 1.6 x 1.0	A, B, C, D
Taiyo-Yuden	MEKK2016H1R0M	1.0	41	4.5	3.7	2.0 x 1.6 x 1.0	A, B, C, D
Cyntec	HTEH20120H-1R0MSR	1.0	45	3.8	3.5	2.0 x 1.2 x 0.8	A, B, C, D
Samsung	CIGT252010EH1R0MNE	1.0	26	5.0	4.3	2.5 x 2.0 x 1.0	A, B, C, D
Sumida	CDMT40D20HF-1R0NC	1.0	26	8.7	9.6	4.3 x 4.3 x 2.1	A, B, C, D
Coilcraft	XAL4020-102MEB	1.0	13	8.7	9.6	4.0 x 4.0 x 2.1	A, B, C, D

Input Capacitor Selection

The input capacitor, C_{IN}, reduces the current peaks drawn from the battery or input power source and reduces switching noise in the device. The impedance of C_{IN} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. For most applications, a 10V 10µF capacitor is sufficient.

Output Capacitor Selection

The output capacitor, C_{OUT}, is required to keep the output-voltage ripple small and to ensure regulation loop stability. C_{OUT} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. For stable operation, the buck-boost requires 8µF of minimum effective output capacitance. Considering DC bias characteristic of ceramic capacitors, a 10V 22µF capacitor is recommended for most applications.

PCB Layout Guidelines

Careful circuit board layout is critical to achieve low switching power losses and clean, stable operation. Figure 5 shows an example PCB layout for the MAX77827 FC2QFN package. For the WLP package, a high density interconnect (HDI) PCB is required. Figure 4 shows an example HDI PCB layout for the MAX77827 WLP package.

When designing the PCB, follow these guidelines:

1. Place the input capacitors C_{IN} and output capacitors C_{OUT} immediately next to the IN pin and OUT pin, respectively, of the IC. Since the IC operates at a high switching frequency, this placement is critical for minimizing parasitic inductance within the input and output current loops, which can cause high voltage spikes and can damage the internal switching MOSFETs.
2. Place the inductor next to the LX bumps/pins (as close as possible) and make the traces between the LX bumps/pins and the inductor short and wide to minimize PCB trace impedance. Excessive PCB impedance reduces converter efficiency. When routing LX traces on a separate layer (as in the examples), make sure to include enough vias to minimize trace impedance. Routing LX traces on multiple layers is recommended to further reduce trace impedance. Furthermore, do not allow LX traces to take up an excessive amount of area. The voltage on this node switches very quickly and additional area creates more radiated emissions.
3. Prioritize the low-impedance ground plane of the PCB directly underneath the IC, C_{OUT}, C_{IN}, and the inductor. Cutting this ground plane risks interrupting the switching current loops.
4. AGND must carefully connect to PGND on the PCBs low-impedance ground plane. Connect AGND to the low-impedance ground plane on the PCB (the same net as PGND) away from any critical loops.
5. The IC requires a supply input (BIAS) which is often the same net as IN. Carefully bypass BIAS to PGND with a dedicated capacitor (C_{BIAS}) as close as possible to the IC. Route a dedicated trace between C_{BIAS} and the BIAS bump/pin. Avoid connecting BIAS directly to the nearest IN bumps/pins without dedicated bypassing.
6. Connect the OUTS bump/pin to the regulating point with a dedicated trace away from noisy nets such as LX1 and LX2.
7. Keep the power traces and load connections short and wide. This is essential for high converter efficiency.
8. Do not neglect ceramic capacitor DC voltage derating. Choose capacitor values and case sizes carefully. See the *Output Capacitor Selection* section and refer to *Tutorial 5527* for more information.

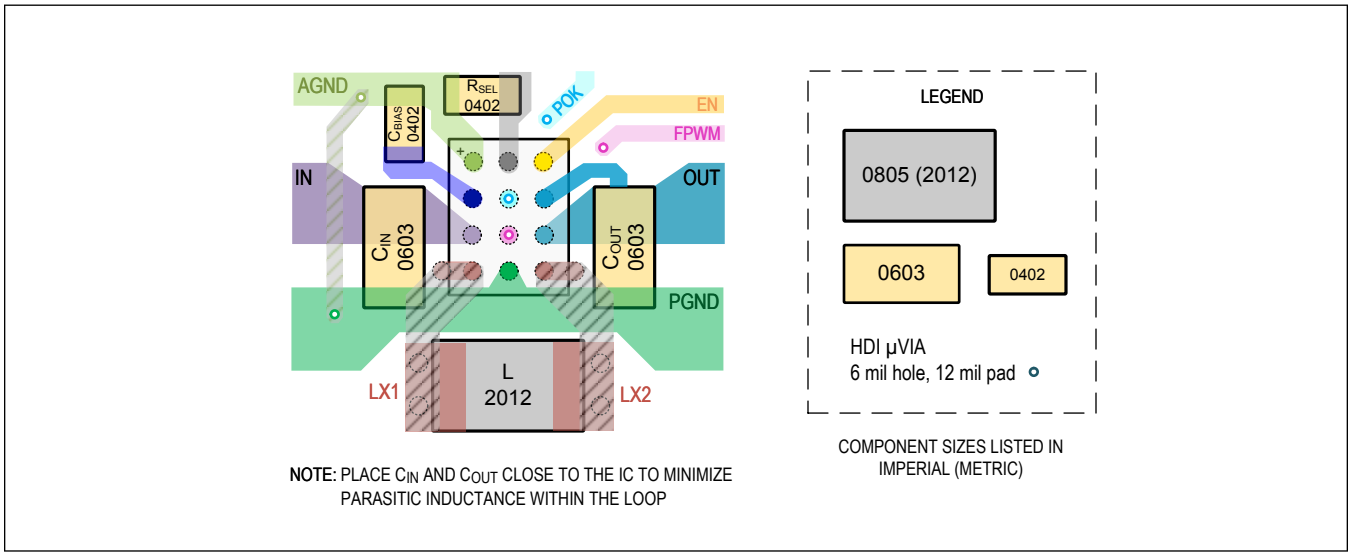


Figure 4. PCB Layout Example (WLP—B and D Options)

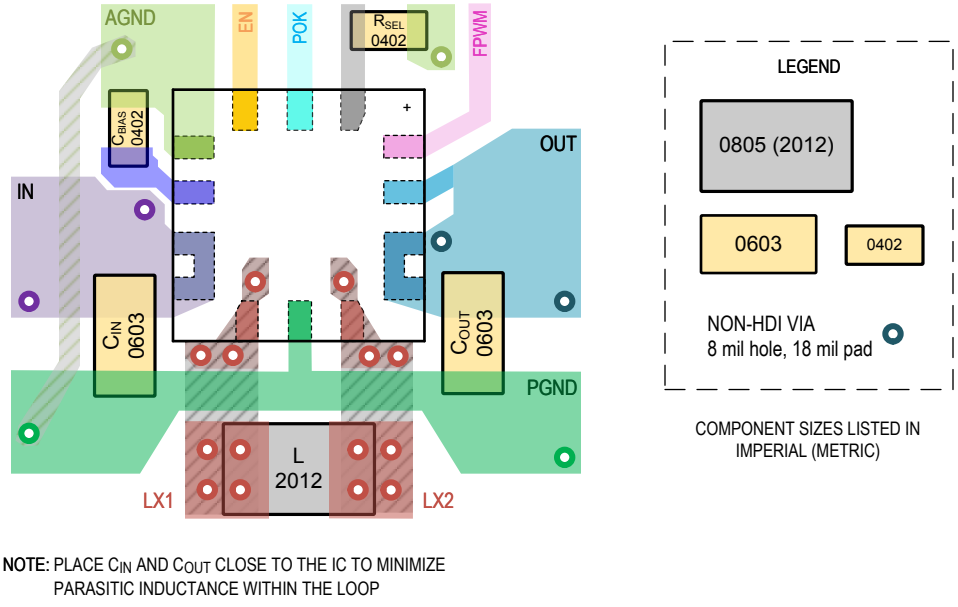
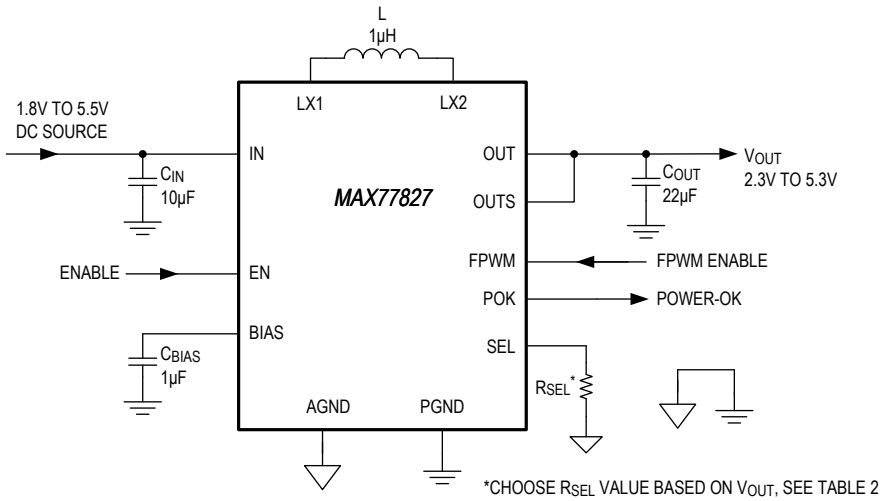


Figure 5. PCB Layout Example (FC2QFN—B and D Options)

Typical Application Circuits

Typical Application Circuit



Ordering Information

PART NUMBER	TYP I_{LIM} (A)	UVLO RISING MAX (V)	PIN-PACKAGE
MAX77827AEWC+T	3.1	1.8	12 WLP
MAX77827BEWC+T	1.8	2.6	12 WLP
MAX77827CEWC+T	3.1	2.6	12 WLP
MAX77827DEWC+T	1.8	1.8	12 WLP
MAX77827AEFD+T	3.1	1.8	14 FC2QFN
MAX77827BEFD+T	1.8	2.6	14 FC2QFN
MAX77827CEFD+T	3.1	2.6	14 FC2QFN
MAX77827DEFD+T	1.8	1.8	14 FC2QFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/19	Initial release	—
1	5/19	Updated Ordering Information table	22
2	6/19	Updated Ordering Information table	22
3	10/19	Updated *General Description*, *Applications*, *Benefits and Features*, and *Package Information* sections, replaced all *Typical Operating Characteristics* and *FC2QFN Pin Configuration*, updated *Pin Description* table, Table 1, Figure 2, and Table 3, replaced *PCB Layout Guidelines* section, updated *Ordering Information* table	1, 6, 9–13, 15, 17, 20–22
4	3/20	Updated *Electrical Characteristics* table, *Start Up* section, Table 1, Table 3, and *Ordering Information* table	7, 8, 15, 20, 23
5	8/21	Updated Table 2	16, 17

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