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MAX77642/MAX77643

Ultra Configurable PMIC Featuring 93% Peak Efficiency Single-Inductor, 3-Output Buck-Boost, 1-LDO for Long Battery Life

General Description

The MAX77642/MAX77643 provide power supply solutions for low-power applications where size and efficiency are critical. The IC features a SIMO buck-boost regulator that provides three independently programmable power rails from a single inductor to minimize total solution size. A 150mA LDO provides ripple rejection for audio and other noise-sensitive applications. The LDO can also be configured as load switches to manage power consumption by disconnecting external blocks when not required.

The MAX77642's SIMO and LDO output voltages are individually programmable through resistors. A peak current limit input is used to set both the inductor's peak current limits of the device with a single resistor. Individual enable pins combined with the flexible resistor programmability allows the device to be tailored for many applications.

This MAX77643's SIMO and LDO output voltages are individually programmable through I²C and in addition, includes two GPIOs with alternate modes for scalability. A bidirectional I²C serial interface allows for configuring and checking the status of the devices. An internal on/off controller provides a controlled startup sequence for the regulators and provides supervisory functionality while they are on. Numerous factory programmable options allow the device to be tailored for many applications, enabling faster time to market.

Applications

- Next Generation Hearables
- Fitness, Health, and Activity Monitors
- Safety and Security Monitors
- Portable Consumer Devices

Benefits and Features

- Highly Integrated
 - 3x Output, Single-Inductor Multiple-Output (SIMO) Buck-Boost Regulator
 - Supports Wide Output Voltage Range from 0.5V to 5.5V for all SIMO Channels
 - 1x 150mA LDO
 - 100mA in LSW mode
 - 2x GPIOs (MAX77643)
 - Watchdog Timer (MAX77643)
- Ultra Low-Power SIMO
 - 5µA Operating Current (3x SIMO Channels + 1x LDOs)
 - 1µA Operating Current per SIMO Channel
 - 0.3µA Shutdown Current
 - 93% Peak Efficiency in Boost-Only Mode
 - 91% Peak Efficiency in Buck-Only Mode
 - Less Than 20mVpp Output Ripple at V_{OUT} = 1.8V
 - Automatic Low-Power Mode to Normal-Power Mode Transition
- Flexible and Configurable
 - Ultra-Configurable Resistor Programmable Output Voltages (MAX77642)
 - I²C-Programmable Output Voltages (MAX77643)
- Small Size
 - 4.24mm² Wafer-Level Package (WLP)
 - 25-Bump, 0.4mm Pitch, 5 x 5 Array

[Ordering Information](#) appears at end of data sheet.

19-100912; Rev 4; 10/21

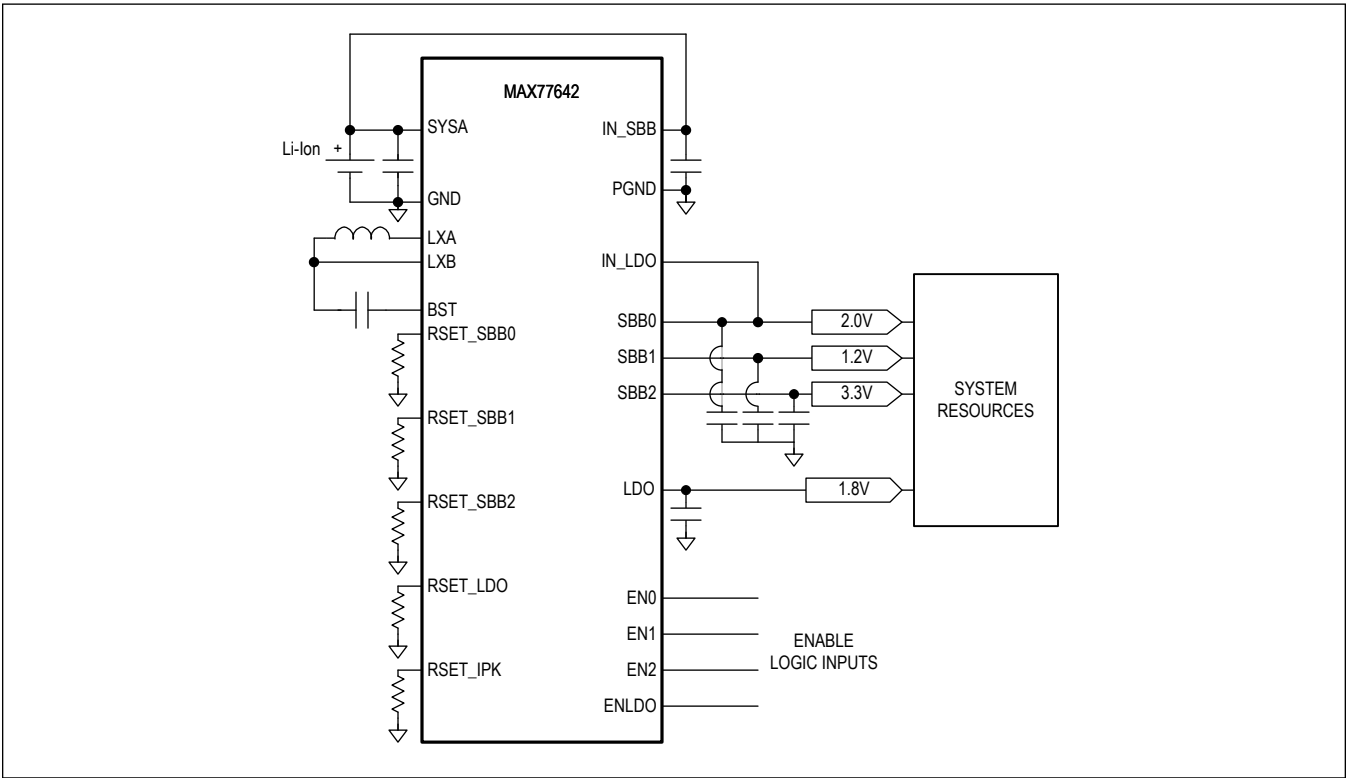
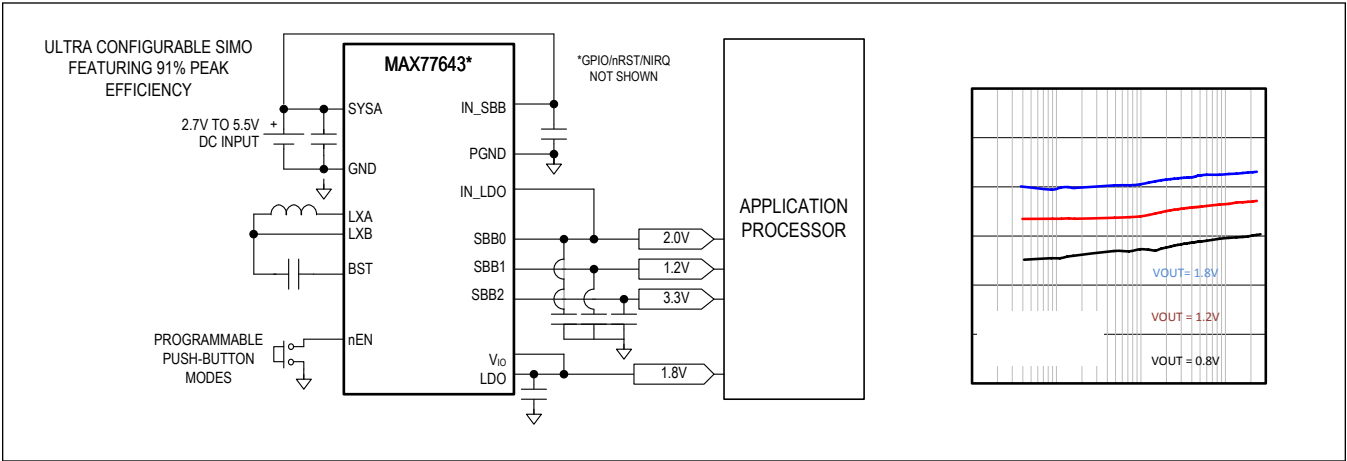
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MAX77642/MAX77643

Ultra Configurable PMIC Featuring 93% Peak Efficiency Single-Inductor, 3-Output Buck-Boost, 1-LDO for Long Battery Life Applications

Simplified Block Diagram



MAX77642/MAX77643

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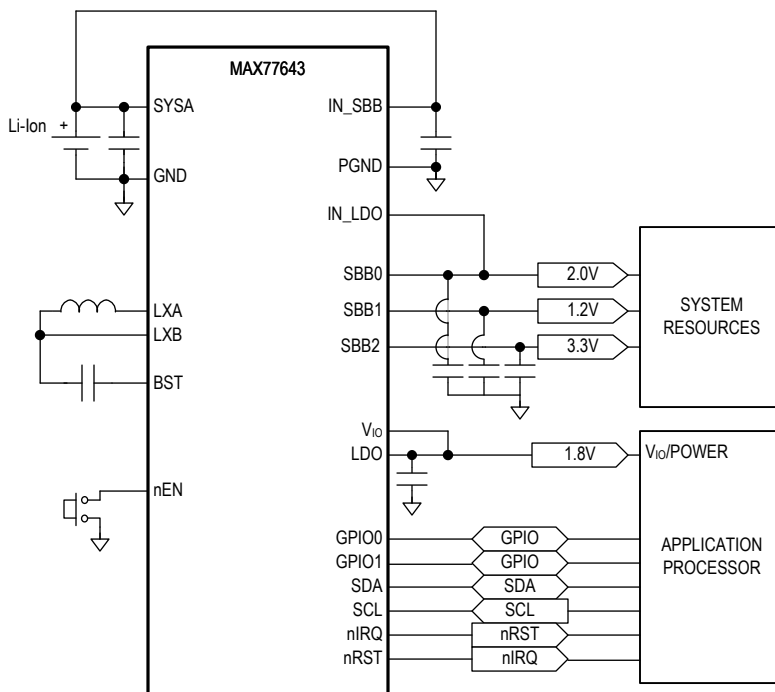


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Absolute Maximum Ratings

nEN, nIRQ, nRST, RSET_SBB0, RSET_SBB1, RSET_SBB2, RSET_LDO, RSET_IPK, EN0, EN1, EN3 to GND -0.3V to $V_{SYSA} + 0.3V$
 SCL, SDA to GND -0.3V to $V_{IO} + 0.3V$
 V_{SYSA} to GND -0.3V to +6.0V
 nIRQ, nRST, SDA, GPIO Continuous Current $\pm 20mA$
 IN_SBB Continuous Current (Note 1) $1.2A_{RMS}$
 IN_SBB to GND -0.3V to +6.0V
 LDO to GND -0.3V to $V_{IN_LDO} + 0.3V$
 IN_LDO to GND -0.3V to $V_{SYSA} + 0.3V$
 LXA Continuous Current (Note 2) $1.2A_{RMS}$
 LXB Continuous Current (Note 2) $1.2A_{RMS}$
 SBB0, SBB1, SBB2 to PGND -0.3V to +6.0V

BST to IN -0.3V to +6.0V
 BST to LXB -0.3V to +6.0V
 SBB0, SBB1, SBB2 Short-Circuit Duration Continuous
 PGND to GND -0.3V to +0.3V
 Operating Temperature Range -40°C to +125°C
 Junction Temperature +150°C
 Storage Temperature Range -65°C to +150°C
 Soldering Temperature (reflow) +260°C
 Continuous Power Dissipation (Multilayer Board, $T_A = +70^\circ C$, derate 20.4mW/°C above +70°C) 1632mW
 GPIO0/1 to GND -0.3V to $V_{IO} + 0.3V$
 SYSA to GND -0.3V to +6.0V
 V_{IO} -0.3V to $V_{SYSA} + 0.3V$

Note 1: Do not repeatedly hot-plug a source to the IN terminal at a rate greater than 10Hz. Hot plugging low impedance sources results in an ~8A momentary (~2μs) current spike.

Note 2: Do not externally bias LXA or LXB. LXA has internal clamping diodes to PGND and IN. LXB has an internal low-side clamping diode to PGND and an internal high-side clamping diode that dynamically connects to a selected SIMO output. It is normal for these diodes to briefly conduct during switching events. When the SIMO regulator is disabled, the LXB to PGND absolute maximum voltage is -0.3V to $V_{SBB0} + 0.3V$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

| | |
|--|--|
| Package Code | N252B2+1 |
| Outline Number | 21-100480 |
| Land Pattern Number | Refer to Application Note 1891 |
| Thermal Resistance, Four-Layer Board: | |
| Junction to Ambient (θ_{JA}) | 49°C/W (2s2p board) |

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

($V_{IN_SBB} = V_{IN_LDO} = V_{SYSA} = 3.7V$, $V_{IO} = 1.8V$, limits are 100% production tested at $T_A = +25^{\circ}C$. Limits over the operating temperature range ($T_A = -40^{\circ}C$ to $+125^{\circ}C$) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|-----------------------------|------------|--|---|-----|-----|-----|---------|
| Operating Voltage Range | V_{IN} | | | 2.7 | | 5.5 | V |
| Shutdown Supply Current | I_{SHDN} | Current measured into IN_SBB and IN_LDO, all resources are off (LDO, SBB0, SBB1, SBB2), $T_A = +25^{\circ}C$ | Main bias is off; this is the standby state | | 0.3 | 1 | μA |
| Main Bias Quiescent Current | I_Q | Main bias is in normal-power mode (CNFG_GLBL.SBIA_LPM = 0) | | | 28 | | μA |
| Quiescent Supply Current | I_Q | Current measured into IN_SBB and IN_LDO. LDO0, SBB0, SBB1, SBB2 are enabled with no load watchdog timer disabled | Main bias is in low-power mode (CNFG_GLBL.SBIA_LPM = 1) | | 4.5 | 11 | μA |

Electrical Characteristics—Global Resources

($V_{IN_SBB} = V_{IN_LDO} = V_{SYSA} = 3.7V$, limits are 100% production tested at $T_A = +25^{\circ}C$, limits over the operating temperature range ($T_A = -40^{\circ}C$ to $+125^{\circ}C$) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---------------------|--|------|------|------|-------------|
| GENERAL CHARACTERISTICS | | | | | | |
| Main Bias Enable Time | t_{SBIA_EN} | | | 0.5 | | ms |
| VOLTAGE MONITORS / POWER-ON RESET (POR) | | | | | | |
| POR Threshold | V_{POR} | V_{SYSA} falling | | 1.55 | | V |
| POR Threshold Hysteresis | | | | 150 | | mV |
| VOLTAGE MONITORS / UNDERVOLTAGE LOCKOUT (UVLO) | | | | | | |
| UVLO Threshold | $V_{SYSAUVLO}$ | V_{SYSA} falling, UVLO_F[3:0] = 0xA (Note 3) | 2.45 | 2.6 | 2.73 | V |
| UVLO Threshold Hysteresis | $V_{SYSAUVLO_HYS}$ | TUVH[3:0] = 0x5 (Note 3) | | 300 | | mV |
| VOLTAGE MONITORS / OVERVOLTAGE LOCKOUT (OVLO) | | | | | | |
| OVLO Threshold | $V_{SYSAOVLO}$ | V_{SYSA} rising | 5.70 | 5.85 | 6.00 | V |
| THERMAL MONITORS | | | | | | |
| Overtemperature Lockout Threshold | T_{OTLO} | T_J rising | | 145 | | $^{\circ}C$ |
| Thermal Alarm Temperature 1 | T_{JAL1} | T_J rising | | 80 | | $^{\circ}C$ |
| Thermal Alarm Temperature 2 | T_{JAL2} | T_J rising | | 100 | | $^{\circ}C$ |

Electrical Characteristics—Global Resources (continued)

($V_{IN_SBB} = V_{IN_LDO} = V_{SYSA} = 3.7V$, limits are 100% production tested at $T_A = +25^\circ C$, limits over the operating temperature range ($T_A = -40^\circ C$ to $+125^\circ C$) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--------------------------------------|-----------------------|---|------------------------|-------|--------|------|-------|
| Thermal Alarm Temperature Hysteresis | | | | 15 | | | °C |
| ENABLE INPUT (nEN, ENx) | | | | | | | |
| nEN Input Leakage Current | I _{nEN_LKG} | V _{nEN} = V _{SYSA} = 5.5V | T _A = +25°C | -1 | ±0.001 | +1 | µA |
| | | | T _A = +85°C | ±0.01 | | | |
| nEN Input Falling Threshold | V _{TH_nEN_F} | nEN Falling | | 0.4 | | | V |
| nEN Input Rising Threshold | V _{TH_nEN_R} | nEN rising | | 1.4 | | | V |
| EN Input Threshold, High | V _{IH} | Voltage threshold, rising | | 1.4 | | | V |
| EN Input Threshold, Low | V _{IL} | Voltage threshold, falling | | 0.4 | | | V |
| Debounce Time | t _{DBNC_nEN} | CNFG_GLBL0.DBEN_nEN = 0 | | 500 | | | µs |
| | | CNFG_GLBL0.DBEN_nEN = 1 | | 30 | | | ms |
| Manual Reset Time | t _{MRST} | CNFG_GLBL0.T_MRST = 1 | | 3 | 4 | 5 | s |
| | | CNFG_GLBL0.T_MRST = 0 | | 7 | 8 | 10.5 | |
| nEN Internal Pullup | R _{nEN-PU} | Pullup to V _{SYSA} | CNFG_GLBL0.PU_DIS = 0 | 200 | | | kΩ |
| | | | CNFG_GLBL0.PU_DIS = 1 | 10000 | | | |
| EN Internal Pulldown | R _{EN-PD} | Pulldown to GND | | 50 | | | nA |
| OPEN-DRAIN INTERRUPT OUTPUT (nIRQ) | | | | | | | |
| Output Voltage Low | V _{OL} | I _{SINK} = 2mA | | 0.4 | | | V |
| Output Falling Edge Time | t _{f_nIRQ} | C _{IRQ} = 25pF | | 2 | | | ns |
| Leakage Current | I _{nIRQ_LKG} | V _{SYSA} = V _{IO} = 5.5V nIRQ is high impedance (no interrupts) V _{nIRQ} = 0V and 5.5V | T _A = +25°C | -1 | ±0.001 | +1 | µA |
| | | | T _A = +85°C | ±0.01 | | | |
| OPEN-DRAIN RESET OUTPUT (nRST) | | | | | | | |
| Output Voltage Low | V _{OL} | I _{SINK} = 2mA | | 0.4 | | | V |
| Output Falling Edge Time | t _{f_nRST} | C _{RST} = 25pF | | 2 | | | ns |
| nRST Deassert Delay Time | t _{RSTODD} | See Figure 11 for more information | | 5.12 | | | ms |
| nRST Assert Delay Time | t _{RSTOAD} | | | 10.24 | | | ms |

Electrical Characteristics—Global Resources (continued)

($V_{IN_SBB} = V_{IN_LDO} = V_{SYS} = 3.7V$, limits are 100% production tested at $T_A = +25^\circ C$, limits over the operating temperature range ($T_A = -40^\circ C$ to $+125^\circ C$) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|-------------------------------------|-----------------------|--|---|----------------------------|--------|-----|-------|
| Leakage Current | I _{nRST_LKG} | V _{SYSA} = V _{IO} = 5.5V nRST is high impedance (no reset) V _{nRST} = 0V and 5.5V | T _A = +25°C | -1 | ±0.001 | +1 | µA |
| | | V _{SYS} = V _{IO} = 5.5V nRST is high impedance (no reset) V _{nRST} = 0V and 5.5V | T _A = +85°C | | ±0.01 | | |
| GENERAL PURPOSE INPUT/OUTPUT (GPIO) | | | | | | | |
| GPIO Supply Voltage Range | | | | V _{IO} | | | V |
| Input Voltage Low | V _{IL} | V _{IO} = 1.8V | | 0.3 x V _{IO} | | | V |
| Input Voltage High | V _{IH} | V _{IO} = 1.8V | | 0.7 x V _{IO} | | | V |
| Input Leakage Current | I _{GPI_LKG} | CNFG_GPIOx.DIR = 1 V _{IO} = 5.5V V _{GPIO} = 0V and 5.5V | T _A = +25°C | -1 | ±0.001 | +1 | µA |
| | | | T _A = +85°C | ±0.01 | | | |
| Output Voltage Low | V _{OL} | I _{SINK} = 2mA | | 0.4 | | | V |
| Output Voltage High | V _{OH} | I _{SOURCE} = 1mA | | 0.8 x V _{IO} | | | V |
| Input Debounce Time | t _{DBNC_GPI} | CNFG_GPIOx.DBEN_GPI = 1 | | 30 | | | ms |
| Output Falling Edge Time | t _{f_GPIO} | C _{GPIO} = 25pF | | 3 | | | ns |
| Output Rising Edge Time | t _{r_GPIO} | C _{GPIO} = 25pF | | 3 | | | ns |
| FLEXIBLE POWER SEQUENCER | | | | | | | |
| FPS Startup Delay | t _{FPS_DLY} | | | 1.43 | | | ms |
| Power-Up Event Periods | t _{EN} | See Figure 10 | | 1.28 | | | ms |
| Power-Down Event Periods | t _{DIS} | See Figure 10 | | 2.56 | | | ms |
| RSET (MAX77642) | | | | | | | |
| Select Resistor Detection Time | t _{RSET} | Total time to detect all five resistors | V _{IN_SBB} = 2.7V, C _{RSET} < 2pF | 3 | | | ms |
| Required Select Resistor Accuracy | R _{SEL_TOL} | Use the nearest ±1% resistor from the R _{SEL} Selection Table. | | -1 +1 | | | % |

Note 3: Programmed at Maxim's factory.

Electrical Characteristics—SIMO Buck-Boost

($V_{IN_SBB} = V_{IN_LDO} = V_{SYS} = 3.7V$, $C_{SBBx} = 10\mu F$, $L = 1.5\mu H$, limits are 100% production tested at $T_A = +25^\circ C$, limits over the operating temperature range ($T_A = -40^\circ C$ to $+125^\circ C$) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--------------|--|---------------------------------------|------|-----------|------------|
| GENERAL CHARACTERISTICS / OUTPUT VOLTAGE RANGE (SBB0) | | | | | | |
| Programmable Output Voltage Range | | | 0.5 | | 5.5 | V |
| Output DAC Bits | | | | 8 | | bits |
| Output DAC LSB Size | | 0.5V to 5.5V | | 25 | | mV |
| GENERAL CHARACTERISTICS / OUTPUT VOLTAGE RANGE (SBB1) | | | | | | |
| Programmable Output Voltage Range | | | 0.5 | | 5.5 | V |
| Output DAC Bits | | | | 8 | | bits |
| Output DAC LSB Size | | 0.5V to 5.5V | | 25 | | mV |
| GENERAL CHARACTERISTICS / OUTPUT VOLTAGE RANGE (SBB2) | | | | | | |
| Programmable Output Voltage Range | | | 0.5 | | 5.5 | V |
| Output DAC Bits | | | | 8 | | bits |
| Output DAC LSB Size | | 0.5V to 5.5V | | 25 | | mV |
| OUTPUT VOLTAGE ACCURACY | | | | | | |
| Output Voltage Accuracy | | V_{SBBx} falling, threshold where LXA switches high. Specified as a percentage of target output voltage. | $T_A = -40^\circ C$ to $+125^\circ C$ | -2.0 | +2.0 | % |
| OUT Over-Regulation Threshold | V_{OV} | $T_A = +25^\circ C$ | | 1.7 | 3.3 | % |
| TIMING CHARACTERISTICS | | | | | | |
| Enable Delay | | Delay time from the SIMO receiving its first enable signal to when it begins to switch in order to service that output | | 10 | | μs |
| Soft-Start Slew Rate | dV/dt_{SS} | $I_{PK} = 1A$, $C_{OUT} = 10\mu F$ | | 5.0 | | $mV/\mu s$ |
| POWER STAGE CHARACTERISTICS | | | | | | |
| LXA Leakage Current | | SBB0, SBB1, SBB2 are disabled, $V_{IN_SBB} = 5.5V$, $V_{LXA} = 0V$, or $5.5V$ | $T_A = +25^\circ C$ | -1.0 | ± 0.1 | μA |
| | | | $T_A = +85^\circ C$ | | ± 1.0 | |
| LXB Leakage Current | | SBB0, SBB1, SBB2 are disabled, $V_{IN_SBB} = 5.5V$, $V_{LXA} = 0V$ or $5.5V$, all $V_{SBBx} = 5.5V$ | $T_A = +25^\circ C$ | -1.0 | ± 0.1 | μA |
| | | | $T_A = +85^\circ C$ | | ± 1.0 | |
| BST Leakage Current | | $V_{IN_SBB} = 5.5V$, $V_{LXB} = 5.5V$, $V_{BST} = 11V$ | $T_A = +25^\circ C$ | | +0.01 | μA |
| | | | $T_A = +85^\circ C$ | | +0.1 | |

Electrical Characteristics—SIMO Buck-Boost (continued)

($V_{IN_SBB} = V_{IN_LDO} = V_{SYS} = 3.7V$, $C_{SBBx} = 10\mu F$, $L = 1.5\mu H$, limits are 100% production tested at $T_A = +25^\circ C$, limits over the operating temperature range ($T_A = -40^\circ C$ to $+125^\circ C$) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|-----------------------|--|---------------------|-------|------|----------|
| Disabled Output Leakage Current | | SBB0, SBB1, SBB2 are disabled, active-discharge disabled (CNFG_SBBx_B.ADE_SBBx = 0), $V_{SBBx} = 5.5V$, $V_{LXB} = 0V$, $V_{SYS} = V_{IN_SBB} = V_{BST} = 5.5V$ | $T_A = +25^\circ C$ | +0.1 | +1.0 | μA |
| | | | $T_A = +85^\circ C$ | +0.2 | | |
| Active Discharge Resistance | R_{AD_SBBx} | SBB0, SBB1, SBB2 are disabled, active discharge enabled (CNFG_SBBx_B.ADE_SBBx = 1) | 60 | 120 | 180 | Ω |
| CONTROL SCHEME | | | | | | |
| Peak Current Limit | I_{P_SBB} (Note 4) | CNFG_SBBx_B.IP_SBBx[1:0] = 0b11 | -18% | 0.335 | +18% | A |
| | | CNFG_SBBx_B.IP_SBBx[1:0] = 0b10 | -14% | 0.500 | +14% | |
| | | CNFG_SBBx_B.IP_SBBx[1:0] = 0b01 | -8% | 0.750 | +8% | |
| | | CNFG_SBBx_B.IP_SBBx[1:0] = 0b00 | -7% | 1.000 | +7% | |

Note 4: Typical values align with bench observations using the stated conditions with an inductor. Minimum and maximum values are tested in production with DC currents without an inductor. See the *Typical Operating Characteristics* SIMO switching waveforms to gain more insight on this specification.

Electrical Characteristics—Low Dropout Linear Regulator (LDO)/Load Switch (LSW)

($V_{IN_SBB} = V_{IN_LDO} = V_{SYS} = 3.7V$, limits are 100% production tested at $T_A = +25^\circ C$, limits over the operating temperature range ($T_A = -40^\circ C$ to $+125^\circ C$) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|--------------------|--|------|-----|-------|---------|
| LDO | | | | | | |
| Input Voltage Range | V_{IN_LDO} | LDO mode | 1.71 | | 5.5 | V |
| | | Switch mode | 1.2 | | 5.5 | |
| Quiescent Supply Current | I_{IN_LDO} | $I_{OUT_LDOx} = 0$ | | 1.4 | 2.4 | μA |
| | | $I_{OUT_LDOx} = 0$, switch mode | | 0.5 | 1.2 | |
| Quiescent Supply Current In Dropout | $I_{IN_DRP_LDO}$ | $I_{OUT_LDOx} = 0$, $V_{IN_LDOx} = 2.9V$, $V_{LDOx} = 3V$ | | 2.1 | 4.6 | μA |
| Maximum Output Current | I_{OUT_LDO} | $V_{IN_LDOx} > 1.8V$ | 150 | | | mA |
| | | $V_{IN_LDOx} = 1.8V$ or lower | 100 | | | |
| Output Voltage (MAX77642) | V_{OUT_LDO} | | 0.5 | | 3.975 | V |
| Output Voltage (MAX77643) | V_{OUT_LDO} | | 0.5 | | 5.0 | V |
| Output Accuracy | | $V_{IN_LDOx} = (V_{OUT_LDOx} + 0.5V)$ or higher, $I_{OUT_LDOx} = 1mA$ | -3.1 | | +3.1 | % |
| Dropout Voltage | V_{DRP_LDO} | $V_{IN_LDOx} = 3V$, LDOx programmed to 3V, $I_{OUT_LDOx} = 100mA$ | | | 100 | mV |

Electrical Characteristics—Low Dropout Linear Regulator (LDO)/Load Switch (LSW) (continued)

($V_{IN_SBB} = V_{IN_LDO} = V_{SYS} = 3.7V$, limits are 100% production tested at $T_A = +25^{\circ}C$, limits over the operating temperature range ($T_A = -40^{\circ}C$ to $+125^{\circ}C$) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------------|---------------|--|------|----------|-------|---------------|
| Line Regulation | | $V_{IN_LDOx} = (V_{OUT_LDOx} + 0.5V)$ to 5.5V | -0.5 | | +0.5 | %/V |
| Load Regulation | | $V_{IN_LDOx} = 1.8V$ or higher, $I_{OUT_LDOx} = 100\mu A$ to 100mA | | 0.001 | 0.005 | %/mA |
| Line Transient | | $V_{IN_LDOx} = 4V$ to 5V, 5 μs rise time | | ± 35 | | mV |
| Load Transient | | $I_{OUT_LDOx} = 100\mu A$ to 10mA, 200ns rise time | | 100 | | mV |
| | | $I_{OUT_LDOx} = 100\mu A$ to 100mA, 200ns rise time | | 200 | | |
| Active Discharge Resistance | R_{AD_LDO} | | 42 | 80 | 200 | Ω |
| Switch Mode On-Resistance | R_{ON_LDO} | $V_{IN_LDOx} = 2.7V$, $I_{OUT_LDOx} = 100mA$ | | | 0.5 | Ω |
| | | $V_{IN_LDOx} = 1.8V$, $I_{OUT_LDOx} = 50mA$ | | | 0.8 | |
| | | $V_{IN_LDOx} = 1.2V$, $I_{OUT_LDOx} = 5mA$ | | | 1.2 | |
| Slew Rate | | $I_{OUT_LDO} = 0mA$, time from 10% to 90% of final register value, $C_{OUT_LDO} = 1\mu F$ | | 2.2 | | V/ms |
| | | $I_{OUT_LDO} = 0mA$, time from 10% to 90% of final register value, $C_{OUT_LDO} = 1\mu F$, switch mode | | 2.2 | | |
| Short Circuit Current Limit | | $V_{IN_LDOx} = 2.7V$, $V_{OUT_LDOx} = GND$ | 230 | 550 | 880 | mA |
| | | $V_{IN_LDOx} = 2.7V$, $V_{OUT_LDOx} = 2.55V$, switch mode | 230 | 550 | | |
| Output Noise | | 10Hz to 100kHz, $V_{IN_LDOx} = 5V$, $V_{OUT_LDOx} = 3.3V$ | | 150 | | μV_{RMS} |
| | | 10Hz to 100kHz, $V_{IN_LDOx} = 5V$, $V_{OUT_LDOx} = 2.5V$ | | 125 | | |
| | | 10Hz to 100kHz, $V_{IN_LDOx} = 5V$, $V_{OUT_LDOx} = 1.2V$ | | 90 | | |
| | | 10Hz to 100kHz, $V_{IN_LDOx} = 5V$, $V_{OUT_LDOx} = 0.9V$ | | 80 | | |
| Output DAC Bits | | | | 8 | | bits |
| Output DAC LSB Size | | | | 25 | | mV |

Electrical Characteristics—I²C Serial Communication

($V_{IN} = 3.7V$, $V_{IO} = 1.8V$, limits are 100% production tested at $T_A = +25^{\circ}C$, limits over the operating temperature range ($T_A = -40^{\circ}C$ to $+125^{\circ}C$) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|----------|--|-----|-----|-----|---------|
| POWER SUPPLY | | | | | | |
| V_{IO} Voltage Range | V_{IO} | | 1.7 | 1.8 | 3.6 | V |
| V_{IO} Bias Current | | $V_{IO} = 3.6V$, $V_{SDA} = V_{SCL} = 0V$ or 3.6V, $T_A = +25^{\circ}C$ | -1 | 0 | +1 | μA |
| | | $V_{IO} = 1.7V$, $V_{SDA} = V_{SCL} = 0V$ or 1.7V | -1 | 0 | +1 | |

Electrical Characteristics—I²C Serial Communication (continued)

($V_{IN} = 3.7V$, $V_{IO} = 1.8V$, limits are 100% production tested at $T_A = +25^\circ C$, limits over the operating temperature range ($T_A = -40^\circ C$ to $+125^\circ C$) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-------------------|---|----------------------|-----|------|---------|
| SDA AND SCL I/O STAGE | | | | | | |
| SCL, SDA Input High Voltage | V_{IH} | $V_{IO} = 1.7V$ to $3.6V$ | $0.7 \times V_{IO}$ | | | V |
| SCL, SDA Input Low Voltage | V_{IL} | $V_{IO} = 1.7V$ to $3.6V$ | $0.3 \times V_{IO}$ | | | V |
| SCL, SDA Input Hysteresis | V_{HYS} | | $0.05 \times V_{IO}$ | | | V |
| SCL, SDA Input Leakage Current | I_I | $V_{IO} = 3.6V$, $V_{SCL} = V_{SDA} = 0V$ and $3.6V$ | -10 | | +10 | μA |
| SDA Output Low Voltage | V_{OL} | Sinking 20mA | | | 0.4 | V |
| SCL, SDA Pin Capacitance | C_I | | | 10 | | pF |
| Output Fall Time from V_{IH} to V_{IL} | t_{OF} (Note 5) | | | | 120 | ns |
| I²C COMPATIBLE INTERFACE TIMING (STANDARD, FAST AND FAST MODE PLUS) (Note 5) | | | | | | |
| Clock Frequency | f_{SCL} | | 0 | | 1000 | kHz |
| Hold Time (REPEATED) START Condition | t_{HD_STA} | | 0.26 | | | μs |
| SCL Low Period | t_{LOW} | | 0.5 | | | μs |
| SCL High Period | t_{HIGH} | | 0.26 | | | μs |
| Setup Time REPEATED START Condition | t_{SU_STA} | | 0.26 | | | μs |
| Data Hold Time | t_{HD_DAT} | | 0 | | | μs |
| Data Setup Time | t_{SU_DAT} | | 50 | | | ns |
| Setup Time for STOP Condition | t_{SU_STO} | | 0.26 | | | μs |
| Bus Free Time between STOP and START Condition | t_{BUF} | | 0.5 | | | μs |
| Pulse Width of Suppressed Spikes | t_{SP} | Maximum pulse width of spikes that must be suppressed by the input filter | | 50 | | ns |
| I²C COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, $C_B = 100pF$) (Note 5) | | | | | | |
| Clock Frequency | f_{SCL} | | | | 3.4 | MHz |
| Setup Time REPEATED START Condition | t_{SU_STA} | | 160 | | | ns |
| Hold Time (REPEATED) START Condition | t_{HD_STA} | | 160 | | | ns |
| SCL Low Period | t_{LOW} | | 160 | | | ns |
| SCL High Period | t_{HIGH} | | 60 | | | ns |
| Data Setup Time | t_{SU_DAT} | | 10 | | | ns |
| Data Hold Time | t_{HD_DAT} | | 0 | | 70 | ns |
| SCL Rise Time | t_{rCL} | $T_A = +25^\circ C$ | 10 | | 40 | ns |

Electrical Characteristics—I²C Serial Communication (continued)

($V_{IN} = 3.7V$, $V_{IO} = 1.8V$, limits are 100% production tested at $T_A = +25^\circ C$, limits over the operating temperature range ($T_A = -40^\circ C$ to $+125^\circ C$) are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------------|---|-----|-----|-----|-------|
| Rise Time of SCL Signal After REPEATED START Condition and After Acknowledge Bit | t_{rCL1} | $T_A = +25^\circ C$ | 10 | | 80 | ns |
| SCL Fall Time | t_{fCL} | $T_A = +25^\circ C$ | 10 | | 40 | ns |
| SDA Rise Time | t_{rDA} | $T_A = +25^\circ C$ | 10 | | 80 | ns |
| SDA Fall Time | t_{fDA} | $T_A = +25^\circ C$ | 10 | | 80 | ns |
| Setup Time for STOP Condition | t_{SU_STO} | | 160 | | | ns |
| Bus Capacitance | C_B | | | | 100 | pF |
| Pulse Width of Suppressed Spikes | t_{SP} | Maximum pulse width of spikes that must be suppressed by the input filter | | 10 | | ns |
| I²C COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, $C_B = 400pF$) (Note 5) | | | | | | |
| Clock Frequency | f_{SCL} | | | | 1.7 | MHz |
| Setup Time REPEATED START Condition | t_{SU_STA} | | 160 | | | ns |
| Hold Time (REPEATED) START Condition | t_{HD_STA} | | 160 | | | ns |
| SCL Low Period | t_{LOW} | | 320 | | | ns |
| SCL High Period | t_{HIGH} | | 120 | | | ns |
| Data Setup Time | t_{SU_DAT} | | 10 | | | ns |
| Data Hold Time | t_{HD_DAT} | | 0 | | 150 | ns |
| SCL Rise Time | t_{rCL} | $T_A = +25^\circ C$ | 20 | | 80 | ns |
| Rise Time of SCL Signal After REPEATED START Condition and After Acknowledge Bit | t_{rCL1} | $T_A = +25^\circ C$ | 20 | | 80 | ns |
| SCL Fall Time | t_{fCL} | $T_A = +25^\circ C$ | 20 | | 80 | ns |
| SDA Rise Time | t_{rDA} | $T_A = +25^\circ C$ | 20 | | 160 | ns |
| SDA Fall Time | t_{fDA} | $T_A = +25^\circ C$ | 20 | | 160 | ns |
| Setup Time for STOP Condition | t_{SU_STO} | | 160 | | | ns |
| Bus Capacitance | C_B | | | | 400 | pF |
| Pulse Width of Suppressed Spikes | t_{SP} | Maximum pulse width of spikes that must be suppressed by the input filter | | 10 | | ns |

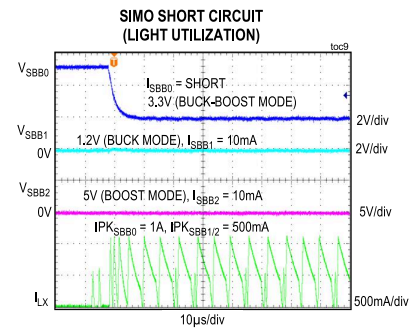
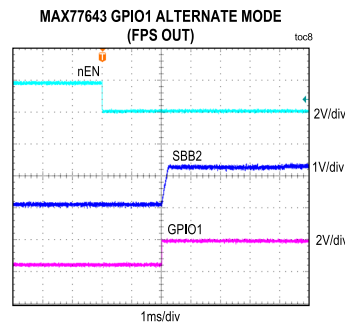
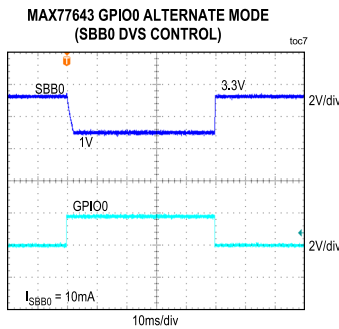
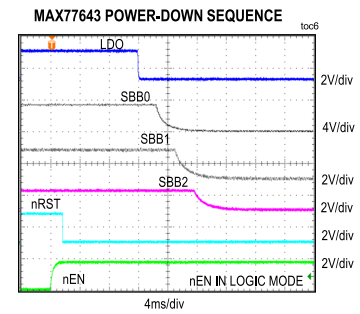
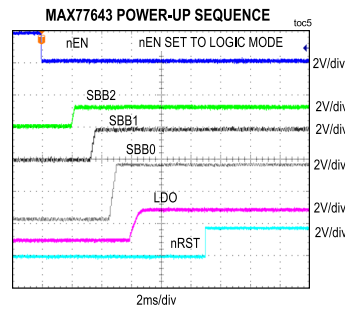
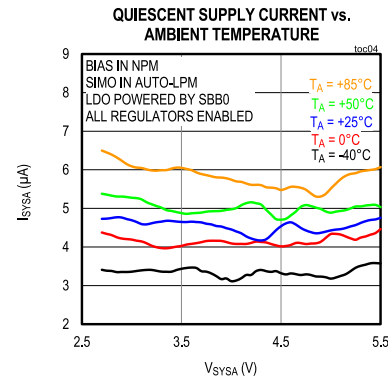
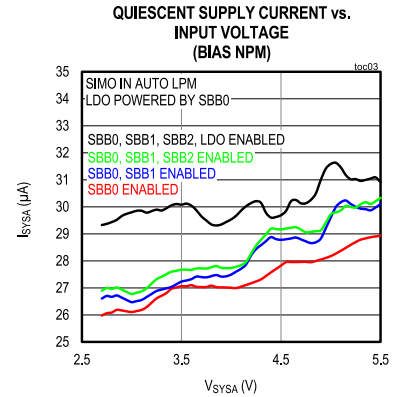
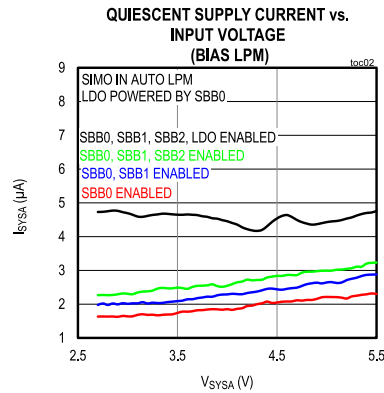
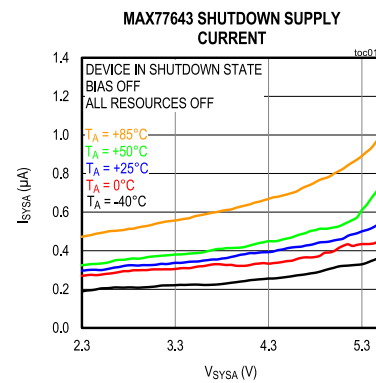
Note 5: Design guidance only. Not production tested.

MAX77642/MAX77643

Ultra Configurable PMIC Featuring 93% Peak Efficiency Single-Inductor, 3-Output Buck-Boost, 1-LDO for Long Battery Life Applications

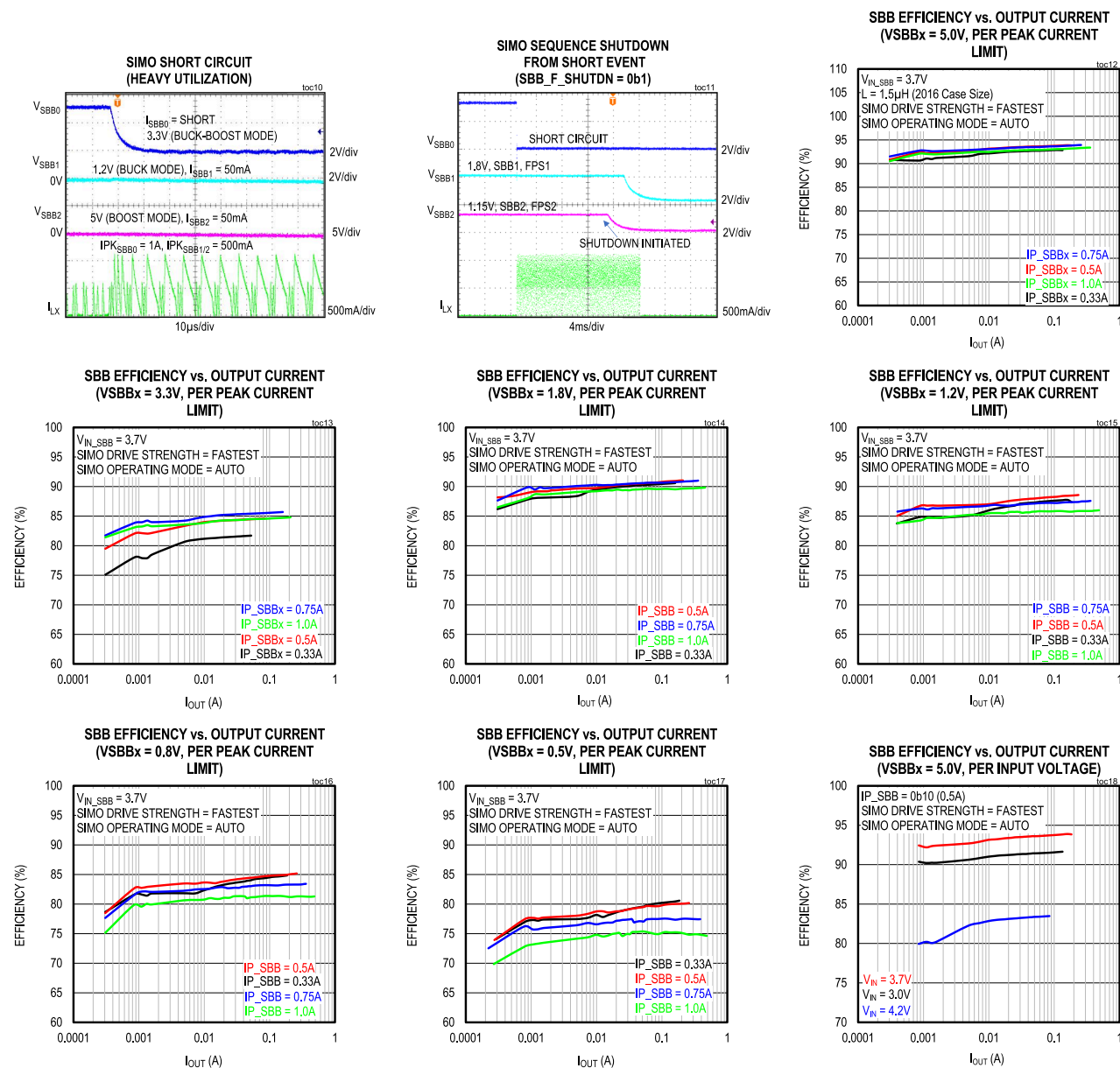
Typical Operating Characteristics

(Typical Applications Circuit. $V_{SYSA} = 3.7V$, $V_{IO} = 1.8V$, $T_A = +25^\circ C$, unless otherwise noted. Inductor = DFE201612E-1R5M, 1.5 μH , 72m Ω)



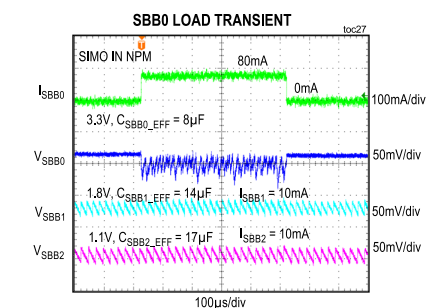
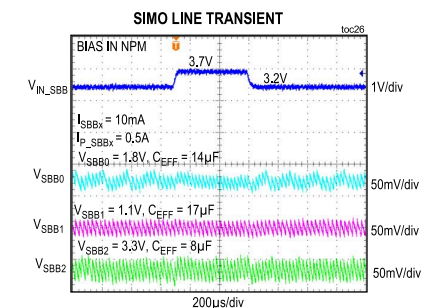
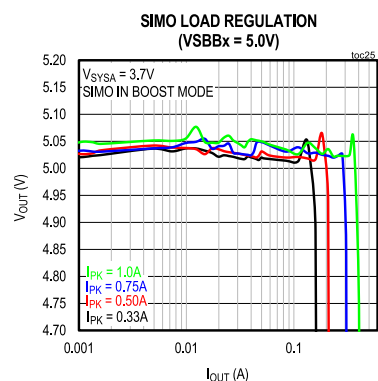
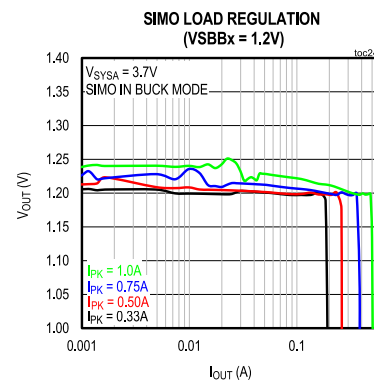
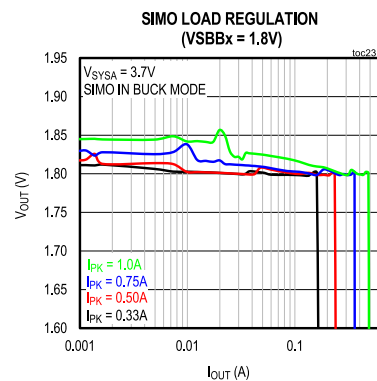
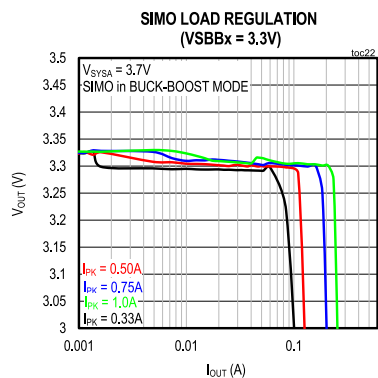
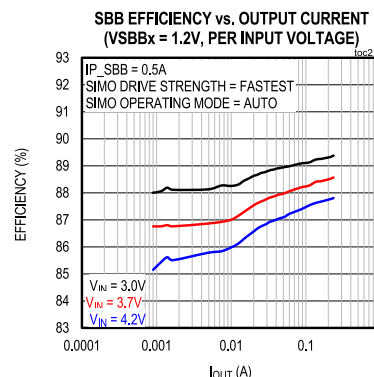
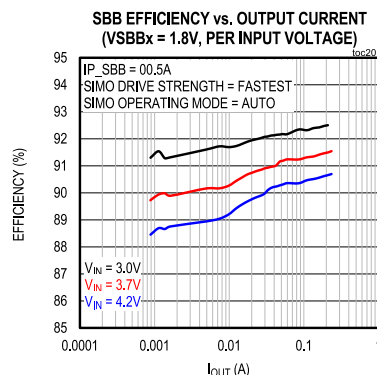
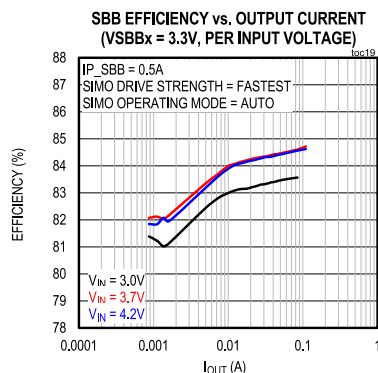
Typical Operating Characteristics (continued)

(Typical Applications Circuit. $V_{SYS} = 3.7V$, $V_{IO} = 1.8V$, $T_A = +25^\circ C$, unless otherwise noted. Inductor = DFE201612E-1R5M, $1.5\mu H$, $72m\Omega$)



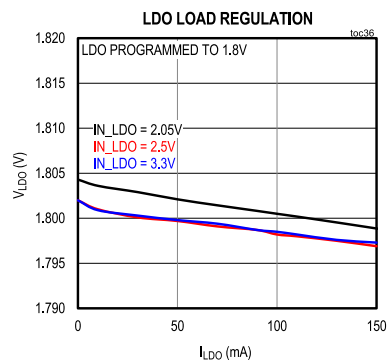
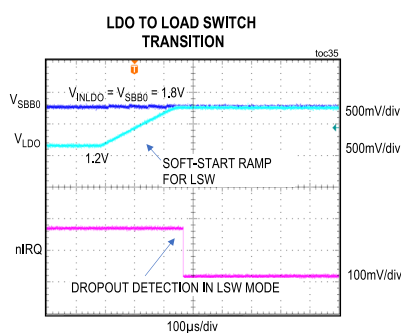
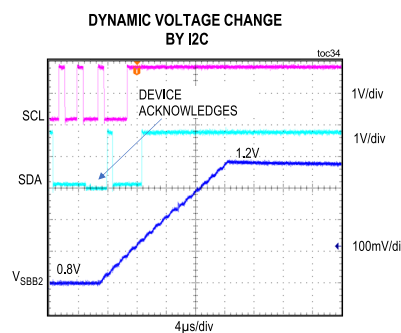
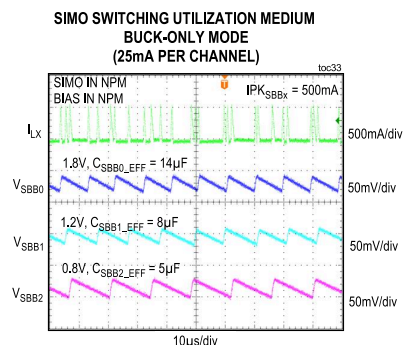
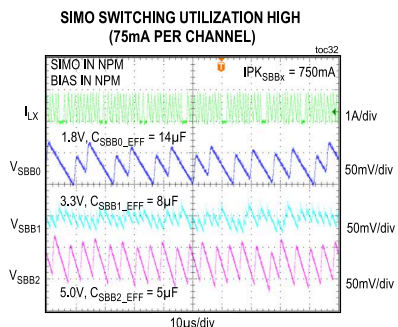
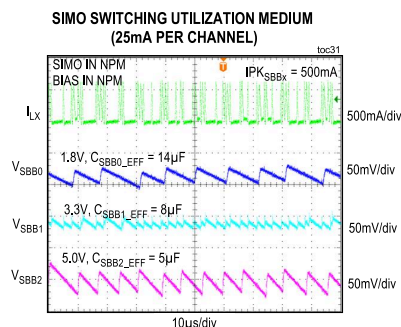
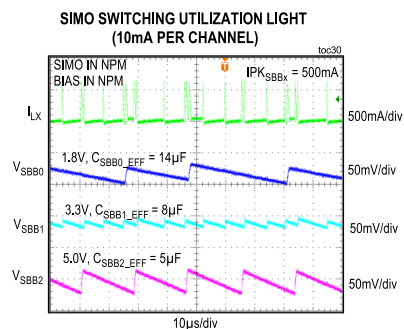
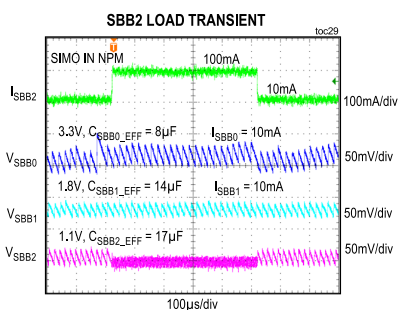
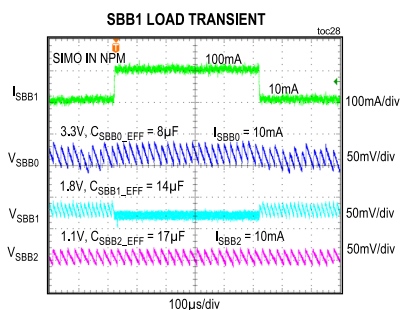
Typical Operating Characteristics (continued)

(Typical Applications Circuit. $V_{SYSA} = 3.7V$, $V_{IO} = 1.8V$, $T_A = +25^\circ C$, unless otherwise noted. Inductor = DFE201612E-1R5M, $1.5\mu H$, $72m\Omega$)



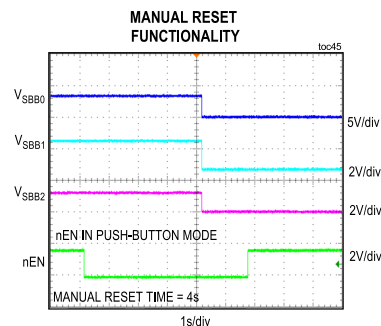
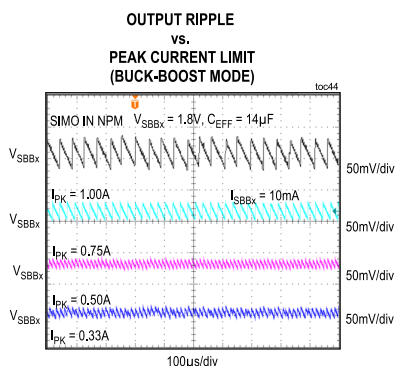
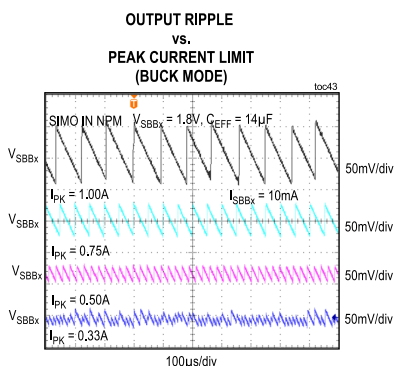
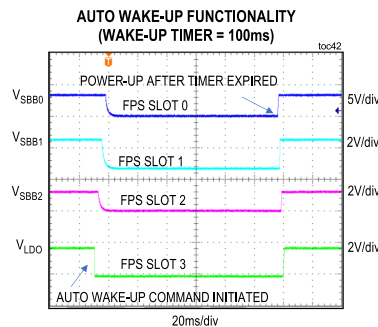
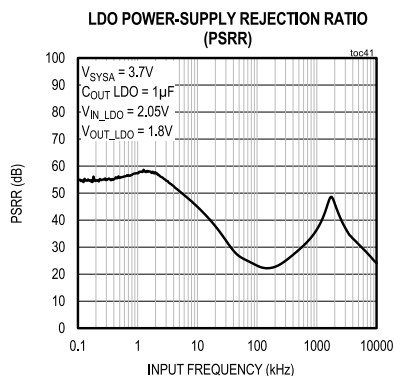
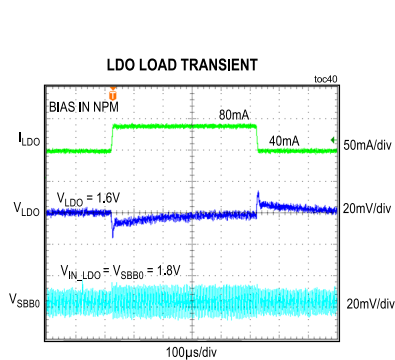
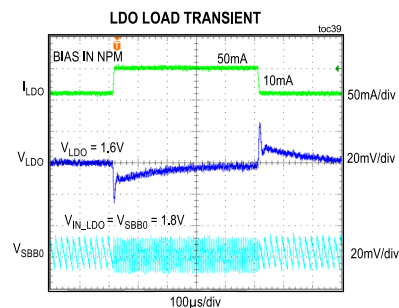
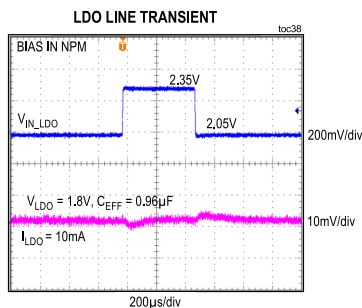
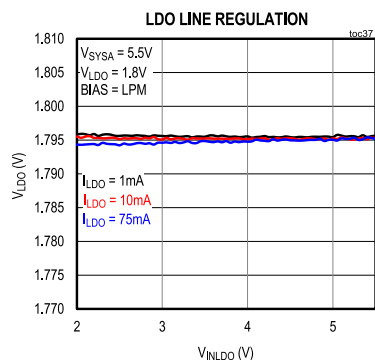
Typical Operating Characteristics (continued)

(Typical Applications Circuit. $V_{SYS} = 3.7V$, $V_{IO} = 1.8V$, $T_A = +25^\circ C$, unless otherwise noted. Inductor = DFE201612E-1R5M, $1.5\mu H$, $72m\Omega$)



Typical Operating Characteristics (continued)

(Typical Applications Circuit. $V_{SYSA} = 3.7V$, $V_{IO} = 1.8V$, $T_A = +25^\circ C$, unless otherwise noted. Inductor = DFE201612E-1R5M, $1.5\mu H$, $72m\Omega$)

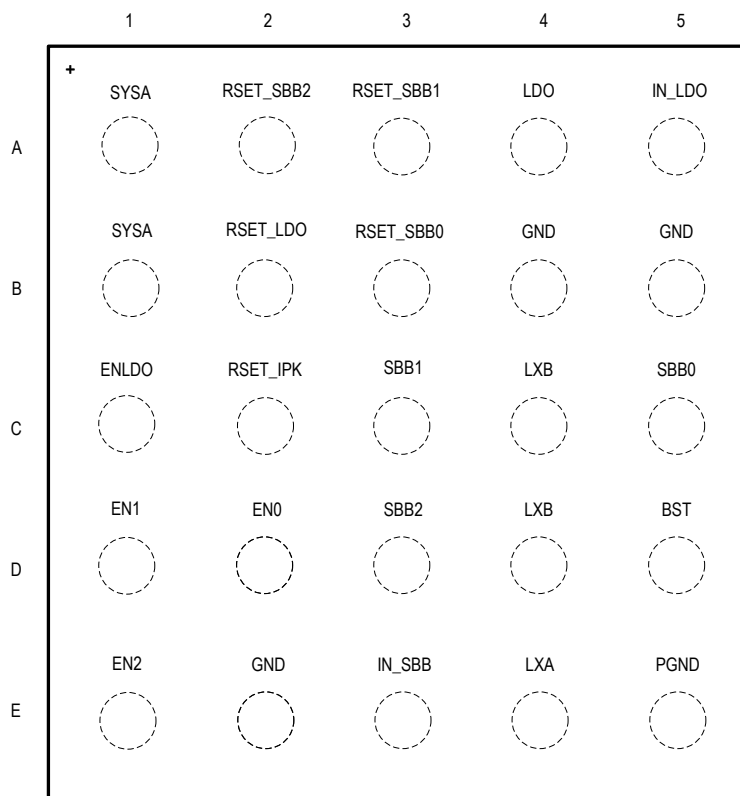


Pin Configurations

MAX77642

TOP VIEW
(BUMP SIDE DOWN)

MAX77642



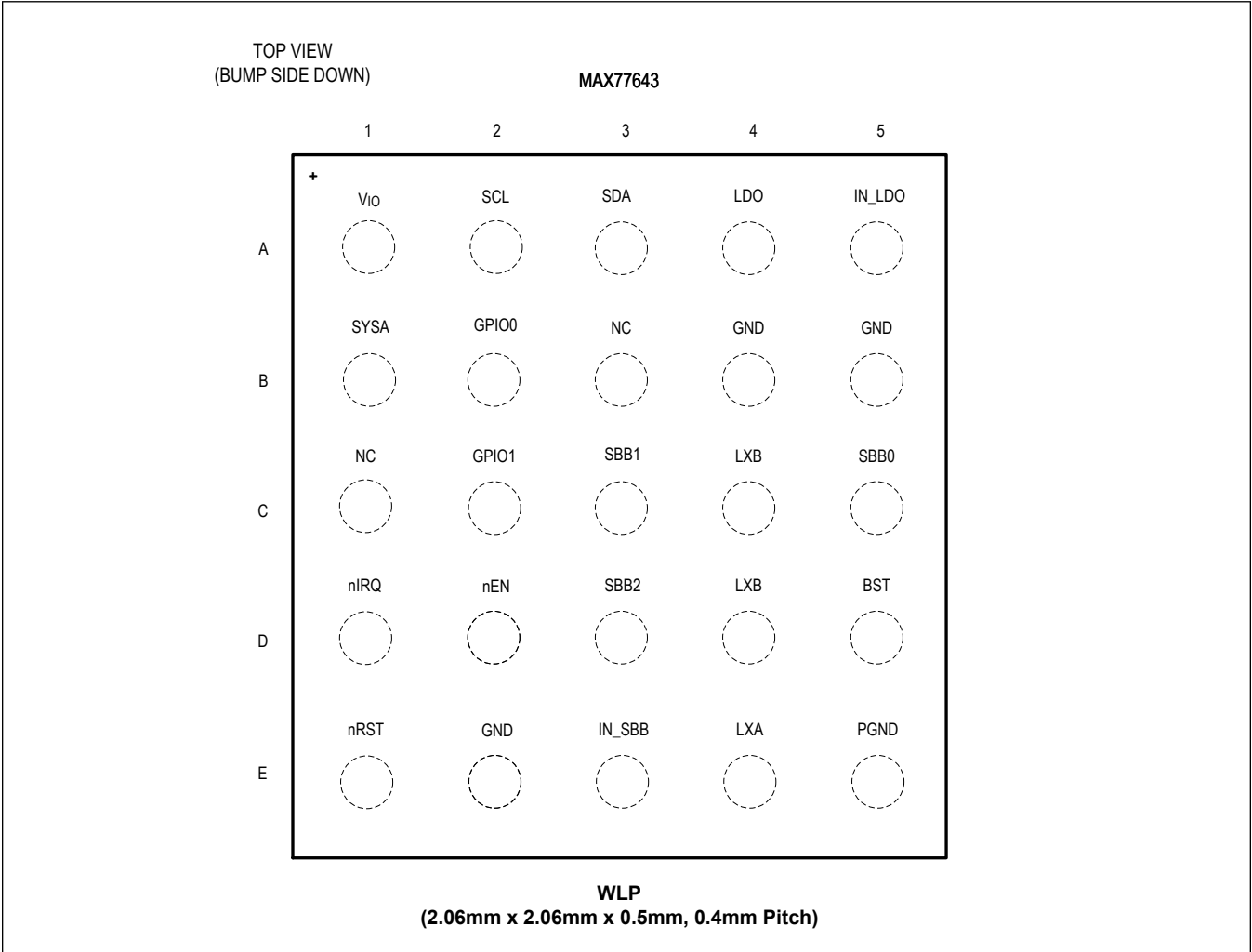
WLP

(2.06mm x 2.06mm X 0.5mm, 0.4mm Pitch)

MAX77642/MAX77643

Ultra Configurable PMIC Featuring 93% Peak Efficiency Single-Inductor, 3-Output Buck-Boost, 1-LDO for Long Battery Life Applications

MAX77643



Pin Description

| PIN | | NAME | FUNCTION | TYPE |
|-----------------|------------|-----------------|--|----------------|
| MAX77642 | MAX77643 | | | |
| TOP LEVEL | | | | |
| — | A1 | V _{IO} | I ² C Interface and GPIO Driver Power | Power Input |
| — | D2 | nEN | Active-Low Enable Input. $\overline{\text{EN}}$ supports push-button or slide-switch configurations. If not used, connect nEN to SYS and use the CNFG_SBBx_B.EN_SBBx[2:0] and CNFG_LDO_B.EN_LDO[2:0] bitfields to enable channels. | Digital Input |
| — | D1 | nIRQ | Active-Low, Open-Drain Interrupt Output. Connect a 100k Ω pullup resistor between IRQ and a voltage equal to or less than V _{SYSA} . | Digital Output |
| — | E1 | nRST | Active-Low, Open-Drain Reset Output. Connect a 100k Ω pullup resistor between nRST and a voltage equal to or less than V _{SYSA} . | Digital Output |
| — | C2 | GPIO1 | General Purpose Input/Output. The GPIO I/O stage is internally biased with V _{IO} . | Digital I/O |
| — | B2 | GPIO0 | General Purpose Input/Output. The GPIO I/O stage is internally biased with V _{IO} . | Digital I/O |
| — | A2 | SCL | I ² C Clock | Digital Input |
| — | A3 | SDA | I ² C Data | Digital I/O |
| B4, B5, E2 | B4, B5, E2 | GND | Quiet Ground. Connect GND to PGND, and the low-impedance ground plane of the PCB. | Ground |
| A2 | — | RSET_SBB2 | Select Resistor Pin SBB2. Connect a resistor from this pin to GND, using the value to configure the output voltage of SBB2. | Resistor Input |
| A3 | — | RSET_SBB1 | Select Resistor Pin SBB1. Connect a resistor from this pin to GND, using the value to configure the output voltage of SBB1. | Resistor Input |
| B3 | — | RSET_SBB0 | Select Resistor Pin SBB0. Connect a resistor from this pin to GND, using the value to configure the output voltage of SBB0. | Resistor Input |
| B2 | — | RSET_LDO | Select Resistor Pin LDO. Connect a resistor from this pin to GND, using the value to configure the output voltage of LDO0. | Resistor Input |
| C2 | — | RSET_IPK | Select Resistor Pin IPK. Connect a resistor from this pin to GND, using the value to configure the peak inductor current. | Resistor Input |
| D2 | — | EN0 | Enable Input for SBB0. Hold high to enable output regulation. Hold low to disable the output. | Digital Input |
| D1 | — | EN1 | Enable Input for SBB1. Hold high to enable output regulation. Hold low to disable the output. | Digital Input |
| E1 | — | EN2 | Enable Input for SBB2. Hold high to enable output regulation. Hold low to disable the output. | Digital Input |
| — | C1, B3 | NC | Not Connected | No Connect |
| C1 | — | ENLDO | Enable Input for LDO. Hold high to enable output regulation. Hold low to disable the output. | Digital Input |
| SIMO BUCK-BOOST | | | | |
| C5 | C5 | SBB0 | SIMO Buck-Boost Output 0. SBB0 is the power output for channel 0 of the SIMO buck-boost. Bypass SBB0 to PGND with a 10 μ F ceramic capacitor. If not used, see the Unused Outputs section. | Power Output |
| C3 | C3 | SBB1 | SIMO Buck-Boost Output 1. SBB1 is the power output for channel 1 of the SIMO buck-boost. Bypass SBB1 to PGND with a 10 μ F ceramic capacitor. If not used, see the Unused Outputs section. | Power Output |

Pin Description (continued)

| PIN | | NAME | FUNCTION | TYPE |
|------------|----------|--------|---|--------------|
| MAX77642 | MAX77643 | | | |
| D3 | D3 | SBB2 | SIMO Buck-Boost Output 2. SBB2 is the power output for channel 2 of the SIMO buck-boost. Bypass SBB0 to PGND with a 10 μ F ceramic capacitor. If not used, see the Unused Outputs section. | Power Output |
| D5 | D5 | BST | SIMO Power Input for the High-Side Output NMOS Drivers. Connect a 10nF ceramic capacitor between BST and LXB. | Power Input |
| C4, D4 | C4, D4 | LXB | Switching Node B. LXB is driven between PGND and SBBx when SBBx is enabled. LXB is driven to PGND when all SIMO channels are disabled. Connect a 1.5 μ H inductor between LXA and LXB. | Power Input |
| E4 | E4 | LXA | Switching Node A. LXA is driven between PGND and IN_SBB when any SIMO channel is enabled. LXA is driven to PGND when all SIMO channels are disabled. Connect a 1.5 μ H inductor between LXA and LXB. | Power I/O |
| E5 | E5 | PGND | Power Ground for the SIMO Low-Side FETs. Connect PGND to GND, and the low-impedance ground plane of the PCB. | Ground |
| A1, B1 | B1 | SYSA | Analog Input Supply. Connect to V _{IN_SBB} . | Power Input |
| E3 | E3 | IN_SBB | SIMO Power Input. Connect IN_SBB to SYSA and bypass to PGND with a minimum of 10 μ F ceramic capacitor as close as possible to the IN_SBB pin. | Power Input |
| LDO | | | | |
| A5 | A5 | IN_LDO | Linear Regulator Input. If connected to a SIMO output with a short trace, IN_LDO can share the output's capacitor. Otherwise, bypass with a 2.2 μ F ceramic capacitor to ground. If not used, connect to ground or leave unconnected. | Power Input |
| A4 | A4 | LDO | Linear Regulator Output. Bypass with a 1.0 μ F ceramic capacitor to GND. If not used, disable LDO and connect this pin to ground or leave unconnected. | Power Output |

MAX77642/MAX77643

Ultra Configurable PMIC Featuring 93% Peak Efficiency Single-Inductor, 3-Output Buck-Boost, 1-LDO for Long Battery Life Applications

Detailed Description

The MAX77642/MAX77643 provide highly-integrated power management solutions for low-power applications. Four regulators are integrated within this device (see [Table 1](#)). A single-inductor, multiple output (SIMO) buck-boost regulator efficiently provides three independently programmable power rails. A 150mA low-dropout linear regulator (LDO) provides ripple rejection for audio and other noise sensitive applications. The MAX77643 includes other features such as two GPIOs with alternate modes for various system requirements. A bidirectional I²C serial interface allows for configuring and checking the status of the device. An internal on/off controller provides regulator sequencing and supervisory functionality for the device.

Table 1. Regulator Summary

| REGULATOR NAME | REGULATOR TOPOLOGY | MAXIMUM I _{OUT} (mA) | V _{IN} RANGE (V) | MAX77643 V _{OUT} RANGE/ RESOLUTION |
|----------------|--------------------|-------------------------------|---------------------------|---|
| SBB0 | SIMO | Up to 500* | 2.7 to 5.5 | 0.5V to 5.5V in 25mV steps |
| SBB1 | SIMO | | 2.7 to 5.5 | 0.5V to 5.5V in 25mV steps |
| SBB2 | SIMO | | 2.7 to 5.5 | 0.5V to 5.5V in 25mV steps |
| LDO | PMOS LDO | 150 | 1.7 to 5.5 | 0.5V to 5.0V in 25mV steps |

*Shared capacity with other SBBx channels. See the [SIMO Available Output Current](#) section for more information.

Part Number Decoding

The MAX77643 has different one-time programmable (OTP) options and variants to support a variety of applications. The OTP options set default settings such as output voltage. Variants are versions of the MAX77643 with different features. See [Figure 1](#) for how to identify these. [Table 2](#) and [Table 3](#) list all available OTP options and variants. Refer to [Maxim Products Naming Convention](#) for more details.

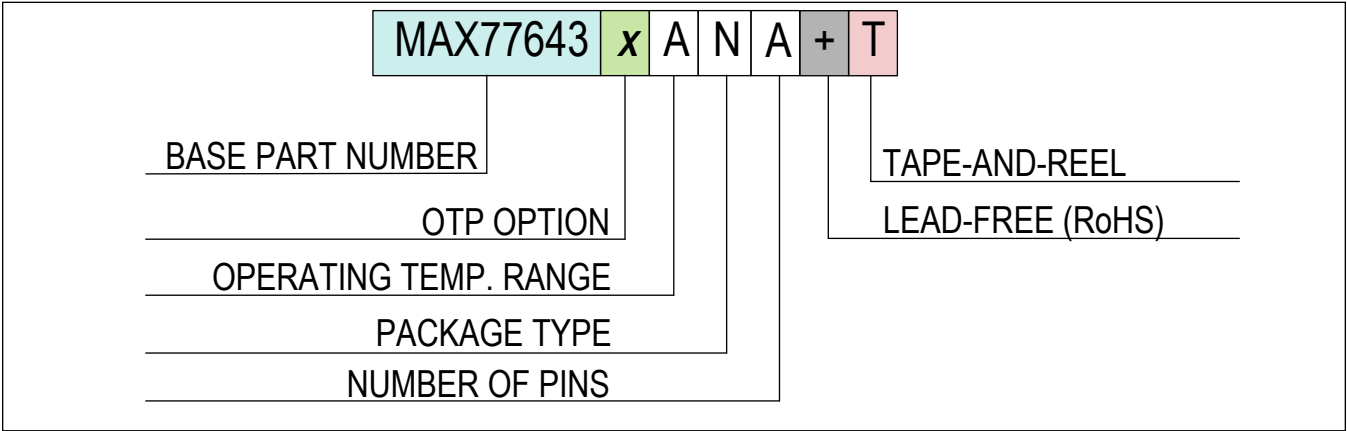


Figure 1. Part Number Decode

Table 2. Variants Table

| PART NUMBER | MAX77642 | MAX77643 |
|---|----------|----------|
| Resistor Programmable Output Voltages | Yes | No |
| Resistor Programmable Peak Current | Yes | No |
| Supports LDO/LSW | Yes | Yes |
| Include GPIOs | No | Yes |
| Individual Enable Pins for LDO and SIMO Outputs | Yes | No |

Table 2. Variants Table (continued)

| PART NUMBER | MAX77642 | MAX77643 |
|--|----------|----------|
| Programmable Flexible Power Sequencer | No | Yes |
| Watchdog Timer | No | Yes |
| Supports I ² C Serial Communication | No | Yes |

Table 3. OTP Options Table

| | | | OTP LETTER AND SETTINGS | | | | | |
|----------|---------------------|-------------------------------------|-------------------------|----------------|----------------|----------------|----------------|----------------|
| BLOCK | BIT FIELD NAME | SETTING NAME | A | B | C | E | D | S |
| Global | PU_DIS | nEN Internal, Strong Pullup Disable | Weak (10MΩ) | Weak (10MΩ) | Weak (10MΩ) | Weak (10MΩ) | Weak (10MΩ) | Weak (10MΩ) |
| | MRST | Manual Reset Time | 4s | 4s | 4s | 4s | 4s | 4s |
| | SBIA_LPM | Bias Power Mode | Low-Power Mode | Low-Power Mode | Low-Power Mode | Low-Power Mode | Low-Power Mode | Low-Power Mode |
| | nEN_MODE | On-Key Default Configuration | Logic-Mode | Logic-Mode | Logic-Mode | Logic-Mode | Logic-Mode | Logic-Mode |
| | DBEN_nEN | Debounce Timer for nEN | 500μs | 500μs | 500μs | 500μs | 500μs | 500μs |
| | ALT_GPIO0 | GPIO0 Mode | GPIO | GPIO | GPIO | GPIO | GPIO | Alt. |
| | ALT_GPIO1 | GPIO1 Mode | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO |
| | ADDR | I ² C Address (7-bit) | 0x48 | 0x4C | 0x44 | 0x40 | 0x48 | 0x48 |
| | UVLO_F[3:0] | UVLO Falling | 2.6V | 2.6V | 2.6V | 2.6V | 2.6V | 2.6V |
| | UVLO_H[3:0] | UVLO Hysteresis | 0.3V | 0.3V | 0.3V | 0.3V | 0.3V | 0.3V |
| | CID[4:0] | Chip ID | 0x02 | 0x7 | 0x8 | 0x9 | 0xB | 0x05 |
| Watchdog | WDT_LOCK | Watchdog Timer Disable Control | Unlocked | Unlocked | Unlocked | Unlocked | Unlocked | Unlocked |
| | WDT_EN | Watchdog Timer Enable | Disabled | Disabled | Disabled | Disabled | Disabled | Disabled |
| SIMO | TV_SBB0[7:0] | SBB0 V _{OUT} | 3.050V | 1.200V | 1.200V | 2.500V | 3.050V | 0.650V |
| | IP_SBB0[1:0] | SBB0 Inductor Current Peak Limit | 0.750A | 0.333A | 0.333A | 0.333A | 0.750A | 0.333A |
| | OP_MODE[1:0] (SBB0) | SBB0 Operating Mode | Buck-Boost | Buck | Buck | Buck | Buck | Buck-Boost |
| | ADE_SBB0 | Active-Discharge Resistor Enable | Enabled | Enabled | Enabled | Enabled | Enabled | Enabled |
| | EN_SBB0[2:0] | SBB0 Enable Control | FPS Slot 0 | Off | Off | Off | Off | FPS Slot 1 |
| | TV_SBB1[7:0] | SBB1 V _{OUT} | 1.800V | 2.500V | 2.500V | 1.100V | 1.800V | 0.800V |
| | IP_SBB1[1:0] | SBB1 Inductor Current Peak Limit | 0.333A | 0.333A | 0.333A | 0.500A | 0.333A | 0.333A |
| | OP_MODE[1:0] (SBB1) | SBB1 Operating Mode | Buck-Boost | Buck | Buck | Buck | Buck-Boost | Buck |
| | ADE_SBB1 | Active-Discharge Resistor Enable | Enabled | Enabled | Enabled | Enabled | Enabled | Enabled |
| | EN_SBB1[2:0] | SBB1 Enable Control | On | Off | Off | Off | On | FPS Slot 2 |
| | TV_SBB2[7:0] | SBB2 V _{OUT} | 1.200V | 1.500V | 1.500V | 1.500V | 1.075V | 1.800V |

Table 3. OTP Options Table (continued)

| | | | OTP LETTER AND SETTINGS | | | | | |
|-----|---------------------|----------------------------------|-------------------------|-----------|-----------|-----------|------------|------------|
| | IP_SBB2[1:0] | SBB2 Inductor Current Peak Limit | 0.333A | 0.333A | 0.333A | 0.333A | 0.500A | 0.333A |
| | OP_MODE[1:0] (SBB2) | SBB2 Operating Mode | Buck-Boost | Buck | Buck | Buck | Buck-Boost | Buck |
| | ADE_SBB2 | Active-Discharge Resistor Enable | Enabled | Enabled | Enabled | Enabled | Enabled | Enabled |
| | EN_SBB2[2:0] | SBB2 Enable Control | FPS Slot 2 | Off | Off | Off | Off | FPS Slot 0 |
| LDO | TV_OFS_LDO | LDO V_{OUT} Offset | No Offset | No Offset | No Offset | No Offset | No Offset | No Offset |
| | TV_LDO[6:0] | LDO V_{OUT} | 2.800V | 1.800V | 1.800V | 1.800V | 2.825V | 1.800V |
| | LDO_MD | LDO or LSW Mode | LDO | LDO | LDO | LDO | LDO | LDO |
| | ADE_LDO | Active-Discharge Resistor Enable | Enabled | Enabled | Enabled | Enabled | Enabled | Enabled |
| | EN_LDO[2:0] | LDO Enable Control | FPS Slot 1 | On | On | On | Off | FPS Slot 3 |

Detailed Description—Global Resources

The global resources encompass a set of circuits that serve the entire device and ensure safe, consistent, and reliable operation.

Features and Benefits

- Voltage Monitors
 - IN power-on-reset (POR) comparator generates a reset signal upon power-up
 - IN undervoltage ensures repeatable behavior when power is applied to and removed from the device
 - IN overvoltage monitor inhibits operation with overvoltage power sources to ensure reliability in faulty environments
- Thermal Monitors
 - +145°C junction temperature shutdown
- Manual Reset
 - 4s or 8s period
- Wake-Up Events
 - nEN input assertion
- Interrupt Handler
 - Interrupt output (nIRQ)
 - All interrupts are maskable
- Push-Button/Slide-Switch/Logic Mode On-Key (nEN)
 - Configurable push-button/slide-switch functionality
 - 500 μ s or 30ms debounce timer interfaces directly with mechanical switches
- On/Off Controller
 - Startup/shutdown sequencing
 - Programmable sequencing delay
- GPIO, nRST Digital I/Os

Voltage Monitors

The device monitors the system voltage (V_{SYS}) to ensure proper operation using three comparators (POR, UVLO, and OVLO). These comparators include hysteresis to prevent their outputs from toggling between states during noisy system transitions.

SYSA POR Comparator

The SYSA POR comparator monitors V_{SYS} and generates a power-on reset (POR) signal. When V_{SYS} is below V_{POR} , the device is held in reset ($\text{SYSRST} = 1$). When V_{SYS} rises above V_{POR} , internal signals and on-chip memory stabilize and the device is released from reset ($\text{SYSRST} = 0$).

SYSA Undervoltage-Lockout Comparator

The SYSA undervoltage-lockout (UVLO) comparator monitors V_{SYS} and generates a SYSUVLO signal when the V_{SYS} falls below UVLO threshold. The SYSUVLO signal is provided to the top-level digital controller. See [Figure 6](#), [Table 5](#), [Figure 7](#), and [Table 6](#) for additional information regarding the UVLO comparator.

SYSA Overvoltage-Lockout Comparator

The device is rated for 5.5V maximum operating voltage (V_{SYS}) with an absolute maximum input voltage of 6.0V. An overvoltage-lockout monitor increases the robustness of the device by inhibiting operation when the supply voltage is greater than V_{SYSAOVLO} . See [Figure 6](#), [Table 5](#), [Figure 7](#), and [Table 6](#) for additional information regarding the OVLO comparator.

Thermal Monitors

The MAX77643 has three global on-chip thermal sensors:

- Junction Temperature Alarm 1 → 80°C
- Junction Temperature Alarm 2 → 100°C
- Junction Temperature Shutdown → 145°C

The junction temperature alarms have maskable rising interrupts as well as status bits (see the Register Map section for more information). Unmasking these thermal alarms is recommended for all systems. If the first alarm is triggered, the system software should attempt to lower system power dissipation. If the second alarm is triggered, then attempts to lower the power dissipation were unsuccessful and the system software should turn the device off. Finally, if the junction temperature rises to junction temperature shutdown, then the MAX77643 sets the ERCFLAG.TOVLD bit and automatically turns itself off.

After a junction temperature shutdown event, the system can be enabled again. The system software can read the ERCFLAG register during initialization to see ERCFLAG.TOVLD = 1 and log that an extreme thermal event has occurred.

Chip Identification

The MAX77643 offers different one-time-programmable (OTP) options to, for example, set the default output voltages. These options are identified by the chip identification number, which can be read in the CID register.

nEN Enable Input (MAX77643)

The nEN is an active-low internally debounced digital input that typically comes from the system's on-key. The debounce time is programmable with CNFG_GLBLx.DBEN_nEN. The primary purpose of this input is to generate a wake-up signal for the PMIC that turns on the regulators. Maskable rising/falling interrupts are available for nEN (INT_GLBLx.nEN_R and INT_GLBLx.nEN_F) for alternate functionality.

The nEN input can be configured to work either with a push-button (CNFG_GLBL0.nEN_MODE = 0b00), a slide-switch (CNFG_GLBL0.nEN_MODE = 0b01), or Logic Mode (CNFG_GLBL0.nEN_MODE = 0b10). See [Figure 3](#) for more information. In both push-button mode and slide-switch mode, the on/off controller looks for a falling edge on the nEN input to initiate a power-up sequence.

EN Enable Input (MAX77642)

The MAX77642 features three enable pins to individually control the on/off state of the SIMO outputs. Drive each enable pin high to turn its respective SIMO output on. Each enable pin has a 50nA pulldown current to ground (as shown in [Figure 2](#)). The pins can be tied high for always on-applications. Do not leave the EN pins unconnected.

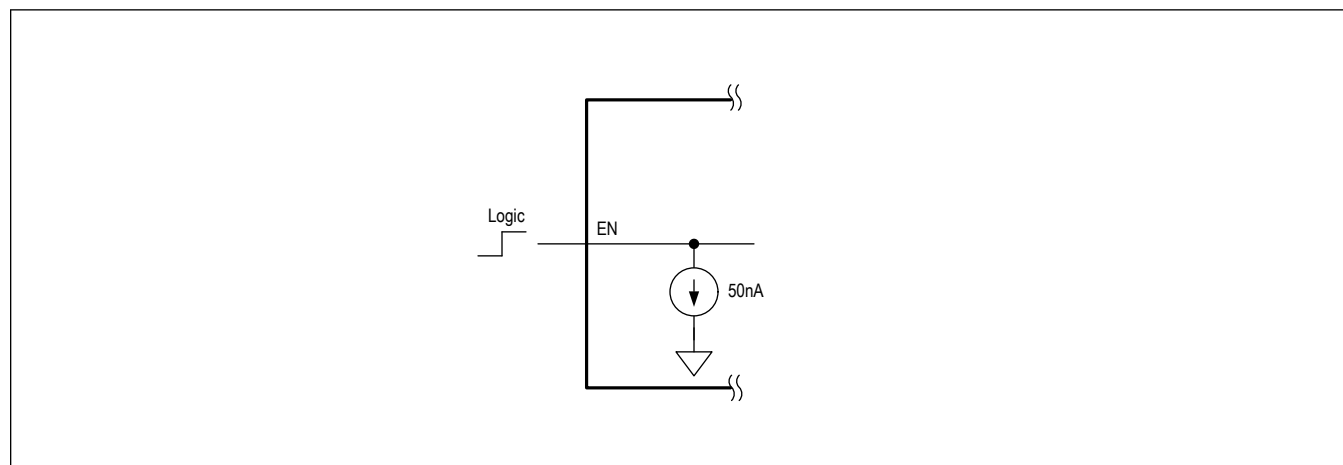


Figure 2. EN Pulldown

nEN Manual Reset (MAX77643)

The nEN works as a manual reset input when the on/off controller is in the "Resource-On" state. The manual reset function is useful for forcing a power-down in case communication with the processor fails. When nEN is configured for

push-button mode and the input is asserted ($nEN = \text{LOW}$) for an extended period (t_{MRST}), the on/off controller initiates a power-down sequence and goes to shutdown mode. When nEN is configured for slide-switch mode and the input is deasserted ($nEN = \text{HIGH}$) for an extended period (t_{MRST}), the on/off controller initiates a power-down sequence and goes to standby mode. When nEN is configured as a logic mode, the on/off controller initiates a power-up sequence and goes into Resource ON mode when the input is asserted ($nEN = \text{LOW}$). When the input is deasserted ($nEN = \text{LOW}$), the on/off controller initiates a power-down sequence and goes into shutdown mode.

nEN Triple-Functionality: Push-Button vs. Slide-Switch vs. Logic (MAX77643)

The nEN digital input can be configured to work with a push-button, a slide-switch, or a logic input. [Figure 3](#) shows nEN 's triple functionality for power-on sequencing and manual reset. The default configuration of the device is push-button mode ($CNFG_GLBL0.nEN_MODE = 0b00$) and no additional programming is necessary. Applications that use a slide-switch on-key and logic configuration must set $CNFG_GLBL0.nEN_MODE = 0b01$ and $CNFG_GLBL0.nEN_MODE = 0b10$ respectively within t_{MRST} .

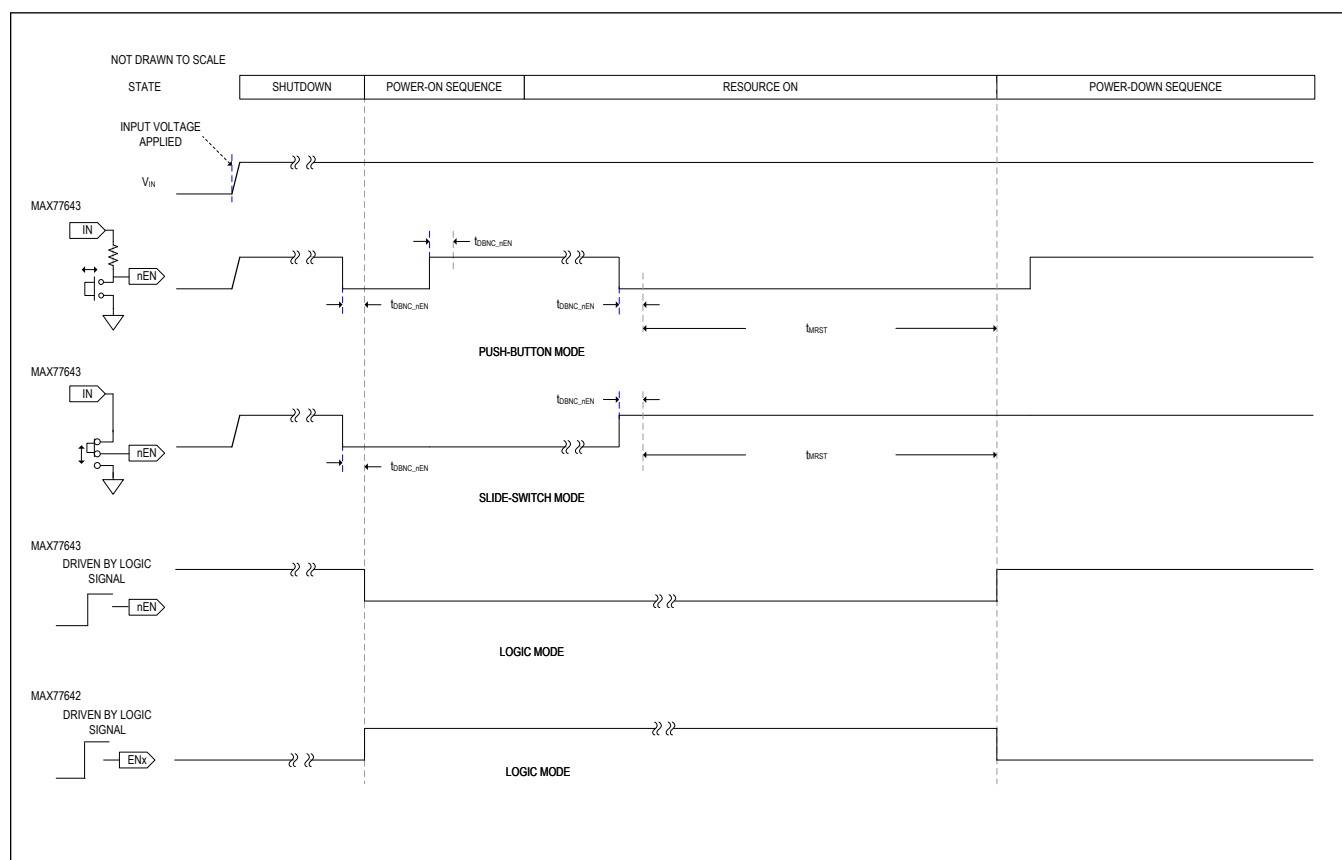


Figure 3. nEN Usage Timing Diagram

nEN Internal Pullup Resistors to V_{SYSA}

The nEN logic thresholds are referenced to V_{SYSA}. There are internal pullup resistors between nEN and V_{SYSA} (R_{nEN_PU}), which can be configured with the CNFG_GLBL0.PU_DIS bit. See [Figure 4](#). While PU_DIS = 0, the pullup value is approximately 200kΩ. While PU_DIS = 1, the pullup value is 10MΩ.

Applications using a slide-switch on-key or push-pull digital output connected to nEN can reduce quiescent current consumption by changing pullup strength to 10MΩ. Applications using normally-open, momentary, and push-button on-keys (as shown in [Figure 4](#)) do not create this leakage path and should use the stronger 200kΩ pullup option.

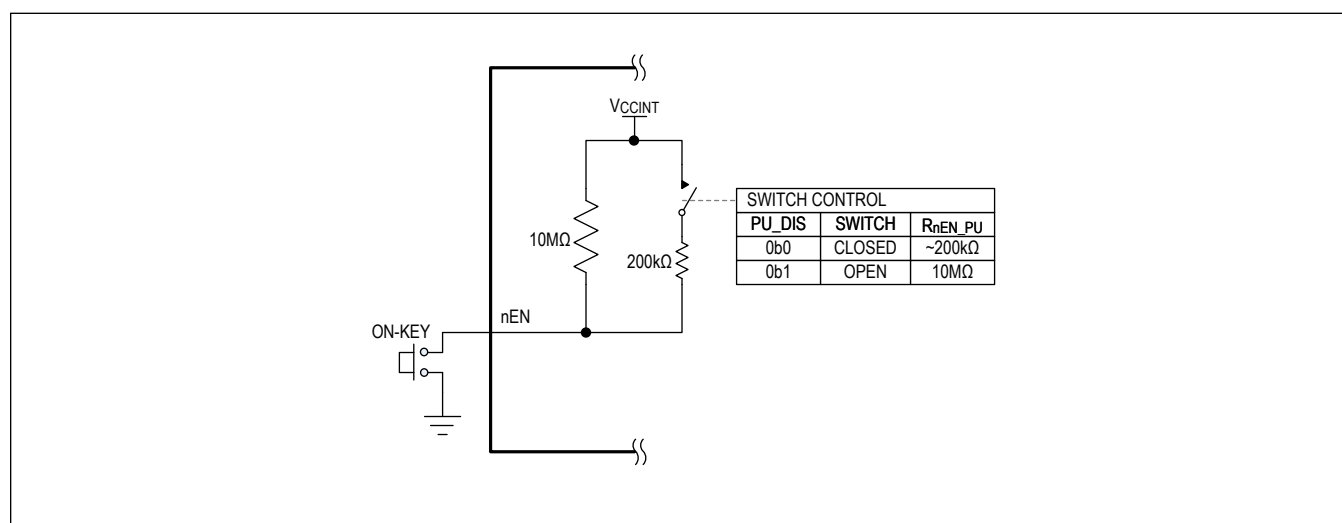


Figure 4. nEN Pullup Resistor Configuration

Interrupts (nIRQ) (MAX77643)

The nIRQ (MAX77643) is an active-low, open-drain output that is typically routed to the host processor's interrupt input to signal an important change in device status. See the *Register Map* section for a comprehensive list of all interrupt bits and status registers.

A pullup resistor to a voltage less than or equal to V_{SYSA} is required for this node. The nIRQ is the logical *NOR* of all unmasked interrupt bits in the register map.

All interrupts are masked by default. Masked interrupt bits do not cause the nIRQ pin to change. Unmask the interrupt bits to allow the nIRQ to assert.

Reset Output (nRST) (MAX77643)

The nRST (MAX77643) is an open-drain, active-low output that is typically used to hold the processor in a reset state when the device is powered down. During a power-up sequence, the nRST deasserts after the last regulator in the power-up chain is enabled (t_{RSTODD}). During a power-down sequence, the nRST output asserts before any regulator is powered down (t_{RSTOAD}). See [Figure 11](#) for nRST timing.

A pullup resistor to a voltage less than or equal to V_{SYSA} is required for this node.

General-Purpose Input Output (GPIO) (MAX77643)

The MAX77643 provides two general-purpose input/output (GPIO) pins increase system flexibility. See [Figure 5](#) for more details.

Clear CNFG_GPIOx.DIR = 0b0 to configure GPIO as a general-purpose output (GPO). The GPO can either be in push-pull mode (CNFG_GPIOx.DRV = 1) or open-drain mode (CNFG_GPIOx.DRV = 0).

- The push-pull output mode is ideal for applications that need fast (~2ns) edges and low power consumption.
- The open-drain mode requires an external pullup resistor (typically 10kΩ to 100kΩ). Connect the external pullup resistor to a bias voltage that is less than or equal to V_{IO} .
 - The open-drain mode can be used to communicate to different logic domains. For example, to send a signal from the GPO on a 1.8V logic domain ($V_{IO} = 1.8V$) to a device on a 1.2V logic domain, connect the external pullup resistor to 1.2V.
 - The open-drain mode can be used to connect several open-drain (or open-collector) devices together on the same bus to create wired logic (wired AND logic is positive-true; wired OR logic is negative-true).
- The general-purpose input (GPI) functions are still available while the pin is configured as a GPO. In other words, the CNFG_GPIOx.DI (input status) bit still functions and does not collide with the state of the CNFG_GPIOx.DIR bit.

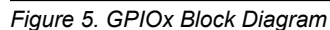
Set CNFG_GPIOx.DIR to have the GPIO function as a GPI. The GPI features a 30ms debounce timer (t_{DBNC_GPI}) that can be enabled or disabled with DBEN_GPI.

- Enable the debounce timer (CNFG_GPIOx.DBEN_GPI = 1) if the GPI is connected to a device that can bounce or chatter, like a mechanical switch.
- If the GPI is connected to a circuit with clean logic transitions and no risk of bounce, disable the debounce timer (CNFG_GPIOx.DBEN_GPI = 0) to eliminate logic delays. With no debounce timer, the GPI input logic propagates to nIRQ in 10ns.

A dedicated internal oscillator is used to create the 30ms (t_{DBNC_GPI}) debounce timer. To obtain low V_{IO} supply current, ensure the GPIO voltage is either logic high or logic low. If the GPIO pin is unconnected (either as a GPI or an open-drain GPO) and V_{IO} is powered, the GPIO voltage trends towards the logic level gray area ($0.3 \times V_{IO} < V_{GPIO} < 0.7 \times V_{IO}$). If V_{GPIO} is in the gray area, V_{IO} current can be more than 10μA.

The GPI features edge detectors that feed into the the top-level interrupt system of the chip. This allows software to use interrupts to service events associated with a GPI change instead of polling for these changes.

- If the application wants nIRQ to go low **only on a GPI rising edge**, then it should **clear** the GPI rising edge interrupt mask bit (INTM_GLBLx.GPI_RM = 0) and **set** the GPI falling edge interrupt mask bit (INTM_GLBLx.GPI_FM = 1).
- If the application wants nIRQ to go low **only on a GPI falling edge**, then it should **set** the GPI rising edge interrupt mask bit (INTM_GLBLx.GPI_RM = 1) and **clear** the GPI falling edge interrupt mask bit (INTM_GLBLx.GPI_FM = 0).
- If the application wants nIRQ to go low **on both GPI falling and rising edges**, then it should **clear** the GPI rising edge interrupt mask bit (INTM_GLBLx.GPI_RM = 0) and **clear** the GPI falling edge interrupt mask bit (INTM_GLBLx.GPI_FM = 0).



The GPIO in the MAX77643 can be configured to have a different function. Whether the GPIO is in GPIO mode or alternate mode can be checked by reading the CNFG_GPIOx.ALT_GPIOx bit. [Table 4](#) summarizes the alternate functions for each GPIO.

| GPIOx | CNFG_GPIOx REGISTER | |
|-------|---------------------|---|
| | ALT_GPIOx = 0 | ALT_GPIOx = 1 |
| GPIO0 | Standard GPIO | Active-high input, controls the DVS feature for SBB0. |
| GPIO1 | Standard GPIO | Active-high output of SBB2's flexible power sequencer (FPS) slot. |

On/Off Controller

The on/off controller monitors multiple power-up (wake-up) and power-down (shutdown) conditions to enable or disable resources that are necessary for the system and its processor to move between its operating modes.

Many systems have one power management controller and one processor and rely on the on/off controller to be the master controller. In this case, the on/off controller receives wake-up events and enables some or all of the regulators to power up a processor. That processor then manages the system. To conceptualize this master operation, see [Figure 7](#) and [Table 6](#). A typical path through the on/off controller is:

1. Apply a battery and start in the shutdown state.
2. Press the system's on-key (nEN = LOW) and follow transitions 3 and 4 to the resource-on state. If any resources are on the FPS, transitions 5A and 5B are followed.
3. The device performs its desired functions in the resource-on state. when it is ready to turn off, a manual reset first drives the transition through transitions 6A and 6B for FPS power down then through the 7 and 0 states to the shutdown state.

Some systems have several power management blocks, a main processor, and subprocessors. These systems can use this device as a subpower management block for a peripheral portion of circuitry as long as there is an I²C port available from a higher level processor. To conceptualize this operation, see [Figure 7](#) and [Table 6](#). A typical path through the on/off controller used in this way is:

1. Apply a battery to the system and start in the shutdown state.
2. The higher level processor can now control this device's resources with I²C commands (e.g., turn on/off regulators).
3. When the higher level processor is ready to turn this device off, it turns off everything through I²C to transition along path 7 to the shutdown state.

Note that in this style of operation, the CNFG_GLBL0.SFT_CTRL[1:0] bits should not be used to turn the device off. The CNFG_GLBL0.SFT_CTRL[1:0] bits establish directives to the on/off controller itself that does not make sense in this subpower management block operation. If the processor uses I²C commands to enable the device's resources, the processor should also use I²C commands to disable them.

Top Level On/Off Controller (MAX77642)

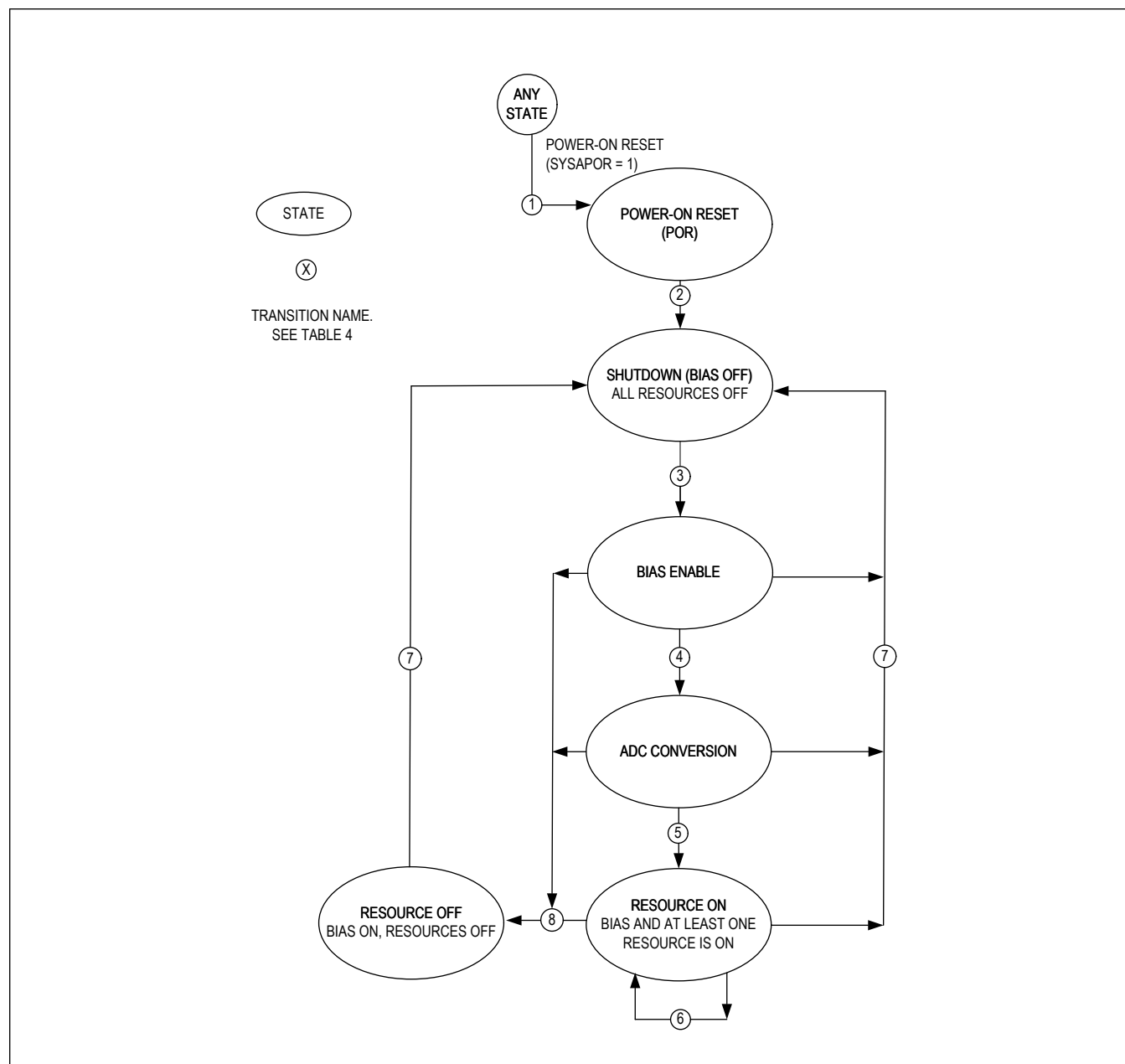


Figure 6. Top Level On/Off Controller State Diagram (MAX77642)

On/Off Controller Transition Table (MAX77642)**Table 5. On/Off Controller Transition/State (MAX77642)**

| TRANSITION | CONDITION (TRANSITION HAPPENS WHEN...) |
|------------|--|
| 1 | System voltage is above the POR threshold ($V_{SYS} > V_{POR}$) |
| 2 | $V_{SYS} \geq V_{SYS(UVLO_R)}$ |
| 3 | First ENx transitions from low to high |
| 4 | Main Bias enable time expires (t_{SBIA_EN}) |
| 5 | ADC detection time expires (t_{RSET}) |
| 6 | Additional ENx transitions from low to high OR ENx transitions from high to low (as long as one SIMO channel or the LDO is enabled) |
| 7 | Last ENx transitions from high to low (all SIMO channels and the LDO are disabled) |
| 8 | Chip overtemperature lockout ($T_J > T_{OTLO}$) OR SYS A undervoltage lockout ($V_{SYS} < V_{SYS(UVLO)}$) OR SYS A overvoltage lockout ($V_{SYS} > V_{SYS(OVLO)}$) |

Top Level On/Off Controller (MAX77643)

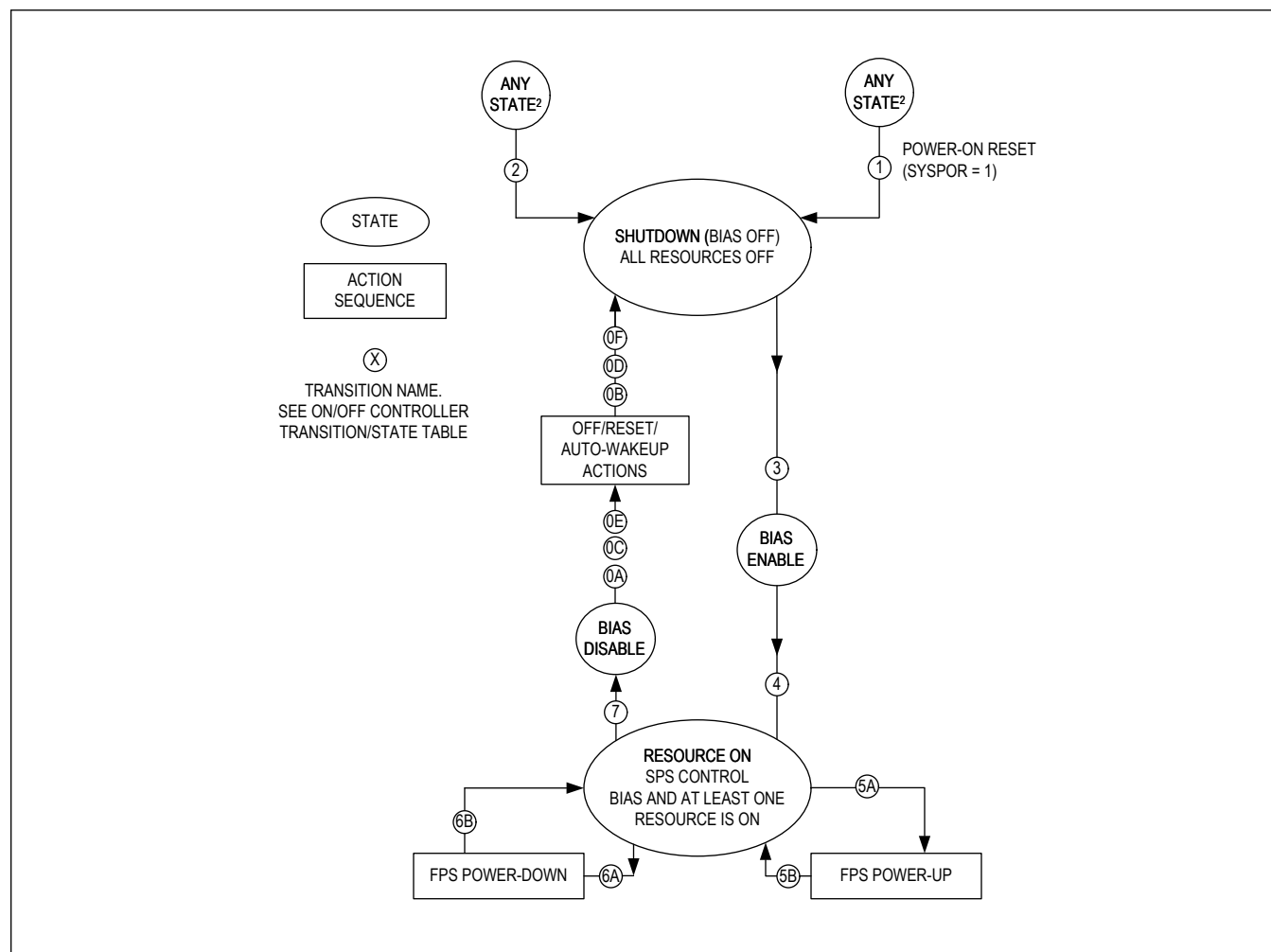


Figure 7. Top Level On/Off Controller State Diagram (MAX77643)

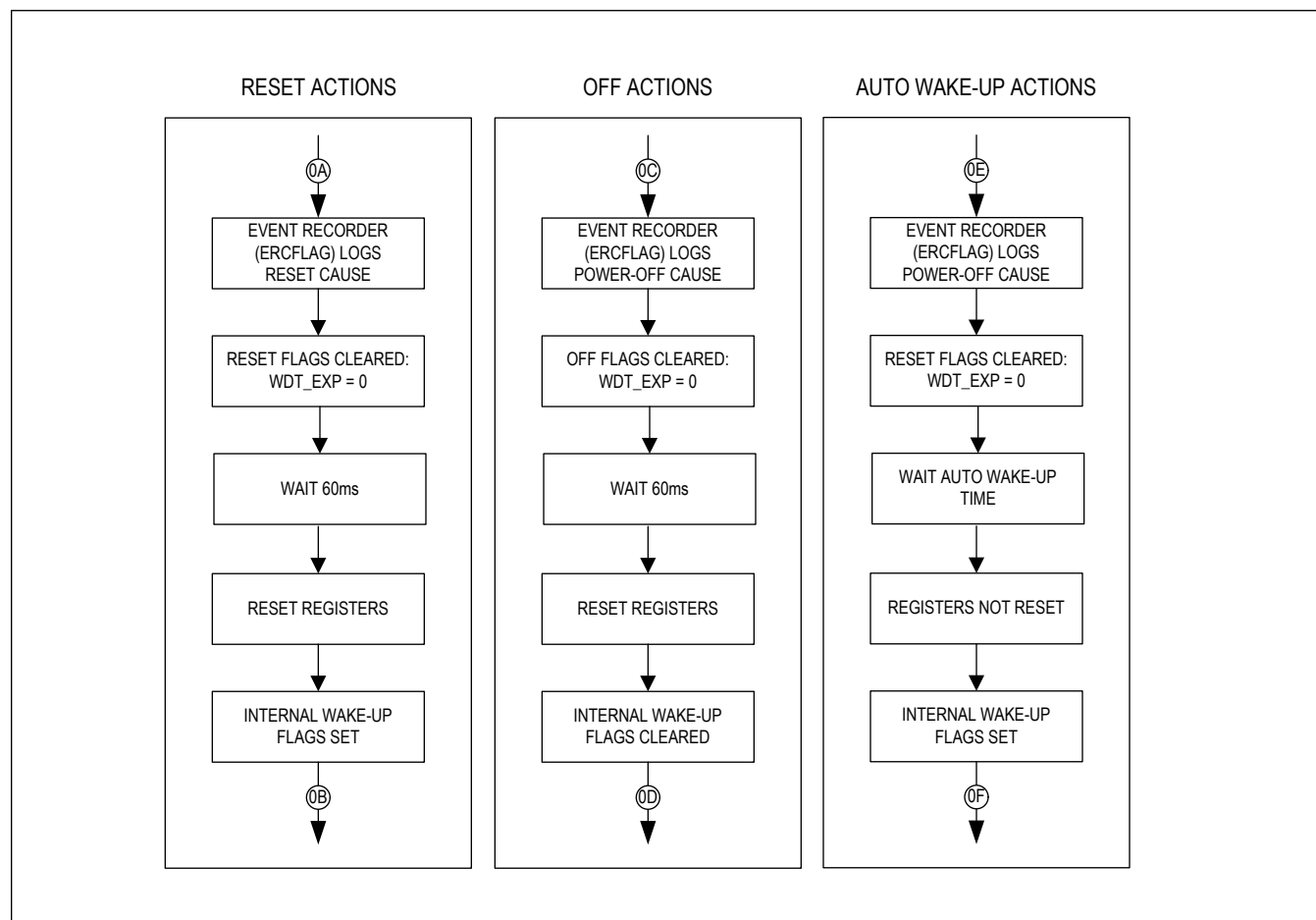
On/Off Controller Transition Table (MAX77643)**Table 6. On/Off Controller Transition/State (MAX77643)**

| TRANSITION | CONDITION (TRANSITION HAPPENS WHEN...) |
|------------|--|
| 0A | Software cold reset (CNFG_GLBL0.SFT_CTRL[1:0] = 0b01) OR Watchdog timer expired and caused reset (ERCFLAG.WDT_RST = 1, CNFG_WDT.WDT_MODE = 1) |
| 0B | Reset actions completed |
| 0C | Software power-off (CNFG_GLBL0.SFT_CTRL[1:0] = 0b10) OR Watchdog expired and caused power-off (ERCFLAG.WDT_OFF = 1, CNFG_WDT.WDT_MODE = 0) OR Chip overtemperature lockout ($T_J > T_{OTLO}$) OR SYSA undervoltage lockout ($V_{SYSA} < V_{SYSAUVLO} + V_{SYSAUVLO_HYS}$) OR SYSA overvoltage lockout ($V_{SYSA} > V_{SYSAOVLO}$) OR Manual reset occurred (ERCFLAG.MRST = 1) |
| 0D | Off actions completed |
| 0E | Software auto wake-up (CNFG_GLBL0.SFT_CTRL = 0b11) |
| 0F | Auto wake-up actions completed |
| 1 | System voltage is above the POR threshold ($V_{SYSA} > V_{POR}$). |
| 2 | Chip overtemperature lockout ($T_J > T_{OTLO}$) OR SYSA undervoltage lockout ($V_{SYSA} < V_{SYSAUVLO} + V_{SYSAUVLO_HYS}$) OR SYSA overvoltage lockout ($V_{SYSA} > V_{SYSAOVLO}$) |
| 3 | Any resources force enabled OR Internal wake-up flags are set (see the Internal Wake-Up Flags (MAX77643) section) |
| 4 | Main bias enable time expires (t_{SBIAS_EN}) AND Conditions in Transition 2 are not met. |
| 5A | FPS power-up sequence has not happened yet AND Resources are not forced off AND Internal wake-up flags are set (see the Internal Wake-Up Flags (MAX77643) section) |
| 5B | FPS power-up sequence completed |
| 6A | FPS power-up sequence completed AND Software cold reset (CNFG_GLBL0.SFT_CTRL[1:0] = 0b01) OR Software power-off (CNFG_GLBL0.SFT_CTRL[1:0] = 0b10) OR Software auto wake-up (CNFG_GLBL0.SFT_CTRL = 0b11) OR Watchdog timer expired OR Manual reset occurred (ERCFLAG.MRT = 1) OR CNFG_GLBL1.SBB_F_SHUTDN = 0b1 AND SBB fault occurs |
| 6B | FPS power-down sequence finished |
| 7 | Last resource turned off |

Internal Wake-Up Flags (MAX77643)

After transitioning to the shutdown state because of a reset, to allow the device to power up again, internal wake-up flags are set to remember the wake-up request. In [Figure 7](#) and [Table 6](#), these internal wake-up flags trigger transition 3. The internal wake-up flags are set when any of the following happen:

- nEN is debounced (see the [nEN Enable Input \(MAX77643\)](#) section)
 - For example, after a push-button is pressed or a slide-switch switched to HIGH.
- Software cold reset command sent (CNFG_GLBL0.SFT_CTRL[1:0] = 0b01)

Reset, Off, and Auto Wake-Up Sequences (MAX77643)*Figure 8. On/Off Controller Reset and Off-Action Sequences*

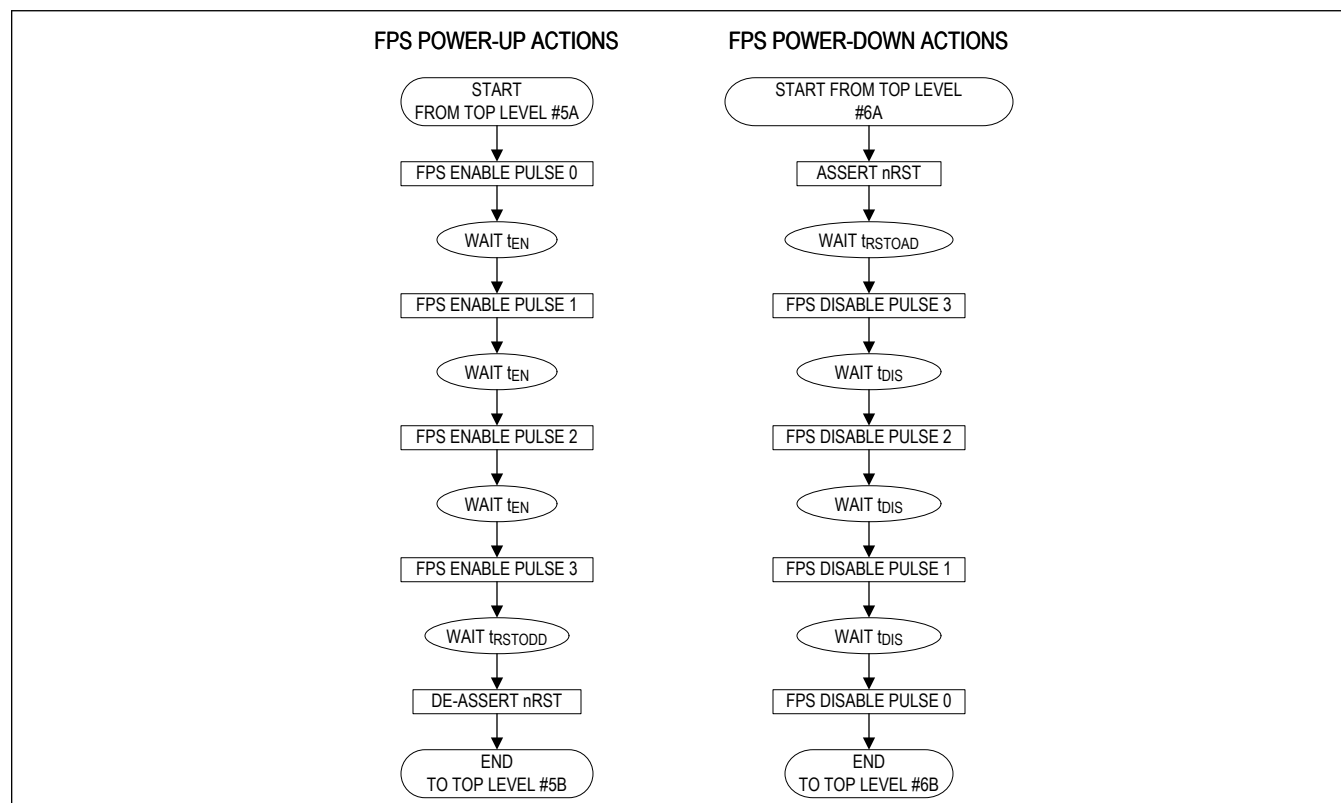
Power-Up/Down Sequence (MAX77643)

Figure 9. Power-Up/Down Sequence

Flexible Power Sequencer (FPS) (MAX77643)

The FPS allows resources to power up under hardware or software control. Additionally, each resource can power up independently or among a group of other regulators with adjustable power-up/down delays (sequencing). [Figure 10](#) shows four resources powering up under the control of the flexible power sequencer.

The flexible sequencing structure consists of one master sequencing timer and four slave resources (SBB0, SBB1, SBB2 and LDO). When the FPS is enabled, a master timer generates four sequencing events for device power-up/down.

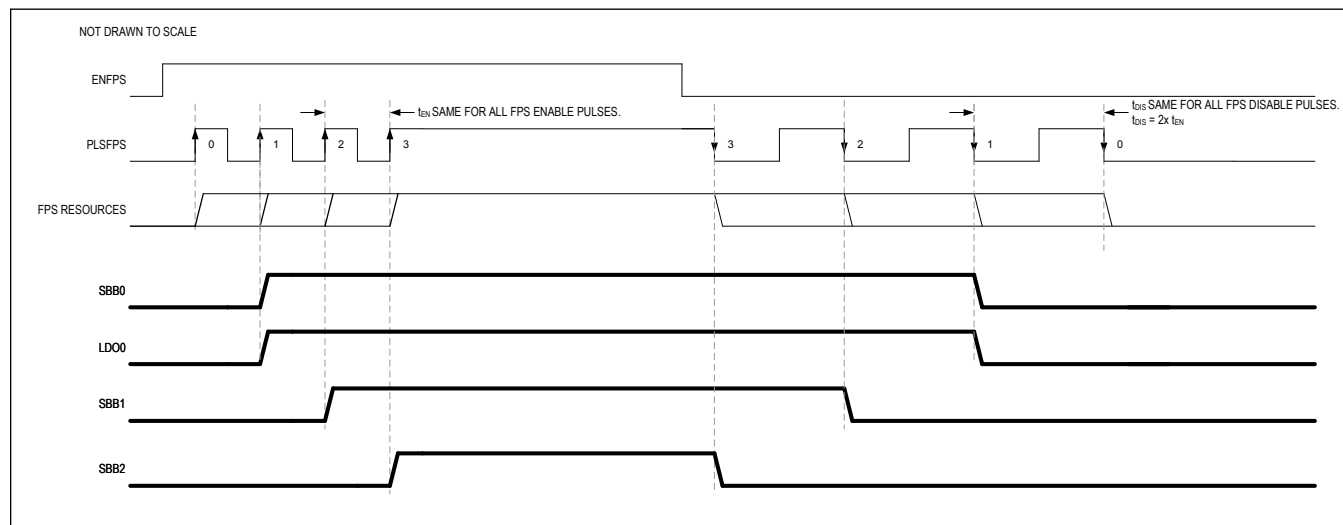


Figure 10. Flexible Power Sequencer Basic Timing Diagram

Startup Timing Diagram Due to nEN (MAX77643)

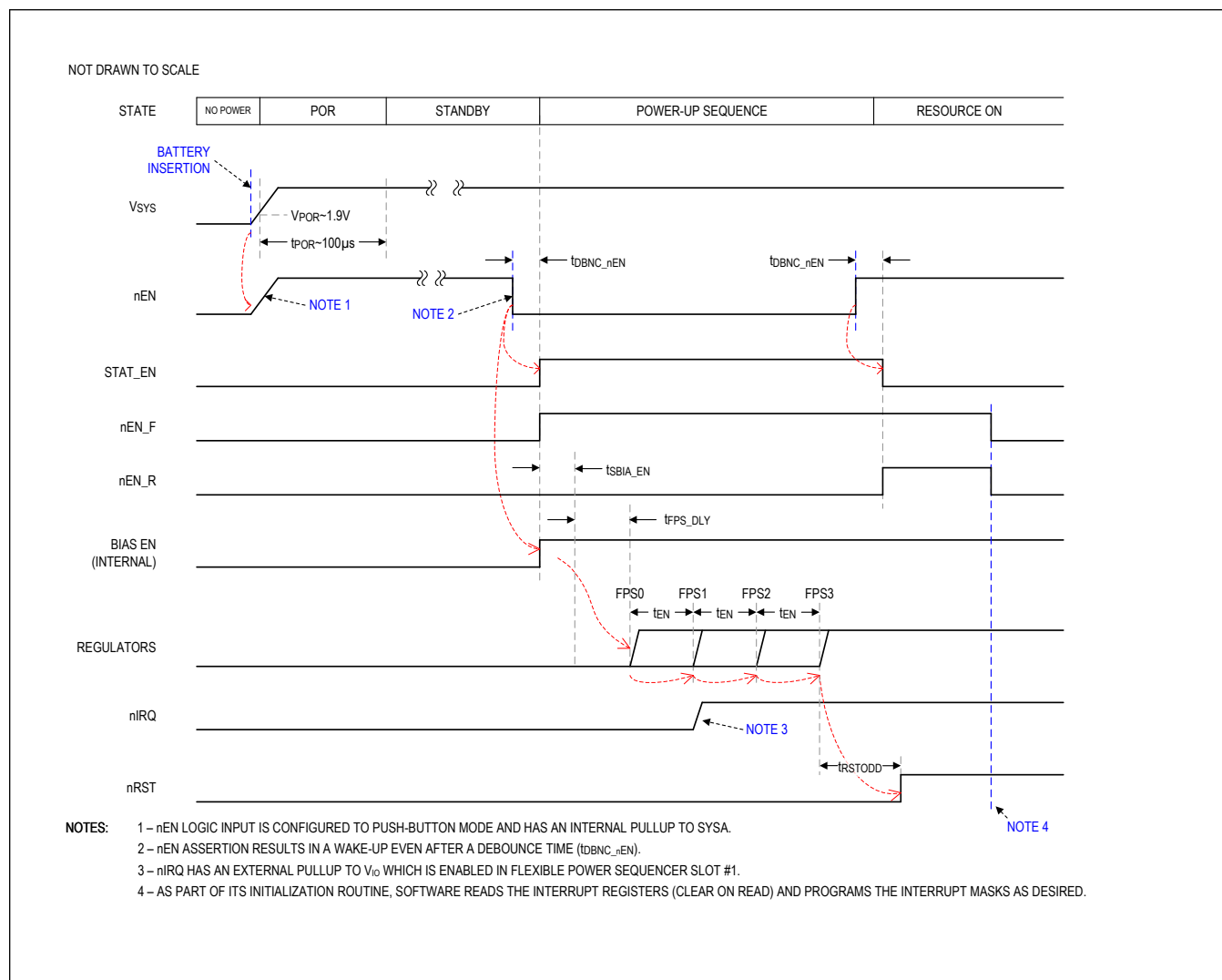


Figure 11. Startup Timing Diagram Due to nEN

Force Enabled/Disabled Channels (MAX77643)

Force enable SIMO and LDO output channels by setting CNFG_SBBx_B.EN_SBBx[2:0] (SIMO) or CNFG_LDOx_B.EN_LDOx[2:0] (LDO) = 0x6. Depending on the OTP, output channels may already be force enabled by default. Output channels configured this way are independent of the flexible power sequence and start up as soon as $SYS > UVLO$ rising. The main bias also automatically turns on.

Likewise, output channels can be force disabled by setting EN_SBBx[2:0] or EN_LDOx[2:0] = 0x4.

Debounced Inputs (nEN, GPI) (MAX77643)

The nEN and GPIO (when operating as an input) have programmable debounce timers on both the rising and falling edges to reject undesired transitions. The input must be at a stable logic level for the entire debounce period for the output to change its logic state. [Figure 12](#) shows an example timing diagram for the nEN debounce.

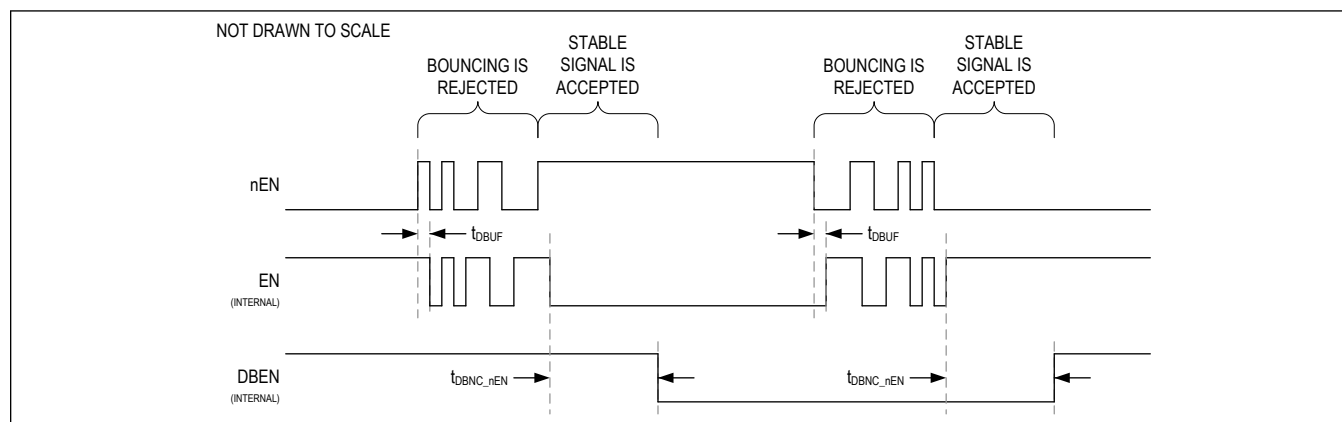


Figure 12. Debounced Inputs

Watchdog Timer (WDT) (MAX77643)

The IC features a watchdog timer function for operational safety. If this timer expires without being cleared, the on/off controller causes the IC to enter the shutdown state and resets configuration registers. See the [On/Off Controller](#) and [On/Off Controller Transition Table \(MAX77643\)](#) sections (transitions 0A and 0C) for more details.

Write CNFG_WDT.WDT_EN = 1 through the I²C interface to enable the timer. The watchdog timer period (t_{WD}) is configurable from 16 seconds to 128 seconds in four steps with CNFG_WDT.WDT_PER[1:0]. The default timer period is 128 seconds. While the watchdog timer is enabled, the CNFG_WDT.WDT_CLR bit must be set through the I²C interface periodically (within t_{WD}) to reset the timer and prevent shutdown. See the *Register Map* and [Figure 13](#) for additional details.

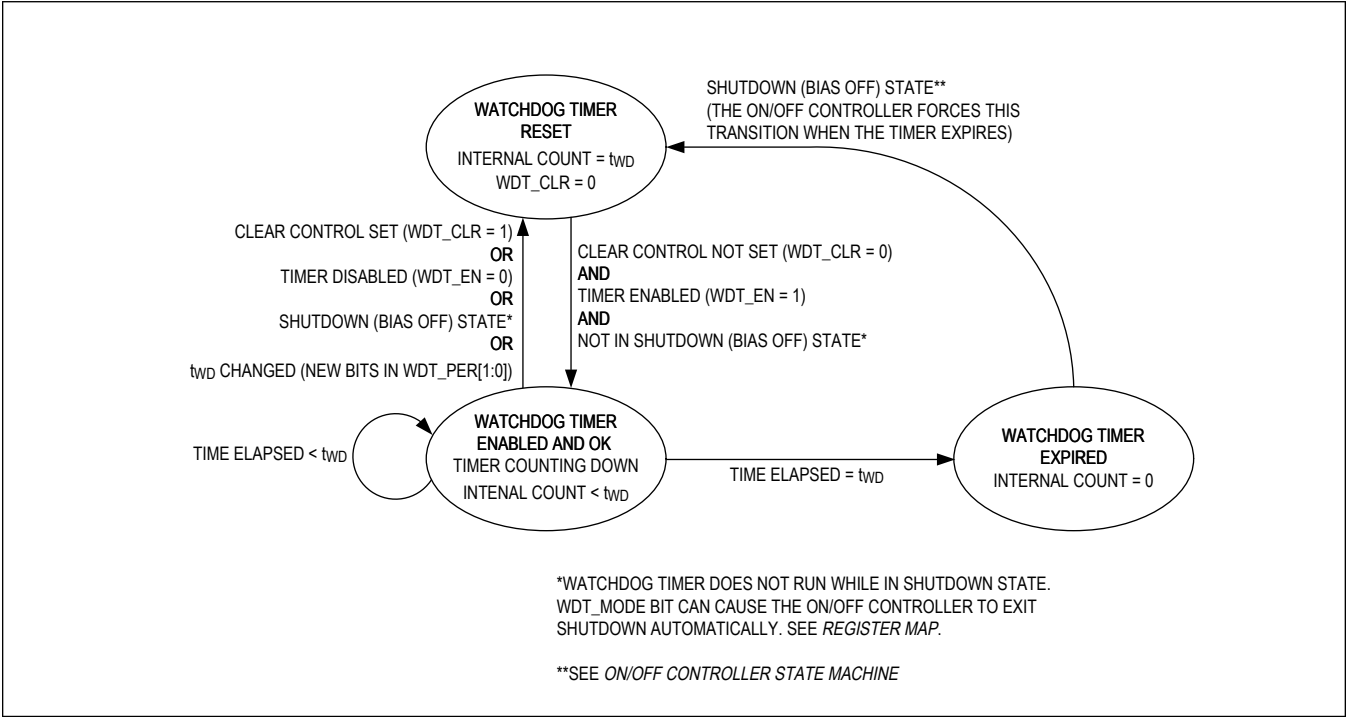


Figure 13. Watchdog Timer State Machine

The timer can be factory-programmed to be enabled by default, disabled by default, or locked from accidental disable. The CNFG_WDT.WDT_LOCK bit is read-only and must be configured at the factory. See [Table 7](#) for a full description.

Table 7. Watchdog Timer Factory-Programmed Safety Options

| WDT_LOCK | WDT_EN | FUNCTION |
|----------|--------|--|
| 0 | 0 | Watchdog timer is disabled by default. Timer can be enabled or disabled by I ² C writes. |
| 0 | 1 | Watchdog timer is enabled by default. Timer can be enabled or disabled by I ² C writes. |
| 1 | 0 | Watchdog timer is disabled by default. Timer can be enabled by an I ² C write, but only a SYSRST can reset the CNFG_WDT.WDT_EN value back to 0. Timer can not be disabled by direct I ² C writes to CNFG_WDT.WDT_EN (write from 1 → 0 is ignored, write from 0 → 1 is accepted). |
| 1 | 1 | Watchdog timer is enabled by default. Nothing can disable the timer. |

Detailed Description—SIMO Buck-Boost

The device has a micropower single-inductor, multiple-output (SIMO) buck-boost DC-to-DC converter designed for applications that emphasize low supply current and small solution size. A single inductor is used to regulate three separate outputs, saving board space while delivering better total system efficiency than equivalent power solutions using one buck and linear regulators.

The buck-boost configuration utilizes the entire battery voltage range due to its ability to create output voltages that are above, below, or equal to the input voltage. Peak inductor current for each output is programmable to optimize the balance between efficiency, output ripple, EMI, PCB design, and load capability.

To further boost efficiency when the output voltage is always lower than the input, individual channels of the SIMO buck-boost converter can be configured to be in buck-only or boost-only mode, reducing switching losses by toggling less switches compared to buck-boost mode. See the [SIMO Buck Mode \(MAX77643\)](#) and [SIMO Boost Mode \(MAX77643\)](#) sections for more details.

SIMO Features and Benefits

- Three Output Channels
- Ideal for Low-Power Designs
 - Delivers up to 500mA at 1.8V from a 3.7V Input
 - $\pm 2\%$ Accurate Output Voltage
- Small Solution Size
 - Multiple Outputs from a Single 1.5 μ H Inductor
 - Small 10 μ F (0402) Output Capacitors
- Flexible and Easy to Use
 - Single Mode of Operation
 - Glitchless Transitions Between Buck, Boost, and Buck-Boost Modes
 - Programmable Peak Inductor Current
 - Programmable On-Chip Active Discharge
 - Programmable Buck-Only and Boost-Only Mode (MAX77643)
 - Resistor Programmable Output Voltages (MAX77642)
- Long Battery Life
 - High Efficiency, > 91% at 1.8V Output
 - Better Total System Efficiency than Buck + LDOs
 - Low Quiescent Current, 1 μ A per Output
 - Low Input Operating Voltage, 2.7V (min)

SIMO Detailed Block Diagram

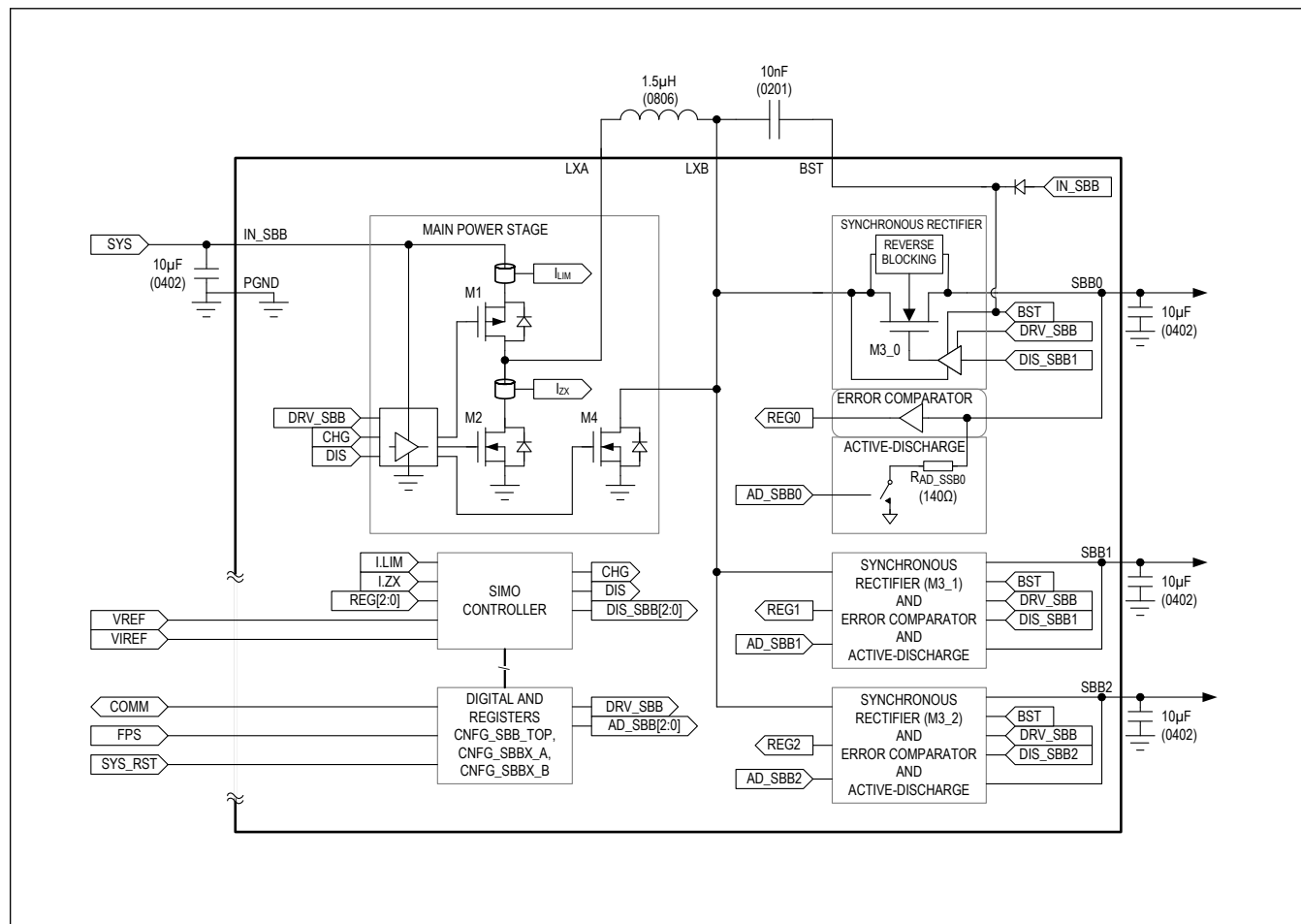


Figure 14. SIMO Detailed Block Diagram

SIMO Control Scheme

The SIMO buck-boost is designed to service multiple outputs simultaneously. A proprietary controller ensures that all outputs get serviced in a timely manner, even while multiple outputs are contending for the energy stored in the inductor. When no regulator needs service, the state machine rests in a low-power rest state.

When the controller determines that a regulator requires service, it charges the inductor ($M1 + M4$) until the peak current limit is reached ($I_{LIM} = CNFG_SBBx_B.IP_SBB[1:0]$). The inductor energy then discharges ($M2 + M3_x$) into the output until the current reaches zero (I_{ZX}). In the event that multiple output channels need servicing at the same time, the controller ensures that no output utilizes all of the switching cycles. Instead, cycles interleave between all the outputs that are demanding service, while outputs that do not need service are skipped.

Drive Strength (MAX77643)

The SIMO regulator's drive strength for its internal power MOSFETs is adjustable using the `CNFG_SBB_TOP.DRV_SBB[1:0]` bit field. The ideal value is determined experimentally for each application. For a PCB layout comparable to the MAX77642/MAX77643 evaluation kit, 0x1 is the best setting and represents a balance between efficiency and EMI. Faster settings result in higher efficiency but generally require stricter layout rules or shielding to avoid additional EMI. Slower settings limit EMI in non-ideal settings (e.g., contained layout, antennae adjacent to the device, etc.). Change the drive strength only once during system initialization.

SIMO Output Voltage Configuration

Each of the SIMO outputs are independently configurable. To set the output voltages at SBB0/1/2 for the MAX77642, connect the appropriate resistors from RSET_SBB0/1/2 to GND as shown in [Table 8](#) and [Table 9](#). The RSET_SBB0/1/2 resistors should have 1% or better tolerance. To set the output voltages at SBB0/1/2 for the MAX77643, use the I²C interface to load the configuration registers CNFG_SBBx_A.TV_SBBx[7:0]. This 8-bit configuration is a linear transfer function that starts at 0.5V and ends at 5.5V with 25mV increments, and sets the output voltage as: $SBBx = 0.5V + 25mV \times TV_SBBx[7:0]$ (decimal).

Table 8. SBB0 Output Voltage Settings

| RSET_SBB0 (kΩ) | OUTPUT VOLTAGE - SBB0 (V) |
|----------------|---------------------------|
| 0.001 | 0.50 |
| 4.99 | 0.60 |
| 6.00 | 0.70 |
| 7.15 | 0.80 |
| 8.45 | 0.90 |
| 10.0 | 1.00 |
| 11.8 | 1.05 |
| 14.0 | 1.10 |
| 16.9 | 1.20 |
| 20.0 | 1.30 |
| 23.7 | 1.40 |
| 28.0 | 1.60 |
| 34.0 | 1.75 |
| 40.2 | 1.80 |
| 47.5 | 1.85 |
| 56.2 | 2.00 |
| 66.5 | 2.20 |
| 80.6 | 2.40 |
| 95.76 | 2.80 |
| 113.0 | 3.00 |
| 133.0 | 3.20 |
| 162.0 | 3.25 |
| 191.0 | 3.30 |
| 226.0 | 3.35 |
| 267.0 | 3.40 |
| 324.0 | 3.80 |
| 383.0 | 4.00 |
| 452.0 | 4.20 |
| 536.0 | 4.40 |
| 634.0 | 4.60 |
| 768.0 | 5.00 |
| 909.0 | 5.20 |

Table 9. SBB1/2 Output Voltage Settings

| RSET_SBB1/2 (kΩ) | OUTPUT VOLTAGE - SBB1/2 (V) |
|------------------|-----------------------------|
| 0.001 | 0.50 |
| 4.99 | 0.60 |
| 6.00 | 0.70 |
| 7.15 | 0.80 |
| 8.45 | 0.90 |
| 10.0 | 1.00 |
| 11.8 | 1.10 |
| 14.0 | 1.20 |
| 16.9 | 1.30 |
| 20.0 | 1.40 |
| 23.7 | 1.60 |
| 28.0 | 1.80 |
| 34.0 | 2.00 |
| 40.2 | 2.20 |
| 47.5 | 2.40 |
| 56.2 | 2.60 |
| 66.5 | 2.80 |
| 80.6 | 3.00 |
| 95.76 | 3.20 |
| 113.0 | 3.30 |
| 133.0 | 3.40 |
| 162.0 | 3.60 |
| 191.0 | 3.80 |
| 226.0 | 4.00 |
| 267.0 | 4.20 |
| 324.0 | 4.40 |
| 383.0 | 4.60 |
| 452.0 | 4.80 |
| 536.0 | 5.00 |
| 634.0 | 5.20 |
| 768.0 | 5.40 |
| 909.0 | 5.50 |

Peak Current Configuration

The peak inductor current limit corresponding to each SIMO output are independently configurable. To set the inductor peak current for the MAX77642, connect the appropriate resistors from RSET_IPK to GND as shown in [Table 10](#). The RSET_IPK resistors should have a 1% or better tolerance. To set the inductor peak current for the MAX77643, use the I²C interface to load the configuration registers CNFG_SBBx_B.IP_SBBx[5:4].

Table 10. Inductor Peak Current Setting

| RSET_IPK (kΩ) | SBB_PK2 (A) | SBB_PK1 (A) | SBB_PK0 (A) |
|---------------|-------------|-------------|-------------|
| Short | 0.5 | 0.5 | 0.5 |
| 4.99 | 0.5 | 0.5 | 1.0 |
| 6.00 | 0.5 | 1.0 | 0.5 |
| 7.15 | 1.0 | 0.5 | 0.5 |
| 8.45 | 1.0 | 1.0 | 0.5 |
| 10.0 | 1.0 | 0.5 | 1.0 |
| 11.8 | 0.5 | 1.0 | 1.0 |
| 14.0 | 1.0 | 1.0 | 1.0 |

SIMO Soft-Start

The soft-start feature of the SIMO limits inrush current during startup. The soft-start feature is achieved by limiting the slew rate of the output voltage during startup (dV/dt_{SS}).

More output capacitance results in higher input current surges during startup. The following equations and example describe the input current surge phenomenon during startup.

In buck-boost mode, the current into the output capacitor (I_{CSBB}) during soft-start is:

$$I_{CSBB} = C_{SBB} \times \frac{dV}{dt_{SS}} \quad \left(\text{Equation 1} \right)$$

where:

- C_{SBB} is the capacitance on the output of the regulator
- dV/dt_{SS} is the voltage change rate of the output

The input current (I_{IN}) during soft-start is:

$$I_{IN} = \frac{(I_{CSBB} + I_{LOAD}) \frac{V_{SBBx}}{V_{IN}}}{\xi} \quad \left(\text{Equation 2} \right)$$

where:

- I_{CSBB} is calculated using Equation 1
- I_{LOAD} is current consumed from the external load
- V_{SBBx} is the output voltage
- V_{IN} is the input voltage
- ξ is the efficiency of the regulator

For example, given the following conditions, the peak input current (I_{IN}) during soft-start is ~71mA:

Given:

- V_{IN} is 3.5V
- V_{SBB2} is 3.3V
- $C_{SBB2} = 10\mu F$
- $dV/dt_{SS} = 5mV/\mu s$
- $R_{LOAD2} = 330\Omega$ ($I_{LOAD2} = 3.3V/330\Omega = 10mA$)
- ξ is 80%

Calculation:

- $I_{CSBB} = 10\mu F \times 5mV/\mu s$ (from Equation 1)
- $I_{CSBB} = 50mA$
- $I_{IN} = \frac{(50mA + 10mA) \frac{3.3V}{3.5V}}{0.85}$ (from Equation 1)
- $I_{IN} \sim 71mA$

SIMO Registers (MAX77643)

Each SIMO buck-boost channel has a dedicated register to program its target output voltage (CNFG_SBBx_A.TV_SBBx[7:0]) and its peak current limit (CNFG_SBBx_B.IP_SBBx[1:0]). Additional controls are available for enabling/disabling the active-discharge resistors (CNFG_SBBx_B.ADE_SBBx), buck-only, boost-only, buck-boost only, and automatic mode (CNFG_SBBx_B.OP_MODE) as well as enabling/disabling the SIMO buck-boost channels (CNFG_SBBx_B.EN_SBBx[2:0]). For a full description of bits, registers, default values, and reset conditions, see the *Register Map*.

SIMO Active Discharge Resistance

Each SIMO buck-boost channel has an active-discharge resistor (R_{AD_SBBx}) that is automatically enabled/disabled based on a CNFG_SBBx_B.ADE_SBBx bit and the status of the SIMO regulator. The active discharge feature may be enabled (CNFG_SBBx_B.ADE_SBBx = 1) or disabled (CNFG_SBBx_B.ADE_SBBx = 0) independently for each SIMO channel. Enabling the active discharge feature helps ensure a complete and timely power down of all system peripherals. If the active-discharge resistor is enabled by default, then the active-discharge resistor is on whenever V_{SYSA} is below $V_{SYSAUVLO}$ and above V_{POR} .

These resistors discharge the output when CNFG_SBBx_B.ADE_SBBx = 1, and their respective SIMO channel is off. If the regulator is forced on through CNFG_SBBx_B.EN_SBBx[2:0] = 0b110 or 0b111, then the resistors do not discharge the output even if the regulator is disabled by the main-bias.

Note that when V_{SYSA} is less than 1.0V, the NMOS transistors that control the active-discharge resistors lose their gate drive and become open.

SIMO Buck Mode (MAX77643)

If the input voltage at IN_SBB never falls below the output voltage of one or more SIMO converter channels, individual channels can be configured to be in buck mode with the CNFG_SBBx_B.OP_MODE bit. In buck mode, when an output needs service, switch M3_x remains closed and M4 remains open (see [Figure 14](#)). Only M1 and M2 are toggled as in a traditional buck converter. Efficiency is boosted due to three major factors:

- Reduced switching loss: Buck mode toggles only two switches versus the four in buck-boost mode. Therefore, there are less switching events during which power is consumed.
- Lower inductor core losses: Inductor current changes from 0A to peak current. The larger the change in current the inductor experiences, the more energy is lost in the inductor core in the form of heat. In buck mode, the peak current can be reduced since less inductor current is needed to support a load. Less inductor current is needed because of direct energy transfer. Direct energy transfer occurs while the inductor is charged, when the input (IN_SBB) is connected directly to the output (SBBx) through the inductor. Therefore, the input not only provides energy to charge the inductor, energy is also supplied to the output capacitor and load devices. Therefore, less current is needed to charge the inductor, which is used to charge the output capacitor in the next switching state.
- Less frequent charging cycles: In buck-boost mode, the output capacitor is charged only while the inductor is being discharged. Again because of direct energy transfer, the output capacitor is charged during both the inductor charge and discharge times. In addition, with the same peak current limit, the inductor charge time is longer with buck mode. Therefore, the output capacitor can support the output voltage longer before needing to be recharged.

Maintain a minimum headroom of 0.7V between IN_SBB and SBBx in buck mode because inductor charge time ($dt = L \times I_{p_SBBx} / (V_{IN_SBB} - V_{SBBx})$) increases as the difference between the IN_SBB and SBBx voltages shrinks. As the inductor current takes longer to reach its peak, the output voltage might take too long to reach its target voltage, and the MAX77643 might trigger a fault flag.

SIMO Boost Mode (MAX77643)

If the input voltage at IN_SBB never rises above the output voltage of one or more SIMO converter channels, individual channels can be configured to be in boost mode with the CNFG_SBBx_B.OP_MODE bit. In boost mode, when an output needs service, switch M1 remains closed and M2 remains open (see [Figure 14](#)). Only M3x and M4 are toggled as in a traditional boost converter. Efficiency is boosted due to three major factors:

- Reduced switching loss: Boost mode toggles only two switches versus the four in buck-boost mode. Therefore, there are less switching events during which power is consumed.
- Lower inductor core losses: Inductor current changes from 0A to peak current. The larger the change in current the inductor experiences, the more energy is lost in the inductor core in the form of heat. In boost mode, the peak current can be reduced since less inductor current is needed to support a load. Less inductor current is needed because of direct energy transfer. Direct energy transfer occurs while the inductor is discharged, when the input (IN_SBB) is connected directly to the output (SBBx) through the inductor. Therefore, the input not only provides energy to charge the inductor, energy is also supplied to the output capacitor and load devices. Therefore, less current is needed to charge the inductor, which is used to charge the output capacitor in the next switching state.
- Less frequent charging cycles: The inductor discharge time is longer with boost mode. Therefore, the output capacitor can support the output voltage longer before needing to be recharged.

Applications Information

SIMO Available Output Current

The available output current on a given SIMO channel is a function of the input voltage, output voltage, the peak current limit setting, and the output current of the other SIMO channels. Maxim offers a calculator found in the design resources tab of the MAX77642/MAX77643's webpage that outlines the available capacity for specific conditions. [Table 11](#) is an extraction from the calculator.

Table 11. SIMO Available Output Current for Common Applications

| PARAMETERS | EXAMPLE 1 | EXAMPLE 2 | EXAMPLE 3 | EXAMPLE 4 | EXAMPLE 5 |
|---------------------|---------------|--------------|----------------|---------------|---------------|
| V _{IN_MIN} | 2.7V | 2.7V | 3.2V | 3.4V | 3.6V |
| R _{L_DCR} | 0.1Ω | 0.1Ω | 0.1Ω | 0.12Ω | 0.12Ω |
| SBB0 | 1.0V at 100mA | 1.0V at 80mA | 1.2V at 50mA | 1.2V at 20mA | 1.2V at 20mA |
| SBB1 | 1.2V at 75mA | 1.2V at 50mA | 2.05V at 100mA | 2.05V at 80mA | 2.05V at 80mA |
| SBB2 | 1.8V at 50mA | 1.8V at 40mA | 3.3V at 30mA | 3.3V at 10mA | 2.05V at 5mA |
| Operating Mode | Buck-Boost | Buck | Buck-Boost | Buck-Boost | Buck |
| I _{P_SBB0} | 1A | 1A | 1A | 0.5A | 1A |
| I _{P_SBB1} | 1A | 1A | 0.75A | 0.5A | 1A |
| I _{P_SBB2} | 1A | 1A | 1A | 0.5A | 0.5A |
| Utilized Capacity | 73% | 77% | 79% | 73% | 79% |

* $ESR_{C_{IN}} = ESR_{C_{OUT}} = 5m\Omega$, $L = 1.5\mu H$

Inductor Selection

Choose an inductance from 1.0μH to 2.2μH; 1.5μH inductors work best for most designs. Larger inductances transfer more energy to the output for each cycle and typically result in larger output voltage ripple and better efficiency. See the [Output Capacitor Selection](#) section for more information on how to size your output capacitor in order to control ripple.

Choose the inductor saturation current to be greater than or equal to the maximum peak current limit setting that is used for all of the SIMO buck-boost channels (I_{P_SBBx}). For example, if SBB0 is set for 0.5A, SBB1 is set for 0.75A, and SBB2 is set for 1.0A, then choose the saturation current to be greater than or equal to 1.0A.

Choose the RMS current rating of the inductor (typically the current at which the temperature rises appreciably) based on the expected load currents for the system. For systems where the expected load currents are not well known, be conservative and choose the RMS current to be greater than or equal to half the higher maximum peak current limit setting [$I_{RMS} \geq \text{MAX} (I_{P_SBB0}, I_{P_SBB1}, I_{P_SBB2}) / 2$]. This is a conservative choice because the SIMO buck-boost regulator implements a discontinuous conduction mode (DCM) control scheme, which returns the inductor current to zero each cycle.

Consider the DC-resistance (DCR), AC-resistance (ACR), and solution size of the inductor. Typically, smaller sized inductors have larger DC-resistance and larger AC-resistance that reduces efficiency and the available output current. Note that many inductor manufacturers have inductor families which contain different versions of core material in order to balance trade-offs between DCR, ACR (i.e., core losses), and component cost. For this SIMO regulator, inductors with the lowest ACR in the 1.0MHz to 2.0MHz region tend to provide the best efficiency.

Input Capacitor Selection

Choose the input bypass capacitance (C_{IN_SBB}) to be 10μF. Larger values of C_{IN_SBB} improve the decoupling for the SIMO regulator.

The C_{IN_SBB} reduces the current peaks drawn from the battery or input power source during SIMO regulator operation and reduces switching noise in the system. The ESR/ESL of the input capacitor should be very low (i.e., $ESR \leq 5m\Omega$ and $ESL \leq 500pH$) for frequencies up to 2MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

To fully utilize the available input voltage range of the SIMO (5.5V, max), use a capacitor with a voltage rating of 6.3V at minimum.

Boost Capacitor Selection

Choose the boost capacitance (C_{BST}) to be 10nF. Smaller values of C_{BST} (< 1nF) result in insufficient gate drive for M3. Larger values of C_{BST} (> 10nF) have the potential to degrade the startup performance. Ceramic capacitors with 0201 or 0402 case size are recommended.

Output Capacitor Selection

Choose each output bypass capacitance (C_{SBBx}) based on the target output voltage ripple (ΔV_{SBBx}). Typical values are 22μF. Larger values of C_{SBBx} improve the output voltage ripple but increase the input surge currents during soft-start and output voltage changes. The output voltage ripple is a function of the inductance (L), the output voltage (V_{SBBx}), and the peak current limit setting (I_{P_SBBx}). See Equation 3 to estimate required, effective capacitance.

$$C_{SBBx} = \frac{I_{P_SBBx}^2 \times L}{2 \times V_{SBBx} \times \Delta V_{SBBx}} \text{(Equation 3)}$$

Maxim also offers a calculator to aid in the selection of the output capacitance found in the design resources tab of the MAX77642/MAX77643 product page. Note that most designs concern themselves with having enough capacitance on the output but there is also a maximum capacitance limitation that is calculated within the SIMO calculator; take care not to exceed the maximum capacitance.

The C_{SBBx} is required to keep the output voltage ripple small. The impedance of the output capacitor (ESR, ESL) should be very low (i.e., $ESR \leq 5m\Omega$ and $ESL \leq 500pH$) for frequencies up to 2MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

A capacitor's effective capacitance decreases with increased DC bias voltage. This effect is more pronounced as capacitor case sizes decrease. Due to this characteristic, it is possible for an 0603 case size capacitor to perform well, while an 0402 case size capacitor of the same value performs poorly. The SIMO regulator is stable with low output capacitance (1μF) but the output voltage ripple would be large; consider the effective output capacitance value after initial tolerance, bias voltage, aging, and temperature derating.

SIMO Switching Frequency

The SIMO buck-boost regulator uses a pulse frequency modulation (PFM) control scheme. The switching frequency for each output is a function of the operating mode, input voltage, output voltage, load current, and inductance. Output capacitance is a minor factor in SIMO switching frequency. Maxim offers a SIMO calculator found in the design resources tab of the MAX77642/MAX77643 product page to estimate expected switching frequency.

[Table 12](#) lists how different factors increase or decrease switching frequency.

Table 12. Switching Frequency Control

| FACTOR | INCREASING FREQUENCY | DECREASING FREQUENCY |
|--------|----------------------|----------------------|
|--------|----------------------|----------------------|

Table 12. Switching Frequency Control (continued)

| | | |
|-----------------------------|----------------------|-------------------------|
| Inductor Current Peak Limit | Lower peak limit | Higher peak limit |
| Operating Mode | Buck-boost mode | Buck mode or boost mode |
| Inductor | Decrease inductance | Increase inductance |
| Output Capacitor | Decrease capacitance | Increase capacitance |
| Input Voltage | Higher voltage | Lower voltage |
| Output Voltage | Higher voltage | Lower voltage |
| Load Current | Higher current | Lower current |

Unused Outputs

Do not leave unused outputs unconnected. If an output left unconnected is accidentally enabled, the charged inductor experiences an open circuit, and the output voltage soars above the absolute maximum rating, damaging the device. If an output is not used, do one of the following:

1. Disable the output (CNFG_SBBx_B.EN_SBBx[2:0] = 0x4 or 0x5) and connect the output to ground. If an unused output is default enabled or can be accidentally enabled, do one of the other recommendations instead.
2. Bypass the unused output with a 1µF capacitor to ground.
3. Connect the unused output to IN_SBB or a different output channel if the unused output is programmed to a lower voltage. Since the output voltage is higher than the unused output, the regulator does not service the unused output even if it is unintentionally enabled.
 - Note that some OTP options have the active-discharge resistors enabled by default. Connecting an unused output to IN_SBB is **not recommended** if the active discharge is enabled by default. If connecting the unused output to a different channel, disable the active-discharge resistor (CNFG_SBBx_B.ADE_SBBx = 0) of the unused channel.

PCB Layout Guide**Capacitors**

Place decoupling capacitors as close as possible to the IC such that connections from capacitor pads to pin and from capacitor pads to ground pins are short. Keeping the connections short lowers parasitic inductance and resistance, improving performance and shrinking the physical size of hot loops.

If connections to the capacitors are through vias, use multiple vias to minimize parasitics. Also, connect loads to the capacitor pads rather than the device pins.

Most critical are the capacitors for the switching regulator: input capacitor at IN_SBB and output capacitors at SBBx.

Input Capacitor at IN_SBB

Minimize the parasitic inductance from PGND to input capacitor to IN_SBB to reduce ringing on the LXA voltage.

Output Capacitors at SBBx

The output capacitors experience large changes in current as the regulator charges (buck mode) and discharges (both modes) the inductor. In buck mode, the capacitor current ramps up at the same rate as mentioned in the [Input Capacitor at IN_SBB](#) section. In buck-boost mode, the capacitor current ramps up very quickly. In both modes, the capacitor current ramps down at a rate of $\frac{dI_{C_SBBx}}{dt} = \frac{V_{SBBx}}{L}$ from inductor peak current. Since the ramp down can occur in less than 1µs, and the current increases rapidly for buck-boost mode, minimize parasitic inductance from SBBx to output capacitor to PGND.

Inductor

Keep the inductor close to the IC to reduce trace resistance; however, prioritize any regulator input/output capacitors over the inductor. Use the appropriate trace width from LXA to inductor to LXB to support the peak inductor current. Likewise, if there are vias in the path, use an appropriate amount of vias to support the peak current.

Ground Connections

As the switching regulator charges and discharges the inductor, current flows from PGND to the input capacitor ground, from output capacitor ground to PGND, or from output capacitor ground to input capacitor ground. Therefore, use a wide, continuous copper plane to connect PGND to the capacitor grounds.

When connecting the GND and PGND pins together, ensure noise from the power ground does not enter the analog ground (where GND is connected). For example, assuming the ground pins are connected through a solid ground plane on an internal layer, one via connecting GND to the internal ground plane may be sufficient to protect GND from most of the noise in the power-ground plane. Likewise, if there are other higher current or noisy circuitry near this device, avoid connecting the GND pin directly to their grounds.

For more guidelines on proper grounding, visit: <https://www.maximintegrated.com/en/design/partners-and-technology/design-technology/ground-layout-board-designers.html>.

Example PCB Layout

Figure 15 shows an example layout of the top layer.

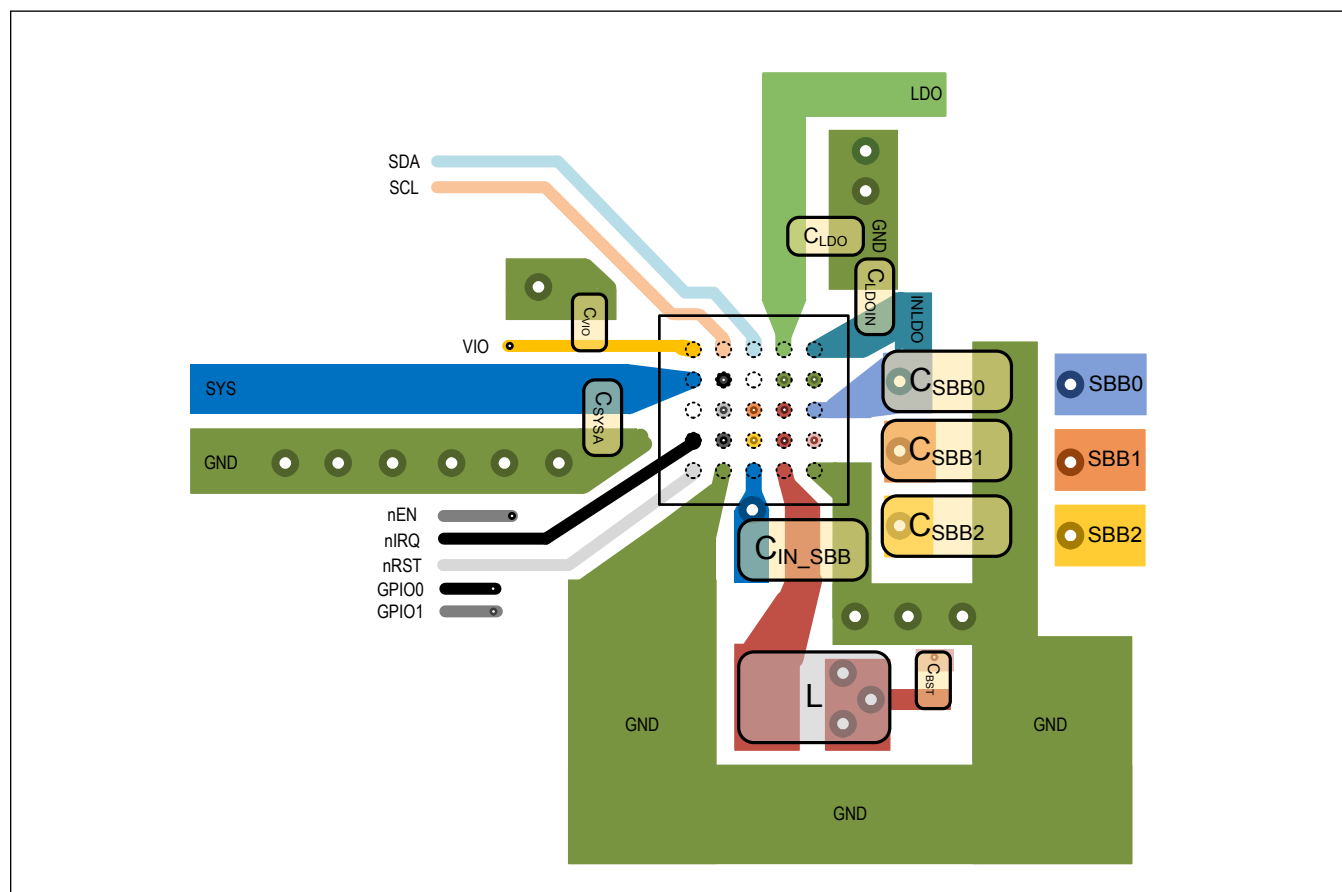


Figure 15. PCB Top-Layer and Component Placement Example

Detailed Description—Low Dropout Linear Regulator (LDO)/Load Switch (LSW)

The device includes an on-chip low-dropout linear regulator (LDO0) that can also be configured as load switches. The LDO is optimized to have low-quiescent current. The input voltage range (V_{IN_LDO}) allows it to be powered directly from the main energy source such as a Li-Poly battery or from an intermediate regulator. The linear regulator delivers up to 150mA.

Features and Benefits

- 1x 150mA LDO
- LDO Input Voltage Range: 1.71V to 5.5V
- LSW Input Voltage Range: 1.20V to 5.5V
- Resistor Adjustable Output Voltage (MAX77642)
- I²C Adjustable Output Voltage (MAX77643)
- 100mV Maximum Dropout Voltage at ECT Conditions
- Programmable On-Chip Active Discharge

LDO/LSW Simplified Block Diagram

The LDO/LSW block has one input (IN_LDO) and one output (LDO) and several ports that exchange information with the rest of the device (V_{REF} , EN_LDO, ADE_LDO). The V_{REF} comes from the main bias circuits. The CNFG_LDO0_B.EN_LDO and CNFG_LDO0_B.ADE_LDO are register bits for controlling the enable and active-discharge feature, respectively. See the *Register Map* for more information.

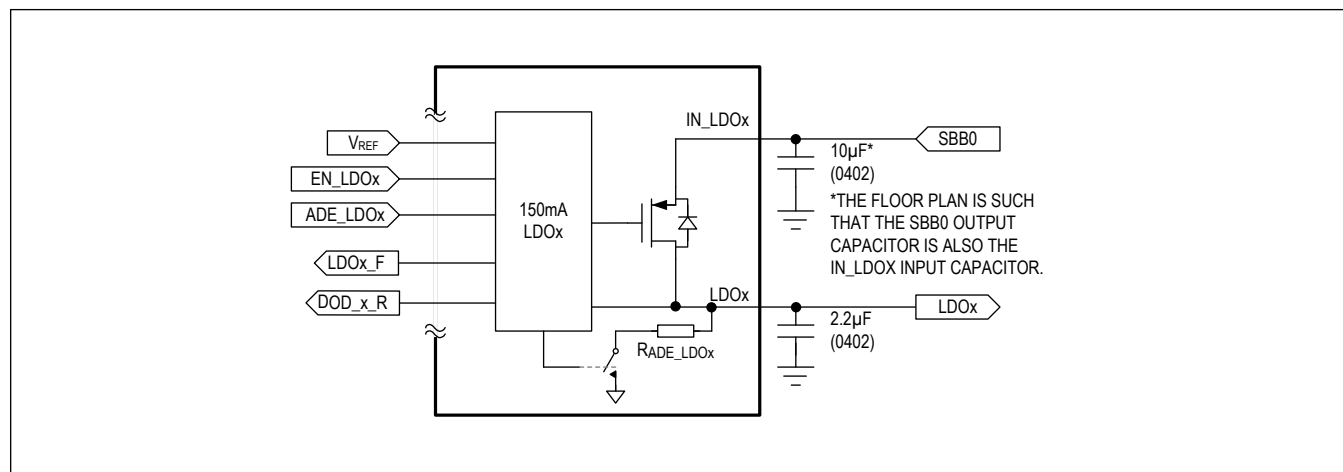


Figure 16. LDO Simplified Block Diagram

LDO Output Voltage Configuration

To set the output voltages for the on-chip LDO for the MAX77642, connect the appropriate resistor from RSET_LDO to GND as shown in [Table 13](#). RSET_LDO resistor should have 1% or better tolerance. To set the output voltages for the on-chip LDO for the MAX77643, use the I²C interface to load the configuration register TV_LDO[7:0]. TV_LDO[7] is used to enable (TV_LDO[7] = 1) or disabled (TV_LDO[7] = 0) a 1.325mV offset to the LDO's output voltage. The bits TV_LDO[6:0] are used to set the output voltage as:

$$LDO = 0.5V + TV_LDO[7] + (25mV \times TV_LDO[6:0] \text{ (decimal)})$$

Table 13. LDO Output Voltage Setting

| RSET_LDO (k Ω) | LDO OUTPUT VOLTAGE (V) |
|------------------------|------------------------|
| Short | 0.50 |
| 4.99 | 0.60 |
| 6.00 | 0.70 |
| 7.15 | 0.80 |
| 8.45 | 0.90 |
| 10.0 | 0.95 |
| 11.8 | 1.00 |
| 14.0 | 1.05 |
| 16.9 | 1.10 |
| 20.0 | 1.15 |
| 23.7 | 1.20 |
| 28.0 | 1.25 |
| 34.0 | 1.30 |
| 40.2 | 1.40 |
| 47.5 | 1.50 |
| 56.2 | 1.60 |
| 66.5 | 1.70 |
| 80.6 | 1.80 |
| 95.76 | 1.90 |
| 113.0 | 2.00 |
| 133.0 | 2.10 |
| 162.0 | 2.20 |
| 191.0 | 2.40 |
| 226.0 | 2.50 |
| 267.0 | 2.60 |
| 324.0 | 2.80 |
| 383.0 | 3.00 |
| 452.0 | 3.20 |
| 536.0 | 3.40 |
| 634.0 | 3.60 |
| 768.0 | 3.80 |
| 909.0 | 4.00 |

LDO/LSW Active-Discharge Resistor

The LDO/LSW block has an active-discharge resistor (R_{AD_LDO}) that is enabled if $CNFG_LDO0_B.ADE_LDO = 1$ and LDO is disabled. Enabling the active discharge feature helps ensure a complete and timely power down of the resource. During power up, if $V_{SYSA} > V_{POR}$ and $CNFG_LDO_B.ADE_LDO = 1$, the active-discharge resistor is enabled.

LDO/LSW Soft-Start

The soft-start feature limits inrush current during startup, and is achieved by limiting the slew rate of the output voltage during startup (dV_{OUT_LDO}/dt_{SS}).

More output capacitance results in higher input current surges during startup. The following equation and example describe the input current surge phenomenon during startup.

The input current (I_{IN_LDO}) during soft-start is calculated as:

$$I_{IN_LDO} = C_{LDO} \frac{dV_{OUT_LDO}}{dt_{SS}} + I_{OUT_LDO}$$

where:

- C_{LDO} is the capacitance on the output of the regulator
- dV_{OUT_LDO}/dt_{SS} is the voltage change rate of the output

For example, given the following conditions, the input current (I_{IN_LDO}) during soft-start is 13.08mA:

Given:

- $C_{LDO} = 2.2\mu F$
- $dV_{OUT_LDO}/dt_{SS} = 2.2mV/\mu s$
- LDO programmed to 1.85V
- $R_{LDO} = 185\Omega$ ($I_{OUT_LDO} = 1.85V/185\Omega = 10mA$)

Calculation:

- $I_{IN} = 2.2\mu F \times 2.2mV/\mu s + 10mA$
- $I_{IN} = 14.84mA$

Load Switch Configuration

The LDO0 can be configured as load switches with the CNFG_LDO0_B.LDO_MD bit. As shown in [Figure 17](#), the transition from LDO to LSW mode is controlled by a defined slew rate until dropout is detected. Once dropout is detected, the load switch is fully closed and the dropout interrupt flag (INT_GLBL.DOD_R) is set.

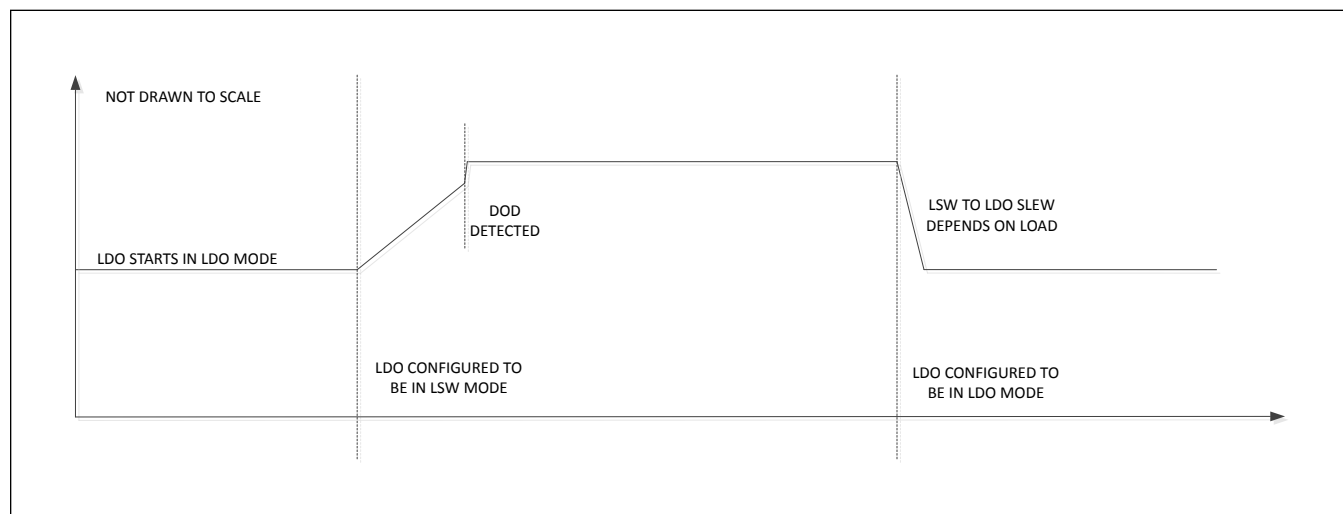


Figure 17. LDO to LSW Transition Waveform

Applications Information

Input Capacitor Selection

Make sure the input bypass capacitance (C_{IN_LDO}) is at least $2.2\mu\text{F}$. Larger values of C_{IN_LDO} improve the decoupling for LDO. The floor plan of the device is such that SBB0 is adjacent to IN_LDO and if the S1MO channel 0 output powers the input of LDO, then its output capacitor (C_{SBB0}) can also serve as C_{IN_LDO} such that only one capacitor is required.

The C_{IN_LDO} reduces the current peaks drawn from the battery or input power source during operation. The impedance of the input capacitor (ESR, ESL) should be very low (i.e., $\text{ESR} \leq 50\text{m}\Omega$ and $\text{ESL} \leq 5\text{nH}$) for frequencies up to 0.5MHz . Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

Output Capacitor Selection

For both LDO and LSW modes, choose the output bypass capacitance (C_{LDO}) to be $1\mu\text{F}$.

In LDO mode, larger values of C_{LDO} improve output PSRR but increase input surge currents during soft-start and output voltage changes. The effective output capacitance should not exceed $2.8\mu\text{F}$ to maintain stability.

While in LDO mode, C_{LDO} is required to keep stability. The series inductance of the output capacitor and its series resistance should be low (i.e., $\text{ESR} \leq 10\text{m}\Omega$ and $\text{ESL} \leq 1\text{nH}$) for frequencies up to 0.5MHz . Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

A capacitor's effective capacitance decreases with increased DC bias voltage. This effect is more pronounced with smaller capacitor case sizes. Due to this characteristic, 0603 case size capacitors tend to perform well while 0402 case size capacitors of the same value perform poorly.

Detailed Description—I²C Serial Communication

General Description

The IC features a revision 3.0 I²C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). This device acts as a slave-only device, relying on the master to generate a clock signal. SCL clock rates from 0Hz to 3.4MHz are supported.

The I²C is an open-drain bus and therefore SDA and SCL require pullups. Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus signals.

[Figure 18](#) shows the functional diagram for the I²C-based communications controller. For additional information on I²C, refer to the *I²C Bus Specification and User Manual* which is available for free through the internet.

Features

- I²C Revision 3.0 Compatible Serial Communications Channel
- 0Hz to 100kHz (Standard Mode)
- 0Hz to 400kHz (Fast Mode)
- 0Hz to 1MHz (Fast-Mode Plus)
- 0Hz to 3.4MHz (High-Speed Mode)
- Does not utilize I²C Clock Stretching

I²C Simplified Block Diagram

There are three pins (aside from GND) for the I²C-compatible interface. The V_{IO} determines the logic level, SCL is the clock line, and SDA is the data line. Note that the interface does **not** have the ability to drive the SCL line.

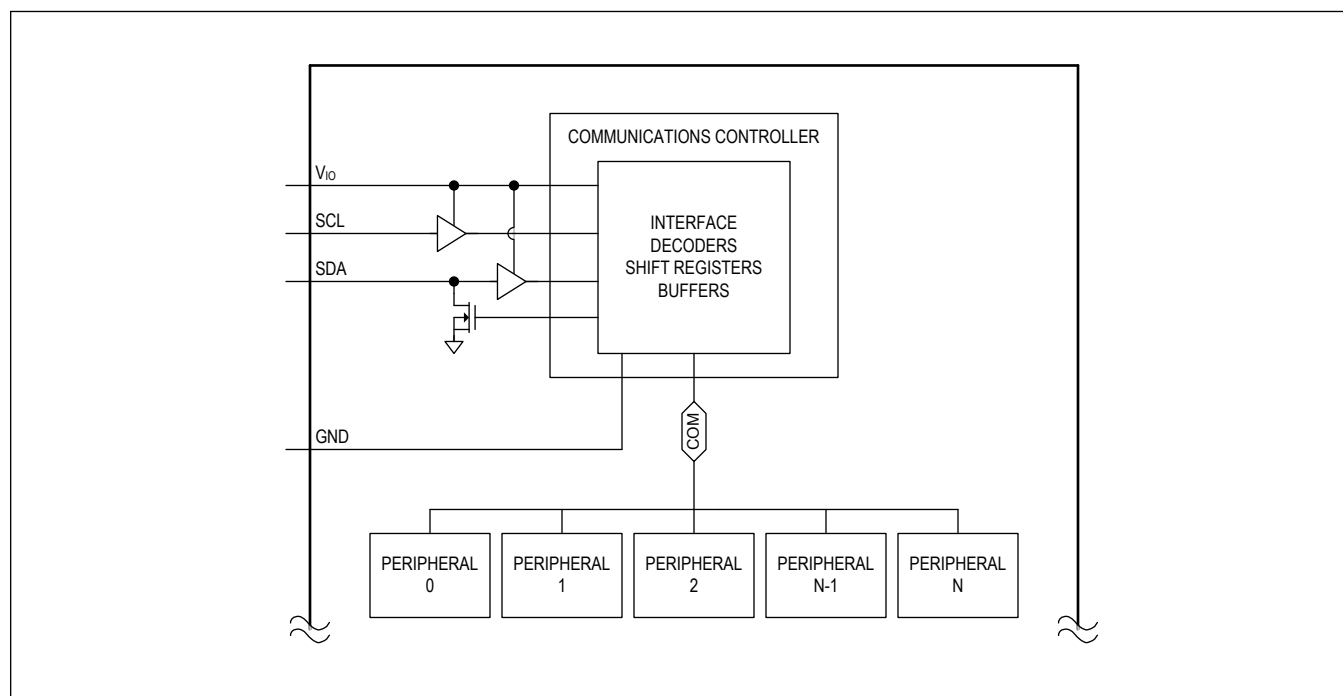


Figure 18. I²C Simplified Block Diagram

I²C System Configuration

The I²C-compatible interface is a multimaster bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

A device on the I²C bus that sends data to the bus is called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates the SCL clock signals to control the data transfer is a master. Any device that is being addressed by the master is considered a slave. The I²C-compatible interface operates as a slave on the I²C bus with transmit and receive capabilities.

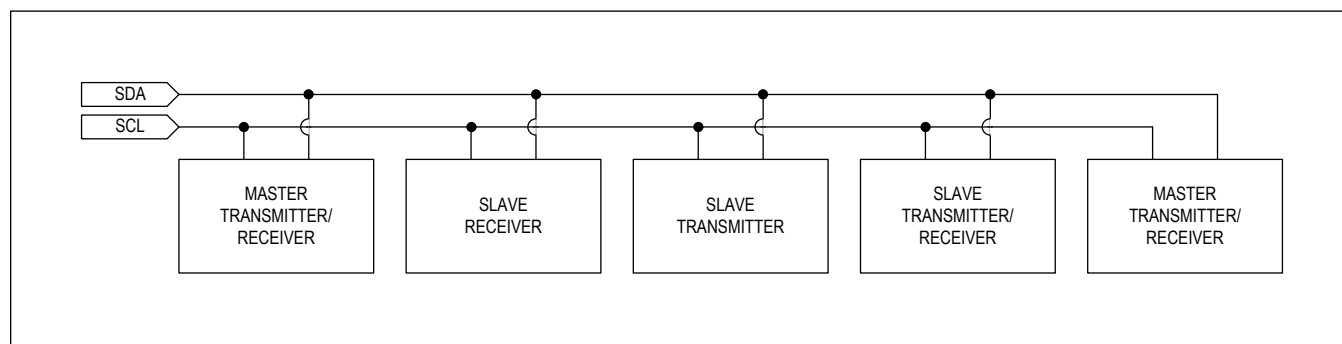


Figure 19. I²C System Configuration

I²C Interface Power

The I²C interface derives its power from V_{IO} . Typically a power input such as V_{IO} would require a local 0.1 μ F ceramic bypass capacitor to ground. However, in highly integrated power distribution systems, a dedicated capacitor might not be necessary. If the impedance between V_{IO} and the next closest capacitor ($\geq 0.1\mu$ F) is less than 100m Ω in series with 10nH, then a local capacitor is not needed. Otherwise, bypass V_{IO} to GND with a 0.1 μ F ceramic capacitor.

The V_{IO} accepts voltages from 1.7V to 3.6V (V_{IO}). Cycling V_{IO} does not reset the I²C registers. When V_{IO} is less than V_{IOUVLO} and V_{SYSA} is less than $V_{SYSAUVLO}$, SDA and SCL are high impedance.

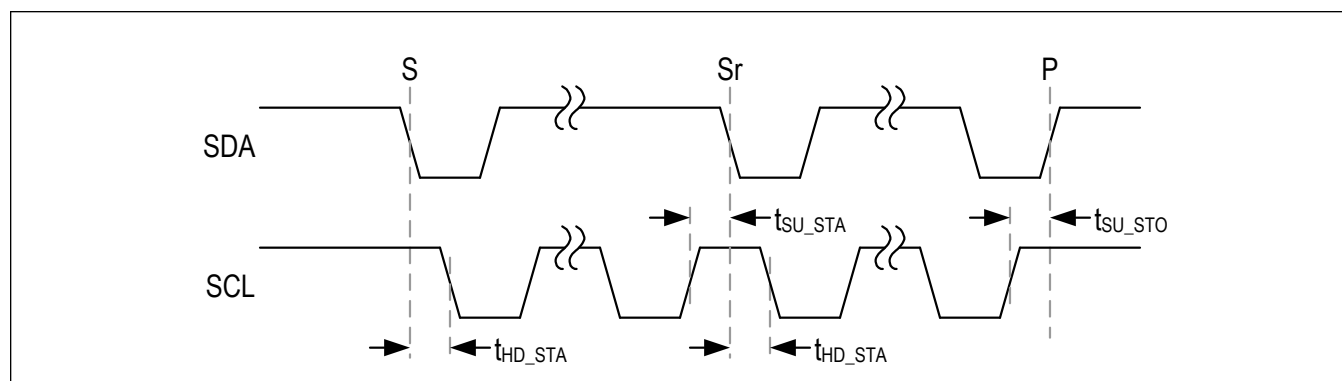
I²C Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals. See the [I²C Start and Stop Conditions](#) section. Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each data packet is 9 bits long: 8 bits of data followed by the acknowledge bit. Data is transferred with the MSB first.

I²C Start and Stop Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high. See [Figure 20](#).

A START condition from the master signals the beginning of a transmission to the device. The master terminates transmission by issuing a not-acknowledge followed by a STOP condition (see the [I²C Acknowledge Bit](#) section for information on not-acknowledge). The STOP condition frees the bus. To issue a series of commands to the slave, the master can issue repeated start (Sr) commands instead of a STOP command to maintain control of the bus. In general a repeated start command is functionally equivalent to a regular start command.

Figure 20. I²C Start and Stop Conditions

I²C Acknowledge Bit

Both the I²C bus master and slave devices generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each 9-bit data packet. To generate an acknowledge (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. See [Figure 21](#). To generate a not-acknowledge (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

This device issues an ACK for all register addresses in the possible address space even if the particular register does not exist.

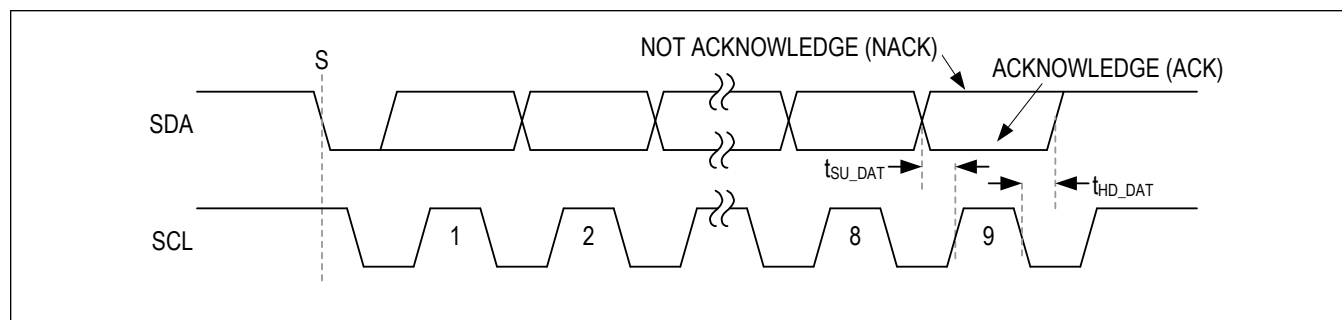


Figure 21. Acknowledge Bit

I2C Slave Address

The I2C controller implements 7-bit slave addressing. An I2C bus master initiates communication with the slave by issuing a START condition followed by the slave address. See [Figure 22](#). The OTP address is factory-programmable for one of two options. See [Table 14](#). All slave addresses not mentioned in [Table 14](#) are not acknowledged.

Table 14. I2C Slave Address Options

| ADDRESS | 7-BIT SLAVE ADDRESS | 8-BIT WRITE ADDRESS | 8-BIT READ ADDRESS |
|--------------------------|---------------------|---------------------|--------------------|
| Main Address (ADDR = 0)* | 0x40, 0b 100 0000 | 0x80, 0b 1000 0000 | 0x81, 0b 1000 0001 |
| Main Address (ADDR = 1)* | 0x48, 0b 100 1000 | 0x90, 0b 1001 0000 | 0x91, 0b 1001 0001 |
| Main Address (ADDR = 2)* | 0x44, 0b 100 0100 | 0x88, 0b 1000 1000 | 0x89, 0b 1000 1001 |
| Main Address (ADDR = 3)* | 0x4C, 0b 100 1100 | 0x98, 0b 1001 1000 | 0x99, 0b 1001 1001 |
| Test Mode** | 0x49, 0b 100 1001 | 0x92, 0b 1001 0010 | 0x93, 0b 1001 0011 |

*Perform all reads and writes on the main address. The ADDR is a factory one-time programmable (OTP) option, allowing for address changes in the event of a bus conflict.

**When test mode is unlocked, the additional address is acknowledged. Test mode details are confidential. If possible, leave the test mode address unallocated to allow for the rare event that debugging needs to be performed in cooperation with Maxim.

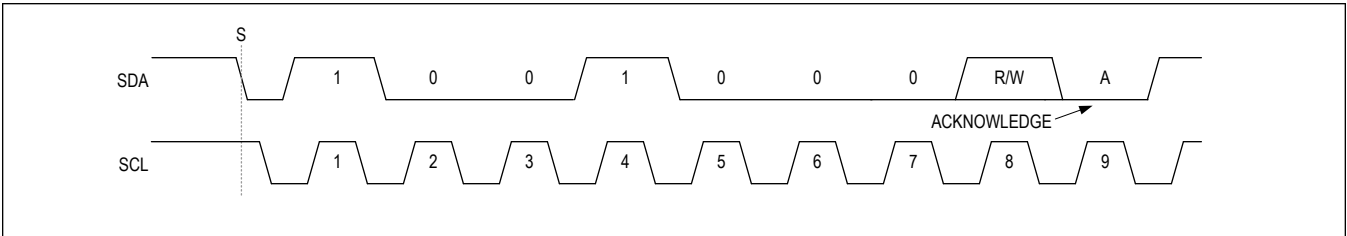


Figure 22. Slave Address Example

I2C Clock Stretching

In general, the clock signal generation for the I2C bus is the responsibility of the master device. The I2C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The IC does not use any form of clock stretching to hold down the clock line.

I2C General Call Address

This device does not implement the I2C specifications general call address and does not acknowledge the general call address (0b0000_0000).

I2C Device ID

This device does not support the I2C Device ID feature.

I²C Communication Speed

This device is compatible with all four communication speed ranges as defined by the revision 3.0 I²C specification:

- 0Hz to 100kHz (Standard Mode)
- 0Hz to 400kHz (Fast Mode)
- 0Hz to 1MHz (Fast-Mode Plus)
- 0Hz to 3.4MHz (High-Speed Mode)

Operating in standard mode, fast mode, and fast-mode plus does not require any special protocols. The main consideration when changing bus speed through this range is the combination of the bus capacitance and pullup resistors. Larger values of bus capacitance and pullup resistance increase the time constant ($C \times R$), slowing bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the *Pullup Resistor Sizing* section of the I²C bus specification and user manual (available for free on the internet) for detailed guidance on the pullup resistor selection. In general for bus capacitances of 200pF, a 100kHz bus needs 5.6k Ω pullup resistors, a 400kHz bus needs about 1.5k Ω pullup resistors, and a 1MHz bus needs 680 Ω pullup resistors. Remember that, while the open-drain bus is low, the pullup resistor is dissipating power, and lower value pullup resistors dissipate more power (V^2/R).

Operating in high-speed mode requires some special considerations. For a full list of considerations, refer to the publicly available I²C bus specification and user manual. Major considerations with respect to this part are:

- The I²C bus master uses current source pullups to shorten the signal rise.
- The I²C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each stop condition, the bus input filters are set for standard mode, fast mode, and fast-mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the [I²C Communication Protocols](#) section.

I²C Communication Protocols

Both writing to and reading from registers are supported as described in the following subsections.

Writing to a Single Register

[Figure 23](#) shows the protocol for the I²C master device to write one byte of data to this device. This protocol is the same as the SMBus specification's write byte protocol.

The write byte protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit ($R/W = 0$).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave updates with the new data.
8. The slave asserts an acknowledge or not acknowledge for the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
9. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

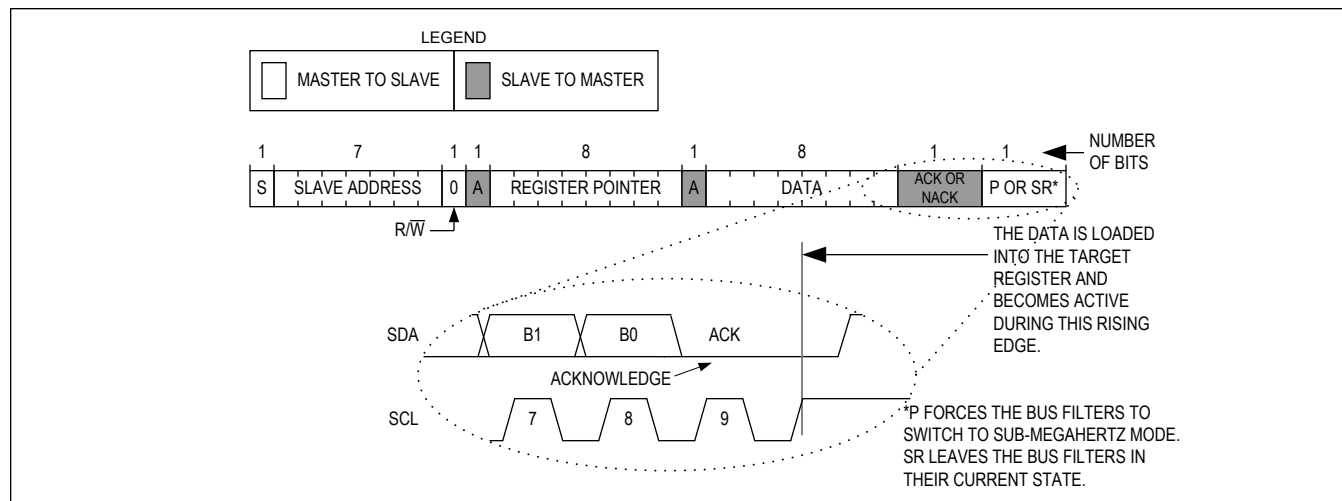


Figure 23. Writing to a Single Register with the Write Byte Protocol

Writing Multiple Bytes to Sequential Registers

Figure 24 shows the protocol for writing to sequential registers. This protocol is similar to the write byte protocol in the [Writing to a Single Register](#) section, except the master continues to write after it receives the first byte of data. When the master is done writing, it issues a stop or repeated start.

The write to sequential registers protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
8. Steps 6 to 7 are repeated as many times as the master requires.
9. During the last acknowledge related clock pulse, the master can issue an acknowledge or a not acknowledge.
10. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

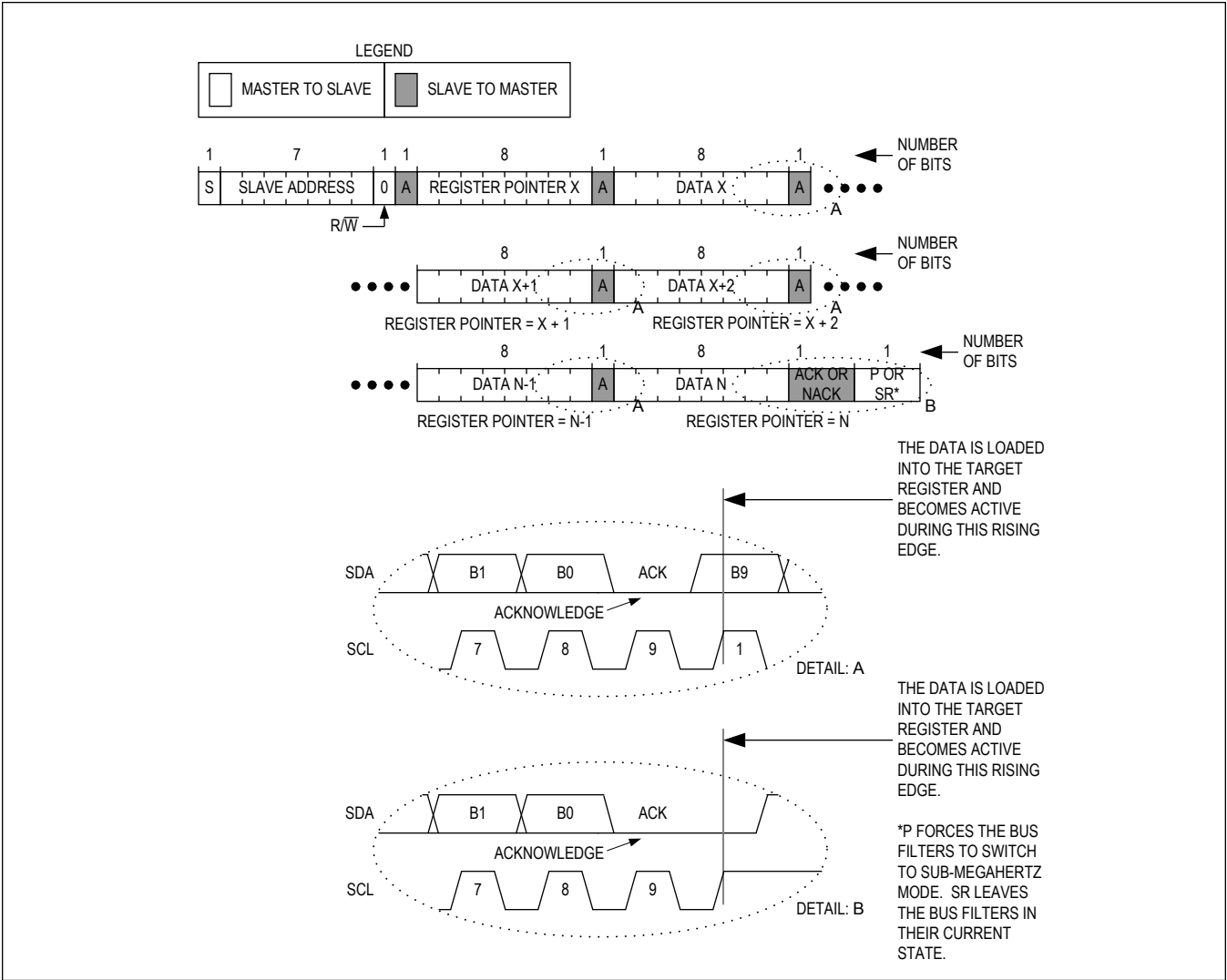


Figure 24. Writing to Sequential Registers X to N

Reading from a Single Register

Figure 25 shows the protocol for the I²C master device to read one byte of data. This protocol is the same as the SMBus specification's read byte protocol.

The read byte protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a repeated start command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/W = 1).
8. The addressed slave asserts an acknowledge by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues a not acknowledge (nA).
11. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when this device receives a stop, the register pointer is not modified. Therefore, if the master re-reads the same register, it can immediately send another read command, omitting the command to send a register pointer.

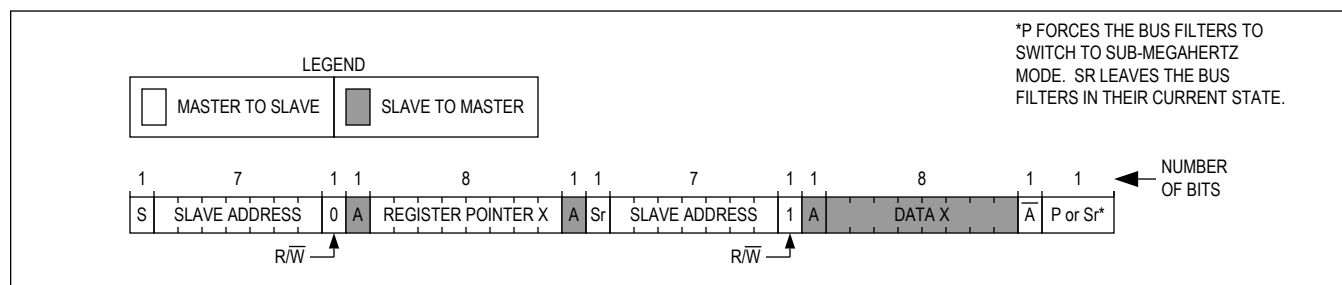


Figure 25. Reading from a Single Register with the Read Byte Protocol

Reading from Sequential Registers

Figure 26 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except the master issues an acknowledge to signal the slave that it wants more data. When the master has all the data it requires, it issues a not acknowledge (nA) and a stop (P) to end the transmission. The continuous read from sequential registers protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a repeated start command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/W = 1).
8. The addressed slave asserts an acknowledge by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues an acknowledge (A) signaling the slave that it wishes to receive more data.
11. Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a not acknowledge (nA) to signal that it wishes to stop receiving data.
12. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a stop (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when this device receives a stop, it does not modify its register pointer. Therefore, if the master re-reads the same register, it can immediately send another read command, omitting the command to send a register pointer.

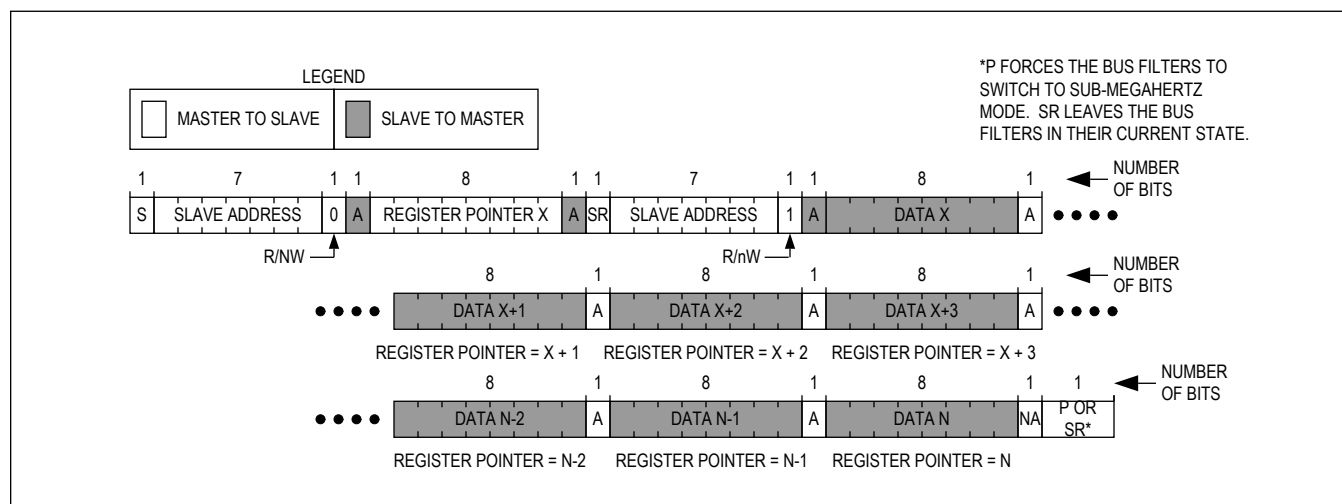


Figure 26. Reading Continuously from Sequential Registers X to N

Engaging HS-Mode for Operation up to 3.4MHz

[Figure 27](#) shows the protocol for engaging HS-mode operation. HS-mode operation allows for a bus operating speed up to 3.4MHz. The engaging HS-mode protocol is as follows:

1. Begin the protocol while operating at a bus speed of 1MHz or lower.
2. The master sends a start command (S).
3. The master sends the 8-bit master code of 0b0000 1XXX where 0bXXX are don't care bits.
4. The addressed slave issues a not acknowledge (nA).
5. The master can increase its bus speed up to 3.4MHz and issue any read/write operation.

The master may continue to issue high-speed read/write operations until a stop (P) is issued. To continue operations in high-speed mode, use repeated start (Sr)

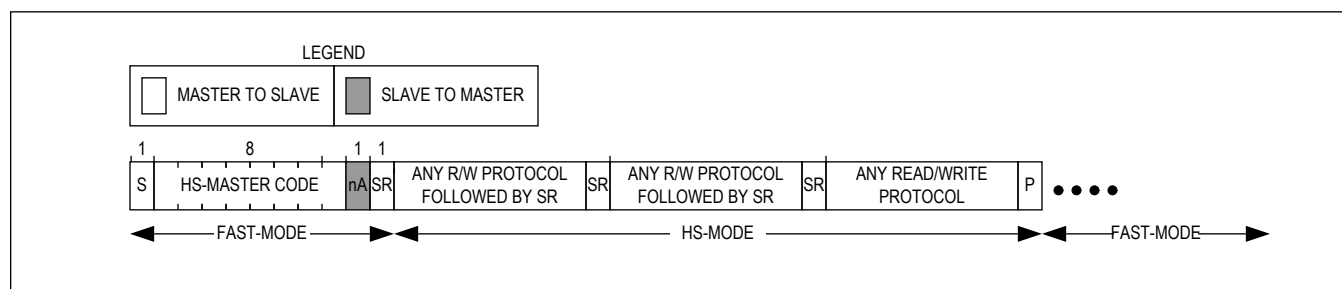


Figure 27. Engaging HS Mode

Register Map

MAX77643

| ADDRESS | NAME | MSB | | | | | | | LSB |
|---------|--------------------------------------|------------------|---------------|----------------|---------------|--------------|------------------|---------------|--------------|
| Global | | | | | | | | | |
| 0x00 | INT_GLBL0[7:0] | RSVD | DOD_R | TJAL2_R | TJAL1_R | nEN_R | nEN_F | GPI0_R | GPI0_F |
| 0x01 | INT_GLBL1[7:0] | RSVD | RSVD | LDO_F | SBB2_F | SBB1_F | SBB0_F | GPI1_R | GPI1_F |
| 0x02 | ERCFLAG[7:0] | SBB_FA ULT_F | WDT_EX P_F | SFT_CR ST_F | SFT_OF F_F | MRST_F | INUVLO | INOVLO | TOVLD |
| 0x03 | STAT_GLBL[7:0] | DIDM | BOK | RSVD | DOD_S | TJAL2_S | TJAL1_S | STAT_E N | STAT_IR Q |
| 0x04 | INTM_GLBL0[7:0] | RSVD | DOD_R M | TJAL2_R M | TJAL1_R M | nEN_RM | nEN_FM | GPI0_R M | GPI0_F M |
| 0x05 | INTM_GLBL1[7:0] | RSVD | RSVD | LDO_M | SBB2_F M | SBB1_F M | SBB0_F M | GPI1_R M | GPI1_F M |
| 0x06 | CNFG_GLBL0[7:0] | PU_DIS | MRST | SBIA_LP M | nEN_MODE[1:0] | | DBEN_n EN | SFT_CTRL[1:0] | |
| 0x07 | CNFG_GLBL1[7:0] | RSVD[4:0] | | | | | SBB_F_ SHUTDN | AUTO_WKT[1:0] | |
| 0x08 | CNFG_GPIO0[7:0] | RSVD[1:0] | | ALT_GPI O0 | DBEN_G PI | DO | DRV | DI | DIR |
| 0x09 | CNFG_GPIO1[7:0] | RSVD[1:0] | | ALT_GPI O1 | DBEN_G PI | DO | DRV | DI | DIR |
| 0x10 | CID[7:0] | – | – | – | CID[4:0] | | | | |
| 0x17 | CNFG_WDT[7:0] | RSVD[1:0] | | WDT_PER[1:0] | | WDT_M ODE | WDT_CL R | WDT_E N | WDT_LO CK |
| SBB | | | | | | | | | |
| 0x28 | CNFG_SBB_TOP[7:0] | DIS_LP M | – | – | – | – | – | DRV_SBB[1:0] | |
| 0x29 | CNFG_SBB0_A[7:0] | TV_SBB0[7:0] | | | | | | | |
| 0x2A | CNFG_SBB0_B[7:0] | OP_MODE[1:0] | | IP_SBB0[1:0] | | ADE_SB B0 | EN_SBB0[2:0] | | |
| 0x2B | CNFG_SBB1_A[7:0] | TV_SBB1[7:0] | | | | | | | |
| 0x2C | CNFG_SBB1_B[7:0] | OP_MODE[1:0] | | IP_SBB1[1:0] | | ADE_SB B1 | EN_SBB1[2:0] | | |
| 0x2D | CNFG_SBB2_A[7:0] | TV_SBB2[7:0] | | | | | | | |
| 0x2E | CNFG_SBB2_B[7:0] | OP_MODE[1:0] | | IP_SBB2[1:0] | | ADE_SB B2 | EN_SBB2[2:0] | | |
| 0x2F | CNFG_DVS_SBB0_A[7:0] | TV_SBB0_DVS[7:0] | | | | | | | |
| LDO | | | | | | | | | |
| 0x38 | CNFG_LDO0_A[7:0] | TV_OFS _LDO | TV_LDO[6:0] | | | | | | |
| 0x39 | CNFG_LDO0_B[7:0] | RSVD[2:0] | | | LDO_MD | ADE_LD O | EN_LDO[2:0] | | |

Register Details

[INT_GLBL0 \(0x00\)](#)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Field | RSVD | DOD_R | TJAL2_R | TJAL1_R | nEN_R | nEN_F | GPI0_R | GPI0_F |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--|
| RSVD | 7 | RSVD | |
| DOD_R | 6 | LDO Dropout Detector Rising Interrupt | 0b0 = The LDO has not detected dropout since the last time this bit was read. 0b1 = The LDO has detected dropout since the last time this bit was read. |
| TJAL2_R | 5 | Thermal Alarm 2 Rising Interrupt | 0b0 = The junction temperature has not risen above TJAL2 since the last time this bit was read. 0b1 = The junction temperature has risen above TJAL2 since the last time this bit was read. |
| TJAL1_R | 4 | Thermal Alarm 1 Rising Interrupt | 0b0 = The junction temperature has not risen above TJAL1 since the last time this bit was read. 0b1 = The junction temperature has risen above TJAL1 since the last time this bit was read. |
| nEN_R | 3 | nEN Rising Interrupt | 0b0 = No nEN rising edges have occurred since the last time this bit was read. 0b1 = A nEN rising edge has occurred since the last time this bit was read. |
| nEN_F | 2 | nEN Falling Interrupt | 0b0 = No nEN falling edges have occurred since the last time this bit was read. 0b1 = A nEN falling edge occurred since the last time this bit was read. |
| GPI0_R | 1 | GPI Rising Interrupt Note that "GPI" refers to the GPIO programmed to be an input. | 0b0 = No GPI rising edges have occurred since the last time this bit was read. 0b1 = A GPI rising edge has occurred since the last time this bit was read. |
| GPI0_F | 0 | GPI Falling Interrupt Note that the GPI is the GPIO programmed to be an input. | 0b0 = No GPI falling edges have occurred since the last time this bit was read. 0b1 = A GPI falling edge has occurred since the last time this bit was read. |

[INT_GLBL1 \(0x01\)](#)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Field | RSVD | RSVD | LDO_F | SBB2_F | SBB1_F | SBB0_F | GPI1_R | GPI1_F |
| Reset | 0b000 | 0b000 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All |
| BITFIELD | BITS | DESCRIPTION | | | DECODE | | | |
| RSVD | 7 | Reserved. Unutilized bit. Write to 0. Reads are don't care. | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|---|
| RSVD | 6 | Reserved. Unutilized bit. Write to 0. Reads are don't care. | |
| LDO_F | 5 | LDO Fault Interrupt | 0b0 = No fault has occurred on LDO since the last time this bit was read. 0b1 = LDO has fallen out of regulation since the last time this bit was read. |
| SBB2_F | 4 | SBB2 Fault Indicator | 0b0 = No fault has occurred on SBB2 since the last time this bit was read. 0b1 = SBB2 has fallen out of regulation since the last time this bit was read. |
| SBB1_F | 3 | SBB1 Fault Indicator | 0b0 = No fault has occurred on SBB1 since the last time this bit was read. 0b1 = SBB1 has fallen out of regulation since the last time this bit was read. |
| SBB0_F | 2 | SBB0 Fault Indicator | 0b0 = No fault has occurred on SBB0 since the last time this bit was read. 0b1 = SBB0 has fallen out of regulation since the last time this bit was read. |
| GPI1_R | 1 | GPI1 Rising Interrupt Note that "GPI" refers to the GPIO programmed to be an input. | 0b0 = No GPI1 rising edges have occurred since the last time this bit was read. 0b1 = A GPI1 rising edge has occurred since the last time this bit was read. |
| GPI1_F | 0 | GPI1 Falling Interrupt Note that the GPI is the GPIO programmed to be an input. | 0b0 = No GPI1 falling edges have occurred since the last time this bit was read. 0b1 = A GPI1 falling edge has occurred since the last time this bit was read. |

ERCFLAG (0x02)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| Field | SBB_FAULT_F | WDT_EXP_F | SFT_CRST_F | SFT_OFF_F | MRST_F | INUVLO | INOVLO | TOVLD |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------|------|---|---|
| SBB_FAULT_F | 7 | SBBx Fault and Shutdown Flag. This bit sets when a SBBx fault and consequent SBBx shutdown occurs. | 0b0 = No SBB shutdown occurred since the last time this bit was read. 0b1 = SBBx fault and SBB shutdown occurred since the last time this bit was read. |
| WDT_EXP_F | 6 | Watchdog Timer OFF or RESET Flag. This bit sets when the watchdog timer expires and causes a power-off or a reset; based on WDT_MODE bitfield setting. | 0b0 = Watchdog timer has not caused a power-off or reset since the last time this bit was read. 0b1 = Watchdog timer has expired and caused a power-off or reset since the last time this bit was read. |
| SFT_CRST_F | 5 | Software Cold Reset Flag | 0b0 = The software cold reset has not occurred since the last read of this register. 0b1 = The software cold reset has occurred since the last read of this register. This indicates that software has set SFT_CTRL[1:0] = 0b01. |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------|------|--------------------------------|--|
| SFT_OFF_F | 4 | Software OFF Flag | 0b0 = The SFT_OFF function has not occurred since the last read of this register. 0b1 = The SFT_OFF function has occurred since the last read of this register. This indicates that software has set SFT_CTRL[1:0] = 0b10. |
| MRST_F | 3 | Manual Reset Timer | 0b0 = A manual reset has not occurred since the last read of this register. 0b1 = A manual reset has occurred since the last read of this register. |
| INUVLO | 2 | IN Domain Undervoltage Lockout | 0b0 = The IN domain undervoltage lockout has not occurred since the last read of this register. 0b1 = The IN domain undervoltage lockout has occurred since the last read of this register. This indicates that the IN domain voltage fell below V_{INUVLO} (~2.6V) |
| INOVLO | 1 | IN Domain Overvoltage Lockout | 0b0 = The IN domain overvoltage lockout has not occurred since the last read of this register. 0b1 = The IN domain overvoltage lockout has occurred since the last read of this register. This indicates that the IN domain voltage rose above V_{INOVLO} (~5.85V) |
| TOVLD | 0 | Thermal Overload | 0b0 = Thermal overload has not occurred since the last read of this register. 0b1 = Thermal overload has occurred since the last read of this register. This indicates that the junction temperature has exceeded +165°C. |

STAT_GLBL (0x03)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------|-----------|-----------------|-----------|-----------|-----------|-----------|-----------|
| Field | DIDM | BOK | RSVD | DOD_S | TJAL2_S | TJAL1_S | STAT_EN | STAT_IRQ |
| Reset | OTP | 0b1 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Read Only | Read Only | Read Clears All | Read Only | Read Only | Read Only | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|---|
| DIDM | 7 | Device Identification Bits for Metal Options | 0b0 = MAX77643 0b1 = Reserved |
| BOK | 6 | BOK Interrupt Status | 0b0 = Main bias is not ready. 0b1 = Main bias enabled and ready. |
| RSVD | 5 | Reserved. Unutilized bit. Write to 0. Reads are don't care. | |
| DOD_S | 4 | LDO Dropout Detector Rising Status | 0b0 = LDO is not in dropout. 0b1 = LDO is in dropout. |
| TJAL2_S | 3 | Thermal Alarm 2 Status | 0b0 = The junction temperature is less than TJAL2. 0b1 = The junction temperature is greater than TJAL2. |
| TJAL1_S | 2 | Thermal Alarm 1 Status | 0b0 = The junction temperature is less than TJAL1. 0b1 = The junction temperature is greater than TJAL1. |
| STAT_EN | 1 | Debounced Status for the nEN Input | 0b0 = nEN is not active (logic high). 0b1 = nEN is active (logic low). |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|---|
| STAT_IRQ | 0 | Software Version of the nIRQ MOSFET Gate Drive | 0b0 = Unmasked gate drive is logic low. 0b1 = Unmasked gate drive is logic high. |

INTM_GLBL0 (0x04)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Field | RSVD | DOD_RM | TJAL2_RM | TJAL1_RM | nEN_RM | nEN_FM | GPI0_RM | GPI0_FM |
| Reset | 0b0 | 0b1 | 0b1 | 0b1 | 0b1 | 0b1 | 0b1 | 0b1 |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--|
| RSVD | 7 | Reserved. Unutilized bit. Write to 0. Reads are don't care. | |
| DOD_RM | 6 | LDO Dropout Detector Rising Interrupt Mask | 0b0 = Unmasked. If DOD_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 0b1 = Masked. nIRQ does not go low due to DOD_R. |
| TJAL2_RM | 5 | Thermal Alarm 2 Rising Interrupt Mask | 0b0 = Unmasked. If TJAL2_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 0b1 = Masked. nIRQ does not go low due to TJAL2_R. |
| TJAL1_RM | 4 | Thermal Alarm 1 Rising Interrupt Mask | 0b0 = Unmasked. If TJAL1_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 0b1 = Masked. nIRQ does not go low due to TJAL1_R. |
| nEN_RM | 3 | nEN Rising Interrupt Mask | 0b0 = Unmasked. If nEN_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 0b1 = Masked. nIRQ does not go low due to nEN_R. |
| nEN_FM | 2 | nEN Falling Interrupt Mask | 0b0 = Unmasked. If nEN_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 0b1 = Masked. nIRQ does not go low due to nEN_F. |
| GPI0_RM | 1 | GPI0 Rising Interrupt Mask | 0b0 = Unmasked. If GPI0_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 0b1 = Masked. nIRQ does not go low due to GPI0_R. |
| GPI0_FM | 0 | GPI0 Falling Interrupt Mask | 0b0 = Unmasked. If GPI0_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 0b1 = Masked. nIRQ does not go low due to GPI0_F. |

[INTM_GLBL1 \(0x05\)](#)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Field | RSVD | RSVD | LDO_M | SBB2_FM | SBB1_FM | SBB0_FM | GPI1_RM | GPI1_FM |
| Reset | 0b0 | 0b0 | 0b1 | 0b0 | 0b0 | 0b0 | 0b1 | 0b1 |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--|
| RSVD | 7 | Reserved. Unutilized bit. Write to 0. Reads are don't care. | |
| RSVD | 6 | Reserved. Unutilized bit. Write to 0. Reads are don't care. | |
| LDO_M | 5 | LDO Fault Interrupt Mask | 0b0 = Unmasked. If LDO_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 0b1 = Masked. nIRQ does not go low due to LDO_F. |
| SBB2_FM | 4 | SBB2 Fault Interrupt Mask | 0b0 = Unmasked. If SBB2_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 0b1 = Masked. nIRQ does not go low due to SBB2_F. |
| SBB1_FM | 3 | SBB1 Fault Interrupt Mask | 0b0 = Unmasked. If SBB1_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 0b1 = Masked. nIRQ does not go low due to SBB1_F. |
| SBB0_FM | 2 | SBB0 Fault Interrupt Mask | 0b0 = Unmasked. If SBB0_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 0b1 = Masked. nIRQ does not go low due to SBB0_F. |
| GPI1_RM | 1 | GPI1 Rising Interrupt Mask | 0b0 = Unmasked. If GPI1_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 0b1 = Masked. nIRQ does not go low due to GPI1_R. |
| GPI1_FM | 0 | GPI1 Falling Interrupt Mask | 0b0 = Unmasked. If GPI1_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 0b1 = Masked. nIRQ does not go low due to GPI1_F. |

[CNFG_GLBL0 \(0x06\)](#)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|---------------|---|-------------|---------------|---|
| Field | PU_DIS | MRST | SBIA_LPM | nEN_MODE[1:0] | | DBEN_nEN | SFT_CTRL[1:0] | |
| Reset | OTP | OTP | OTP | OTP | | OTP | 0b00 | |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | | Write, Read | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|---|
| PU_DIS | 7 | nEN Internal Pullup Resistor | 0b0 = Strong internal nEN pullup (200kΩ) 0b1 = Weak internal nEN pullup (10MΩ) |
| MRST | 6 | Sets the Manual Reset Time (t _{MRST}) | 0b0 = 8s 0b1 = 4s |
| SBIA_LPM | 5 | Main Bias Power Mode | 0b0 = Main bias is in normal-power mode by software. 0b1 = Main bias is in low-power mode by software. |
| nEN_MODE | 4:3 | nEN Input (ON-KEY) Default Configuration Mode | 0b00 = Push-button mode 0b01 = Slide-switch mode 0b10 = Logic mode 0b11 = Reserved |
| DBEN_nEN | 2 | Debounce Timer Enable for the nEN Pin | 0b0 = 500μs Debounce 0b1 = 30ms Debounce Applies only to push button and slide switch Mmode |
| SFT_CTRL | 1:0 | Software Reset Functions Note that the SFT_CRST and SFT_OFF commands initiate the power-down sequence flow as described in the data sheet. This power-down sequence flow has delay elements that add up to 205.24ms (60ms delay + 10.24ms nRST assert delay + 4x2.56ms power-down slot delays + 125ms output discharge delay). If issuing the SFT_CRST and/or SFT_OFF functions in software, wait for more than 300ms before trying to issue any additional commands through I ² C. | 0b00 = No action 0b01 = Software cold reset (SFT_CRST). The device powers down, resets, and then powers up again. 0b10 = Software off (SFT_OFF). The device powers down, resets, and then remains off and waiting for a wake-up event. 0b11 = Auto Wake Up (SFT_AUTO) The device powers down, and then automatically starts power up sequence after time determined in AUTO_WKT. Note that the registers do not get reset with Auto Wake Up. |

CNFG_GLBL1 (0x07)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|------------------|---------------|---|
| Field | RSVD[4:0] | | | | | SBB_F_SH UTDN | AUTO_WKT[1:0] | |
| Reset | 0b0000 | | | | | 0b0 | 0x00 | |
| Access Type | Write, Read | | | | | Write, Read | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------|------|---|--|
| RSVD | 7:3 | Reserved. Unutilized bit. Write to 0. Reads are don't care. | |
| SBB_F_SHU TDN | 2 | SBB Shutdown from SBB Fault | 0b0 = The SBB regulators do not shut off when an SBB fault occurs. 0b1 = The SBB regulators powers down sequentially when a SBB fault occurs. |
| AUTO_WKT | 1:0 | Auto Wake-Up Timer | 0b00 = 100ms Auto Wake-up Time 0b01 = 200ms Auto Wake-up Time 0b10 = 500ms Auto Wake-up Time 0b11 = 1000ms Auto Wake-up Time |

[CNFG_GPIO0 \(0x08\)](#)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|-------------|-------------|-------------|-------------|-----------|-------------|
| Field | RSVD[1:0] | | ALT_GPIO0 | DBEN_GPI | DO | DRV | DI | DIR |
| Reset | 0b0 | | OTP | 0b0 | 0b0 | 0b0 | 0b0 | 0b1 |
| Access Type | Write, Read | | Write, Read | Write, Read | Write, Read | Write, Read | Read Only | Write, Read |

| BITLEN | BITS | DESCRIPTION | DECODE |
|-----------|------|--|--|
| RSVD | 7:6 | Reserved. Unutilized bit. Write to 0. Reads are don't care. | |
| ALT_GPIO0 | 5 | Alternate Mode Enable for GPIO0 | 0b0 = Standard GPIO 0b1 = GPIO controls whether SBB0 is set by TV_SBB0 or TV_SBB0_DVS |
| DBEN_GPI | 4 | General Purpose Input Debounce Timer Enable | 0b0 = No debounce 0b1 = 30ms debounce |
| DO | 3 | General Purpose Output Data Output | This bit is a don't care when DIR = 1 (configured as input). When set for GPO (DIR = 0): 0b0 = GPIO is output logic low. 0b1 = GPIO is output logic high when set as push-pull output (DRV = 1). GPIO is high-impedance when set as an open-drain output (DRV = 0). |
| DRV | 2 | General Purpose Output Driver Type | This bit is a don't care when DIR = 1 (configured as input). When set for GPO (DIR = 0): 0b0 = Open-drain 0b1 = Push-pull |
| DI | 1 | GPIO Digital Input Value. Irrespective of whether the GPIO is set for GPI (DIR = 1) or GPO (DIR = 0), DI reflects the state of the GPIO. | 0b0 = Input logic low 0b1 = Input logic high |
| DIR | 0 | GPIO Direction | 0b0 = General purpose output (GPO) 0b1 = General purpose input (GPI) |

[CNFG_GPIO1 \(0x09\)](#)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|-------------|-------------|-------------|-------------|-----------|-------------|
| Field | RSVD[1:0] | | ALT_GPIO1 | DBEN_GPI | DO | DRV | DI | DIR |
| Reset | 0b00 | | OTP | 0b0 | 0b0 | 0b0 | 0b0 | 0b1 |
| Access Type | Write, Read | | Write, Read | Write, Read | Write, Read | Write, Read | Read Only | Write, Read |

| BITLEN | BITS | DESCRIPTION | DECODE |
|-----------|------|---|--|
| RSVD | 7:6 | Reserved. Unutilized bit. Write to 0. Reads are don't care. | |
| ALT_GPIO1 | 5 | Alternate Mode Enable for GPIO1 | 0b0 = Standard GPIO 0b1 = Flexible power sequencer active-high output for SBB2. |
| DBEN_GPI | 4 | General Purpose Input Debounce Timer Enable | 0b0 = No debounce 0b1 = 30ms debounce |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|--|
| DO | 3 | General Purpose Output Data Output | This bit is a don't care when DIR = 1 (configured as input). When set for GPO (DIR = 0): 0b0 = GPIO is output logic low. 0b1 = GPIO is output logic high when set as push-pull output (DRV = 1). GPIO is high-impedance when set as an open-drain output (DRV = 0). |
| DRV | 2 | General Purpose Output Driver Type | This bit is a don't care when DIR = 1 (configured as input). When set for GPO (DIR = 0): 0b0 = Open-drain 0b1 = Push-pull |
| DI | 1 | GPIO Digital Input Value. Irrespective of whether the GPIO is set for GPI (DIR = 1) or GPO (DIR = 0), DI reflects the state of the GPIO. | 0b0 = Input logic low 0b1 = Input logic high |
| DIR | 0 | GPIO Direction | 0b0 = General purpose output (GPO) 0b1 = General purpose input (GPI) |

CID (0x10)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|-----------|---|---|---|---|
| Field | – | – | – | CID[4:0] | | | | |
| Reset | – | – | – | OTP | | | | |
| Access Type | – | – | – | Read Only | | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|---|
| CID | 4:0 | Chip Identification Code The chip identification code refers to a set of reset values in the register map, or the "OTP configuration." |

CNFG_WDT (0x17)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|--------------|---|-------------|-------------|-------------|-----------|
| Field | RSVD[1:0] | | WDT_PER[1:0] | | WDT_MOD_E | WDT_CLR | WDT_EN | WDT_LOCK |
| Reset | 0b00 | | 0b11 | | 0b0 | 0b0 | OTP | OTP |
| Access Type | Write, Read | | Write, Read | | Write, Read | Write, Read | Write, Read | Read Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|---|
| RSVD | 7:6 | Reserved. Unutilized bit. Write to 0. Reads are don't care. | |
| WDT_PER | 5:4 | Watchdog Timer Period. Sets t_{WD} . Watchdog timer is reset to the programmed value as soon as this bitfield is changed. | 0b00 = 16 seconds 0b01 = 32 seconds 0b10 = 64 seconds 0b11 = 128 seconds |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|---|
| WDT_MODE | 3 | Watchdog Timer Expired Action. Determines what the IC does after the watchdog timer expires. | 0b0 = Watchdog timer expire causes power-off. 0b1 = Watchdog timer expire causes power reset. |
| WDT_CLR | 2 | Watchdog Timer Clear Control. Set this bit to feed (reset) the watchdog timer. | 0b0 = Watchdog timer period is not reset. 0b1 = Watchdog timer is reset back to t_{WD} . |
| WDT_EN | 1 | Watchdog Timer Enable. Write protected depending on WDT_LOCK. | 0b0 = Watchdog timer is not enabled. 0b1 = Watchdog timer is enabled. The timer expires if not reset by setting WDT_CLR. |
| WDT_LOCK | 0 | Factory-Set Safety Bit for the Watchdog Timer. Determines if the timer can be disabled through WDT_EN or not. | 0b0 = Watchdog timer can be enabled and disabled with WDT_EN. 0b1 = Watchdog timer can not be disabled with WDT_EN. However, WDT_EN can still be used to enable the watchdog timer. |

CNFG_SBB_TOP (0x28)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|--------------|---|
| Field | DIS_LPM | – | – | – | – | – | DRV_SBB[1:0] | |
| Reset | 0b0 | – | – | – | – | – | OTP | |
| Access Type | Write, Read | – | – | – | – | – | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--|
| DIS_LPM | 7 | Disables the Automatic Low-Power Mode for Each SIMO Channel. | 0b0 = Automatic low power mode for each SIMO channel 0b1 = Disable low power mode feature for each SIMO channel |
| DRV_SBB | 1:0 | SIMO Buck-Boost (All Channels) Drive Strength Trim. See the <i>Drive Strength</i> section for more details. | 0b00 = Fastest transition time 0b01 = A little slower than 0b00 0b10 = A little slower than 0b01 0b11 = A little slower than 0b10 |

CNFG_SBB0_A (0x29)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field | TV_SBB0[7:0] | | | | | | | |
| Reset | OTP | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|--|
| TV_SBB0 | 7:0 | SIMO Buck-Boost Channel 0 Target Output Voltage This 8-bit configuration is a linear transfer function that starts at 0.5V and ends at 5.5V with 25mV increments. | 0x00 = 0.500V 0x01 = 0.525V 0x02 = 0.550V 0x03 = 0.575V 0x04 = 0.600V 0x05 = 0.625V 0x06 = 0.650V 0x07 = 0.675V 0x08 = 0.700V ... 0xC5 = 5.425V 0xC6 = 5.450V 0xC7 = 5.475V 0xC8 to 0xFF = 5.500V |

CNFG_SBB0_B (0x2A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|--------------|---|-------------|--------------|---|---|
| Field | OP_MODE[1:0] | | IP_SBB0[1:0] | | ADE_SBB0 | EN_SBB0[2:0] | | |
| Reset | OTP | | OTP | | OTP | OTP | | |
| Access Type | Write, Read | | Write, Read | | Write, Read | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|---|
| OP_MODE | 7:6 | Operation Mode of SBB0 | 0b00 = Automatic 0b01 = Buck mode 0b10 = Boost mode 0b11 = Buck-boost mode |
| IP_SBB0 | 5:4 | SIMO Buck-Boost Channel 0 Peak Current Limit | 0b00 = 1.000A 0b01 = 0.750A 0b10 = 0.500A 0b11 = 0.333A |
| ADE_SBB0 | 3 | SIMO Buck-Boost Channel 0 Active-Discharge Enable | 0b0 = The active discharge function is disabled. When SBB0 is disabled, its discharge rate is a function of the output capacitance and the external load. 0b1 = The active discharge function is enabled. When SBB0 is disabled, an internal resistor (RAD_SBB0) is activated from SBB0 to PGND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal RAD_SBB0 load. |
| EN_SBB0 | 2:0 | Enable Control for SIMO Buck-Boost Channel 0. Select the FPS slot that the channel powers up and powers down in or whether the channel is forced on or off. Prior to enabling the SIMO, program the bias circuits to normal-power mode (SBIA_LPM = 0). After the SIMO is enabled, the bias circuits may be programmed back to low-power mode (SBIA_LPM = 1) to decrease quiescent current. | 0b000 = FPS slot 0 0b001 = FPS slot 1 0b010 = FPS slot 2 0b011 = FPS slot 3 0b100 = Off irrespective of FPS 0b101 = Same as 0b100 0b110 = On irrespective of FPS 0b111 = Same as 0b110 |

CNFG_SBB1_A (0x2B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field | TV_SBB1[7:0] | | | | | | | |
| Reset | OTP | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|--|
| TV_SBB1 | 7:0 | SIMO Buck-Boost Channel 1 Target Output Voltage This 8-bit configuration is a linear transfer function that starts at 0.5V and ends at 5.5V with 25mV increments. | 0x00 = 0.500V 0x01 = 0.525V 0x02 = 0.550V 0x03 = 0.575V 0x04 = 0.600V 0x05 = 0.625V 0x06 = 0.650V 0x07 = 0.675V 0x08 = 0.700V ... 0xC5 = 5.425V 0xC6 = 5.450V 0xC7 = 5.475V 0xC8 to 0xFF = 5.500V |

CNFG_SBB1_B (0x2C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|--------------|---|-------------|--------------|---|---|
| Field | OP_MODE[1:0] | | IP_SBB1[1:0] | | ADE_SBB1 | EN_SBB1[2:0] | | |
| Reset | OTP | | OTP | | OTP | OTP | | |
| Access Type | Write, Read | | Write, Read | | Write, Read | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|---|
| OP_MODE | 7:6 | Operation Mode of SBB1 | 0b00 = Automatic 0b01 = Buck mode 0b10 = Boost mode 0b11 = Buck-boost mode |
| IP_SBB1 | 5:4 | SIMO Buck-Boost Channel 1 Peak Current Limit | 0b00 = 1.000A 0b01 = 0.750A 0b10 = 0.500A 0b11 = 0.333A |
| ADE_SBB1 | 3 | SIMO Buck-Boost Channel 1 Active-Discharge Enable | 0b0 = The active discharge function is disabled. When SBB1 is disabled, its discharge rate is a function of the output capacitance and the external load. 0b1 = The active discharge function is enabled. When SBB1 is disabled, an internal resistor (RAD_SBB1) is activated from SBB1 to PGND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal RAD_SBB1 load. |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|---|
| EN_SBB1 | 2:0 | <p>Enable Control for SIMO Buck-Boost Channel 1. Select the FPS slot that the channel powers up and powers down in or whether the channel is forced on or off.</p> <p>Prior to enabling the SIMO, program the bias circuits to normal-power mode (SBIA_LPM = 0). After the SIMO is enabled, the bias circuits may be programmed back to low-power mode (SBIA_LPM = 1) to decrease quiescent current.</p> | <p>0b000 = FPS slot 0 0b001 = FPS slot 1 0b010 = FPS slot 2 0b011 = FPS slot 3 0b100 = Off irrespective of FPS 0b101 = Same as 0b100 0b110 = On irrespective of FPS 0b111 = Same as 0b110</p> |

CNFG_SBB2_A (0x2D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field | TV_SBB2[7:0] | | | | | | | |
| Reset | OTP | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--|
| TV_SBB2 | 7:0 | <p>SIMO Buck-Boost Channel 2 Target Output Voltage</p> <p>This 8-bit configuration is a linear transfer function that starts at 0.5V and ends at 5.5V with 25mV increments.</p> | <p>0x00 = 0.500V 0x01 = 0.525V 0x02 = 0.550V 0x03 = 0.575V 0x04 = 0.600V 0x05 = 0.625V 0x06 = 0.650V 0x07 = 0.675V 0x08 = 0.700V ... 0xC5 = 5.425V 0xC6 = 5.450V 0xC7 = 5.475V 0xC8 to 0xFF = 5.500V</p> |

CNFG_SBB2_B (0x2E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|--------------|---|-------------|--------------|---|---|
| Field | OP_MODE[1:0] | | IP_SBB2[1:0] | | ADE_SBB2 | EN_SBB2[2:0] | | |
| Reset | OTP | | OTP | | OTP | OTP | | |
| Access Type | Write, Read | | Write, Read | | Write, Read | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|---|
| OP_MODE | 7:6 | Operation Mode of SBB2 | <p>0b00 = Automatic 0b01 = Buck mode 0b10 = Boost mode 0b11 = Buck-boost mode</p> |
| IP_SBB2 | 5:4 | SIMO Buck-Boost Channel 2 Peak Current Limit | <p>0b00 = 1.000A 0b01 = 0.750A 0b10 = 0.500A 0b11 = 0.333A</p> |

| BITLED | BITS | DESCRIPTION | DECODE |
|----------|------|---|---|
| ADE_SBB2 | 3 | SIMO Buck-Boost Channel 2 Active-Discharge Enable | 0b0 = The active discharge function is disabled. When SBB2 is disabled, its discharge rate is a function of the output capacitance and the external load. 0b1 = The active discharge function is enabled. When SBB2 is disabled, an internal resistor (RAD_SBB2) is activated from SBB2 to PGND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal RAD_SBB2 load. |
| EN_SBB2 | 2:0 | Enable Control for SIMO Buck-Boost Channel 2. Select the FPS slot that the channel powers up and powers down in or whether the channel is forced on or off. Prior to enabling the SIMO, program the bias circuits to normal power mode (SBIA_LPM = 0). After the SIMO is enabled, the bias circuits may be programmed back to low power mode (SBIA_LPM = 1) to decrease quiescent current. | 0b000 = FPS slot 0 0b001 = FPS slot 1 0b010 = FPS slot 2 0b011 = FPS slot 3 0b100 = Off irrespective of FPS 0b101 = Same as 0b100 0b110 = On irrespective of FPS 0b111 = Same as 0b110 |

CNFG_DVS_SBB0_A (0x2F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|--|---|---|--|---|---|---|
| Field | TV_SBB0_DVS[7:0] | | | | | | | |
| Reset | 0x14 | | | | | | | |
| Access Type | Write, Read | | | | | | | |
| BITFIELD | BITS | DESCRIPTION | | | DECODE | | | |
| TV_SBB0_DVS | 7:0 | SIMO Buck-Boost Channel 0 Target Output Voltage This 7-bit configuration is a linear transfer function that starts at 0.5V and ends at 5.5V with 25mV increments. | | | 0x00 = 0.500V 0x01 = 0.525V 0x02 = 0.550V 0x03 = 0.575V 0x04 = 0.600V 0x05 = 0.625V 0x06 = 0.650V 0x07 = 0.675V 0x08 = 0.700V ... 0xC5 = 5.425V 0xC6 = 5.450V 0xC7 = 5.475V 0xC8 to 0xFF = 5.500V | | | |

CNFG_LDO0_A (0x38)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|---|---|---|---|---|---|
| Field | TV_OFS_LDO | TV_LDO[6:0] | | | | | | |
| Reset | 0xOTP | OTP | | | | | | |
| Access Type | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------|------|--|--|
| TV_OFS_LDO | 7 | LDO Output Voltage. This bit applies a 1.325V offset to the output voltage of the LDO. | 0b0 = No Offset 0b1 = 1.325V Offset |
| TV_LDO | 6:0 | LDO Target Output Voltage This 7-bit configuration is a linear transfer function that starts at 0.5V and ends at 3.675V with 25mV increments. | 0x00 = 0.500V 0x01 = 0.525V 0x02 = 0.550V 0x03 = 0.575V 0x04 = 0.600V 0x05 = 0.625V 0x06 = 0.650V 0x07 = 0.675V 0x08 = 0.700V ... 0x7E = 3.650V 0x7F = 3.675V When TV_LDO[7] = 0, TV_LDO[6:0] sets the LDO's output voltage range from 0.5V to 3.675V. When TV_LDO[7] = 1, TV_LDO[6:0] sets the LDO's output voltage from 1.825V to 5V. |

CNFG_LDO0_B (0x39)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|-------------|-------------|-------------|---|---|
| Field | RSVD[2:0] | | | LDO_MD | ADE_LDO | EN_LDO[2:0] | | |
| Reset | 0b0 | | | OTP | OTP | OTP | | |
| Access Type | Write, Read | | | Write, Read | Write, Read | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--|
| RSVD | 7:5 | Reserved. Unutilized bit. Write to 0. Reads are don't care. | |
| LDO_MD | 4 | Operation Mode of LDO | 0b0 = Low dropout linear regulator (LDO) mode 0b1 = Load switch (LSW) mode |
| ADE_LDO | 3 | LDO Active-Discharge Enable | 0b0 = The active discharge function is disabled. When LDO0 is disabled, its discharge rate is a function of the output capacitance and the external load. 0b1 = The active discharge function is enabled. When LDO is disabled, an internal resistor (RAD_LDO) is activated from LDO to GND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal RAD_LDO load. |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|---|
| EN_LDO | 2:0 | Enable Control for LDO. Select the FPS slot that the channel powers up and powers down in or whether the channel is forced on or off. | 0b000 = FPS slot 0 0b001 = FPS slot 1 0b010 = FPS slot 2 0b011 = FPS slot 3 0b100 = Off irrespective of FPS 0b101 = Same as 0b100 0b110 = On irrespective of FPS 0b111 = Same as 0b110 |

Typical Application Circuits

Typical Applications Circuit

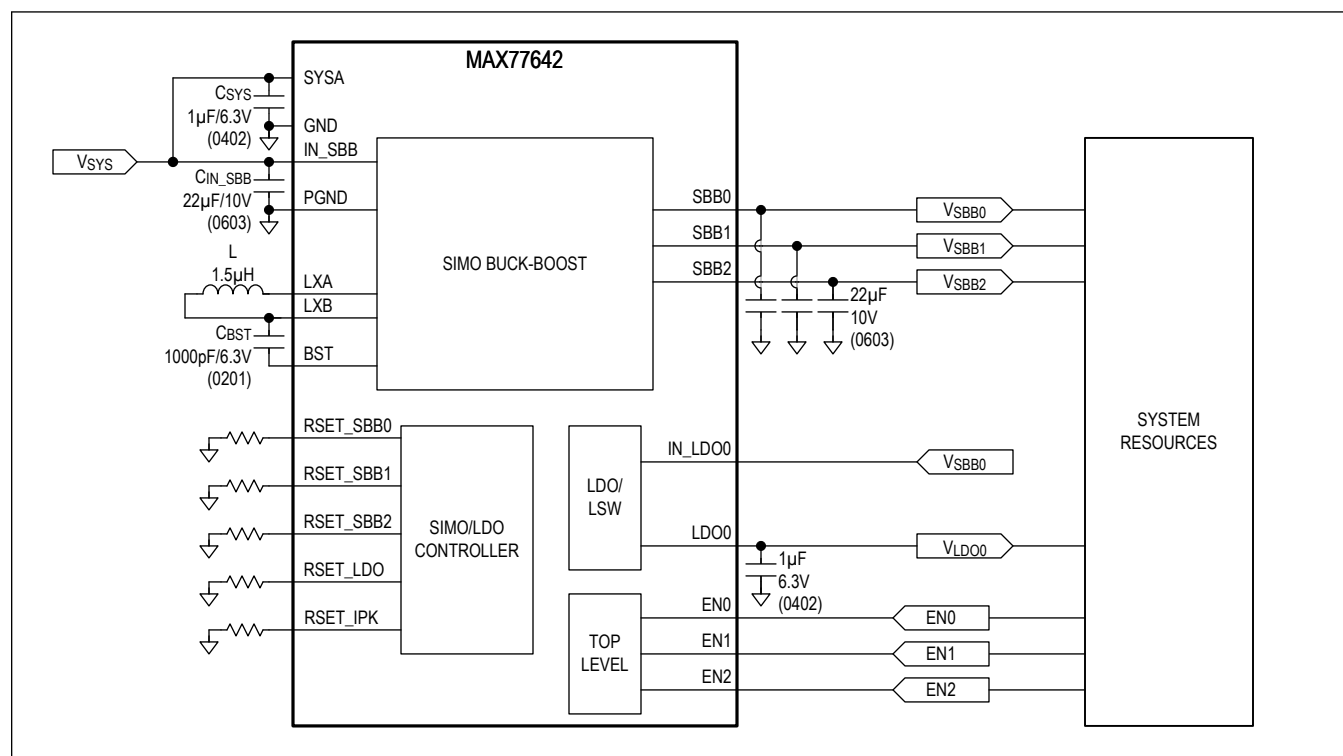


Figure 28. Typical Applications Circuit - R_SEL Version (MAX77642)

Ultra Configurable PMIC Featuring 93% Peak Efficiency Single-Inductor, 3-Output Buck-Boost, 1-LDO for Long Battery Life Applications

[illegible]

Ordering Information

**Custom samples only. Not for production or stock. Contact factory for more information.*

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|--------------------|------------------|--|---------------------------|
| 0 | 8/20 | Initial release | — |
| 1 | 10/20 | Updated the <i>Ordering Information</i> table | 88 |
| 2 | 4/21 | Updated Table 3, <i>Register Map</i> tables, and <i>Ordering Information</i> table | 28, 72, 79, 80, 86, 87 |
| 3 | 5/21 | Updated Figure 1, Table 3, <i>Register Details</i> , and <i>Ordering Information</i> table | 27–29, 73, 84 |
| 4 | 10/21 | Updated <i>Electrical Characteristics</i> — <i>SIMO Buck-Boost</i> table, Table 3, Figure 9, <i>Register Map</i> , and <i>Register Details</i> | 13, 28, 29, 42, 73, 75 |

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