

MAX77596

24V, 300mA, Buck Converter with 1.1 μ A IQ

General Description

The MAX77596 is a small, synchronous buck converter with integrated switches. The device is designed to deliver up to 300mA with input voltages from 3.5V to 24V, while using only 1.1 μ A quiescent current at no load (fixed-output version). Voltage quality can be monitored by observing the RESET signal. The device can operate near dropout by running at 98% duty cycle, making it ideal for battery-powered applications.

The device offers fixed 3.3V and 5V output versions, as well as an adjustable version. The adjustable version allows the user to program the output voltage between 1V and 10V by using a resistor-divider. Frequency is fixed at 1.7MHz, which allows for small external components and reduced output ripple. The device offers both forced-PWM and skip modes of operation, with ultra-low quiescent current of 1.1 μ A in skip mode.

The MAX77596 is available in a small (2mm x 2.5mm) 10-pin TDFN package and operates across the -40°C to +85°C temperature range.

Applications

- Portable Devices Powered from 2s, 3s, or 4s Li+ Batteries
- USB Type-C Devices
- Point-of-Load Applications

Benefits and Features

- Flexible Power for Systems That Require a Wide Input Voltage Range
 - V_{IN} Range: 3.5V to 24V
 - Up to 300mA Output Current
 - Fixed 3.3V, 5V, or Programmable 1V to 10V Output Voltage
 - 98% (Max) Duty Cycle Operation with Low Dropout
 - Operates from 5V, 12V, or 20V USB Type-C Input Power
 - Operates from 2S, 3S, or 4S Li-Ion Battery
- Minimizes Power Consumption and Extends Battery Life
 - 1.1 μ A Quiescent Current (3.3V Fixed Output Voltage)
 - 86% Peak Efficiency at 12 V_{IN} , 3.3 V_{OUT}
- Minimizes Solution Size
 - 1.7MHz Operating Frequency
 - Small 2.0mm x 2.5mm x 0.75mm 10-Pin TDFN Package
- Robust Solution
 - Short-Circuit, Thermal Protections
 - 6.67ms Internal Soft-Start Minimizes Inrush Current
 - Current-Mode Control Architecture
 - Up to 42V Input Voltage Tolerance

Absolute Maximum Ratings

(Voltages Referenced to PGND)

SUP	-0.3V to +42V
EN	-0.3V to V_{SUP} + 0.3V
BST to LX	+6V
BST	-0.3V to +47V
MODE, OUT/FB, RESET	-0.3V to V_{BIAS} + 0.3V
AGND	-0.3V to +0.3V
BIAS	-0.3V to +6.0V

OUT/FB Short-Circuit Duration	Continuous
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)	
(derate 9.8mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)	784mW
Operating Temperature Range	-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$
Junction Temperature	+150 $^\circ\text{C}$
Storage Temperature Range	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Lead Temperature (soldering, 10s)	300 $^\circ\text{C}$
Soldering Temperature (reflow)	+260 $^\circ\text{C}$

Package Thermal Characteristics (Note 1)

TDFN

Junction-to-Ambient Thermal Resistance (θ_{JA}).....102 $^\circ\text{C}/\text{W}$

Junction-to-Case Thermal Resistance (θ_{JC}).....2.9 $^\circ\text{C}/\text{W}$

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristic

($V_{SUP} = V_{EN} = 14\text{V}$, $V_{MODE} = 0\text{V}$, $T_A = T_J = -40^\circ\text{C}$ to +85 $^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{SUP}		3.5	24		V
Supply Voltage	V_{SUP}	$t < 500\text{ms}$ (Note 3)		42		V
Supply Current	I_{SUP}	Shutdown ($V_{EN} = 0\text{V}$)	0.75	3.0		μA
		No load, fixed 3.3V V_{OUT}	1.1	3.0		
		No load, fixed 5.0V V_{OUT}	1.8	5.0		
		No load, adjustable V_{OUT}	32	70		
		$T_A = +25^\circ\text{C}$			80	
		$T_A = -40^\circ\text{C}$ to +85 $^\circ\text{C}$				
		$V_{MODE} = V_{BIAS}$, no load, FPWM, no switching	0.5	1	1.5	mA
UV Lockout	V_{UVLO}	V_{BIAS} rising	3.0	3.2	3.4	V
		Hysteresis			0.4	
BIAS Regulator Voltage	V_{BIAS}	$V_{SUP} = 5.5\text{V}$ to 24V (MAX77596ETBC+)		5		V
BIAS Current Limit			10			mA
BUCK CONVERTER						
Voltage Accuracy	$V_{OUT,3.3\text{V}}$	$V_{OUT} = 3.3\text{V}$, $6\text{V} \leq V_{SUP} \leq 24\text{V}$, $I_{LOAD} = 0$ to 300mA	3.1	3.3	3.4	V
	$V_{OUT,5.0\text{V}}$	$V_{OUT} = 5.0\text{V}$, $6\text{V} \leq V_{SUP} \leq 24\text{V}$, $I_{LOAD} = 0$ to 300mA	4.8	5.0	5.15	
Output Voltage Range	V_{OUT}	Adjustable output versions	1	10		V
FB Voltage Accuracy	V_{FB}	Adjustable output versions, $3.5\text{V} \leq V_{SUP} \leq 24\text{V}$, $I_{LOAD} = 300\mu\text{A}$	0.98	1.0	1.03	V
FB Input Current	I_{FB}	$V_{FB} = 1\text{V}$		0.02		μA
FB Load Regulation	ΔV_{LOAD}	$I_{LOAD} = 0.3\text{mA}$ to 300mA		2		%

Electrical Characteristics (continued)

($V_{SUP} = V_{EN} = 14V$, $V_{MODE} = 0V$, $T_A = T_J = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.) (Note 2)

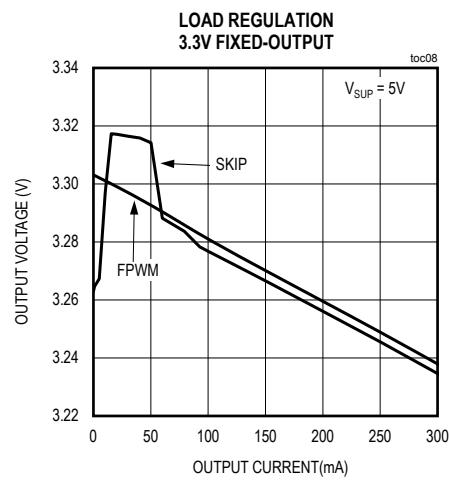
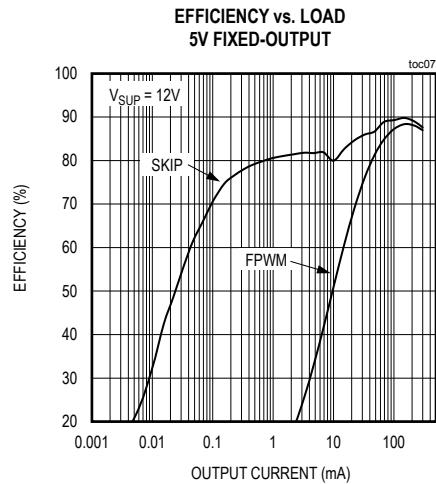
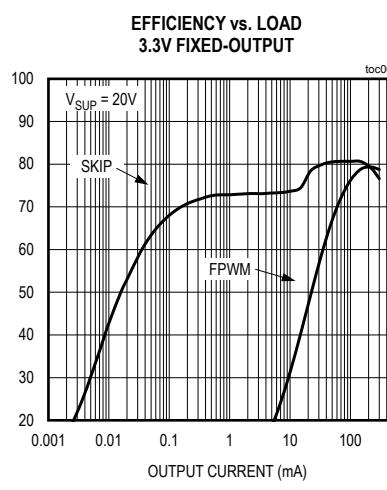
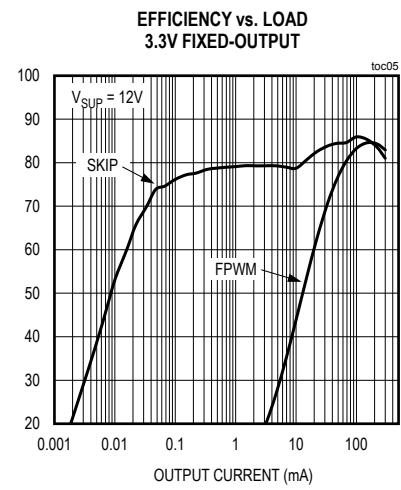
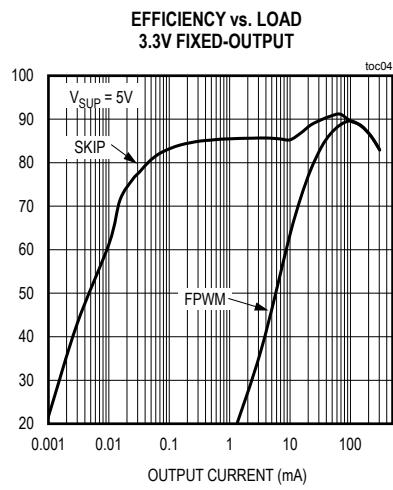
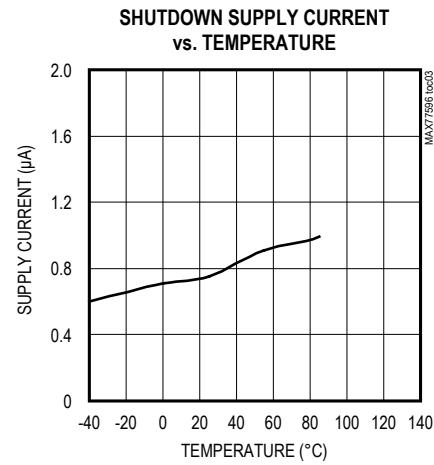
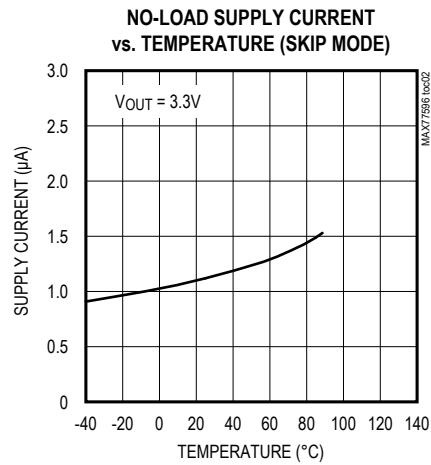
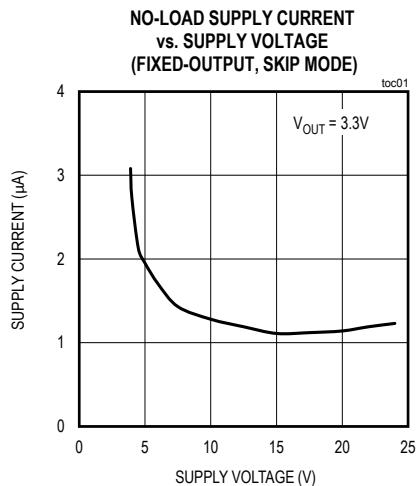
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FB Line Regulation	ΔV_{LINE}	$6V \leq V_{SUP} \leq 24V$		0.02		%/V
High-Side DMOS R_{DSON}	$R_{ON,HS}$	$V_{BIAS} = 5V$, $I_{LX} = 200mA$		1000	2200	$m\Omega$
Low-Side DMOS R_{DSON}	$R_{ON,LS}$	$V_{BIAS} = 5V$, $I_{LX} = 200mA$		500	1200	$m\Omega$
DMOS High-Side Current-Limit Threshold	I_{MAX}		425	500	575	mA
DMOS High-Side Skip-Mode Peak-Current Threshold	I_{SKIP}		70	100	130	mA
DMOS Low-Side Zero-Crossing Threshold	I_{ZX}			40		mA
DMOS Low-Side Negative Current-Limit Threshold	I_{NEG}	FPWM mode		-320		mA
Soft-Start Ramp Time	t_{SS}			6.67		ms
LX Rise Time	$t_{RISE,LX}$	(Note 3)		6		ns
Minimum On-Time	t_{ON_MIN}			34		ns
Maximum Duty Cycle	DC_{MAX}			98		%
PWM Switching Frequency	f_{SW}		1.58	1.7	1.82	MHz
RESET OUTPUT (RESET)						
RESET Threshold	V_{THR_RES}	V_{OUT} rising	90	92	94	% V_{OUT}
	V_{THF_RES}	V_{OUT} falling	88	90	92	
RESET Debounce	t_{DEB}			12		μ s
RESET High Leakage Current	$I_{LEAK,RES}$	$T_A = +25^\circ C$		1		μ A
RESET Low Level	$V_{OUT,RES}$	Sinking 1mA		0.4		V
LOGIC LEVELS						
EN Input High Threshold	$V_{IH,EN}$		2.4			V
EN Input Low Threshold	$V_{IL,EN}$			0.4		V
EN Input Current	$I_{IN,EN}$			0.1		μ A
MODE Input High Threshold	$V_{IH,MODE}$		1.4			V
MODE Input Low Threshold	$V_{IL,MODE}$			0.4		V
MODE Internal Pulldown	$R_{PD,MODE}$		1000			$k\Omega$
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}	(Note 3)		+175		$^\circ C$
Thermal-Shutdown Hysteresis	$T_{SHDN,HYS}$	(Note 3)		+15		$^\circ C$

Note 2: Limits are 100% tested at $T_A = +25^\circ C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 3: Guaranteed by design; not production tested.

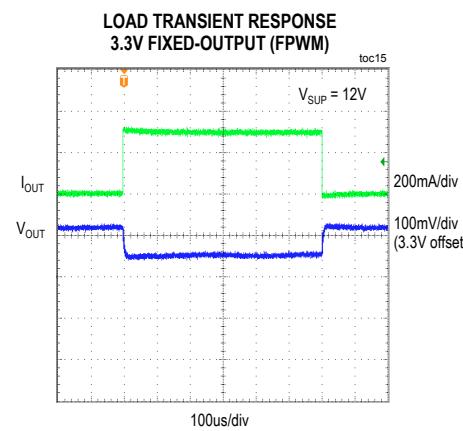
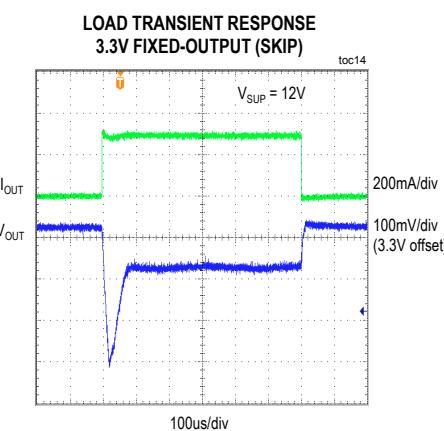
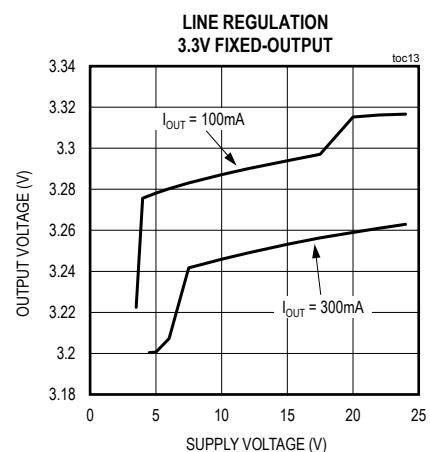
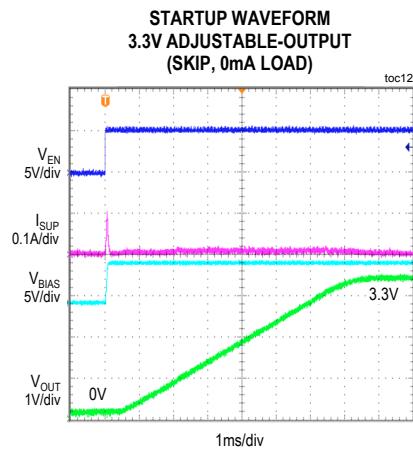
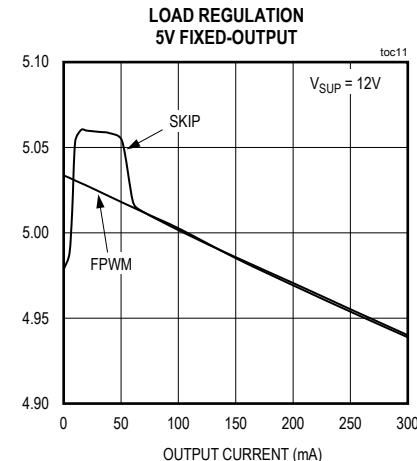
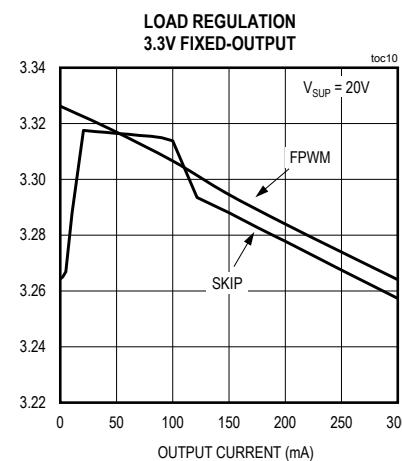
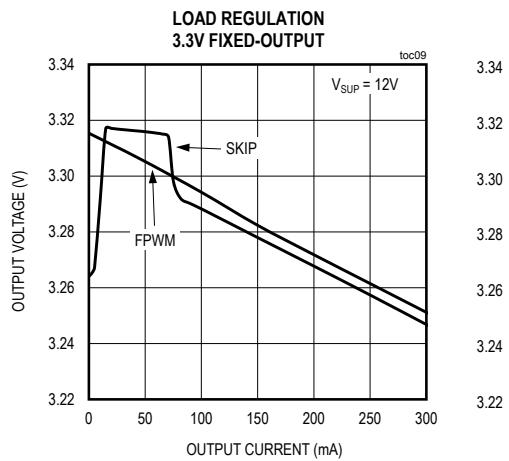
Typical Operating Characteristics

($V_{SUP} = V_{EN} = 12V$, $T_A = +25^{\circ}C$, unless otherwise noted.)



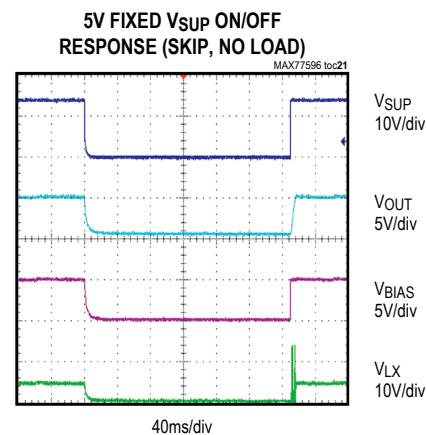
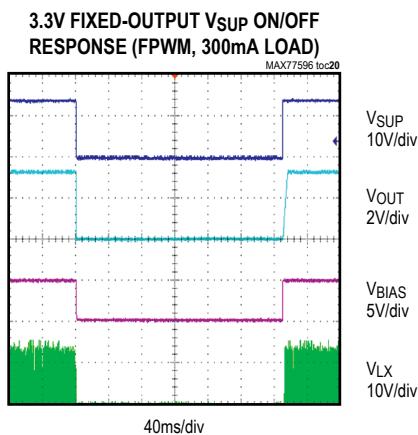
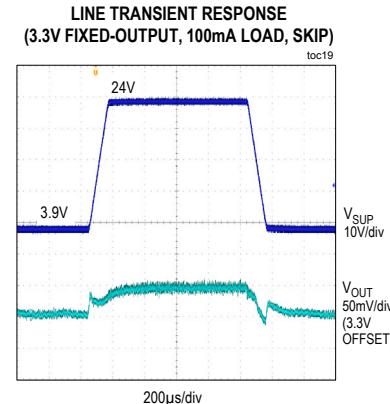
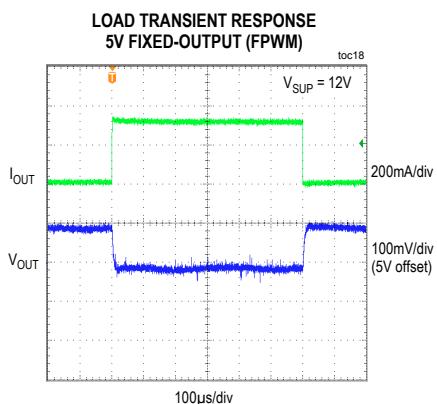
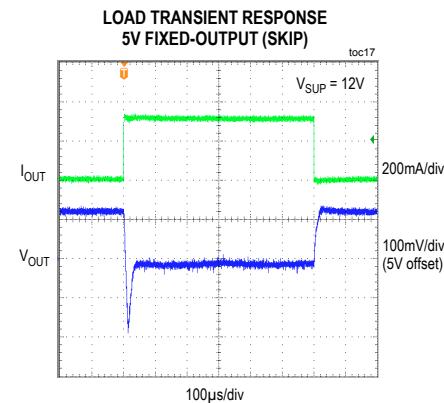
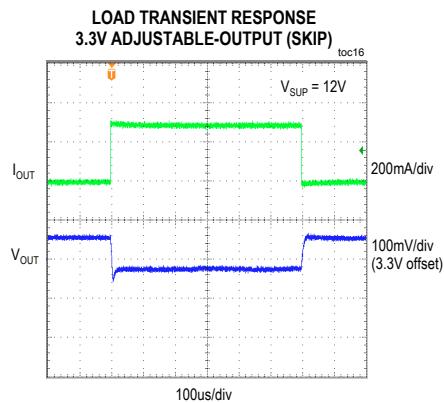
Typical Operating Characteristics (continued)

($V_{SUP} = V_{EN} = 12V$, $T_A = +25^{\circ}C$, unless otherwise noted.)



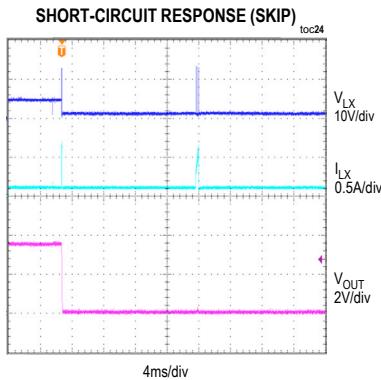
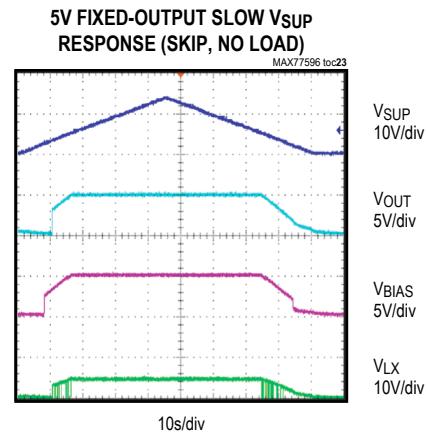
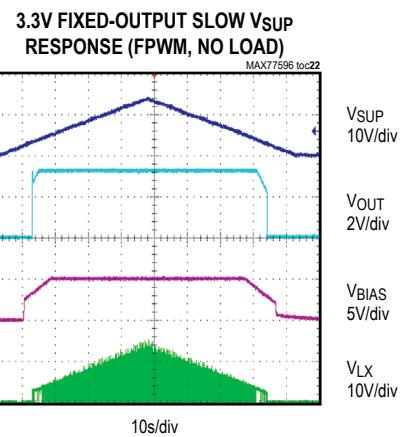
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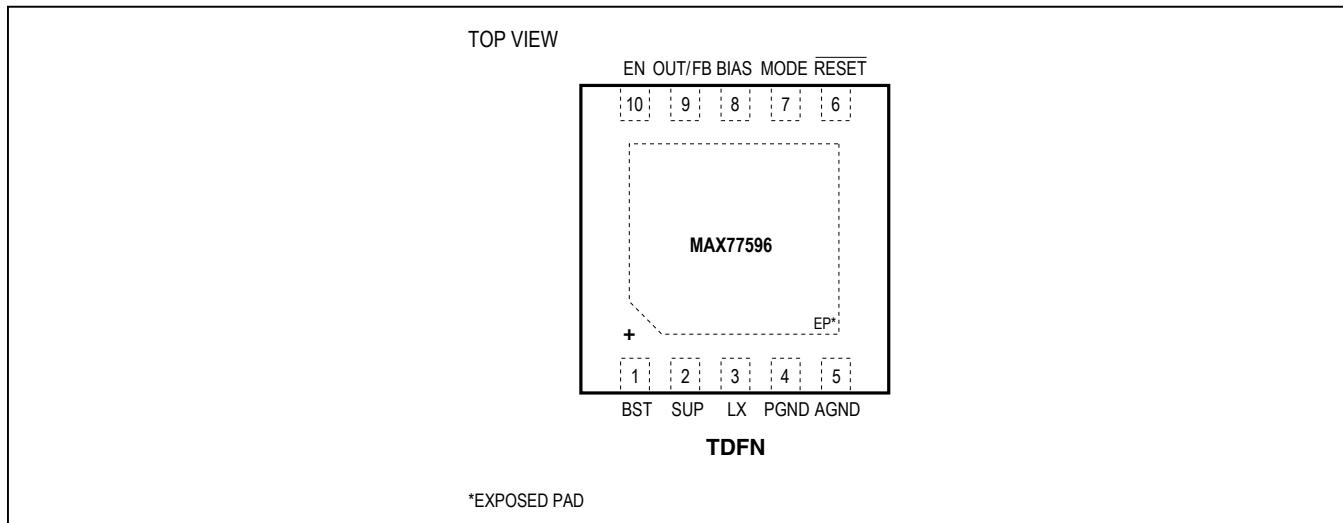


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($V_{SUP} = V_{EN} = 12V$, $T_A = +25^\circ C$, unless otherwise noted.)



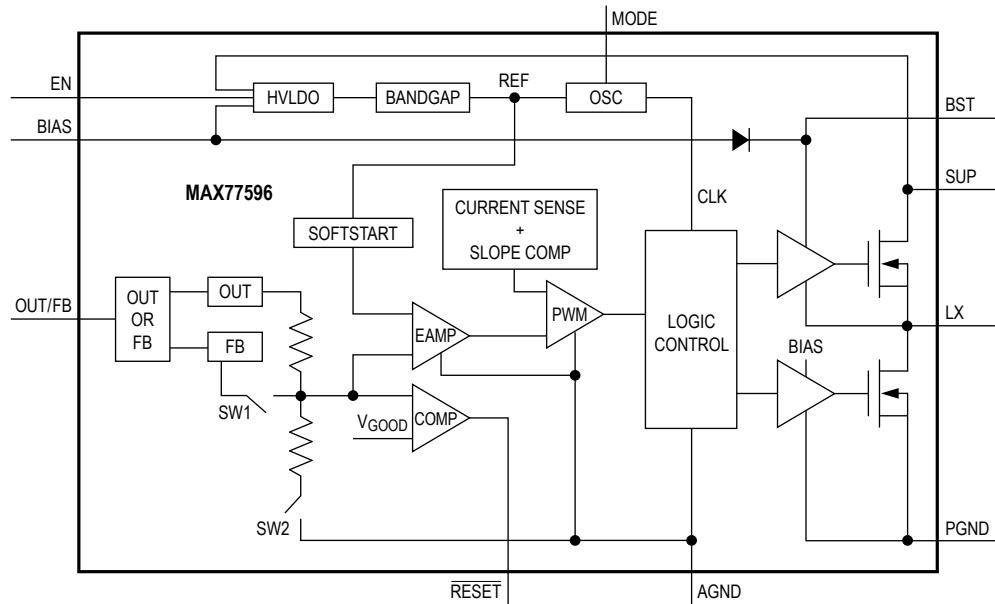
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	BST	High-Side Driver Supply. Connect a 0.1 μ F bootstrap capacitor between LX and BST.
2	SUP	IC Supply Input. Connect a minimum of 4.7 μ F ceramic capacitor from SUP to PGND.
3	LX	Buck Switching Node. LX is high impedance when the device is off.
4	PGND	Power Ground. Connect to AGND under the device in a star configuration.
5	AGND	Analog Ground. Connect to PGND under the device in a star configuration.
6	RESET	Open-Drain Reset Output. An external pullup resistor is required.
7	MODE	Mode Switch-Control Input. Connect to ground or leave open to enable skip-mode operation under light loads. Connect to BIAS to enable forced-PWM mode. MODE has a 1M Ω internal pulldown.
8	BIAS	5V Internal Logic Supply. Connect a 1 μ F ceramic capacitor to AGND. Do not load this pin externally.
9	OUT/FB	MAX77596ETBA+/MAX77596ETBB+ (Fixed Output): Buck Regulator Voltage-Sense Input. Bypass OUT to PGND with a minimum 22 μ F X5R ceramic capacitor. MAX77596ETBC+ (Adjustable Output): Feedback Input. Connect FB to a resistive divider between the buck output and AGND to set the output voltage.
10	EN	SUP Voltage-Compatible Enable Input. Drive EN low to disable the device. Drive EN high to enable the device.
—	EP	Exposed Pad. Connect EP to a large copper ground plane for effective power dissipation. Do not use EP as the only IC ground connection. EP must be connected to PGND.

Block Diagram



**NOTE 1: FOR INTERNAL FEEDBACK VERSION, SW1 IS OPEN AND SW2 CLOSED.
EXTERNAL PIN IS CALLED OUT.**

**NOTE 2: FOR EXTERNAL FEEDBACK VERSION, SW1 IS CLOSED AND SW2 OPEN.
EXTERNAL PIN IS CALLED FB.**

Detailed Description

The MAX77596 is a small, current-mode buck converter that features synchronous rectification and requires no external compensation network. The device operates from a 3.5V to 24V supply voltage and can deliver up to 300mA output current. Frequency is fixed at 1.7MHz, which allows for small external components and reduced output ripple.

The device offers fixed 3.3V output, fixed 5V output, and adjustable output options. The adjustable version can be set between 1V and 10V by using an external resistive divider. Voltage quality can be monitored by observing the $\overline{\text{RESET}}$ signal. The device offers both forced-PWM and skip mode, with ultra-low-quiescent current of 1.1 μ A in skip mode.

DC-DC Converter Control Architecture

The step-down converter uses a PWM peak current-mode control scheme with a load-line architecture. Peak current-mode control provides several advantages over voltage-mode control, including precise control of the inductor current on a cycle-by-cycle basis, simpler compensation, and inherent compensation for line voltage variation.

An internal transconductance amplifier establishes an integrated error voltage. The heart of the PWM controller is an open-loop comparator: one input is the integrated voltage-feedback signal; the other consists of the amplified current-sense signal plus slope-compensation ramp. Integrated high-side current sensing is used, which reduces component count and layout risk by eliminating the need to carefully route sensitive external signals. Error-amplifier compensation is also integrated, once again simplifying the power-supply designer's task while eliminating external components.

The controller features a load-line architecture. The output voltage is positioned slightly above nominal regulation at no load and slightly below nominal regulation at full load. As output load changes, a small but controlled amount of load regulation ("load-line") error occurs on the output voltage. This voltage positioning architecture allows the output voltage to respond to sudden load transients in a critically damped manner, and effectively reduces the amount of output capacitance needed when compared to classical integrating controllers. See the

Typical Operating Characteristics section of the data sheet for information about the converter's typical voltage regulation behavior versus load.

The device can operate in either forced-PWM or skip mode. In forced-PWM mode, the converter maintains a constant switching frequency, regardless of load, to allow for easier filtering of the switching noise. The device includes proprietary circuitry that dramatically reduces quiescent current consumption in skip mode, improving light-load efficiency. See the *Forced PWM/Skip Modes* section for further details.

System Enable (EN)

An enable control input (EN) activates the device from its low-power shutdown mode. EN is compatible with inputs from levels down to 2.4V. The high-voltage compatibility allows EN to be connected directly to SUP.

Linear Regulator Output (BIAS)

The device includes a 5V linear regulator output (BIAS) that provides power to the internal circuit blocks. Connect a 1 μ F ceramic capacitor from BIAS to AGND. Do not load this pin externally.

Undervoltage Lockout

When VBIAS drops below the undervoltage-lockout (UVLO) level of $V_{UVLO} = 2.8V$ (typ), the device assumes that the supply voltage is too low for proper operation, so the UVLO circuitry inhibits switching. When VBIAS rises above the UVLO rising threshold, the controller enters the startup sequence and then resumes normal operation.

Startup and Soft-Start

The device features an internal soft-start timer. The output-voltage soft-start ramp time is 6.67ms (typ). If a short circuit or undervoltage is encountered after the soft-start timer has expired, the device is disabled for 16.5ms (typ) and then reattempts soft-start again. This pattern repeats until the short circuit has been removed.

RESET Output

The device features an open-drain $\overline{\text{RESET}}$ output to monitor the output voltage. The $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high (high impedance) after the regulator output increases above 92% of the nominal regulated voltage. $\overline{\text{RESET}}$ goes low

when the regulator output drops to below 90% of the nominal regulated voltage.

Forced PWM/Skip Modes

The device features a logic-level input (MODE) to switch between forced-PWM and skip modes. Connecting MODE to BIAS enables the forced-PWM operation. Connecting MODE to ground, or leaving unconnected, enables skip-mode operation with ultra-low-quiescent current of 1.1 μ A. In skip-mode operation, the converter's switching frequency is load dependent until the output load reaches the skip threshold. At higher load current, the switching frequency does not change and the operating mode is similar to the forced-PWM mode. Skip mode helps improve efficiency in light-load applications by allowing the converter to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the converter does not switch the MOSFETs on and off as often as is the case in the forced-PWM mode. Consequently, the gate charge and switching losses are much lower in skip mode.

Current Limit/Short-Circuit Protection

The device has fault protection designed to protect itself from abnormal conditions. If the output is soft shorted (meaning the output is overloaded but over 25% of regulation), cycle-by-cycle current limit limits how high the inductor current goes for any cycle. If the output is hard shorted to ground and the output falls to less than 25% of regulation, the part goes into a mode where it switches until 15 cycles are ended by current limit, then waits for 16.5ms before trying to soft-start again. This mode of operation limits the amount of power dissipated by the device under these conditions. The device also has overtemperature protection. If the die temperature exceeds approximately 175°C, the device stops switching until the die temperature drops by approximately 15°C and then resumes operation, including going through soft-start again.

Applications Information

Setting the Output Voltage

The device's adjustable output-voltage version (see the *Selector Guide* for more details) allows the user to set the output to any voltage between 1V and 10V. Connect a resistive divider from output (V_{OUT}) to FB to AGND to set the output voltage (Figure 1). Select R₂ (FB to AGND resistor) less than or equal to 100k Ω . Calculate R₁ (V_{OUT} to FB resistor) with the following equation:

$$R_1 = R_2 \times \left[\left(\frac{V_{OUT}}{V_{FB}} \right) - 1 \right]$$

where V_{FB} = 1V (see the *Electrical Characteristics*).

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). To select inductance value, the ratio of inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good compromise between size and loss is a 30% peak-to-peak ripple current to average current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR then determines the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{SUP} - V_{OUT})}{V_{SUP} \times f_{SW} \times I_{OUT} \times LIR}$$

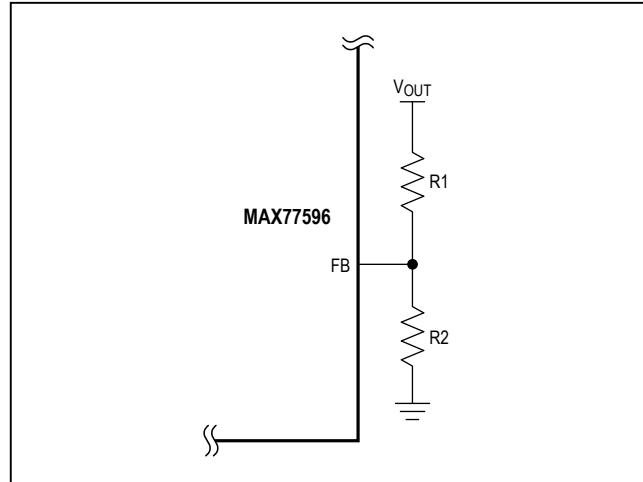


Figure 1. Adjustable Output-Voltage Setting

Table 1. Inductor Values for 300mA Output Current

V _{SUP} /V _{OUT} (V)	14V/5V	14V/3.3V
INDUCTOR (μ H) I _{LOAD} = 300mA	10 μ H (typ) 22 μ H (max)	10 μ H (typ) 22 μ H (max)

where V_{SUP}, V_{OUT}, and I_{OUT} are typical values (so that efficiency is optimum for typical conditions). The switching frequency is 1.7MHz. Table 1 lists some of the inductor values for 300mA output current and several output voltages.

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT} \times (V_{SUP} - V_{OUT})}}{V_{SUP}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{SUP} = 2V_{OUT}$), so $I_{RMS(MAX)} = I_{LOAD(MAX)}/2$.

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input voltage ripple is composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{SUP} - V_{OUT}) \times V_{OUT}}{V_{SUP} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}} \text{ and } D = \frac{V_{OUT}}{V_{SUP}}$$

where I_{OUT} is the maximum output current and D is the duty cycle.

Output Capacitor

The output filter capacitor must have low enough ESR to meet output ripple and load transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions. When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output voltage ripple. Therefore, the size of the output capacitor depends on the maximum ESR required to meet the output voltage ripple ($V_{RIPPLE(P-P)}$) specifications:

$$V_{RIPPLE(P-P)} = ESR \times I_{LOAD(MAX)} \times LIR$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Therefore, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value.

When using low-capacitance filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent voltage droop and voltage rise from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising-load edge is no longer a problem.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low-switching power losses and clean, stable operation. Use a multi-layer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

- 1) The input capacitor (4.7 μ F, see Figures 3 and 4) should be placed immediately next to the SUP pin of the device. Since the device operates at 1.7MHz switching frequency, this placement is critical for effective decoupling of high-frequency noise from the SUP pin.
- 2) Solder the exposed pad to a large copper plane area under the device. To effectively use this copper area as heat exchanger between the PCB and ambient, expose the copper area on the top and bottom sides. Add a few small vias or one large via on the copper pad for efficient heat transfer. Connect the exposed pad to PGND, ideally at the return terminal of the output capacitor.
- 3) Isolate the power components and high-current path from the sensitive analog circuitry. Doing so is essential to prevent any noise coupling into the analog signals.
- 4) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- 5) Connect PGND and AGND together at the return terminal of the output capacitor. Do not connect them anywhere else.
- 6) Keep the power traces and load connections short. This practice is essential for high efficiency.
- 7) Place the BIAS capacitor ground next to the AGND pin and connect with a short and wide trace.

Typical Application Circuits

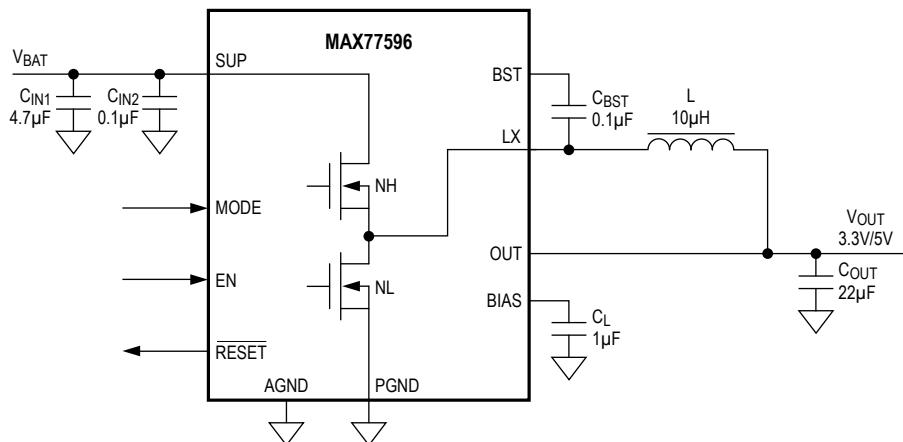


Figure 2. MAX77596ETBA+/MAX77596ETBB+, Fixed Output Voltage (3.3V/5V), 10-Pin TDFN

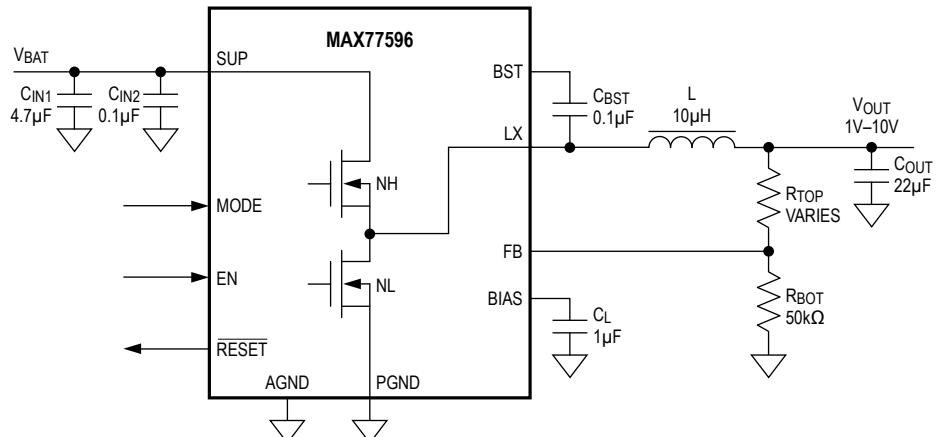


Figure 3. MAX77596ETBC+, Variable Output Voltage, 10-Pin TDFN

Ordering Information

PART	V _{OUT}	PIN-PACKAGE
MAX77596ETBA+	Fixed 5V	10 TDFN-EP*
MAX77596ETBB+	Fixed 3.3V	10 TDFN-EP*
MAX77596ETBC+	Adjustable	10 TDFN-EP*

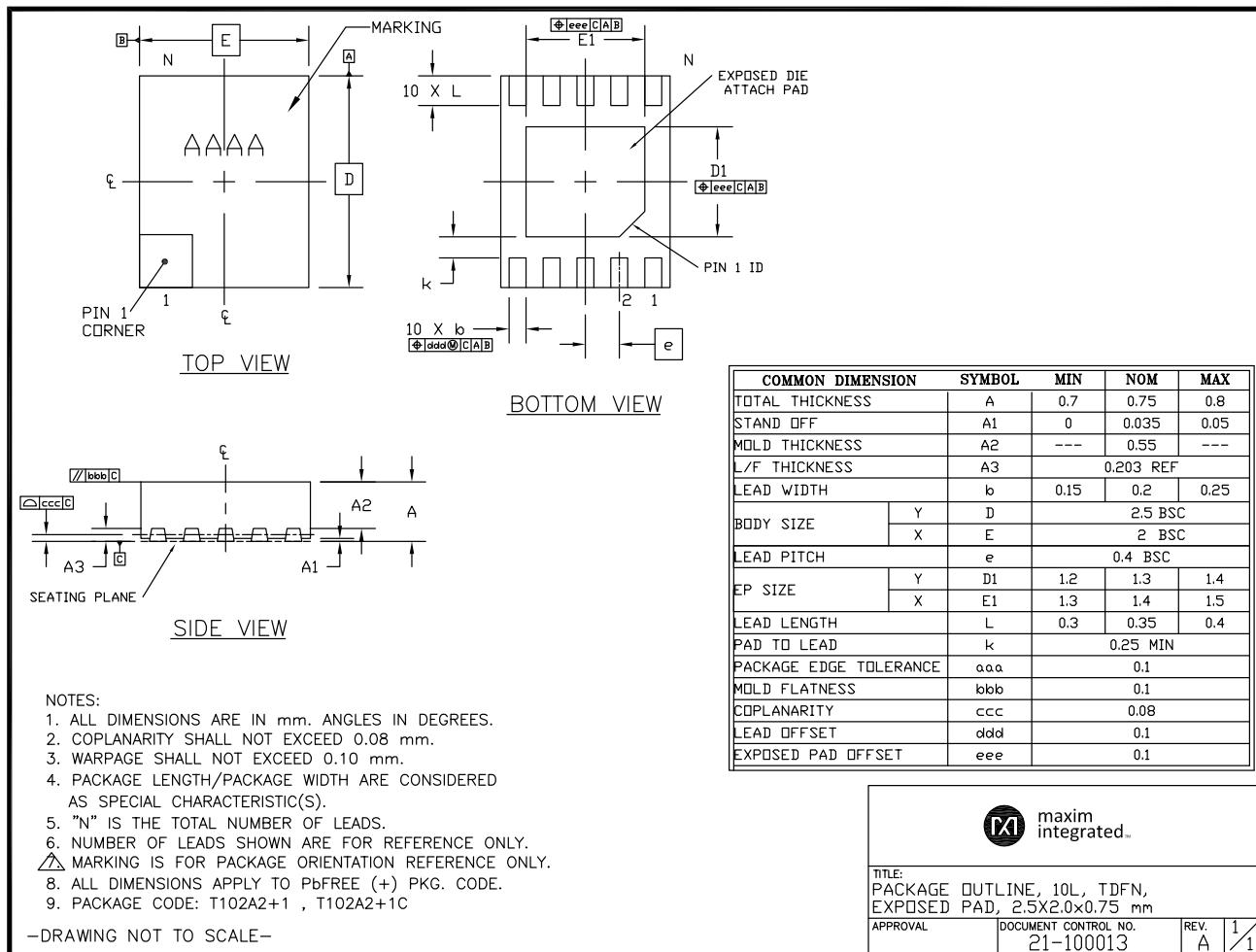
*EP = Exposed pad.

+Denotes a lead(Pb)-free/RoHS-compliant package.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 TDFN	T102A2+1C	21-100013	—



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/15	Initial release	—
1	3/16	Updated <i>General Description, Benefits and Features, Electrical Characteristics, Typical Operating Characteristics, Block Diagram, Detailed Description, Figure 2 caption, Figure 3, and Ordering Information</i>	1, 4–7, 9, 10, 13, 14

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