

Low-Power Dual-/Triple-Voltage SC70 µP Supervisory Circuits

General Description

The MAX6736–MAX6745 are low-power dual-/triplevoltage microprocessor (μ P) supervisors. These devices assert a reset if any monitored supply falls below its factory-trimmed or adjustable threshold and maintain reset for a minimum timeout period after all supplies rise above their thresholds. The integrated dual/triple supervisory circuits significantly reduce size and power compared to separate ICs or discrete components. The low supply current of 6µA makes these devices ideal for portable equipment.

The MAX6736/MAX6737 are dual fixed-voltage μ P supervisors with a manual reset input. The MAX6738/MAX6739 have one fixed and one adjustable reset threshold and a manual reset input. The MAX6740/MAX6743 are triple-voltage μ P supervisors with two fixed and one user-adjustable reset threshold inputs. The MAX6741/MAX6744 are dual-voltage μ P supervisors with a power-OK (POK) output ideal for power-supply sequencing. The MAX6742/MAX6745 monitor the primary V_{CC} supply and have an independent power-fail comparator.

The MAX6736–MAX6745 monitor I/O supply voltages (V_{CC1}) from 1.8V to 5.0V and core supply voltages (V_{CC2}) from 0.9V to 3.3V with factory-trimmed reset threshold voltage options (Table 1). An external adjustable RSTIN input option allows monitoring voltages down to 0.5V.

A variety of push-pull or open-drain reset outputs along with manual reset input and power-fail input/output features are available (see the *Selector Guide*). The MAX6736–MAX6745 are offered in a space-saving 5-pin SC70 package and operate over the -40°C to +85°C temperature range.

	Applications
Portable/Battery-	Controllers
Powered Equipment	PDAs
Multivoltage Systems	GPS Equipment
Notebook Computers	POS Equipment

_Features

- Dual-/Triple-Supply Reset Voltage Monitors
- Precision Factory-Set Reset Thresholds for Monitoring from 0.9V to 5.0V
- Adjustable Reset Input Down to 0.488V
- 150ms and 1200ms (min) Reset Timeout Period Options
- V_{CC}1 Power-OK Output for Power-Supply Sequencing Applications (MAX6741/MAX6744)
- Power-Fail Input/Power-Fail Output (MAX6742/MAX6745)
- ♦ 6µA Supply Current
- Tiny SC70 Package

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX6736XKDT	-40°C to +85°C	5 SC70-5
MAX6737XKDT	-40°C to +85°C	5 SC70-5

Note: The first "__" or "_" are placeholders for the threshold voltage levels of the devices. Desired threshold levels are set by the part number suffix found in Tables 1 and 2. The "_" after the D is a placeholder for the reset timeout period suffix found in Table 3. For example, the MAX6736XKLTD3-T is a dual-voltage supervisor $V_{TH}1 = 4.625V$, $V_{TH}2 = 3.075V$, and a 150ms minimum reset timeout period. All devices are available in tape-and-reel only. There is a 2500-piece minimum order increment for standard versions (see Table 1). Sample stock is typically held on standard versions only. Nonstandard versions require a minimum order increment of 10,000 pieces. Contact factory for availability.

Devices are available in both leaded and lead-free packaging. Specify lead-free by replacing "-T" with "+T" when ordering.

Ordering Information and Selector Guide continued at end of data sheet.

Pin Configurations, Typical Application Circuits, and Functional Diagram appear at end of data sheet.

Selector Guide

PART	VOLTAGE MONITORS	OPEN-DRAIN RESET	PUSH-PULL RESET	MANUAL RESET	POWER-FAIL INPUT/ OUTPUT	POK OUTPUT	RSTIN INPUT
MAX6736	2 fixed	Х	—	Х	—	_	_
MAX6737	2 fixed	—	Х	Х	—		
MAX6738	1 fixed, 1 adj	Х		Х	_	_	Х

*Manual reset detect on RESET output.

Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

Vcc1, Vcc2, POK1 to GND	-0.3V to +6V
Open-Drain RESET, PFO to GND	0.3V to +6V
Push-Pull RESET to GND	0.3V to (V _{CC} 1 + 0.3V)
MR, RSTIN, PFI to GND	0.3V to (V _{CC} 1 + 0.3V)
Input/Output Current, All Pins	
Continuous Power Dissipation (T _A =	+70°C)
5-Pin SC70 (derate 3.1mW/°C ab	ove $+70^{\circ}C$) 247mW

Operating Temperature Range	40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.2V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL		MIN	ТҮР	МАХ	UNITS		
	V _{CC} 1,	$T_A = -40^{\circ}C$ to $0^{\circ}C$		1.2		5.5	V	
Operating voltage hange	V _{CC} 2	$T_{A} = 0^{\circ}C \text{ to } +88$	5°C	1.0		5.5	v	
V. d. Gurralia Querrant	1	V _{CC} 1 = 3.3V, V not asserted	$C_{CC}1 > V_{CC}2$, no load, reset		5	10		
VCCT Supply Current	ICC I	V _{CC} 1 = 1.8V, V not asserted	$C_{CC1} < V_{CC2}$, no load, reset		5	10	μΑ	
V O Guarda O arrest		V _{CC} 2 = 1.8V, V not asserted	CC2 < VCC1, no load, reset		1	2		
VCC2 Supply Current	ICC2	V _{CC} 2 = 3.3V, V not asserted		10	20	μA		
			$T_A = 0^{\circ}C$ to $+85^{\circ}C$	4.500	4.625	4.750		
	V=1	MAX67L	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	4.425		4.825		
		MAX67M	$T_A = 0^{\circ}C$ to $+85^{\circ}C$	4.250	4.375	4.500		
			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	4.175		4.575		
		MAX67T	$T_A = 0^{\circ}C \text{ to } +85^{\circ}C$	3.000	3.075	3.150		
			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	2.950		3.200		
		MAX67S	$T_A = 0^{\circ}C \text{ to } +85^{\circ}C$	2.850	2.925	3.000		
			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	2.800		3.050		
Reset Threshold for Voc1		MAX67R	$T_A = 0^{\circ}C \text{ to } +85^{\circ}C$	2.550	2.625	2.700		
	V U		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	2.505		2.745	v	
		MAX67 7	$T_A = 0^{\circ}C \text{ to } +85^{\circ}C$	2.250	2.313	2.375		
			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	2.213		2.413		
		MAX67 Y	$T_A = 0^{\circ}C$ to $+85^{\circ}C$	2.125	2.188	2.250		
			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	2.088		2.288		
		MAX67 W	$T_A = 0^{\circ}C$ to $+85^{\circ}C$	1.620	1.665	1.710		
			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	1.593		1.737		
		MAX67 V	$T_A = 0^{\circ}C$ to $+85^{\circ}C$	1.530	1.575	1.620		
			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	1.503		1.647		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 1.2V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	ТҮР	MAX	UNITS
			$T_A = 0^{\circ}C$ to $+85^{\circ}C$	3.000	3.075	3.150	
		MAX671	$T_A = -40^{\circ}C$ to $+85^{\circ}C$	2.905		3.050	
			$T_A = 0^{\circ}C$ to +85°C	2.850	2.925	3.000	
		MAX675	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	2.800		3.050	
			$T_A = 0^{\circ}C$ to $+85^{\circ}C$	2.550	2.625	2.700	
		WAX67R	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	2.505		2.745	
			$T_A = 0^{\circ}C$ to $+85^{\circ}C$	2.250	2.313	2.375	
		MAX67Z	$T_A = -40^{\circ}C$ to $+85^{\circ}C$	2.213		2.413	
			$T_A = 0^{\circ}C$ to +85°C	2.125	2.188	2.250	
		MAX67Y	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	2.088		2.288	
			$T_A = 0^{\circ}C$ to $+85^{\circ}C$	1.620	1.665	1.710	
		IVIAX67VV	$T_A = -40^{\circ}C$ to $+85^{\circ}C$	1.593		1.737	
			$T_A = 0^{\circ}C$ to +85°C	1.530	1.575	1.620	
Reset Threshold for V _{CC} 2	VTH2	WAX67V	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	1.503		1.647	V
			$T_A = 0^{\circ}C$ to $+85^{\circ}C$	1.350	1.388	1.425	
		MAX67I	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	1.328		1.448	
		MAX67H	$T_A = 0^{\circ}C$ to +85°C	1.275	1.313	1.350	
			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	1.253		1.373	
		MAX67G	$T_A = 0^{\circ}C$ to +85°C	1.080	1.110	1.140	
			$T_A = -40^{\circ}C$ to $+85^{\circ}C$	1.062		1.158	
		MAX67F	$T_A = 0^{\circ}C$ to $+85^{\circ}C$	1.020	1.050	1.080	
			$T_A = -40^{\circ}C$ to $+85^{\circ}C$	1.002		1.098	
		MAX67E	$T_A = 0^{\circ}C$ to +85°C	0.810	0.833	0.855	
			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	0.797		0.869	
			$T_A = 0^{\circ}C \text{ to } + 85^{\circ}C$	0.765	0.788	0.810	
		MAX67D	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	0.752		0.824	
RSTIN Threshold (MAX6738/		$T_A = 0^{\circ}C$ to +8	5°C	0.476	0.488	0.500	V
MAX6739/MAX6740/MAX6743)	VTH-RSTIN	$T_A = -40^{\circ}C$ to +	-85°C	0.468		0.507	v
RSTIN Input Current		V _{RSTIN} ≥ 0.1V (Note 2)	-10		+10	nA
Reset Threshold Hysteresis		V _{TH} 1, V _{TH} 2, RS	STIN, PFI		0.5		%
		V _{CC} 1 ≥ 1.0V, Is +85°C	$SINK = 50\mu A$, $T_A = 0^{\circ}C$ to			0.3	
RESET, POK1 Output Low	Vol	V _{CC} 1 ≥ 1.2V, Is	SINK = 100µA			0.3	V
		$V_{CC}1 \ge 2.13V$,	I _{SINK} = 1.2mA			0.3	
		$V_{CC1} \ge 4.25V, I_{SINK} = 3.2mA,$				0.4	
DESET Output High (Bush Bull)	Vou	$V_{CC}1 \ge 2.38V$, deasserted	$CC1 \ge 2.38V$, ISOURCE = 500µA, output leasserted				V
neser Output nigh (rush-rull)	∨он	$V_{CC}1 \ge 4.75V$, deasserted	$V_{CC}1 \ge 4.75V$, $I_{SOURCE} = 800\mu$ A, output deasserted				V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 1.2V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS
RESET Output Open-Drain Leakage Current (MAX6736/MAX6738)	Ilkg	Output not asserted low (Note 2)			500	nA
POK1 Output Open-Drain Leakage		Output not asserted low (Note 2)			500	nA
V _{CC} Reset Delay	t _{RD}	V _{CC} 1, V _{CC} 2, or RSTIN falling at 10mV/µs from V _{TH} + 100mV to V _{TH} - 100mV		35		μs
V _{CC} Reset Timeout Period	top	MAX67XKD3	150	225	300	
(Note 3)	ιRΡ	MAX67XKD7	1200	1800	2400	ms
MANUAL RESET (MAX6736–MA)	(6739 only)					
MR to V _{CC} 1 Internal Pullup Impedance			0.75	1.5	3.00	kΩ
MR Timeout Period	t _{MRP}	Both D3 and D7 timing options	150	225	300	ms
MR Minimum Input Pulse Width	t _{MPW}		1			μs
MR Glitch Rejection				100		ns
	VIL				0.3 × V _{CC} 1	V
INIT INPUL VOILAGE	VIH		0.8 × V _{CC} 1			v
MR to RESET Delay				300		ns
V _{CC} 1 POWER-OK OUTPUT (MAX	6741/MAX67	44 only)				
POK1 Timeout Period	tрокр		37.5	56.25	75.0	ms
PUSHBUTTON RESET (MAX6740	/MAX6741/M	IAX6742 only)				
RESET to V _{CC} 1 Internal Pullup Impedance			25	50	100	kΩ
Manual Reset Detect Debounce Period	tDEB	(Note 4)	37.5	56.25	75.0	ms
Manual Reset Timeout		MAX67XKD3	150	225	300	
Period (Note 3)		MAX67XKD7	1200	1800	2400	ms
Manual Reset Minimum Input Pulse Width	t _{MPW}	(Note 4)	1			μs
Manual Reset Release Detect Threshold		(Note 4)		0.5 × V _{CC} 1		V
Manual Reset Glitch Rejection		(Note 4)		100		ns
Manual Reset to RESET Delay				300		ns



ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 1.2V to 5.5V, $T_A = -40^{\circ}$ C to +85°C, unless otherwise noted. Typical values are at $T_A = +25^{\circ}$ C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS		
POWER-FAIL COMPARATOR (MAX6742/MAX6745 only)								
Dower Fail In Threshold (Nieto E)		$T_A = 0^{\circ}C \text{ to } +85^{\circ}C$	0.476	0.488	0.500	V		
Fower Fail III Threshold (Note 5)	VIH-PH	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	0.468		0.507	v		
Power Fail In Current	IPFI	$V_{PFI} \ge 0.1V$ (Note 2)	-10		+10	nA		
		V _{CC} 1 ≥ 1.53V, I _{SINK} = 500µA			0.3			
PFO Output Low	V _{OL}	$V_{CC}1 \ge 2.03V$, $I_{SINK} = 1.2mA$			0.3	V		
		$V_{CC}1 \ge 4.25V$, $I_{SINK} = 3.2mA$			0.4			
PFI to PFO Propagation Delay	tP	PFI falling at 10mV/µs from V _{TH-PFI} + 100mV to V _{TH-PFI} - 100mV or rising at 10mV/µs from V _{TH-PFI} - 100mV to V _{TH-PFI} + 100mV (Note 5)		35		μs		
PFO Startup Delay		To output valid (Note 5)		5		ms		

Note 1: All devices are 100% tested at $T_A = +25^{\circ}C$. All temperature limits are guaranteed by design.

Note 2: Guaranteed by design.

 $(T_A = +25^{\circ}C, unless otherwise noted.)$

Note 3: t_{RD} timeout period begins after POK1 timeout period (t_{POKP}) and V_{CC}2 ≥ V_{TH}2 (max) (MAX6741/MAX6744).

Note 4: Refers to the manual reset function obtained by forcing the RESET output low.

Note 5: $V_{CC}1 \ge 1.6V$.



Typical Operating Characteristics



SUPPLY CURRENT (µA)

Typical Operating Characteristics (continued)

 $(T_A = +25^{\circ}C, \text{ unless otherwise noted.})$















V_{CC} TO RESET OUTPUT DELAY vs. TEMPERATURE



POWER-FAIL INPUT TO POWER-FAIL OUTPUT DELAY vs. TEMPERATURE





Typical Operating Characteristics (continued)

 $(T_A = +25^{\circ}C, \text{ unless otherwise noted.})$









OUTPUT HIGH VOLTAGE vs. Source current





Pin Description

PIN						
MAX6736 MAX6737	MAX6738 MAX6739	MAX6740 MAX6743	MAX6741 MAX6744	MAX6742 MAX6745	NAME	FUNCTION
1	1	1	1	1	RESET	Reset Output, Push-Pull or Open Drain Active Low. $\overline{\text{RESET}}$ changes from high to low when any monitored power-supply input (V _{CC} 1, V _{CC} 2, RSTIN) drops below its selected reset threshold. It remains low until all monitored power-supply inputs exceed their selected reset thresholds for the V _{CC} reset timeout period. $\overline{\text{RESET}}$ is forced low if $\overline{\text{MR}}$ is low for at least the $\overline{\text{MR}}$ minimum input pulse width. It remains low for the $\overline{\text{MR}}$ reset timeout period after $\overline{\text{MR}}$ goes high. The pushpull output is referenced to V _{CC} 1. The MAX6736/MAX6738 open-drain outputs require an external pullup resistor. The MAX6740/MAX6741/MAX6742 open-drain outputs have an internal 50k Ω pullup resistor to V _{CC} 1 and provide a manual reset function.
2	2	2	2	2	GND	Ground
3	3				MR	Manual Reset, Active Low. Pull low for at least $\overline{\text{MR}}$ minimum input pulse width to force $\overline{\text{RESET}}$ low. Reset remains active as long as $\overline{\text{MR}}$ is low and for the $\overline{\text{MR}}$ reset timeout period after $\overline{\text{MR}}$ goes high. There is an internal 1.5k Ω pullup resistor to V _{CC} 1.
4	_	4	4	_	V _{CC} 2	Voltage Input 1. Power supply and input for the secondary μP voltage reset monitor.
	4	3		Adjustable Reset Threshold Input. R RSTIN RSTIN is below the internal 0.488V re adjustable reset threshold with an ex network. Connect RSTIN to V _{CC} 1 if u		Adjustable Reset Threshold Input. RESET is asserted when RSTIN is below the internal 0.488V reference level. Set the adjustable reset threshold with an external resistor-divider network. Connect RSTIN to V _{CC} 1 if unused.
5	5	5	5	5	V _{CC} 1	Voltage Input 2. Power supply and input for the primary μP voltage reset monitor.
	_	_	_	4	PFI	Power-Fail Comparator Input. PFO is asserted when PFI is below 0.488V. PFO is deasserted without any reset timeout period when PFI goes above 0.488V. Connect PFI to an external resistor network to set the desired monitor threshold.
	_	_	_	3	PFO	Power-Fail Comparator Output, Open Drain Active Low. PFO is asserted when PFI is below 0.488V.
_			3	_	POK1	$V_{CC}1$ Power-OK Output, Open Drain Active High. POK1 remains low as long as $V_{CC}1$ is below $V_{TH}1$. POK1 output goes high after $V_{CC}1$ exceeds $V_{TH}1$ for the POK1 timeout period. POK1 logic is independent of the \overline{MR} or $V_{CC}2$ inputs. The output can be used to control $V_{CC}1$ -to- $V_{CC}2$ supply sequencing.



Table 1. Reset Voltage Threshold Suffix Guide for MAX6736/MAX6737/MAX6740/ MAX6741/MAX6743/MAX6744

PART NO. SUFFIX ()	V _{CC} 1 NOMINAL VOLTAGE THRESHOLD (V)	V _{CC} 2 NOMINAL VOLTAGE THRESHOLD (V)	PART NO. SUFFIX ()	V _{CC} 1 NOMINAL VOLTAGE THRESHOLD (V)	V _{CC} 2 NOMINAL VOLTAGE THRESHOLD (V)
LT	4.625	3.075	RD	2.625	0.788
MS	4.375	2.925	ZW	2.313	1.665
MR	4.375	2.625	ZI	2.313	1.388
TZ	3.075	2.313	ZG	2.313	1.110
TW	3.075	1.665	ZE	2.313	0.833
TI	3.075	1.388	YV	2.188	1.575
TG	3.075	1.110	YH	2.188	1.313
TE	3.075	0.833	YF	2.188	1.050
SY	2.925	2.188	YD	2.188	0.788
SV	2.925	1.575	wт	1.665	3.075
SH	2.925	1.313	WI	1.665	1.388
SF	2.925	1.050	WG	1.665	1.110
SD	2.925	0.788	WE	1.665	0.833
RY	2.625	2.188	VR	1.575	2.625
RV	2.625	1.575	VH	1.575	1.313
RH	2.625	1.313	VF	1.575	1.050
RF	2.625	1.050	VD	1.575	0.788

Note: Standard versions, shown in bold, are available in the D3 timeout option only. Samples are typically held on standard versions only. There is a 10,000-piece order increment on nonstandard versions. **Other threshold voltage combinations may be available; contact factory for availability.**

Table 2. Reset Voltage Threshold SuffixGuide for MAX6738/MAX6739/MAX6742/MAX6745

PART NO. SUFFIX (_)	V _{CC} 1 NOMINAL VOLTAGE THRESHOLD (V)
L	4.625
М	4.375
Т	3.075
S	2.925
R	2.625
Z	2.313
Y	2.188
W	1.665
v	1.575

Note: Standard versions, shown in bold, are available in the D3 timeout option only. Samples are typically held on standard versions only. There is a 10,000-piece order increment on non-standard versions. **Other threshold voltages may be available; contact factory for availability**.

Table 3. VCC Timeout Period SuffixGuide

TIMEOUT PERIOD SUFFIX	ACTIVE TIMEOUT PERIOD			
	MIN (ms)	MAX (ms)		
D3	150	300		
D7	1200	2400		





Figure 1. Timing Diagram

Detailed Description

Supply Voltages

The MAX6736-MAX6745 µP supervisory circuits maintain system integrity by alerting the µP to fault conditions. These devices are optimized for systems that monitor two or three supply voltages. The reset output state is guaranteed to remain valid while either V_{CC}1 or VCC2 is above 1.2V.

Threshold Levels

The MAX6736/MAX6737/MAX6740/MAX6741/MAX6743/ MAX6744 input voltage threshold combinations are indicated by a two-letter code in Table 1. The MAX6738/ MAX6739/MAX6742/MAX6745 input voltage thresholds are indicated by a one-letter code in Table 2. Contact the factory for the availability of other voltage thresholds.

Reset Output

The MAX6736-MAX6745 provide an active-low reset output (RESET). RESET is asserted when the voltage at either V_{CC}1 or V_{CC}2 falls below the voltage threshold level, RSTIN drops below the threshold, or MR is pulled low. Once reset is asserted, it stays low for the reset timeout period. If V_{CC}1, V_{CC}2, or RSTIN goes below the reset threshold before the reset timeout period is completed, the internal timer restarts. The MAX6736/MAX6738/ MAX6740/MAX6741/MAX6742 have open-drain reset outputs, while the MAX6737/MAX6739/MAX6743/MAX6744/ MAX6745 have push-pull reset outputs (Figure 1).

The MAX6740/MAX6741/MAX6742 include a RESET output with a manual reset detect function. The opendrain RESET output has an internal 50k Ω pullup to V_{CC}1. The RESET output is low while the output is pulled to GND and remains low for at least the manual reset timeout period after the external GND pulldown is



\/



Figure 2. MAX6740/MAX6741/MAX6742 Manual Reset Timing Diagram

released. The manual reset detect function is internally debounced for the t_{DEB} timeout period, so the output can be connected directly to a momentary pushbutton switch, if desired (Figure 2).

Manual Reset Input

Many microprocessor-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset while the monitored supplies remain above their reset thresholds. The MAX6736–MAX6739 have a dedicated active-low MR input. The RESET is asserted low while MR is held low and remains asserted for the manual reset timeout period after MR returns high. The MR input has an internal 1.5k Ω pullup resistor to V_{CC1} and can be left unconnected if not used. MR can be driven with CMOS logic levels, open-drain/open-collector outputs, or a momentary pushbutton switch to GND to create a manual reset function.

Adjustable Input Voltage

The MAX6738/MAX6739 and MAX6740/MAX6743 provide an additional input to monitor a second or third system voltage. The threshold voltage at RSTIN is typi-



Figure 3. Monitoring an Additional Voltage

cally 488mV. Connect a resistor-divider network to the circuit as shown in Figure 3 to establish an externally controlled threshold voltage, V_{EXT TH}.

Low leakage current at RSTIN allows the use of largevalued resistors, resulting in reduced power consumption of the system.

Power-Fail Comparator

PFI is the noninverting input to an auxiliary comparator. A 488mV internal reference (V_{TH-PFI}) is connected to the inverting input of the comparator. If PFI is less than 488mV, PFO is asserted low. PFO deasserts without a timeout period when PFI rises above the externally set threshold. Common uses for the power-fail comparator include monitoring for low battery conditions or a failing DC-DC converter input voltage (see the *Typical Application Circuits*). The asserted PFO output can place a system in a low-power suspend mode or support an orderly system shutdown before monitored V_{CC} voltages drop below the reset thresholds. Connect PFI to an external resistor-divider network as shown in Figure 4 to set the desired trip threshold. Connect PFI to V_{CC}1 if unused.

Applications Information

Interfacing to the µP with Bidirectional Reset Pins

Most microprocessors with bidirectional reset pins can interface directly to open-drain RESET output options. Systems simultaneously requiring a push-pull RESET output and a bidirectional reset interface can be in logic contention. To prevent contention, connect a 4.7k Ω resistor between RESET and the μ P's reset I/O port as shown in Figure 5.



Figure 4. Using Power-Fail Input to Monitor an Additional Power Supply

Adding Hysteresis to the Power-Fail Comparator

The power-fail comparator has a typical input hysteresis of 2.5mV. This is sufficient for most applications in which a power-supply line is being monitored through an external voltage-divider. If additional noise margin is desired, connect a resistor between PFO and PFI, as



Figure 5. Interfacing to µPs with Bidirectional Reset I/O

shown in Figure 6. Select the values of R1, R2, and R3 such that PFI sees V_{TH-PFI} (488mV) when V_{EXT} falls to its power-fail trip point (V_{FAIL}) and when V_{EXT} rises to its power-good trip point (V_{GOOD}). The hysteresis window extends between the specified V_{FAIL} and V_{GOOD} thresholds. R3 adds the additional hysteresis by sinking current from the R1/R2 divider network when the PFO output is logic low and sourcing current into the network when PFO is logic high. R3 is typically an order of magnitude greater than R1 or R2.

The current through R2 should be at least 1µA to ensure that the 10nA (max) PFI input current does not significantly shift the trip points. Therefore, for most applications:

 $\label{eq:response} \begin{array}{l} R2 < VTH-PFI \ / \ 1mA < 0.488V \ / \ 1mA < 488k\Omega \\ \hline \hline PFO \ is an open-drain output requiring an external pullup resistor, R4. Select R4 to be less than 1% of R3. \\ V_{GOOD} = DESIRED \ V_{EXT} \ GOOD \ VOLTAGE \ THRESHOLD \\ V_{FAIL} = DESIRED \ V_{EXT} \ FAIL \ VOLTAGE \ THRESHOLD \\ V_{PU} = \ V_{PULLUP} \ (FOR \ OPEN-DRAIN \ \overline{PFO}) \\ R2 = 488k\Omega \ (FOR > 1\muA \ R2 \ CURRENT) \end{array}$

$$R1 = R2 \frac{\left(V_{GOOD} - V_{TH-PFI}\right) - \frac{\left(V_{TH-PFI}(V_{GOOD} - V_{FAIL}\right)}{V_{PU}}}{V_{TH - PFI}}$$

$$\label{eq:R3} \begin{split} \text{R3} &= (\text{R1} \times \text{V}_{\text{PU}}) \, / \, (\text{V}_{\text{GOOD}} - \text{V}_{\text{FAIL}}) \\ \text{R4} &\leq 0.01 \times \text{R3} \end{split}$$

Power Sequencing Applications

Many dual-voltage processors/ASICs require specific power-up/power-down sequences for the I/O and core supplies.



Figure 6. Adding Hysteresis to Power Fail for Push-Pull PFO



The MAX6741/MAX6744 offer a V_{CC1} POK (POK1) ideal for V_{CC1}-to-V_{CC2} sequencing. POK1 remains low as long as V_{CC1} is below its V_{TH1} threshold. When V_{CC1} exceeds V_{TH1} for the POK1 timeout period (t_{POKP}), the open-drain POK1 output is deasserted. The POK1 output can then enable the V_{CC2} power supply (use an external POK1 pullup resistor). RESET is deasserted when both V_{CC1} and V_{CC2} remain above their selected thresholds for the reset timeout period (t_{RP}). The POK1 output can be used for I/O before core or core before I/O sequencing, depending on the selected V_{CC1}/V_{CC2} thresholds. See the *Typical Application Circuit* and Figure 1.

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using the circuit shown in Figure 4. When the negative supply is valid, \overrightarrow{PFO} is low. When the negative supply voltage drops, \overrightarrow{PFO} goes high. The circuit's accuracy is affected by the PFI threshold tolerance, V_{CC}, R1, and R2.

Transient Immunity

The MAX6736–MAX6745 supervisors are relatively immune to short-duration falling V_{CC} transients (glitches). It is usually undesirable to reset the μ P when V_{CC} experiences only small glitches. The *Typical Operating Characteristics* show Maximum V_{CC1}/V_{CC2} Transient Duration vs. Reset Threshold Overdrive, for which reset pulses are not generated. The graph shows the maximum pulse width that a falling V_{CC} transient might typically have without causing a reset pulse to be issued. As the amplitude of the transient increases, the maximum allowable pulse width decreases. A 0.1µF bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

Chip Information

TRANSISTOR COUNT: 249 PROCESS: BICMOS



Functional Diagram

Selector Guide (continue							ntinued)
PART	VOLTAGE MONITORS	OPEN-DRAIN RESET	PUSH-PULL RESET	MANUAL RESET	POWER-FAIL INPUT/ OUTPUT	POK OUTPUT	RSTIN INPUT
MAX6739	1 fixed, 1 adj	—	Х	Х	—		Х
MAX6740	2 fixed, 1 adj	Χ*	—	Х*			Х
MAX6741	2 fixed	Х*	—	Х*	_	Х	_
MAX6742	1 fixed	Χ*	—	Χ*	Х		
MAX6743	2 fixed, 1adj	—	Х	_	_		Х
MAX6744	2 fixed	—	Х	_	—	Х	_
MAX6745	1 fixed	—	Х	_	Х	_	_

*Manual reset detect on RESET output.



Typical Application Circuits



Pin Configurations

MAX6736-MAX6745



Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX6738XK_DT	-40°C to +85°C	5 SC70-5
MAX6739XK_DT	-40°C to +85°C	5 SC70-5
MAX6740XKDT	-40°C to +85°C	5 SC70-5
MAX6741XKDT	-40°C to +85°C	5 SC70-5
MAX6742XK_DT	-40°C to +85°C	5 SC70-5
MAX6743XKDT	-40°C to +85°C	5 SC70-5
MAX6744XKDT	-40°C to +85°C	5 SC70-5
MAX6745XK_DT	-40°C to +85°C	5 SC70-5

Note: The first "__" or "_" are placeholders for the threshold voltage levels of the devices. Desired threshold levels are set by the part number suffix found in Tables 1 and 2. The "_" after the D is a placeholder for the reset timeout period suffix found in Table 3. For example, the MAX6736XKLTD3-T is a dual-voltage supervisor $V_{TH}1 = 4.625V$, $V_{TH}2 = 3.075V$, and a 150ms minimum reset timeout period. All devices are available in tape-and-reel only. There is a 2500-piece minimum order increment for standard versions (see Table 1). Sample stock is typically held on standard versions only. Nonstandard versions require a minimum order increment of 10,000 pieces. Contact factory for availability.

Devices are available in both leaded and lead-free packaging. Specify lead-free by replacing "-T" with "+T" when ordering.

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Printed USA

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

MAXIM is a registered trademark of Maxim Integrated Products, Inc.

MAX6736-MAX6745

16

© 2005 Maxim Integrated Products

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX6736XKRVD7+	MAX6736XKSFD3+T	MAX6736XKTWD7+	MAX6736XKVDD3+	MAX6736XKZGD3+T
MAX6736XKZWD3+T	MAX6737XKSFD3+T	MAX6737XKSVD3+T	MAX6737XKTGD3+T	MAX6744XKSHD3+T
MAX6744XKSVD3+T	MAX6737XKSHD3+T	MAX6737XKTZD3+T	MAX6736XKTGD3+T	MAX6744XKTZD3+T
MAX6737XKZGD3+T	MAX6736XKSHD3+T	MAX6737XKZWD3+T	MAX6736XKSDD3+T	MAX6744XKWTD3+T
MAX6736XKYHD3+T	MAX6744XKYHD3+T	MAX6741XKVHD3+T	MAX6736XKSYD3+T	MAX6736XKVRD3+T
MAX6737XKVRD3+T	MAX6736XKYDD3+T	MAX6736XKRVD3+T	MAX6736XKLTD3+T	MAX6736XKWGD3+T
MAX6736XKVHD3+T	MAX6736XKSVD3+T	MAX6744XKZGD3+T	MAX6736XKWTD3+T	MAX6744XKYDD3+T
MAX6740XKWTD3+T	MAX6744XKWGD3+T	MAX6736XKSHD3+		