MAX618 — 28V Internal Switch, Step-Up DC-DC Converter

General Description

The MAX618 CMOS, PWM, step-up DC-DC converter generates output voltages up to 28V and accepts inputs from +3V to +28V. An internal 2A, 0.3Ω switch eliminates the need for external power MOSFETs while supplying output currents up to 500mA or more. A PWM control scheme combined with Idle Mode™ operation at light loads minimizes noise and ripple while maximizing efficiency over a wide load range. No-load operating current is 500µA, which allows efficiency up to 93%.

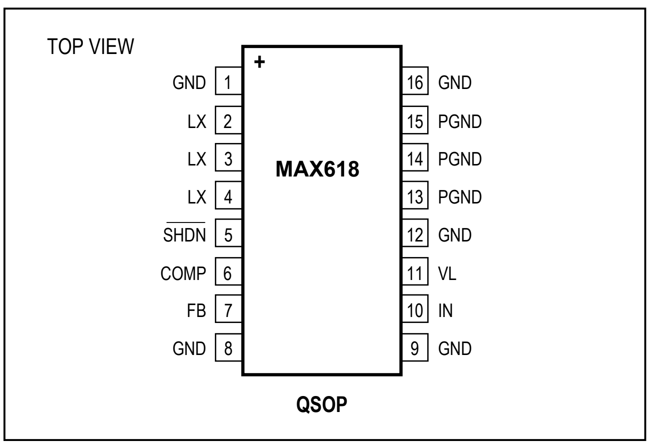
A fast 250kHz switching frequency allows the use of small surface-mount inductors and capacitors. A shutdown mode extends battery life when the device is not in use. Adaptive slope compensation allows the MAX618 to accommodate a wide range of input and output voltages with a simple, single compensation capacitor.

The MAX618 is available in a thermally enhanced 16-pin QSOP package that is the same size as an industry-standard 8-pin SO but dissipates up to 1W. An evaluation kit (MAX618EVKIT) is available to help speed designs.

Applications

- Industrial +24V and +28V Systems
- LCD Displays
- Palmtop Computers

Pin Configuration



Idle Mode is a trademark of Maxim Integrated Products, Inc.

Features

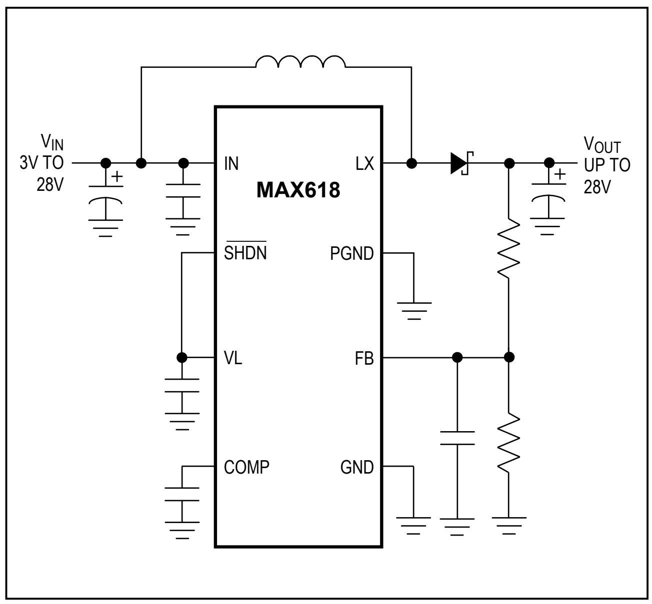
- Adjustable Output Voltage Up to +28V
- Up to 93% Efficiency
- Wide Input Voltage Range (+3V to +28V)
- Up to 500mA Output Current at +12V
- 500µA Quiescent Supply Current
- 3µA Shutdown Current
- 250kHz Switching Frequency
- Small 1W, 16-Pin QSOP Package

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX618EEE+	-40°C to +85°C	16 QSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Typical Application Circuit



Absolute Maximum Ratings

IN to GND ....-0.3V to +30V
LX to GND ....-0.3V to +30V
VL to GND ....-0.3V to +6V
$\overline{SHDN}$, COMP, FB to GND ....-0.3V to (VL + 0.3V)
PGND to GND...±0.3V

Continuous Power Dissipation (T_A = +70°C) (Note 1)
16-Pin QSOP (derate 15mW/°C above +70°C)..................1W
Operating Temperature Range ....-40°C to +85°C
Junction Temperature..+150°C
Storage Temperature Range ....-65°C to +150°C
Soldering Temperature (reflow) ....+260°C

Note 1: With part mounted on 0.9 in.^{2} of copper.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{IN} = +6V, PGND = GND, C_{VL} = 4.7μF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}		3		28	V
Supply Current, No Load	I_{IN}	V_{IN} = 3V to 28V, V_{FB} = 1.6V, $\overline{SHDN}$ = VL		500	700	μA
Supply Current, Full Load, VL Connected to IN	I_{IN}	V_{IN} = 3V to 5.5V, V_{FB} = 1.4V, $\overline{SHDN}$ = VL = IN		5	6.5	mA
Supply Current, Full Load	I_{IN}	V_{IN} = 3.4V to 28V, V_{FB} = 1.4V, $\overline{SHDN}$ = VL, $V_{VL} < V_{IN}$		2.5	3.5	mA
Shutdown Supply Current	I_{IN}	V_{IN} = 28V, V_{FB} = 1.6V, $\overline{SHDN}$ = GND		3	8	μA
VL Output Voltage	V_{VL}	V_{IN} = 3.5V or 28V, no load	2.9	3.05	3.2	V
VL Load Regulation	ΔV_{VL}	I_{LOAD} = 0 to 2mA, V_{FB} = 1.6V		25	40	mV
VL Undervoltage Lockout		Rising edge, 1% hysteresis	2.58	2.7	2.8	V
FB Set Voltage	V_{FB}		1.47	1.5	1.53	V
FB Input Bias Current	I_{FB}	V_{FB} = 1.6V		1	50	nA
Line Regulation	ΔV_{OUT}	V_{IN} = 3V to 6V,V_{OUT} = 12V		0.01	0.08	%/V
Load Regulation	ΔV_{OUT}	V_{OUT} = 12V, I_{LOAD} = 10mA to 500mA		0.2		%
LX Voltage	V_{LX}				28	V
LX Switch Current Limit	I_{LXON}	PWM mode	1.7	2.2	2.7	A
Idle Mode Current Limit Threshold			0.25	0.35	0.45	A
LX On-Resistance	R_{LXON}			0.3	0.6	Ω
LX Leakage Current	I_{LXOFF}	V_{LX} = 28V		0.02	10	μA
COMP Maximum Output Current	I_{COMP}	FB = GND	100	200		μA
COMP Voltage to Switch Current Transconductance		ΔFB = 0.1V	0.8	1		mmho
$\overline{SHDN}$ Input Logic Low	V_{IL}				0.8	V
$\overline{SHDN}$ Input Logic High	V_{IH}		2.0			V
Shutdown Input Current		$\overline{SHDN}$ = GND or VL			1	μA
Switching Frequency	f		200	250	300	kHz
Maximum Duty Cycle	DC		90	95		%

Electrical Characteristics (continued)

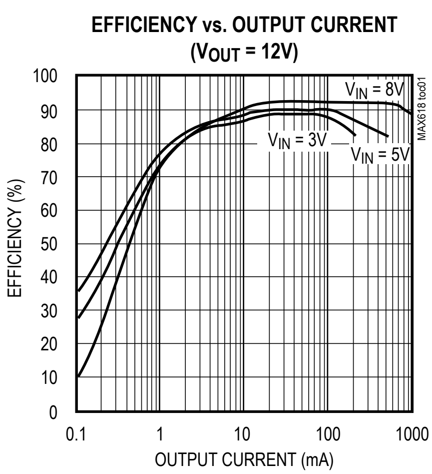
(V_{IN} = +6V, PGND = GND, C_{VL} = 4.7µF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

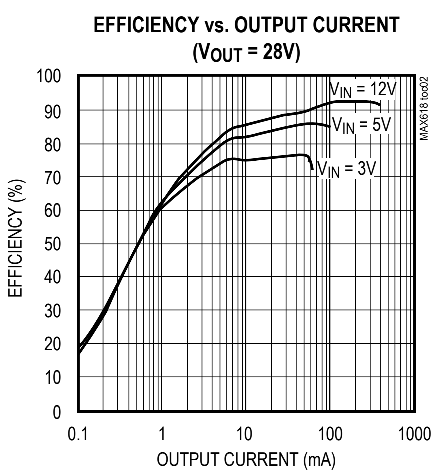
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}		3		28	V
Supply Current, No Load	I_{IN}	V_{IN} = 3V to 28V, V_{FB} = 1.6V, $\overline{SHDN}$ = VL			800	µA
Supply Current, Full Load, VL Connected to IN	I_{IN}	V_{IN} = 3V to 5.5, V_{FB} = 1.4V, $\overline{SHDN}$ = VL = IN			7.5	mA
Supply Current, Full Load	I_{IN}	V_{IN} = 3.4V to 28V, V_{FB} = 1.4V, $\overline{SHDN}$ = VL, $V_{VL} < V_{IN}$			4	mA
Supply Current Shutdown	I_{IN}	V_{IN} = 28V, V_{FB} = 1.6V, $\overline{SHDN}$ = GND			10	µA
VL Output Voltage	V_{VL}	V_{IN} = 3.5V or 28V, no load	2.85		3.3	V
VL Undervoltage Lockout	V_{VL}	Rising edge, 1% hysteresis	2.55		2.85	V
FB Set Voltage	V_{FB}		1.455		1.545	V
LX Voltage Range	V_{LXON}				28	V
LX Switch Current Limit	I_{LXON}	PWM mode	1.4		3	A
LX On-Resistance	R_{LXON}				0.6	Ω
Switching Frequency	f		188		312	kHz

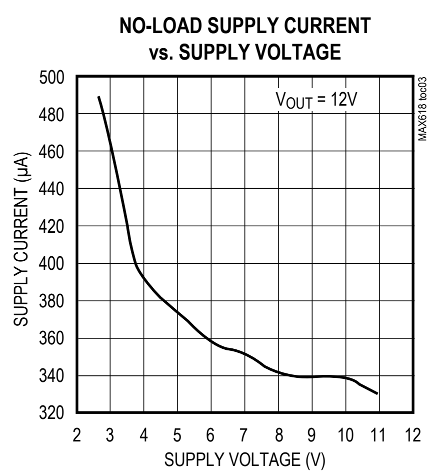
Note 2: Specifications to -40°C are guaranteed by design, not production tested.

Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C.)



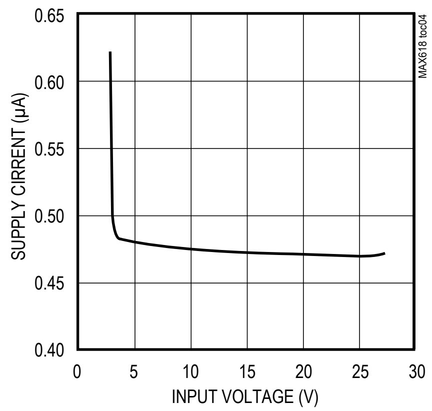




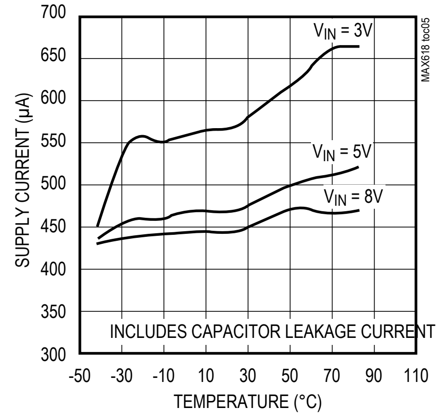
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C.)

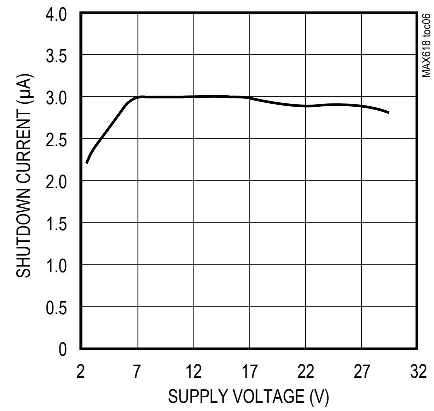
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



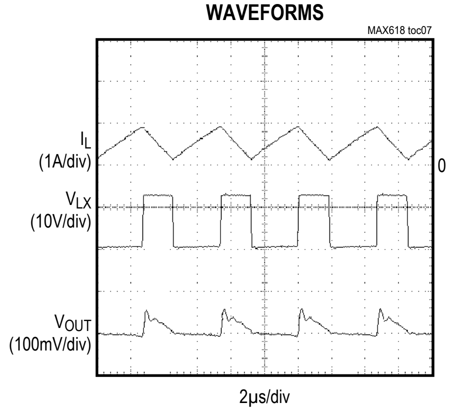
SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN CURRENT vs. SUPPLY VOLTAGE

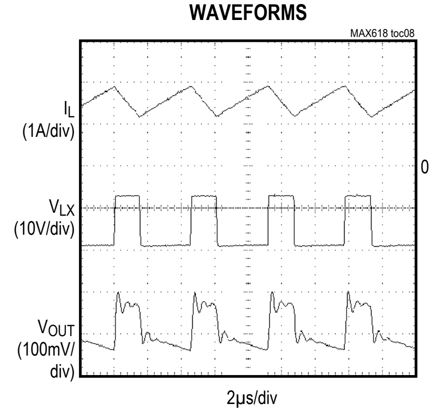


MEDIUM-LOAD SWITCHING WAVEFORMS



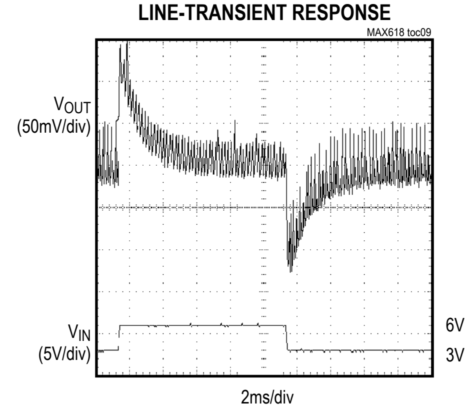
V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 200mA

HEAVY-LOAD SWITCHING WAVEFORMS



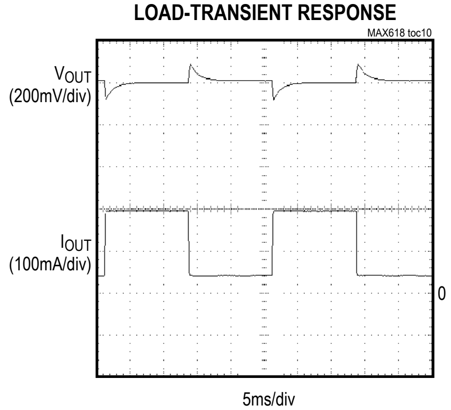
V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 500mA

LINE-TRANSIENT RESPONSE



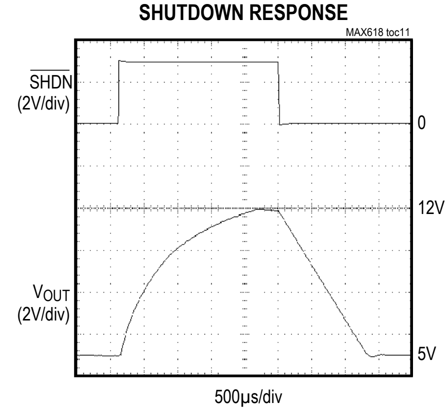
I_{OUT} = 200mA, V_{OUT} = 12V

LOAD-TRANSIENT RESPONSE



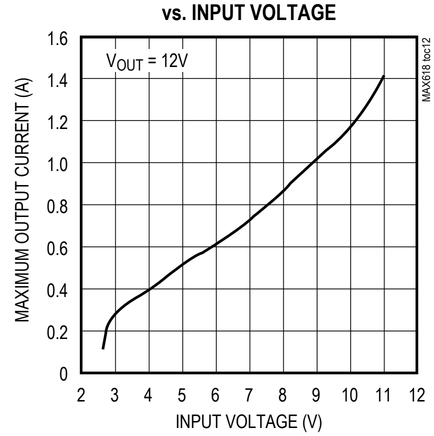
V_{IN} = 5V, V_{OUT} = 12V

SHUTDOWN RESPONSE



V_{IN} = 5V, V_{OUT} = 12V, I_{LOAD} = 500mA

MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1, 8, 9, 12, 16	GND	Ground
2, 3, 4	LX	Drain of Internal n-channel Switch. Connect the inductor between IN and LX.
5	$\overline{SHDN}$	Shutdown Input. A logic low puts the MAX618 in shutdown mode and reduces supply current to 3µA. **$\overline{SHDN}$ must not exceed VL.** In shutdown, the output falls to V_{IN} less one diode drop.
6	COMP	Compensation Input. Bypass to GND with the value of capacitance shown in Table 2.
7	FB	Feedback Input. Connect a resistor-divider network to set V_{OUT}. FB threshold is 1.5V.
10	IN	LDO Regulator Supply Input. IN accepts inputs up to +28V. Bypass to GND with a 1µF ceramic capacitor as close to pins 10 and 12 as possible.
11	VL	Internal 3.1V LDO Regulator Output. Bypass to GND with a 4.7µF capacitor.
13, 14, 15	PGND	Power Ground. Source of internal N-channel switch.

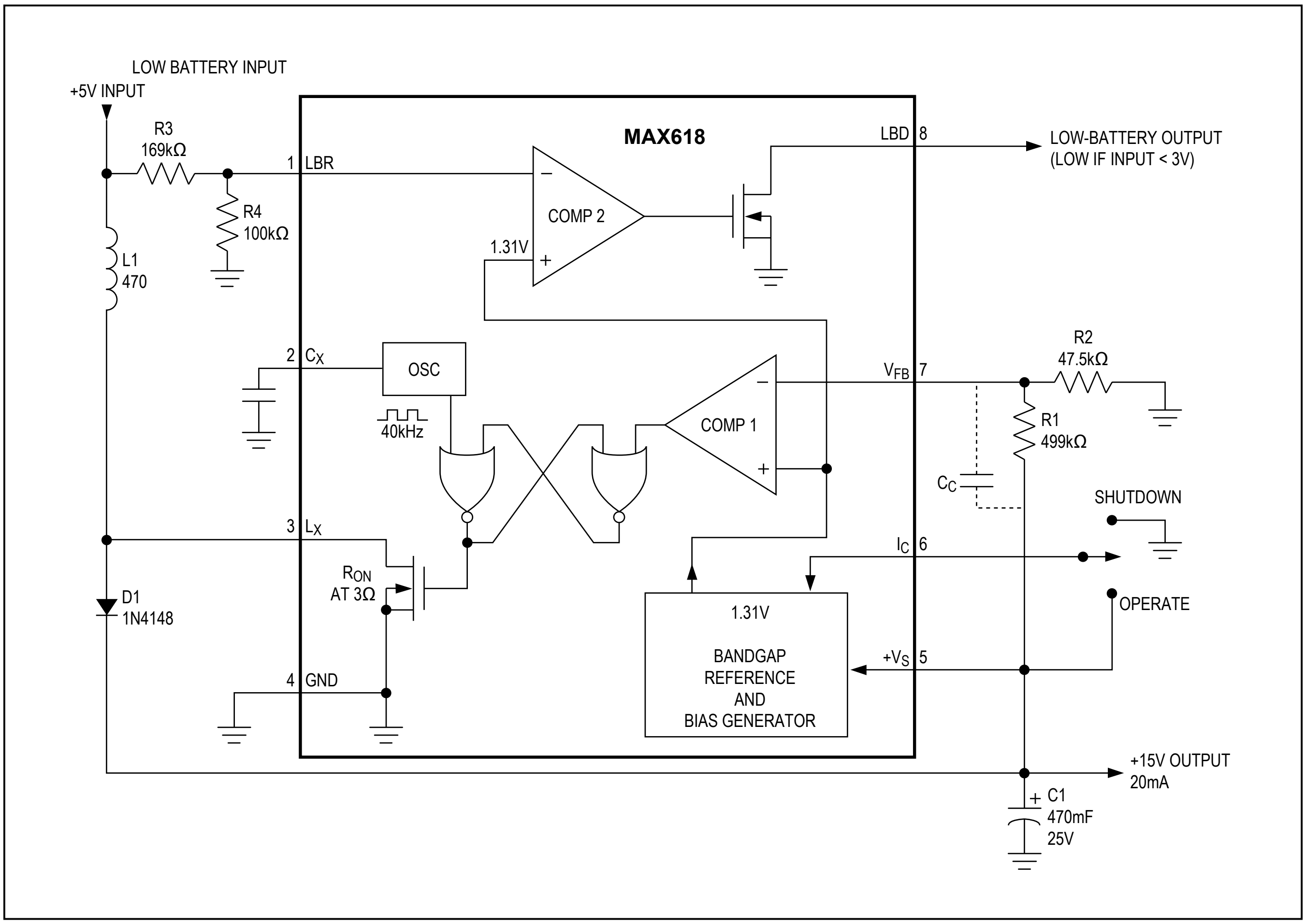


Figure 1. Single-Supply Operation

Detailed Description

The MAX618 pulse-width modulation (PWM) DC-DC converter with an internal 28V switch operates in a wide range of DC-DC conversion applications including boost, SEPIC, and flyback configurations. The MAX618 uses fixed-frequency PWM operation and Maxim's proprietary Idle Mode control to optimize efficiency over a wide range of loads. It also features a shutdown mode to minimize quiescent current when not in operation.

PWM Control Scheme and Idle Mode Operation

The MAX618 combines continuous-conduction PWM operation at medium to high loads and Idle Mode operation at light loads to provide high efficiency over a wide range of load conditions. The MAX618 control scheme actively monitors the output current and automatically switches between PWM and Idle Mode to optimize efficiency and load regulation. Figure 2 shows a functional diagram of the MAX618's control scheme.

The MAX618 normally operates in low-noise, continuous-conduction PWM mode, switching at 250kHz. In PWM mode, the internal MOSFET switch turns on with each clock pulse. It remains on until either the error comparator trips or the inductor current reaches the 2A switch-current limit. The error comparator compares the feedback-error signal, current-sense signal, and slope-compensation signal in one circuit block. When the switch turns off, energy transfers from the inductor to the output capacitor. Output current is limited by the 2A MOSFET current limit

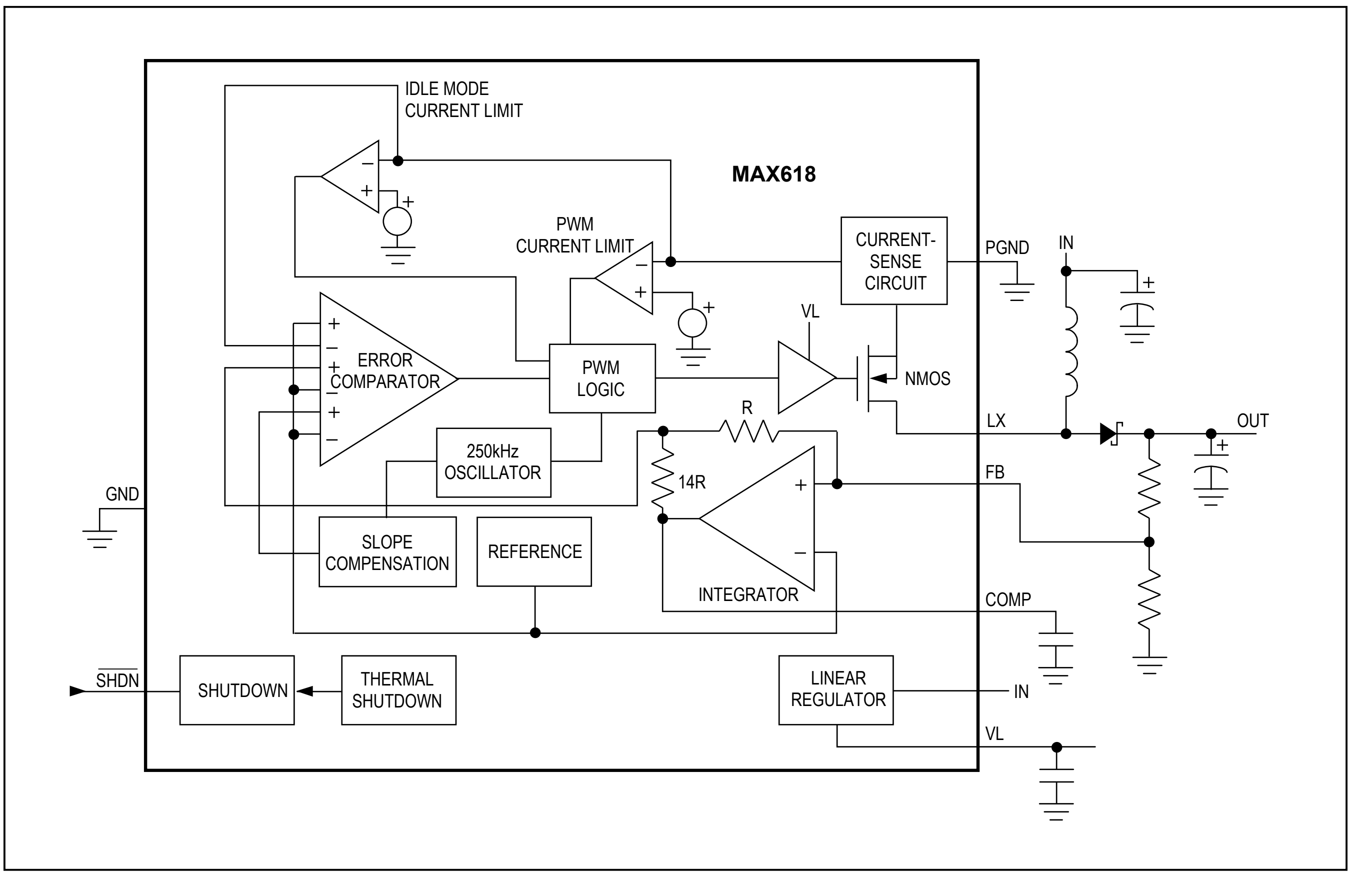


Figure 2. Functional Diagram

and the MAX618's package power-dissipation limit. See the *Maximum Output Current* section for details.

In Idle Mode, the MAX618 improves light-load efficiency by reducing inductor current and skipping cycles to reduce the losses in the internal switch, diode, and inductor. In this mode, a switching cycle initiates only when the error comparator senses that the output voltage is about to drop out of regulation. When this occurs, the NMOS switch turns on and remains on until the inductor current exceeds the nominal 350mA Idle Mode current limit.

Refer to Table 1 for an estimate of load currents at which the MAX618 transitions between PWM and Idle Mode.

Compensation Scheme

Although the higher loop gain of voltage-controlled architectures tends to provide tighter load regulation, current-controlled architectures are generally easier to compensate over wide input and output voltage ranges. The MAX618 uses both control schemes in parallel: the dominant, low-frequency components of the error signal are tightly regulated with a voltage-control loop, while a current-control loop improves stability at higher frequencies. Compensation is achieved through the selection of the output capacitor (C_{OUT}), the integrator capacitor (C_{COMP}), and the pole capacitor (C_P) from FB to GND. C_P cancels the zero formed by C_{OUT} and its ESR. Refer to the *Capacitor Selection* section for guidance on selecting these capacitors.

VL Low-Dropout Regulator

The MAX618 contains a 3.1V low-dropout linear regulator to power internal circuitry. The regulator's input is IN and its output is VL. The IN to VL dropout voltage is 100mV, so that when IN is less than 3.2V, VL is typically 100mV below IN. The MAX618 still operates when the LDO is in dropout, as long as VL remains above the 2.7V undervoltage lockout. Bypass VL with a 4.7μF ceramic capacitor placed as close to the VL and GND pins as possible.

VL can be overdriven by an external supply between 2.7V and 5.5V. In systems with +3.3V or +5V logic power supplies available, improve efficiency by powering VL and V_{IN} directly from the logic supply as shown in Figure 3.

Table 1. PWM/Idle-Mode Transition Load Current (I_{OUT} in Amps) vs. Input and Output Voltage

V_{IN}	V_{OUT}																								
	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
3	0.20	0.20	0.18	0.15	0.12	0.10	0.09	0.08	0.07	0.06	0.05	0.04	0.04	0.04	0.03	0.03	0.03	0.03	0.03	0.02	0.02	0.02	0.02	0.02	0.02
4		0.18	0.21	0.20	0.17	0.15	0.13	0.12	0.10	0.09	0.08	0.07	0.07	0.06	0.05	0.05	0.04	0.04	0.04	0.03	0.03	0.03	0.03	0.03	0.03
5			0.16	0.20	0.21	0.19	0.17	0.16	0.14	0.13	0.11	0.10	0.09	0.09	0.08	0.07	0.07	0.06	0.06	0.05	0.05	0.04	0.04	0.04	0.04
6				0.15	0.20	0.21	0.20	0.19	0.18	0.16	0.15	0.13	0.12	0.11	0.10	0.10	0.09	0.08	0.08	0.07	0.07	0.06	0.06	0.05	0.05
7					0.17	0.19	0.21	0.21	0.20	0.19	0.17	0.16	0.15	0.14	0.13	0.12	0.11	0.10	0.10	0.09	0.08	0.08	0.07	0.07	0.07
8						0.19	0.18	0.20	0.21	0.20	0.20	0.19	0.17	0.16	0.15	0.14	0.13	0.13	0.12	0.11	0.10	0.10	0.09	0.09	0.08
9							0.20	0.17	0.20	0.21	0.21	0.20	0.19	0.18	0.18	0.17	0.16	0.15	0.14	0.13	0.12	0.12	0.11	0.10	0.10
10								0.21	0.16	0.19	0.20	0.21	0.21	0.20	0.19	0.18	0.17	0.17	0.16	0.15	0.14	0.13	0.13	0.12	0.11
11									0.22	0.15	0.19	0.20	0.21	0.21	0.20	0.20	0.19	0.18	0.17	0.17	0.16	0.15	0.14	0.14	0.13
12										0.23	0.15	0.18	0.20	0.21	0.21	0.21	0.20	0.20	0.19	0.18	0.18	0.17	0.16	0.15	0.15
13											0.24	0.16	0.17	0.19	0.20	0.21	0.21	0.20	0.20	0.19	0.19	0.18	0.17	0.17	0.16
14												0.25	0.17	0.17	0.19	0.20	0.21	0.21	0.21	0.20	0.20	0.19	0.19	0.18	0.17
15													0.25	0.18	0.16	0.18	0.20	0.20	0.21	0.21	0.21	0.20	0.20	0.19	0.19
16														0.26	0.19	0.16	0.18	0.19	0.20	0.21	0.21	0.21	0.20	0.20	0.20
17															0.26	0.20	0.15	0.17	0.19	0.20	0.20	0.21	0.21	0.21	0.20
18																0.27	0.20	0.15	0.17	0.19	0.20	0.20	0.21	0.21	0.21
19																	0.27	0.21	0.16	0.17	0.18	0.19	0.20	0.21	0.21
20																		0.27	0.21	0.17	0.16	0.18	0.19	0.20	0.20
21																			0.28	0.22	0.17	0.16	0.18	0.19	0.20
22																				0.28	0.22	0.18	0.15	0.17	0.19
23																					0.28	0.23	0.18	0.15	0.17
24																						0.28	0.23	0.19	0.15
25																							0.29	0.24	0.19
26																								0.29	0.24
27																									0.29

Operating Configurations

The MAX618 can be connected in one of three configurations described in Table 2 and shown in Figures 1, 3, and 4. The VL linear regulator allows operation from a single supply between +3V and +28V as shown in Figure 1.

The circuit in Figure 3 allows a logic supply to power the MAX618 while using a separate source for DC-DC conversion power (inductor voltage). The logic supply (between 2.7V and 5.5V) connects to VL and IN. VL = IN; voltages of 3.3V or more improve efficiency by providing greater gate drive for the internal MOSFET.

The circuit in Figure 4 allows separate supplies to power IN and the inductor voltage. It differs from the connection in Figure 3 in that the MAX618 chip supply is not limited to 5.5V.

Table 2. Input Configurations

CIRCUIT	CONNECTION	V_{IN} RANGE	INDUCTOR VOLTAGE	BENEFITS/COMMENTS
Figure 1	Input voltage connects to IN and inductor.	3V to V_{OUT} (up to 28V)	V_{IN}	• Single supply operation. • $\overline{SHDN}$ must be connected to or pulled up to VL. On/off control requires an open-drain or open-collector connection to $\overline{SHDN}$.
Figure 3	IN and VL connect together. Inductor voltage supplied by a separate source.	2.7V to 5.5V	0V to V_{OUT} (up to 28V)	• Increased efficiency. • $\overline{SHDN}$ can be driven by logic powered from the supply connected to IN and VL, or can be connected to or pulled up to VL. • Input power source (inductor voltage) is separate from the MAX618's bias (V_{IN} = VL) and can be less than or greater than V_{IN}.
Figure 4	IN and inductor voltage supplied by separate sources.	3V to 28V	0V to V_{OUT} (up to 28V)	• Input power source (inductor voltage) is separate from the MAX618's bias (V_{IN}) and can be less than or greater than V_{IN}. • $\overline{SHDN}$ must be connected to or pulled up to VL. On/off control requires an open-drain or open-collector connection to $\overline{SHDN}$.

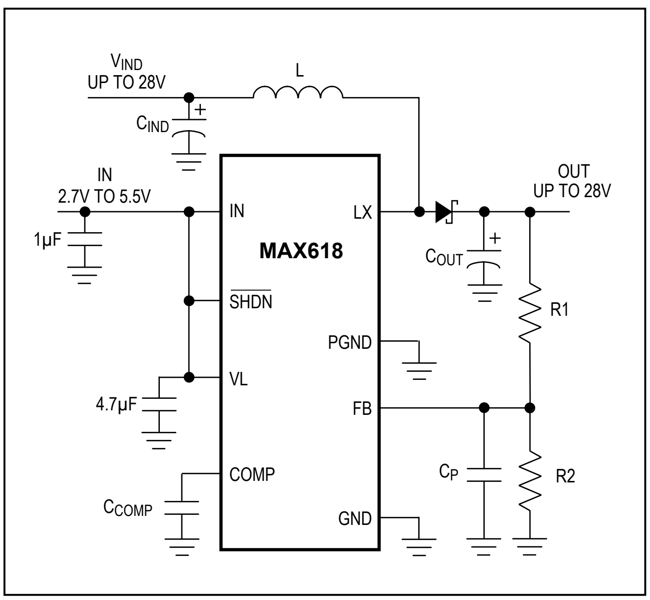


Figure 3. Dual-Supply Operation (V_{IN} = 2.7V to 5.5V)

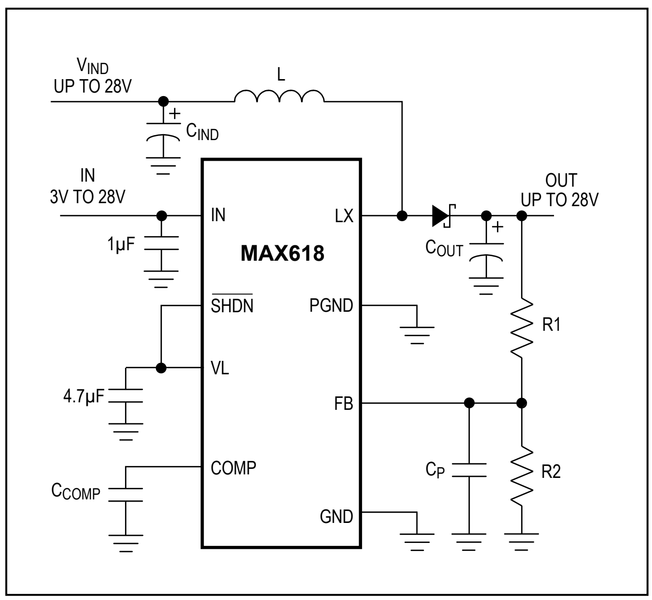


Figure 4. Dual-Supply Operation (V_{IN} = 3V to 28V)

Shutdown Mode

In shutdown mode ($\overline{SHDN}$ = 0), the MAX618's feedback and control circuit, reference, and internal biasing circuitry turn off and reduce the IN supply current to 3µA (10µA max). When in shutdown, a current path remains from the input to the output through the external inductor and diode. Consequently, the output falls to V_{IN} less one diode drop in shutdown.

$\overline{SHDN}$ may not exceed VL. For always-on operation, connect SHDN to VL. To add on/off control to the circuit of Figure 1 or 4, pull $\overline{SHDN}$ to VL with a resistor (10kΩ to 100kΩ) and drive $\overline{SHDN}$ with an open-drain logic gate or switch as shown in Figure 5. Alternatively, the circuit of Figure 3 allows direct $\overline{SHDN}$ drive by any logic-level gate powered from the same supply that powers VL and IN, as shown in Figure 6.

Design Procedure

The MAX618 operates in a number of DC-DC converter configurations including step-up, SEPIC, and flyback. The following design discussion is limited to step-up converters.

Setting the Output Voltage

Two external resistors (R1 and R2) set the output voltage. First, select a value for R2 between 10kΩ and 200kΩ. Calculate R1 with:

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

where V_{FB} is 1.5V.

Determining the Inductor Value

The MAX618's high switching frequency allows the use of a small value inductor. The recommended inductor value is proportional to the output voltage and is given by the following:

$$L = \frac{V_{OUT}}{7 \times 10^5}$$

After solving for the above equation, round down as necessary to select a standard inductor value.

When selecting an inductor, choose one rated to 250kHz, with a saturation current exceeding the peak inductor current, and with a DC resistance under 200mΩ. Ferrite core or equivalent inductors are generally appropriate (see MAX618 EV kit data sheet). Calculate the peak inductor current with the following equation:

$$I_{LX(PEAK)} = I_{OUT}\frac{V_{OUT}}{V_{IN}} + 2\mu s\left(\frac{V_{IN}}{L}\right)\left(\frac{(V_{OUT} - V_{IN})}{V_{OUT}}\right)$$

Note that the peak inductor current is internally limited to 2A.

Diode Selection

The MAX618's high switching frequency demands a high-speed rectifier. Schottky diodes are preferred for most applications because of their fast recovery time and low forward voltage. Make sure that the diode's peak current rating exceeds the 2A peak switch current, and that its breakdown voltage exceeds the output voltage.

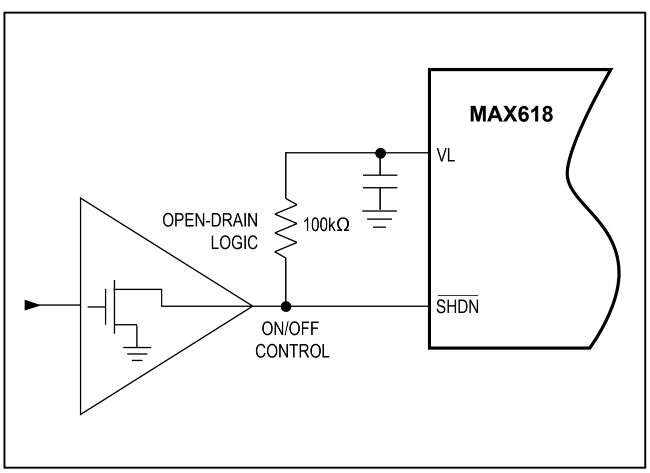


Figure 5. Adding On/Off Control to Circuit of Figure 1 or 4

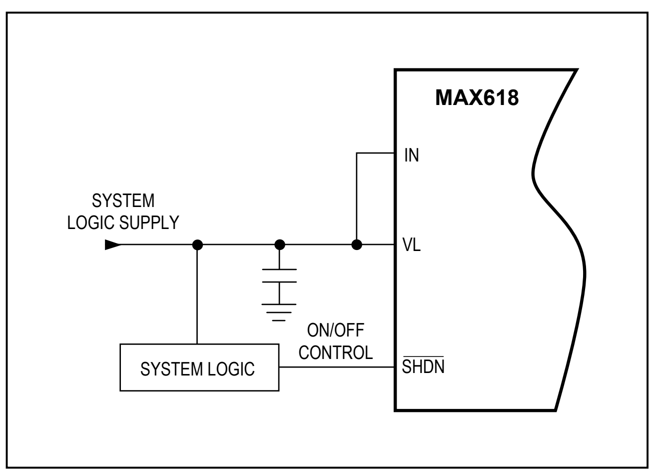


Figure 6. Adding On/Off Control to Circuit of Figure 3

Maximum Output Current

The MAX618's 2.2A LX current limit determines the output power that can be supplied for most applications. In some cases, particularly when the input voltage is low, output power is sometimes restricted by package dissipation limits. The MAX618 is protected by a thermal shutdown circuit that turns off the switch when the die temperature exceeds +150°C. When the device cools by 10°C, the switch is enabled again. Table 3 details output current with a variety of input and output voltages. Each listing in Table 3 is either the limit set by an LX current limit or by package dissipation at +85°C ambient, whichever is lower. The values in Table 3 assume a 40mΩ inductor resistance.

Capacitor Selection

Input Capacitors

The input bypass capacitor (C_{IND}) reduces the input ripple created by the boost configuration. High-impedance sources require high C_{IND} values. However, 68μF is generally adequate for input currents up to 2A. Low-ESR capacitors are recommended because they will decrease the ripple created on the input and improve efficiency. Capacitors with ESR below 0.3Ω are generally appropriate.

In addition to the input bypass capacitor, bypass IN with a 1μF ceramic capacitor placed as close to the IN and GND pins as possible. Bypass VL with a 4.7μF ceramic capacitor placed as close to the VL and GND pins as possible.

Output Capacitor

Use Table 4 to find the minimum output capacitance necessary to ensure stable operation. In addition, choose an output capacitor with low ESR to reduce the output ripple. The dominant component of output ripple is the product of the peak-to-peak inductor ripple current and the ESR of the output capacitor. ESR below 50mΩ generates acceptable levels of output ripple for most applications.

Integrator Capacitor

The compensation capacitor (C_{COMP}) sets the dominant pole in the MAX618's transfer function. The proper compensation capacitance depends upon output capacitance. Table 5 shows the capacitance value needed for the output capacitances specified in Table 4. However, if a different output capacitor is used (e.g., a standard value), then recalculate the value of capacitance needed for the integrator capacitor with the following formula:

$$C_{COMP} = \frac{C_{COMP}(\text{Table 5}) \times C_{OUT}}{C_{OUT}(\text{Table 4})}$$

Pole Compensation Capacitor

The pole capacitor (C_P) cancels the unwanted zero introduced by C_{OUT}'s ESR, and thereby ensures stability in PWM operation. The exact value of the pole capacitor is not critical, but it should be near the value calculated by the following equation:

$$C_P = \frac{R_{ESR} \times C_{OUT}(R_1 + R_2)}{R_1 \times R_2}$$

where R_{ESR} is C_{OUT}'s ESR.

Layout Considerations

Proper PC board layout is essential due to high current levels and fast switching waveforms that radiate noise. Use the MAX618 evaluation kit or equivalent PC layout to perform initial prototyping. Breadboards, wire-wrap, and proto-boards are not recommended when prototyping switching regulators.

It is important to connect the GND pin, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a single point to minimize ground noise and improve regulation. Also, minimize lead lengths to reduce stray capacitance, trace resistance, and radiated noise, with preference given to the feedback circuit, the ground circuit, and LX. Place the feedback resistors as close to the FB pin as possible. Place a 1μF input bypass capacitor as close as possible to IN and GND.

Refer to the MAX618 evaluation kit for an example of proper board layout.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 QSOP	EF16+8F	21-0055

Table 3. Typical Output Current vs. Input and Output Voltages

V_{IN}	V_{OUT}																								
	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
3	0.77	0.59	0.49	0.41	0.34	0.29	0.25	0.22	0.20	0.18	0.17	0.15	0.14	0.13	0.12	0.12	0.11	0.10	0.10	0.09	0.09	0.08	0.08	0.08	0.07
4		0.96	0.76	0.64	0.56	0.49	0.43	0.38	0.34	0.31	0.28	0.26	0.24	0.22	0.21	0.19	0.18	0.17	0.16	0.16	0.15	0.14	0.14	0.13	0.12
5			1.09	0.89	0.76	0.67	0.60	0.54	0.50	0.45	0.41	0.37	0.34	0.32	0.30	0.28	0.26	0.25	0.23	0.22	0.21	0.20	0.19	0.18	0.18
6				1.18	0.99	0.85	0.76	0.68	0.63	0.58	0.54	0.50	0.46	0.42	0.39	0.37	0.34	0.32	0.31	0.29	0.28	0.26	0.25	0.24	0.23
7					1.26	1.07	0.93	0.83	0.76	0.70	0.65	0.60	0.57	0.53	0.50	0.46	0.43	0.41	0.38	0.36	0.35	0.33	0.31	0.30	0.29
8						1.32	1.13	1.00	0.90	0.82	0.76	0.71	0.66	0.62	0.59	0.56	0.53	0.50	0.47	0.44	0.42	0.40	0.38	0.36	0.35
9							1.37	1.19	1.06	0.96	0.88	0.81	0.76	0.71	0.67	0.64	0.61	0.58	0.55	0.53	0.50	0.47	0.45	0.43	0.41
10								1.41	1.24	1.11	1.01	0.93	0.86	0.81	0.76	0.72	0.68	0.65	0.62	0.59	0.57	0.55	0.52	0.50	0.47
11									1.44	1.28	1.15	1.05	0.97	0.91	0.85	0.80	0.76	0.72	0.69	0.66	0.63	0.61	0.58	0.56	0.54
12										1.47	1.31	1.19	1.10	1.02	0.95	0.89	0.84	0.80	0.76	0.73	0.70	0.67	0.64	0.62	0.60
13											1.49	1.34	1.23	1.13	1.05	0.99	0.93	0.88	0.83	0.80	0.76	0.73	0.70	0.67	0.65
14												1.52	1.37	1.26	1.16	1.09	1.02	0.96	0.91	0.87	0.83	0.79	0.76	0.73	0.71
15													1.53	1.40	1.29	1.19	1.12	1.05	0.99	0.94	0.90	0.86	0.82	0.79	0.76
16														1.55	1.42	1.31	1.22	1.14	1.08	1.02	0.97	0.93	0.89	0.85	0.82
17															1.57	1.44	1.33	1.25	1.17	1.11	1.05	1.00	0.95	0.91	0.88
18																1.58	1.46	1.36	1.27	1.20	1.13	1.07	1.02	0.98	0.94
19																	1.59	1.47	1.37	1.29	1.22	1.15	1.10	1.05	1.00
20																		1.60	1.49	1.39	1.31	1.24	1.18	1.12	1.07
21																			1.61	1.50	1.41	1.33	1.26	1.20	1.14
22																				1.62	1.51	1.42	1.35	1.28	1.22
23																					1.63	1.53	1.44	1.36	1.29
24																						1.64	1.54	1.45	1.38
25																							1.64	1.55	1.46
26																								1.65	1.56
27																									1.66

Table 4. Minimum C_{OUT} for Stability (µF)

V_{IN}	V_{OUT} 4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
3	173	128	100	80	65	54	46	40	35	31	28	25	23	21	19	18	17	15	15	14	13	12	12	11	10
4		151	118	96	80	68	59	51	45	39	35	32	29	27	24	23	21	20	18	17	16	15	15	14	13
5			132	107	90	77	67	59	52	46	41	37	34	31	29	26	25	23	21	20	19	18	17	16	15
6				117	97	83	72	64	57	51	46	42	38	35	32	30	28	26	24	23	21	20	19	18	17
7					104	89	77	68	61	55	50	45	42	39	35	33	30	28	26	25	23	22	21	20	19
8						94	82	72	64	58	52	48	44	41	38	35	33	31	29	27	25	24	22	21	20
9							86	76	67	61	55	50	46	42	39	37	34	32	30	29	27	25	24	23	21
10								79	70	63	57	52	48	44	41	38	36	34	32	30	28	27	25	24	23
11									73	66	59	54	50	46	43	40	37	35	33	31	29	28	26	25	24
12										68	62	56	51	47	44	41	38	36	34	32	30	29	27	26	25
13											64	58	53	49	45	42	39	37	35	33	31	29	28	27	25
14												60	55	50	47	43	40	38	36	34	32	30	29	27	26
15													56	52	48	44	42	39	37	35	33	31	29	28	27
16														53	49	46	43	40	37	35	33	32	30	29	27
17															50	47	44	41	38	36	34	32	31	29	28
18																48	45	42	39	37	35	33	31	30	28
19																	46	43	40	38	36	34	32	30	29
20																		43	41	38	36	34	33	31	29
21																			42	39	37	35	33	32	30
22																				40	38	36	34	32	31
23																					38	36	34	33	31
24																						37	35	33	32
25																							35	34	32
26																								34	33
27																									33

Table 5. Minimum C_{COMP} for Stability (nF)

V_{IN}	V_{OUT}																								
	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
3	40	46	54	64	73	83	94	105	118	130	143	157	172	187	203	219	236	253	271	290	309	329	349	370	391
4		42	45	51	58	66	74	82	91	100	109	119	130	141	152	164	176	188	201	214	228	242	257	272	287
5			43	45	49	54	60	67	75	81	88	96	103	111	120	128	137	147	156	166	176	187	197	209	220
6				44	45	48	52	57	62	68	74	80	86	92	99	105	112	119	127	134	142	150	159	167	176
7					45	45	47	50	54	58	63	68	74	79	85	90	95	101	107	113	119	125	132	139	146
8						46	45	47	49	52	56	60	64	68	73	78	83	88	93	98	103	108	113	119	124
9							46	46	47	48	51	54	57	61	64	68	73	77	82	86	91	95	99	104	109
10								47	46	46	48	50	52	55	58	61	65	69	72	77	81	85	89	93	97
11									47	46	46	48	49	51	54	56	59	62	65	69	72	76	80	84	88
12										48	47	47	47	49	50	52	55	57	60	63	66	69	72	75	79
13											48	47	47	47	48	50	52	54	56	58	61	63	66	69	72
14												49	47	47	47	48	49	51	53	55	57	59	61	64	66
15													49	47	47	47	48	49	50	52	53	55	57	59	62
16														49	48	47	47	48	49	50	51	53	54	56	58
17															49	48	47	47	48	48	49	51	52	53	55
18																50	48	47	47	48	48	49	50	51	53
19																	50	48	47	47	48	48	49	50	51
20																		50	48	48	47	48	48	49	49
21																			50	49	48	47	48	48	48
22																				50	49	48	48	48	48
23																					50	49	48	48	48
24																						51	49	48	48
25																							51	49	48
26																								51	49
27																									51

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/09	Initial release	—
1	12/09	Updated part to lead-free, added soldering temperatures (reflow), and corrected error in equation	1, 2, 10
2	4/15	No /V ordering information; removed Automotive reference from *Applications* section	1

