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## MAX5855

# 16-Bit, 4.9Gbps Wideband Interpolating and Modulating RF DAC with JESD204B Interface

## General Description

The MAX5855 high-performance, interpolating and modulating, 16-bit, 4.9Gbps RF DAC can directly synthesize up to 1000MHz of instantaneous bandwidth from DC to frequencies greater than 2.45GHz. The device is optimized for cable access and digital video broadcast applications and meets spectral emission requirements for a broad set of radio transmitters and modulators including DOCSIS 3.1/3.0, DVB-C/C2, DVB-T2, DVB-S2X, ISDB-T, and EPoC.

The device integrates interpolation filters, a digital quadrature modulator, a numerically controlled oscillator (NCO), clock multiplying PLL + VCO and a 14-bit RF DAC core. The 4x linear phase interpolation filter simplifies reconstruction filtering, while enhancing passband dynamic performance, and reducing the input data bandwidth required from an FPGA. The NCO allows for fully agile modulation of the input baseband signal for direct RF synthesis.

The MAX5855 input interface accepts 16-bit input data by way of a five-lane, JESD204B SerDes data input interface that is Subclass-0 compliant and operates at a data rate of 9.8304Gbps.

The MAX5855 clock input has a flexible interface that accepts a differential sine-wave or square-wave reference input clock signal at 245.75MHz, 491.52MHz, or 983.04MHz. A clock multiplying PLL and VCO is used to internally generate the 4.9152GHz sampling clock from the reference clock. The device provides a divided reference clock output to ensure synchronization between the data source and the DAC.

The integrated RF DAC uses a differential current-steering architecture that includes a differential 50Ω internal termination and can produce a 3dBm full-scale output signal level on a 50Ω external load. Operating from 1.0V and 1.8V power supplies, the device consumes 2.7W at 4.9Gbps. The device is offered in a compact 144-pin, 10mm x 10mm, FCCSP package and is specified for the extended industrial temperature range (-40°C to +85°C).

## Applications

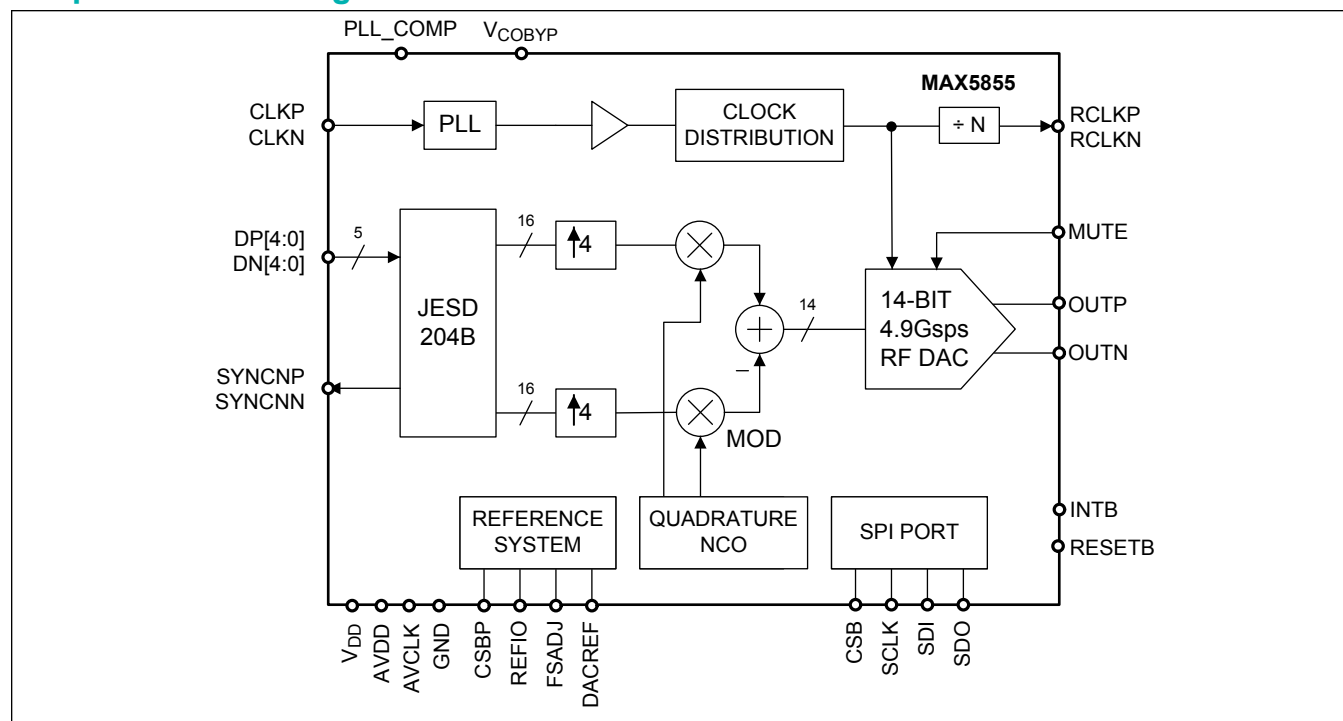
- DOCSIS 3.1/3.0 Remote PHY and CCAP
- Digital Video Broadcast Modulators
  - DVB-C/C2/DVB-T2/DVB-S2X/ISDB-T
- Ethernet PON Over Coax (EPoC)
- Point-to-Point Wireless
- Instrumentation

## Benefits and Features

- Simplifies RF Design and Enables New Communication Architectures
  - Eliminates I/Q Imbalance and LO Feedthrough
  - Enables Multi-Band RF Modulation
- Direct RF Synthesis of 1GHz Bandwidth
  - 4.9152Gbps DAC Output Update Rate
  - High-Performance 14-Bit RF DAC Core
  - Digital Baseband I/Q with 4x Interpolation
  - Digital Quadrature Modulator + NCO for Full Agility
  - Sub-1Hz NCO Resolution
  - Integrated Clock Multiplying PLL + VCO
- Flexible and Configurable
  - 5-Lane JESD204B Input Data Interface
    - Subclass-0 Compliant
    - 9.8304Gbps Per Lane
  - Divided Reference Clock Output
  - SPI Interface for Device Configuration

Ordering Information appears at end of data sheet.

## Simplified Block Diagram



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## Absolute Maximum Ratings

VDD2, AVCLK2, AVDD2, AVDD2PLL, VDD2PLL: -0.3V to +2.1V  
 OUTP, OUTN: -0.3V to (V<sub>AVDD2</sub> + 0.5)V  
 MUTE, RESETB, CSB, SCLK, SDO, SDI, INTB, TDA: -0.3V to (V<sub>VDD2</sub> + 0.3, MAX 2.1)V  
 TESTP, TESTN, SYNCNP, SYNCNN, RCLKP, RCLKN: -0.3V to (V<sub>VDD2</sub> + 0.3, MAX 2.1)V  
 DP0, DN0, DP1, DN1, DP2, DN2, DP3, DN3, DP4, DN4: -0.3V to (V<sub>VDD2</sub> + 0.3, MAX 1.6)V  
 JRES, CAPT, TESTEN: (V<sub>VSSPLL</sub> - 0.3)V to (V<sub>VDD2PLL</sub> + 0.3, MAX 2.1)V  
 VCOBYP: -0.3V to (V<sub>AVCLK2</sub> + 0.3, MAX 2.1)V  
 PLLCOMP: -0.3V to (V<sub>AVDD2PLL</sub> + 0.3, MAX 2.1)V

VSSPLL, TDC, DACREF: (V<sub>GND</sub> - 0.3)V to (V<sub>GND</sub> + 0.3)V  
 VDD, AVDD, AVCLK, AVDDPLL: -0.3V to +1.2V  
 REFIO, FSADJ, CSBP: -0.3V to (V<sub>AVDD2</sub> + 0.3, MAX 2.1)V  
 CLKP, CLKN: -0.3V to (V<sub>AVDDPLL</sub> + 0.3, MAX 1.2)V  
 SDO, INTB Maximum Continuous Current: 8mA  
 Continuous Power Dissipation (T<sub>A</sub> = +85°C): 4.0W  
**Thermal Characteristics**  
 Operating Temperature Range (T<sub>A</sub>): -40°C to +85°C  
 Operating Junction Temperature (T<sub>J</sub>): +110°C  
 Maximum Junction Temperature: +150°C  
 Storage Temperature Range: -60°C to +150°C  
 Soldering Temperature (reflow): +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Information

### 144 FCCSP

|                                                        |                         |
|--------------------------------------------------------|-------------------------|
| Package Code                                           | X14400F+1               |
| Outline Number                                         | <a href="#">21-0732</a> |
| Land Pattern Number                                    | <a href="#">90-0289</a> |
| <b>Thermal Resistance, Four-Layer Board:</b>           |                         |
| Junction-to-Ambient (θ <sub>JA</sub> )                 | 16.2°C/W                |
| Junction-to-Case Thermal Resistance (θ <sub>JC</sub> ) | 2.5°C/W                 |

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

( $V_{DD} = V_{AVCLK} = V_{AVDD} = V_{AVDDPLL} = 1.0V$ ,  $V_{DD2} = V_{AVCLK2} = V_{AVDD2} = V_{AVDD2PLL} = V_{DD2PLL} = 1.8V$ ,  $P_{CLK} = 0dBm$ ,  $f_{CLK} = 983.04MHz$ ,  $f_{DAC} = 4915.2Mps$ , 4x interpolation, 5-lanes, 9830.4Mbps per lane, external reference at 1.206V,  $R_{SET} = 965\Omega$  between FSADJ and DACREF,  $I_{OUTFS} = 40mA$ , output is  $50\Omega$  double-terminated and transformer coupled (see [Figure 25](#)), PLL on.  $T_A \geq -40^\circ C$  and  $T_J \leq +110^\circ C$ , unless otherwise noted. Typical values are at  $T_J = +65 \pm 15^\circ C$ . (Note 1))

| PARAMETER                                                                | SYMBOL      | CONDITIONS                                                                     | MIN                         | TYP               | MAX | UNITS    |
|--------------------------------------------------------------------------|-------------|--------------------------------------------------------------------------------|-----------------------------|-------------------|-----|----------|
| <b>STATIC PERFORMANCE</b>                                                |             |                                                                                |                             |                   |     |          |
| Input Data Word Width                                                    | N           |                                                                                |                             | 16                |     | Bits     |
| DAC Resolution                                                           |             |                                                                                |                             | 14                |     | Bits     |
| Differential Non-Linearity                                               | DNL         | <a href="#">Figure 26</a>                                                      |                             | $\pm 1.5$         |     | LSB      |
| Integral Non-Linearity                                                   | INL         | <a href="#">Figure 26</a>                                                      |                             | $\pm 3$           |     | LSB      |
| Offset Voltage Error                                                     | OS          |                                                                                |                             | 0.003             |     | %FS      |
| Minimum Full-Scale Output Current                                        | $I_{OUTFS}$ |                                                                                |                             | 10                |     | mA       |
| Maximum Full-Scale Output Current                                        | $I_{OUTFS}$ |                                                                                |                             | 40                |     | mA       |
| Output-Voltage Gain Error                                                | $GE_{FS}$   | $f_{OUT} = DC$ , <a href="#">Figure 26</a>                                     |                             | $\pm 3$           |     | %FS      |
| Maximum Output Compliance                                                |             |                                                                                |                             | $V_{AVDD2} + 0.4$ |     | V        |
| Minimum Output Compliance                                                |             |                                                                                |                             | $V_{AVDD2} - 0.4$ |     | V        |
| Output Resistance                                                        | $R_{OUT}$   | Differential DAC output resistance                                             |                             | 50                |     | $\Omega$ |
| <b>DYNAMIC PERFORMANCE</b>                                               |             |                                                                                |                             |                   |     |          |
| DAC Sample Rate                                                          | $f_{DAC}$   |                                                                                |                             | 4915.2            |     | Mps      |
| Adjusted DAC Update Rate                                                 | $AUR_{DAC}$ | (Note 2)                                                                       |                             | 1228.8            |     | Mps      |
| Maximum Input Sample Rate                                                | $f_{S\_IN}$ | For the complex I/Q dataset                                                    |                             | 1228.8            |     | MHz      |
| SFDR to Nyquist                                                          | SFDR        | CW tone, -1dBFS                                                                | $f_{OUT} = 500MHz$          | 73                |     | dB       |
|                                                                          |             |                                                                                | $f_{OUT} = 1000MHz$         | 74                |     |          |
|                                                                          |             |                                                                                | $f_{OUT} = 1500MHz$         | 69                |     |          |
| Maximum HD2, HD3, $f_{DAC}/2$ - $f_{OUT}$ , Measured in 1st Nyquist Zone |             | CW tone, -3dBFS                                                                | $f_{OUT} = 1842.5MHz$       | -71               |     | dBc      |
| Intermodulation Distortion                                               | IMD         | Two-tone signal, $f_{DAC} = 4.9152GHz$ , $f_1 = 1842MHz$ and $f_2 = 1843MHz$   | Average total power -15dBFS | -74               |     | dBc      |
|                                                                          |             | Two-tone signal, $f_{DAC} = 4.9152GHz$ , $f_1 = 1842MHz$ , and $f_2 = 1843MHz$ | Average total power -33dBFS | -80               |     | dBFS     |

**Electrical Characteristics (continued)**

( $V_{DD} = V_{AVCLK} = V_{AVDD} = V_{AVDDPLL} = 1.0V$ ,  $V_{DD2} = V_{AVCLK2} = V_{AVDD2} = V_{AVDD2PLL} = V_{DD2PLL} = 1.8V$ ,  $P_{CLK} = 0dBm$ ,  $f_{CLK} = 983.04MHz$ ,  $f_{DAC} = 4915.2Msps$ , 4x interpolation, 5-lanes, 9830.4Mbps per lane, external reference at 1.206V,  $R_{SET} = 965\Omega$  between FSADJ and DACREF,  $I_{OUTFS} = 40mA$ , output is  $50\Omega$  double-terminated and transformer coupled (see [Figure 25](#)), PLL on.  $T_A \geq -40^\circ C$  and  $T_J \leq +110^\circ C$ , unless otherwise noted. Typical values are at  $T_J = +65 \pm 15^\circ C$ . (Note 1))

| PARAMETER                                                                 | SYMBOL           | CONDITIONS                                                                                |                                             | MIN | TYP    | MAX   | UNITS  |
|---------------------------------------------------------------------------|------------------|-------------------------------------------------------------------------------------------|---------------------------------------------|-----|--------|-------|--------|
| Out-of-Band Noise and Spurious, Eight 6MHz 256-QAM Carriers (Note 5)      | ACPR             | f <sub>OUT</sub> = 575MHz<br>(Note 3, Note 4)                                             | Adjacent channel                            |     | -69.8  | -62.9 | dBc    |
|                                                                           |                  |                                                                                           | Next-adjacent channel                       |     | -70.5  | -63.1 |        |
|                                                                           |                  |                                                                                           | Third-adjacent channel                      |     | -70.9  | -64.0 |        |
|                                                                           |                  | f <sub>OUT</sub> = 575MHz<br>(Note 3)                                                     | Noise in any other channel                  |     | -65.4  |       |        |
|                                                                           |                  | f <sub>OUT</sub> = 975MHz,<br>Average Total Power =<br>-12dBFS (Note 6)                   | Adjacent channel                            |     | -67.4  |       |        |
|                                                                           |                  |                                                                                           | Next-adjacent channel                       |     | -67.9  |       |        |
|                                                                           |                  |                                                                                           | Third-adjacent channel                      |     | -68.5  |       |        |
|                                                                           |                  |                                                                                           | Noise in any other channel                  |     | -63.8  |       |        |
| Out-of-Band Noise and Spurious, Thirty Two 6MHz 256-QAM Carriers (Note 5) | ACPR             | f <sub>OUT</sub> = 1100MHz,<br>Average Total Power =<br>-15dBFS (Note 6)                  | Adjacent channel                            |     | -64.4  |       | dBc    |
|                                                                           |                  |                                                                                           | Next-adjacent channel                       |     | -64.1  |       |        |
|                                                                           |                  |                                                                                           | Third-adjacent channel                      |     | -64.1  |       |        |
|                                                                           |                  |                                                                                           | Noise in any other channel                  |     | -57.3  |       |        |
| Harmonic Distortion, Four 6MHz 256-QAM Carriers                           | HD               | f <sub>OUT</sub> = 575MHz,<br>Average Total Power = -12dBFS<br>(Note 4, Note 6)           | Second Harmonic Distortion                  |     | -66.8  | -55.4 | dBc    |
|                                                                           |                  |                                                                                           | Third Harmonic Distortion                   |     | -67.7  | -60.4 |        |
| Noise Density                                                             | ND               | CW tone at 1842.5MHz, -15dBFS, Measured at 10MHz offset from carrier, in 200kHz bandwidth |                                             |     | -157.5 |       | dBm/Hz |
| DAC RESPONSE CHARACTERISTIC                                               |                  |                                                                                           |                                             |     |        |       |        |
| Output Power (CW)<br>(Note 7)                                             | P <sub>OUT</sub> | 0dBFS CW tone at DAC input, f <sub>OUT</sub> = 100MHz                                     | Excludes losses                             |     | 3.2    |       | dBm    |
|                                                                           |                  |                                                                                           | Excludes losses, includes sin(x)/x roll-off |     | 3.2    |       |        |
|                                                                           |                  | 0dBFS CW tone at DAC input, f <sub>DAC</sub> = 4915.2Msps, f <sub>OUT</sub> = 2140MHz     | Excludes losses                             |     | 0.4    |       |        |
|                                                                           |                  |                                                                                           | Excludes losses, includes sin(x)/x roll-off |     | -2.5   |       |        |
| Output Bandwidth                                                          |                  | f <sub>DAC</sub> = 4915.2Msps, -1dB bandwidth, excludes losses (Note 7)                   |                                             |     | 2600   |       | MHz    |

**Electrical Characteristics (continued)**

( $V_{DD} = V_{AVCLK} = V_{AVDD} = V_{AVDDPLL} = 1.0V$ ,  $V_{DD2} = V_{AVCLK2} = V_{AVDD2} = V_{AVDD2PLL} = V_{DD2PLL} = 1.8V$ ,  $P_{CLK} = 0dBm$ ,  $f_{CLK} = 983.04MHz$ ,  $f_{DAC} = 4915.2Mps$ , 4x interpolation, 5-lanes, 9830.4Mbps per lane, external reference at 1.206V,  $R_{SET} = 965\Omega$  between FSADJ and DACREF,  $I_{OUTFS} = 40mA$ , output is 50 $\Omega$  double-terminated and transformer coupled (see Figure 25), PLL on.  $T_A \geq -40^\circ C$  and  $T_J \leq +110^\circ C$ , unless otherwise noted. Typical values are at  $T_J = +65 \pm 15^\circ C$ . (Note 1))

| PARAMETER                                                                  | SYMBOL      | CONDITIONS                                                                  | MIN                  | TYP                      | MAX                  | UNITS            |
|----------------------------------------------------------------------------|-------------|-----------------------------------------------------------------------------|----------------------|--------------------------|----------------------|------------------|
| Output Settling Time for Full-Scale Input Step (Note 8)                    |             | To $\pm 0.024\%$ of output full-scale in 4x interpolation mode              |                      | 20                       |                      | ns               |
| <b>INTERPOLATION FILTERS</b>                                               |             |                                                                             |                      |                          |                      |                  |
| Interpolation Rates                                                        | R           | Complex path                                                                |                      | 4x                       |                      |                  |
| Passband Width                                                             | PBW         | Ripple < 0.01dB                                                             |                      | $0.407 \times f_{S\_IN}$ |                      | MHz              |
| Stopband Rejection                                                         |             | 4x interpolation, $0.593 \times f_{S\_IN}$                                  |                      | 80                       |                      | dB               |
| Data Latency (Excluding JESD204B Latency)                                  |             | 4x interpolation                                                            |                      | 424                      |                      | DAC Clock Cycles |
| <b>NCO</b>                                                                 |             |                                                                             |                      |                          |                      |                  |
| Maximum Frequency                                                          |             |                                                                             |                      | 2457.6                   |                      | MHz              |
| Frequency Control Word Resolution                                          |             |                                                                             |                      | 33                       |                      | Bits             |
| <b>REFERENCE (REFIO)</b>                                                   |             |                                                                             |                      |                          |                      |                  |
| Reference Input Range                                                      |             |                                                                             | 1.1                  |                          | 1.3                  | V                |
| Reference Output Voltage                                                   | $V_{REFIO}$ | Internal Reference                                                          | 1.1                  | 1.2                      | 1.3                  | V                |
| Reference Input Resistance                                                 | $R_{REFIO}$ |                                                                             |                      | 10                       |                      | k $\Omega$       |
| Reference Voltage Drift                                                    |             |                                                                             |                      | $\pm 110$                |                      | ppm/ $^\circ C$  |
| <b>CMOS LOGIC INPUTS/OUTPUTS (SCLK, CSB, MUTE, RESETB, SDI, SDO, INTB)</b> |             |                                                                             |                      |                          |                      |                  |
| Input High Voltage                                                         | $V_{IH}$    |                                                                             | $0.7 \times V_{DD2}$ |                          |                      | V                |
| Input Low Voltage                                                          | $V_{IL}$    |                                                                             |                      |                          | $0.3 \times V_{DD2}$ | V                |
| Input Current                                                              | $I_{IN}$    | Excluding RESETB                                                            | -1                   | $\pm 0.1$                | +1                   | $\mu A$          |
| RESETB Input Current                                                       | $I_{INRB}$  |                                                                             | -1                   |                          | +55                  | $\mu A$          |
| Input Capacitance                                                          | $C_{IN}$    |                                                                             |                      | 3                        |                      | pF               |
| Output High Voltage                                                        | $V_{OH}$    | $I_{LOAD} = 200\mu A$ , INTB has a 1k $\Omega$ pullup resistor to $V_{DD2}$ | $0.8 \times V_{DD2}$ |                          |                      | V                |
| Output Low Voltage                                                         | $V_{OL}$    | $I_{SINK} = 200\mu A$ , INTB has a 1k $\Omega$ pullup resistor to $V_{DD2}$ |                      |                          | $0.2 \times V_{DD2}$ | V                |
| Output Leakage Current                                                     |             | Three-state, SDO pin                                                        | -4                   | $\pm 2.5$                | +4                   | $\mu A$          |
| <b>JESD204B INPUTS (DP4-DP0, DN4-DN0)</b>                                  |             |                                                                             |                      |                          |                      |                  |
| Differential Input Return Loss                                             | $RL_{DIFF}$ |                                                                             |                      | 8                        |                      | dB               |

**Electrical Characteristics (continued)**

( $V_{DD} = V_{AVCLK} = V_{AVDD} = V_{AVDDPLL} = 1.0V$ ,  $V_{DD2} = V_{AVCLK2} = V_{AVDD2} = V_{AVDD2PLL} = V_{DD2PLL} = 1.8V$ ,  $P_{CLK} = 0dBm$ ,  $f_{CLK} = 983.04MHz$ ,  $f_{DAC} = 4915.2Mbps$ , 4x interpolation, 5-lanes, 9830.4Mbps per lane, external reference at 1.206V,  $R_{SET} = 965\Omega$  between FSADJ and DACREF,  $I_{OUTFS} = 40mA$ , output is 50 $\Omega$  double-terminated and transformer coupled (see [Figure 25](#)), PLL on.  $T_A \geq -40^\circ C$  and  $T_J \leq +110^\circ C$ , unless otherwise noted. Typical values are at  $T_J = +65 \pm 15^\circ C$ . (Note 1))

| PARAMETER                                                  | SYMBOL        | CONDITIONS                                                     | MIN   | TYP           | MAX   | UNITS    |
|------------------------------------------------------------|---------------|----------------------------------------------------------------|-------|---------------|-------|----------|
| Common-mode Input Return Loss                              | $RL_{CM}$     |                                                                |       | 6             |       | dB       |
| Receiver Differential Resistance                           | $R_{RXDIFF}$  | At DC                                                          | 80    |               | 120   | $\Omega$ |
| Minimum Differential Input Voltage                         | $V_{MIN\_IN}$ |                                                                |       | 110           |       | mVp-p    |
| Maximum Differential Input Voltage                         | $V_{MAX\_IN}$ |                                                                |       | 1050          |       | mVp-p    |
| Discrete Serial Data Rate per Lane                         | $f_{SER\_IN}$ |                                                                |       | 9830.4        |       | Mbps     |
| <b>LVDS LOGIC OUTPUT (SYNCPNP, SYNCNN, RCLKP, RCLKN)</b>   |               |                                                                |       |               |       |          |
| Differential Output Logic High Voltage                     | $V_{OH}$      | $R_{LOAD} = 100\Omega$ differential                            | 250   |               | 450   | mV       |
| Differential Output Logic Low Voltage                      | $V_{OL}$      | $R_{LOAD} = 100\Omega$ differential                            | -450  |               | -250  | mV       |
| Output Common Mode Voltage                                 | $V_{OCM}$     |                                                                | 1.125 | 1.25          | 1.375 | V        |
| Output Maximum Frequency                                   | $f_{RCLK}$    | $R_{LOAD} = 100\Omega$ differential, $C_{LOAD} = 5pF$          |       | 245.76        |       | MHz      |
| <b>CLOCK INPUT (CLKP, CLKN)</b>                            |               |                                                                |       |               |       |          |
| Power Level at Differential CLKP/CLKN Clock Input (Note 6) | $P_{CLK}$     | Sine-wave input, PLL on                                        |       | > -3          |       | dBm      |
| Common-Mode Voltage                                        | $V_{COM}$     | AC-coupled, internally biased                                  |       | 0.5           |       | V        |
| Differential Input Resistance                              | $R_{CLK}$     |                                                                |       | 100           |       | $\Omega$ |
| <b>INTERNAL DAC CLOCK PLL</b>                              |               |                                                                |       |               |       |          |
| Internal DAC Clock PLL Frequency Range                     | $f_{PLL}$     |                                                                |       | 4915.2        |       | MHz      |
| PLL Input Frequencies                                      | $f_{CLK}$     | (Note 9)                                                       |       | $f_{PLL}/MLT$ |       | MHz      |
| Minimum PLL Input Frequency Multiplier                     | $MLT_{MIN}$   | (Note 9)                                                       |       | 5             |       |          |
| Maximum PLL Input Frequency Multiplier                     | $MLT_{MAX}$   | (Note 9)                                                       |       | 20            |       |          |
| Phase Noise at 6MHz Offset                                 |               | Simulated at PLL output, does not include DAC core phase noise |       | -142          |       | dBc/Hz   |
| Cycle-to-Cycle Jitter                                      |               | Simulated at PLL output, does not include DAC core jitter      |       | 245           |       | fs       |

**Electrical Characteristics (continued)**

( $V_{DD} = V_{AVCLK} = V_{AVDD} = V_{AVDDPLL} = 1.0V$ ,  $V_{DD2} = V_{AVCLK2} = V_{AVDD2} = V_{AVDD2PLL} = V_{DD2PLL} = 1.8V$ ,  $P_{CLK} = 0dBm$ ,  $f_{CLK} = 983.04MHz$ ,  $f_{DAC} = 4915.2Msps$ , 4x interpolation, 5-lanes, 9830.4Mbps per lane, external reference at 1.206V,  $R_{SET} = 965\Omega$  between FSADJ and DACREF,  $I_{OUTFS} = 40mA$ , output is 50 $\Omega$  double-terminated and transformer coupled (see [Figure 25](#)), PLL on.  $T_A \geq -40^\circ C$  and  $T_J \leq +110^\circ C$ , unless otherwise noted. Typical values are at  $T_J = +65 \pm 15^\circ C$ . (Note 1))

| PARAMETER                                              | SYMBOL                                                                                                    | CONDITIONS                               | MIN          | TYP | MAX  | UNITS                      |
|--------------------------------------------------------|-----------------------------------------------------------------------------------------------------------|------------------------------------------|--------------|-----|------|----------------------------|
| RESET TIMING                                           |                                                                                                           |                                          |              |     |      |                            |
| RESET to Ready Delay                                   | t <sub>RRDY</sub>                                                                                         |                                          | 350000       |     |      | f <sub>CLK</sub><br>Cycles |
| SERIAL PORT INTERFACE (Note 4)                         |                                                                                                           |                                          |              |     |      |                            |
| SCLK Frequency                                         | f <sub>SCLK</sub>                                                                                         | 1/t <sub>SCLK</sub>                      | 20           |     |      | MHz                        |
| SCLK to CSB Falling Edge Setup Time                    | t <sub>CSS</sub>                                                                                          |                                          | 10           |     |      | ns                         |
| Minimum SCLK to CSB Falling Edge Hold Time             | t <sub>CSH</sub>                                                                                          |                                          | 40           |     |      | ns                         |
| Minimum SCLK Falling Edge to CSB Rising Edge Hold Time | t <sub>CRH</sub>                                                                                          |                                          | 9.765        |     |      | ns                         |
| SDI to SCLK Hold Time                                  | t <sub>SDH</sub>                                                                                          | Data write                               | 0            |     |      | ns                         |
| SDI to SCLK Setup Time                                 | t <sub>SDS</sub>                                                                                          | Data write                               | 5            |     |      | ns                         |
| Minimum SCLK to SDO Data Delay                         | t <sub>SDD_MIN</sub>                                                                                      | Data read, 10pF load from SDO to ground  | 1.5          |     |      | ns                         |
|                                                        |                                                                                                           | Data read, 100pF load from SDO to ground | 3.5          |     |      |                            |
| Maximum SCLK to SDO Data Delay                         | t <sub>SDD_MAX</sub>                                                                                      | Data read, 10pF load from SDO to ground  | 8            |     |      | ns                         |
|                                                        |                                                                                                           | Data read, 100pF load from SDO to ground | 11           |     |      |                            |
| POWER SUPPLY                                           |                                                                                                           |                                          |              |     |      |                            |
| 1.0V Supply Voltage Range                              | V <sub>DD</sub> , V <sub>AVDD</sub> , V <sub>AVDDPLL</sub> , V <sub>AVCLK</sub>                           |                                          | 0.95         | 1.0 | 1.05 | V                          |
| 1.8V Supply Voltage Range                              | V <sub>DD2</sub> , V <sub>AVCLK2</sub> , V <sub>AVDD2</sub> , V <sub>AVDD2PLL</sub> , V <sub>DD2PLL</sub> |                                          | 1.71         | 1.8 | 1.89 | V                          |
| 1.0V Digital Supply Current                            | I <sub>VDD</sub>                                                                                          | (Note 3)                                 | 550      750 |     |      | mA                         |
| 1.8V Digital Supply Current                            | I <sub>VDD2</sub>                                                                                         | (Note 3)                                 | 500      550 |     |      | mA                         |
| 1.0V Clock Supply Current                              | I <sub>AVCLK</sub>                                                                                        | (Note 3)                                 | 350      400 |     |      | mA                         |
| 1.8V Clock Supply Current                              | I <sub>AVCLK2</sub>                                                                                       | (Note 3)                                 | 51      60   |     |      | mA                         |

**Electrical Characteristics (continued)**

( $V_{DD} = V_{AVCLK} = V_{AVDD} = V_{AVDDPLL} = 1.0V$ ,  $V_{DD2} = V_{AVCLK2} = V_{AVDD2} = V_{AVDD2PLL} = V_{DD2PLL} = 1.8V$ ,  $P_{CLK} = 0dBm$ ,  $f_{CLK} = 983.04MHz$ ,  $f_{DAC} = 4915.2Msps$ , 4x interpolation, 5-lanes, 9830.4Mbps per lane, external reference at 1.206V,  $R_{SET} = 965\Omega$  between FSADJ and DACREF,  $I_{OUTFS} = 40mA$ , output is  $50\Omega$  double-terminated and transformer coupled (see [Figure 25](#)), PLL on.  $T_A \geq -40^\circ C$  and  $T_J \leq +110^\circ C$ , unless otherwise noted. Typical values are at  $T_J = +65 \pm 15^\circ C$ . (Note 1))

| PARAMETER                        | SYMBOL         | CONDITIONS | MIN | TYP  | MAX  | UNITS |
|----------------------------------|----------------|------------|-----|------|------|-------|
| 1.0V Analog Supply Current       | $I_{AVDD}$     | (Note 3)   |     | 230  | 270  | mA    |
| 1.8V Analog Supply Current       | $I_{AVDD2}$    | (Note 3)   |     | 270  | 295  | mA    |
| 1.0V Clock PLL Supply Current    | $I_{AVDDPLL}$  | (Note 3)   |     | 7    | 15   | mA    |
| 1.8V Clock PLL Supply Current    | $I_{AVDD2PLL}$ | (Note 3)   |     | 28   | 35   | mA    |
| 1.8V JESD204B PLL Supply Current | $I_{VDD2PLL}$  | (Note 3)   |     | 27   | 35   | mA    |
| Total Power Dissipation          | $P_{TOTAL}$    | (Note 3)   |     | 2700 | 3100 | mW    |

**Note 1:** All specifications are guaranteed by test at  $T_J = +60^\circ C$  and  $T_J = +115^\circ C$  to an accuracy of  $\pm 10^\circ C$ , unless otherwise noted. Specifications at  $T_J < +60^\circ C$  are guaranteed by design and characterization. Timing specifications are guaranteed by design and characterization.

**Note 2:** Adjusted DAC update rate is defined as the rate at which the digital signal is converted to an analog signal and the output analog values are changed by the DAC.

**Note 3:** Eight 6MHz 256-QAM carriers,  $f_{OUT} = 575MHz$ , Average Total Power = -12dBFS, input power is referenced to a  $50\Omega$  load.

**Note 4:** Specification guaranteed by design and characterization and functionally tested during production.

**Note 5:** Adjacent channel is 750kHz from channel block edge to 6MHz from channel block edge. Next adjacent channel is 6MHz from channel block edge to 12MHz from channel block edge. Third adjacent channel is 12MHz from channel block edge to 18MHz from channel block edge.

**Note 6:** Input power is referenced to a  $50\Omega$  load.

**Note 7:** Excludes losses from cables and matching network at DAC output, also excludes  $\sin(x)/x$  roll-off unless otherwise noted.

**Note 8:** Settling time is dominated by the interpolation filter step response.

**Note 9:** DAC PLL reference input frequency multiplier (MLT), is defined by the ratio of the PLL feedback divide value (M) and the input reference divide value (N).  $MLT = M \div N$ , where M is 20 and N can be 1, 2, or 4; consistent with valid configurations listed in [Table 5](#).

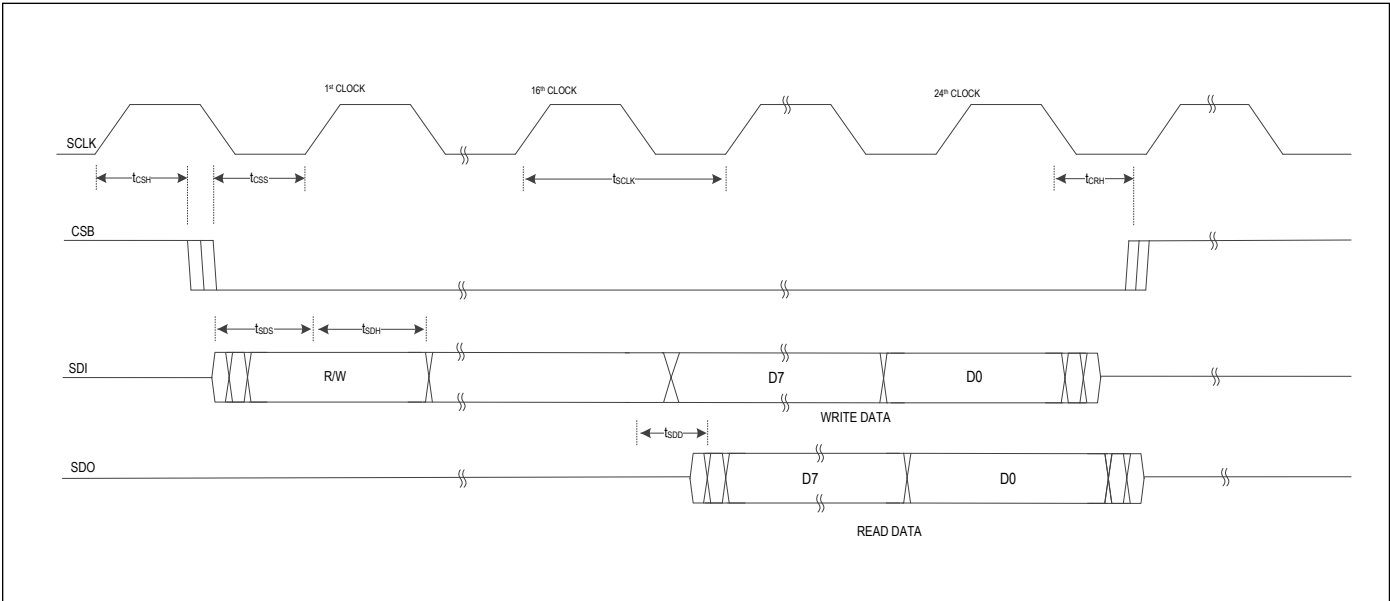
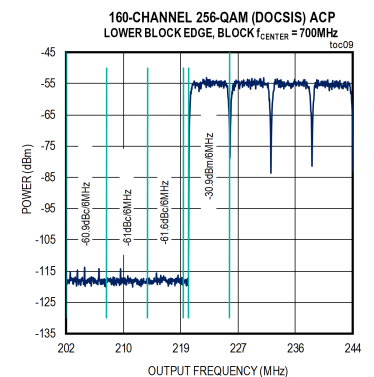
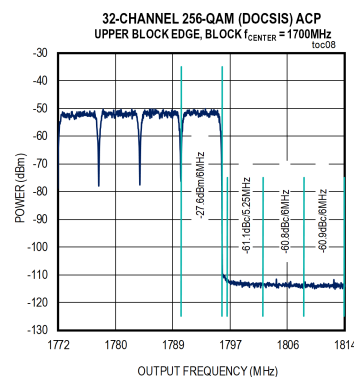
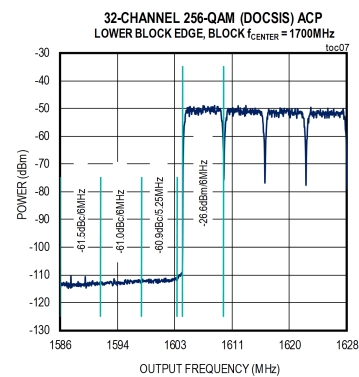
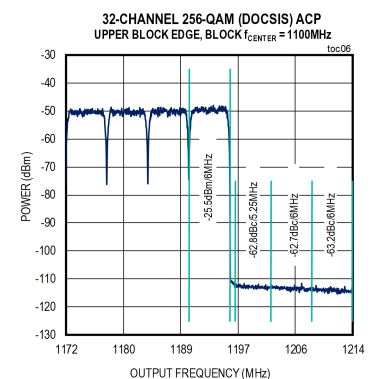
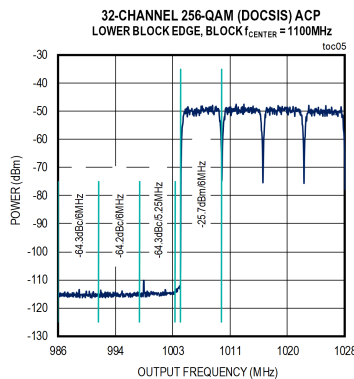
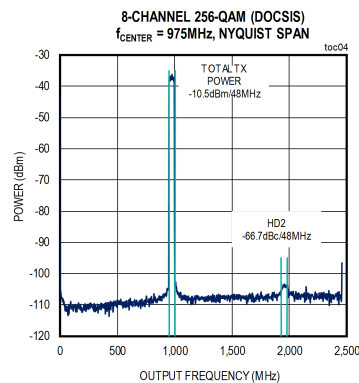
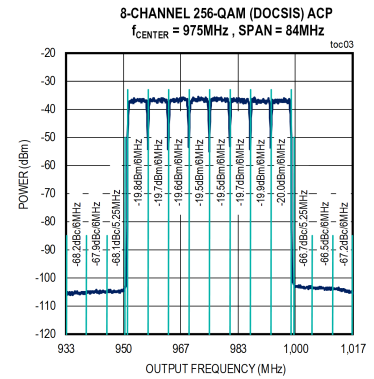
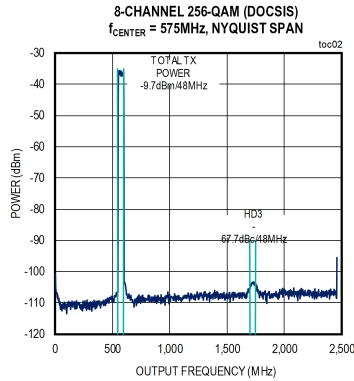
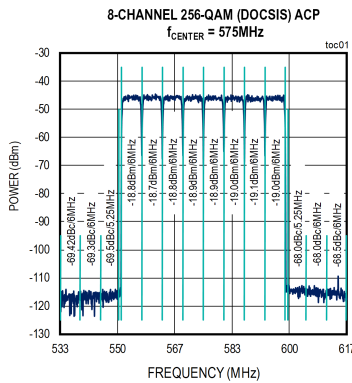


Figure 1. Serial Interface Timing Diagram

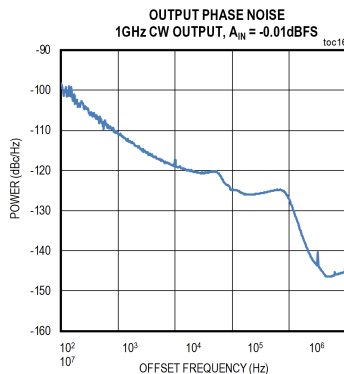
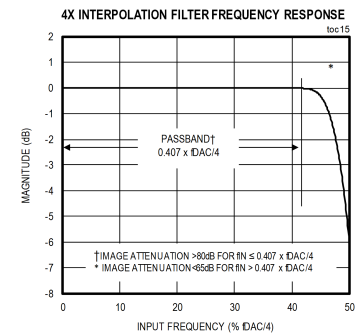
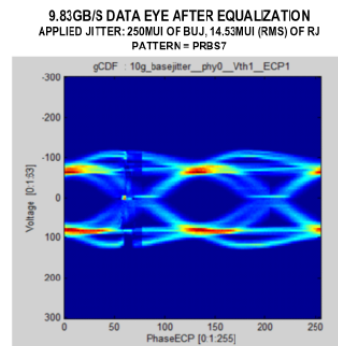
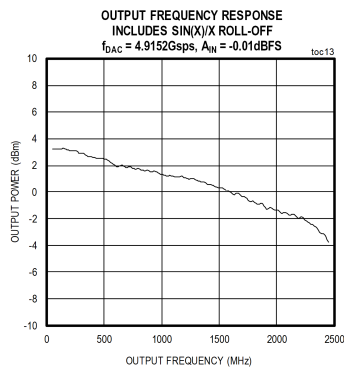
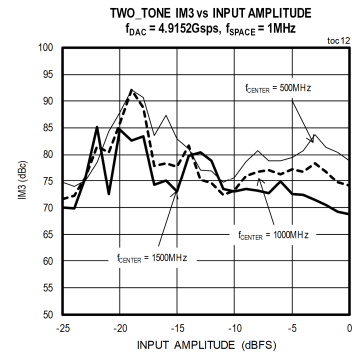
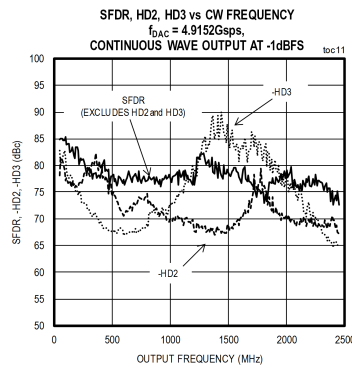
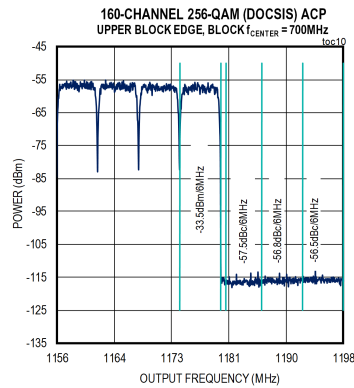
## Typical Operating Characteristics

( $V_{DD} = V_{AVCLK} = V_{AVDD} = V_{AVDDPLL} = 1.0V$ ,  $V_{DD2} = V_{AVCLK2} = V_{AVDD2} = V_{AVDD2PLL} = V_{DD2PLL} = 1.8V$ ,  $P_{CLK} = 0dBm$ ,  $f_{CLK} = 983.04MHz$ ,  $f_{DAC} = 4915.2Mbps$ , 4x interpolation, 5-lanes, 9830.4Mbps per lane, external reference at 1.20625V,  $R_{SET} = 965\Omega$  between FSADJ and DACREF,  $I_{OUTFS} = 40mA$ , output is 50 $\Omega$  double-terminated and transformer coupled (see Figure 25), PLL on. Typical values are at  $T_J = +65 \pm 15^\circ C$ .)



## Typical Operating Characteristics (continued)

( $V_{DD} = V_{AVCLK} = V_{AVDD} = V_{AVDDPLL} = 1.0V$ ,  $V_{DD2} = V_{AVCLK2} = V_{AVDD2} = V_{AVDD2PLL} = V_{DD2PLL} = 1.8V$ ,  $P_{CLK} = 0dBm$ ,  $f_{CLK} = 983.04MHz$ ,  $f_{DAC} = 4915.2Mps$ , 4x interpolation, 5-lanes, 9830.4Mbps per lane, external reference at 1.20625V,  $R_{SET} = 965\Omega$  between FSADJ and DACREF,  $I_{OUTFS} = 40mA$ , output is 50 $\Omega$  double-terminated and transformer coupled (see Figure 25), PLL on. Typical values are at  $T_J = +65 \pm 15^\circ C$ .)



# 16-Bit, 4.9Gbps Wideband Interpolating and Modulating RF DAC with JESD204B Interface

TOP VIEW

DIE
  GND
  SUPPLIES
  CRITICAL ANALOG AND RF
  RF DATA AND CLOCK
  ANALOG. DIGITAL IO
  NO CONNECT

| Pin | Signal  | Category   |
|-----|---------|------------|
| A1  | REFIO   | IO         |
| A2  | CSBP    | IO         |
| A3  | AVCLK   | Supply     |
| A4  | AVDD2   | Supply     |
| A5  | AVDD2   | Supply     |
| A6  | OUTP    | IO         |
| A7  | OUTN    | IO         |
| A8  | AVDD2   | Supply     |
| A9  | AVDD2   | Supply     |
| A10 | AVCLK   | Supply     |
| A11 | VCORTN  | IO         |
| A12 | PLLCOMP | IO         |
| B1  | DACREF  | IO         |
| B2  | FSADJ   | IO         |
| B3  | GND     | GND        |
| B4  | AVDD2   | Supply     |
| B5  | AVDD2   | Supply     |
| B6  | OUTP    | IO         |
| B7  | OUTN    | IO         |
| B8  | AVDD2   | Supply     |
| B9  | AVDD2   | Supply     |
| B10 | GND     | GND        |
| B11 | VCORBYP | IO         |
| B12 | AVCLK2  | IO         |
| C1  | GND     | GND        |
| C2  | AVDD2   | Supply     |
| C3  | AVDD2   | Supply     |
| C4  | GND     | GND        |
| C5  | GND     | GND        |
| C6  | GND     | GND        |
| C7  | GND     | GND        |
| C8  | GND     | GND        |
| C9  | GND     | GND        |
| C10 | GND     | GND        |
| C11 | GND     | GND        |
| C12 | GND     | GND        |
| D1  | GND     | GND        |
| D2  | GND     | GND        |
| D3  | GND     | GND        |
| D4  | GND     | GND        |
| D5  | GND     | GND        |
| D6  | GND     | GND        |
| D7  | GND     | GND        |
| D8  | GND     | GND        |
| D9  | GND     | GND        |
| D10 | GND     | GND        |
| D11 | AVCLK2  | Supply     |
| D12 | CLKP    | IO         |
| E1  | SCLK    | IO         |
| E2  | CSB     | IO         |
| E3  | GND     | GND        |
| E4  | AVDD    | Supply     |
| E5  | GND     | GND        |
| E6  | GND     | GND        |
| E7  | GND     | GND        |
| E8  | GND     | GND        |
| E9  | AVDD    | Supply     |
| E10 | GND     | GND        |
| E11 | AVCLK   | Supply     |
| E12 | CLKN    | IO         |
| F1  | SDI     | IO         |
| F2  | RESETB  | IO         |
| F3  | GND     | GND        |
| F4  | GND     | GND        |
| F5  | VDD     | Supply     |
| F6  | VDD     | Supply     |
| F7  | VDD     | Supply     |
| F8  | VDD     | Supply     |
| F9  | GND     | GND        |
| F10 | GND     | GND        |
| F11 | GND     | GND        |
| F12 | GND     | GND        |
| G1  | SDO     | IO         |
| G2  | INTB    | IO         |
| G3  | MUTE    | IO         |
| G4  | VDD2    | Supply     |
| G5  | VDD     | Supply     |
| G6  | GND     | GND        |
| G7  | GND     | GND        |
| G8  | VDD     | Supply     |
| G9  | VDD2    | Supply     |
| G10 | GND     | GND        |
| G11 | GND     | GND        |
| G12 | GND     | GND        |
| H1  | SYNCP   | IO         |
| H2  | DP0     | IO         |
| H3  | NC      | No Connect |
| H4  | VDD2    | Supply     |
| H5  | GND     | GND        |
| H6  | GND     | GND        |
| H7  | GND     | GND        |
| H8  | GND     | GND        |
| H9  | VDD2    | Supply     |
| H10 | GND     | GND        |
| H11 | NC      | No Connect |
| H12 | TESTP   | IO         |
| J1  | SYNCP   | IO         |
| J2  | DN0     | IO         |
| J3  | NC      | No Connect |
| J4  | VDD2    | Supply     |
| J5  | GND     | GND        |
| J6  | GND     | GND        |
| J7  | GND     | GND        |
| J8  | GND     | GND        |
| J9  | VDD2    | Supply     |
| J10 | GND     | GND        |
| J11 | NC      | No Connect |
| J12 | TESTN   | IO         |
| K1  | GND     | GND        |
| K2  | GND     | GND        |
| K3  | GND     | GND        |
| K4  | GND     | GND        |
| K5  | GND     | GND        |
| K6  | RCLKP   | IO         |
| K7  | RCLKN   | IO         |
| K8  | GND     | GND        |
| K9  | GND     | GND        |
| K10 | GND     | GND        |
| K11 | TDA     | IO         |
| K12 | GND     | GND        |
| L1  | DP1     | IO         |
| L2  | GND     | GND        |
| L3  | DP2     | IO         |
| L4  | GND     | GND        |
| L5  | TESTEN  | IO         |
| L6  | NC      | No Connect |
| L7  | NC      | No Connect |
| L8  | VDD2PLL | Supply     |
| L9  | GND     | GND        |
| L10 | DP3     | IO         |
| L11 | GND     | GND        |
| L12 | DP4     | IO         |
| M1  | DN1     | IO         |
| M2  | GND     | GND        |
| M3  | DN2     | IO         |
| M4  | GND     | GND        |
| M5  | JRES    | IO         |
| M6  | GND     | GND        |
| M7  | VSSPLL  | Supply     |
| M8  | CAPT    | IO         |
| M9  | GND     | GND        |
| M10 | DN3     | IO         |
| M11 | TDC     | IO         |
| M12 | DN4     | IO         |

## Pin Description

| PIN                                                                                                                                                                                                              | NAME     | FUNCTION                                                                                                                                                                                                                                                                             |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A1                                                                                                                                                                                                               | REFIO    | Reference Voltage Input/Output. REFIO outputs an internal 1.2V band-gap reference voltage. REFIO has a 10k $\Omega$ series resistance and can be driven using an external 1.2V reference voltage. Connect a 1 $\mu$ F capacitor between REFIO and DACREF.                            |
| A2                                                                                                                                                                                                               | CSBP     | DAC Current Source Bypass. Connect 1.0 $\mu$ F capacitor between CSBP and DACREF.                                                                                                                                                                                                    |
| A3, A10                                                                                                                                                                                                          | AVCLK    | 1.0V Supply Input for Clock                                                                                                                                                                                                                                                          |
| A4-A5,<br>A8-A9,<br>B4-B5,<br>B8-B9,<br>C2-C3                                                                                                                                                                    | AVDD2    | Analog 1.8V Supply Input                                                                                                                                                                                                                                                             |
| A6, B6                                                                                                                                                                                                           | OUTP     | Positive Terminal of Differential DAC Output                                                                                                                                                                                                                                         |
| A7, B7                                                                                                                                                                                                           | OUTN     | Negative Terminal of Differential DAC Output                                                                                                                                                                                                                                         |
| A11                                                                                                                                                                                                              | VCORTN   | Ground for VCO Loop Filter                                                                                                                                                                                                                                                           |
| A12                                                                                                                                                                                                              | PLLCOMP  | Analog I/O for DAC PLL Loop Filter Connection                                                                                                                                                                                                                                        |
| B1                                                                                                                                                                                                               | DACREF   | Internal DAC Reference Ground Used for DAC Current Source Bypass Ground. Do not connect to board ground (GND).                                                                                                                                                                       |
| B2                                                                                                                                                                                                               | FSADJ    | Analog Input for DAC Full-Scale Output Current Adjustment. A resistor from FSADJ to DACREF sets the full-scale output current of the DAC. To obtain a 40mA full-scale output current using the internal reference voltage, connect a 965 $\Omega$ resistor between FSADJ and DACREF. |
| B3, B10,<br>C1,<br>C4-C12,<br>D1-D10,<br>E3, E5-E8,<br>E10,<br>F3-F4,<br>F9-F12,<br>G6-G7,<br>G10-G12,<br>H5-H8,<br>H10,<br>J5-J8, J10,<br>K1-K5,<br>K8-K10,<br>K12, L2,<br>L4, L9,<br>L11, M2,<br>M4, M6,<br>M9 | GND      | Ground                                                                                                                                                                                                                                                                               |
| B11                                                                                                                                                                                                              | VCOBYP   | VCO Loop Filter Connection                                                                                                                                                                                                                                                           |
| B12                                                                                                                                                                                                              | AVCLK2   | 1.8V Supply Input for Clock                                                                                                                                                                                                                                                          |
| D11                                                                                                                                                                                                              | AVDD2PLL | 1.8V DAC Clock PLL Supply                                                                                                                                                                                                                                                            |

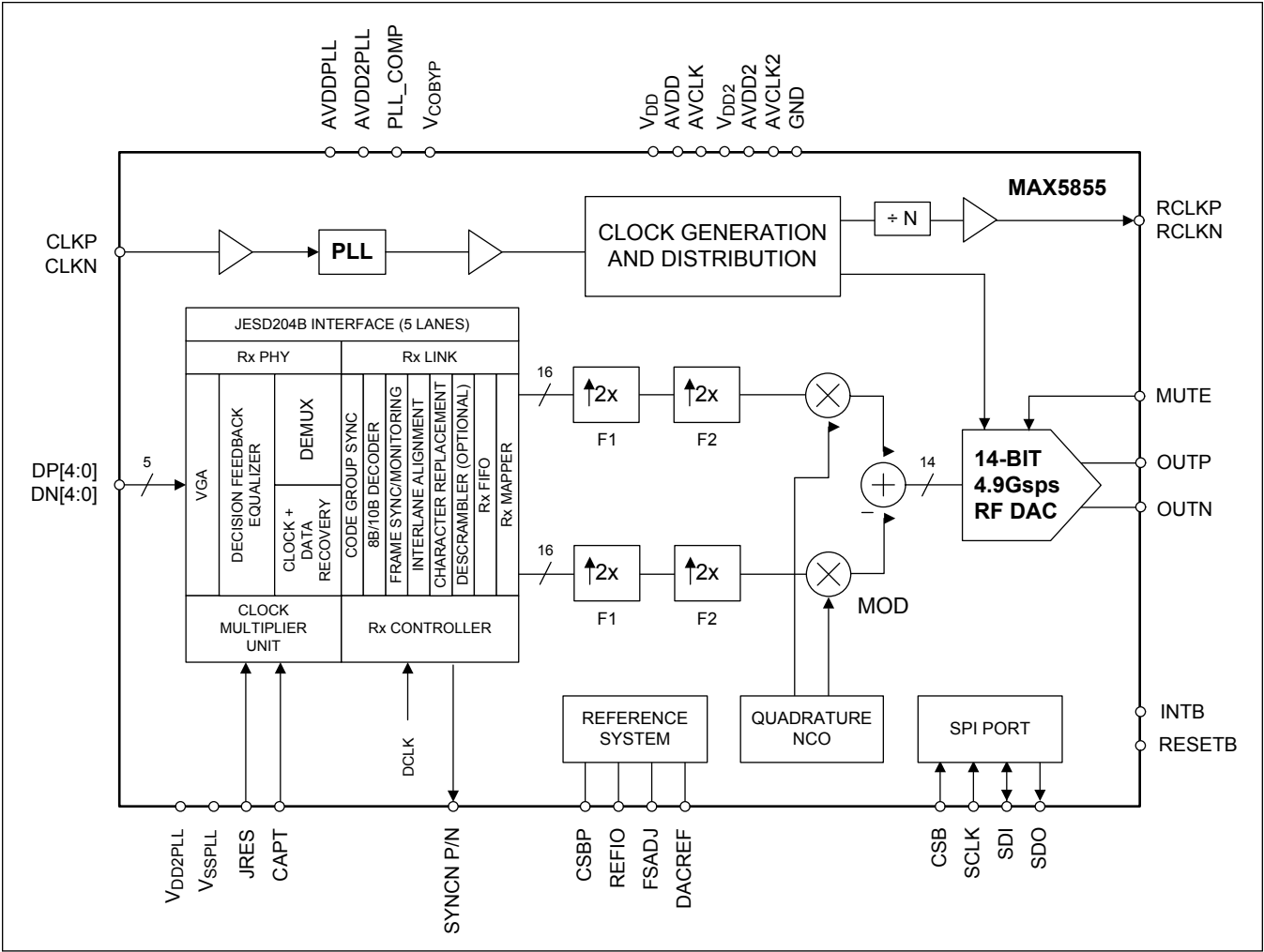
## Pin Description (continued)

| PIN                                   | NAME                | FUNCTION                                                                                                                                                                                                                                                                                      |
|---------------------------------------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D12, E12                              | CLKP,<br>CLKN       | Clock Input. Multipurpose pin that generates following internal clocks based on use case:<br><br>1) Reference clock for DAC PLL which in turn generates the DACCLK.<br><br>2) Device clock (DCLK) for JESD204B interface.<br><br>An internal 100Ω termination resistor connects CLKP to CLKN. |
| E1                                    | SCLK                | Digital CMOS Input for Serial Port Interface Clock                                                                                                                                                                                                                                            |
| E2                                    | CSB                 | Digital CMOS Input for Serial Port Interface. MAX5855 is selected when CSB = low.                                                                                                                                                                                                             |
| E4, E9                                | AVDD                | Analog 1.0V Supply Input                                                                                                                                                                                                                                                                      |
| E11                                   | AVDDPLL             | 1.0V DAC Clock PLL Supply                                                                                                                                                                                                                                                                     |
| F1                                    | SDI                 | Digital CMOS Input/Output for Serial Port Interface. Data input in 4-wire SPI mode and data input/output in 3-wire SPI mode.                                                                                                                                                                  |
| F2                                    | RESETB              | Digital CMOS Input with an Internal 50kΩ Pulldown Resistor. Device is reset when RESETB is low. Hold RESETB low during device startup. RESETB must be set high for normal operation after startup.                                                                                            |
| F5-F8, G5,<br>G8                      | V <sub>DD</sub>     | 1.0V Supply Input for Digital Core                                                                                                                                                                                                                                                            |
| G1                                    | SDO                 | Digital CMOS Output for Serial Port Interface. Data output in 4-wire SPI mode.                                                                                                                                                                                                                |
| G2                                    | INTB                | Digital CMOS Output for Interrupt                                                                                                                                                                                                                                                             |
| G3                                    | MUTE                | Digital CMOS Input. With MUTE high the DAC output is muted and with MUTE low, the DAC output is active.                                                                                                                                                                                       |
| G4, G9,<br>H3-H4,<br>H9, J3-J4,<br>J9 | V <sub>DD2</sub>    | 1.8V Supply Input for Digital I/O                                                                                                                                                                                                                                                             |
| H1, J1                                | SYNCP,<br>SYNCPN    | LVDS Output. Active-low JESD204B error reporting signal (SYNC~) from Rx device (DAC) to Tx device (FPGA/ASIC).                                                                                                                                                                                |
| H2, L1, L3,<br>L10, L12               | DP0-DP4             | Analog Input. JESD204B Serial Data Positive Input Lanes 0-4.                                                                                                                                                                                                                                  |
| H3, H11,<br>J3, J11,<br>L6, L7        | NC                  | No Connect                                                                                                                                                                                                                                                                                    |
| H12, J12                              | TESTP,<br>TESTN     | Factory Use Only. Connect to GND.                                                                                                                                                                                                                                                             |
| J2, M1,<br>M3, M10,<br>M12            | DN0-DN4             | Analog Input. JESD204B Serial Data Negative Input Lanes 0-4.                                                                                                                                                                                                                                  |
| K6-K7                                 | RCLKP,<br>RCLKN     | LVDS Reference Clock Output for Sample Rate Synchronization to DAC Clock. If not used, terminate differential with a 100Ω resistor.                                                                                                                                                           |
| K11                                   | TDA                 | Temperature Sensor Diode Anode. Connect TDC and TDA to ground if not used.                                                                                                                                                                                                                    |
| L5                                    | TESTEN              | Factory Use Only. Connect to GND.                                                                                                                                                                                                                                                             |
| L8                                    | V <sub>DD2PLL</sub> | JESD204B PLL 1.8V Power Supply                                                                                                                                                                                                                                                                |
| M5                                    | JRES                | Analog Input. JESD204B Current Biasing.                                                                                                                                                                                                                                                       |
| M7                                    | V <sub>SSPLL</sub>  | Clock Multiplier Unit (CMU) PLL Ground                                                                                                                                                                                                                                                        |

Pin Description (continued)

| PIN | NAME | FUNCTION                                                                     |
|-----|------|------------------------------------------------------------------------------|
| M8  | CAPT | Analog Input. JESD204B PLL Loop Filter Input.                                |
| M11 | TDC  | Temperature Sensor Diode Cathode. Connect TDC and TDA to ground if not used. |

Functional Diagrams



## Detailed Description

The MAX5855 is a high-performance, interpolating and modulating, 14-bit, 4.9Gsps RF DAC designed for DOCSIS 3.1/3.0 remote PHY devices, CCAP, digital video broadcast modulators, point-to-point wireless, and instrumentation. The device can synthesize up to 1GHz of instantaneous bandwidth at frequencies up to the Nyquist bandwidth ( $f_{DAC}/2$ ) of the DAC. The major functional blocks of the device include a five-lane JESD204B interface which accepts 16-bit input data, interpolation filters, a digital quadrature modulator and NCO, clock multiplying PLL + VCO and a 14-bit, 4.9Gsps RF DAC core. The supporting functional blocks include the clock distribution system, reference system, and SPI interface. See the detailed [Functional Diagram](#).

The 16-bit input data enhances the accuracy of the interpolation and modulation functions and ensures true 14-bit data is presented to the RF DAC core. The 16-bit input baseband data is supplied to the device using a five lane JESD204B (DP[4:0]/DN[4:0]) interface operating at 9.8304Gbps.

The five-lane JESD204B interface has the following major components:

- A high-speed input receiver (Rx) consisting of a physical (PHY) layer for each of the five lanes and a common clock multiplier unit (CMU). The PHY layer contains a variable gain amplifier (VGA) which receives the incoming signal and decision feedback equalizer (DFE) to suppress inter-symbol interference. The PHY layer also includes a clock and data recovery (CDR) unit to latch the incoming single-bit data and a de-serializer (DEMUX) to convert the data to a 20-bit parallel data bus.
- A receiver link layer (Rx Link) takes the 20 bits from the PHY and restores the 16-bit DAC data for each of the I and Q channels. The Rx link consists of five Rx lanes, five Rx FIFOs, a Rx mapper and a Rx controller. The five Rx lanes perform code group synchronization, 8b/10b decoding, frame synchronization and monitoring, interlane alignment and monitoring, character replacement, and optional descrambling. The five lanes are fed into Rx FIFOs where data is aligned by the Rx controller. Using the Rx mapper, data from each physical channel is mapped to a logical channel.

The DSP path consists of 4x linear phase interpolation filters for each of the I and Q channels. Interpolation reduces the required input data rate to the device, relaxing the requirements on the FPGA or ASIC. In addition, interpolation increases the separation between the desired signal and its aliased image easing filter design requirements.

After passing through the 4x interpolation stage, the complex signal is modulated using the LO signal generated by the NCO and the digital quadrature modulator. The NCO allows for fully agile modulation of the input baseband signal for direct RF synthesis with 32 bits of frequency-setting resolution. Placing the modulator at the output of the interpolator chain allows for fully agile placement of the output carrier frequency within the Nyquist band of the DAC. The quadrature modulator produces a real signal at its output, which is fed into the 14-bit DAC core where it is converted to an analog RF signal. The analog output produces a full-scale current between 10mA and 40mA, driving 50Ω differential loads.

The clock distribution system provides a low-noise differential input buffer for the external master DAC clock (CLKP/CLKN) and delivers all the necessary clocks to the internal blocks. The master DAC clock input accepts a differential sine-wave or square-wave signal. A clock multiplying PLL and VCO is used to internally generate the 4915.2MHz sampling clock using reference frequencies of 245.76MHz, 491.52MHz or 983.04MHz. The device provides a divided reference clock (RCLKP/RCLKN) to ensure synchronization between the data source (FPGA or ASIC) and the DAC. The SYNCN output can be used for error reporting from the DAC to the data source.

The reference system delivers the reference current to the DAC current source array and all bias currents necessary for circuit operation. The reference system also includes a bypassable band-gap reference, which can be used as a reference for the DAC full-scale current.

The SPI port is a bidirectional interface used for reading and writing status and control registers to configure the device.

The device operates from 1.0V and 1.8V power-supply voltages and consumes 2.7W at 4.9Gsps.

Supported DAC Update Rate and JESD204B Data Rates

Table 1. Complex I/Q Base Band Up-Conversion

|                                        |         |
|----------------------------------------|---------|
| DAC Update Rate: DACCLK (MSPs)         | 4915.20 |
| Input Sample Rate – I and Q each (MHz) | 1228.8  |
| Instantaneous Bandwidth (MHz)          | 1000    |

Table 2. Lane Rate

|                          |         |
|--------------------------|---------|
| DACCLK (MSPs)            | 4915.20 |
| Number of JESD204B Lanes | 5       |
| Lane Rate (Mbps)         | 9830.4  |

JESD204B Interface

The JESD204B interface consists of five PHY lanes with one CMU. Each lane takes a 1-bit stream and converts it to a 20-bit bus. The link layer (LINK) takes the 20-bit bus from the PHY and restores the original 16-bit DAC data for each of the I and Q channels (Figure 2).

The JESD204B receiver specifications are compliant with LV-OIF-6G-SR and LV-OIF-11G-SR specifications from the JEDEC standard.

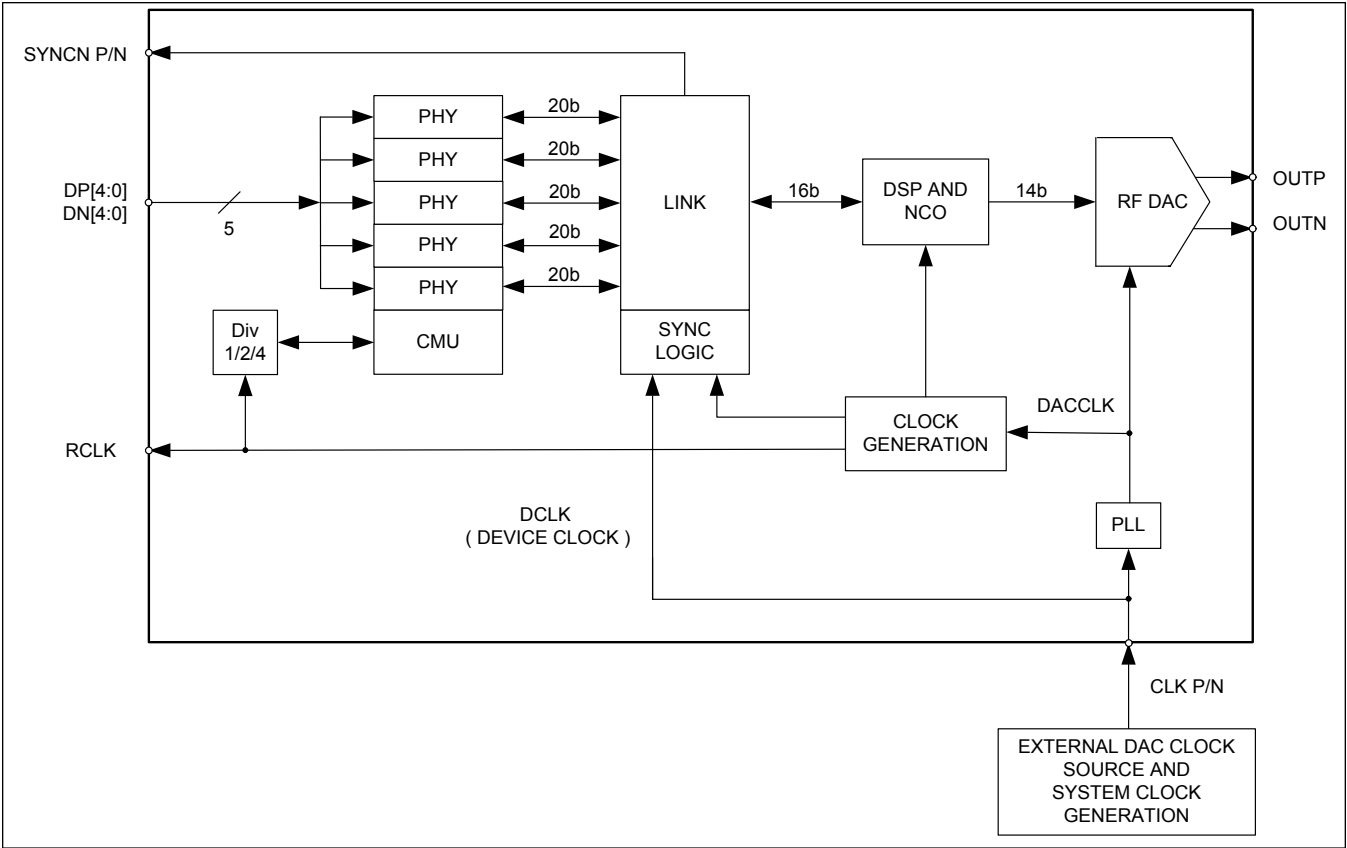


Figure 2. Simplified Diagram of JESD204B Internal to MAX5855

**JESD204B Data Interface Features**

A summary of the MAX5855 PHY and LINK features is provided below:

**Rx PHY Features**

- Programmable gain

**LINK Features**

- 8b/10b decoding
- Code group synchronization
- Inter Lane Alignment (ILA)
- $1 + x^{14} + x^{15}$  polynomial scrambling
- Character replacement
- Multiple Converter Device Alignment-Multiple Lanes (MCDA-ML) compliant
- Subclass-0 support
- Number of lanes (L): 5
- Number of data converters (M): 2
- Number of octets per frame (F): 4
- Number of samples per frame (S): 5

**Other Features**

- Disable scramble mode
- Elastic buffer depth of 320 serial bit-periods
- Detection of following 8b/10b control characters: K28.0, K28.3, K28.4, K28.5, K28.7
- Detection of following errors/conditions
  - 8b/10b running disparity error
  - 8b/10b not-in-table error
  - Unexpected control character detection
  - Code group synchronization error
  - Frame realignment detection
  - Lane realignment detection
  - Link configuration error
  - ILA failure detection
  - ILA sequence error
- Various error conditions can be enabled for error reporting through SYNC~ interface
- Continuous /K/ and ILA sequence detection
- PHY PRBS data detection for debug

Mapping of Physical to Logical Channels

Each physical channel can be mapped to any logical channel before the octet-to-sample conversion. The octet-to-sample conversion for the JESD204B link is determined by the number of lanes, number of octets-per-frame (JESD204B), and number of samples per frame. The mapping required for proper operation of the MAX5855 is shown in [Figure 3](#).

| Lane 4                | Lane 3                | Lane 2                | Lane 1                | Lane 0                |                     |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|---------------------|
| Q <sub>3</sub> [15:8] | Q <sub>1</sub> [15:8] | I <sub>4</sub> [15:8] | I <sub>2</sub> [15:8] | I <sub>0</sub> [15:8] | MLFSN' = 2_5_4_5_16 |
| Q <sub>3</sub> [7:0]  | Q <sub>1</sub> [7:0]  | I <sub>4</sub> [7:0]  | I <sub>2</sub> [7:0]  | I <sub>0</sub> [7:0]  |                     |
| Q <sub>4</sub> [15:8] | Q <sub>2</sub> [15:8] | Q <sub>0</sub> [15:8] | I <sub>3</sub> [15:8] | I <sub>1</sub> [15:8] |                     |
| Q <sub>4</sub> [7:0]  | Q <sub>2</sub> [7:0]  | Q <sub>0</sub> [7:0]  | I <sub>3</sub> [7:0]  | I <sub>1</sub> [7:0]  |                     |
| Q <sub>8</sub> [15:8] | Q <sub>6</sub> [15:8] | I <sub>9</sub> [15:8] | I <sub>7</sub> [15:8] | I <sub>5</sub> [15:8] |                     |
| Q <sub>8</sub> [7:0]  | Q <sub>6</sub> [7:0]  | I <sub>9</sub> [7:0]  | I <sub>7</sub> [7:0]  | I <sub>5</sub> [7:0]  |                     |
| Q <sub>9</sub> [15:8] | Q <sub>7</sub> [15:8] | Q <sub>5</sub> [15:8] | I <sub>8</sub> [15:8] | I <sub>6</sub> [15:8] |                     |
| Q <sub>9</sub> [7:0]  | Q <sub>7</sub> [7:0]  | Q <sub>5</sub> [7:0]  | I <sub>8</sub> [7:0]  | I <sub>6</sub> [7:0]  |                     |

Figure 3. Octet-To-Sample Conversion

High-Speed Input Receiver (Rx)

As shown in [Figure 4](#), the high-speed input receiver consists of a VGA, DFE (Decision Feedback Equalizer), CDR unit, and DEMUX. The VGA and DFE provide autonomous adaptive equalization in order to optimize the input receiver filter coefficients on a per-lane basis. The coefficients are optimized to best recover the data dependent jitter introduced by the incoming channel. The initial receiver gain and equalization settings are shadowed by internal registers that the user may override.

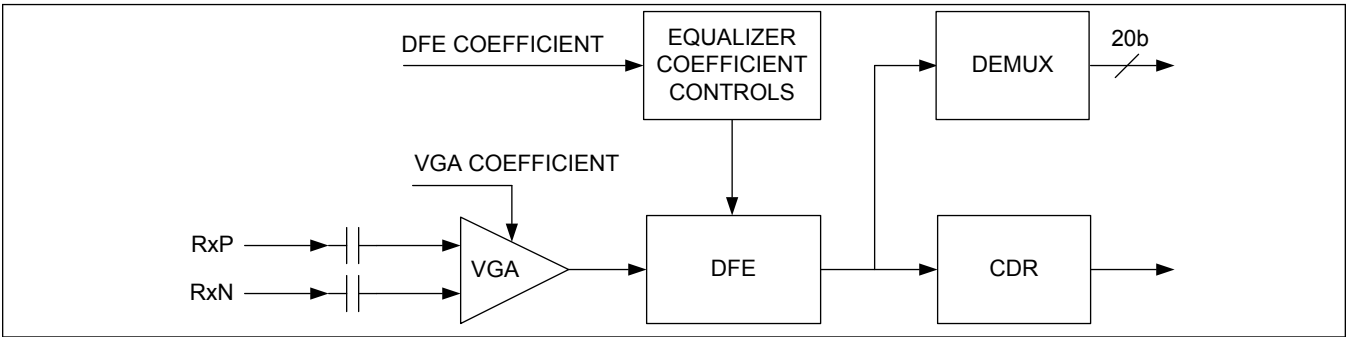


Figure 4. JESD204B Rx Physical Layer, Simplified Block Diagram

The VGA is a high-speed input receiver with high gain, allowing for excellent input sensitivity while still preserving the linearity required for optimal performance of the DFE. The receiver expects the incoming high-speed signal to be driven differential and AC-coupled to the transmitter. The receiver's common-mode input voltage is set by a self-biasing network eliminating the need for any external board circuitry. The receiver provides 100Ω differential on-chip termination between the true and complement input signals, RxP and RxN. The VGA gain settings are based on the amplitude of the incoming signal and the optimal setting to the DFE circuitry; the gain range is ±20dB, as shown in [Figure 5](#). In addition to the gain

function, there is also a boost function in the VGA to compensate for the high-frequency loss in the channel.

The PHY receiver automatically determines and sets the optimized level of equalization to suppress inter-symbol interference (ISI) caused by a dispersive channel known as decision feedback equalization. The DFE makes use of previously received data to estimate the current bit. Any trailing ISI caused by a previous bit is reconstructed and then subtracted. This technique allows for the recovery of very glossy backplane and connector channels. The PHY equalizer is designed to meet or exceed the JESD204B standard.

The CDR unit is responsible for the centering of the incoming data eye for optimal sampling and error free operation. The PHY clock and data recovery unit has multiple loop bandwidth settings to aid in achieving optimal performance for jitter tolerance.

The recovered clock generated from CDR is used to latch in the single bit data, then the DEMUX block de-serializes the single bit to 20-bit parallel data bus to subsequently be used by the Rx LINK.

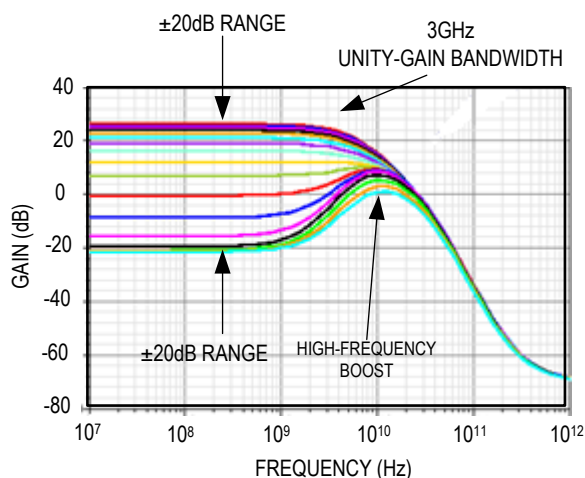


Figure 5. VGA Gain Range

**JESD204B Receiver Equalization**

The MAX5855 JESD204B receiver equalization capability exceeds the JEDEC specification for maximum interconnect length of 20cm.

The plots in [Figure 6](#) demonstrate that the JESD204B receiver equalization capability over a 30in (76cm) length of cable using the following test conditions:

- Data Rate: 9.8304Gbps
- Channel: 30in Nelco 4000-13SI plus cables and FMC connector
- 30in Nelco Traces = -14.7dB loss at 4.914GHz (see [Figure 7](#))
- Cables and connector ~ 3dB loss at 4.914GHz

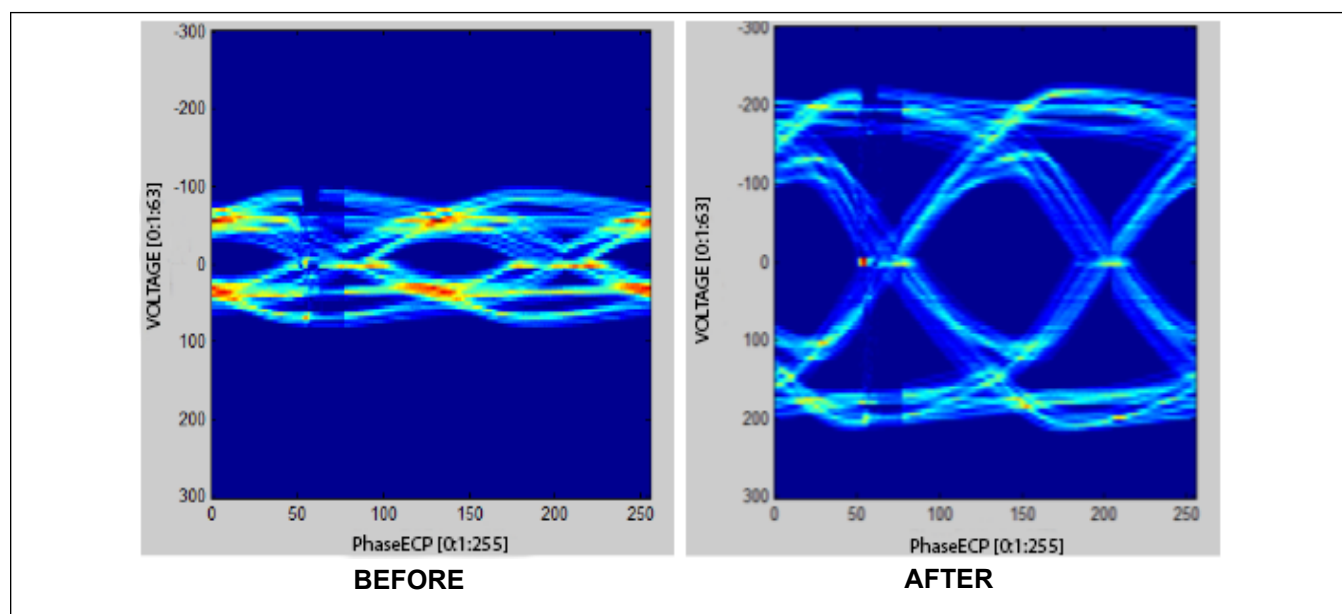


Figure 6. Receiver Equalization Eye Diagram Before and After Lane Training

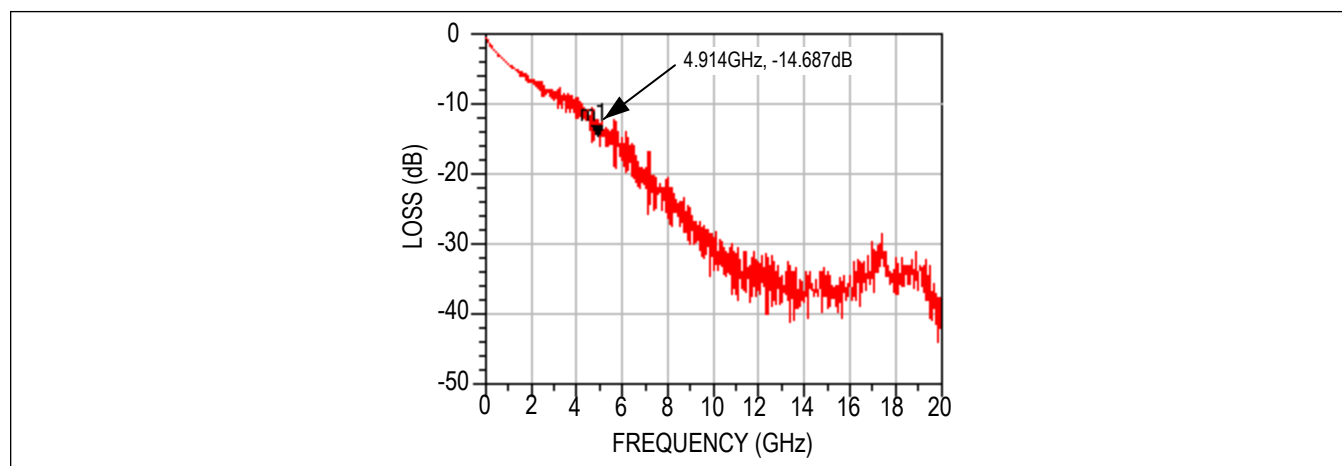


Figure 7. Channel Loss Curve (30in Nelco)

### Lane Skew Requirement

The skew between the various lanes is absorbed within the FIFOs and through the initial lane alignment process. The FIFO depth determines the amount of lane skew that can be absorbed for a particular Rx LINK configuration. A FIFO depth of 32 bytes would account for up to 320 SerDes bit periods of skew between the various lanes. In actuality, the maximum supported skew is smaller than this due to multiple bytes written to and read from the FIFO in a single write/read clock cycle in various modes. The maximum supported skew is also reduced due to the write- to read-clock synchronization uncertainty. A minimum and maximum FIFO depth can be set (CfgrFIFO at address 0x041C) and the configured FIFO range determines the actual lane skew supported by the MAX5855.

### Link Layer (LINK)

The Rx LINK layer for the MAX5855 consists of 5 lanes interfacing to the 5 PHYs. The data from the 5 lanes is passed through FIFOs in order to align the configured number of lanes in JESD204B Subclass-0 mode. The Rx controller generates a SYNCN signal for error reporting as specified by the JESD204B standard. The data from the FIFOs are then mapped into I and Q sample data for the DSP to process.

Each of the 5 lanes in the Rx LINK operates independently and includes code group synchronization operating on the 20-bit input from the PHY, 8b/10b decoding, frame synchronization and monitoring, lane alignment and monitoring, character replacement and optional descrambling. All these functions are specified in the JESD204B standard. In addition to extracting the octets, which are later combined into I and Q samples, the Rx LINK also monitors and acts on various error conditions. Most error conditions can be enabled for error reporting to the transmit logic service through the SYNCN signal. See link layer configuration registers for more detail.

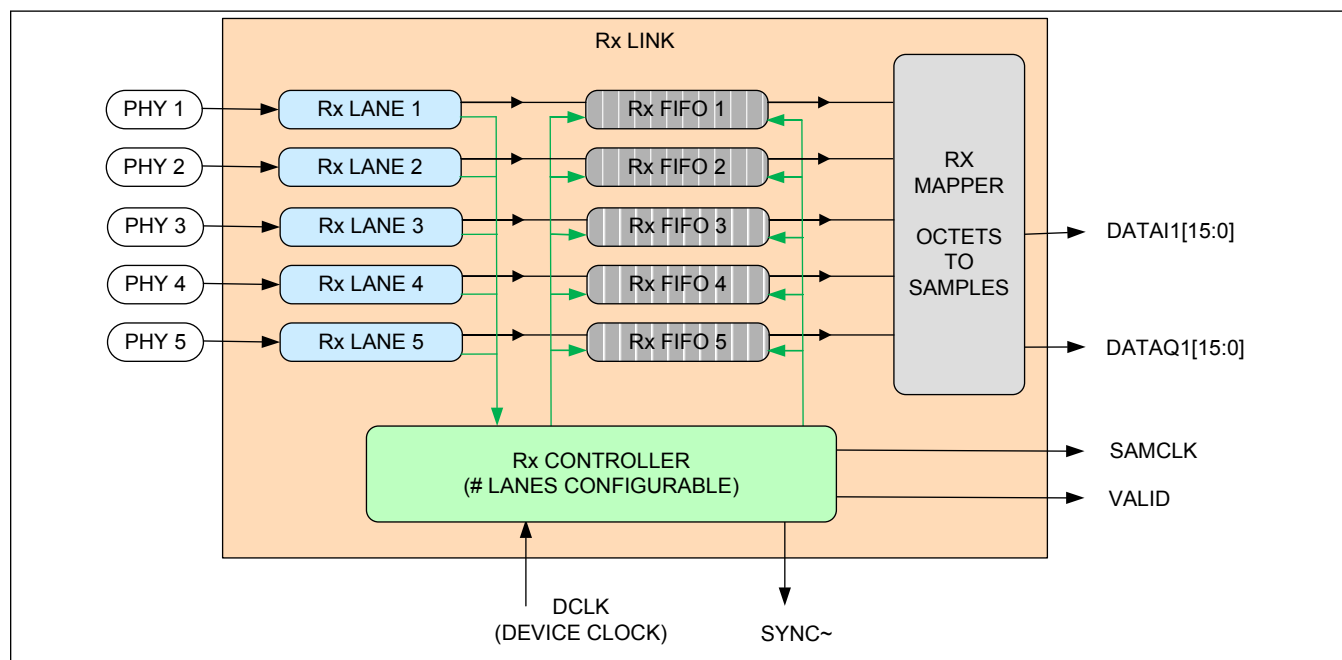


Figure 8. JESD204B Receive Link Layer Block Diagram

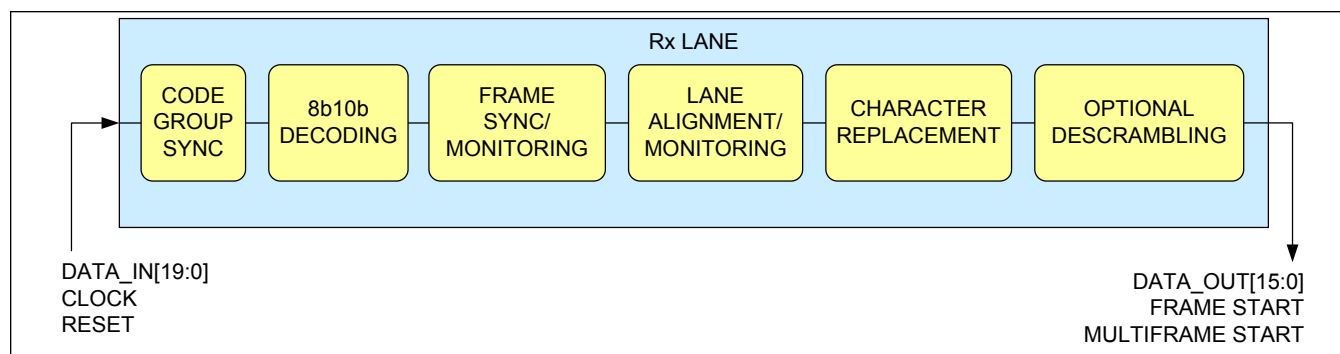


Figure 9. JESD204B Receive Lane Block Diagram

On the input-side of the Rx LANE there are 20 bits of data and the CLOCK from the PHY, along with a synchronous RESET. On the output-side are 16 bits of data (two octets), FRAME START, and MULTIFRAME START signals, which mark the two bytes of data.

### Interface Timing for Subclass-0

The JESD204B LINK layer protocol requires the frame clock of both the transmitter and receiver devices to be synchronized. Figure 10 shows the JESD204B-TX device's synchronization with the MAX5855 using the SYNCN signal. Initially, the internal clocks of the two devices are running independently. As shown, the SYNCN signal is generated by the MAX5855 using its frame clock which, in turn, is used by the JESD204B-TX device to align its own frame clock.

The Rx Controller waits for the FIFO write to start in all the enabled lanes and then initiates a read start to all the FIFOs. The FIFO reads start at the Frame/Multiframe boundary following the lane alignment sequence. This process aligns the data on all enabled lanes with a minimum latency through the Rx LINK.

See JEDEC Standard No. 204B.01, Figure 11.

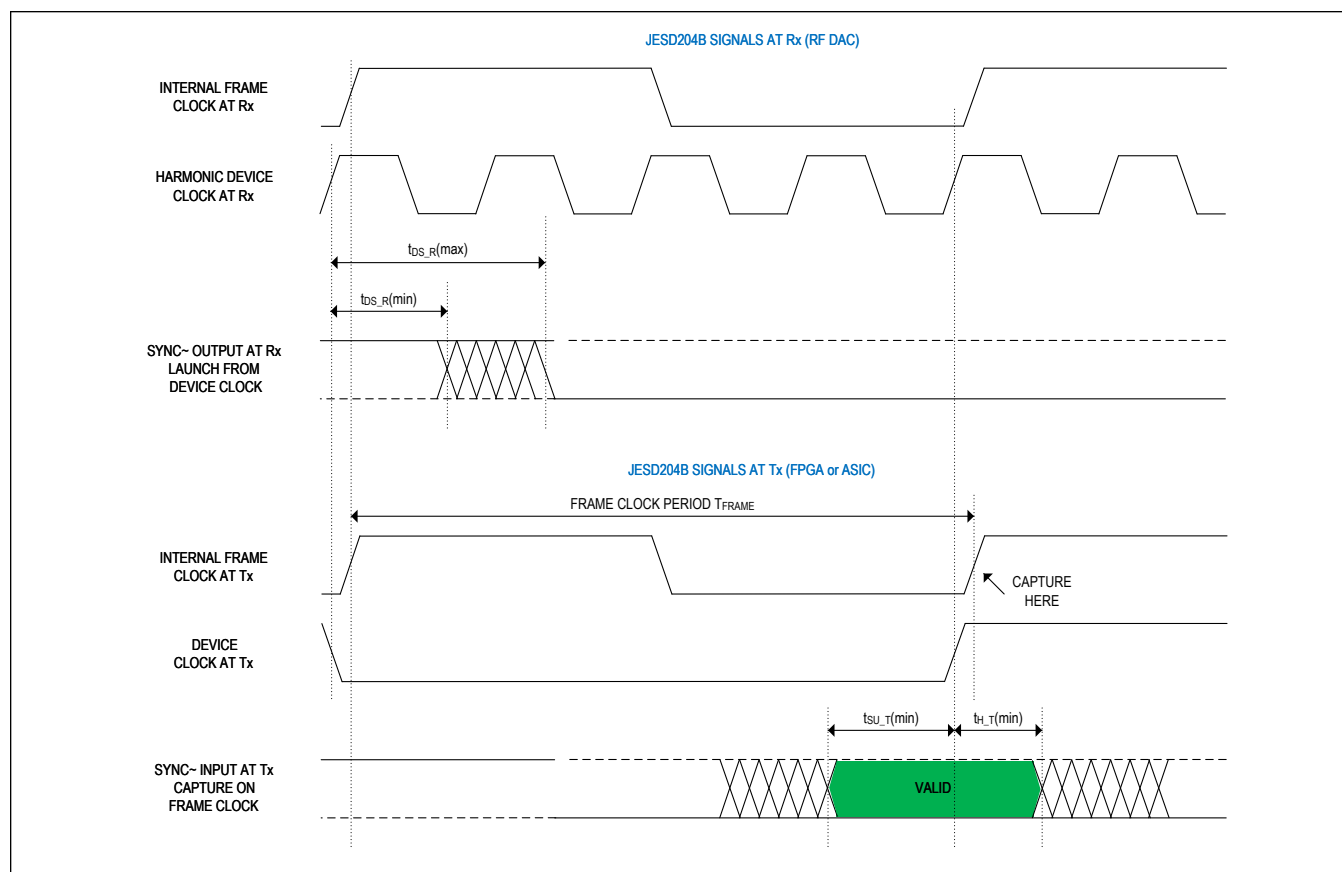


Figure 10. Interface Timing for Subclass-0

## Serial Control Interface

The serial control interface is comprised of the CSB, SCLK, SDI, and SDO pins that support a typical 4-wire SPI interface. It also supports a 3-wire SPI interface, where the SDI pin acts as both digital data input and output, commonly referred to as SDIO.

The MAX5855 is always a slave device with the master controlling CSB, SCLK, and SDI. The SPI clock frequency must meet certain constraints for proper operation and response from the MAX5855. See [SPI to PCLK Frequency Ratio](#) section.

In 4-wire SPI interface mode, CSB, SCLK, and SDI are 1.8V CMOS-level digital input pins. SDO is a 1.8V CMOS output signal when the MAX5855 is transmitting serial data. SDO is a high impedance output at all other times. CSB is the chip-select pin. While CSB is low, the MAX5855 device is open to communication through the SCLK, SDI, and SDO pins. Each communication cycle is comprised of a single read/write bit, a 15-bit address word, and an 8-bit data word. The serial interface clock, SCLK, latches data into the MAX5855 on the rising edge and clocks data out of the MAX5855 on the falling edge. A logic '1' for the R/W bit signifies a read operation and a logic '0' indicates a write operation.

The R/W bit and the address word are sent to the device through the SDI pin. The R/W bit is transmitted first, followed by the address word in MSB to LSB order while in the default MSB-first format. In the LSB-first format, the address word is transmitted first, LSB to MSB, followed by the R/W bit. Input or output data are transmitted MSB or LSB-first order, based on the format setting. Further descriptions assume MSB-first format.

For a write operation, a data word is immediately written to the SDI after the last bit of the address. For a read operation, the data word is transmitted from the MAX5855 on the SDO signal line. The transmission starts on the falling edge of SCLK immediately after the last bit is latched into the device. The SDO driver enters a high-impedance state on the next

falling SCLK edge immediately after the bit is transmitted. CSB must toggle from low to high and then back to low before another communication cycle can resume. An exception is burst mode operation.

When burst mode is enabled, a continued assertion of CSB after the data word will auto decrement/increment the address word depending on the configuration for a successive read/write. Every 8 cycles of SCLK will access a successive address for either write or a read based on the R/W bit in the initial command.

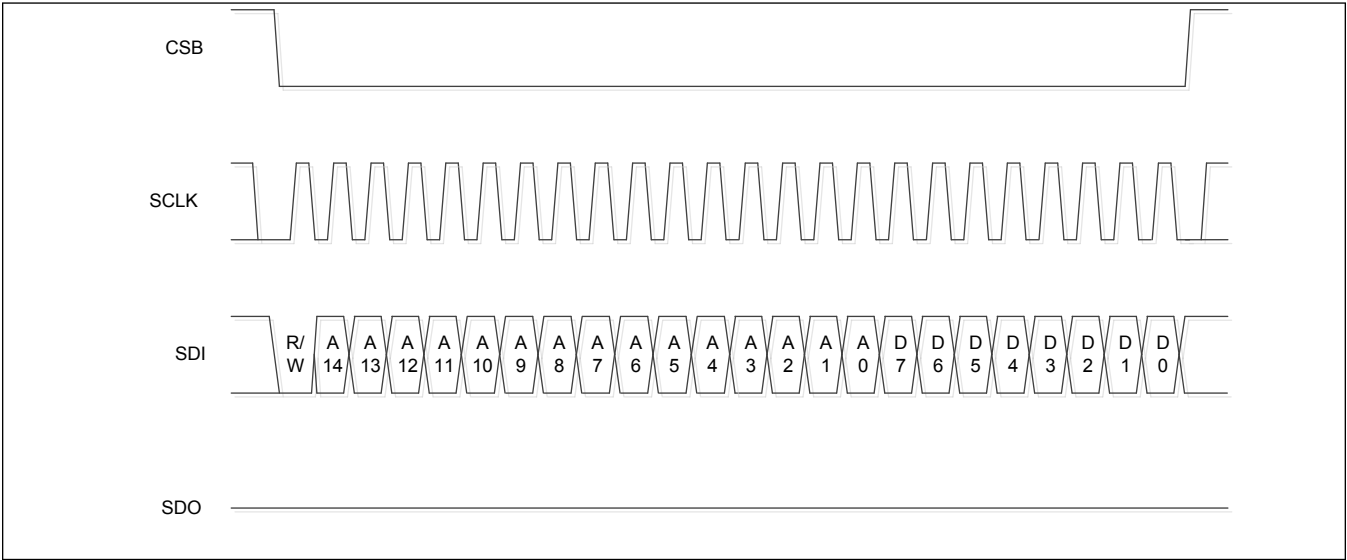


Figure 11. SPI Single Write with MSB-First Format

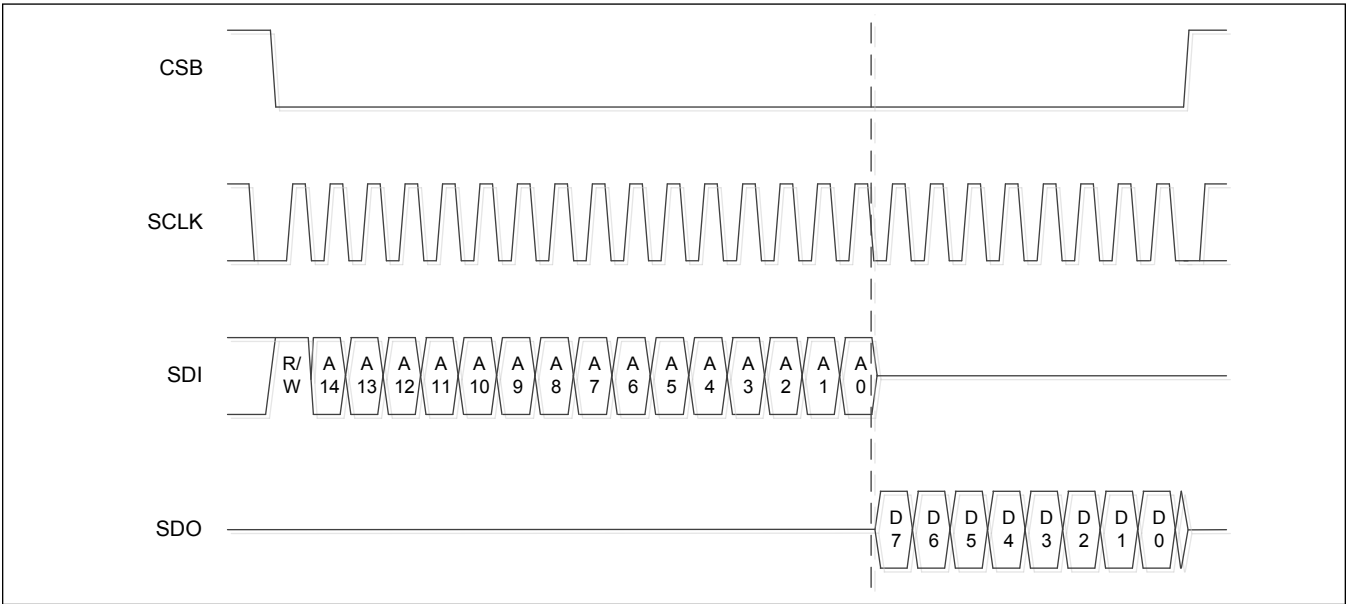


Figure 12. SPI Single Read with MSB-First Format

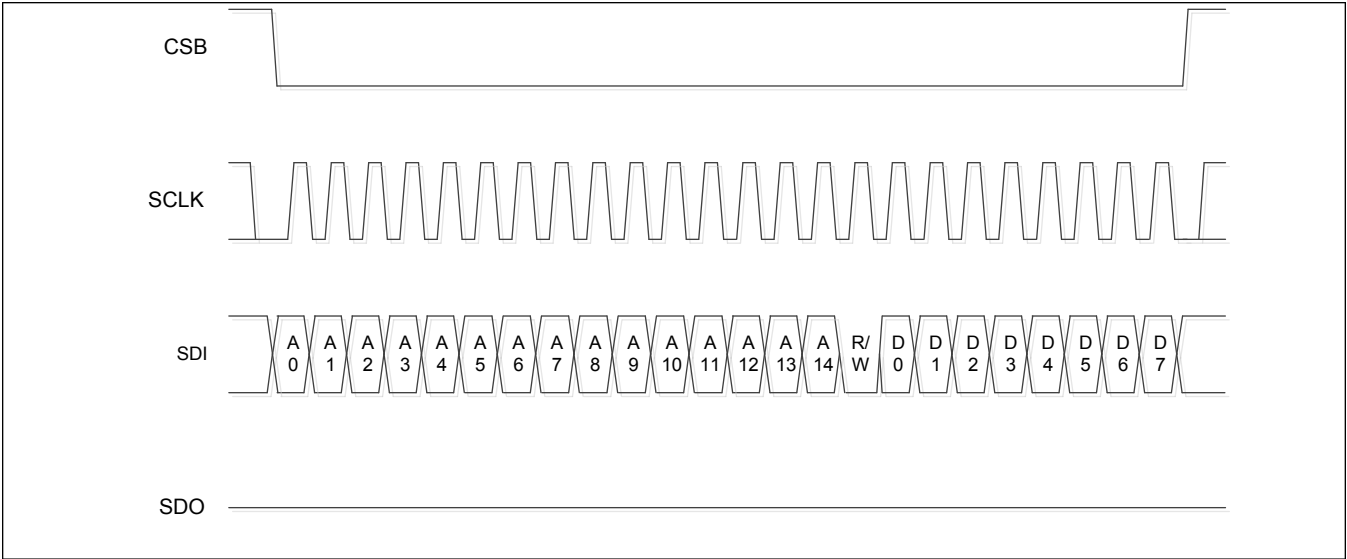


Figure 13. SPI Single Write with LSB-First Format

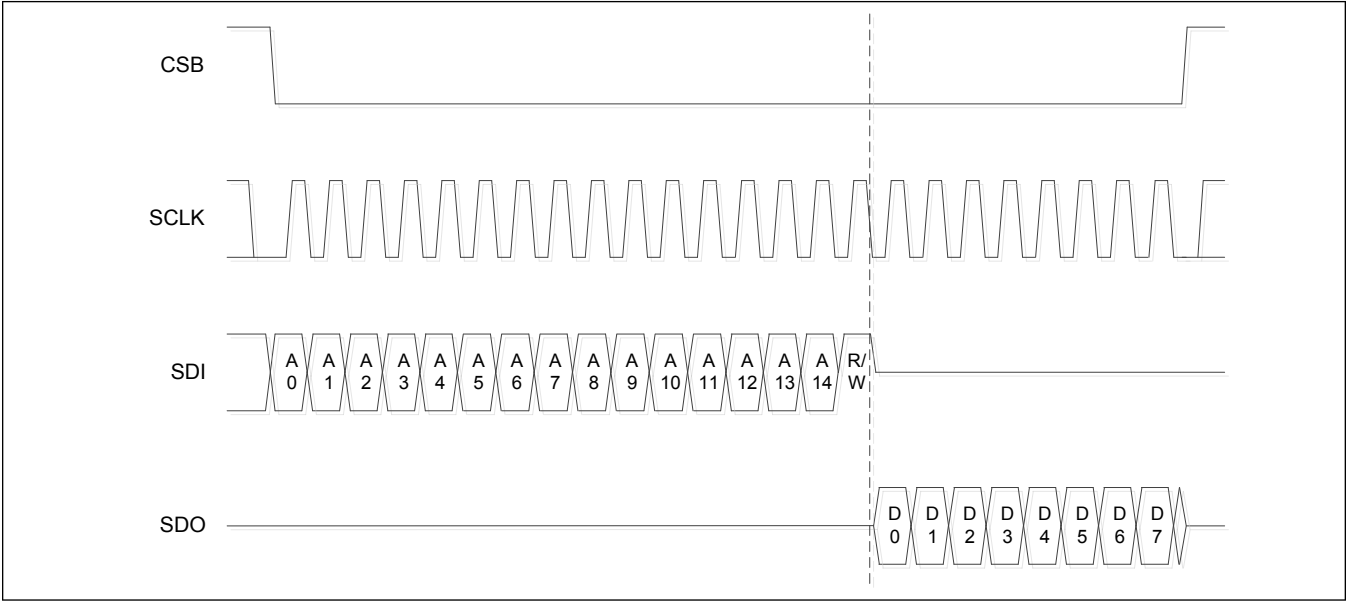


Figure 14. SPI Single Read with LSB-First Format

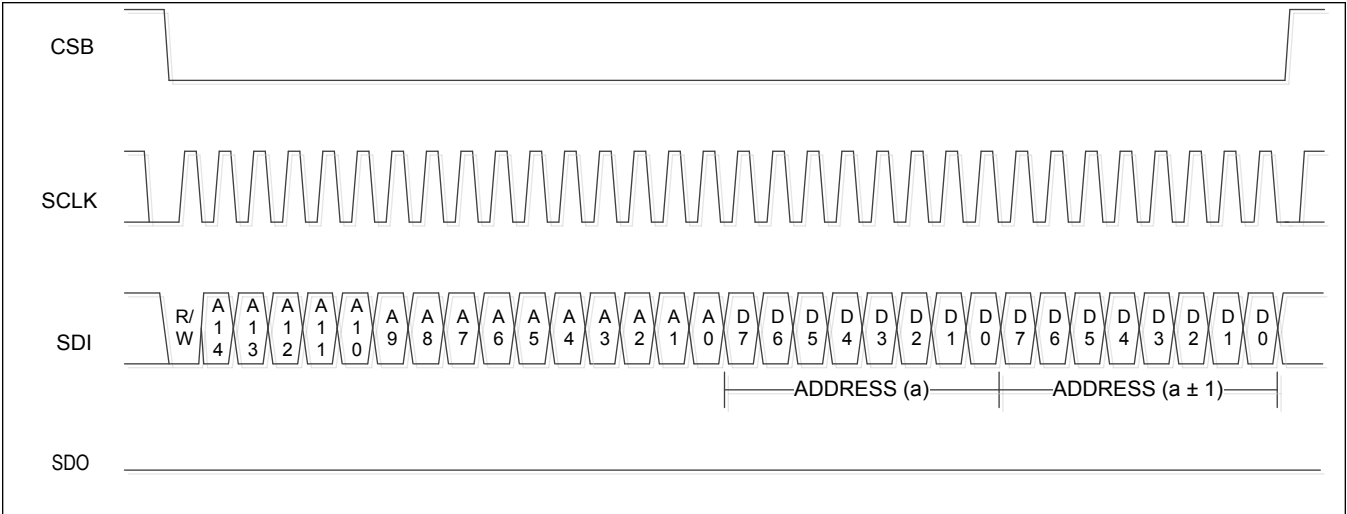


Figure 15. SPI Burst Write with MSB-First Format

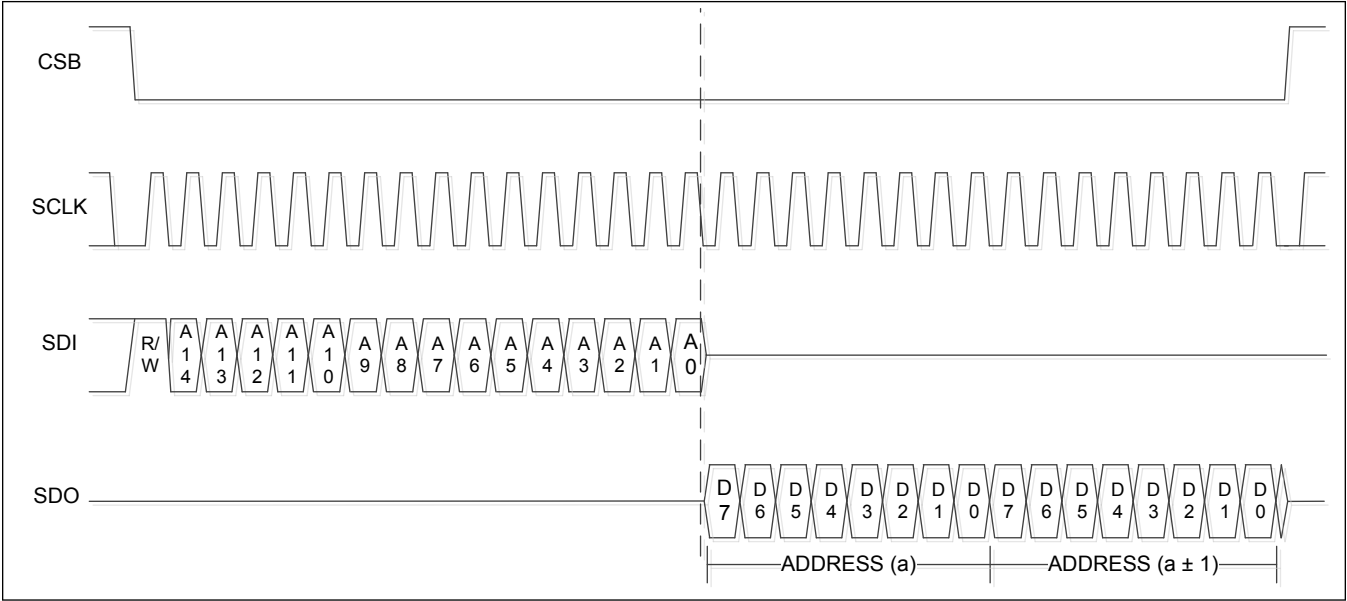


Figure 16. SPI Burst Read with MSB-First Format

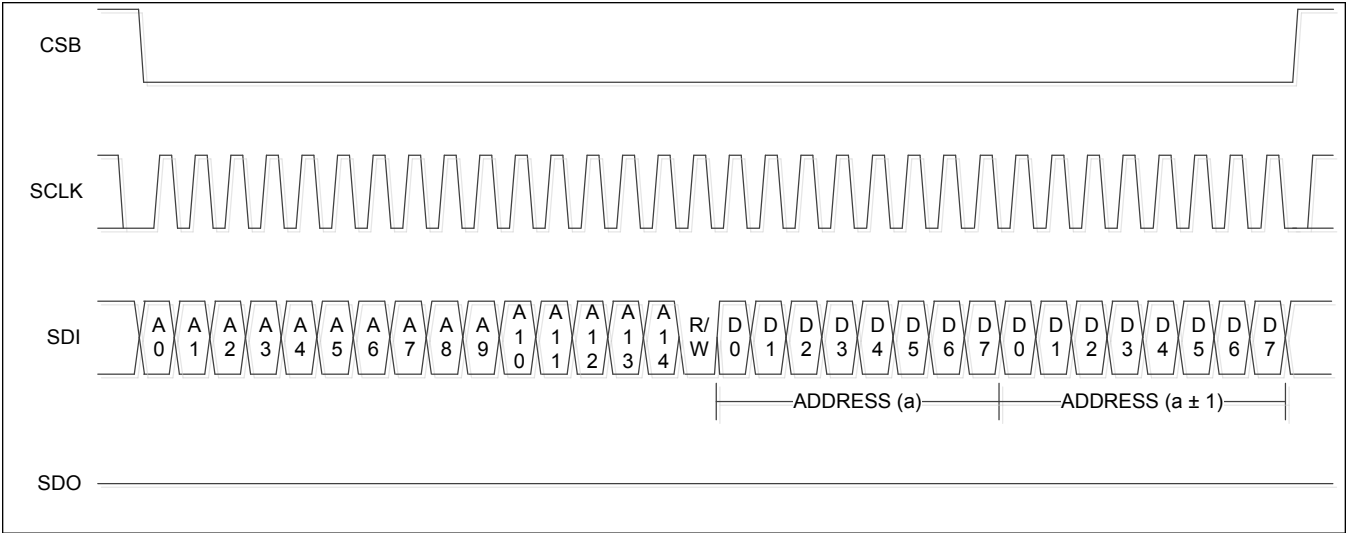


Figure 17. SPI Burst Write with LSB-First Format

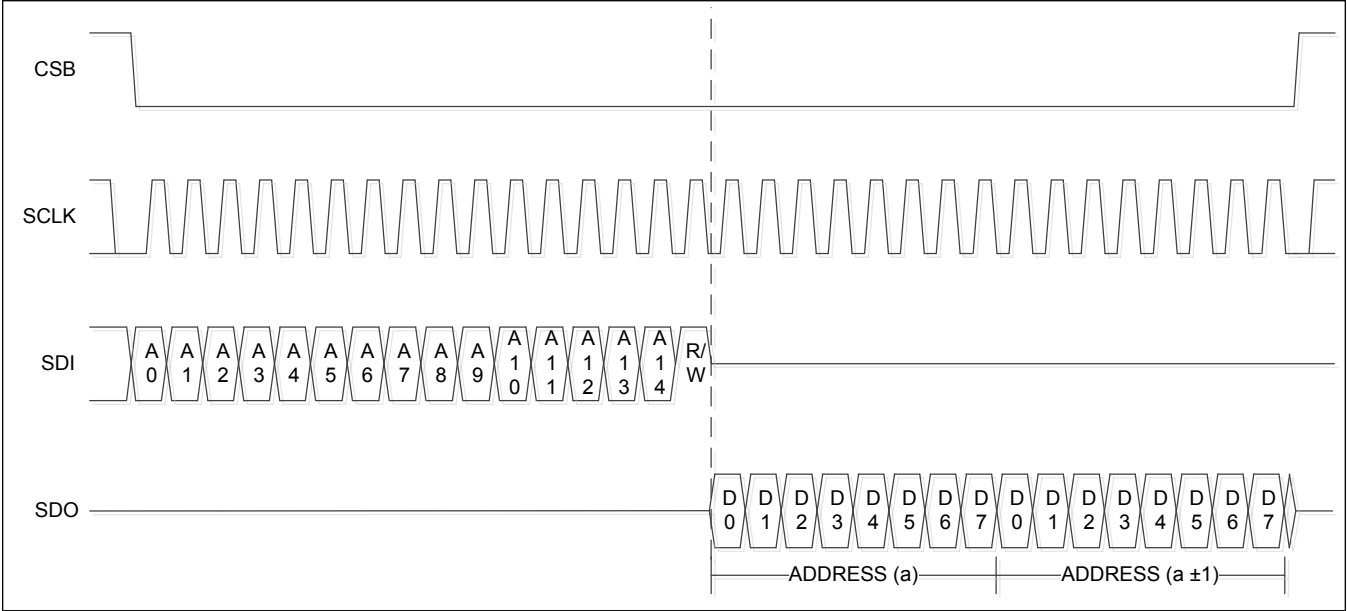


Figure 18. SPI Burst Read with LSB-First Format

Interrupt Control

The INTB pin is a 1.8V CMOS logic output that signals an interrupt condition when in a low state. The interrupt system is comprised of a status register and an interrupt mask register. The interrupt signal is an 8-input logic NOR of the EINT register bit-wise ANDed with the DSP status register. The interrupt tree for the device is shown in [Figure 19](#). The JESD204B interface has its own second level of interrupt registers and interrupt mask registers as defined in the register map. The interrupt masks and registers can be modified through the serial interface. [Table 3](#) shows all the status register bits that can be enabled to generate an interrupt.

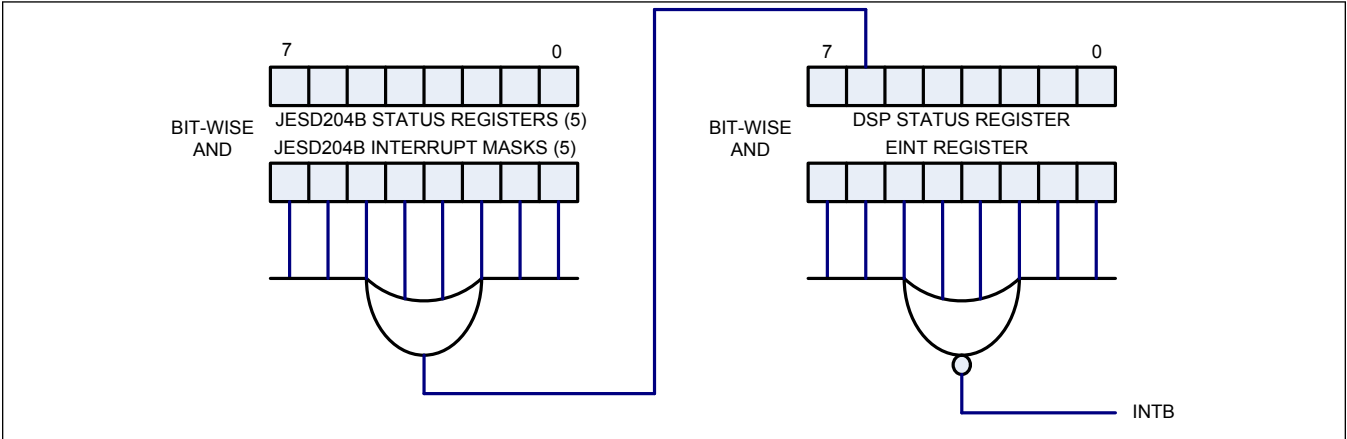


Figure 19. Interrupt Tree

Table 3. Status Register Bits

| DSP Status Register (1st Level Interrupt)       |                                                                                          |
|-------------------------------------------------|------------------------------------------------------------------------------------------|
| BANK.REGISTER.BIT                               | FUNCTION                                                                                 |
| DSP.STATUS.JSDIM                                | Real-time, DAC mute from JESD LINK Layer is active                                       |
| DSP.STATUS.JSDII                                | Real-time, interrupt from JESD LINK Layer is active                                      |
| DSP.STATUS.TRDY                                 | Latched, internal trim load is complete and the SPI bus is unblocked for external access |
| DSP.STATUS.PLLck                                | Latched, DAC PLL was <b>unlocked</b> .                                                   |
| JESD204B Status Registers (2nd Level Interrupt) |                                                                                          |
| BANK.REGISTER.BIT                               | FUNCTION                                                                                 |
| RLaneRegs0-4.StatRlane.FrNSync                  | Real-time, Frame synchronization state machine is not synchronized on Lane N             |
| RLaneRegs0-4.StatRlane.LnReAlign                | Latched, lane realignment occurred on Lane N                                             |
| RLaneRegs0-4.StatRlane.FrReAlign                | Latched, frame realignment occurred on Lane N                                            |
| RLaneRegs0-4.StatRlane.DISP                     | Latched, Disparity error detected on Lane N                                              |
| RLaneRegs0-4.StatRlane.NIT                      | Latched, NIT error detected on Lane N                                                    |
| RLaneRegs0-4.StatRlane.CGS                      | Latched, Code Group Synchronization state-machine was not synchronized on Lane N         |
| RLaneRegs0-4.StatRlane.FIFOempty                | Latched, FIFO empty on Lane N                                                            |
| RLaneRegs0-4.StatRlane.FIFOfull                 | Latched, FIFO full on Lane N                                                             |
| RLaneRegs0-4.StatRlane.PRBSerr                  | Latched, PHY interface PRBS monitor detected an error on Lane N                          |
| RLaneRegs0-4.StatRlane.KContErr                 | Latched, non-/K/ character detected on Lane N                                            |

Table 3. Status Register Bits (continued)

|                                  |                                                                                                                |
|----------------------------------|----------------------------------------------------------------------------------------------------------------|
| RLaneRegs0-4.StatRIane.FChkErr   | Latched, ILA sequence FCHK error detected on Lane N                                                            |
| RLaneRegs0-4.StatRIane.LCfgrErr  | Latched, ILA sequence lane configuration error detected on Lane N                                              |
| RLaneRegs0-4.StatRIane.ILAerr    | Latched, ILA sequence decode (/R/, /Q/, /A/ character) error detected on Lane N                                |
| RLinkRegs.StatRlinkILA.ILAnsnc   | Real-time, ILA synchronization not achieved                                                                    |
| RLinkRegs.StatRlinkILA.ILAfaiure | Latched, ILA failed, indicates that at least one FIFO in a JESD lane overflowed before the FIFO reads started. |
| RLinkRegs.StatRlinkPRBS.PRBSerr1 | Latched, Converter 2 (Q-sample) PRBS error detected                                                            |
| RLinkRegs.StatRlinkPRBS.PRBSerr0 | Latched, Converter 1 (I-sample) PRBS error detected                                                            |
| RLinkRegs.StatRlinkSTP.STPerr1   | Latched, Converter 2 (Q-sample) short test pattern error detected                                              |
| RLinkRegs.StatRlinkSTP.STPerr0   | Latched, Converter 1 (I-sample) short test pattern error detected                                              |

Digital Control Pins

The MAX5855 contains two 1.8V CMOS logic input control pins: RESETB and MUTE. The device is placed in a reset state when RESETB is logic-low. On power-up, RESETB should remain low until all supply voltages have stabilized and an external clock is applied to CLKP/CLKN.

The MUTE pin and the register-based MUTE control when the device enters the mute mode. In mute mode, the DAC digital input is set to mid-scale. A logic-high on the MUTE pin will place the device into mute mode while a logic-low may allow normal operation. The main purpose of MUTE pin is to eliminate any transmit power during the receive time of a TDMA system while the purpose of the MUTE bit is to protect the system PA during startup or error conditions. The register-based mute can be configured through the serial interface enabling the mute mode internally regardless of the state of the MUTE pin. Similar to the interrupt mask registers, there are mute enable registers which generate the internal mute signal under defined conditions. Table 3 shows all the status register bits that can be used to generate the internal mute. The states of all registers in the device are preserved while the RF DAC output is muted.

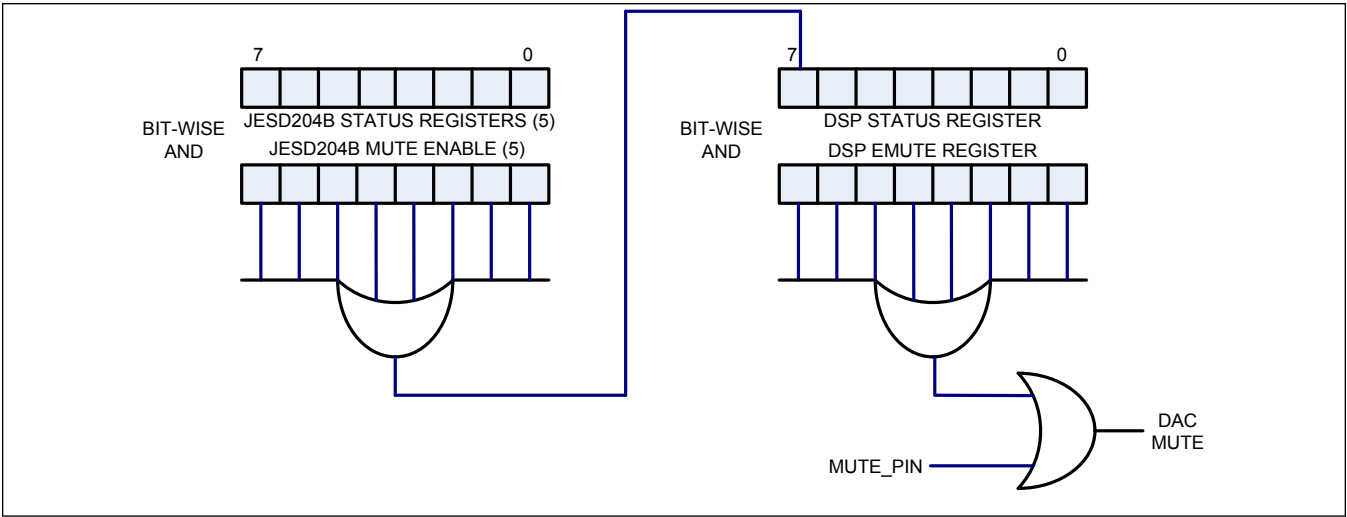


Figure 20. Mute Generation Logic

## Frequency Planning

Using a DAC to generate RF transmission signals requires consideration of aliased harmonics and internally generated divided clocks. To ensure the dominant second (HD2) and third order (HD3) harmonics do not fold back into the signal band, the DAC update rate needs to be greater than four times the highest frequency in the band of interest.

Figure 21a and Figure 21b show the location of the 2nd and 3rd harmonic distortion products for the case of the DAC being updated at 2 times and 4 times the maximum desired frequency in the band of interest (DOCSIS 3.1 example shown).

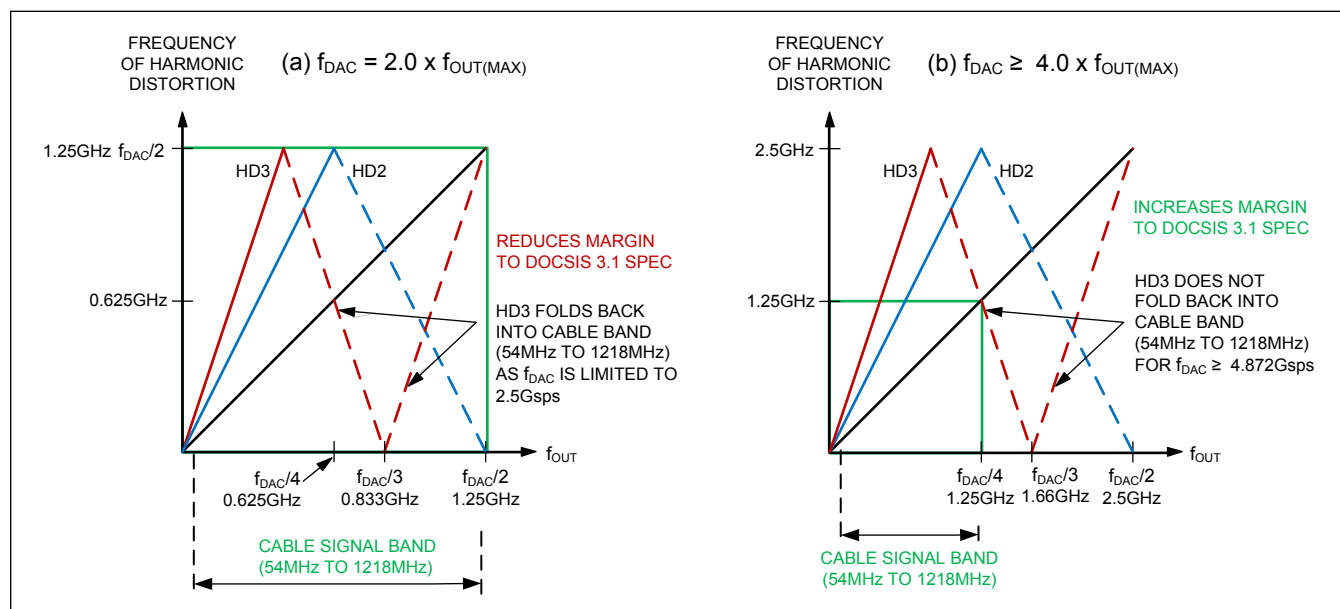


Figure 21. Effect of DAC Update Rate on Folded HD2 and HD3

### Quadrature Modulator and NCO

The device includes a quadrature modulator (Figure 22) that produces an image rejected Real output of the Complex input I-data and Q-data, utilizing a complex numerically controlled oscillator (NCO).

The complex NCO employs a 33-bit phase accumulator to provide a RF signal frequency programmable from DC (0Hz) up to  $f_{DAC}/2$ . The user needs to calculate and program the following three parameters for proper configuration of the NCO: the Frequency Control Word (FCW), the Numerator Frequency Word (NFW), and the Denominator Frequency Word (DFW).

$$FCW_{full} = \frac{2^{33} \times f_{NCO}}{f_{DAC}} \quad (1)$$

Where  $FCW_{full}$  is the real, floating point, or integer + fractional value of the Frequency Control Word,  $f_{DAC}$  is the DAC Sample Rate and  $f_{NCO}$  is the target output center frequency of the NCO.

The full FCW is made up of the characteristic or Integer part of the quotient and the fractional remainder or mantissa portion of  $FCW_{full}$ :

$$FCW_{full} = FCW + \frac{NFW}{DFW} \quad (2)$$

Where FCW is represented by a 32-bit word, NFW is the Numerator Frequency Word represented by an 18-bit word and the DFW is the Denominator Frequency Word represented with a 19-bit word.

The characteristic or integer part of  $FCW_{full}$  is the NCO's primary Frequency Control Word. The remainder or mantissa of the  $FCW_{full}$  quotient is converted into two rational integer numbers by removing the common integer multiplication factor. This can be accomplished through brute-force means to find a numerator less than the decimal value of 262144 ( $2^{18} - 1$  or smaller) and a denominator less than 524288 ( $2^{19} - 1$  or smaller). The easiest way to calculate this fraction would be to round the decimal remainder to 5 digits and divide by 100,000. Simplifying the fraction will result in valid programmable values for NFW and DFW.

$$FCW = \text{int}(FCW_{full}) \quad (3)$$

$$\frac{NFW}{DFW} = \text{rem}(FCW_{full}) \quad (4)$$

When setting DFW to 100,000 and rounding the decimal remainder to 5 digits the mantissa can be accurately represented as a ratio of two numbers: NFW and DFW.

To determine the programming precision of the NCO based on the least-significant bit (LSB) size of the NCO, use the following equation:

$$FCW_{1Hz} = \frac{2^{33}}{f_{DAC}} \quad (5)$$

Where  $FCW_{1Hz}$  is the LSBs required (whole and fractional) to adjust the NCO frequency by a 1Hz step.

$$f_{NCO/LSB} = \frac{1}{FCW_{1Hz}} = \frac{f_{DAC}}{2^{33}} \quad (6)$$

Where  $f_{NCO/LSB}$  is the frequency change to the NCO ( $f_{NCO}$ ) given a single, whole LSB step of the NCO control word.

This  $f_{NCO/LSB}$  value essentially shows the precision of the NCO with the largest step size being about 0.7Hz per LSB change in the NCO control word. Using the fractional portion of the FCW will result in precision adjustments as small as 2.7μHz.

#### Example 1

Use the following system values to calculate the FCW, NFW, and DFW:

$f_{DAC} = 4915.2\text{MHz}$ , and  $f_{NCO} = 575\text{MHz}$

Starting with equation (1):

$$FCW_{full} = \frac{2^{33} \times f_{NCO}}{f_{DAC}} = \frac{2^{33} \times 575M}{4915.2M}$$

$$FCW_{full} = 1004885333.\bar{3}...$$

Using equations (3) and (4):

$$FCW = \text{int}(1004885333.3333) = 1004885333$$

$$\frac{NFW}{DFW} = \text{rem}(1004885333.3333) = 0.33333$$

$$\frac{NFW}{DFW} = \frac{33333}{100000} \approx \frac{205}{615}$$

$$NFW = 205, \quad DFW = 615$$

Equation (1) can be used in reverse to find an NCO frequency based off of an integer multiple of FCW (where the fractional portion does not require programming):

$$f_{NCO} = \frac{f_{DAC} \times FCW}{2^{33}} = \frac{4915.2M \times 1004885333}{2^{33}}$$

$$f_{NCO} = 574.999999809\text{MHz}$$

The above result confirms that the target NCO frequency is produced to a sub-1Hz precision.

Calculating the  $f_{NCO}/\text{LSB}$  using equation (6):

$$f_{NCO}/\text{LSB} = \frac{f_{DAC}}{2^{33}} = \frac{4915.2M}{2^{33}} = 0.5722\text{Hz/LSB}$$

Thus, without using the fractional NCO words, the NCO can be adjusted to a resolution of better than 0.6Hz and in this example, set to a precise value within 0.191Hz of the target frequency.

### Example 2

Use the following system values:

$$f_{DAC} = 4915.20\text{MHz}, \text{ and } f_{NCO} = 573\text{MHz}$$

Using equation (1):

$$FCW_{full} = \frac{2^{33} \times f_{NCO}}{f_{DAC}} = \frac{2^{33} \times 573M}{4915.20M}$$

$$FCW_{full} = 1001390080.00000$$

Using equations (3) and (4):

$$FCW = \text{int}(100390080.00000) = 1001390080$$

$$\frac{NFW}{DFW} = \text{rem}(1001390080.00000) = 0.00000$$

$$NFW = 0, \quad DFW = 0$$

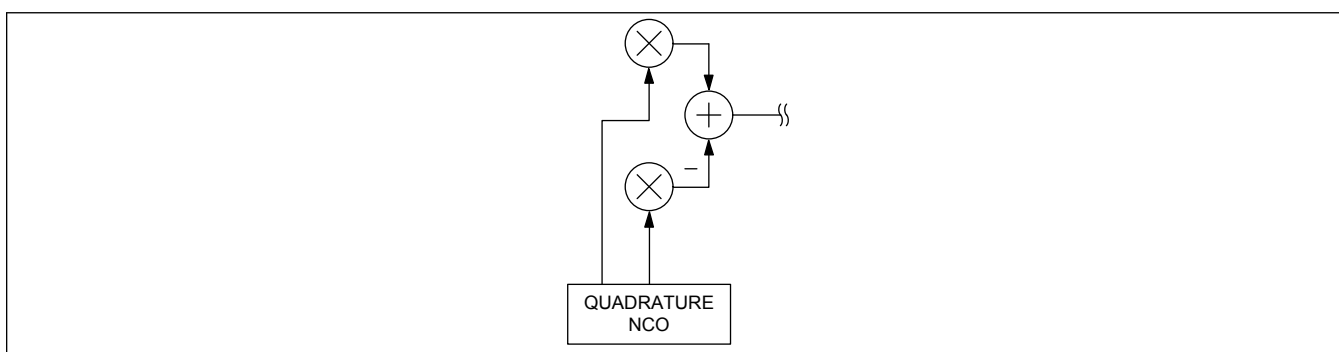


Figure 22. Complex NCO and Modulator

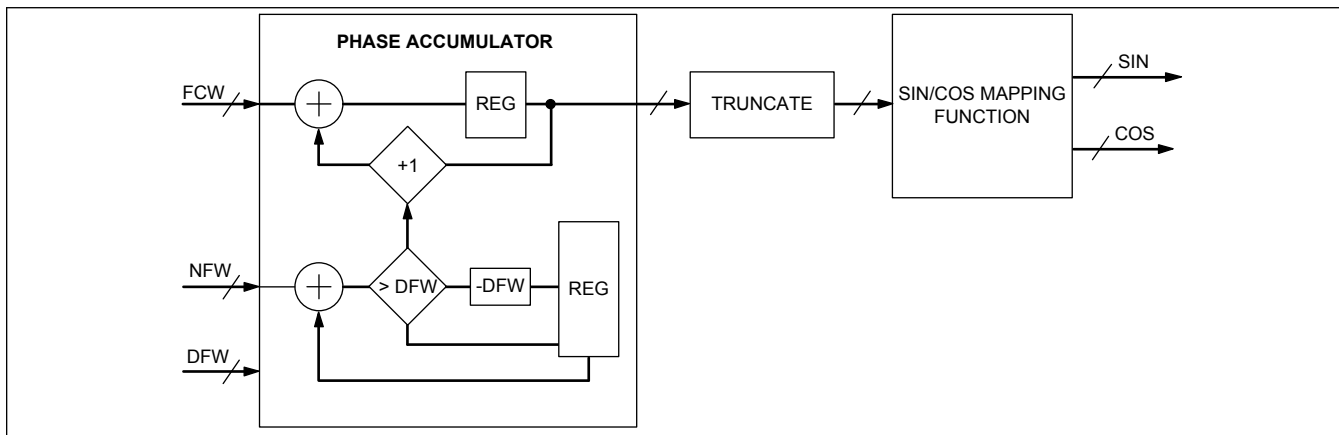


Figure 23. NCO Block Diagram

The following is example Matlab code for calculating NCO values. When calculating FCW, NFW, and DFW, use long format types for more precise results.

```
% Find out MAX5855 NCO values
format long
```

```
% Define DAC clock frequency
FDAC = 4915.2e6 x M
```

```
% Define desired NCO frequency
```

```
FNCO = 1796.769375e6;
```

```
FCWfull = 233 × FNCO/FDAC;
```

```
% Calculate FCW, NFW and DFW
```

```
FCW = floor(FCWfull)
```

```
rats(FCWfull-FCW)
```

```
% END
```

## Analog Interface

### Reference Interface

The device operates with either the on-chip 1.2V bandgap reference or an external reference voltage source as shown in [[Setting the DAC Output Full-scale Using an (a) Internal or (b) External Reference Voltage]]a and [[Setting the DAC Output Full-scale Using an (a) Internal or (b) External Reference Voltage]]b. REFIO serves as the input for an external, low-impedance reference source, or as the reference output when the internal reference is used. REFIO must be decoupled to DACREF with a 1μF capacitor when using the internal reference. REFIO must be buffered with an external amplifier if heavier loading is required, due to the 10kΩ series resistance.

The reference circuit employs a control amplifier designed to regulate the full-scale, differential output current, I<sub>OUTFS</sub>. The output current is calculated as follows:

$$I_{OUTFS} = 32 \times I_{REF} \quad (7)$$

$$I_{REF} = \frac{V_{REFIO}}{R_{SET}} \quad (8)$$

Where I<sub>REF</sub> is the reference output current and I<sub>OUTFS</sub> is the full-scale output current of the DAC.

In general, the dynamic performance of the DAC improves with increasing full-scale current. Using the 1.2V (typ) internal reference and R<sub>SET</sub> of 960Ω results in the maximum full-scale output current of 40mA.

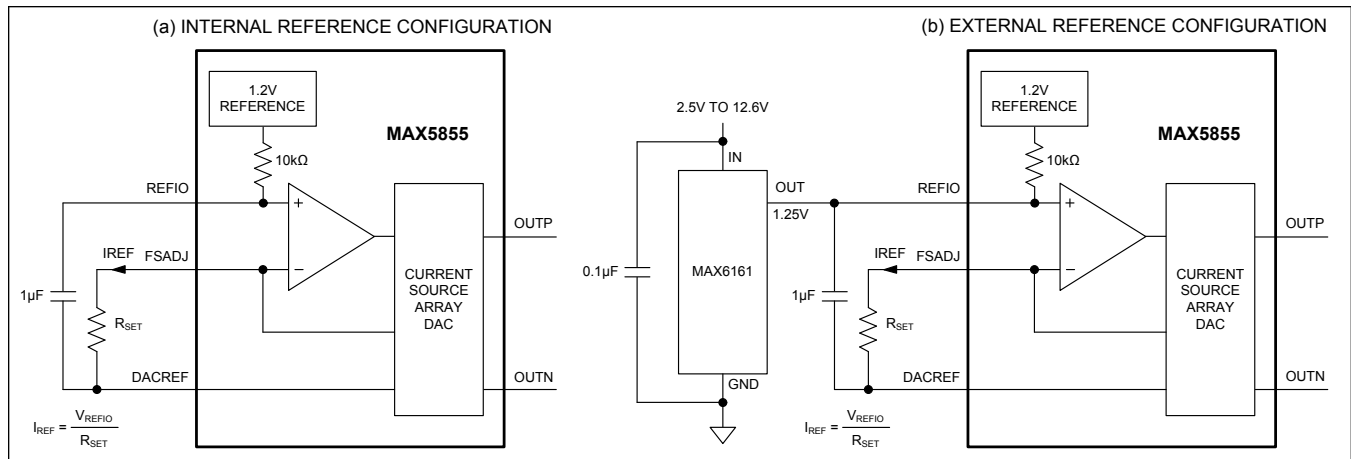


Figure 24. Setting the DAC Output Full-Scale Using an (a) Internal or (b) External Reference Voltage

### Analog Output

The device is a differential current-steering DAC with built-in output termination resistors. The outputs are terminated to AVDD2 providing a 50Ω differential output resistance. In addition to the signal current, a constant current sink ( $I_{FIX}$ ) equal to one half  $I_{OUTFS}$  is connected to each differential DAC output. [Figure 25](#) shows an equivalent circuit for the internal output structure of the device. The circuit has some resistive, capacitive, and inductive elements. These elements have been minimized in order to achieve the highest possible output bandwidth (2GHz, typical).

In addition, the device requires a differential external termination (i.e., double termination). This external termination can be accomplished with a differential 50Ω load or a single-ended 50Ω load interfaced through a transformer. RF chokes to the AVDD2 supply should be used with the transformer coupled output. A typical transformer coupled configuration for high-frequency operation is shown in [Figure 25](#).

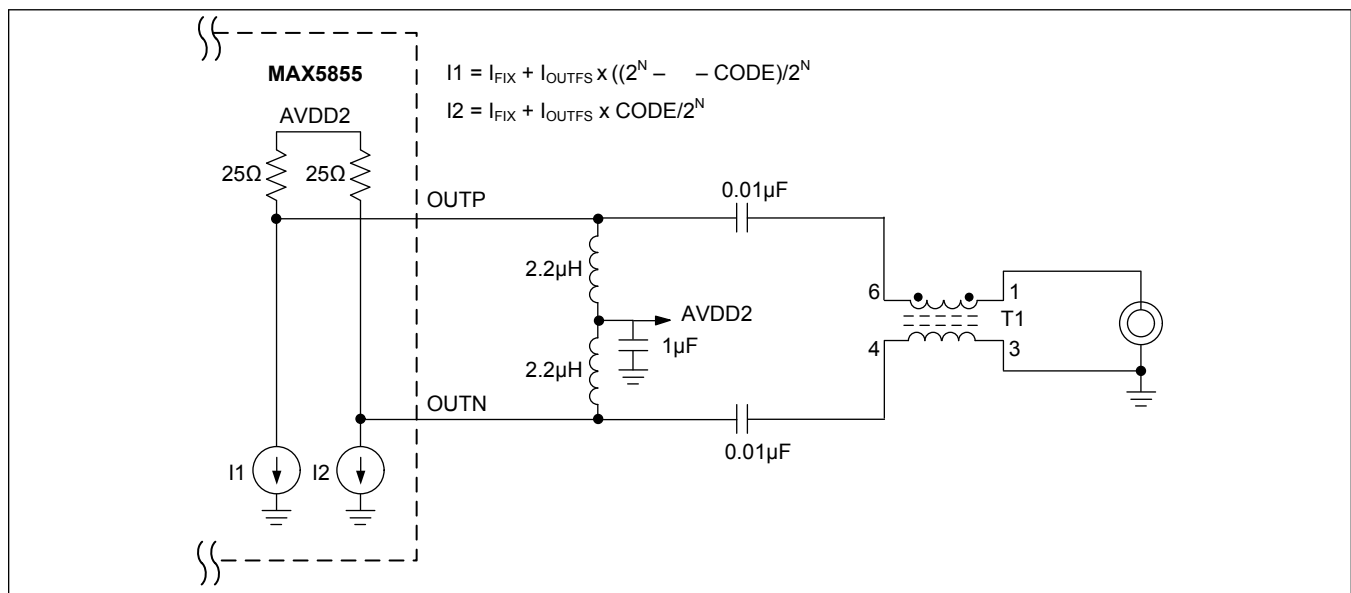


Figure 25. Typical DAC Output Configuration

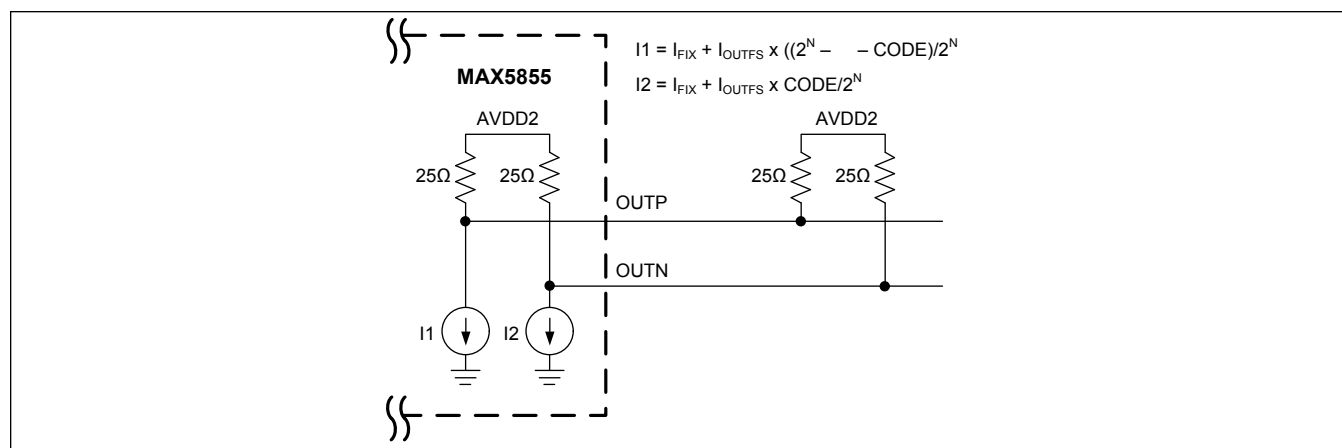


Figure 26. Output Configuration for Low-Frequency Operation

For applications where the DC information is important, the output configuration in [Figure 26](#) can be used. 25Ω resistors to AVDD2 are required for DC coupling. The DC configuration will lower the output common-mode voltage which may reduce performance slightly. The output termination along with the full-scale current must maintain a voltage swing within the Output Compliance range of the device (as specified in the [Electrical Characteristics](#) table).

### Clock Interface

The DAC contains a differential high-frequency clock input, CLKP/CLKN, and an internal clock multiplying PLL to ease clock distribution. The DAC is updated on the rising edge of CLKP/CLKN at a frequency of 4915.2MHz. See the [DAC Clock PLL](#) section for operation with the PLL.

The high-frequency clock should be a balanced, fully differential signal with a 50%, or near-50% duty cycle. The clock input has internal (on-chip) 100Ω differential termination. The clock requires a minimum input power of 0dBm. The clock inputs must be AC-coupled to the source as they are internally self-biased.

### Clock Subsystem

#### Overview

The MAX5855 clock subsystem is outlined in [Figure 27](#). The differential DAC input clock CLKP/N is received through a differential clock interface buffer.

From the clock buffer output, the signal is used as a reference for the on-chip DAC PLL.

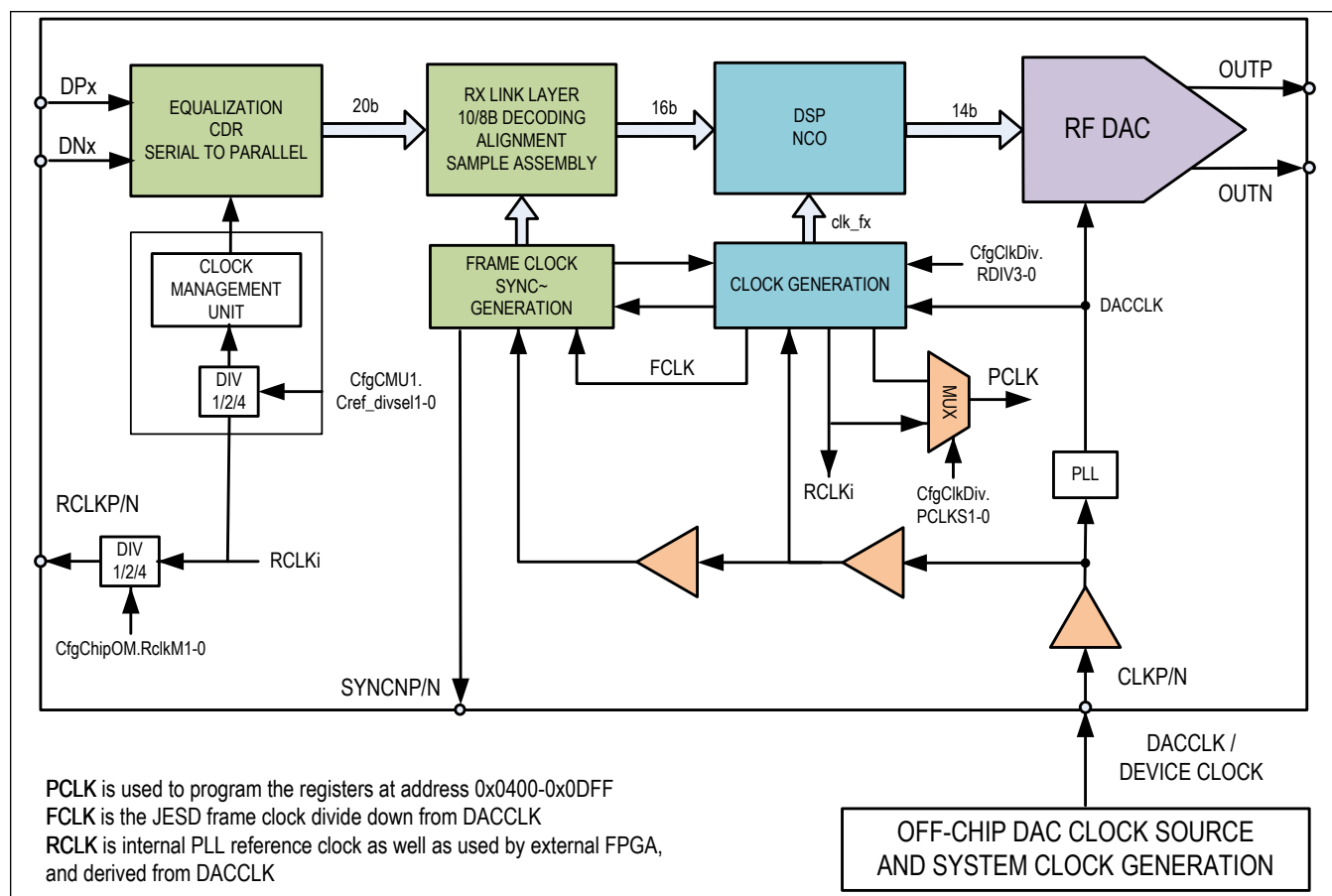


Figure 27. MAX5855 Clock Subsystem

The DAC output signal phase noise and jitter will mostly be determined by the on-chip PLL performance. The reference clock phase noise will dominate within the 100kHz PLL loop bandwidth. In that frequency range the input clock phase noise will be amplified by  $20 \times \log(F_{DAC}/F_{REF})$ .

### DAC Clock PLL

The MAX5855 differential high-frequency clock input (CLKP/CLKN) accepts an external reference clock signal that is multiplied internally by a phase-locked-loop (PLL). The PLL includes user-programmable multiplication factors which provide flexibility in the reference clock selection. Figure 28 shows the functional block diagram of the PLL.

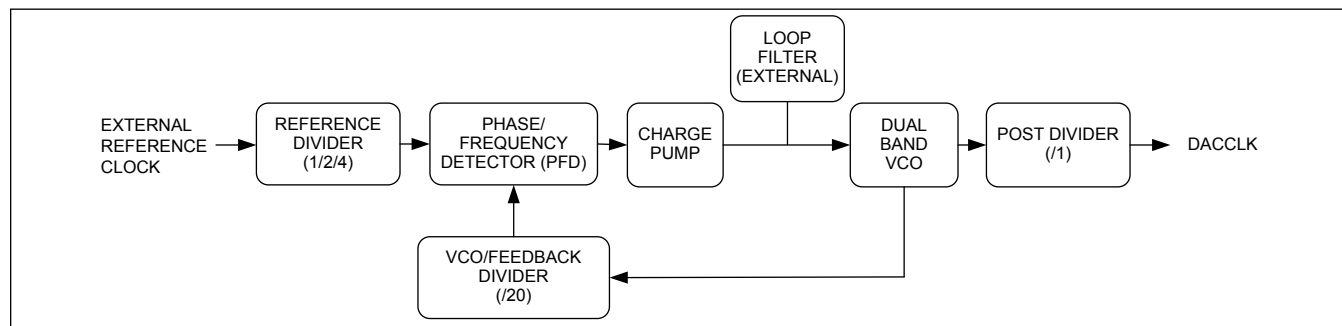


Figure 28. DAC Clock PLL Functional Block Diagram

The reference input signal is divided by 1, 2, or 4 under user control before being applied to the phase/frequency detector (PFD). The VCO output is divided by a programmable divide-by 20 before it is fed back to the PFD.

### VCO Band Select

The VCO has a frequency range that supports 4.9152GHz operation. The combination of reference frequency, reference divide and feedback divide values, and VCO band select must be chosen to operate the VCO within its allowed frequency range.

### Lock Detect

The DAC clock PLL includes a lock detect indicator which can be read out of the SPI status register (DSP.StatPLL0). Bit PLL\_LOCK is set high when the PLL is locked and low when the PLL is unlocked.

### PLL External Components

The DAC clock PLL requires external loop filter components. [Figure 29](#) shows the schematic for the loop filter. The loop filter components should be placed as close as possible to the MAX5855 to avoid noise coupling into the circuit. In addition to the loop filter, there is a bypass capacitor that must be placed very close to the MAX5855. The C1 nF and C2 pF capacitor values strongly depends on system PCB design and are unique for most designs (see [Applications Guidelines](#)).

The user may wish to select different operating conditions for the PLL loop filter than those specified. The following values may be useful for calculating new compensation component values:

VCO Gain:  $K_{VCO} = 115\text{MHz/V}$

Charge Pump Current:  $I_{CP} = 480\mu\text{A}$

PLL Feedback Divider Setting:  $N = \langle \text{CfgPLL2.DVAL}[3:2] \text{ and } \text{CfgPLL1.DVAL}[1:0] \rangle$

Internal Smoothing Capacitance:  $C_S = 43\text{pF}$

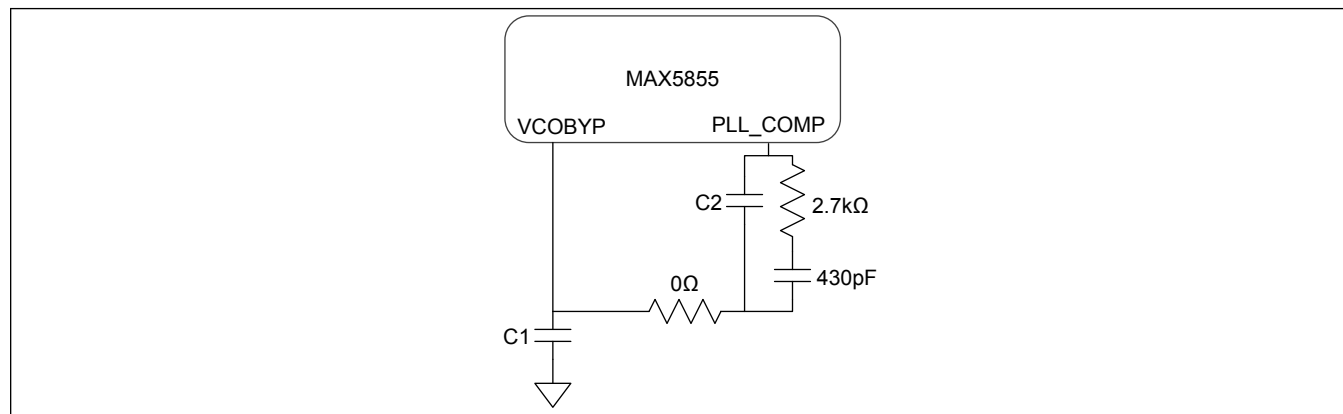


Figure 29. DAC Clock PLL External Components

### RCLK Description and Use

The MAX5855 outputs a divided reference clock RCLK (RCLKP/RCLKN) that is equal to the DAC clock frequency divided by a factor (Defined by programming the register bits DSP.CfgClkDiv.RDIV) to ensure synchronization with the system clock. Caution must be exercised when programming the DSP.CfgClkDiv.RDIV register due to its performance impact on other internal blocks. See [Frequency Settings and Configuration](#) section for more details.

The output clock RCLKP/RCLKN frequency can be further lowered by programming the control bits in the DSP.CfgChipOM.RclkM register.

**Interpolation Filters**

The MAX5855 has powerful digital signal process capability with its built-in digital interpolation filters with an interpolation ratio of 4x (complex path). [Table 4](#) shows the digital filter coefficients of 4x (F1 2x, F2 2x cascaded) interpolation ratios.

**Table 4. Digital Filter Coefficients**

| TAP                                                                                           | F1 2x (COMPLEX PATH) | F2 2x (COMPLEX PATH) |
|-----------------------------------------------------------------------------------------------|----------------------|----------------------|
| 1                                                                                             | 0.00004577636718750  | 0.00138854980468750  |
| 2, 4, 6, 8, 12, 14, 16, 18                                                                    | 0                    | 0                    |
| 3                                                                                             | -0.00015258789062500 | -0.01086425781250000 |
| 5                                                                                             | 0.00039672851562500  | 0.04589843750000000  |
| 7                                                                                             | -0.00083923339843750 | -0.14880371093750000 |
| 9                                                                                             | 0.00161743164062500  | 0.61239624023437500  |
| 10                                                                                            | 0                    | 1                    |
| 11                                                                                            | -0.00286865234375000 | 0.61239624023437500  |
| 13                                                                                            | 0.00479125976562500  | -0.14880371093750000 |
| 15                                                                                            | -0.00762939453125000 | 0.04589843750000000  |
| 17                                                                                            | 0.01168060302734380  | -0.01086425781250000 |
| 19                                                                                            | -0.01736450195312500 | 0.00138854980468750  |
| 20, 22, 24, 26, 28, 30, 32, 36, 38, 40, 42,<br>44, 46, 48, 50, 52, 54, 56, 58, 60, 62, 64, 66 | 0                    |                      |
| 21                                                                                            | 0.02522850036621090  |                      |
| 23                                                                                            | -0.03616333007812500 |                      |
| 25                                                                                            | 0.05177307128906250  |                      |
| 27                                                                                            | -0.07537841796875000 |                      |
| 29                                                                                            | 0.11575317382812500  |                      |
| 31                                                                                            | -0.20507812500000000 |                      |
| 33                                                                                            | 0.63421630859375000  |                      |
| 34                                                                                            | 1                    |                      |
| 35                                                                                            | 0.63421630859375000  |                      |
| 37                                                                                            | -0.20507812500000000 |                      |
| 39                                                                                            | 0.11575317382812500  |                      |
| 41                                                                                            | -0.07537841796875000 |                      |
| 43                                                                                            | 0.05177307128906250  |                      |
| 45                                                                                            | -0.03616333007812500 |                      |
| 47                                                                                            | 0.02522850036621090  |                      |
| 49                                                                                            | -0.01736450195312500 |                      |
| 51                                                                                            | 0.01168060302734380  |                      |
| 53                                                                                            | -0.00762939453125000 |                      |
| 55                                                                                            | 0.00479125976562500  |                      |
| 57                                                                                            | -0.00286865234375000 |                      |
| 59                                                                                            | 0.00161743164062500  |                      |
| 61                                                                                            | -0.00083923339843750 |                      |

**Table 4. Digital Filter Coefficients (continued)**

|    |                      |  |
|----|----------------------|--|
| 63 | 0.00039672851562500  |  |
| 65 | -0.00015258789062500 |  |
| 67 | 0.00004577636718750  |  |

**Register Definition and Description**

The detailed description about the configuration registers in the MAX5855 can be found in the Register Map section, which can be configured through SPI serial control interface.

**SPI to PCLK Frequency Ratio**

The MAX5855 use a internally generated clock (PCLK) for the configuration of registers with the address between 0x0400 and 0x0DFF (RLinkRegs, RLaneRegs0-4, SerDesRegs, CMURegs, PHY0-4 register banks). PCLK is simply a divided down version of the internal DAC clock (DACCLK), and varies in proportion to that frequency. PCLK has the minimum and maximum frequency range required for the proper operation of the device.

- PCLK must be at least 14 times faster than the SPI clock.
- PCLK frequency cannot be greater than 300MHz.

This clock period relation is not required if the user is accessing any register below the 0x0400 address range (GLBL and DSP banks). The PCLK can be set in the DSP.CfgClkDiv.PCLK to 0x1, which uses the RCLK as the PCLK source. This configuration must be performed before accessing any register between addresses 0x0400 and 0x0DFF.

To select RCLK, write the appropriate division factor noted in the DSP.CfgClkDiv.RDIV register description.

**SPI to  $f_{DAC}$  Frequency Ratio**

The DAC clock is used to derive internal functional clocks and these divided-down clocks interact with the SPI clock (SCLK) during the register configuration. Therefore, the SPI clock frequency selection must not exceed 20MHz.

Note: SPI interface also has hold time requirement for the CSB pin. The hold time between a CSB signal going HIGH to the falling edge of last SCLK is 48  $f_{DAC}$  clock periods. See [Electrical Characteristics](#) notes for other serial interface timing details.

**Device Configuration**

The device configuration must be performed using a prescribed sequence.

The first step is to configure the SPI interface format. This is done by writing to the SPI register GLBL.CfgIFA at address 0x00. The control bits in this register form a symmetrical word (palindrome) such that the register can be programmed regardless of preexisting LSB-first or MSB-first operation. After writing to this register, the SPI interface will be ready for further programming.

The clock mode and the PLL must be configured immediately after the SPI interface.

The next step in the device configuration involves setting up the internal clocks while the CLKP/CLKN input is active. Programming and enabling the PLL clock path may result in internal glitches due to the clock path MUX and PLL settling. Once the PLL is enabled, the user must wait at least 20ms to allow the PLL to settle and lock before continuing on to the next configuration step.

The final step in configuring the PLL is to reset the internal clock dividers. The states of the dividers may have been corrupted by clock glitches during the preceding process.

If the device is powered up close to the low limit of the operating temperature range (cold), the digital PLL tuning may lock into a state which is not optimized for hot operation. To address this issue, it may be necessary to wait until the device self-heats before a restart of the PLL digital tuning is initiated. A 200ms wait cycle is recommended after the part is configured to allow for warm-up if needed.

After the PLL digital tuning has been restarted, it is necessary to wait 20ms for the PLL to settle and lock again prior to

resetting the internal clock dividers.

Once these preceding configurations are complete, the user should allow about 1ms for the internal DSP path to clear out before enabling the DAC output (unmute). If this pause is not included, the DAC output may produce spurious signals due to erroneous data flushing through the DSP signal path.

The MAX5855 configuration sequence is shown in the flowchart of [Figure 30](#).

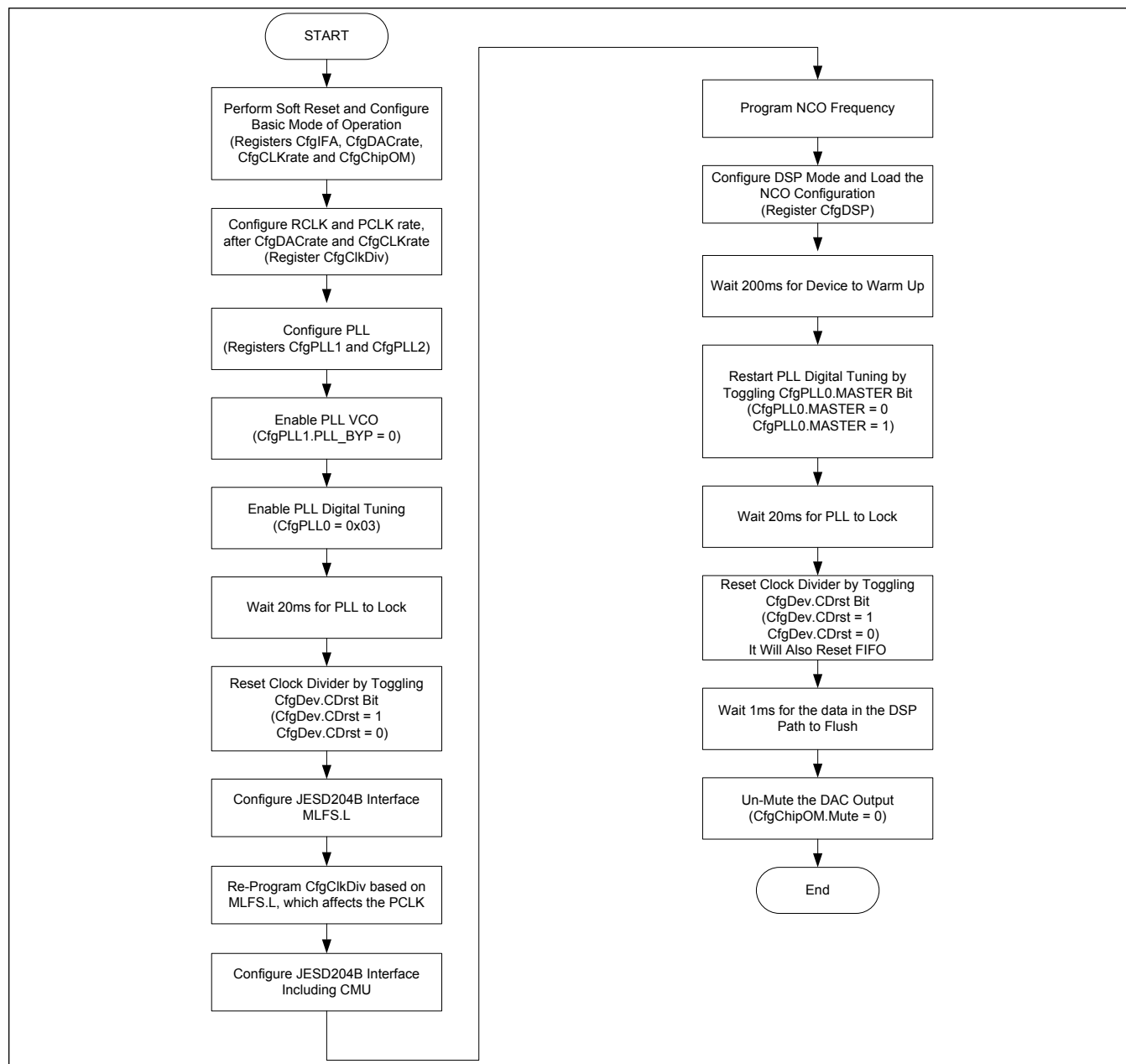


Figure 30. Device Configuration Flowchart

## Frequency Settings and Configuration

**Table 5. Frequency Planning and Configuration with CLKP/N Used as JESD204B Device Clock**

|                              |                |               |                  |                         | FRAME/SAMPLE<br>EXTERNAL |                         |                         |                         |                         |                         | FRAME/<br>SAMPLE<br>DIV DACCLK |                         |
|------------------------------|----------------|---------------|------------------|-------------------------|--------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|--------------------------------|-------------------------|
|                              |                |               |                  |                         | FRAME RATE<br>DIV 1      |                         | FRAME RATE<br>DIV 2     |                         | FRAME RATE<br>DIV 4     |                         |                                |                         |
| DACCLK<br>FREQUENCY<br>(GHz) | UPDATE<br>RATE | JESD<br>LANES | SAMPLE/<br>FRAME | LANE<br>RATES<br>(Gbps) | INPUT<br>CLOCK<br>(MHz)  | CONFIG<br>CLOCK<br>RATE | INPUT<br>CLOCK<br>(MHz) | CONFIG<br>CLOCK<br>RATE | INPUT<br>CLOCK<br>(MHz) | CONFIG<br>CLOCK<br>RATE | JESD<br>F-<br>RATE<br>(MHz)    | CLOCK<br>DIV F-<br>RATE |
| 4.91520                      | 5              | 5             | 5                | 9.8304                  | 245.76                   | 0                       | 491.52                  | 3                       | 983.04                  | 5                       | 245.76                         | 20                      |

**Update Rate** Selected DAC update rate multiplier: GLBL.CfgDACRate.Drate

**JESD Lanes** Number of JESD Lanes: RLinkRegs.CfgRLinkParam1.CfgL

**Sample/Frame** Number of JESD Samples Per Frame: RLinkRegs.CfgRLinkParam1.CfgS

**Frame/Sample** Clock source selection from the External Clock or a divided-down version of DACCLK: RLinkRegs.CfgRLinkCtrl.rclk = 0 or 1, respectively. For device clock input less than 1GHz, set to 0.

**Frame Rate Div X** JESD Frame Rate divisor 1, 2, or 4 of the Device Clock with RLinkRegs.CfgRLinkSet.DDIV=0, 1, or 2 respectively

**Input Clock** External device clock CLKP/CLKN

**Config Clock Rate** Programmed CLKP configuration value: GLBL.CfgCLKRate.Crate

**JESD F-Rate** JESD Frame Rate derived from the DAC update rate

**Clock Div F-Rate** Clock divider setting to generate the JESD Frame Rate: DSP.CfgClkDiv.RDIV

**Configuration Script Tool**

As noted in other sections of this document, proper sequential configuration of the MAX5855 DAC is essential to operating the device as intended. To assist the user with this configuration process, a PERL script tool has been developed which takes ten input parameters and provides an output file containing a sequence of commands that can be written to the device in order to program it for these user-defined operating conditions.

The user provides the input parameters through a text file (with a .txt extension) and the script will generate a sequence of SPI commands and stores them in an output text file (with a .cfg extension). The configuration parameters and the acceptable options used to create the input text file are listed in [Table 6](#).

**Table 6. Configuration Input Parameters**

| ITEM | PARAMETER     | OPTIONS               | COMMENTS                                                                |                  | EXAMPLE |
|------|---------------|-----------------------|-------------------------------------------------------------------------|------------------|---------|
| 1    | DAC Rate      | 4915                  | Value in Msps, must be used as given in the options column              |                  | 4915    |
| 2    | CLKPN Rate    | 983, 491, 245         | CLKP/CLKN clock rate in MHz                                             | Device Clock = 1 | 491     |
| 3    | INTP Ratio    | 4                     | Interpolation Ratio, set to 4                                           |                  | 4       |
| 4    | Lane Count    | 5                     | Number of JESD204B lanes to be used                                     |                  | 5       |
| 5    | Subclass      | 0                     | JESD204B Subclass selection                                             |                  | 0       |
| 6    | Device Clock  | 1                     | JESD204B Frame sample clock derived from...                             | CLKP/CLKN        | 1       |
| 7    | SYSREF Mode   | 0                     | SYSREF mode, set to 0                                                   |                  | 0       |
| 8    | NCO Frequency | 0, 1, ..., 2948, 2949 | f <sub>NCO</sub> in MHz, value between DC and the DAC Rate divided by 2 |                  | 1000    |
| 9    | RCLK Div      | 1, 2, 4               | Sample-Rate-to-RCLK ratio                                               |                  | 1       |
| 10   | ScrambleDis   | 0                     | JESD204B lane scrambler                                                 | enabled          | 0       |
|      |               | 1                     |                                                                         | disabled         |         |

Example input file example\_config.txt, contains the below parameter settings:

```

DAC Rate    = 4915
CLKPN Rate  = 491
INTP Ratio  = 4
Lane Count  = 5
Subclass    = 0
Device Clock = 1
SYSREF Mode = 0
NCO Freq    = 1000
RCLK Div    = 1
ScrambleDis = 0

```

To execute the PERL script command line type the following:

```
perl gen_MAX585x_config.pl example_config.txt
```

Checking setup ...

Creating example\_config.cfg file for following setup:

```

DAC update Rate ..... 4915MHz
CLKPN Input Rate .... 491MHz
DSP INTP Ratio ..... 4

```

```
RxLink Lane Count ... 5
RxLink Subclass ..... 0
RxLink Clock source . Device Clock
RxLink SYSREF mode .. One-shot
NCO Freq ..... 1000MHz
RCLK Out ..... Frame Rate/1
Scramble Disable .... 0 (1:off, 0:on)
(SERDES = 10G, Full Rate; Frame Rate = 245.75M)
```

The resulting output command file can be used to configure the device through the SPI. Each line of the .cfg file contains the register address and the data value to be programmed. Within the output .cfg file, wait statements will be inserted at the required points in the programming sequence to indicate a need for a pause before the next write command.

The following is list of the first 7 lines of the example\_config.cfg output file:

```
// For Trimmed version of part
// Script version used: v1.0
// SS:MIN:HR:DAY:MM:YY
// 21:12:11:26:10:17
0x0000,0xBD; //GLBL.CfgIFA.AddIncr=1'b1, Wire4=1'b1, SftRst=1'b1 (self-clearing)
0x0010,0x05; //GLBL.CfgDACrate=4'b0101
0x0011,0x03; //GLBL.CfgCLKrate=4'b0011
...
```

## Register Map

## MAX5855

| ADDRESS | NAME            | MSB         |            |          |       |            |            |            | LSB     |
|---------|-----------------|-------------|------------|----------|-------|------------|------------|------------|---------|
| GLBL    |                 |             |            |          |       |            |            |            |         |
| 0x00    | CfgIFA[7:0]     | SftRst      | LSBF       | AddIncr  | Wire4 | Wire4_0    | AddIncr0   | LSBF0      | SftRst0 |
| 0x01    | CfgIFB[7:0]     | StrmDis     | rsvd6      | –        | rsvd4 | rsvd3      | –          | –          | rsvd0   |
| 0x02    | CfgDev[7:0]     | rsvd[4:0]   |            |          |       |            | CDrst      | PDM[1:0]   |         |
| 0x03    | ChipType[7:0]   | –           | –          | –        | –     | Type[3:0]  |            |            |         |
| 0x04    | ChipID1[7:0]    | CIDLSB[1:0] |            | PID[1:0] |       | FID[3:0]   |            |            |         |
| 0x05    | ChipID2[7:0]    | CIDMSB[7:0] |            |          |       |            |            |            |         |
| 0x06    | ChipRev[7:0]    | –           | –          | –        | –     | Rev[3:0]   |            |            |         |
| 0x0C    | VendID1[7:0]    | VIDLSB[7:0] |            |          |       |            |            |            |         |
| 0x0D    | VendID2[7:0]    | VIDMSB[7:0] |            |          |       |            |            |            |         |
| 0x10    | CfgDACrate[7:0] | –           | –          | –        | –     | Drate[3:0] |            |            |         |
| 0x11    | CfgCLKrate[7:0] | –           | –          | –        | –     | Crate[3:0] |            |            |         |
| 0x12    | CfgREGS[7:0]    | –           | –          | –        | –     | –          | –          | rsvd       | IntCfg  |
| DSP     |                 |             |            |          |       |            |            |            |         |
| 0x100   | CfgChipOM[7:0]  | –           | RclkM[1:0] |          | INVQ  | –          | Mute       | –          | DFMT    |
| 0x101   | CfgDSP[7:0]     | R[3:0]      |            |          |       | RstDSP     | RstFIFO    | NCOE       | NCOLD   |
| 0x102   | CfgNCOF0[7:0]   | FCW[7:0]    |            |          |       |            |            |            |         |
| 0x103   | CfgNCOF1[7:0]   | FCW[15:8]   |            |          |       |            |            |            |         |
| 0x104   | CfgNCOF2[7:0]   | FCW[23:16]  |            |          |       |            |            |            |         |
| 0x105   | CfgNCOF3[7:0]   | FCW[31:24]  |            |          |       |            |            |            |         |
| 0x106   | CfgNCON0[7:0]   | NFW[7:0]    |            |          |       |            |            |            |         |
| 0x107   | CfgNCON1[7:0]   | NFW[15:8]   |            |          |       |            |            |            |         |
| 0x108   | CfgNCON2[7:0]   | –           | –          | –        | –     | –          | –          | NFW[17:16] |         |
| 0x109   | CfgNCOD0[7:0]   | DFW[7:0]    |            |          |       |            |            |            |         |
| 0x10A   | CfgNCOD1[7:0]   | DFW[15:8]   |            |          |       |            |            |            |         |
| 0x10B   | CfgNCOD2[7:0]   | –           | –          | –        | –     | –          | DFW[18:16] |            |         |
| 0x10C   | CfgNCOU[7:0]    | –           | –          | –        | –     | –          | –          | RLM[1:0]   |         |
| 0x10D   | CfgNCOUT0[7:0]  | TIM[7:0]    |            |          |       |            |            |            |         |
| 0x10E   | CfgNCOUT1[7:0]  | TIM[7:0]    |            |          |       |            |            |            |         |
| 0x10F   | CfgNCOUT2[7:0]  | TIM[7:0]    |            |          |       |            |            |            |         |
| 0x110   | CfgPM[7:0]      | –           | –          | –        | –     | –          | Start      | Mode       | Reset   |
| 0x111   | CfgPMT[7:0]     | PMT[7:0]    |            |          |       |            |            |            |         |
| 0x112   | CfgPMIC0[7:0]   | PMIC[7:0]   |            |          |       |            |            |            |         |
| 0x113   | CfgPMIC1[7:0]   | PMIC[7:0]   |            |          |       |            |            |            |         |
| 0x114   | CfgPMIC2[7:0]   | PMIC[7:0]   |            |          |       |            |            |            |         |
| 0x115   | CfgPMIC3[7:0]   | PMIC[7:0]   |            |          |       |            |            |            |         |
| 0x116   | CfgPMIC4[7:0]   | PMIC[7:0]   |            |          |       |            |            |            |         |

| ADDRESS   | NAME                                  | MSB                         |                                  |                            |                            |                               |                       |                           | LSB                           |
|-----------|---------------------------------------|-----------------------------|----------------------------------|----------------------------|----------------------------|-------------------------------|-----------------------|---------------------------|-------------------------------|
| 0x117     | <a href="#">CfgPMIC5[7:0]</a>         | <a href="#">PMIC[7:0]</a>   |                                  |                            |                            |                               |                       |                           |                               |
| 0x118     | <a href="#">StatPM0[7:0]</a>          | <a href="#">PMST[7:0]</a>   |                                  |                            |                            |                               |                       |                           |                               |
| 0x119     | <a href="#">StatPM1[7:0]</a>          | <a href="#">PMDON<br/>E</a> | -                                | -                          | -                          | <a href="#">PMST[3:0]</a>     |                       |                           |                               |
| 0x15A     | <a href="#">CfgSync[7:0]</a>          | -                           | <a href="#">ClkDiv_S<br/>ync</a> | -                          | -                          | -                             | -                     | -                         | -                             |
| 0x15B     | <a href="#">CfgFIFO[7:0]</a>          | <a href="#">rsvd[4:0]</a>   |                                  |                            |                            |                               | <a href="#">Dupl</a>  | <a href="#">SwapIQ</a>    | <a href="#">RevBitO<br/>d</a> |
| 0x15D     | <a href="#">CfgRSV0[7:0]</a>          | <a href="#">RSV[7:0]</a>    |                                  |                            |                            |                               |                       |                           |                               |
| 0x15E     | <a href="#">CfgRSV1[7:0]</a>          | <a href="#">RSV[7:0]</a>    |                                  |                            |                            |                               |                       |                           |                               |
| 0x15F     | <a href="#">CfgRSV2[7:0]</a>          | <a href="#">RSV[7:0]</a>    |                                  |                            |                            |                               |                       |                           |                               |
| 0x160     | <a href="#">CfgRSV3[7:0]</a>          | <a href="#">RSV[7:0]</a>    |                                  |                            |                            |                               |                       |                           |                               |
| 0x162     | <a href="#">EMUTE[7:0]</a>            | <a href="#">EM[7:0]</a>     |                                  |                            |                            |                               |                       |                           |                               |
| 0x163     | <a href="#">EINT[7:0]</a>             | <a href="#">INT_EN[7:0]</a> |                                  |                            |                            |                               |                       |                           |                               |
| 0x164     | <a href="#">STATUS[7:0]</a>           | <a href="#">JSDIM</a>       | <a href="#">JSDII</a>            | <a href="#">rsvd[2:0]</a>  |                            |                               | <a href="#">TRDY</a>  | -                         | <a href="#">PLLick</a>        |
| 0x165     | <a href="#">RSVD7[7:0]</a>            | <a href="#">rsvd[7:0]</a>   |                                  |                            |                            |                               |                       |                           |                               |
| 0x166     | <a href="#">DEVSNO[7:0]</a>           | <a href="#">SN[7:0]</a>     |                                  |                            |                            |                               |                       |                           |                               |
| 0x167     | <a href="#">DEVSNO1[7:0]</a>          | -                           | -                                | -                          | -                          | -                             | -                     | -                         | -                             |
| 0x168     | <a href="#">DEVSNO2[7:0]</a>          | -                           | -                                | -                          | -                          | -                             | -                     | -                         | -                             |
| 0x180     | <a href="#">CfgPLL0[7:0]</a>          | -                           | -                                | -                          | -                          | -                             | -                     | -                         | <a href="#">MASTER</a>        |
| 0x181     | <a href="#">CfgPLL1[7:0]</a>          | -                           | <a href="#">PLL_BY<br/>P</a>     | <a href="#">DVAL0[1:0]</a> |                            | <a href="#">PVAL</a>          | <a href="#">RVAL0</a> | -                         | -                             |
| 0x182     | <a href="#">CfgPLL2[7:0]</a>          | -                           | -                                | -                          | <a href="#">DVAL1[1:0]</a> |                               | <a href="#">RVAL1</a> | -                         | <a href="#">VCO_SE<br/>L</a>  |
| 0x183     | <a href="#">StatPLL0[7:0]</a>         | <a href="#">rsvd[3:0]</a>   |                                  |                            |                            | <a href="#">PLL_LO<br/>CK</a> | -                     | -                         | -                             |
| 0x185     | <a href="#">CfgClkDiv[7:0]</a>        | <a href="#">RDIV[3:0]</a>   |                                  |                            |                            | <a href="#">RSV[1:0]</a>      |                       | <a href="#">PCLK[1:0]</a> |                               |
| RLinkRegs |                                       |                             |                                  |                            |                            |                               |                       |                           |                               |
| 0x400     | <a href="#">CfgRLinkSet[31:24]</a>    | -                           | -                                | -                          | -                          | -                             | -                     | -                         | -                             |
|           | <a href="#">CfgRLinkSet[23:16]</a>    | -                           | -                                | -                          | -                          | -                             | -                     | <a href="#">SyncInit</a>  | <a href="#">SyncPol</a>       |
|           | <a href="#">CfgRLinkSet[15:8]</a>     | -                           | -                                | -                          | -                          | -                             | -                     | <a href="#">IgnDisp</a>   | <a href="#">ScrmD</a>         |
|           | <a href="#">CfgRLinkSet[7:0]</a>      | -                           | -                                | <a href="#">DDiv[1:0]</a>  |                            | <a href="#">Subclass[1:0]</a> |                       | <a href="#">RstSRL</a>    | <a href="#">RstILA</a>        |
| 0x404     | <a href="#">CfgRLinkParam1[31:24]</a> | -                           | -                                | -                          | <a href="#">CfgS[4:0]</a>  |                               |                       |                           |                               |
|           | <a href="#">CfgRLinkParam1[23:16]</a> | <a href="#">CfgF[7:0]</a>   |                                  |                            |                            |                               |                       |                           |                               |
|           | <a href="#">CfgRLinkParam1[15:8]</a>  | -                           | -                                | -                          | <a href="#">CfgL[4:0]</a>  |                               |                       |                           |                               |
|           | <a href="#">CfgRLinkParam1[7:0]</a>   | <a href="#">CfgM[7:0]</a>   |                                  |                            |                            |                               |                       |                           |                               |
| 0x408     | <a href="#">CfgRLinkParam2[31:24]</a> | <a href="#">DID[7:0]</a>    |                                  |                            |                            |                               |                       |                           |                               |
|           | <a href="#">CfgRLinkParam2[23:16]</a> | <a href="#">HD</a>          | -                                | -                          | -                          | <a href="#">BID[3:0]</a>      |                       |                           |                               |
|           | <a href="#">CfgRLinkParam2[15:8]</a>  | <a href="#">CfgNP[2:0]</a>  |                                  |                            | <a href="#">CfgN[4:0]</a>  |                               |                       |                           |                               |
|           | <a href="#">CfgRLinkParam2[7:0]</a>   | -                           | -                                | -                          | <a href="#">CfgK[4:0]</a>  |                               |                       |                           |                               |
| 0x410     | <a href="#">CfgRLinkCtrl[31:24]</a>   | -                           | -                                | -                          | -                          | -                             | -                     | -                         | -                             |
|           | <a href="#">CfgRLinkCtrl[23:16]</a>   | -                           | <a href="#">SCtrl[1:0]</a>       |                            | <a href="#">DFSycn</a>     | -                             | -                     | -                         | -                             |

| ADDRESS | NAME                                  | MSB                               |                               |                               |                                   |                               |                               |                           | LSB                             |
|---------|---------------------------------------|-----------------------------------|-------------------------------|-------------------------------|-----------------------------------|-------------------------------|-------------------------------|---------------------------|---------------------------------|
|         | <a href="#">CfgRLinkCtrl[15:8]</a>    | –                                 | –                             | –                             | –                                 | –                             | –                             | –                         | <a href="#">SErrC</a>           |
|         | <a href="#">CfgRLinkCtrl[7:0]</a>     | –                                 | –                             | –                             | –                                 | <a href="#">BitSwap</a>       | –                             | <a href="#">AsyncAvl</a>  | <a href="#">rclk</a>            |
| 0x414   | <a href="#">CfgRLinkMFrame[31:24]</a> | –                                 | –                             | –                             | –                                 | –                             | –                             | <a href="#">SNum[8:7]</a> |                                 |
|         | <a href="#">CfgRLinkMFrame[23:16]</a> | <a href="#">SNum[6:0]</a>         |                               |                               |                                   |                               |                               |                           | <a href="#">MFSel[8]</a>        |
|         | <a href="#">CfgRLinkMFrame[15:8]</a>  | <a href="#">MFSel[7:0]</a>        |                               |                               |                                   |                               |                               |                           |                                 |
|         | <a href="#">CfgRLinkMFrame[7:0]</a>   | –                                 | –                             | <a href="#">ILADly[5:0]</a>   |                                   |                               |                               |                           |                                 |
| 0x418   | <a href="#">CfgRSYNCRN[31:24]</a>     | –                                 | –                             | –                             | –                                 | –                             | –                             | –                         | –                               |
|         | <a href="#">CfgRSYNCRN[23:16]</a>     | –                                 | –                             | –                             | –                                 | –                             | –                             | –                         | –                               |
|         | <a href="#">CfgRSYNCRN[15:8]</a>      | –                                 | <a href="#">RepErr1<br/>4</a> | <a href="#">RepErr1<br/>3</a> | <a href="#">RepErr1<br/>2</a>     | <a href="#">RepErr1<br/>1</a> | <a href="#">RepErr1<br/>0</a> | <a href="#">RepErr9</a>   | <a href="#">RepErr8</a>         |
|         | <a href="#">CfgRSYNCRN[7:0]</a>       | –                                 | <a href="#">RepErr6</a>       | <a href="#">RepErr5</a>       | –                                 | –                             | <a href="#">RepErr2</a>       | <a href="#">RepErr1</a>   | <a href="#">RepErr0</a>         |
| 0x41C   | <a href="#">CfgRFIFO[31:24]</a>       | –                                 | –                             | –                             | –                                 | –                             | –                             | –                         | –                               |
|         | <a href="#">CfgRFIFO[23:16]</a>       | –                                 | –                             | –                             | –                                 | –                             | –                             | –                         | –                               |
|         | <a href="#">CfgRFIFO[15:8]</a>        | –                                 | –                             | –                             | <a href="#">MaxFD[4:0]</a>        |                               |                               |                           |                                 |
|         | <a href="#">CfgRFIFO[7:0]</a>         | –                                 | –                             | –                             | <a href="#">MinFD[4:0]</a>        |                               |                               |                           |                                 |
| 0x420   | <a href="#">CfgRTestCtrl[31:24]</a>   | –                                 | –                             | –                             | –                                 | –                             | –                             | –                         | <a href="#">LnCntTypeSel[3]</a> |
|         | <a href="#">CfgRTestCtrl[23:16]</a>   | <a href="#">LnCntTypeSel[2:0]</a> |                               |                               | <a href="#">RxCntLaneSel[4:0]</a> |                               |                               |                           |                                 |
|         | <a href="#">CfgRTestCtrl[15:8]</a>    | –                                 | –                             | <a href="#">SamLoad</a>       | <a href="#">RxLoad</a>            | <a href="#">CDcorEn</a>       | <a href="#">Rsvd0</a>         | –                         | –                               |
|         | <a href="#">CfgRTestCtrl[7:0]</a>     | –                                 | –                             | –                             | <a href="#">PRBStype[1:0]</a>     |                               | –                             | <a href="#">RxPRBSen</a>  | <a href="#">SamPRBS15En</a>     |
| 0x424   | <a href="#">CfgRLinkSTP1[31:24]</a>   | –                                 | –                             | –                             | –                                 | –                             | –                             | –                         | –                               |
|         | <a href="#">CfgRLinkSTP1[23:16]</a>   | –                                 | –                             | –                             | –                                 | –                             | –                             | –                         | –                               |
|         | <a href="#">CfgRLinkSTP1[15:8]</a>    | <a href="#">Sample1[15:8]</a>     |                               |                               |                                   |                               |                               |                           |                                 |
|         | <a href="#">CfgRLinkSTP1[7:0]</a>     | <a href="#">Sample1[7:0]</a>      |                               |                               |                                   |                               |                               |                           |                                 |
| 0x428   | <a href="#">CfgRLinkSTP2[31:24]</a>   | –                                 | –                             | –                             | –                                 | –                             | –                             | –                         | –                               |
|         | <a href="#">CfgRLinkSTP2[23:16]</a>   | –                                 | –                             | –                             | –                                 | –                             | –                             | –                         | –                               |
|         | <a href="#">CfgRLinkSTP2[15:8]</a>    | <a href="#">Sample2[15:8]</a>     |                               |                               |                                   |                               |                               |                           |                                 |
|         | <a href="#">CfgRLinkSTP2[7:0]</a>     | <a href="#">Sample2[7:0]</a>      |                               |                               |                                   |                               |                               |                           |                                 |
| 0x430   | <a href="#">CfgRLinkIntEn[31:24]</a>  | –                                 | –                             | –                             | –                                 | –                             | –                             | –                         | –                               |
|         | <a href="#">CfgRLinkIntEn[23:16]</a>  | –                                 | –                             | –                             | –                                 | –                             | –                             | –                         | –                               |
|         | <a href="#">CfgRLinkIntEn[15:8]</a>   | –                                 | –                             | –                             | –                                 | –                             | –                             | –                         | –                               |
|         | <a href="#">CfgRLinkIntEn[7:0]</a>    | –                                 | –                             | –                             | –                                 | <a href="#">ILAnsync</a>      | –                             | –                         | <a href="#">ILAfail</a>         |
| 0x434   | <a href="#">CfgRLinkMuteEn[31:24]</a> | –                                 | –                             | –                             | –                                 | –                             | –                             | –                         | –                               |
|         | <a href="#">CfgRLinkMuteEn[23:16]</a> | –                                 | –                             | –                             | –                                 | –                             | –                             | –                         | –                               |
|         | <a href="#">CfgRLinkMuteEn[15:8]</a>  | –                                 | –                             | –                             | –                                 | –                             | –                             | –                         | –                               |
|         | <a href="#">CfgRLinkMuteEn[7:0]</a>   | –                                 | –                             | –                             | –                                 | <a href="#">ILAnsync</a>      | –                             | –                         | <a href="#">ILAfail</a>         |
| 0x438   | <a href="#">StatRLinkILA[31:24]</a>   | –                                 | –                             | –                             | –                                 | –                             | –                             | –                         | –                               |
|         | <a href="#">StatRLinkILA[23:16]</a>   | –                                 | –                             | –                             | –                                 | –                             | –                             | –                         | –                               |

| ADDRESS     | NAME                                  | MSB                          |                                |                                |                         |                          |                         |                                | LSB                             |
|-------------|---------------------------------------|------------------------------|--------------------------------|--------------------------------|-------------------------|--------------------------|-------------------------|--------------------------------|---------------------------------|
|             | <a href="#">StatRLinkILA[15:8]</a>    | –                            | –                              | –                              | –                       | –                        | –                       | –                              | –                               |
|             | <a href="#">StatRLinkILA[7:0]</a>     | –                            | –                              | –                              | –                       | <a href="#">ILAnsync</a> | –                       | –                              | <a href="#">ILAfailur<br/>e</a> |
| 0x43C       | <a href="#">StatRLinkSTP[31:24]</a>   | –                            | –                              | –                              | –                       | –                        | –                       | –                              | –                               |
|             | <a href="#">StatRLinkSTP[23:16]</a>   | –                            | –                              | –                              | –                       | –                        | –                       | –                              | –                               |
|             | <a href="#">StatRLinkSTP[15:8]</a>    | –                            | –                              | –                              | –                       | –                        | –                       | –                              | –                               |
|             | <a href="#">StatRLinkSTP[7:0]</a>     | –                            | –                              | –                              | –                       | –                        | –                       | <a href="#">STPerr1</a>        | <a href="#">STPerr0</a>         |
| 0x440       | <a href="#">StatRLinkPRBS[31:24]</a>  | –                            | –                              | –                              | –                       | –                        | –                       | –                              | –                               |
|             | <a href="#">StatRLinkPRBS[23:16]</a>  | –                            | –                              | –                              | –                       | –                        | –                       | –                              | –                               |
|             | <a href="#">StatRLinkPRBS[15:8]</a>   | –                            | –                              | –                              | –                       | –                        | –                       | –                              | –                               |
|             | <a href="#">StatRLinkPRBS[7:0]</a>    | –                            | –                              | –                              | –                       | –                        | –                       | <a href="#">PRBSerr<br/>1</a>  | <a href="#">PRBSerr<br/>0</a>   |
| 0x460       | <a href="#">CntRLaneInvid[31:24]</a>  | –                            | –                              | –                              | –                       | –                        | –                       | –                              | –                               |
|             | <a href="#">CntRLaneInvid[23:16]</a>  | –                            | –                              | –                              | –                       | –                        | –                       | –                              | –                               |
|             | <a href="#">CntRLaneInvid[15:8]</a>   | <a href="#">InvCnt[15:8]</a> |                                |                                |                         |                          |                         |                                |                                 |
|             | <a href="#">CntRLaneInvid[7:0]</a>    | <a href="#">InvCnt[7:0]</a>  |                                |                                |                         |                          |                         |                                |                                 |
| 0x464       | <a href="#">CntRLaneDbg[31:24]</a>    | –                            | –                              | –                              | –                       | –                        | –                       | –                              | –                               |
|             | <a href="#">CntRLaneDbg[23:16]</a>    | –                            | –                              | –                              | –                       | –                        | –                       | –                              | –                               |
|             | <a href="#">CntRLaneDbg[15:8]</a>     | <a href="#">DbgCnt[15:8]</a> |                                |                                |                         |                          |                         |                                |                                 |
|             | <a href="#">CntRLaneDbg[7:0]</a>      | <a href="#">DbgCnt[7:0]</a>  |                                |                                |                         |                          |                         |                                |                                 |
| RLaneRegs 0 |                                       |                              |                                |                                |                         |                          |                         |                                |                                 |
| 0x480       | <a href="#">CfgRLaneSet[31:24]</a>    | <a href="#">LnSrc[4:0]</a>   |                                |                                |                         |                          | –                       | <a href="#">LkSel</a>          | <a href="#">LnEn</a>            |
|             | <a href="#">CfgRLaneSet[23:16]</a>    | –                            | –                              | –                              | –                       | –                        | –                       | –                              | –                               |
|             | <a href="#">CfgRLaneSet[15:8]</a>     | –                            | –                              | –                              | –                       | –                        | –                       | –                              | –                               |
|             | <a href="#">CfgRLaneSet[7:0]</a>      | –                            | –                              | <a href="#">LID[4:0]</a>       |                         |                          |                         |                                | <a href="#">LnRst</a>           |
| 0x484       | <a href="#">CfgRLaneIntEn[31:24]</a>  | –                            | <a href="#">DContErr</a>       | –                              | <a href="#">PRBSerr</a> | <a href="#">KContErr</a> | <a href="#">FChkErr</a> | <a href="#">LCfgErr</a>        | <a href="#">ILAerr</a>          |
|             | <a href="#">CfgRLaneIntEn[23:16]</a>  | –                            | –                              | –                              | –                       | –                        | –                       | <a href="#">FIFOem<br/>pty</a> | <a href="#">FIFOfull</a>        |
|             | <a href="#">CfgRLaneIntEn[15:8]</a>   | –                            | –                              | –                              | –                       | –                        | –                       | –                              | –                               |
|             | <a href="#">CfgRLaneIntEn[7:0]</a>    | <a href="#">FrNSync</a>      | <a href="#">LnReAlig<br/>n</a> | <a href="#">FrReAlig<br/>n</a> | –                       | –                        | <a href="#">DISP</a>    | <a href="#">NIT</a>            | <a href="#">CGS</a>             |
| 0x488       | <a href="#">CfgRLaneMuteEn[31:24]</a> | –                            | <a href="#">DContErr</a>       | –                              | <a href="#">PRBSerr</a> | <a href="#">KContErr</a> | <a href="#">FChkErr</a> | <a href="#">LCfgErr</a>        | <a href="#">ILAerr</a>          |
|             | <a href="#">CfgRLaneMuteEn[23:16]</a> | –                            | –                              | –                              | –                       | –                        | –                       | <a href="#">FIFOem<br/>pty</a> | <a href="#">FIFOfull</a>        |
|             | <a href="#">CfgRLaneMuteEn[15:8]</a>  | –                            | –                              | –                              | –                       | –                        | –                       | –                              | –                               |
|             | <a href="#">CfgRLaneMuteEn[7:0]</a>   | <a href="#">FrNSync</a>      | <a href="#">LnReAlig<br/>n</a> | <a href="#">FrReAlig<br/>n</a> | –                       | –                        | <a href="#">DISP</a>    | <a href="#">NIT</a>            | <a href="#">CGS</a>             |
| 0x48C       | <a href="#">StatRLane[31:24]</a>      | –                            | <a href="#">DContErr</a>       | –                              | <a href="#">PRBSerr</a> | <a href="#">KContErr</a> | <a href="#">FChkErr</a> | <a href="#">LCfgErr</a>        | <a href="#">ILAerr</a>          |
|             | <a href="#">StatRLane[23:16]</a>      | –                            | –                              | –                              | –                       | –                        | –                       | <a href="#">FIFOem<br/>pty</a> | <a href="#">FIFOfull</a>        |
|             | <a href="#">StatRLane[15:8]</a>       | –                            | –                              | <a href="#">FIFODepth[5:0]</a> |                         |                          |                         |                                |                                 |
|             | <a href="#">StatRLane[7:0]</a>        | <a href="#">FrNSync</a>      | <a href="#">LnReAlig</a>       | <a href="#">FrReAlig</a>       | –                       | –                        | <a href="#">DISP</a>    | <a href="#">NIT</a>            | <a href="#">CGS</a>             |

| ADDRESS            | NAME                                  | MSB                     |                                |                                |                         |                          |                         |                                | LSB                      |
|--------------------|---------------------------------------|-------------------------|--------------------------------|--------------------------------|-------------------------|--------------------------|-------------------------|--------------------------------|--------------------------|
|                    |                                       |                         | <u>n</u>                       | <u>n</u>                       |                         |                          |                         |                                |                          |
| <b>RLaneRegs 1</b> |                                       |                         |                                |                                |                         |                          |                         |                                |                          |
| 0x490              | <a href="#">CfgRLaneSet[31:24]</a>    |                         | <a href="#">LnSrc[4:0]</a>     |                                |                         |                          | –                       | <a href="#">LkSel</a>          | <a href="#">LnEn</a>     |
|                    | <a href="#">CfgRLaneSet[23:16]</a>    | –                       | –                              | –                              | –                       | –                        | –                       | –                              | –                        |
|                    | <a href="#">CfgRLaneSet[15:8]</a>     | –                       | –                              | –                              | –                       | –                        | –                       | –                              | –                        |
|                    | <a href="#">CfgRLaneSet[7:0]</a>      | –                       | –                              | <a href="#">LID[4:0]</a>       |                         |                          |                         |                                | <a href="#">LnRst</a>    |
| 0x494              | <a href="#">CfgRLaneIntEn[31:24]</a>  | –                       | <a href="#">DContErr</a>       | –                              | <a href="#">PRBSerr</a> | <a href="#">KContErr</a> | <a href="#">FChkErr</a> | <a href="#">LCfgErr</a>        | <a href="#">ILAerr</a>   |
|                    | <a href="#">CfgRLaneIntEn[23:16]</a>  | –                       | –                              | –                              | –                       | –                        | –                       | <a href="#">FIFOem<br/>pty</a> | <a href="#">FIFOfull</a> |
|                    | <a href="#">CfgRLaneIntEn[15:8]</a>   | –                       | –                              | –                              | –                       | –                        | –                       | –                              | –                        |
|                    | <a href="#">CfgRLaneIntEn[7:0]</a>    | <a href="#">FrNSync</a> | <a href="#">LnReAlig<br/>n</a> | <a href="#">FrReAlig<br/>n</a> | –                       | –                        | <a href="#">DISP</a>    | <a href="#">NIT</a>            | <a href="#">CGS</a>      |
| 0x498              | <a href="#">CfgRLaneMuteEn[31:24]</a> | –                       | <a href="#">DContErr</a>       | –                              | <a href="#">PRBSerr</a> | <a href="#">KContErr</a> | <a href="#">FChkErr</a> | <a href="#">LCfgErr</a>        | <a href="#">ILAerr</a>   |
|                    | <a href="#">CfgRLaneMuteEn[23:16]</a> | –                       | –                              | –                              | –                       | –                        | –                       | <a href="#">FIFOem<br/>pty</a> | <a href="#">FIFOfull</a> |
|                    | <a href="#">CfgRLaneMuteEn[15:8]</a>  | –                       | –                              | –                              | –                       | –                        | –                       | –                              | –                        |
|                    | <a href="#">CfgRLaneMuteEn[7:0]</a>   | <a href="#">FrNSync</a> | <a href="#">LnReAlig<br/>n</a> | <a href="#">FrReAlig<br/>n</a> | –                       | –                        | <a href="#">DISP</a>    | <a href="#">NIT</a>            | <a href="#">CGS</a>      |
| 0x49C              | <a href="#">StatRLane[31:24]</a>      | –                       | <a href="#">DContErr</a>       | –                              | <a href="#">PRBSerr</a> | <a href="#">KContErr</a> | <a href="#">FChkErr</a> | <a href="#">LCfgErr</a>        | <a href="#">ILAerr</a>   |
|                    | <a href="#">StatRLane[23:16]</a>      | –                       | –                              | –                              | –                       | –                        | –                       | <a href="#">FIFOem<br/>pty</a> | <a href="#">FIFOfull</a> |
|                    | <a href="#">StatRLane[15:8]</a>       | –                       | –                              | <a href="#">FIFODepth[5:0]</a> |                         |                          |                         |                                |                          |
|                    | <a href="#">StatRLane[7:0]</a>        | <a href="#">FrNSync</a> | <a href="#">LnReAlig<br/>n</a> | <a href="#">FrReAlig<br/>n</a> | –                       | –                        | <a href="#">DISP</a>    | <a href="#">NIT</a>            | <a href="#">CGS</a>      |
| <b>RLaneRegs 2</b> |                                       |                         |                                |                                |                         |                          |                         |                                |                          |
| 0x4A0              | <a href="#">CfgRLaneSet[31:24]</a>    |                         | <a href="#">LnSrc[4:0]</a>     |                                |                         |                          | –                       | <a href="#">LkSel</a>          | <a href="#">LnEn</a>     |
|                    | <a href="#">CfgRLaneSet[23:16]</a>    | –                       | –                              | –                              | –                       | –                        | –                       | –                              | –                        |
|                    | <a href="#">CfgRLaneSet[15:8]</a>     | –                       | –                              | –                              | –                       | –                        | –                       | –                              | –                        |
|                    | <a href="#">CfgRLaneSet[7:0]</a>      | –                       | –                              | <a href="#">LID[4:0]</a>       |                         |                          |                         |                                | <a href="#">LnRst</a>    |
| 0x4A4              | <a href="#">CfgRLaneIntEn[31:24]</a>  | –                       | <a href="#">DContErr</a>       | –                              | <a href="#">PRBSerr</a> | <a href="#">KContErr</a> | <a href="#">FChkErr</a> | <a href="#">LCfgErr</a>        | <a href="#">ILAerr</a>   |
|                    | <a href="#">CfgRLaneIntEn[23:16]</a>  | –                       | –                              | –                              | –                       | –                        | –                       | <a href="#">FIFOem<br/>pty</a> | <a href="#">FIFOfull</a> |
|                    | <a href="#">CfgRLaneIntEn[15:8]</a>   | –                       | –                              | –                              | –                       | –                        | –                       | –                              | –                        |
|                    | <a href="#">CfgRLaneIntEn[7:0]</a>    | <a href="#">FrNSync</a> | <a href="#">LnReAlig<br/>n</a> | <a href="#">FrReAlig<br/>n</a> | –                       | –                        | <a href="#">DISP</a>    | <a href="#">NIT</a>            | <a href="#">CGS</a>      |
| 0x4A8              | <a href="#">CfgRLaneMuteEn[31:24]</a> | –                       | <a href="#">DContErr</a>       | –                              | <a href="#">PRBSerr</a> | <a href="#">KContErr</a> | <a href="#">FChkErr</a> | <a href="#">LCfgErr</a>        | <a href="#">ILAerr</a>   |
|                    | <a href="#">CfgRLaneMuteEn[23:16]</a> | –                       | –                              | –                              | –                       | –                        | –                       | <a href="#">FIFOem<br/>pty</a> | <a href="#">FIFOfull</a> |
|                    | <a href="#">CfgRLaneMuteEn[15:8]</a>  | –                       | –                              | –                              | –                       | –                        | –                       | –                              | –                        |
|                    | <a href="#">CfgRLaneMuteEn[7:0]</a>   | <a href="#">FrNSync</a> | <a href="#">LnReAlig<br/>n</a> | <a href="#">FrReAlig<br/>n</a> | –                       | –                        | <a href="#">DISP</a>    | <a href="#">NIT</a>            | <a href="#">CGS</a>      |
| 0x4AC              | <a href="#">StatRLane[31:24]</a>      | –                       | <a href="#">DContErr</a>       | –                              | <a href="#">PRBSerr</a> | <a href="#">KContErr</a> | <a href="#">FChkErr</a> | <a href="#">LCfgErr</a>        | <a href="#">ILAerr</a>   |

| ADDRESS            | NAME                                  | MSB                        |                           |                                |                         |                          |                         |                           | LSB                      |
|--------------------|---------------------------------------|----------------------------|---------------------------|--------------------------------|-------------------------|--------------------------|-------------------------|---------------------------|--------------------------|
|                    | <a href="#">StatRLane[23:16]</a>      | –                          | –                         | –                              | –                       | –                        | –                       | <a href="#">FIFOempty</a> | <a href="#">FIFOfull</a> |
|                    | <a href="#">StatRLane[15:8]</a>       | –                          | –                         | <a href="#">FIFODepth[5:0]</a> |                         |                          |                         |                           |                          |
|                    | <a href="#">StatRLane[7:0]</a>        | <a href="#">FrNSync</a>    | <a href="#">LnReAlign</a> | <a href="#">FrReAlign</a>      | –                       | –                        | <a href="#">DISP</a>    | <a href="#">NIT</a>       | <a href="#">CGS</a>      |
| <b>RLaneRegs 3</b> |                                       |                            |                           |                                |                         |                          |                         |                           |                          |
| 0x4B0              | <a href="#">CfgRLaneSet[31:24]</a>    | <a href="#">LnSrc[4:0]</a> |                           |                                |                         |                          | –                       | <a href="#">LkSel</a>     | <a href="#">LnEn</a>     |
|                    | <a href="#">CfgRLaneSet[23:16]</a>    | –                          | –                         | –                              | –                       | –                        | –                       | –                         | –                        |
|                    | <a href="#">CfgRLaneSet[15:8]</a>     | –                          | –                         | –                              | –                       | –                        | –                       | –                         | –                        |
|                    | <a href="#">CfgRLaneSet[7:0]</a>      | –                          | –                         | <a href="#">LID[4:0]</a>       |                         |                          |                         |                           | <a href="#">LnRst</a>    |
| 0x4B4              | <a href="#">CfgRLaneIntEn[31:24]</a>  | –                          | <a href="#">DContErr</a>  | –                              | <a href="#">PRBSerr</a> | <a href="#">KContErr</a> | <a href="#">FChkErr</a> | <a href="#">LCfgErr</a>   | <a href="#">ILAerr</a>   |
|                    | <a href="#">CfgRLaneIntEn[23:16]</a>  | –                          | –                         | –                              | –                       | –                        | –                       | <a href="#">FIFOempty</a> | <a href="#">FIFOfull</a> |
|                    | <a href="#">CfgRLaneIntEn[15:8]</a>   | –                          | –                         | –                              | –                       | –                        | –                       | –                         | –                        |
|                    | <a href="#">CfgRLaneIntEn[7:0]</a>    | <a href="#">FrNSync</a>    | <a href="#">LnReAlign</a> | <a href="#">FrReAlign</a>      | –                       | –                        | <a href="#">DISP</a>    | <a href="#">NIT</a>       | <a href="#">CGS</a>      |
| 0x4B8              | <a href="#">CfgRLaneMuteEn[31:24]</a> | –                          | <a href="#">DContErr</a>  | –                              | <a href="#">PRBSerr</a> | <a href="#">KContErr</a> | <a href="#">FChkErr</a> | <a href="#">LCfgErr</a>   | <a href="#">ILAerr</a>   |
|                    | <a href="#">CfgRLaneMuteEn[23:16]</a> | –                          | –                         | –                              | –                       | –                        | –                       | <a href="#">FIFOempty</a> | <a href="#">FIFOfull</a> |
|                    | <a href="#">CfgRLaneMuteEn[15:8]</a>  | –                          | –                         | –                              | –                       | –                        | –                       | –                         | –                        |
|                    | <a href="#">CfgRLaneMuteEn[7:0]</a>   | <a href="#">FrNSync</a>    | <a href="#">LnReAlign</a> | <a href="#">FrReAlign</a>      | –                       | –                        | <a href="#">DISP</a>    | <a href="#">NIT</a>       | <a href="#">CGS</a>      |
| 0x4BC              | <a href="#">StatRLane[31:24]</a>      | –                          | <a href="#">DContErr</a>  | –                              | <a href="#">PRBSerr</a> | <a href="#">KContErr</a> | <a href="#">FChkErr</a> | <a href="#">LCfgErr</a>   | <a href="#">ILAerr</a>   |
|                    | <a href="#">StatRLane[23:16]</a>      | –                          | –                         | –                              | –                       | –                        | –                       | <a href="#">FIFOempty</a> | <a href="#">FIFOfull</a> |
|                    | <a href="#">StatRLane[15:8]</a>       | –                          | –                         | <a href="#">FIFODepth[5:0]</a> |                         |                          |                         |                           |                          |
|                    | <a href="#">StatRLane[7:0]</a>        | <a href="#">FrNSync</a>    | <a href="#">LnReAlign</a> | <a href="#">FrReAlign</a>      | –                       | –                        | <a href="#">DISP</a>    | <a href="#">NIT</a>       | <a href="#">CGS</a>      |
| <b>RLaneRegs 4</b> |                                       |                            |                           |                                |                         |                          |                         |                           |                          |
| 0x4C0              | <a href="#">CfgRLaneSet[31:24]</a>    | <a href="#">LnSrc[4:0]</a> |                           |                                |                         |                          | –                       | <a href="#">LkSel</a>     | <a href="#">LnEn</a>     |
|                    | <a href="#">CfgRLaneSet[23:16]</a>    | –                          | –                         | –                              | –                       | –                        | –                       | –                         | –                        |
|                    | <a href="#">CfgRLaneSet[15:8]</a>     | –                          | –                         | –                              | –                       | –                        | –                       | –                         | –                        |
|                    | <a href="#">CfgRLaneSet[7:0]</a>      | –                          | –                         | <a href="#">LID[4:0]</a>       |                         |                          |                         |                           | <a href="#">LnRst</a>    |
| 0x4C4              | <a href="#">CfgRLaneIntEn[31:24]</a>  | –                          | <a href="#">DContErr</a>  | –                              | <a href="#">PRBSerr</a> | <a href="#">KContErr</a> | <a href="#">FChkErr</a> | <a href="#">LCfgErr</a>   | <a href="#">ILAerr</a>   |
|                    | <a href="#">CfgRLaneIntEn[23:16]</a>  | –                          | –                         | –                              | –                       | –                        | –                       | <a href="#">FIFOempty</a> | <a href="#">FIFOfull</a> |
|                    | <a href="#">CfgRLaneIntEn[15:8]</a>   | –                          | –                         | –                              | –                       | –                        | –                       | –                         | –                        |
|                    | <a href="#">CfgRLaneIntEn[7:0]</a>    | <a href="#">FrNSync</a>    | <a href="#">LnReAlign</a> | <a href="#">FrReAlign</a>      | –                       | –                        | <a href="#">DISP</a>    | <a href="#">NIT</a>       | <a href="#">CGS</a>      |
| 0x4C8              | <a href="#">CfgRLaneMuteEn[31:24]</a> | –                          | <a href="#">DContErr</a>  | –                              | <a href="#">PRBSerr</a> | <a href="#">KContErr</a> | <a href="#">FChkErr</a> | <a href="#">LCfgErr</a>   | <a href="#">ILAerr</a>   |
|                    | <a href="#">CfgRLaneMuteEn[23:16]</a> | –                          | –                         | –                              | –                       | –                        | –                       | <a href="#">FIFOempty</a> | <a href="#">FIFOfull</a> |

| ADDRESS           | NAME                                   | MSB                           |                           |                                |                         |                          |                         |                                | LSB                      |
|-------------------|----------------------------------------|-------------------------------|---------------------------|--------------------------------|-------------------------|--------------------------|-------------------------|--------------------------------|--------------------------|
|                   | <a href="#">CfgRLaneMuteEn[15:8]</a>   | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgRLaneMuteEn[7:0]</a>    | <a href="#">FrNSync</a>       | <a href="#">LnReAlign</a> | <a href="#">FrReAlign</a>      | –                       | –                        | <a href="#">DISP</a>    | <a href="#">NIT</a>            | <a href="#">CGS</a>      |
| 0x4CC             | <a href="#">StatRLane[31:24]</a>       | –                             | <a href="#">DContErr</a>  | –                              | <a href="#">PRBSerr</a> | <a href="#">KContErr</a> | <a href="#">FChkErr</a> | <a href="#">LCfgErr</a>        | <a href="#">ILAerr</a>   |
|                   | <a href="#">StatRLane[23:16]</a>       | –                             | –                         | –                              | –                       | –                        | –                       | <a href="#">FIFOempty</a>      | <a href="#">FIFOfull</a> |
|                   | <a href="#">StatRLane[15:8]</a>        | –                             | –                         | <a href="#">FIFODepth[5:0]</a> |                         |                          |                         |                                |                          |
|                   | <a href="#">StatRLane[7:0]</a>         | <a href="#">FrNSync</a>       | <a href="#">LnReAlign</a> | <a href="#">FrReAlign</a>      | –                       | –                        | <a href="#">DISP</a>    | <a href="#">NIT</a>            | <a href="#">CGS</a>      |
| <b>SerDesRegs</b> |                                        |                               |                           |                                |                         |                          |                         |                                |                          |
| 0x600             | <a href="#">CfgSerDes[31:24]</a>       | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgSerDes[23:16]</a>       | –                             | –                         | –                              | –                       | –                        | –                       | <a href="#">RxRateSel[1:0]</a> |                          |
|                   | <a href="#">CfgSerDes[15:8]</a>        | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgSerDes[7:0]</a>         | <a href="#">PhyWMode[1:0]</a> |                           | <a href="#">BCast[1:0]</a>     |                         | –                        | <a href="#">PhyKill</a> | –                              | <a href="#">Rst</a>      |
| 0x608             | <a href="#">CfgTrainAct[31:24]</a>     | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgTrainAct[23:16]</a>     | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgTrainAct[15:8]</a>      | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgTrainAct[7:0]</a>       | –                             | –                         | –                              | <a href="#">Ln_4</a>    | <a href="#">Ln_3</a>     | <a href="#">Ln_2</a>    | <a href="#">Ln_1</a>           | <a href="#">Ln_0</a>     |
| 0x60C             | <a href="#">CfgTrainDeAct[31:24]</a>   | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgTrainDeAct[23:16]</a>   | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgTrainDeAct[15:8]</a>    | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgTrainDeAct[7:0]</a>     | –                             | –                         | –                              | <a href="#">Ln_4</a>    | <a href="#">Ln_3</a>     | <a href="#">Ln_2</a>    | <a href="#">Ln_1</a>           | <a href="#">Ln_0</a>     |
| 0x610             | <a href="#">CfgIdleGate[31:24]</a>     | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgIdleGate[23:16]</a>     | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgIdleGate[15:8]</a>      | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgIdleGate[7:0]</a>       | –                             | –                         | –                              | <a href="#">Ln_4</a>    | <a href="#">Ln_3</a>     | <a href="#">Ln_2</a>    | <a href="#">Ln_1</a>           | <a href="#">Ln_0</a>     |
| 0x614             | <a href="#">CfgDoneGate[31:24]</a>     | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgDoneGate[23:16]</a>     | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgDoneGate[15:8]</a>      | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgDoneGate[7:0]</a>       | –                             | –                         | –                              | <a href="#">Ln_4</a>    | <a href="#">Ln_3</a>     | <a href="#">Ln_2</a>    | <a href="#">Ln_1</a>           | <a href="#">Ln_0</a>     |
| 0x618             | <a href="#">CfgReserved[31:24]</a>     | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgReserved[23:16]</a>     | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgReserved[15:8]</a>      | <a href="#">Rsvd[15:8]</a>    |                           |                                |                         |                          |                         |                                |                          |
|                   | <a href="#">CfgReserved[7:0]</a>       | <a href="#">Rsvd[7:0]</a>     |                           |                                |                         |                          |                         |                                |                          |
| 0x61C             | <a href="#">CfgIntEnRLMS[31:24]</a>    | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgIntEnRLMS[23:16]</a>    | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgIntEnRLMS[15:8]</a>     | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgIntEnRLMS[7:0]</a>      | –                             | –                         | –                              | <a href="#">Ln_4</a>    | <a href="#">Ln_3</a>     | <a href="#">Ln_2</a>    | <a href="#">Ln_1</a>           | <a href="#">Ln_0</a>     |
| 0x620             | <a href="#">CfgIntEnTrainDn[31:24]</a> | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgIntEnTrainDn[23:16]</a> | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgIntEnTrainDn[15:8]</a>  | –                             | –                         | –                              | –                       | –                        | –                       | –                              | –                        |
|                   | <a href="#">CfgIntEnTrainDn[7:0]</a>   | –                             | –                         | –                              | <a href="#">Ln_4</a>    | <a href="#">Ln_3</a>     | <a href="#">Ln_2</a>    | <a href="#">Ln_1</a>           | <a href="#">Ln_0</a>     |

| ADDRESS | NAME                                    | MSB                                 |                               |                               |                      |                              |                                 |                      | LSB                  |
|---------|-----------------------------------------|-------------------------------------|-------------------------------|-------------------------------|----------------------|------------------------------|---------------------------------|----------------------|----------------------|
| 0x624   | <a href="#">CfgIntEnSigDet[31:24]</a>   | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">CfgIntEnSigDet[23:16]</a>   | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">CfgIntEnSigDet[15:8]</a>    | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">CfgIntEnSigDet[7:0]</a>     | –                                   | –                             | –                             | <a href="#">Ln_4</a> | <a href="#">Ln_3</a>         | <a href="#">Ln_2</a>            | <a href="#">Ln_1</a> | <a href="#">Ln_0</a> |
| 0x628   | <a href="#">CfgMuteEnRLMS[31:24]</a>    | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">CfgMuteEnRLMS[23:16]</a>    | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">CfgMuteEnRLMS[15:8]</a>     | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">CfgMuteEnRLMS[7:0]</a>      | –                                   | –                             | –                             | <a href="#">Ln_4</a> | <a href="#">Ln_3</a>         | <a href="#">Ln_2</a>            | <a href="#">Ln_1</a> | <a href="#">Ln_0</a> |
| 0x62C   | <a href="#">CfgMuteEnTrainDn[31:24]</a> | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">CfgMuteEnTrainDn[23:16]</a> | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">CfgMuteEnTrainDn[15:8]</a>  | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">CfgMuteEnTrainDn[7:0]</a>   | –                                   | –                             | –                             | <a href="#">Ln_4</a> | <a href="#">Ln_3</a>         | <a href="#">Ln_2</a>            | <a href="#">Ln_1</a> | <a href="#">Ln_0</a> |
| 0x630   | <a href="#">CfgMuteEnSigDet[31:24]</a>  | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">CfgMuteEnSigDet[23:16]</a>  | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">CfgMuteEnSigDet[15:8]</a>   | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">CfgMuteEnSigDet[7:0]</a>    | –                                   | –                             | –                             | <a href="#">Ln_4</a> | <a href="#">Ln_3</a>         | <a href="#">Ln_2</a>            | <a href="#">Ln_1</a> | <a href="#">Ln_0</a> |
| 0x634   | <a href="#">StatRLMS[31:24]</a>         | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">StatRLMS[23:16]</a>         | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">StatRLMS[15:8]</a>          | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">StatRLMS[7:0]</a>           | –                                   | –                             | –                             | <a href="#">Ln_4</a> | <a href="#">Ln_3</a>         | <a href="#">Ln_2</a>            | <a href="#">Ln_1</a> | <a href="#">Ln_0</a> |
| 0x638   | <a href="#">StatTrainDn[31:24]</a>      | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">StatTrainDn[23:16]</a>      | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">StatTrainDn[15:8]</a>       | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">StatTrainDn[7:0]</a>        | –                                   | –                             | –                             | <a href="#">Ln_4</a> | <a href="#">Ln_3</a>         | <a href="#">Ln_2</a>            | <a href="#">Ln_1</a> | <a href="#">Ln_0</a> |
| 0x63C   | <a href="#">StatSigDet[31:24]</a>       | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">StatSigDet[23:16]</a>       | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">StatSigDet[15:8]</a>        | –                                   | –                             | –                             | –                    | –                            | –                               | –                    | –                    |
|         | <a href="#">StatSigDet[7:0]</a>         | –                                   | –                             | –                             | <a href="#">Ln_4</a> | <a href="#">Ln_3</a>         | <a href="#">Ln_2</a>            | <a href="#">Ln_1</a> | <a href="#">Ln_0</a> |
| CMURegs |                                         |                                     |                               |                               |                      |                              |                                 |                      |                      |
| 0x644   | <a href="#">CfgCMU1[31:24]</a>          | <a href="#">Rsvd1</a>               | –                             | –                             | –                    | –                            | <a href="#">cd_tune1p0[2:0]</a> |                      |                      |
|         | <a href="#">CfgCMU1[23:16]</a>          | <a href="#">Cref_divsel1p0[1:0]</a> |                               | –                             | –                    | <a href="#">Rsvd0[13:10]</a> |                                 |                      |                      |
|         | <a href="#">CfgCMU1[15:8]</a>           | <a href="#">Rsvd0[9:2]</a>          |                               |                               |                      |                              |                                 |                      |                      |
|         | <a href="#">CfgCMU1[7:0]</a>            | <a href="#">Rsvd0[1:0]</a>          |                               | <a href="#">FBDIV[1:0]</a>    |                      | <a href="#">VCOSSEL[1:0]</a> |                                 | –                    | –                    |
| PHY 0   |                                         |                                     |                               |                               |                      |                              |                                 |                      |                      |
| 0x80C   | <a href="#">EQU_CTRL3[31:24]</a>        | –                                   | –                             | <a href="#">D1_coeff[5:0]</a> |                      |                              |                                 |                      |                      |
|         | <a href="#">EQU_CTRL3[23:16]</a>        | –                                   | <a href="#">D2_coeff[6:0]</a> |                               |                      |                              |                                 |                      |                      |
|         | <a href="#">EQU_CTRL3[15:8]</a>         | –                                   | <a href="#">D3_coeff[6:0]</a> |                               |                      |                              |                                 |                      |                      |

## MAX5855

16-Bit, 4.9Gbps Wideband Interpolating  
and Modulating RF DAC with JESD204B Interface

| ADDRESS | NAME                             | MSB                               |                                  |                                  |   |                             |                              |                                | LSB |
|---------|----------------------------------|-----------------------------------|----------------------------------|----------------------------------|---|-----------------------------|------------------------------|--------------------------------|-----|
|         | <a href="#">EQU_CTRL3[7:0]</a>   | –                                 | <a href="#">D4_coeff[6:0]</a>    |                                  |   |                             |                              |                                |     |
| 0x810   | <a href="#">EQU_CTRL4[31:24]</a> | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EQU_CTRL4[23:16]</a> | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EQU_CTRL4[15:8]</a>  | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EQU_CTRL4[7:0]</a>   | <a href="#">AGC_coeff[7:0]</a>    |                                  |                                  |   |                             |                              |                                |     |
| 0x81C   | <a href="#">EQU_CTRL7[31:24]</a> | <a href="#">AGC_init_D1[7:0]</a>  |                                  |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRL7[23:16]</a> | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EQU_CTRL7[15:8]</a>  | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EQU_CTRL7[7:0]</a>   | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
| 0x828   | <a href="#">EQU_CTRLA[31:24]</a> | –                                 | –                                | <a href="#">D1_init[5:0]</a>     |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLA[23:16]</a> | –                                 | <a href="#">D2_init[6:0]</a>     |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLA[15:8]</a>  | –                                 | <a href="#">D3_init[6:0]</a>     |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLA[7:0]</a>   | –                                 | <a href="#">D4_init[6:0]</a>     |                                  |   |                             |                              |                                |     |
| 0x82C   | <a href="#">EQU_CTRLB[31:24]</a> | –                                 | –                                | –                                | – | <a href="#">capsel[1:0]</a> |                              | <a href="#">Mode6G<br/>phb</a> | –   |
|         | <a href="#">EQU_CTRLB[23:16]</a> | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EQU_CTRLB[15:8]</a>  | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EQU_CTRLB[7:0]</a>   | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
| 0x83C   | <a href="#">EYE_MON2[31:24]</a>  | <a href="#">D1ErrChPhPri[7:0]</a> |                                  |                                  |   |                             |                              |                                |     |
|         | <a href="#">EYE_MON2[23:16]</a>  | <a href="#">D1ErrChPhSec[7:0]</a> |                                  |                                  |   |                             |                              |                                |     |
|         | <a href="#">EYE_MON2[15:8]</a>   | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EYE_MON2[7:0]</a>    | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
| 0x864   | <a href="#">TX_CTRL1[31:24]</a>  | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">TX_CTRL1[23:16]</a>  | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">TX_CTRL1[15:8]</a>   | –                                 | –                                | –                                | – | –                           | <a href="#">cd_tune[2:0]</a> |                                |     |
|         | <a href="#">TX_CTRL1[7:0]</a>    | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
| 0x880   | <a href="#">EQU_CTRLD[31:24]</a> | –                                 | –                                | <a href="#">DFE2_initD3[5:0]</a> |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLD[23:16]</a> | –                                 | <a href="#">DFE2_initD2[6:0]</a> |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLD[15:8]</a>  | –                                 | <a href="#">DFE1_initD3[6:0]</a> |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLD[7:0]</a>   | –                                 | <a href="#">DFE1_initD2[6:0]</a> |                                  |   |                             |                              |                                |     |
| 0x884   | <a href="#">EQU_CTRLF[31:24]</a> | –                                 | <a href="#">DFE4Init_D3[6:0]</a> |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLF[23:16]</a> | –                                 | <a href="#">DFE4Init_D2[6:0]</a> |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLF[15:8]</a>  | –                                 | <a href="#">DFE3Init_D3[6:0]</a> |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLF[7:0]</a>   | –                                 | <a href="#">DFE3Init_D2[6:0]</a> |                                  |   |                             |                              |                                |     |
| 0x88C   | <a href="#">EQU_CTRLG[31:24]</a> | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EQU_CTRLG[23:16]</a> | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EQU_CTRLG[15:8]</a>  | <a href="#">AGCInit_D3[7:0]</a>   |                                  |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLG[7:0]</a>   | <a href="#">AGCInit_D2[7:0]</a>   |                                  |                                  |   |                             |                              |                                |     |
| PHY 1   |                                  |                                   |                                  |                                  |   |                             |                              |                                |     |
| 0x90C   | <a href="#">EQU_CTRL3[31:24]</a> | –                                 | –                                | <a href="#">D1_coeff[5:0]</a>    |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRL3[23:16]</a> | –                                 | <a href="#">D2_coeff[6:0]</a>    |                                  |   |                             |                              |                                |     |

## MAX5855

16-Bit, 4.9Gbps Wideband Interpolating  
and Modulating RF DAC with JESD204B Interface

| ADDRESS | NAME                              | MSB                               |                                  |                                  |   |                             |                              |                                | LSB |
|---------|-----------------------------------|-----------------------------------|----------------------------------|----------------------------------|---|-----------------------------|------------------------------|--------------------------------|-----|
|         | <a href="#">EQU_CTRL3[15:8]</a>   | —                                 | <a href="#">D3_coeff[6:0]</a>    |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRL3[7:0]</a>    | —                                 | <a href="#">D4_coeff[6:0]</a>    |                                  |   |                             |                              |                                |     |
| 0x910   | <a href="#">EQU_CTRL4[31:24]</a>  | —                                 | —                                | —                                | — | —                           | —                            | —                              | —   |
|         | <a href="#">EQU_CTRL4[23:16]</a>  | —                                 | —                                | —                                | — | —                           | —                            | —                              | —   |
|         | <a href="#">EQU_CTRL4[15:8]</a>   | —                                 | —                                | —                                | — | —                           | —                            | —                              | —   |
|         | <a href="#">EQU_CTRL4[7:0]</a>    | <a href="#">AGC_coeff[7:0]</a>    |                                  |                                  |   |                             |                              |                                |     |
| 0x91C   | <a href="#">EQU_CTRL7[31:24]</a>  | <a href="#">AGC_init_D1[7:0]</a>  |                                  |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRL7[23:16]</a>  | —                                 | —                                | —                                | — | —                           | —                            | —                              | —   |
|         | <a href="#">EQU_CTRL7[15:8]</a>   | —                                 | —                                | —                                | — | —                           | —                            | —                              | —   |
|         | <a href="#">EQU_CTRL7[7:0]</a>    | —                                 | —                                | —                                | — | —                           | —                            | —                              | —   |
| 0x928   | <a href="#">EQU_CTRLA[31:24]</a>  | —                                 | —                                | <a href="#">D1_init[5:0]</a>     |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLA[23:16]</a>  | —                                 | <a href="#">D2_init[6:0]</a>     |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLA[15:8]</a>   | —                                 | <a href="#">D3_init[6:0]</a>     |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLA[7:0]</a>    | —                                 | <a href="#">D4_init[6:0]</a>     |                                  |   |                             |                              |                                |     |
| 0x92C   | <a href="#">EQU_CTRLB[31:24]</a>  | —                                 | —                                | —                                | — | <a href="#">capsel[1:0]</a> |                              | <a href="#">Mode6G<br/>phb</a> | —   |
|         | <a href="#">EQU_CTRLB[23:16]</a>  | —                                 | —                                | —                                | — | —                           | —                            | —                              | —   |
|         | <a href="#">EQU_CTRLB[15:8]</a>   | —                                 | —                                | —                                | — | —                           | —                            | —                              | —   |
|         | <a href="#">EQU_CTRLB[7:0]</a>    | —                                 | —                                | —                                | — | —                           | —                            | —                              | —   |
| 0x93C   | <a href="#">EYE_MON2[31:24]</a>   | <a href="#">D1ErrChPhPri[7:0]</a> |                                  |                                  |   |                             |                              |                                |     |
|         | <a href="#">EYE_MON2[23:16]</a>   | <a href="#">D1ErrChPhSec[7:0]</a> |                                  |                                  |   |                             |                              |                                |     |
|         | <a href="#">EYE_MON2[15:8]</a>    | —                                 | —                                | —                                | — | —                           | —                            | —                              | —   |
|         | <a href="#">EYE_MON2[7:0]</a>     | —                                 | —                                | —                                | — | —                           | —                            | —                              | —   |
| 0x964   | <a href="#">TX_CTRL1[31:24]</a>   | —                                 | —                                | —                                | — | —                           | —                            | —                              | —   |
|         | <a href="#">TX_CTRL1[23:16]</a>   | —                                 | —                                | —                                | — | —                           | —                            | —                              | —   |
|         | <a href="#">TX_CTRL1[15:8]</a>    | —                                 | —                                | —                                | — | —                           | <a href="#">cd_tune[2:0]</a> |                                |     |
|         | <a href="#">TX_CTRL1[7:0]</a>     | —                                 | —                                | —                                | — | —                           | —                            | —                              | —   |
| 0x980   | <a href="#">EQU_CTRLD[31:24]</a>  | —                                 | —                                | <a href="#">DFE2_initD3[5:0]</a> |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLD[23:16]</a>  | —                                 | <a href="#">DFE2_initD2[6:0]</a> |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLD[15:8]</a>   | —                                 | <a href="#">DFE1_initD3[6:0]</a> |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLD[7:0]</a>    | —                                 | <a href="#">DFE1_initD2[6:0]</a> |                                  |   |                             |                              |                                |     |
| 0x984   | <a href="#">EQU_CTRL_E[31:24]</a> | —                                 | <a href="#">DFE4Init_D3[6:0]</a> |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRL_E[23:16]</a> | —                                 | <a href="#">DFE4Init_D2[6:0]</a> |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRL_E[15:8]</a>  | —                                 | <a href="#">DFE3Init_D3[6:0]</a> |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRL_E[7:0]</a>   | —                                 | <a href="#">DFE3Init_D2[6:0]</a> |                                  |   |                             |                              |                                |     |
| 0x98C   | <a href="#">EQU_CTRLG[31:24]</a>  | —                                 | —                                | —                                | — | —                           | —                            | —                              | —   |
|         | <a href="#">EQU_CTRLG[23:16]</a>  | —                                 | —                                | —                                | — | —                           | —                            | —                              | —   |
|         | <a href="#">EQU_CTRLG[15:8]</a>   | <a href="#">AGCInit_D3[7:0]</a>   |                                  |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLG[7:0]</a>    | <a href="#">AGCInit_D2[7:0]</a>   |                                  |                                  |   |                             |                              |                                |     |
| PHY 2   |                                   |                                   |                                  |                                  |   |                             |                              |                                |     |
| 0xA0C   | <a href="#">EQU_CTRL3[31:24]</a>  | —                                 | —                                | <a href="#">D1_coeff[5:0]</a>    |   |                             |                              |                                |     |

| ADDRESS | NAME                             | MSB                               |                                  |                                  |   |                             |                              |                                | LSB |
|---------|----------------------------------|-----------------------------------|----------------------------------|----------------------------------|---|-----------------------------|------------------------------|--------------------------------|-----|
|         | <a href="#">EQU_CTRL3[23:16]</a> | –                                 | <a href="#">D2_coeff[6:0]</a>    |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRL3[15:8]</a>  | –                                 | <a href="#">D3_coeff[6:0]</a>    |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRL3[7:0]</a>   | –                                 | <a href="#">D4_coeff[6:0]</a>    |                                  |   |                             |                              |                                |     |
| 0xA10   | <a href="#">EQU_CTRL4[31:24]</a> | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EQU_CTRL4[23:16]</a> | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EQU_CTRL4[15:8]</a>  | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EQU_CTRL4[7:0]</a>   | <a href="#">AGC_coeff[7:0]</a>    |                                  |                                  |   |                             |                              |                                |     |
| 0xA1C   | <a href="#">EQU_CTRL7[31:24]</a> | <a href="#">AGC_init_D1[7:0]</a>  |                                  |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRL7[23:16]</a> | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EQU_CTRL7[15:8]</a>  | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EQU_CTRL7[7:0]</a>   | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
| 0xA28   | <a href="#">EQU_CTRLA[31:24]</a> | –                                 | –                                | <a href="#">D1_init[5:0]</a>     |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLA[23:16]</a> | –                                 | <a href="#">D2_init[6:0]</a>     |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLA[15:8]</a>  | –                                 | <a href="#">D3_init[6:0]</a>     |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLA[7:0]</a>   | –                                 | <a href="#">D4_init[6:0]</a>     |                                  |   |                             |                              |                                |     |
| 0xA2C   | <a href="#">EQU_CTRLB[31:24]</a> | –                                 | –                                | –                                | – | <a href="#">capsel[1:0]</a> |                              | <a href="#">Mode6G<br/>phb</a> | –   |
|         | <a href="#">EQU_CTRLB[23:16]</a> | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EQU_CTRLB[15:8]</a>  | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EQU_CTRLB[7:0]</a>   | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
| 0xA3C   | <a href="#">EYE_MON2[31:24]</a>  | <a href="#">D1ErrChPhPri[7:0]</a> |                                  |                                  |   |                             |                              |                                |     |
|         | <a href="#">EYE_MON2[23:16]</a>  | <a href="#">D1ErrChPhSec[7:0]</a> |                                  |                                  |   |                             |                              |                                |     |
|         | <a href="#">EYE_MON2[15:8]</a>   | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EYE_MON2[7:0]</a>    | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
| 0xA64   | <a href="#">TX_CTRL1[31:24]</a>  | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">TX_CTRL1[23:16]</a>  | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">TX_CTRL1[15:8]</a>   | –                                 | –                                | –                                | – | –                           | <a href="#">cd_tune[2:0]</a> |                                |     |
|         | <a href="#">TX_CTRL1[7:0]</a>    | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
| 0xA80   | <a href="#">EQU_CTRLD[31:24]</a> | –                                 | –                                | <a href="#">DFE2_initD3[5:0]</a> |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLD[23:16]</a> | –                                 | <a href="#">DFE2_initD2[6:0]</a> |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLD[15:8]</a>  | –                                 | <a href="#">DFE1_initD3[6:0]</a> |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLD[7:0]</a>   | –                                 | <a href="#">DFE1_initD2[6:0]</a> |                                  |   |                             |                              |                                |     |
| 0xA84   | <a href="#">EQU_CTRLF[31:24]</a> | –                                 | <a href="#">DFE4Init_D3[6:0]</a> |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLF[23:16]</a> | –                                 | <a href="#">DFE4Init_D2[6:0]</a> |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLF[15:8]</a>  | –                                 | <a href="#">DFE3Init_D3[6:0]</a> |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLF[7:0]</a>   | –                                 | <a href="#">DFE3Init_D2[6:0]</a> |                                  |   |                             |                              |                                |     |
| 0xA8C   | <a href="#">EQU_CTRLG[31:24]</a> | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EQU_CTRLG[23:16]</a> | –                                 | –                                | –                                | – | –                           | –                            | –                              | –   |
|         | <a href="#">EQU_CTRLG[15:8]</a>  | <a href="#">AGCInit_D3[7:0]</a>   |                                  |                                  |   |                             |                              |                                |     |
|         | <a href="#">EQU_CTRLG[7:0]</a>   | <a href="#">AGCInit_D2[7:0]</a>   |                                  |                                  |   |                             |                              |                                |     |
| PHY 3   |                                  |                                   |                                  |                                  |   |                             |                              |                                |     |

| ADDRESS | NAME                             | MSB |   |   |   |   |                             |                                   | LSB |
|---------|----------------------------------|-----|---|---|---|---|-----------------------------|-----------------------------------|-----|
| 0xB0C   | <a href="#">EQU_CTRL3[31:24]</a> | –   | – |   |   |   |                             | <a href="#">D1_coeff[5:0]</a>     |     |
|         | <a href="#">EQU_CTRL3[23:16]</a> | –   |   |   |   |   |                             | <a href="#">D2_coeff[6:0]</a>     |     |
|         | <a href="#">EQU_CTRL3[15:8]</a>  | –   |   |   |   |   |                             | <a href="#">D3_coeff[6:0]</a>     |     |
|         | <a href="#">EQU_CTRL3[7:0]</a>   | –   |   |   |   |   |                             | <a href="#">D4_coeff[6:0]</a>     |     |
| 0xB10   | <a href="#">EQU_CTRL4[31:24]</a> | –   | – | – | – | – | –                           | –                                 | –   |
|         | <a href="#">EQU_CTRL4[23:16]</a> | –   | – | – | – | – | –                           | –                                 | –   |
|         | <a href="#">EQU_CTRL4[15:8]</a>  | –   | – | – | – | – | –                           | –                                 | –   |
|         | <a href="#">EQU_CTRL4[7:0]</a>   |     |   |   |   |   |                             | <a href="#">AGC_coeff[7:0]</a>    |     |
| 0xB1C   | <a href="#">EQU_CTRL7[31:24]</a> |     |   |   |   |   |                             | <a href="#">AGC_init_D1[7:0]</a>  |     |
|         | <a href="#">EQU_CTRL7[23:16]</a> | –   | – | – | – | – | –                           | –                                 | –   |
|         | <a href="#">EQU_CTRL7[15:8]</a>  | –   | – | – | – | – | –                           | –                                 | –   |
|         | <a href="#">EQU_CTRL7[7:0]</a>   | –   | – | – | – | – | –                           | –                                 | –   |
| 0xB28   | <a href="#">EQU_CTRLA[31:24]</a> | –   | – |   |   |   |                             | <a href="#">D1_init[5:0]</a>      |     |
|         | <a href="#">EQU_CTRLA[23:16]</a> | –   |   |   |   |   |                             | <a href="#">D2_init[6:0]</a>      |     |
|         | <a href="#">EQU_CTRLA[15:8]</a>  | –   |   |   |   |   |                             | <a href="#">D3_init[6:0]</a>      |     |
|         | <a href="#">EQU_CTRLA[7:0]</a>   | –   |   |   |   |   |                             | <a href="#">D4_init[6:0]</a>      |     |
| 0xB2C   | <a href="#">EQU_CTRLB[31:24]</a> | –   | – | – | – |   | <a href="#">capsel[1:0]</a> | <a href="#">Mode6G<br/>phb</a>    | –   |
|         | <a href="#">EQU_CTRLB[23:16]</a> | –   | – | – | – | – | –                           | –                                 | –   |
|         | <a href="#">EQU_CTRLB[15:8]</a>  | –   | – | – | – | – | –                           | –                                 | –   |
|         | <a href="#">EQU_CTRLB[7:0]</a>   | –   | – | – | – | – | –                           | –                                 | –   |
| 0xB3C   | <a href="#">EYE_MON2[31:24]</a>  |     |   |   |   |   |                             | <a href="#">D1ErrChPhPri[7:0]</a> |     |
|         | <a href="#">EYE_MON2[23:16]</a>  |     |   |   |   |   |                             | <a href="#">D1ErrChPhSec[7:0]</a> |     |
|         | <a href="#">EYE_MON2[15:8]</a>   | –   | – | – | – | – | –                           | –                                 | –   |
|         | <a href="#">EYE_MON2[7:0]</a>    | –   | – | – | – | – | –                           | –                                 | –   |
| 0xB64   | <a href="#">TX_CTRL1[31:24]</a>  | –   | – | – | – | – | –                           | –                                 | –   |
|         | <a href="#">TX_CTRL1[23:16]</a>  | –   | – | – | – | – | –                           | –                                 | –   |
|         | <a href="#">TX_CTRL1[15:8]</a>   | –   | – | – | – | – |                             | <a href="#">cd_tune[2:0]</a>      |     |
|         | <a href="#">TX_CTRL1[7:0]</a>    | –   | – | – | – | – | –                           | –                                 | –   |
| 0xB80   | <a href="#">EQU_CTRLD[31:24]</a> | –   | – |   |   |   |                             | <a href="#">DFE2_initD3[5:0]</a>  |     |
|         | <a href="#">EQU_CTRLD[23:16]</a> | –   |   |   |   |   |                             | <a href="#">DFE2_initD2[6:0]</a>  |     |
|         | <a href="#">EQU_CTRLD[15:8]</a>  | –   |   |   |   |   |                             | <a href="#">DFE1_initD3[6:0]</a>  |     |
|         | <a href="#">EQU_CTRLD[7:0]</a>   | –   |   |   |   |   |                             | <a href="#">DFE1_initD2[6:0]</a>  |     |
| 0xB84   | <a href="#">EQU_CTRLF[31:24]</a> | –   |   |   |   |   |                             | <a href="#">DFE4Init_D3[6:0]</a>  |     |
|         | <a href="#">EQU_CTRLF[23:16]</a> | –   |   |   |   |   |                             | <a href="#">DFE4Init_D2[6:0]</a>  |     |
|         | <a href="#">EQU_CTRLF[15:8]</a>  | –   |   |   |   |   |                             | <a href="#">DFE3Init_D3[6:0]</a>  |     |
|         | <a href="#">EQU_CTRLF[7:0]</a>   | –   |   |   |   |   |                             | <a href="#">DFE3Init_D2[6:0]</a>  |     |
| 0xB8C   | <a href="#">EQU_CTRLG[31:24]</a> | –   | – | – | – | – | –                           | –                                 | –   |
|         | <a href="#">EQU_CTRLG[23:16]</a> | –   | – | – | – | – | –                           | –                                 | –   |
|         | <a href="#">EQU_CTRLG[15:8]</a>  |     |   |   |   |   |                             | <a href="#">AGCInit_D3[7:0]</a>   |     |
|         | <a href="#">EQU_CTRLG[7:0]</a>   |     |   |   |   |   |                             | <a href="#">AGCInit_D2[7:0]</a>   |     |

| ADDRESS      | NAME                             | MSB |   |   |   |                                   |                                |                                  | LSB |
|--------------|----------------------------------|-----|---|---|---|-----------------------------------|--------------------------------|----------------------------------|-----|
| <b>PHY 4</b> |                                  |     |   |   |   |                                   |                                |                                  |     |
| 0xC0C        | <a href="#">EQU_CTRL3[31:24]</a> | –   | – |   |   |                                   |                                | <a href="#">D1_coeff[5:0]</a>    |     |
|              | <a href="#">EQU_CTRL3[23:16]</a> | –   |   |   |   |                                   |                                | <a href="#">D2_coeff[6:0]</a>    |     |
|              | <a href="#">EQU_CTRL3[15:8]</a>  | –   |   |   |   |                                   |                                | <a href="#">D3_coeff[6:0]</a>    |     |
|              | <a href="#">EQU_CTRL3[7:0]</a>   | –   |   |   |   |                                   |                                | <a href="#">D4_coeff[6:0]</a>    |     |
| 0xC10        | <a href="#">EQU_CTRL4[31:24]</a> | –   | – | – | – | –                                 | –                              | –                                | –   |
|              | <a href="#">EQU_CTRL4[23:16]</a> | –   | – | – | – | –                                 | –                              | –                                | –   |
|              | <a href="#">EQU_CTRL4[15:8]</a>  | –   | – | – | – | –                                 | –                              | –                                | –   |
|              | <a href="#">EQU_CTRL4[7:0]</a>   |     |   |   |   | <a href="#">AGC_coeff[7:0]</a>    |                                |                                  |     |
| 0xC1C        | <a href="#">EQU_CTRL7[31:24]</a> |     |   |   |   | <a href="#">AGC_init_D1[7:0]</a>  |                                |                                  |     |
|              | <a href="#">EQU_CTRL7[23:16]</a> | –   | – | – | – | –                                 | –                              | –                                | –   |
|              | <a href="#">EQU_CTRL7[15:8]</a>  | –   | – | – | – | –                                 | –                              | –                                | –   |
|              | <a href="#">EQU_CTRL7[7:0]</a>   | –   | – | – | – | –                                 | –                              | –                                | –   |
| 0xC28        | <a href="#">EQU_CTRLA[31:24]</a> | –   | – |   |   |                                   |                                | <a href="#">D1_init[5:0]</a>     |     |
|              | <a href="#">EQU_CTRLA[23:16]</a> | –   |   |   |   |                                   |                                | <a href="#">D2_init[6:0]</a>     |     |
|              | <a href="#">EQU_CTRLA[15:8]</a>  | –   |   |   |   |                                   |                                | <a href="#">D3_init[6:0]</a>     |     |
|              | <a href="#">EQU_CTRLA[7:0]</a>   | –   |   |   |   |                                   |                                | <a href="#">D4_init[6:0]</a>     |     |
| 0xC2C        | <a href="#">EQU_CTRLB[31:24]</a> | –   | – | – | – | <a href="#">capsel[1:0]</a>       | <a href="#">Mode6G<br/>phb</a> |                                  | –   |
|              | <a href="#">EQU_CTRLB[23:16]</a> | –   | – | – | – | –                                 | –                              | –                                | –   |
|              | <a href="#">EQU_CTRLB[15:8]</a>  | –   | – | – | – | –                                 | –                              | –                                | –   |
|              | <a href="#">EQU_CTRLB[7:0]</a>   | –   | – | – | – | –                                 | –                              | –                                | –   |
| 0xC3C        | <a href="#">EYE_MON2[31:24]</a>  |     |   |   |   | <a href="#">D1ErrChPhPri[7:0]</a> |                                |                                  |     |
|              | <a href="#">EYE_MON2[23:16]</a>  |     |   |   |   | <a href="#">D1ErrChPhSec[7:0]</a> |                                |                                  |     |
|              | <a href="#">EYE_MON2[15:8]</a>   | –   | – | – | – | –                                 | –                              | –                                | –   |
|              | <a href="#">EYE_MON2[7:0]</a>    | –   | – | – | – | –                                 | –                              | –                                | –   |
| 0xC64        | <a href="#">TX_CTRL1[31:24]</a>  | –   | – | – | – | –                                 | –                              | –                                | –   |
|              | <a href="#">TX_CTRL1[23:16]</a>  | –   | – | – | – | –                                 | –                              | –                                | –   |
|              | <a href="#">TX_CTRL1[15:8]</a>   | –   | – | – | – | –                                 |                                | <a href="#">cd_tune[2:0]</a>     |     |
|              | <a href="#">TX_CTRL1[7:0]</a>    | –   | – | – | – | –                                 | –                              | –                                | –   |
| 0xC80        | <a href="#">EQU_CTRLD[31:24]</a> | –   | – |   |   |                                   |                                | <a href="#">DFE2_initD3[5:0]</a> |     |
|              | <a href="#">EQU_CTRLD[23:16]</a> | –   |   |   |   |                                   |                                | <a href="#">DFE2_initD2[6:0]</a> |     |
|              | <a href="#">EQU_CTRLD[15:8]</a>  | –   |   |   |   |                                   |                                | <a href="#">DFE1_initD3[6:0]</a> |     |
|              | <a href="#">EQU_CTRLD[7:0]</a>   | –   |   |   |   |                                   |                                | <a href="#">DFE1_initD2[6:0]</a> |     |
| 0xC84        | <a href="#">EQU_CTRLF[31:24]</a> | –   |   |   |   |                                   |                                | <a href="#">DFE4Init_D3[6:0]</a> |     |
|              | <a href="#">EQU_CTRLF[23:16]</a> | –   |   |   |   |                                   |                                | <a href="#">DFE4Init_D2[6:0]</a> |     |
|              | <a href="#">EQU_CTRLF[15:8]</a>  | –   |   |   |   |                                   |                                | <a href="#">DFE3Init_D3[6:0]</a> |     |
|              | <a href="#">EQU_CTRLF[7:0]</a>   | –   |   |   |   |                                   |                                | <a href="#">DFE3Init_D2[6:0]</a> |     |
| 0xC8C        | <a href="#">EQU_CTRLG[31:24]</a> | –   | – | – | – | –                                 | –                              | –                                | –   |
|              | <a href="#">EQU_CTRLG[23:16]</a> | –   | – | – | – | –                                 | –                              | –                                | –   |
|              | <a href="#">EQU_CTRLG[15:8]</a>  |     |   |   |   | <a href="#">AGCInit_D3[7:0]</a>   |                                |                                  |     |

| ADDRESS | NAME                           | MSB                             |  |  |  |  |  | LSB |
|---------|--------------------------------|---------------------------------|--|--|--|--|--|-----|
|         | <a href="#">EQU_CTRLG[7:0]</a> | <a href="#">AGClnit_D2[7:0]</a> |  |  |  |  |  |     |

## Register Details

### [CfglFA \(0x00\)](#)

Configure Interface A

| BIT         | 7                      | 6                    | 5                       | 4                     | 3                       | 2                        | 1                     | 0                       |
|-------------|------------------------|----------------------|-------------------------|-----------------------|-------------------------|--------------------------|-----------------------|-------------------------|
| Field       | <a href="#">SftRst</a> | <a href="#">LSBF</a> | <a href="#">AddIncr</a> | <a href="#">Wire4</a> | <a href="#">Wire4_0</a> | <a href="#">AddIncr0</a> | <a href="#">LSBF0</a> | <a href="#">SftRst0</a> |
| Reset       | 0b0                    | 0b0                  | 0b0                     | 0b0                   | 0b0                     | 0b0                      | 0b0                   | 0b0                     |
| Access Type | Write 1 to Clear, Read | Write, Read          | Write, Read             | Write, Read           | Write, Read             | Write, Read              | Write, Read           | Write 1 to Clear, Read  |

| BITFIELD | BITS | DESCRIPTION                                                                                                          | DECODE                                                                                                           |
|----------|------|----------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|
| SftRst   | 7    | Writing a 1 to this bit resets everything except address 0x0000, 0x0001 and SPI interface. This bit is self clearing |                                                                                                                  |
| LSBF     | 6    | Select MSB-LSB first data format                                                                                     | 0x0: MSB first for input control/data and output data<br>0x1: LSB first for input control/data nad output data   |
| AddIncr  | 5    | Configure the auto-increment or decrement for address in burst mode                                                  | 0x0: Decrement address for SPI burst mode<br>0x1: Increment address for SPI burst mode                           |
| Wire4    | 4    | Configure 3 or 4 wire SPI mode                                                                                       | 0x0: 3-Wire SPI mode, SDI used for both input and output<br>0x1: 4-Wire SPI mode, SDI is input and SDO is output |
| Wire4_0  | 3    | Same as Bit4 and both should have the same value                                                                     |                                                                                                                  |
| AddIncr0 | 2    | Same as Bit5 and both should have the same value                                                                     |                                                                                                                  |
| LSBF0    | 1    | Same as Bit6 and both should have the same value                                                                     |                                                                                                                  |
| SftRst0  | 0    | Same as Bit7 and both should have the same value                                                                     |                                                                                                                  |

### [CfglFB \(0x01\)](#)

Configure Interface B

| BIT         | 7                       | 6                     | 5 | 4                     | 3                     | 2 | 1 | 0                     |
|-------------|-------------------------|-----------------------|---|-----------------------|-----------------------|---|---|-----------------------|
| Field       | <a href="#">StrmDis</a> | <a href="#">rsvd6</a> | – | <a href="#">rsvd4</a> | <a href="#">rsvd3</a> | – | – | <a href="#">rsvd0</a> |
| Reset       | 0b0                     | 0b0                   | – | 0b0                   | 0b0                   | – | – | 0b0                   |
| Access Type | Write, Read             | Write, Read           | – | Write, Read           | Write, Read           | – | – | Write, Read           |

| BITFIELD | BITS | DESCRIPTION                  | DECODE                                                                        |
|----------|------|------------------------------|-------------------------------------------------------------------------------|
| StrmDis  | 7    | Configure the Burst SPI mode | 0x0: SPI Streaming mode is enabled<br>0x1: SPI Streaming mode is disabled and |

| BITFIELD | BITS | DESCRIPTION  | DECODE                                       |
|----------|------|--------------|----------------------------------------------|
|          |      |              | continued CSB forces instruction-data format |
| rsvd6    | 6    | Reserved Bit |                                              |
| rsvd4    | 4    | Reserved Bit |                                              |
| rsvd3    | 3    | Reserved Bit |                                              |
| rsvd0    | 0    | Reserved Bit |                                              |

**CfgDev (0x02)**

## Device Configuration

| BIT         | 7           | 6 | 5 | 4 | 3 | 2           | 1           | 0 |
|-------------|-------------|---|---|---|---|-------------|-------------|---|
| Field       | rsvd[4:0]   |   |   |   |   | CDrst       | PDM[1:0]    |   |
| Reset       | 0x0         |   |   |   |   | 0b0         | 0x0         |   |
| Access Type | Write, Read |   |   |   |   | Write, Read | Write, Read |   |

| BITFIELD | BITS | DESCRIPTION                    | DECODE                                                                                                                                                                                                                                                                                                                                    |
|----------|------|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| rsvd     | 7:3  | Reserved Bits                  |                                                                                                                                                                                                                                                                                                                                           |
| CDrst    | 2    | Clock Divider Reset            | 0x0: Clock Divider is not reset<br>0x1: Clock Divider is reset                                                                                                                                                                                                                                                                            |
| PDM      | 1:0  | Power-Down Modes Configuration | 0x0: Normal operation mode<br>0x1: (Optional) Low power normal operation with reduced power and corresponding performance<br>0x2: (Optional) Medium power standby mode, non-operational but return to full operation in minimum amount of time<br>0x3: Sleep mode with lowest power dissipation with chip inactivity except SPI interface |

**ChipType (0x03)**

## Chip Type Status

| BIT         | 7 | 6 | 5 | 4 | 3         | 2 | 1 | 0 |
|-------------|---|---|---|---|-----------|---|---|---|
| Field       | – | – | – | – | Type[3:0] |   |   |   |
| Reset       | – | – | – | – | 0x4       |   |   |   |
| Access Type | – | – | – | – | Read Only |   |   |   |

| BITFIELD | BITS | DESCRIPTION      | DECODE                                                                                                                                                                         |
|----------|------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Type     | 3:0  | Chip Type Status | 0x0: Not Assigned<br>0x1: RF<br>0x2: IF<br>0x3: High-Speed ADC<br>0x4: High-Speed DAC<br>0x5: Clock Buffer<br>0x6: PLL<br>0x7: Precision ADC<br>0x8: Precision DAC<br>0x9: RAD |

| BITFIELD | BITS | DESCRIPTION | DECODE                                                                                                 |
|----------|------|-------------|--------------------------------------------------------------------------------------------------------|
|          |      |             | 0xA: Reserved<br>0xB: Reserved<br>0xC: Reserved<br>0xD: Reserved<br>0xE: Reserved<br>0xF: Not Assigned |

**ChipID1 (0x04)**

Chip ID LSB

| BIT         | 7           | 6 | 5         | 4 | 3         | 2 | 1 | 0 |
|-------------|-------------|---|-----------|---|-----------|---|---|---|
| Field       | CIDLSB[1:0] |   | PID[1:0]  |   | FID[3:0]  |   |   |   |
| Reset       | 0x0         |   | 0x0       |   | 0x0       |   |   |   |
| Access Type | Read Only   |   | Read Only |   | Read Only |   |   |   |

| BITFIELD | BITS | DESCRIPTION                  |
|----------|------|------------------------------|
| CIDLSB   | 7:6  | Product Unique Chip ID-2LSB  |
| PID      | 5:4  | Product-Line part of Chip ID |
| FID      | 3:0  | Functional part of Chip ID   |

**ChipID2 (0x05)**

Chip ID MSB

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | CIDMSB[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x80        |   |   |   |   |   |   |   |
| Access Type | Read Only   |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                 |
|----------|------|-----------------------------|
| CIDMSB   | 7:0  | Product Unique Chip ID-8MSB |

**ChipRev (0x06)**

Chip Revision

| BIT         | 7 | 6 | 5 | 4 | 3         | 2 | 1 | 0 |
|-------------|---|---|---|---|-----------|---|---|---|
| Field       | – | – | – | – | Rev[3:0]  |   |   |   |
| Reset       | – | – | – | – | 0x0       |   |   |   |
| Access Type | – | – | – | – | Read Only |   |   |   |

| BITFIELD | BITS | DESCRIPTION      |
|----------|------|------------------|
| Rev      | 3:0  | Chip Revision ID |

**VendID1 (0x0C)**

Vendor ID LSB

| BIT         | 7                           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">VIDLSB[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x6A                        |   |   |   |   |   |   |   |
| Access Type | Read Only                   |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION        |
|----------|------|--------------------|
| VIDLSB   | 7:0  | Vendor ID LSB Byte |

**[VendID2 \(0x0D\)](#)**

Vendor ID MSB

| BIT         | 7                           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">VIDMSB[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x0B                        |   |   |   |   |   |   |   |
| Access Type | Read Only                   |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION        |
|----------|------|--------------------|
| VIDMSB   | 7:0  | Vendor ID MSB Byte |

**[CfgDACrate \(0x10\)](#)**

Configure DAC Update Rate

| BIT         | 7 | 6 | 5 | 4 | 3                          | 2 | 1 | 0 |
|-------------|---|---|---|---|----------------------------|---|---|---|
| Field       | – | – | – | – | <a href="#">Drate[3:0]</a> |   |   |   |
| Reset       | – | – | – | – | 0x5                        |   |   |   |
| Access Type | – | – | – | – | Write, Read                |   |   |   |

| BITFIELD | BITS | DESCRIPTION        | DECODE                                                                                                                                                                                                                               |
|----------|------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Drate    | 3:0  | Configure DAC rate | 0x0: Reserved<br>0x1: Reserved<br>0x3: Reserved<br>0x5: 4915.2MHz (default)<br>0x7: Reserved<br>0x8: Reserved<br>0x9: Reserved<br>0xA: Reserved<br>0xB: Reserved<br>0xC: Reserved<br>0xD: Reserved<br>0xE: Reserved<br>0xF: Reserved |

**[CfgCLKrate \(0x11\)](#)**

Configure CLKP/N Input Rate

| BIT         | 7 | 6 | 5 | 4 | 3                          | 2 | 1 | 0 |
|-------------|---|---|---|---|----------------------------|---|---|---|
| Field       | – | – | – | – | <a href="#">Crate[3:0]</a> |   |   |   |
| Reset       | – | – | – | – | 0xD                        |   |   |   |
| Access Type | – | – | – | – | Write, Read                |   |   |   |

| BITFIELD | BITS | DESCRIPTION               | DECODE                                                                                                                                                                                                                                 |
|----------|------|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Crate    | 3:0  | CLKP/N rate configuration | 0x0: 245.76MHz<br>0x1: Reserved<br>0x2: Reserved<br>0x3: 491.52MHz<br>0x4: Reserved<br>0x5: 983.04MHz<br>0x6: Reserved<br>0x7: Reserved<br>0x8: Reserved<br>0x9: Reserved<br>0xB: Reserved<br>0xD: Reserved (Default)<br>0xF: Reserved |

**[CfgREGS \(0x12\)](#)**

Configure Register options

| BIT         | 7 | 6 | 5 | 4 | 3 | 2 | 1                    | 0                      |
|-------------|---|---|---|---|---|---|----------------------|------------------------|
| Field       | – | – | – | – | – | – | <a href="#">rsvd</a> | <a href="#">IntCfg</a> |
| Reset       | – | – | – | – | – | – | 0b0                  | 0b0                    |
| Access Type | – | – | – | – | – | – | Write, Read          | Write, Read            |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                               | DECODE                                                                                                                          |
|----------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|
| rsvd     | 1    | Reseverd Bit                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                 |
| IntCfg   | 0    | Enable the Internal Configuration Mode.<br>GLBL.CfgIFC.xfer triggers the internal configuration process and after it is complete, the DSP.STATUS.TRDY latched status is set.<br>The registers/fields configured are<br>DSP.CfgPLL1<br>DSP.CfgPLL2<br>DSP.CfgClkDiv<br>SerDesRegs.CfgSerDes.RxRateSel<br>SerDesRegs.CfgSerDes.PhyWMode<br>CMURegs.CfgfCMU1 | 0x0: Internal register configuration is disabled<br>0x1: When CfgIFC.Xfer bit is set, some registers are configured internally. |

**[CfgChipOM \(0x100\)](#)**

Configure Chip Operation Mode

| BIT         | 7 | 6                          | 5 | 4                    | 3 | 2                    | 1 | 0                    |
|-------------|---|----------------------------|---|----------------------|---|----------------------|---|----------------------|
| Field       | – | <a href="#">RclkM[1:0]</a> |   | <a href="#">INVQ</a> | – | <a href="#">Mute</a> | – | <a href="#">DFMT</a> |
| Reset       | – | 0x0                        |   | 0b0                  | – | 0b1                  | – | 0b0                  |
| Access Type | – | Write, Read                |   | Write, Read          | – | Write, Read          | – | Write, Read          |

| BITFIELD | BITS | DESCRIPTION                             | DECODE                                                                                                                                                                                                                   |
|----------|------|-----------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RclkM    | 6:5  | RCLK output mode                        | 0x0: DAC clock divided by (interpolation ratio x 1)<br>0x1: DAC clock divided by (interpolation ratio x 2)<br>0x2: DAC clock divided by (interpolation ratio x 4)<br>0x3: DAC clock divided by (interpolation ratio x 4) |
| INVQ     | 4    | Configure the Q inversion               | 0x0: Disable DAC I-Q data Q being inverted to make I-Q<br>0x1: Enable DAC I-Q data Q being inverted to make I+Q                                                                                                          |
| Mute     | 2    | Control DAC mute/unmute mode            | 0x0: DAC in normal mode<br>0x1: Put DAC into mute mode                                                                                                                                                                   |
| DFMT     | 0    | Configure the DAC interface data format | 0x0: DAC Input data in two's complement format<br>0x1: DAC Input data in offset binary format                                                                                                                            |

**CfgDSP (0x101)**

Configure DSP engine

| BIT         | 7                      | 6 | 5 | 4 | 3                      | 2                       | 1                    | 0                     |
|-------------|------------------------|---|---|---|------------------------|-------------------------|----------------------|-----------------------|
| Field       | <a href="#">R[3:0]</a> |   |   |   | <a href="#">RstDSP</a> | <a href="#">RstFIFO</a> | <a href="#">NCOE</a> | <a href="#">NCOLD</a> |
| Reset       | 0x0                    |   |   |   | 0b0                    | 0b0                     | 0b0                  | 0b0                   |
| Access Type | Read Only              |   |   |   | Write, Read            | Write, Read             | Write, Read          | Write 1 to Set, Read  |

| BITFIELD | BITS | DESCRIPTION                                                             | DECODE                                                                                    |
|----------|------|-------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|
| R        | 7:4  | Reserved                                                                |                                                                                           |
| RstDSP   | 3    | Reset DSP (Input FIFO, interpolation filters, complex modulator, NCO)   | 0x0: No Reset<br>0x1: Reset DSP                                                           |
| RstFIFO  | 2    | Reset input data FIFO                                                   | 0x0: No Reset<br>0x1: Reset FIFO                                                          |
| NCOE     | 1    | Enable/Disable Extended NCO mode                                        | 0x0: Disable Extended NCO mode for DAC<br>0x1: Enable Extended NCO mode for 10KHz spacing |
| NCOLD    | 0    | Writing a 1 loads NCO configuration for DAC. This bit is self clearing. | 0x0<br>0x1: Loads NCO configuration for DAC                                               |

**CfgNCOF0 (0x102)**

Configure NCO Frequency Control Word for DAC DSP, bits[7:0]

| BIT         | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">FCW[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                     |   |   |   |   |   |   |   |
| Access Type | Write, Read              |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                 |
|----------|------|-------------------------------------------------------------|
| FCW      | 7:0  | Configure NCO Frequency Control Word for DAC DSP, bits[7:0] |

**CfgNCOF1 (0x103)**

Configure NCO Frequency Control Word for DAC DSP, bits[15:8]

| BIT         | 7                         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">FCW[15:8]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                      |   |   |   |   |   |   |   |
| Access Type | Write, Read               |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                  |
|----------|------|--------------------------------------------------------------|
| FCW      | 7:0  | Configure NCO Frequency Control Word for DAC DSP, bits[15:8] |

**CfgNCOF2 (0x104)**

Configure NCO Frequency Control Word for DAC DSP, bits[23:16]

| BIT         | 7                          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">FCW[23:16]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                       |   |   |   |   |   |   |   |
| Access Type | Write, Read                |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                   |
|----------|------|---------------------------------------------------------------|
| FCW      | 7:0  | Configure NCO Frequency Control Word for DAC DSP, bits[23:16] |

**CfgNCOF3 (0x105)**

Configure NCO Frequency Control Word for DAC DSP, bits[31:24]

| BIT         | 7                          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">FCW[31:24]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                       |   |   |   |   |   |   |   |
| Access Type | Write, Read                |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                   |
|----------|------|---------------------------------------------------------------|
| FCW      | 7:0  | Configure NCO Frequency Control Word for DAC DSP, bits[31:24] |

**CfgNCON0 (0x106)**

Configure NCO Frequency Control Word Numerator Word for DAC DSP, bits[7:0]

| BIT         | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">NFW[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                     |   |   |   |   |   |   |   |
| Access Type | Write, Read              |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                |
|----------|------|----------------------------------------------------------------------------|
| NFW      | 7:0  | Configure NCO Frequency Control Word Numerator Word for DAC DSP, bits[7:0] |

**CfgNCON1 (0x107)**

Configure NCO Frequency Control Word Numerator Word for DAC DSP, bits[15:8]

| BIT         | 7                         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">NFW[15:8]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                      |   |   |   |   |   |   |   |
| Access Type | Write, Read               |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                 |
|----------|------|-----------------------------------------------------------------------------|
| NFW      | 7:0  | Configure NCO Frequency Control Word Numerator Word for DAC DSP, bits[15:8] |

**CfgNCON2 (0x108)**

Configure NCO Frequency Control Word Numerator Word for DAC DSP, bits[17:16]

| BIT         | 7 | 6 | 5 | 4 | 3 | 2 | 1                          | 0 |
|-------------|---|---|---|---|---|---|----------------------------|---|
| Field       | – | – | – | – | – | – | <a href="#">NFW[17:16]</a> |   |
| Reset       | – | – | – | – | – | – | 0x0                        |   |
| Access Type | – | – | – | – | – | – | Write, Read                |   |

| BITFIELD | BITS | DESCRIPTION                                                                  |
|----------|------|------------------------------------------------------------------------------|
| NFW      | 1:0  | Configure NCO Frequency Control Word Numerator Word for DAC DSP, bits[17:16] |

**CfgNCOD0 (0x109)**

Configure NCO Frequency Control Word Denominator Word for DAC DSP, bits [7:0]

| BIT         | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">DFW[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                     |   |   |   |   |   |   |   |
| Access Type | Write, Read              |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                  |
|----------|------|------------------------------------------------------------------------------|
| DFW      | 7:0  | Configure NCO Frequency Control Word Denominator Word for DAC DSP, bits[7:0] |

**CfgNCOD1 (0x10A)**

Configure NCO Frequency Control Word Denominator Word for DAC DSP, bits [15:8]

| BIT         | 7                         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">DFW[15:8]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                      |   |   |   |   |   |   |   |
| Access Type | Write, Read               |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                   |
|----------|------|-------------------------------------------------------------------------------|
| DFW      | 7:0  | Configure NCO Frequency Control Word Denominator Word for DAC DSP, bits[15:8] |

**CfgNCOD2 (0x10B)**

Configure NCO Frequency Control Word Denominator Word for DAC DSP, bits [18:16]

| BIT         | 7 | 6 | 5 | 4 | 3 | 2                          | 1 | 0 |
|-------------|---|---|---|---|---|----------------------------|---|---|
| Field       | – | – | – | – | – | <a href="#">DFW[18:16]</a> |   |   |
| Reset       | – | – | – | – | – | 0x0                        |   |   |
| Access Type | – | – | – | – | – | Write, Read                |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                    |
|----------|------|--------------------------------------------------------------------------------|
| DFW      | 2:0  | Configure NCO Frequency Control Word Denominator Word for DAC DSP, bits[18:16] |

**CfgNCOU (0x10C)**

Configure NCO Update for DAC DSP

| BIT         | 7 | 6 | 5 | 4 | 3 | 2 | 1                        | 0 |
|-------------|---|---|---|---|---|---|--------------------------|---|
| Field       | – | – | – | – | – | – | <a href="#">RLM[1:0]</a> |   |
| Reset       | – | – | – | – | – | – | 0x0                      |   |
| Access Type | – | – | – | – | – | – | Write, Read              |   |

| BITFIELD | BITS | DESCRIPTION                            | DECODE                                                                                             |
|----------|------|----------------------------------------|----------------------------------------------------------------------------------------------------|
| RLM      | 1:0  | NCO Frequency Control Word update mode | 0x0: Load immediately with no glitch control<br>0x2: Use step increment/decrement mode for loading |

**CfgNCOUT0 (0x10D)**

Configure NCO Update Timer for DAC DSP, bit[7:0]

| BIT         | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">TIM[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                     |   |   |   |   |   |   |   |
| Access Type | Write, Read              |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                 |
|----------|------|-----------------------------------------------------------------------------|
| TIM      | 7:0  | NCO Update Timer value in NCO clock cycles (x8) before NCO update is forced |

**CfgNCOUT1 (0x10E)**

Configure NCO Update Timer for DAC DSP, bits[15:8]

| BIT         | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">TIM[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                     |   |   |   |   |   |   |   |
| Access Type | Write, Read              |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                          |
|----------|------|----------------------------------------------------------------------|
| TIM      | 7:0  | NCO Update Timer value in NCO clock cycles (x8) before NCO update is |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|-------------|
|          |      | forced      |

**CfgNCOUT2 (0x10F)**

Configure NCO Update Timer for DAC DSP, bits[23:16]

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | TIM[7:0]    |   |   |   |   |   |   |   |
| Reset       | 0x00        |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                 |
|----------|------|-----------------------------------------------------------------------------|
| TIM      | 7:0  | NCO Update Timer value in NCO clock cycles (x8) before NCO update is forced |

**CfgPM (0x110)**

Configure Power Monitor for DAC DSP

| BIT         | 7 | 6 | 5 | 4 | 3 | 2           | 1           | 0                    |
|-------------|---|---|---|---|---|-------------|-------------|----------------------|
| Field       | – | – | – | – | – | Start       | Mode        | Reset                |
| Reset       | – | – | – | – | – | 0b0         | 0b0         | 0b0                  |
| Access Type | – | – | – | – | – | Write, Read | Write, Read | Write 1 to Set, Read |

| BITFIELD | BITS | DESCRIPTION                                                            | DECODE                                                                           |
|----------|------|------------------------------------------------------------------------|----------------------------------------------------------------------------------|
| Start    | 2    | Power Monitor Start                                                    |                                                                                  |
| Mode     | 1    | Power Monitor Mode                                                     | 0x0: Count samples below the threshold<br>0x1: Count samples above the threshold |
| Reset    | 0    | Writing a 1 resets the power monitor count. This bit is self clearing. | 0x0<br>0x1: Resets the power monitor count.                                      |

**CfgPMT (0x111)**

Configure Power Monitor Threshold for DAC DSP

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | PMT[7:0]    |   |   |   |   |   |   |   |
| Reset       | 0x00        |   |   |   |   |   |   |   |
| Access Type | Write, Read |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                             |
|----------|------|-----------------------------------------|
| PMT      | 7:0  | Configure Power Monitor Threshold value |

**CfgPMIC0 (0x112)**

Configure Power Monitor Init Count 6 x 8 = 48 bits for DAC DSP, bits[7:0]

| BIT         | 7                         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">PMIC[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                      |   |   |   |   |   |   |   |
| Access Type | Write, Read               |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION           |
|----------|------|-----------------------|
| PMIC     | 7:0  | Count value bits[7:0] |

**[CfgPMIC1 \(0x113\)](#)**

Configure Power Monitor Init Count 6 x 8 = 48 bits for DAC DSP

| BIT         | 7                         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">PMIC[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                      |   |   |   |   |   |   |   |
| Access Type | Write, Read               |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION            |
|----------|------|------------------------|
| PMIC     | 7:0  | Count value bits[15:8] |

**[CfgPMIC2 \(0x114\)](#)**

Configure Power Monitor Init Count 6 x 8 = 48 bits for DAC DSP

| BIT         | 7                         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">PMIC[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                      |   |   |   |   |   |   |   |
| Access Type | Write, Read               |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION             |
|----------|------|-------------------------|
| PMIC     | 7:0  | Count value bits[23:16] |

**[CfgPMIC3 \(0x115\)](#)**

Configure Power Monitor Init Count 6 x 8 = 48 bits for DAC DSP

| BIT         | 7                         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">PMIC[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                      |   |   |   |   |   |   |   |
| Access Type | Write, Read               |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION             |
|----------|------|-------------------------|
| PMIC     | 7:0  | Count value bits[31:24] |

**[CfgPMIC4 \(0x116\)](#)**

Configure Power Monitor Init Count 6 x 8 = 48 bits for DAC DSP

| BIT         | 7                         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">PMIC[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                      |   |   |   |   |   |   |   |
| Access Type | Write, Read               |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION             |
|----------|------|-------------------------|
| PMIC     | 7:0  | Count value bits[39:32] |

**[CfgPMIC5 \(0x117\)](#)**

Configure Power Monitor Init Count 6 x 8 = 48 bits for DAC DSP, bits[47:40]

| BIT         | 7                         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">PMIC[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                      |   |   |   |   |   |   |   |
| Access Type | Write, Read               |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION             |
|----------|------|-------------------------|
| PMIC     | 7:0  | Count value bits[47:40] |

**[StatPM0 \(0x118\)](#)**

Power Monitor Status for DAC DSP

| BIT         | 7                         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">PMST[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                      |   |   |   |   |   |   |   |
| Access Type | Read Only                 |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                             |
|----------|------|-------------------------------------------------------------------------|
| PMST     | 7:0  | Power Monitor Status indicating the threshold crossing count, bits[7:0] |

**[StatPM1 \(0x119\)](#)**

Power Monitor Status for DAC DSP

| BIT         | 7                      | 6 | 5 | 4 | 3                         | 2 | 1 | 0 |
|-------------|------------------------|---|---|---|---------------------------|---|---|---|
| Field       | <a href="#">PMDONE</a> | – | – | – | <a href="#">PMST[3:0]</a> |   |   |   |
| Reset       | 0b0                    | – | – | – | 0x0                       |   |   |   |
| Access Type | Read Only              | – | – | – | Read Only                 |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                  | DECODE                                                                                |
|----------|------|----------------------------------------------|---------------------------------------------------------------------------------------|
| PMDONE   | 7    | Power Monitor Status                         | 0x0: Power Monitor Status update in progress<br>0x1: Power Monitor Status update done |
| PMST     | 3:0  | Power Monitor Status for DAC DSP, bits[11:8] |                                                                                       |

**[CfgSync \(0x15A\)](#)**

Configure multiple-DAC synchronization for DAC DSP

| BIT         | 7 | 6                           | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|-----------------------------|---|---|---|---|---|---|
| Field       | – | <a href="#">ClkDiv_Sync</a> | – | – | – | – | – | – |
| Reset       | – | 0b0                         | – | – | – | – | – | – |
| Access Type | – | Write, Read                 | – | – | – | – | – | – |

| BITFIELD    | BITS | DESCRIPTION                                     | DECODE                                                                                                  |
|-------------|------|-------------------------------------------------|---------------------------------------------------------------------------------------------------------|
| ClkDiv_Sync | 6    | Enable/Disable reset to the Clock Divider Block | 0x0:<br>Disable reset to the Clock Divider Block<br><br>0x1:<br>Enable reset to the Clock Divider Block |

**[CfgFIFO \(0x15B\)](#)**

Configure Input FIFO for DAC

| BIT         | 7                         | 6 | 5 | 4 | 3 | 2                    | 1                      | 0                         |
|-------------|---------------------------|---|---|---|---|----------------------|------------------------|---------------------------|
| Field       | <a href="#">rsvd[4:0]</a> |   |   |   |   | <a href="#">Dupl</a> | <a href="#">SwapIQ</a> | <a href="#">RevBitOrd</a> |
| Reset       | 0x0                       |   |   |   |   |                      |                        |                           |
| Access Type | Write, Read               |   |   |   |   | Write, Read          | Write, Read            | Write, Read               |

| BITFIELD  | BITS | DESCRIPTION                                     | DECODE                                                  |
|-----------|------|-------------------------------------------------|---------------------------------------------------------|
| rsvd      | 7:3  | Reserved Bits                                   |                                                         |
| Dupl      | 2    | Duplicate I data in the input FIFO for DAC      | 0x0: Do not duplicate I<br>0x1: Duplicate I             |
| SwapIQ    | 1    | Reverse I/Q Order in the input FIFO for DAC     | 0x0: Normal I/Q Order<br>0x1: Reverse I/Q Order         |
| RevBitOrd | 0    | Reverse LSB/MSB Order in the input FIFO for DAC | 0x0: Normal LSB/MSB Order<br>0x1: Reverse LSB/MSB Order |

**[CfgRSV0 \(0x15D\)](#)**

Configure Reserved, bits[7:0]

| BIT         | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">RSV[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                     |   |   |   |   |   |   |   |
| Access Type | Write, Read              |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|-------------|
| RSV      | 7:0  | Reserved    |

**[CfgRSV1 \(0x15E\)](#)**

Configure Reserved, bits[15:8]

| BIT         | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">RSV[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                     |   |   |   |   |   |   |   |
| Access Type | Write, Read              |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|-------------|
| RSV      | 7:0  | Reserved    |

**[CfgRSV2 \(0x15F\)](#)**

Configure Reserved, bits[23:16]

| BIT         | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">RSV[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                     |   |   |   |   |   |   |   |
| Access Type | Write, Read              |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|-------------|
| RSV      | 7:0  | Reserved    |

**[CfgRSV3 \(0x160\)](#)**

Configure Reserved, bits[31:24]

| BIT         | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">RSV[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                     |   |   |   |   |   |   |   |
| Access Type | Write, Read              |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|-------------|
| RSV      | 7:0  | Reserved    |

**[EMUTE \(0x162\)](#)**

Mute Enable Register for DAC

| BIT         | 7                       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">EM[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                    |   |   |   |   |   |   |   |
| Access Type | Write, Read             |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                    | DECODE                                                                                      |
|----------|------|------------------------------------------------|---------------------------------------------------------------------------------------------|
| EM       | 7:0  | Enable/Disable Mute bit 0-7 in register STATUS | 0x0: Disable Mute bit 0-7 in register STATUS<br>0x1: Enable Mute bit 0-7 in register STATUS |

**[EINT \(0x163\)](#)**

Interrupt Enable Register for DAC DSP

| BIT         | 7                           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">INT_EN[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                        |   |   |   |   |   |   |   |
| Access Type | Write, Read                 |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                         | DECODE                                                                                                |
|----------|------|-----------------------------------------------------|-------------------------------------------------------------------------------------------------------|
| INT_EN   | 7:0  | Enable/Disable interrupt bit 0-7 in register STATUS | 0x0: Disable interrupt bit 0-7 in register STATUS<br>0x1: Enable interrupt bit 0-7 in register STATUS |

**[STATUS \(0x164\)](#)**

Status Register for DAC DSP

| BIT         | 7                     | 6                     | 5                         | 4 | 3 | 2                      | 1 | 0                      |
|-------------|-----------------------|-----------------------|---------------------------|---|---|------------------------|---|------------------------|
| Field       | <a href="#">JSDIM</a> | <a href="#">JSDII</a> | <a href="#">rsvd[2:0]</a> |   |   | <a href="#">TRDY</a>   | – | <a href="#">PLLICK</a> |
| Reset       |                       |                       |                           |   |   |                        | – |                        |
| Access Type | Read Only             | Read Only             | Read Only                 |   |   | Write 0 to Clear, Read | – | Write 0 to Clear, Read |

| BITFIELD | BITS | DESCRIPTION                                                              | DECODE                                                                                                                                                                                      |
|----------|------|--------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| JSDIM    | 7    | JSDI Link layer Mute active/inactive status                              | 0x0: Indicates JSDI Link layer Mute is not active<br>0x1: Indicates JSDI Link layer Mute is active                                                                                          |
| JSDII    | 6    | JSDI Link layer Interrupt active/inactive status                         | 0x0: Indicates JSDI Link layer Interrupt is not active<br>0x1: Indicates JSDI Link layer Interrupt is active                                                                                |
| rsvd     | 5:3  | Reserved Bits                                                            |                                                                                                                                                                                             |
| TRDY     | 2    | Trim loading complete or internal configuration complete, latched status | 0x0: Trim loading is in progress<br>0x1:<br>Trim loading complete after RESETB deassertion, latched status<br>Internal Configuration complete after setting GLB.CfgIFC.Xfer, latched status |
| PLLICK   | 0    | DAC PLL loss-of-lock, latched status                                     | 0x0: DAC PLL locked<br>0x1: DAC PLL loss-of-lock, latched status                                                                                                                            |

**[RSVD7 \(0x165\)](#)**

Reserved Address Space

| BIT         | 7                         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">rsvd[7:0]</a> |   |   |   |   |   |   |   |
| Reset       |                           |   |   |   |   |   |   |   |
| Access Type | Read Only                 |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|-------------|
| rsvd     | 7:0  |             |

**DEVSN0 (0x166)**

RF DAC Serial Number, bits[7:0]

| BIT         | 7                       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">SN[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x00                    |   |   |   |   |   |   |   |
| Access Type | Read Only               |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                             |
|----------|------|-----------------------------------------|
| SN       | 7:0  | MAX5855 RF DAC Serial Number, bits[7:0] |

**DEVSN1 (0x167)**

RF DAC Serial Number, bits[15:8]

**DEVSN2 (0x168)**

RF DAC Serial Number, bits[23:16]

**CfgPLL0 (0x180)**

Configure DAC PLL, bits[7:0]

| BIT         | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0                      |
|-------------|---|---|---|---|---|---|---|------------------------|
| Field       | – | – | – | – | – | – | – | <a href="#">MASTER</a> |
| Reset       | – | – | – | – | – | – | – | 0b0                    |
| Access Type | – | – | – | – | – | – | – | Write, Read            |

| BITFIELD | BITS | DESCRIPTION                                                                                                                     | DECODE                                                                             |
|----------|------|---------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|
| MASTER   | 0    | MASTER: 1V digital control logic input (active low) that resets counter clock (div-by-4096), edge detector, and counter=000000. | 0x0<br>0x1: Force restart PLL digital tuning by toggling from 1 to 0 and back to 1 |

**CfgPLL1 (0x181)**

Configure DAC PLL, bits[15:8]

| BIT         | 7 | 6                       | 5                          | 4 | 3                    | 2                     | 1 | 0 |
|-------------|---|-------------------------|----------------------------|---|----------------------|-----------------------|---|---|
| Field       | – | <a href="#">PLL_BYP</a> | <a href="#">DVAL0[1:0]</a> |   | <a href="#">PVAL</a> | <a href="#">RVAL0</a> | – | – |
| Reset       | – | 0b1                     | 0x0                        |   | 0b0                  | 0b0                   | – | – |
| Access Type | – | Write, Read             | Write, Read                |   | Write, Read          | Write, Read           | – | – |

| BITFIELD | BITS | DESCRIPTION                                                                                                     | DECODE                                                                                                        |
|----------|------|-----------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|
| PLL_BYP  | 6    | PLL_BYP: 1V digital control logic input                                                                         | 0x0<br>0x1: Reserved                                                                                          |
| DVAL0    | 5:4  | DVAL<1:0>: 1V digital control logic input to control feedback FB divider. See table below for DVAL[3:0] values. | 0x0: Reserved<br>0x1: 20<br>0x2: Reserved<br>0x3: Reserved<br>0x4: Reserved<br>0x5: Reserved<br>0x6: Reserved |

| BITFIELD | BITS | DESCRIPTION                                                                                        | DECODE                                                                                                                                                |
|----------|------|----------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |      |                                                                                                    | 0x7: Reserved<br>0x8: Reserved<br>0x9: Reserved<br>0xA: Reserved<br>0xB: Reserved<br>0xC: Reserved<br>0xD: Reserved<br>0xE: Reserved<br>0xF: Reserved |
| PVAL     | 3    | PVAL: 1V digital control logic input to control output divider.                                    | 0x0: Reserved<br>0x1: div-by-1 (bypass mode)                                                                                                          |
| RVAL0    | 2    | RVAL<0>: 1V digital control logic input to control reference divider. RVAL<1:0> table shows below. | 0x0: Reserved<br>0x1: div-by-4<br>0x2: div-by-2<br>0x3: div-by-1 (bypass mode)                                                                        |

**CfgPLL2 (0x182)**

Configure DAC PLL, bits[23:16]

| BIT         | 7 | 6 | 5 | 4           | 3 | 2           | 1 | 0           |
|-------------|---|---|---|-------------|---|-------------|---|-------------|
| Field       | – | – | – | DVAL1[1:0]  |   | RVAL1       | – | VCO_SEL     |
| Reset       | – | – | – | 0x0         |   | 0b0         | – | 0b0         |
| Access Type | – | – | – | Write, Read |   | Write, Read | – | Write, Read |

| BITFIELD | BITS | DESCRIPTION                                                                                        | DECODE                                                                                                                                                                                                                                                                 |
|----------|------|----------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DVAL1    | 4:3  | DVAL<3:2>. See below for DVAL[3:0] table.                                                          | 0x0: Reserved<br>0x1: 20<br>0x2: Reserved<br>0x3: Reserved<br>0x4: Reserved<br>0x5: Reserved<br>0x6: Reserved<br>0x7: Reserved<br>0x8: Reserved<br>0x9: Reserved<br>0xA: Reserved<br>0xB: Reserved<br>0xC: Reserved<br>0xD: Reserved<br>0xE: Reserved<br>0xF: Reserved |
| RVAL1    | 2    | RVAL<1>: 1V digital control logic input to control reference divider. RVAL<1:0> table shows below. | 0x0: Reserved<br>0x1: div-by-4<br>0x2: div-by-2<br>0x3: div-by-1 (bypass mode)                                                                                                                                                                                         |
| VCO_SEL  | 0    | VCO_SEL: 1V digital control logic input. Logic "0" selects the lowband VCO.                        | 0x0: Selects the lowband VCO<br>0x1: Reserved                                                                                                                                                                                                                          |

**StatPLL0 (0x183)**

DAC PLL Status, bits[7:0]

| BIT         | 7         | 6 | 5 | 4 | 3         | 2 | 1 | 0 |
|-------------|-----------|---|---|---|-----------|---|---|---|
| Field       | rsvd[3:0] |   |   |   | PLL_LOCK  | – | – | – |
| Reset       |           |   |   |   |           | – | – | – |
| Access Type | Read Only |   |   |   | Read Only | – | – | – |

| BITFIELD | BITS | DESCRIPTION     | DECODE                                 |
|----------|------|-----------------|----------------------------------------|
| rsvd     | 7:4  | Reserved Bits   |                                        |
| PLL_LOCK | 3    | PLL lock detect | 0x0: PLL not locked<br>0x1: PLL locked |

**CfgClkDiv (0x185)**

Clock Generator Output Divider

| BIT         | 7           | 6 | 5 | 4 | 3           | 2 | 1           | 0 |
|-------------|-------------|---|---|---|-------------|---|-------------|---|
| Field       | RDIV[3:0]   |   |   |   | RSV[1:0]    |   | PCLK[1:0]   |   |
| Reset       | 0x6         |   |   |   | 0x0         |   | 0x0         |   |
| Access Type | Write, Read |   |   |   | Write, Read |   | Write, Read |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                                                           | DECODE                                                                                                                                                                                                                                                                      |
|----------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RDIV     | 7:4  | Clock divider setting for RCLKi. RCLKi is set to Internal DAC Clock rate divided by the RDIV3:0 setting. RCLKi drives the input of the following RCLK (CfgChipOM.RclkM1-0) and CMU (CfgCMU1.Cref_divsel1p0) dividers. | 0x0: Off<br>0x1: Reserved<br>0x2: Reserved<br>0x3: Reserved<br>0x4: Reserved<br>0x5: Reserved<br>0x6: Reserved<br>0x7: Reserved<br>0x8: Divide by 20<br>0x9: Reserved<br>0xA: Reserved<br>0xB: Reserved<br>0xC: Reserved<br>0xD: Reserved<br>0xE: Reserved<br>0xF: Reserved |
| RSV      | 3:2  | Reserved Bits                                                                                                                                                                                                         |                                                                                                                                                                                                                                                                             |
| PCLK     | 1:0  | Divide ratio for PCLK used by the APB bus in the RxLink Layer                                                                                                                                                         | 0x1: RCLK<br>0x2: Reserved<br>0x3: Reserved                                                                                                                                                                                                                                 |

**CfgRLinkSet (0x400)**

Configure Rx Link Settings

| BIT         | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 23 | 22 | 21                        | 20 | 19                            | 18 | 17                       | 16                      |
|-------------|----|----|---------------------------|----|-------------------------------|----|--------------------------|-------------------------|
| Field       | –  | –  | –                         | –  | –                             | –  | <a href="#">SyncInit</a> | <a href="#">SyncPol</a> |
| Reset       | –  | –  | –                         | –  | –                             | –  | 0x0                      | 0x0                     |
| Access Type | –  | –  | –                         | –  | –                             | –  | Write, Read              | Write, Read             |
| BIT         | 15 | 14 | 13                        | 12 | 11                            | 10 | 9                        | 8                       |
| Field       | –  | –  | –                         | –  | –                             | –  | <a href="#">IgnDisp</a>  | <a href="#">ScrmD</a>   |
| Reset       | –  | –  | –                         | –  | –                             | –  | 0x0                      | 0x0                     |
| Access Type | –  | –  | –                         | –  | –                             | –  | Write, Read              | Write, Read             |
| BIT         | 7  | 6  | 5                         | 4  | 3                             | 2  | 1                        | 0                       |
| Field       | –  | –  | <a href="#">DDiv[1:0]</a> |    | <a href="#">Subclass[1:0]</a> |    | <a href="#">RstSRL</a>   | <a href="#">RstILA</a>  |
| Reset       | –  | –  | 0x0                       |    | 0x0                           |    | 0x0                      | 0x0                     |
| Access Type | –  | –  | Write, Read               |    | Write, Read                   |    | Write, Read              | Write, Read             |

| BITFIELD | BITS | DESCRIPTION                                                   | DECODE                                                                                                                                                                                                                                                                                                                                                                              |
|----------|------|---------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SyncInit | 17   | Out-of-reset value for SYNC~                                  | 0: RxLink SYNC~ initial value is 0<br>1: RxLink SYNC~ initial value is 1                                                                                                                                                                                                                                                                                                            |
| SyncPol  | 16   | SYNCRN polarity control                                       | 0: RxLink SYNC~ error reporting is active-low, which includes both resynchronization request and error reporting; normal state is high and resync request/error state is low per JESD204B standard<br>1: RxLink SYNC~ error reporting is active-high, which includes both resynchronization request and error reporting; normal state is low and resync request/error state is high |
| IgnDisp  | 9    | Running Disparity errors ignore for data processing control   | 0: Running Disparity errors are not ignored<br>1: Running Disparity errors are ignored                                                                                                                                                                                                                                                                                              |
| ScrmD    | 8    | Descrambler disable control                                   | 0: Descrambling is enabled<br>1: Descrambling is disabled                                                                                                                                                                                                                                                                                                                           |
| DDiv     | 5:4  | Device Clock to Frame Clock ratio select                      | 0: Device Clock to Frame Clock ratio is 1<br>1: Device Clock to Frame Clock ratio is 2<br>2: Device Clock to Frame Clock ratio is 4<br>3: Device Clock to Frame Clock ratio is 8                                                                                                                                                                                                    |
| Subclass | 3:2  | JESD204B subclass                                             | 0: Subclass 0<br>1: Subclass 1 (Not supported)<br>2: Subclass 2 (Not supported)<br>3: Reserved                                                                                                                                                                                                                                                                                      |
| RstSRL   | 1    | Soft Reset to clear all Status Registers Latched, active-high | 0: Latched statuses are not cleared<br>1: Latched statuses are cleared                                                                                                                                                                                                                                                                                                              |
| RstILA   | 0    | Soft Reset for ILA engine, active-high                        | 0: ILA engine is not reset<br>1: ILA engine is reset                                                                                                                                                                                                                                                                                                                                |

**CfgRLinkParam1 (0x404)**

Configure Link for parameters M, L, F and S

| BIT         | 31                        | 30 | 29                                                  | 28                        | 27 | 26 | 25 | 24 |
|-------------|---------------------------|----|-----------------------------------------------------|---------------------------|----|----|----|----|
| Field       | –                         | –  | –                                                   | <a href="#">CfgS[4:0]</a> |    |    |    |    |
| Reset       | –                         | –  | –                                                   | 0x0                       |    |    |    |    |
| Access Type | –                         | –  | –                                                   | Write, Read               |    |    |    |    |
| BIT         | 23                        | 22 | 21                                                  | 20                        | 19 | 18 | 17 | 16 |
| Field       | <a href="#">CfgF[7:0]</a> |    |                                                     |                           |    |    |    |    |
| Reset       | 0x0                       |    |                                                     |                           |    |    |    |    |
| Access Type | Write, Read               |    |                                                     |                           |    |    |    |    |
| BIT         | 15                        | 14 | 13                                                  | 12                        | 11 | 10 | 9  | 8  |
| Field       | –                         | –  | –                                                   | <a href="#">CfgL[4:0]</a> |    |    |    |    |
| Reset       | –                         | –  | –                                                   | 0x0                       |    |    |    |    |
| Access Type | –                         | –  | –                                                   | Write, Read               |    |    |    |    |
| BIT         | 7                         | 6  | 5                                                   | 4                         | 3  | 2  | 1  | 0  |
| Field       | <a href="#">CfgM[7:0]</a> |    |                                                     |                           |    |    |    |    |
| Reset       | 0x0                       |    |                                                     |                           |    |    |    |    |
| Access Type | Write, Read               |    |                                                     |                           |    |    |    |    |
| BITFIELD    | BITS                      |    | DESCRIPTION                                         |                           |    |    |    |    |
| CfgS        | 28:24                     |    | Number of samples per frame is (CfgS+1)             |                           |    |    |    |    |
| CfgF        | 23:16                     |    | Number of octets per frame is (CfgF+1)              |                           |    |    |    |    |
| CfgL        | 12:8                      |    | Number of active lanes in the Link is (CfgL+1)      |                           |    |    |    |    |
| CfgM        | 7:0                       |    | Number of active converters in the Link is (CfgM+1) |                           |    |    |    |    |

**CfgRLinkParam2 (0x408)**

Configure Link for parameter K and ILA sequence configuration

| BIT         | 31                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|--------------------------|----|----|----|----|----|----|----|
| Field       | <a href="#">DID[7:0]</a> |    |    |    |    |    |    |    |
| Reset       | 0x0                      |    |    |    |    |    |    |    |
| Access Type | Write, Read              |    |    |    |    |    |    |    |

| BIT         | 23                         | 22 | 21 | 20                        | 19                       | 18 | 17 | 16 |
|-------------|----------------------------|----|----|---------------------------|--------------------------|----|----|----|
| Field       | <a href="#">HD</a>         | –  | –  | –                         | <a href="#">BID[3:0]</a> |    |    |    |
| Reset       | 0x0                        | –  | –  | –                         | 0x0                      |    |    |    |
| Access Type | Write, Read                | –  | –  | –                         | Write, Read              |    |    |    |
| BIT         | 15                         | 14 | 13 | 12                        | 11                       | 10 | 9  | 8  |
| Field       | <a href="#">CfgNP[2:0]</a> |    |    | <a href="#">CfgN[4:0]</a> |                          |    |    |    |
| Reset       | 0x0                        |    |    | 0x00                      |                          |    |    |    |
| Access Type | Write, Read                |    |    | Write, Read               |                          |    |    |    |
| BIT         | 7                          | 6  | 5  | 4                         | 3                        | 2  | 1  | 0  |
| Field       | –                          | –  | –  | <a href="#">CfgK[4:0]</a> |                          |    |    |    |
| Reset       | –                          | –  | –  | 0x0                       |                          |    |    |    |
| Access Type | –                          | –  | –  | Write, Read               |                          |    |    |    |

| BITFIELD | BITS  | DESCRIPTION                                                              |
|----------|-------|--------------------------------------------------------------------------|
| DID      | 31:24 | Device ID used for ILA sequence checking                                 |
| HD       | 23    | HD bit used for ILA sequence checking                                    |
| BID      | 19:16 | Bank ID used for ILA sequence checking                                   |
| CfgNP    | 15:13 | Number of bits per sample rounded up to nibble groups is (CfgNP + 1) x 4 |
| CfgN     | 12:8  | Number of bits per sample is (CfgN + 1)                                  |
| CfgK     | 4:0   | Number of frames per multiframe is (CfgK + 1)                            |

**[CfgRLinkCtrl \(0x410\)](#)**

Configure Rx Link Control

| BIT         | 31 | 30                         | 29 | 28                     | 27 | 26 | 25 | 24 |
|-------------|----|----------------------------|----|------------------------|----|----|----|----|
| Field       | –  | –                          | –  | –                      | –  | –  | –  | –  |
| Reset       | –  | –                          | –  | –                      | –  | –  | –  | –  |
| Access Type | –  | –                          | –  | –                      | –  | –  | –  | –  |
| BIT         | 23 | 22                         | 21 | 20                     | 19 | 18 | 17 | 16 |
| Field       | –  | <a href="#">SCtrl[1:0]</a> |    | <a href="#">DFSycn</a> | –  | –  | –  | –  |
| Reset       | –  | 0x0                        |    | 0x0                    | –  | –  | –  | –  |
| Access Type | –  | Write, Read                |    | Write, Read            | –  | –  | –  | –  |

| BIT         | 15 | 14 | 13 | 12 | 11                      | 10 | 9                        | 8                     |
|-------------|----|----|----|----|-------------------------|----|--------------------------|-----------------------|
| Field       | –  | –  | –  | –  | –                       | –  | –                        | <a href="#">SErrC</a> |
| Reset       | –  | –  | –  | –  | –                       | –  | –                        | 0x0                   |
| Access Type | –  | –  | –  | –  | –                       | –  | –                        | Write, Read           |
| BIT         | 7  | 6  | 5  | 4  | 3                       | 2  | 1                        | 0                     |
| Field       | –  | –  | –  | –  | <a href="#">BitSwap</a> | –  | <a href="#">AsyncAvl</a> | <a href="#">rclk</a>  |
| Reset       | –  | –  | –  | –  | 0x0                     | –  | 0x0                      | 0x1                   |
| Access Type | –  | –  | –  | –  | Write, Read             | –  | Write, Read              | Write, Read           |

| BITFIELD | BITS  | DESCRIPTION                                         | DECODE                                                                                                                                                               |
|----------|-------|-----------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SCtrl    | 22:21 | ILA sequence detection control                      | 0: ILA sequence detection is enabled<br>1: ILA sequence detection is disabled for the first CfgRLinkMFrame.SNum frames<br>2: ILA sequence detection is disabled      |
| DFSyc    | 20    | ILA restart on frame resynchronization control      | 0: Enable ILA restart on frame resynchronization<br>1: Disable ILA restart on frame resynchronization                                                                |
| SErrC    | 8     | SYNC~ assert/deassert cycle control                 | 0: SYNC~ error reporting assertion/deassertion per JESD204B<br>1: Enable SYNC~ error reporting assertion/deassertion on any frame - JESD204A                         |
| BitSwap  | 3     | Bit Swap control                                    | 0: Disable Bit Swap MSB<-->LSB within an octet of the Lane data<br>1: Enable Bit Swap MSB<-->LSB within an octet of the Lane data                                    |
| AsyncAvl | 1     | Initial Frame Synchronization state machine control | 0: Initial Frame Synchronization state machine includes the FS_CHECK state<br>1: Initial Frame Synchronization state machine bypasses the FS_CHECK state             |
| rclk     | 0     | Frame/sample clock source                           | 0: Divided down Device Clock is used as frame/sample clock<br>1: Frame clock input from DAC/DSP is used as frame/sample clock when the Device Clock is not available |

**[CfgRLinkMFrame \(0x414\)](#)**

Configure Multiframe control

| BIT         | 31 | 30 | 29 | 28 | 27 | 26 | 25                        | 24 |
|-------------|----|----|----|----|----|----|---------------------------|----|
| Field       | –  | –  | –  | –  | –  | –  | <a href="#">SNum[8:7]</a> |    |
| Reset       | –  | –  | –  | –  | –  | –  | 0x3                       |    |
| Access Type | –  | –  | –  | –  | –  | –  | Write, Read               |    |

| BIT         | 23                         | 22    | 21                          | 20                                                                                                                                                                                             | 19 | 18 | 17 | 16                       |
|-------------|----------------------------|-------|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|--------------------------|
| Field       | <a href="#">SNum[6:0]</a>  |       |                             |                                                                                                                                                                                                |    |    |    | <a href="#">MFSEL[8]</a> |
| Reset       | 0x3                        |       |                             |                                                                                                                                                                                                |    |    |    | 0x4                      |
| Access Type | Write, Read                |       |                             |                                                                                                                                                                                                |    |    |    | Write, Read              |
| BIT         | 15                         | 14    | 13                          | 12                                                                                                                                                                                             | 11 | 10 | 9  | 8                        |
| Field       | <a href="#">MFSEL[7:0]</a> |       |                             |                                                                                                                                                                                                |    |    |    |                          |
| Reset       | 0x4                        |       |                             |                                                                                                                                                                                                |    |    |    |                          |
| Access Type | Write, Read                |       |                             |                                                                                                                                                                                                |    |    |    |                          |
| BIT         | 7                          | 6     | 5                           | 4                                                                                                                                                                                              | 3  | 2  | 1  | 0                        |
| Field       | –                          | –     | <a href="#">ILADLY[5:0]</a> |                                                                                                                                                                                                |    |    |    |                          |
| Reset       | –                          | –     | 0x0                         |                                                                                                                                                                                                |    |    |    |                          |
| Access Type | –                          | –     | Write, Read                 |                                                                                                                                                                                                |    |    |    |                          |
| BITFIELD    |                            | BITS  |                             | DESCRIPTION                                                                                                                                                                                    |    |    |    |                          |
| SNum        |                            | 25:17 |                             | ILA sequence number of multiframes                                                                                                                                                             |    |    |    |                          |
| MFSEL       |                            | 16:8  |                             | ILA multiframe count for FIFO write start                                                                                                                                                      |    |    |    |                          |
| ILADLY      |                            | 5:0   |                             | ILA Delay frame clock count for FIFO read start, ILADLY configuration sets the FIFO read start time relative to the multiframe boundary, for a desired FIFO depth possibly to minimize latency |    |    |    |                          |

**CfgRSYNCRN (0x418)**

SYNCRN~ Error Reporting control

| BIT         | 31 | 30                       | 29                       | 28                       | 27                       | 26                       | 25                      | 24                      |
|-------------|----|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|-------------------------|-------------------------|
| Field       | –  | –                        | –                        | –                        | –                        | –                        | –                       | –                       |
| Reset       | –  | –                        | –                        | –                        | –                        | –                        | –                       | –                       |
| Access Type | –  | –                        | –                        | –                        | –                        | –                        | –                       | –                       |
| BIT         | 23 | 22                       | 21                       | 20                       | 19                       | 18                       | 17                      | 16                      |
| Field       | –  | –                        | –                        | –                        | –                        | –                        | –                       | –                       |
| Reset       | –  | –                        | –                        | –                        | –                        | –                        | –                       | –                       |
| Access Type | –  | –                        | –                        | –                        | –                        | –                        | –                       | –                       |
| BIT         | 15 | 14                       | 13                       | 12                       | 11                       | 10                       | 9                       | 8                       |
| Field       | –  | <a href="#">RepErr14</a> | <a href="#">RepErr13</a> | <a href="#">RepErr12</a> | <a href="#">RepErr11</a> | <a href="#">RepErr10</a> | <a href="#">RepErr9</a> | <a href="#">RepErr8</a> |
| Reset       | –  | 0x0                      | 0x0                      | 0x0                      | 0x0                      | 0x0                      | 0x0                     | 0x0                     |
| Access Type | –  | Write, Read              | Write, Read              | Write, Read              | Write, Read              | Write, Read              | Write, Read             | Write, Read             |

| BIT         | 7 | 6                       | 5                       | 4 | 3 | 2                       | 1                       | 0                       |
|-------------|---|-------------------------|-------------------------|---|---|-------------------------|-------------------------|-------------------------|
| Field       | – | <a href="#">RepErr6</a> | <a href="#">RepErr5</a> | – | – | <a href="#">RepErr2</a> | <a href="#">RepErr1</a> | <a href="#">RepErr0</a> |
| Reset       | – | 0x0                     | 0x0                     | – | – | 0x0                     | 0x0                     | 0x0                     |
| Access Type | – | Write, Read             | Write, Read             | – | – | Write, Read             | Write, Read             | Write, Read             |

| BITFIELD | BITS | DESCRIPTION                                                                                                                           | DECODE                                                                                                                                |
|----------|------|---------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|
| RepErr14 | 14   | ILA Fail error control for Error Reporting, only if JESD204B-TX needs to monitor the RxLink errors                                    | 0: ILA Fail error is disabled<br>1: ILA Fail error is enabled                                                                         |
| RepErr13 | 13   | Reserved                                                                                                                              |                                                                                                                                       |
| RepErr12 | 12   | FIFO empty error control for Error Reporting                                                                                          | 0: FIFO empty error is disabled<br>1: FIFO empty error is enabled                                                                     |
| RepErr11 | 11   | FIFO full error control for Error Reporting                                                                                           | 0: FIFO full error is disabled<br>1: FIFO full error is enabled                                                                       |
| RepErr10 | 10   | Lane Configuration in ILA sequence FCS check error control for Error Reporting                                                        | 0: Lane Configuration in ILA sequence FCS check error is disabled<br>1: Lane Configuration in ILA sequence FCS check error is enabled |
| RepErr9  | 9    | Lane Configuration in ILA sequence mismatch error control for Error Reporting, This is corresponding to the StatRLane.LCfgrErr status | 0: Lane Configuration in ILA sequence mismatch error is disabled<br>1: Lane Configuration in ILA sequence mismatch error is enabled   |
| RepErr8  | 8    | ILA sequence control character error control for Error Reporting, This is corresponding to the StatRLane.ILAerr status                | 0: ILA sequence control character error is disabled<br>1: ILA sequence control character error is enabled                             |
| RepErr6  | 6    | Lane realignment event control for Error Reporting                                                                                    | 0: Lane realignment event is disabled<br>1: Lane realignment event is enabled                                                         |
| RepErr5  | 5    | Frame realignment event control for Error Reporting                                                                                   | 0: Frame realignment event is disabled<br>1: Frame realignment event is enabled                                                       |
| RepErr2  | 2    | 8b10b Running Disparity error control for Error Reporting                                                                             | 0: 8b10b Running Disparity error is disabled<br>1: 8b10b Running Disparity error is enabled                                           |
| RepErr1  | 1    | 8b10b NIT error control for Error Reporting                                                                                           | 0: 8b10b Not-in-table error is disabled<br>1: 8b10b Not-in-table error is enabled                                                     |
| RepErr0  | 0    | Reserved                                                                                                                              |                                                                                                                                       |

**CfgRFIFO (0x41C)**

Configure Rx Lane FIFOs

| BIT         | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 23 | 22 | 21 | 20                         | 19 | 18 | 17 | 16 |
|-------------|----|----|----|----------------------------|----|----|----|----|
| Field       | –  | –  | –  | –                          | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –                          | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –                          | –  | –  | –  | –  |
| BIT         | 15 | 14 | 13 | 12                         | 11 | 10 | 9  | 8  |
| Field       | –  | –  | –  | <a href="#">MaxFD[4:0]</a> |    |    |    |    |
| Reset       | –  | –  | –  | 0x1A                       |    |    |    |    |
| Access Type | –  | –  | –  | Write, Read                |    |    |    |    |
| BIT         | 7  | 6  | 5  | 4                          | 3  | 2  | 1  | 0  |
| Field       | –  | –  | –  | <a href="#">MinFD[4:0]</a> |    |    |    |    |
| Reset       | –  | –  | –  | 0x6                        |    |    |    |    |
| Access Type | –  | –  | –  | Write, Read                |    |    |    |    |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                                                                                                                                                                                   |
|----------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MaxFD    | 12:8 | Maximum FIFO depth for FIFO full status: The FIFO full latched status is indicated if the Lane FIFO depth ever increases beyond this configuration. This field should be set at least CfgF + 1 away from the maximum of 32 with some additional margin for clock domain crossing. The default value of 26 (1Ah) should work for all the modes |
| MinFD    | 4:0  | Minimum FIFO depth for FIFO empty status: The FIFO empty latched status is indicated if the Lane FIFO depth ever decreases below this configuration. This field should be set at least CfgF + 1 away from the minimum of 0 with some additional margin for clock domain crossing. The default value of 6 (06h) should work for all the modes  |

**[CfgRTestCtrl \(0x420\)](#)**

Configure Rx Link Test feature control

| BIT         | 31                                | 30 | 29 | 28 | 27                                | 26 | 25 | 24                              |
|-------------|-----------------------------------|----|----|----|-----------------------------------|----|----|---------------------------------|
| Field       | –                                 | –  | –  | –  | –                                 | –  | –  | <a href="#">LnCntTypeSel[3]</a> |
| Reset       | –                                 | –  | –  | –  | –                                 | –  | –  | 0x0                             |
| Access Type | –                                 | –  | –  | –  | –                                 | –  | –  | Write, Read                     |
| BIT         | 23                                | 22 | 21 | 20 | 19                                | 18 | 17 | 16                              |
| Field       | <a href="#">LnCntTypeSel[2:0]</a> |    |    |    | <a href="#">RxCntLaneSel[4:0]</a> |    |    |                                 |
| Reset       | 0x0                               |    |    |    | 0x0                               |    |    |                                 |
| Access Type | Write, Read                       |    |    |    | Write, Read                       |    |    |                                 |

| BIT         | 15 | 14 | 13                      | 12                            | 11                      | 10                    | 9                        | 8                           |
|-------------|----|----|-------------------------|-------------------------------|-------------------------|-----------------------|--------------------------|-----------------------------|
| Field       | –  | –  | <a href="#">SamLoad</a> | <a href="#">RxLoad</a>        | <a href="#">CDcorEn</a> | <a href="#">Rsvd0</a> | –                        | –                           |
| Reset       | –  | –  | 0x0                     | 0x0                           | 0x0                     | 0x0                   | –                        | –                           |
| Access Type | –  | –  | Write 1 to Toggle, Read | Write 1 to Toggle, Read       | Write, Read             | Write, Read           | –                        | –                           |
| BIT         | 7  | 6  | 5                       | 4                             | 3                       | 2                     | 1                        | 0                           |
| Field       | –  | –  | –                       | <a href="#">PRBStype[1:0]</a> |                         | –                     | <a href="#">RxPRBSen</a> | <a href="#">SamPRBS15En</a> |
| Reset       | –  | –  | –                       | 0x0                           |                         | –                     | 0x0                      | 0x0                         |
| Access Type | –  | –  | –                       | Write, Read                   |                         | –                     | Write, Read              | Write, Read                 |

| BITFIELD     | BITS  | DESCRIPTION                                                                                                                                                                                                             | DECODE                                                                                                                                                                                                                                                                                                                                                                                                             |
|--------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LnCntTypeSel | 24:21 | Lane debug counter error type select                                                                                                                                                                                    | 0: No counts, counter disabled<br>1: NIT errors<br>2: Running Disparity errors<br>3: /K/ detect count<br>4: /R/ detect count<br>5: /Q/ detect count<br>6: /A/ detect count<br>7: /F/ detect count<br>8: Unexpected control character count for unknown control character outside /K/, /A/, /F/, /R/ and /Q/ is detected<br>9: ILA sequence control character error count corresponding to the StatRLane.ILAerr bit |
| RxCntLaneSel | 20:16 | Invalid character counter Lane select for CntRLaneInvld                                                                                                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                                                    |
| SamLoad      | 13    | Pulse generation for sample clock domain counter/status update when set to 1, read value should be ignored. This bit is used to load the Lane FIFO depths FIFODepth in the StatRLane registers                          |                                                                                                                                                                                                                                                                                                                                                                                                                    |
| RxLoad       | 12    | Pulse generation for Rx SerDes clock domain counter/status update when set to 1, read value should be ignored. This bit is used to load the Lane debug counter values InvCnt in CntRLaneInvld and DbgCnt in CntRLaneDbg |                                                                                                                                                                                                                                                                                                                                                                                                                    |
| CDcorEn      | 11    | Counter clear control                                                                                                                                                                                                   | 0: Counter data clear-on-read disable<br>1: Counter data clear-on-read enable                                                                                                                                                                                                                                                                                                                                      |
| Rsvd0        | 10    | Rsvd0                                                                                                                                                                                                                   |                                                                                                                                                                                                                                                                                                                                                                                                                    |
| PRBStype     | 4:3   | PRBS type for SerDes PHY interface                                                                                                                                                                                      | 0: PRBS7 for SerDes Interface when enabled<br>1: PRBS23 for SerDes Interface when enabled<br>2: PRBS31 for SerDes Interface when enabled                                                                                                                                                                                                                                                                           |
| RxPRBSen     | 1     | Rx PRBS control for SerDes PHY interface                                                                                                                                                                                | 0: Disable PRBS checking on receive SerDes interface<br>1: Enable PRBS checking on receive SerDes interface, pattern based on PRBStype[1:0] This bit                                                                                                                                                                                                                                                               |

| BITFIELD     | BITS | DESCRIPTION                                                                                  | DECODE                                                                                                                                                                           |
|--------------|------|----------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|              |      |                                                                                              | should be toggled 0→1 to load the incoming data before starting error detection                                                                                                  |
| SamPRBS15 En | 0    | Sample interface PRBS15 checker control, PRBS checker enabled one sample per frame at a time | 0: Disable PRBS15 checker on sample data for all converters<br>1: Enable PRBS15 checker on sample data for all converters, to be toggled 0→1 to initialize and start the checker |

**CfgRLinkSTP1 (0x424)**

Configure Rx Link Converter Short Test Pattern 1

| BIT         | 31                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|-------------------------------|----|----|----|----|----|----|----|
| Field       | –                             | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –                             | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –                             | –  | –  | –  | –  | –  | –  | –  |
| BIT         | 23                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Field       | –                             | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –                             | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –                             | –  | –  | –  | –  | –  | –  | –  |
| BIT         | 15                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| Field       | <a href="#">Sample1[15:8]</a> |    |    |    |    |    |    |    |
| Reset       | 0x0                           |    |    |    |    |    |    |    |
| Access Type | Write, Read                   |    |    |    |    |    |    |    |
| BIT         | 7                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Field       | <a href="#">Sample1[7:0]</a>  |    |    |    |    |    |    |    |
| Reset       | 0x0                           |    |    |    |    |    |    |    |
| Access Type | Write, Read                   |    |    |    |    |    |    |    |

| BITFIELD | BITS | DESCRIPTION                                       |
|----------|------|---------------------------------------------------|
| Sample1  | 15:0 | Sample 1 of alternating sample Short Test Pattern |

**CfgRLinkSTP2 (0x428)**

Configure Rx Link Converter Short Test Pattern 2

| BIT         | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 23                            | 22 | 21                                                | 20 | 19 | 18 | 17 | 16 |
|-------------|-------------------------------|----|---------------------------------------------------|----|----|----|----|----|
| Field       | –                             | –  | –                                                 | –  | –  | –  | –  | –  |
| Reset       | –                             | –  | –                                                 | –  | –  | –  | –  | –  |
| Access Type | –                             | –  | –                                                 | –  | –  | –  | –  | –  |
| BIT         | 15                            | 14 | 13                                                | 12 | 11 | 10 | 9  | 8  |
| Field       | <a href="#">Sample2[15:8]</a> |    |                                                   |    |    |    |    |    |
| Reset       | 0x0                           |    |                                                   |    |    |    |    |    |
| Access Type | Write, Read                   |    |                                                   |    |    |    |    |    |
| BIT         | 7                             | 6  | 5                                                 | 4  | 3  | 2  | 1  | 0  |
| Field       | <a href="#">Sample2[7:0]</a>  |    |                                                   |    |    |    |    |    |
| Reset       | 0x0                           |    |                                                   |    |    |    |    |    |
| Access Type | Write, Read                   |    |                                                   |    |    |    |    |    |
| BITFIELD    | BITS                          |    | DESCRIPTION                                       |    |    |    |    |    |
| Sample2     | 15:0                          |    | Sample 2 of alternating sample Short Test Pattern |    |    |    |    |    |

**[CfgRLinkIntEn \(0x430\)](#)**

Configure Rx Link Interrupt Enables

| BIT         | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |
| BIT         | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |
| BIT         | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 7 | 6 | 5 | 4 | 3                        | 2 | 1 | 0                       |
|-------------|---|---|---|---|--------------------------|---|---|-------------------------|
| Field       | – | – | – | – | <a href="#">ILAnsync</a> | – | – | <a href="#">ILAfail</a> |
| Reset       | – | – | – | – | 0x0                      | – | – | 0x0                     |
| Access Type | – | – | – | – | Write, Read              | – | – | Write, Read             |

| BITFIELD | BITS | DESCRIPTION                                                    |
|----------|------|----------------------------------------------------------------|
| ILAnsync | 3    | Enable Interrupt on ILA synchronization not achieved real-time |
| ILAfail  | 0    | Enable Interrupt on ILA failure latched                        |

**[CfgRLinkMuteEn \(0x434\)](#)**

Configure Rx Link DAC Mute Enables

| BIT         | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------|----|----|----|----|----|----|---|---|
| Field       | –  | –  | –  | –  | –  | –  | – | – |
| Reset       | –  | –  | –  | –  | –  | –  | – | – |
| Access Type | –  | –  | –  | –  | –  | –  | – | – |

| BIT         | 7 | 6 | 5 | 4 | 3                        | 2 | 1 | 0                       |
|-------------|---|---|---|---|--------------------------|---|---|-------------------------|
| Field       | – | – | – | – | <a href="#">ILAnsync</a> | – | – | <a href="#">ILAfail</a> |
| Reset       | – | – | – | – | 0x0                      | – | – | 0x0                     |
| Access Type | – | – | – | – | Write, Read              | – | – | Write, Read             |

| BITFIELD | BITS | DESCRIPTION                                               |
|----------|------|-----------------------------------------------------------|
| ILAnsync | 3    | Enable Mute on ILA synchronization not achieved real-time |
| ILAfail  | 0    | Enable Mute on ILA failure latched                        |

**[StatRLinkILA \(0x438\)](#)**

RxLink ILA engine latched statuses

| BIT         | 31 | 30   | 29 | 28                                                                                                                                                                                                                                                                                                                                                                  | 27                       | 26 | 25 | 24                         |
|-------------|----|------|----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|----|----|----------------------------|
| Field       | –  | –    | –  | –                                                                                                                                                                                                                                                                                                                                                                   | –                        | –  | –  | –                          |
| Reset       | –  | –    | –  | –                                                                                                                                                                                                                                                                                                                                                                   | –                        | –  | –  | –                          |
| Access Type | –  | –    | –  | –                                                                                                                                                                                                                                                                                                                                                                   | –                        | –  | –  | –                          |
| BIT         | 23 | 22   | 21 | 20                                                                                                                                                                                                                                                                                                                                                                  | 19                       | 18 | 17 | 16                         |
| Field       | –  | –    | –  | –                                                                                                                                                                                                                                                                                                                                                                   | –                        | –  | –  | –                          |
| Reset       | –  | –    | –  | –                                                                                                                                                                                                                                                                                                                                                                   | –                        | –  | –  | –                          |
| Access Type | –  | –    | –  | –                                                                                                                                                                                                                                                                                                                                                                   | –                        | –  | –  | –                          |
| BIT         | 15 | 14   | 13 | 12                                                                                                                                                                                                                                                                                                                                                                  | 11                       | 10 | 9  | 8                          |
| Field       | –  | –    | –  | –                                                                                                                                                                                                                                                                                                                                                                   | –                        | –  | –  | –                          |
| Reset       | –  | –    | –  | –                                                                                                                                                                                                                                                                                                                                                                   | –                        | –  | –  | –                          |
| Access Type | –  | –    | –  | –                                                                                                                                                                                                                                                                                                                                                                   | –                        | –  | –  | –                          |
| BIT         | 7  | 6    | 5  | 4                                                                                                                                                                                                                                                                                                                                                                   | 3                        | 2  | 1  | 0                          |
| Field       | –  | –    | –  | –                                                                                                                                                                                                                                                                                                                                                                   | <a href="#">ILAnsync</a> | –  | –  | <a href="#">ILAfailure</a> |
| Reset       | –  | –    | –  | –                                                                                                                                                                                                                                                                                                                                                                   | 0x0                      | –  | –  | 0x0                        |
| Access Type | –  | –    | –  | –                                                                                                                                                                                                                                                                                                                                                                   | Read Only                | –  | –  | Write 0 to Clear, Read     |
| BITFIELD    |    | BITS |    | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                         |                          |    |    |                            |
| ILAnsync    |    | 3    |    | ILA synchronization not achieved status, real-time, indicating that the Lane FIFO writes did not start for the lanes enabled for Initial Lane Alignment process through the CfgRLaneSet.LkSel configuration                                                                                                                                                         |                          |    |    |                            |
| ILAfailure  |    | 0    |    | ILA failure latched status, indicating that at least one of the Lane FIFOs overflowed before the FIFO reads started waiting for ILA DELAY set with CfgRLinkMFrame.ILADly during the Initial Lane Alignment process or if FIFO writes did not start on a Lane that is not included in the Initial Lane Alignment process through the CfgRLaneSet.LkSel configuration |                          |    |    |                            |

**[StatRLinkSTP \(0x43C\)](#)**

Rx Link Sample Interface Short Test Pattern checker status

| BIT         | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 23 | 22   | 21 | 20                                          | 19 | 18 | 17                      | 16                      |
|-------------|----|------|----|---------------------------------------------|----|----|-------------------------|-------------------------|
| Field       | –  | –    | –  | –                                           | –  | –  | –                       | –                       |
| Reset       | –  | –    | –  | –                                           | –  | –  | –                       | –                       |
| Access Type | –  | –    | –  | –                                           | –  | –  | –                       | –                       |
| BIT         | 15 | 14   | 13 | 12                                          | 11 | 10 | 9                       | 8                       |
| Field       | –  | –    | –  | –                                           | –  | –  | –                       | –                       |
| Reset       | –  | –    | –  | –                                           | –  | –  | –                       | –                       |
| Access Type | –  | –    | –  | –                                           | –  | –  | –                       | –                       |
| BIT         | 7  | 6    | 5  | 4                                           | 3  | 2  | 1                       | 0                       |
| Field       | –  | –    | –  | –                                           | –  | –  | <a href="#">STPerr1</a> | <a href="#">STPerr0</a> |
| Reset       | –  | –    | –  | –                                           | –  | –  | 0x0                     | 0x0                     |
| Access Type | –  | –    | –  | –                                           | –  | –  | Write 0 to Clear, Read  | Write 0 to Clear, Read  |
| BITFIELD    |    | BITS |    | DESCRIPTION                                 |    |    |                         |                         |
| STPerr1     |    | 1    |    | STP error for each converter status latched |    |    |                         |                         |
| STPerr0     |    | 0    |    | STP error for each converter status latched |    |    |                         |                         |

**[StatRLinkPRBS \(0x440\)](#)**

Rx Link Sample Interface PRBS15 checker status

| BIT         | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |
| BIT         | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |
| BIT         | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 7 | 6 | 5 | 4 | 3 | 2 | 1                        | 0                        |
|-------------|---|---|---|---|---|---|--------------------------|--------------------------|
| Field       | – | – | – | – | – | – | <a href="#">PRBSerr1</a> | <a href="#">PRBSerr0</a> |
| Reset       | – | – | – | – | – | – | 0x0                      | 0x0                      |
| Access Type | – | – | – | – | – | – | Write 0 to Clear, Read   | Write 0 to Clear, Read   |

| BITFIELD | BITS | DESCRIPTION                                  |
|----------|------|----------------------------------------------|
| PRBSerr1 | 1    | PRBS error for each converter status latched |
| PRBSerr0 | 0    | PRBS error for each converter status latched |

**[CntRLaneInvald \(0x460\)](#)**

Rx Lane Counter for 8b10b Invalid errors

| BIT         | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 15                           | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------|------------------------------|----|----|----|----|----|---|---|
| Field       | <a href="#">InvCnt[15:8]</a> |    |    |    |    |    |   |   |
| Reset       | 0x0                          |    |    |    |    |    |   |   |
| Access Type | Read Only                    |    |    |    |    |    |   |   |

| BIT         | 7                           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">InvCnt[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x0                         |   |   |   |   |   |   |   |
| Access Type | Read Only                   |   |   |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION                                                                                                                                                                 |
|----------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| InvCnt   | 15:0 | Invalid character count for lane # controlled by CfgRTestCtrl.RxCntLaneSel, loaded on setting CfgRTestCtrl.RxLoad to 1, Invalid characters include NIT and Disparity errors |

**[CntRLaneDbg \(0x464\)](#)**

Rx Lane Counter for Debug

| BIT         | 31                           | 30 | 29                                                                                                                                                              | 28 | 27 | 26 | 25 | 24 |
|-------------|------------------------------|----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|
| Field       | –                            | –  | –                                                                                                                                                               | –  | –  | –  | –  | –  |
| Reset       | –                            | –  | –                                                                                                                                                               | –  | –  | –  | –  | –  |
| Access Type | –                            | –  | –                                                                                                                                                               | –  | –  | –  | –  | –  |
| BIT         | 23                           | 22 | 21                                                                                                                                                              | 20 | 19 | 18 | 17 | 16 |
| Field       | –                            | –  | –                                                                                                                                                               | –  | –  | –  | –  | –  |
| Reset       | –                            | –  | –                                                                                                                                                               | –  | –  | –  | –  | –  |
| Access Type | –                            | –  | –                                                                                                                                                               | –  | –  | –  | –  | –  |
| BIT         | 15                           | 14 | 13                                                                                                                                                              | 12 | 11 | 10 | 9  | 8  |
| Field       | <a href="#">DbgCnt[15:8]</a> |    |                                                                                                                                                                 |    |    |    |    |    |
| Reset       | 0x0                          |    |                                                                                                                                                                 |    |    |    |    |    |
| Access Type | Read Only                    |    |                                                                                                                                                                 |    |    |    |    |    |
| BIT         | 7                            | 6  | 5                                                                                                                                                               | 4  | 3  | 2  | 1  | 0  |
| Field       | <a href="#">DbgCnt[7:0]</a>  |    |                                                                                                                                                                 |    |    |    |    |    |
| Reset       | 0x0                          |    |                                                                                                                                                                 |    |    |    |    |    |
| Access Type | Read Only                    |    |                                                                                                                                                                 |    |    |    |    |    |
| BITFIELD    | BITS                         |    | DESCRIPTION                                                                                                                                                     |    |    |    |    |    |
| DbgCnt      | 15:0                         |    | Rx Lane Debug count type controlled by CfgRTestCtrl.RxCntTypeSel for lane # controlled by CfgRTestCtrl.RxCntLaneSel, loaded on setting CfgRTestCtrl.RxLoad to 1 |    |    |    |    |    |

**[CfgRLaneSet \(0x480, 0x490, 0x4A0, 0x4B0, 0x4C0\)](#)**

Configure Rx Lane Settings

| BIT         | 31                         | 30 | 29 | 28 | 27 | 26 | 25                    | 24                   |
|-------------|----------------------------|----|----|----|----|----|-----------------------|----------------------|
| Field       | <a href="#">LnSrc[4:0]</a> |    |    |    |    | –  | <a href="#">LkSel</a> | <a href="#">LnEn</a> |
| Reset       | 0x0                        |    |    |    |    | –  | 0x1                   | 0x0                  |
| Access Type | Write, Read                |    |    |    |    | –  | Write, Read           | Write, Read          |
| BIT         | 23                         | 22 | 21 | 20 | 19 | 18 | 17                    | 16                   |
| Field       | –                          | –  | –  | –  | –  | –  | –                     | –                    |
| Reset       | –                          | –  | –  | –  | –  | –  | –                     | –                    |
| Access Type | –                          | –  | –  | –  | –  | –  | –                     | –                    |

| BIT         | 15 | 14 | 13                       | 12 | 11 | 10 | 9 | 8                     |
|-------------|----|----|--------------------------|----|----|----|---|-----------------------|
| Field       | –  | –  | –                        | –  | –  | –  | – | –                     |
| Reset       | –  | –  | –                        | –  | –  | –  | – | –                     |
| Access Type | –  | –  | –                        | –  | –  | –  | – | –                     |
| BIT         | 7  | 6  | 5                        | 4  | 3  | 2  | 1 | 0                     |
| Field       | –  | –  | <a href="#">LID[4:0]</a> |    |    |    |   | <a href="#">LnRst</a> |
| Reset       | –  | –  | 0x0                      |    |    |    |   | 0x0                   |
| Access Type | –  | –  | Write, Read              |    |    |    |   | Write, Read           |

| BITFIELD | BITS  | DESCRIPTION                                                                   | DECODE                                                                                                                                                                                         |
|----------|-------|-------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LnSrc    | 31:27 | Physical Rx Lane number sourced for Logical Rx Lane at lane-to-sample mapping |                                                                                                                                                                                                |
| LkSel    | 25    | ILA Lock Select Control                                                       | 0: Lane is excluded from ILA process<br>1: Lane is included in ILA process based on FIFO write start, ILA is performed in subclass 0 by waiting for FIFO writes on all Lanes with this bit set |
| LnEn     | 24    | Rx Lane Enable Control                                                        | 0: Rx Lane is Disabled<br>1: Rx Lane is Enabled                                                                                                                                                |
| LID      | 5:1   | Lane ID for used for ILA sequence checking                                    |                                                                                                                                                                                                |
| LnRst    | 0     | Lane reset control                                                            | 0: Rx Lane is not in reset<br>1: Rx Lane is in reset                                                                                                                                           |

**[CfgRLaneIntEn \(0x484, 0x494, 0x4A4, 0x4B4, 0x4C4\)](#)**

Configure Rx Lane Interrupt Enables

| BIT         | 31 | 30                       | 29 | 28                      | 27                       | 26                      | 25                        | 24                       |
|-------------|----|--------------------------|----|-------------------------|--------------------------|-------------------------|---------------------------|--------------------------|
| Field       | –  | <a href="#">DContErr</a> | –  | <a href="#">PRBSerr</a> | <a href="#">KContErr</a> | <a href="#">FChkErr</a> | <a href="#">LCfgErr</a>   | <a href="#">ILAerr</a>   |
| Reset       | –  | 0x0                      | –  | 0x0                     | 0x0                      | 0x0                     | 0x0                       | 0x0                      |
| Access Type | –  | Write, Read              | –  | Write, Read             | Write, Read              | Write, Read             | Write, Read               | Write, Read              |
| BIT         | 23 | 22                       | 21 | 20                      | 19                       | 18                      | 17                        | 16                       |
| Field       | –  | –                        | –  | –                       | –                        | –                       | <a href="#">FIFOempty</a> | <a href="#">FIFOfull</a> |
| Reset       | –  | –                        | –  | –                       | –                        | –                       | 0x0                       | 0x0                      |
| Access Type | –  | –                        | –  | –                       | –                        | –                       | Write, Read               | Write, Read              |
| BIT         | 15 | 14                       | 13 | 12                      | 11                       | 10                      | 9                         | 8                        |
| Field       | –  | –                        | –  | –                       | –                        | –                       | –                         | –                        |
| Reset       | –  | –                        | –  | –                       | –                        | –                       | –                         | –                        |
| Access Type | –  | –                        | –  | –                       | –                        | –                       | –                         | –                        |

| BIT         | 7                       | 6                         | 5                         | 4 | 3 | 2                    | 1                   | 0                   |
|-------------|-------------------------|---------------------------|---------------------------|---|---|----------------------|---------------------|---------------------|
| Field       | <a href="#">FrNSync</a> | <a href="#">LnReAlign</a> | <a href="#">FrReAlign</a> | – | – | <a href="#">DISP</a> | <a href="#">NIT</a> | <a href="#">CGS</a> |
| Reset       | 0x0                     | 0x0                       | 0x0                       | – | – | 0x0                  | 0x0                 | 0x0                 |
| Access Type | Write, Read             | Write, Read               | Write, Read               | – | – | Write, Read          | Write, Read         | Write, Read         |

| BITFIELD  | BITS | DESCRIPTION                                                                                                 |
|-----------|------|-------------------------------------------------------------------------------------------------------------|
| DContErr  | 30   | Enable Interrupt on Rx Lane continuous D21.5 not-detect latched                                             |
| PRBSerr   | 28   | Enable Interrupt on Rx Lane SerDes interface PRBS error latched                                             |
| KContErr  | 27   | Enable Interrupt on Rx Lane continuous /K/ not-detect latched                                               |
| FChkErr   | 26   | Enable Interrupt on Rx Lane ILA sequence FCHK error latched                                                 |
| LCfgErr   | 25   | Enable Interrupt on Rx Lane ILA sequence lane configuration error latched                                   |
| ILAerr    | 24   | Enable Interrupt on Rx Lane ILA sequence decode error latched                                               |
| FIFOempty | 17   | Enable Interrupt on Rx Lane FIFO empty detected on FIFO depth smaller than RLinkRegs.CfgRFIFO.MinFD latched |
| FIFOfull  | 16   | Enable Interrupt on Rx Lane FIFO full detected on FIFO depth greater than RLinkRegs.CfgRFIFO.MaxFD latched  |
| FrNSync   | 7    | Enable Interrupt on Frame synchronization state machine not in Sync real-time                               |
| LnReAlign | 6    | Enable Interrupt on Lane realignment occurred latched                                                       |
| FrReAlign | 5    | Enable Interrupt on Frame realignment occurred latched                                                      |
| DISP      | 2    | Enable Interrupt on 8B10B Disparity error latched                                                           |
| NIT       | 1    | Enable Interrupt on 8B10B NIT error latched                                                                 |
| CGS       | 0    | Enable Interrupt on Code Group Synchronization out of Sync latched                                          |

**[CfgRLaneMuteEn \(0x488, 0x498, 0x4A8, 0x4B8, 0x4C8\)](#)**

Configure Rx Lane DAC Mute Enables

| BIT         | 31 | 30                       | 29 | 28                      | 27                       | 26                      | 25                      | 24                     |
|-------------|----|--------------------------|----|-------------------------|--------------------------|-------------------------|-------------------------|------------------------|
| Field       | –  | <a href="#">DContErr</a> | –  | <a href="#">PRBSerr</a> | <a href="#">KContErr</a> | <a href="#">FChkErr</a> | <a href="#">LCfgErr</a> | <a href="#">ILAerr</a> |
| Reset       | –  | 0x0                      | –  | 0x0                     | 0x0                      | 0x0                     | 0x0                     | 0x0                    |
| Access Type | –  | Write, Read              | –  | Write, Read             | Write, Read              | Write, Read             | Write, Read             | Write, Read            |

| BIT         | 23 | 22 | 21 | 20 | 19 | 18 | 17                        | 16                       |
|-------------|----|----|----|----|----|----|---------------------------|--------------------------|
| Field       | –  | –  | –  | –  | –  | –  | <a href="#">FIFOempty</a> | <a href="#">FIFOfull</a> |
| Reset       | –  | –  | –  | –  | –  | –  | 0x0                       | 0x0                      |
| Access Type | –  | –  | –  | –  | –  | –  | Write, Read               | Write, Read              |

| BIT         | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------|----|----|----|----|----|----|---|---|
| Field       | –  | –  | –  | –  | –  | –  | – | – |
| Reset       | –  | –  | –  | –  | –  | –  | – | – |
| Access Type | –  | –  | –  | –  | –  | –  | – | – |

| BIT         | 7                       | 6                         | 5                         | 4 | 3 | 2                    | 1                   | 0                   |
|-------------|-------------------------|---------------------------|---------------------------|---|---|----------------------|---------------------|---------------------|
| Field       | <a href="#">FrNSync</a> | <a href="#">LnReAlign</a> | <a href="#">FrReAlign</a> | – | – | <a href="#">DISP</a> | <a href="#">NIT</a> | <a href="#">CGS</a> |
| Reset       | 0x0                     | 0x0                       | 0x0                       | – | – | 0x0                  | 0x0                 | 0x0                 |
| Access Type | Write, Read             | Write, Read               | Write, Read               | – | – | Write, Read          | Write, Read         | Write, Read         |

| BITFIELD  | BITS | DESCRIPTION                                                                                            |
|-----------|------|--------------------------------------------------------------------------------------------------------|
| DContErr  | 30   | Enable Mute on Rx Lane continuous D21.5 not-detect latched                                             |
| PRBSerr   | 28   | Enable Mute on Rx Lane SerDes interface PRBS error latched                                             |
| KContErr  | 27   | Enable Mute on Rx Lane continuous /K/ not-detect latched                                               |
| FChkErr   | 26   | Enable Mute on Rx Lane ILA sequence FCHK error latched                                                 |
| LCfgErr   | 25   | Enable Mute on Rx Lane ILA sequence lane configuration error latched                                   |
| ILAerr    | 24   | Enable Mute on Rx Lane ILA sequence decode error latched                                               |
| FIFOempty | 17   | Enable Mute on Rx Lane FIFO empty detected on FIFO depth smaller than RLinkRegs.CfgRFIFO.MinFD latched |
| FIFOfull  | 16   | Enable Mute on Rx Lane FIFO full detected on FIFO depth greater than RLinkRegs.CfgRFIFO.MaxFD latched  |
| FrNSync   | 7    | Enable Mute on Frame synchronization state machine not in Sync real-time                               |
| LnReAlign | 6    | Enable Mute on Lane realignment occurred latched                                                       |
| FrReAlign | 5    | Enable Mute on Frame realignment occurred latched                                                      |
| DISP      | 2    | Enable Mute on 8B10B Disparity error latched                                                           |
| NIT       | 1    | Enable Mute on 8B10B NIT error latched                                                                 |
| CGS       | 0    | Enable Mute on Code Group Synchronization out of Sync latched                                          |

**[StatRLane \(0x48C, 0x49C, 0x4AC, 0x4BC, 0x4CC\)](#)****Rx Lane Status Register**

| BIT         | 31 | 30                       | 29                             | 28                      | 27                       | 26                      | 25                        | 24                       |
|-------------|----|--------------------------|--------------------------------|-------------------------|--------------------------|-------------------------|---------------------------|--------------------------|
| Field       | –  | <a href="#">DContErr</a> | –                              | <a href="#">PRBSerr</a> | <a href="#">KContErr</a> | <a href="#">FChkErr</a> | <a href="#">LCfgErr</a>   | <a href="#">ILAerr</a>   |
| Reset       | –  | 0x0                      | –                              | 0x0                     | 0x0                      | 0x0                     | 0x0                       | 0x0                      |
| Access Type | –  | Write 0 to Clear, Read   | –                              | Write 0 to Clear, Read  | Write 0 to Clear, Read   | Write 0 to Clear, Read  | Write 0 to Clear, Read    | Write 0 to Clear, Read   |
| BIT         | 23 | 22                       | 21                             | 20                      | 19                       | 18                      | 17                        | 16                       |
| Field       | –  | –                        | –                              | –                       | –                        | –                       | <a href="#">FIFOempty</a> | <a href="#">FIFOfull</a> |
| Reset       | –  | –                        | –                              | –                       | –                        | –                       | 0x0                       | 0x0                      |
| Access Type | –  | –                        | –                              | –                       | –                        | –                       | Write 0 to Clear, Read    | Write 0 to Clear, Read   |
| BIT         | 15 | 14                       | 13                             | 12                      | 11                       | 10                      | 9                         | 8                        |
| Field       | –  | –                        | <a href="#">FIFODepth[5:0]</a> |                         |                          |                         |                           |                          |
| Reset       | –  | –                        | 0x0                            |                         |                          |                         |                           |                          |
| Access Type | –  | –                        | Read Only                      |                         |                          |                         |                           |                          |

| BIT         | 7                       | 6                         | 5                         | 4 | 3 | 2                      | 1                      | 0                      |
|-------------|-------------------------|---------------------------|---------------------------|---|---|------------------------|------------------------|------------------------|
| Field       | <a href="#">FrNSync</a> | <a href="#">LnReAlign</a> | <a href="#">FrReAlign</a> | – | – | <a href="#">DISP</a>   | <a href="#">NIT</a>    | <a href="#">CGS</a>    |
| Reset       | 0x0                     | 0x0                       | 0x0                       | – | – | 0x0                    | 0x0                    | 0x0                    |
| Access Type | Read Only               | Write 0 to Clear, Read    | Write 0 to Clear, Read    | – | – | Write 0 to Clear, Read | Write 0 to Clear, Read | Write 0 to Clear, Read |

| BITFIELD  | BITS | DESCRIPTION                                                                                                                                                                   |
|-----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DContErr  | 30   | Rx Lane continuous D21.5 not-detect latched                                                                                                                                   |
| PRBSerr   | 28   | Rx Lane SerDes interface PRBS error latched                                                                                                                                   |
| KContErr  | 27   | Rx Lane continuous /K/ not-detect latched                                                                                                                                     |
| FChkErr   | 26   | Rx Lane ILA sequence FCHK error latched                                                                                                                                       |
| LCfgErr   | 25   | Rx Lane ILA sequence lane configuration error latched                                                                                                                         |
| ILAerr    | 24   | Rx Lane ILA sequence decode error latched                                                                                                                                     |
| FIFOempty | 17   | Rx Lane FIFO empty detected on FIFO depth smaller than RLinkRegs.CfgRFIFO.MinFD latched                                                                                       |
| FIFOfull  | 16   | Rx Lane FIFO full detected on FIFO depth greater than RLinkRegs.CfgRFIFO.MaxFD latched                                                                                        |
| FIFOdepth | 13:8 | Rx Lane FIFO depth real-time updated when RLinkRegs.CfgRTTestCtrl.SamLoad is set to 1                                                                                         |
| FrNSync   | 7    | Frame synchronization state machine not in Sync real-time                                                                                                                     |
| LnReAlign | 6    | Lane realignment occurred latched                                                                                                                                             |
| FrReAlign | 5    | Frame realignment occurred latched                                                                                                                                            |
| DISP      | 2    | 8B10B Disparity error latched                                                                                                                                                 |
| NIT       | 1    | 8B10B NIT error latched                                                                                                                                                       |
| CGS       | 0    | Code Group Synchronization out of Sync latched indicating that Lane configuration (excluding FCHK) described in section 8.3 of JESD204B-01 mismatches the local configuration |

**[CfgSerDes \(0x600\)](#)**

SerDes common configuration for all lanes

| BIT         | 31 | 30 | 29 | 28 | 27 | 26 | 25                             | 24 |
|-------------|----|----|----|----|----|----|--------------------------------|----|
| Field       | –  | –  | –  | –  | –  | –  | –                              | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –                              | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –                              | –  |
| BIT         | 23 | 22 | 21 | 20 | 19 | 18 | 17                             | 16 |
| Field       | –  | –  | –  | –  | –  | –  | <a href="#">RxRateSel[1:0]</a> |    |
| Reset       | –  | –  | –  | –  | –  | –  | 0x3                            |    |
| Access Type | –  | –  | –  | –  | –  | –  | Write, Read                    |    |

| BIT         | 15                            | 14 | 13                         | 12 | 11 | 10                      | 9 | 8                   |
|-------------|-------------------------------|----|----------------------------|----|----|-------------------------|---|---------------------|
| Field       | –                             | –  | –                          | –  | –  | –                       | – | –                   |
| Reset       | –                             | –  | –                          | –  | –  | –                       | – | –                   |
| Access Type | –                             | –  | –                          | –  | –  | –                       | – | –                   |
| BIT         | 7                             | 6  | 5                          | 4  | 3  | 2                       | 1 | 0                   |
| Field       | <a href="#">PhyWMode[1:0]</a> |    | <a href="#">BCast[1:0]</a> |    | –  | <a href="#">PhyKill</a> | – | <a href="#">Rst</a> |
| Reset       | 0x0                           |    | 0x0                        |    | –  | 0x0                     | – | 0x1                 |
| Access Type | Write, Read                   |    | Write, Read                |    | –  | Write, Read             | – | Write, Read         |

| BITFIELD  | BITS  | DESCRIPTION                              | DECODE                                                                                                                                                                       |
|-----------|-------|------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RxRateSel | 17:16 | Rx Rate select for CDR                   | 0: Eighth rate<br>1: Quarter rate<br>2: Half rate<br>3: Full rate                                                                                                            |
| PhyWMode  | 7:6   | PHY 32-bit register interface write mode | 0: Buffer upper 3 bytes and transfer all 4 bytes on write to byte0<br>1: Buffer lower 3 bytes and transfer all 4 bytes on write to byte3<br>2: Enable individual byte writes |
| BCast     | 5:4   | PHY register broadcast write control     | 0: No Broadcast CPU writes to all PHYs<br>1: Broadcast CPU writes to all PHYs<br>2: Broadcast CPU writes to all PHYs enabled in RxLink<br>3: Reserved                        |
| PhyKill   | 2     | SerDes PHY Kill control                  | 0: SerDes PHY not in kill state<br>1: SerDes PHY in kill state                                                                                                               |
| Rst       | 0     | RLMS block Reset control                 | 0: RLMS block not in reset state<br>1: RLMS block in reset state                                                                                                             |

**CfgTrainAct (0x608)**

Force activate training control

| BIT         | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |
| BIT         | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 15 | 14 | 13 | 12                   | 11                   | 10                   | 9                    | 8                    |
|-------------|----|----|----|----------------------|----------------------|----------------------|----------------------|----------------------|
| Field       | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| Reset       | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| Access Type | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| BIT         | 7  | 6  | 5  | 4                    | 3                    | 2                    | 1                    | 0                    |
| Field       | –  | –  | –  | <a href="#">Ln_4</a> | <a href="#">Ln_3</a> | <a href="#">Ln_2</a> | <a href="#">Ln_1</a> | <a href="#">Ln_0</a> |
| Reset       | –  | –  | –  | 0x0                  | 0x0                  | 0x0                  | 0x0                  | 0x0                  |
| Access Type | –  | –  | –  | Write, Read          | Write, Read          | Write, Read          | Write, Read          | Write, Read          |

| BITFIELD | BITS | DESCRIPTION                        | DECODE                                                      |
|----------|------|------------------------------------|-------------------------------------------------------------|
| Ln__4    | 4    | Force activate training for Lane N | 0: Do not force training active<br>1: Force training active |
| Ln__3    | 3    | Force activate training for Lane N | 0: Do not force training active<br>1: Force training active |
| Ln__2    | 2    | Force activate training for Lane N | 0: Do not force training active<br>1: Force training active |
| Ln__1    | 1    | Force activate training for Lane N | 0: Do not force training active<br>1: Force training active |
| Ln__0    | 0    | Force activate training for Lane N | 0: Do not force training active<br>1: Force training active |

**CfgTrainDeAct (0x60C)**

Force activate training control

| BIT         | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |
| BIT         | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |
| BIT         | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 7 | 6 | 5 | 4                    | 3                    | 2                    | 1                    | 0                    |
|-------------|---|---|---|----------------------|----------------------|----------------------|----------------------|----------------------|
| Field       | – | – | – | <a href="#">Ln_4</a> | <a href="#">Ln_3</a> | <a href="#">Ln_2</a> | <a href="#">Ln_1</a> | <a href="#">Ln_0</a> |
| Reset       | – | – | – | 0x1                  | 0x1                  | 0x1                  | 0x1                  | 0x1                  |
| Access Type | – | – | – | Write, Read          | Write, Read          | Write, Read          | Write, Read          | Write, Read          |

| BITFIELD | BITS | DESCRIPTION                          | DECODE                                                          |
|----------|------|--------------------------------------|-----------------------------------------------------------------|
| Ln__4    | 4    | Force deactivate training for Lane N | 0: Do not force training deactive<br>1: Force training deactive |
| Ln__3    | 3    | Force deactivate training for Lane N | 0: Do not force training deactive<br>1: Force training deactive |
| Ln__2    | 2    | Force deactivate training for Lane N | 0: Do not force training deactive<br>1: Force training deactive |
| Ln__1    | 1    | Force deactivate training for Lane N | 0: Do not force training deactive<br>1: Force training deactive |
| Ln__0    | 0    | Force deactivate training for Lane N | 0: Do not force training deactive<br>1: Force training deactive |

**[CfgIdleGate \(0x610\)](#)**

Gate data off to RxLink on SerDes SigDet control

| BIT         | 31   | 30                                       | 29 | 28                   | 27                                                | 26                   | 25                   | 24                   |
|-------------|------|------------------------------------------|----|----------------------|---------------------------------------------------|----------------------|----------------------|----------------------|
| Field       | –    | –                                        | –  | –                    | –                                                 | –                    | –                    | –                    |
| Reset       | –    | –                                        | –  | –                    | –                                                 | –                    | –                    | –                    |
| Access Type | –    | –                                        | –  | –                    | –                                                 | –                    | –                    | –                    |
|             |      |                                          |    |                      |                                                   |                      |                      |                      |
| BIT         | 23   | 22                                       | 21 | 20                   | 19                                                | 18                   | 17                   | 16                   |
| Field       | –    | –                                        | –  | –                    | –                                                 | –                    | –                    | –                    |
| Reset       | –    | –                                        | –  | –                    | –                                                 | –                    | –                    | –                    |
| Access Type | –    | –                                        | –  | –                    | –                                                 | –                    | –                    | –                    |
|             |      |                                          |    |                      |                                                   |                      |                      |                      |
| BIT         | 15   | 14                                       | 13 | 12                   | 11                                                | 10                   | 9                    | 8                    |
| Field       | –    | –                                        | –  | –                    | –                                                 | –                    | –                    | –                    |
| Reset       | –    | –                                        | –  | –                    | –                                                 | –                    | –                    | –                    |
| Access Type | –    | –                                        | –  | –                    | –                                                 | –                    | –                    | –                    |
|             |      |                                          |    |                      |                                                   |                      |                      |                      |
| BIT         | 7    | 6                                        | 5  | 4                    | 3                                                 | 2                    | 1                    | 0                    |
| Field       | –    | –                                        | –  | <a href="#">Ln_4</a> | <a href="#">Ln_3</a>                              | <a href="#">Ln_2</a> | <a href="#">Ln_1</a> | <a href="#">Ln_0</a> |
| Reset       | –    | –                                        | –  | 0x1                  | 0x1                                               | 0x1                  | 0x1                  | 0x1                  |
| Access Type | –    | –                                        | –  | Write, Read          | Write, Read                                       | Write, Read          | Write, Read          | Write, Read          |
|             |      |                                          |    |                      |                                                   |                      |                      |                      |
| BITFIELD    | BITS | DESCRIPTION                              |    |                      | DECODE                                            |                      |                      |                      |
| Ln_4        | 4    | Gate data off to RxLink on SerDes SigDet |    |                      | 0: Do no gate data off to RxLink on SerDes SigDet |                      |                      |                      |

| BITLEN | BITFIELD | BITS | DESCRIPTION                                                 | DECODE                                                                                                                |
|--------|----------|------|-------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|
|        |          |      | control for Lane N                                          | 1: Gate data off to RxLink when SerDes SigDet is high for lane N                                                      |
| Ln__3  |          | 3    | Gate data off to RxLink on SerDes SigDet control for Lane N | 0: Do no gate data off to RxLink on SerDes SigDet<br>1: Gate data off to RxLink when SerDes SigDet is high for lane N |
| Ln__2  |          | 2    | Gate data off to RxLink on SerDes SigDet control for Lane N | 0: Do no gate data off to RxLink on SerDes SigDet<br>1: Gate data off to RxLink when SerDes SigDet is high for lane N |
| Ln__1  |          | 1    | Gate data off to RxLink on SerDes SigDet control for Lane N | 0: Do no gate data off to RxLink on SerDes SigDet<br>1: Gate data off to RxLink when SerDes SigDet is high for lane N |
| Ln__0  |          | 0    | Gate data off to RxLink on SerDes SigDet control for Lane N | 0: Do no gate data off to RxLink on SerDes SigDet<br>1: Gate data off to RxLink when SerDes SigDet is high for lane N |

**CfgDoneGate (0x614)**

Gate data off to RxLink on SerDes TrainDone control

| BIT         | 31   | 30                                                             | 29 | 28                   | 27                                                                                                                          | 26                   | 25                   | 24                   |
|-------------|------|----------------------------------------------------------------|----|----------------------|-----------------------------------------------------------------------------------------------------------------------------|----------------------|----------------------|----------------------|
| Field       | —    | —                                                              | —  | —                    | —                                                                                                                           | —                    | —                    | —                    |
| Reset       | —    | —                                                              | —  | —                    | —                                                                                                                           | —                    | —                    | —                    |
| Access Type | —    | —                                                              | —  | —                    | —                                                                                                                           | —                    | —                    | —                    |
|             |      |                                                                |    |                      |                                                                                                                             |                      |                      |                      |
| BIT         | 23   | 22                                                             | 21 | 20                   | 19                                                                                                                          | 18                   | 17                   | 16                   |
| Field       | —    | —                                                              | —  | —                    | —                                                                                                                           | —                    | —                    | —                    |
| Reset       | —    | —                                                              | —  | —                    | —                                                                                                                           | —                    | —                    | —                    |
| Access Type | —    | —                                                              | —  | —                    | —                                                                                                                           | —                    | —                    | —                    |
|             |      |                                                                |    |                      |                                                                                                                             |                      |                      |                      |
| BIT         | 15   | 14                                                             | 13 | 12                   | 11                                                                                                                          | 10                   | 9                    | 8                    |
| Field       | —    | —                                                              | —  | —                    | —                                                                                                                           | —                    | —                    | —                    |
| Reset       | —    | —                                                              | —  | —                    | —                                                                                                                           | —                    | —                    | —                    |
| Access Type | —    | —                                                              | —  | —                    | —                                                                                                                           | —                    | —                    | —                    |
|             |      |                                                                |    |                      |                                                                                                                             |                      |                      |                      |
| BIT         | 7    | 6                                                              | 5  | 4                    | 3                                                                                                                           | 2                    | 1                    | 0                    |
| Field       | —    | —                                                              | —  | <a href="#">Ln_4</a> | <a href="#">Ln_3</a>                                                                                                        | <a href="#">Ln_2</a> | <a href="#">Ln_1</a> | <a href="#">Ln_0</a> |
| Reset       | —    | —                                                              | —  | 0x1                  | 0x1                                                                                                                         | 0x1                  | 0x1                  | 0x1                  |
| Access Type | —    | —                                                              | —  | Write, Read          | Write, Read                                                                                                                 | Write, Read          | Write, Read          | Write, Read          |
|             |      |                                                                |    |                      |                                                                                                                             |                      |                      |                      |
| BITFIELD    | BITS | DESCRIPTION                                                    |    |                      | DECODE                                                                                                                      |                      |                      |                      |
| Ln__4       | 4    | Gate data off to RxLink on SerDes TrainDone control for Lane N |    |                      | 0: Do not gate data off to RxLink on SerDes TrainDone<br>1: Gate data off to RxLink when SerDes TrainDone is low for lane N |                      |                      |                      |

| BITFIELD | BITS | DESCRIPTION                                                    | DECODE                                                                                                                      |
|----------|------|----------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|
| Ln__3    | 3    | Gate data off to RxLink on SerDes TrainDone control for Lane N | 0: Do not gate data off to RxLink on SerDes TrainDone<br>1: Gate data off to RxLink when SerDes TrainDone is low for lane N |
| Ln__2    | 2    | Gate data off to RxLink on SerDes TrainDone control for Lane N | 0: Do not gate data off to RxLink on SerDes TrainDone<br>1: Gate data off to RxLink when SerDes TrainDone is low for lane N |
| Ln__1    | 1    | Gate data off to RxLink on SerDes TrainDone control for Lane N | 0: Do not gate data off to RxLink on SerDes TrainDone<br>1: Gate data off to RxLink when SerDes TrainDone is low for lane N |
| Ln__0    | 0    | Gate data off to RxLink on SerDes TrainDone control for Lane N | 0: Do not gate data off to RxLink on SerDes TrainDone<br>1: Gate data off to RxLink when SerDes TrainDone is low for lane N |

**CfgReserved (0x618)**

CfgReserved for future use

| BIT         | 31                         | 30   | 29 | 28          | 27 | 26 | 25 | 24 |
|-------------|----------------------------|------|----|-------------|----|----|----|----|
| Field       | –                          | –    | –  | –           | –  | –  | –  | –  |
| Reset       | –                          | –    | –  | –           | –  | –  | –  | –  |
| Access Type | –                          | –    | –  | –           | –  | –  | –  | –  |
|             |                            |      |    |             |    |    |    |    |
| BIT         | 23                         | 22   | 21 | 20          | 19 | 18 | 17 | 16 |
| Field       | –                          | –    | –  | –           | –  | –  | –  | –  |
| Reset       | –                          | –    | –  | –           | –  | –  | –  | –  |
| Access Type | –                          | –    | –  | –           | –  | –  | –  | –  |
|             |                            |      |    |             |    |    |    |    |
| BIT         | 15                         | 14   | 13 | 12          | 11 | 10 | 9  | 8  |
| Field       | <a href="#">Rsvd[15:8]</a> |      |    |             |    |    |    |    |
| Reset       | 0x0                        |      |    |             |    |    |    |    |
| Access Type | Write, Read                |      |    |             |    |    |    |    |
|             |                            |      |    |             |    |    |    |    |
| BIT         | 7                          | 6    | 5  | 4           | 3  | 2  | 1  | 0  |
| Field       | <a href="#">Rsvd[7:0]</a>  |      |    |             |    |    |    |    |
| Reset       | 0x0                        |      |    |             |    |    |    |    |
| Access Type | Write, Read                |      |    |             |    |    |    |    |
|             |                            |      |    |             |    |    |    |    |
| BITFIELD    |                            | BITS |    | DESCRIPTION |    |    |    |    |
| Rsvd        |                            | 15:0 |    | Reserved    |    |    |    |    |

**CfgIntEnRLMS (0x61C)**

Interrupt Enable register for RLMS block status

| BIT         | 31 | 30 | 29 | 28                   | 27                   | 26                   | 25                   | 24                   |
|-------------|----|----|----|----------------------|----------------------|----------------------|----------------------|----------------------|
| Field       | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| Reset       | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| Access Type | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| BIT         | 23 | 22 | 21 | 20                   | 19                   | 18                   | 17                   | 16                   |
| Field       | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| Reset       | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| Access Type | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| BIT         | 15 | 14 | 13 | 12                   | 11                   | 10                   | 9                    | 8                    |
| Field       | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| Reset       | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| Access Type | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| BIT         | 7  | 6  | 5  | 4                    | 3                    | 2                    | 1                    | 0                    |
| Field       | –  | –  | –  | <a href="#">Ln_4</a> | <a href="#">Ln_3</a> | <a href="#">Ln_2</a> | <a href="#">Ln_1</a> | <a href="#">Ln_0</a> |
| Reset       | –  | –  | –  | 0x0                  | 0x0                  | 0x0                  | 0x0                  | 0x0                  |
| Access Type | –  | –  | –  | Write, Read          | Write, Read          | Write, Read          | Write, Read          | Write, Read          |

| BITFIELD             | BITS | DESCRIPTION                                |
|----------------------|------|--------------------------------------------|
| <a href="#">Ln_4</a> | 4    | Enable interrupt on RLMS status for Lane N |
| <a href="#">Ln_3</a> | 3    | Enable interrupt on RLMS status for Lane N |
| <a href="#">Ln_2</a> | 2    | Enable interrupt on RLMS status for Lane N |
| <a href="#">Ln_1</a> | 1    | Enable interrupt on RLMS status for Lane N |
| <a href="#">Ln_0</a> | 0    | Enable interrupt on RLMS status for Lane N |

**CfgIntEnTrainDn (0x620)**

Interrupt Enable register for Training Done status

| BIT         | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 23 | 22 | 21 | 20                   | 19                   | 18                   | 17                   | 16                   |
|-------------|----|----|----|----------------------|----------------------|----------------------|----------------------|----------------------|
| Field       | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| Reset       | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| Access Type | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| BIT         | 15 | 14 | 13 | 12                   | 11                   | 10                   | 9                    | 8                    |
| Field       | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| Reset       | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| Access Type | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| BIT         | 7  | 6  | 5  | 4                    | 3                    | 2                    | 1                    | 0                    |
| Field       | –  | –  | –  | <a href="#">Ln_4</a> | <a href="#">Ln_3</a> | <a href="#">Ln_2</a> | <a href="#">Ln_1</a> | <a href="#">Ln_0</a> |
| Reset       | –  | –  | –  | 0x0                  | 0x0                  | 0x0                  | 0x0                  | 0x0                  |
| Access Type | –  | –  | –  | Write, Read          | Write, Read          | Write, Read          | Write, Read          | Write, Read          |

| BITFIELD             | BITS | DESCRIPTION                                  |
|----------------------|------|----------------------------------------------|
| <a href="#">Ln_4</a> | 4    | Enable interrupt on Training done for Lane N |
| <a href="#">Ln_3</a> | 3    | Enable interrupt on Training done for Lane N |
| <a href="#">Ln_2</a> | 2    | Enable interrupt on Training done for Lane N |
| <a href="#">Ln_1</a> | 1    | Enable interrupt on Training done for Lane N |
| <a href="#">Ln_0</a> | 0    | Enable interrupt on Training done for Lane N |

**[CfgIntEnSigDet \(0x624\)](#)**

Interrupt Enable register for Signal Detect status

| BIT         | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |
| BIT         | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |
| BIT         | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 7 | 6 | 5 | 4                    | 3                    | 2                    | 1                    | 0                    |
|-------------|---|---|---|----------------------|----------------------|----------------------|----------------------|----------------------|
| Field       | – | – | – | <a href="#">Ln_4</a> | <a href="#">Ln_3</a> | <a href="#">Ln_2</a> | <a href="#">Ln_1</a> | <a href="#">Ln_0</a> |
| Reset       | – | – | – | 0x0                  | 0x0                  | 0x0                  | 0x0                  | 0x0                  |
| Access Type | – | – | – | Write, Read          | Write, Read          | Write, Read          | Write, Read          | Write, Read          |

| BITFIELD             | BITS | DESCRIPTION                                  |
|----------------------|------|----------------------------------------------|
| <a href="#">Ln_4</a> | 4    | Enable interrupt on Signal Detect for Lane N |
| <a href="#">Ln_3</a> | 3    | Enable interrupt on Signal Detect for Lane N |
| <a href="#">Ln_2</a> | 2    | Enable interrupt on Signal Detect for Lane N |
| <a href="#">Ln_1</a> | 1    | Enable interrupt on Signal Detect for Lane N |
| <a href="#">Ln_0</a> | 0    | Enable interrupt on Signal Detect for Lane N |

**[CfgMuteEnRLMS \(0x628\)](#)**

Mute Enable register for RLMS block status

| BIT         | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------|----|----|----|----|----|----|---|---|
| Field       | –  | –  | –  | –  | –  | –  | – | – |
| Reset       | –  | –  | –  | –  | –  | –  | – | – |
| Access Type | –  | –  | –  | –  | –  | –  | – | – |

| BIT         | 7 | 6 | 5 | 4                    | 3                    | 2                    | 1                    | 0                    |
|-------------|---|---|---|----------------------|----------------------|----------------------|----------------------|----------------------|
| Field       | – | – | – | <a href="#">Ln_4</a> | <a href="#">Ln_3</a> | <a href="#">Ln_2</a> | <a href="#">Ln_1</a> | <a href="#">Ln_0</a> |
| Reset       | – | – | – | 0x0                  | 0x0                  | 0x0                  | 0x0                  | 0x0                  |
| Access Type | – | – | – | Write, Read          | Write, Read          | Write, Read          | Write, Read          | Write, Read          |

| BITFIELD             | BITS | DESCRIPTION                               |
|----------------------|------|-------------------------------------------|
| <a href="#">Ln_4</a> | 4    | Enable DAC mute on RLMS status for Lane N |
| <a href="#">Ln_3</a> | 3    | Enable DAC mute on RLMS status for Lane N |
| <a href="#">Ln_2</a> | 2    | Enable DAC mute on RLMS status for Lane N |
| <a href="#">Ln_1</a> | 1    | Enable DAC mute on RLMS status for Lane N |

| BITFIELD | BITS | DESCRIPTION                               |
|----------|------|-------------------------------------------|
| Ln__0    | 0    | Enable DAC mute on RLMS status for Lane N |

**CfgMuteEnTrainDn (0x62C)**

Mute Enable register for Training Done status

| BIT         | 31 | 30 | 29 | 28                    | 27                    | 26                    | 25                    | 24                    |
|-------------|----|----|----|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| Field       | –  | –  | –  | –                     | –                     | –                     | –                     | –                     |
| Reset       | –  | –  | –  | –                     | –                     | –                     | –                     | –                     |
| Access Type | –  | –  | –  | –                     | –                     | –                     | –                     | –                     |
| BIT         | 23 | 22 | 21 | 20                    | 19                    | 18                    | 17                    | 16                    |
| Field       | –  | –  | –  | –                     | –                     | –                     | –                     | –                     |
| Reset       | –  | –  | –  | –                     | –                     | –                     | –                     | –                     |
| Access Type | –  | –  | –  | –                     | –                     | –                     | –                     | –                     |
| BIT         | 15 | 14 | 13 | 12                    | 11                    | 10                    | 9                     | 8                     |
| Field       | –  | –  | –  | –                     | –                     | –                     | –                     | –                     |
| Reset       | –  | –  | –  | –                     | –                     | –                     | –                     | –                     |
| Access Type | –  | –  | –  | –                     | –                     | –                     | –                     | –                     |
| BIT         | 7  | 6  | 5  | 4                     | 3                     | 2                     | 1                     | 0                     |
| Field       | –  | –  | –  | <a href="#">Ln__4</a> | <a href="#">Ln__3</a> | <a href="#">Ln__2</a> | <a href="#">Ln__1</a> | <a href="#">Ln__0</a> |
| Reset       | –  | –  | –  | 0x0                   | 0x0                   | 0x0                   | 0x0                   | 0x0                   |
| Access Type | –  | –  | –  | Write, Read           | Write, Read           | Write, Read           | Write, Read           | Write, Read           |

| BITFIELD | BITS | DESCRIPTION                                 |
|----------|------|---------------------------------------------|
| Ln__4    | 4    | Enable DAC mute on Training done for Lane N |
| Ln__3    | 3    | Enable DAC mute on Training done for Lane N |
| Ln__2    | 2    | Enable DAC mute on Training done for Lane N |
| Ln__1    | 1    | Enable DAC mute on Training done for Lane N |
| Ln__0    | 0    | Enable DAC mute on Training done for Lane N |

**CfgMuteEnSigDet (0x630)**

Mute Enable register for Signal Detect status

| BIT         | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 23 | 22 | 21 | 20                   | 19                   | 18                   | 17                   | 16                   |
|-------------|----|----|----|----------------------|----------------------|----------------------|----------------------|----------------------|
| Field       | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| Reset       | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| Access Type | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| BIT         | 15 | 14 | 13 | 12                   | 11                   | 10                   | 9                    | 8                    |
| Field       | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| Reset       | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| Access Type | –  | –  | –  | –                    | –                    | –                    | –                    | –                    |
| BIT         | 7  | 6  | 5  | 4                    | 3                    | 2                    | 1                    | 0                    |
| Field       | –  | –  | –  | <a href="#">Ln_4</a> | <a href="#">Ln_3</a> | <a href="#">Ln_2</a> | <a href="#">Ln_1</a> | <a href="#">Ln_0</a> |
| Reset       | –  | –  | –  | 0x0                  | 0x0                  | 0x0                  | 0x0                  | 0x0                  |
| Access Type | –  | –  | –  | Write, Read          | Write, Read          | Write, Read          | Write, Read          | Write, Read          |

| BITFIELD             | BITS | DESCRIPTION                                 |
|----------------------|------|---------------------------------------------|
| <a href="#">Ln_4</a> | 4    | Enable DAC mute on Signal Detect for Lane N |
| <a href="#">Ln_3</a> | 3    | Enable DAC mute on Signal Detect for Lane N |
| <a href="#">Ln_2</a> | 2    | Enable DAC mute on Signal Detect for Lane N |
| <a href="#">Ln_1</a> | 1    | Enable DAC mute on Signal Detect for Lane N |
| <a href="#">Ln_0</a> | 0    | Enable DAC mute on Signal Detect for Lane N |

**[StatRLMS \(0x634\)](#)**

RLMS status register

| BIT         | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |
| BIT         | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |
| BIT         | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 7 | 6 | 5 | 4                    | 3                    | 2                    | 1                    | 0                    |
|-------------|---|---|---|----------------------|----------------------|----------------------|----------------------|----------------------|
| Field       | – | – | – | <a href="#">Ln_4</a> | <a href="#">Ln_3</a> | <a href="#">Ln_2</a> | <a href="#">Ln_1</a> | <a href="#">Ln_0</a> |
| Reset       | – | – | – | 0x0                  | 0x0                  | 0x0                  | 0x0                  | 0x0                  |
| Access Type | – | – | – | Read Only            | Read Only            | Read Only            | Read Only            | Read Only            |

| BITFIELD             | BITS | DESCRIPTION                               |
|----------------------|------|-------------------------------------------|
| <a href="#">Ln_4</a> | 4    | RLMS combined status real-time for Lane N |
| <a href="#">Ln_3</a> | 3    | RLMS combined status real-time for Lane N |
| <a href="#">Ln_2</a> | 2    | RLMS combined status real-time for Lane N |
| <a href="#">Ln_1</a> | 1    | RLMS combined status real-time for Lane N |
| <a href="#">Ln_0</a> | 0    | RLMS combined status real-time for Lane N |

**[StatTrainDn \(0x638\)](#)**

Training done status register latched

| BIT         | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------|----|----|----|----|----|----|---|---|
| Field       | –  | –  | –  | –  | –  | –  | – | – |
| Reset       | –  | –  | –  | –  | –  | –  | – | – |
| Access Type | –  | –  | –  | –  | –  | –  | – | – |

| BIT         | 7 | 6 | 5 | 4                    | 3                    | 2                    | 1                    | 0                    |
|-------------|---|---|---|----------------------|----------------------|----------------------|----------------------|----------------------|
| Field       | – | – | – | <a href="#">Ln_4</a> | <a href="#">Ln_3</a> | <a href="#">Ln_2</a> | <a href="#">Ln_1</a> | <a href="#">Ln_0</a> |
| Reset       | – | – | – | 0x0                  | 0x0                  | 0x0                  | 0x0                  | 0x0                  |
| Access Type | – | – | – | Read Only            | Read Only            | Read Only            | Read Only            | Read Only            |

| BITFIELD             | BITS | DESCRIPTION                             |
|----------------------|------|-----------------------------------------|
| <a href="#">Ln_4</a> | 4    | Training done latched status for Lane N |
| <a href="#">Ln_3</a> | 3    | Training done latched status for Lane N |
| <a href="#">Ln_2</a> | 2    | Training done latched status for Lane N |
| <a href="#">Ln_1</a> | 1    | Training done latched status for Lane N |

| BITFIELD | BITS | DESCRIPTION                             |
|----------|------|-----------------------------------------|
| Ln__0    | 0    | Training done latched status for Lane N |

**StatSigDet (0x63C)**

SerDes Signal Detect real-time status register

| BIT         | 31 | 30 | 29 | 28                    | 27                    | 26                    | 25                    | 24                    |
|-------------|----|----|----|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| Field       | –  | –  | –  | –                     | –                     | –                     | –                     | –                     |
| Reset       | –  | –  | –  | –                     | –                     | –                     | –                     | –                     |
| Access Type | –  | –  | –  | –                     | –                     | –                     | –                     | –                     |
| BIT         | 23 | 22 | 21 | 20                    | 19                    | 18                    | 17                    | 16                    |
| Field       | –  | –  | –  | –                     | –                     | –                     | –                     | –                     |
| Reset       | –  | –  | –  | –                     | –                     | –                     | –                     | –                     |
| Access Type | –  | –  | –  | –                     | –                     | –                     | –                     | –                     |
| BIT         | 15 | 14 | 13 | 12                    | 11                    | 10                    | 9                     | 8                     |
| Field       | –  | –  | –  | –                     | –                     | –                     | –                     | –                     |
| Reset       | –  | –  | –  | –                     | –                     | –                     | –                     | –                     |
| Access Type | –  | –  | –  | –                     | –                     | –                     | –                     | –                     |
| BIT         | 7  | 6  | 5  | 4                     | 3                     | 2                     | 1                     | 0                     |
| Field       | –  | –  | –  | <a href="#">Ln__4</a> | <a href="#">Ln__3</a> | <a href="#">Ln__2</a> | <a href="#">Ln__1</a> | <a href="#">Ln__0</a> |
| Reset       | –  | –  | –  | 0x0                   | 0x0                   | 0x0                   | 0x0                   | 0x0                   |
| Access Type | –  | –  | –  | Read Only             | Read Only             | Read Only             | Read Only             | Read Only             |

| BITFIELD | BITS | DESCRIPTION                                                           |
|----------|------|-----------------------------------------------------------------------|
| Ln__4    | 4    | High indicates phy RX receivers are below the LOS threshold on Lane N |
| Ln__3    | 3    | High indicates phy RX receivers are below the LOS threshold on Lane N |
| Ln__2    | 2    | High indicates phy RX receivers are below the LOS threshold on Lane N |
| Ln__1    | 1    | High indicates phy RX receivers are below the LOS threshold on Lane N |
| Ln__0    | 0    | High indicates phy RX receivers are below the LOS threshold on Lane N |

**CfgCMU1 (0x644)**

Configure CMU word 1

| BIT         | 31                    | 30 | 29 | 28 | 27 | 26                              | 25 | 24 |
|-------------|-----------------------|----|----|----|----|---------------------------------|----|----|
| Field       | <a href="#">Rsvd1</a> | –  | –  | –  | –  | <a href="#">cd_tune1p0[2:0]</a> |    |    |
| Reset       | 0x0                   | –  | –  | –  | –  | 0x0                             |    |    |
| Access Type | Write, Read           | –  | –  | –  | –  | Write, Read                     |    |    |

| BIT         | 23                                  | 22 | 21                         | 20 | 19                           | 18 | 17 | 16 |
|-------------|-------------------------------------|----|----------------------------|----|------------------------------|----|----|----|
| Field       | <a href="#">Cref_divsel1p0[1:0]</a> |    | –                          | –  | <a href="#">Rsvd0[13:10]</a> |    |    |    |
| Reset       | 0x0                                 |    | –                          | –  | 0x0                          |    |    |    |
| Access Type | Write, Read                         |    | –                          | –  | Write, Read                  |    |    |    |
| BIT         | 15                                  | 14 | 13                         | 12 | 11                           | 10 | 9  | 8  |
| Field       | <a href="#">Rsvd0[9:2]</a>          |    |                            |    |                              |    |    |    |
| Reset       | 0x0                                 |    |                            |    |                              |    |    |    |
| Access Type | Write, Read                         |    |                            |    |                              |    |    |    |
| BIT         | 7                                   | 6  | 5                          | 4  | 3                            | 2  | 1  | 0  |
| Field       | <a href="#">Rsvd0[1:0]</a>          |    | <a href="#">FBDIV[1:0]</a> |    | <a href="#">VCOSEL[1:0]</a>  |    | –  | –  |
| Reset       | 0x0                                 |    | 0x0                        |    | 0x0                          |    | –  | –  |
| Access Type | Write, Read                         |    | Write, Read                |    | Write, Read                  |    | –  | –  |

| BITFIELD       | BITS  | DESCRIPTION                      | DECODE                                                                 |
|----------------|-------|----------------------------------|------------------------------------------------------------------------|
| Rsvd1          | 31    | Reserved 1                       |                                                                        |
| cd_tune1p0     | 26:24 | Clocktree tuning for center freq | 0: 10G<br>4: Reserved<br>7: Reserved                                   |
| Cref_divsel1p0 | 23:22 | Refclk path divider selection    | 0: Reserved<br>1: CMU refclk divide by 2<br>2: Reserved<br>3: Reserved |
| Rsvd0          | 19:6  | Reserved 0                       |                                                                        |
| FBDIV          | 5:4   | Feedback divider control         | 0: Reserved<br>1: Divide by 80<br>3: Reserved                          |
| VCOSEL         | 3:2   | VCO select                       | 0: 10G VCO<br>1: Reserved<br>2: Reserved<br>3: Reserved                |

**EQU\_CTRL3 (0x80C, 0x90C, 0xA0C, 0xB0C, 0xC0C)**

Equalizer Control 3

| BIT         | 31 | 30 | 29                            | 28 | 27 | 26 | 25 | 24 |
|-------------|----|----|-------------------------------|----|----|----|----|----|
| Field       | –  | –  | <a href="#">D1_coeff[5:0]</a> |    |    |    |    |    |
| Reset       | –  | –  | 0x4                           |    |    |    |    |    |
| Access Type | –  | –  | Write, Read                   |    |    |    |    |    |

| BIT         | 23 | 22                            | 21 | 20 | 19 | 18 | 17 | 16 |
|-------------|----|-------------------------------|----|----|----|----|----|----|
| Field       | –  | <a href="#">D2_coeff[6:0]</a> |    |    |    |    |    |    |
| Reset       | –  | 0x0                           |    |    |    |    |    |    |
| Access Type | –  | Write, Read                   |    |    |    |    |    |    |
| BIT         | 15 | 14                            | 13 | 12 | 11 | 10 | 9  | 8  |
| Field       | –  | <a href="#">D3_coeff[6:0]</a> |    |    |    |    |    |    |
| Reset       | –  | 0x0                           |    |    |    |    |    |    |
| Access Type | –  | Write, Read                   |    |    |    |    |    |    |
| BIT         | 7  | 6                             | 5  | 4  | 3  | 2  | 1  | 0  |
| Field       | –  | <a href="#">D4_coeff[6:0]</a> |    |    |    |    |    |    |
| Reset       | –  | 0x0                           |    |    |    |    |    |    |
| Access Type | –  | Write, Read                   |    |    |    |    |    |    |

| BITFIELD | BITS  | DESCRIPTION                                                                                                                                                                                                                                                                                                                            |
|----------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D1_coeff | 29:24 | DFE coefficient D1, binary-encoded magnitude, negative gain only. Drives a 6-bit magnitude DAC. Example values: 6'h00 = 0 amplitude 6'h3F = maximum negative amplitude -0.5                                                                                                                                                            |
| D2_coeff | 22:16 | DFE coefficient D2 sign/binary-encoded magnitude. Drives a 7-bit DAC with the highest bit representing the sign. Example values: 7'h3F = maximum positive amplitude = 0.25 7'h01 = smallest positive amplitude = 0.25/63 7'h00 = 0 amplitude 7'h41 = smallest negative amplitude = -0.25/63 7'h7F = maximum negative amplitude = -0.25 |
| D3_coeff | 14:8  | DFE coefficient D3 sign/binary-encoded magnitude. Drives a 7-bit DAC with the highest bit representing the sign. See D2_coeff above for examples.                                                                                                                                                                                      |
| D4_coeff | 6:0   | DFE coefficient D4 sign/binary-encoded magnitude. Drives a 7-bit DAC with the highest bit representing the sign. See D2_coeff above for examples.                                                                                                                                                                                      |

**EQU\_CTRL4 (0x810, 0x910, 0xA10, 0xB10, 0xC10)**

## Equalizer Control 4

| BIT         | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|----|----|----|----|----|----|----|----|
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |
| BIT         | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Field       | –  | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –  | –  | –  |

| BIT         | 15                             | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------|--------------------------------|----|----|----|----|----|---|---|
| Field       | –                              | –  | –  | –  | –  | –  | – | – |
| Reset       | –                              | –  | –  | –  | –  | –  | – | – |
| Access Type | –                              | –  | –  | –  | –  | –  | – | – |
| BIT         | 7                              | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| Field       | <a href="#">AGC_coeff[7:0]</a> |    |    |    |    |    |   |   |
| Reset       | 0x80                           |    |    |    |    |    |   |   |
| Access Type | Write, Read                    |    |    |    |    |    |   |   |

| BITFIELD  | BITS | DESCRIPTION                                                                             |
|-----------|------|-----------------------------------------------------------------------------------------|
| AGC_coeff | 7:0  | VGA gain, binary encoded. 00h = +10db (NOTE THIS INVERSION IS INTENTIONAL!) FFh = -10db |

**EQU\_CTRL7 (0x81C, 0x91C, 0xA1C, 0xB1C, 0xC1C)**

Equalizer Control 7

| BIT         | 31                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|----------------------------------|----|----|----|----|----|----|----|
| Field       | <a href="#">AGC_init_D1[7:0]</a> |    |    |    |    |    |    |    |
| Reset       | 0x81                             |    |    |    |    |    |    |    |
| Access Type | Write, Read                      |    |    |    |    |    |    |    |
| BIT         | 23                               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Field       | –                                | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –                                | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –                                | –  | –  | –  | –  | –  | –  | –  |
| BIT         | 15                               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| Field       | –                                | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –                                | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –                                | –  | –  | –  | –  | –  | –  | –  |
| BIT         | 7                                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Field       | –                                | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –                                | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –                                | –  | –  | –  | –  | –  | –  | –  |

| BITFIELD    | BITS  | DESCRIPTION                                                                                                                            |
|-------------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| AGC_init_D1 | 31:24 | Full-Rate AGC initialization value. This value is the value loaded on an LOS event dependent on how the LOS_reseed_mode is configured. |

**EQU\_CTRLA (0x828, 0x928, 0xA28, 0xB28, 0xC28)**

## Equalizer Control A

| BIT         | 31 | 30                           | 29                           | 28 | 27 | 26 | 25 | 24 |
|-------------|----|------------------------------|------------------------------|----|----|----|----|----|
| Field       | –  | –                            | <a href="#">D1_init[5:0]</a> |    |    |    |    |    |
| Reset       | –  | –                            | 0x0                          |    |    |    |    |    |
| Access Type | –  | –                            | Write, Read                  |    |    |    |    |    |
| BIT         | 23 | 22                           | 21                           | 20 | 19 | 18 | 17 | 16 |
| Field       | –  | <a href="#">D2_init[6:0]</a> |                              |    |    |    |    |    |
| Reset       | –  | 0x0                          |                              |    |    |    |    |    |
| Access Type | –  | Write, Read                  |                              |    |    |    |    |    |
| BIT         | 15 | 14                           | 13                           | 12 | 11 | 10 | 9  | 8  |
| Field       | –  | <a href="#">D3_init[6:0]</a> |                              |    |    |    |    |    |
| Reset       | –  | 0x0                          |                              |    |    |    |    |    |
| Access Type | –  | Write, Read                  |                              |    |    |    |    |    |
| BIT         | 7  | 6                            | 5                            | 4  | 3  | 2  | 1  | 0  |
| Field       | –  | <a href="#">D4_init[6:0]</a> |                              |    |    |    |    |    |
| Reset       | –  | 0x0                          |                              |    |    |    |    |    |
| Access Type | –  | Write, Read                  |                              |    |    |    |    |    |

| BITFIELD | BITS  | DESCRIPTION                                                                                                                                                                    |
|----------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D1_init  | 29:24 | Full-Rate D1 initialization value. See D1_coeff for format (register 0x0C). This value is the value loaded on an LOS event dependent on how the LOS_reseed_mode is configured. |
| D2_init  | 22:16 | Full-Rate D2 initialization value. See D2_coeff for format (register 0x0C). This value is the value loaded on an LOS event dependent on how the LOS_reseed_mode is configured. |
| D3_init  | 14:8  | Full-Rate D3 initialization value. See D2_coeff for format (register 0x0C). This value is the value loaded on an LOS event dependent on how the LOS_reseed_mode is configured. |
| D4_init  | 6:0   | Full-Rate D4 initialization value. See D2_coeff for format (register 0x0C). This value is the value loaded on an LOS event dependent on how the LOS_reseed_mode is configured. |

**EQU\_CTRLB (0x82C, 0x92C, 0xA2C, 0xB2C, 0xC2C)**

## Equalizer Control B

| BIT         | 31 | 30    | 29 | 28                                                                       | 27                          | 26 | 25                        | 24 |
|-------------|----|-------|----|--------------------------------------------------------------------------|-----------------------------|----|---------------------------|----|
| Field       | –  | –     | –  | –                                                                        | <a href="#">capsel[1:0]</a> |    | <a href="#">Mode6Gphb</a> | –  |
| Reset       | –  | –     | –  | –                                                                        | 0x0                         |    | 0x0                       | –  |
| Access Type | –  | –     | –  | –                                                                        | Write, Read                 |    | Write, Read               | –  |
| BIT         | 23 | 22    | 21 | 20                                                                       | 19                          | 18 | 17                        | 16 |
| Field       | –  | –     | –  | –                                                                        | –                           | –  | –                         | –  |
| Reset       | –  | –     | –  | –                                                                        | –                           | –  | –                         | –  |
| Access Type | –  | –     | –  | –                                                                        | –                           | –  | –                         | –  |
| BIT         | 15 | 14    | 13 | 12                                                                       | 11                          | 10 | 9                         | 8  |
| Field       | –  | –     | –  | –                                                                        | –                           | –  | –                         | –  |
| Reset       | –  | –     | –  | –                                                                        | –                           | –  | –                         | –  |
| Access Type | –  | –     | –  | –                                                                        | –                           | –  | –                         | –  |
| BIT         | 7  | 6     | 5  | 4                                                                        | 3                           | 2  | 1                         | 0  |
| Field       | –  | –     | –  | –                                                                        | –                           | –  | –                         | –  |
| Reset       | –  | –     | –  | –                                                                        | –                           | –  | –                         | –  |
| Access Type | –  | –     | –  | –                                                                        | –                           | –  | –                         | –  |
| BITFIELD    |    | BITS  |    | DESCRIPTION                                                              |                             |    |                           |    |
| capsel      |    | 27:26 |    | Error slicer phase interpolator capacitor setting, value of 11 for 9.83G |                             |    |                           |    |
| Mode6Gphb   |    | 25    |    | PHY clock phase interpolator coarse tuning, value of 1 for 9.8GHz CMU    |                             |    |                           |    |

**EYE\_MON2 (0x83C, 0x93C, 0xA3C, 0xB3C, 0xC3C)**

Eye Monitor 2

| BIT         | 31                                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|-----------------------------------|----|----|----|----|----|----|----|
| Field       | <a href="#">D1ErrChPhPri[7:0]</a> |    |    |    |    |    |    |    |
| Reset       | 0xBB                              |    |    |    |    |    |    |    |
| Access Type | Write, Read                       |    |    |    |    |    |    |    |
| BIT         | 23                                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Field       | <a href="#">D1ErrChPhSec[7:0]</a> |    |    |    |    |    |    |    |
| Reset       | 0x40                              |    |    |    |    |    |    |    |
| Access Type | Write, Read                       |    |    |    |    |    |    |    |

| BIT         | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------|----|----|----|----|----|----|---|---|
| Field       | –  | –  | –  | –  | –  | –  | – | – |
| Reset       | –  | –  | –  | –  | –  | –  | – | – |
| Access Type | –  | –  | –  | –  | –  | –  | – | – |
| BIT         | 7  | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| Field       | –  | –  | –  | –  | –  | –  | – | – |
| Reset       | –  | –  | –  | –  | –  | –  | – | – |
| Access Type | –  | –  | –  | –  | –  | –  | – | – |

| BITFIELD     | BITS  | DESCRIPTION                                                                                                         |
|--------------|-------|---------------------------------------------------------------------------------------------------------------------|
| D1ErrChPhPri | 31:24 | Primary error (even) channel phase command                                                                          |
| D1ErrChPhSec | 23:16 | Secondary error (odd) channel phase command. This places the error channel one UI behind the primary sampling phase |

**TX\_CTRL1 (0x864, 0x964, 0xA64, 0xB64, 0xC64)**

Tx Control 1

| BIT         | 31 | 30 | 29 | 28 | 27 | 26                           | 25 | 24 |
|-------------|----|----|----|----|----|------------------------------|----|----|
| Field       | –  | –  | –  | –  | –  | –                            | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –                            | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –                            | –  | –  |
| BIT         | 23 | 22 | 21 | 20 | 19 | 18                           | 17 | 16 |
| Field       | –  | –  | –  | –  | –  | –                            | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –                            | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –                            | –  | –  |
| BIT         | 15 | 14 | 13 | 12 | 11 | 10                           | 9  | 8  |
| Field       | –  | –  | –  | –  | –  | <a href="#">cd_tune[2:0]</a> |    |    |
| Reset       | –  | –  | –  | –  | –  | 0x7                          |    |    |
| Access Type | –  | –  | –  | –  | –  | Write, Read                  |    |    |
| BIT         | 7  | 6  | 5  | 4  | 3  | 2                            | 1  | 0  |
| Field       | –  | –  | –  | –  | –  | –                            | –  | –  |
| Reset       | –  | –  | –  | –  | –  | –                            | –  | –  |
| Access Type | –  | –  | –  | –  | –  | –                            | –  | –  |

| BITFIELD | BITS | DESCRIPTION                                                        |
|----------|------|--------------------------------------------------------------------|
| cd_tune  | 10:8 | Clock driver frequency tuning, value of 000 for 9.83GHz CMU active |

**EQU\_CTRLD (0x880, 0x980, 0xA80, 0xB80, 0xC80)**

## Equalizer Control D

| BIT         | 31    | 30                               | 29                                      | 28 | 27 | 26 | 25 | 24 |
|-------------|-------|----------------------------------|-----------------------------------------|----|----|----|----|----|
| Field       | –     | –                                | <a href="#">DFE2_initD3[5:0]</a>        |    |    |    |    |    |
| Reset       | –     | –                                | 0x0                                     |    |    |    |    |    |
| Access Type | –     | –                                | Write, Read                             |    |    |    |    |    |
| BIT         | 23    | 22                               | 21                                      | 20 | 19 | 18 | 17 | 16 |
| Field       | –     | <a href="#">DFE2_initD2[6:0]</a> |                                         |    |    |    |    |    |
| Reset       | –     | 0x0                              |                                         |    |    |    |    |    |
| Access Type | –     | Write, Read                      |                                         |    |    |    |    |    |
| BIT         | 15    | 14                               | 13                                      | 12 | 11 | 10 | 9  | 8  |
| Field       | –     | <a href="#">DFE1_initD3[6:0]</a> |                                         |    |    |    |    |    |
| Reset       | –     | 0x0                              |                                         |    |    |    |    |    |
| Access Type | –     | Write, Read                      |                                         |    |    |    |    |    |
| BIT         | 7     | 6                                | 5                                       | 4  | 3  | 2  | 1  | 0  |
| Field       | –     | <a href="#">DFE1_initD2[6:0]</a> |                                         |    |    |    |    |    |
| Reset       | –     | 0x0                              |                                         |    |    |    |    |    |
| Access Type | –     | Write, Read                      |                                         |    |    |    |    |    |
| BITFIELD    | BITS  |                                  | DESCRIPTION                             |    |    |    |    |    |
| DFE2_initD3 | 29:24 |                                  | Quarter-rate DFE2 initialization value. |    |    |    |    |    |
| DFE2_initD2 | 22:16 |                                  | Half-rate DFE2 initialization value.    |    |    |    |    |    |
| DFE1_initD3 | 14:8  |                                  | Quarter-rate DFE1 initialization value. |    |    |    |    |    |
| DFE1_initD2 | 6:0   |                                  | Half-rate DFE1 initialization value.    |    |    |    |    |    |

**EQU\_CTRL E (0x884, 0x984, 0xA84, 0xB84, 0xC84)**

## Equalizer Control E

| BIT         | 31 | 30                               | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|----|----------------------------------|----|----|----|----|----|----|
| Field       | –  | <a href="#">DFE4Init_D3[6:0]</a> |    |    |    |    |    |    |
| Reset       | –  | 0x0                              |    |    |    |    |    |    |
| Access Type | –  | Write, Read                      |    |    |    |    |    |    |

| BIT         | 23    | 22                               | 21                                          | 20 | 19 | 18 | 17 | 16 |
|-------------|-------|----------------------------------|---------------------------------------------|----|----|----|----|----|
| Field       | –     | <a href="#">DFE4Init_D2[6:0]</a> |                                             |    |    |    |    |    |
| Reset       | –     | 0x0                              |                                             |    |    |    |    |    |
| Access Type | –     | Write, Read                      |                                             |    |    |    |    |    |
| BIT         | 15    | 14                               | 13                                          | 12 | 11 | 10 | 9  | 8  |
| Field       | –     | <a href="#">DFE3Init_D3[6:0]</a> |                                             |    |    |    |    |    |
| Reset       | –     | 0x0                              |                                             |    |    |    |    |    |
| Access Type | –     | Write, Read                      |                                             |    |    |    |    |    |
| BIT         | 7     | 6                                | 5                                           | 4  | 3  | 2  | 1  | 0  |
| Field       | –     | <a href="#">DFE3Init_D2[6:0]</a> |                                             |    |    |    |    |    |
| Reset       | –     | 0x0                              |                                             |    |    |    |    |    |
| Access Type | –     | Write, Read                      |                                             |    |    |    |    |    |
| BITFIELD    | BITS  |                                  | DESCRIPTION                                 |    |    |    |    |    |
| DFE4Init_D3 | 30:24 |                                  | Quarter-rate DFE4 coefficient initial value |    |    |    |    |    |
| DFE4Init_D2 | 22:16 |                                  | Half-rate DFE4 coefficient initial value    |    |    |    |    |    |
| DFE3Init_D3 | 14:8  |                                  | Quarter-rate DFE3 coefficient initial value |    |    |    |    |    |
| DFE3Init_D2 | 6:0   |                                  | Half-rate DFE3 coefficient initial value    |    |    |    |    |    |

**[EQU\\_CTRLG \(0x88C, 0x98C, 0xA8C, 0xB8C, 0xC8C\)](#)**

Equalizer Control G

| BIT         | 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------|---------------------------------|----|----|----|----|----|----|----|
| Field       | –                               | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –                               | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –                               | –  | –  | –  | –  | –  | –  | –  |
| BIT         | 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Field       | –                               | –  | –  | –  | –  | –  | –  | –  |
| Reset       | –                               | –  | –  | –  | –  | –  | –  | –  |
| Access Type | –                               | –  | –  | –  | –  | –  | –  | –  |
| BIT         | 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| Field       | <a href="#">AGCInit_D3[7:0]</a> |    |    |    |    |    |    |    |
| Reset       | 0x83                            |    |    |    |    |    |    |    |
| Access Type | Write, Read                     |    |    |    |    |    |    |    |

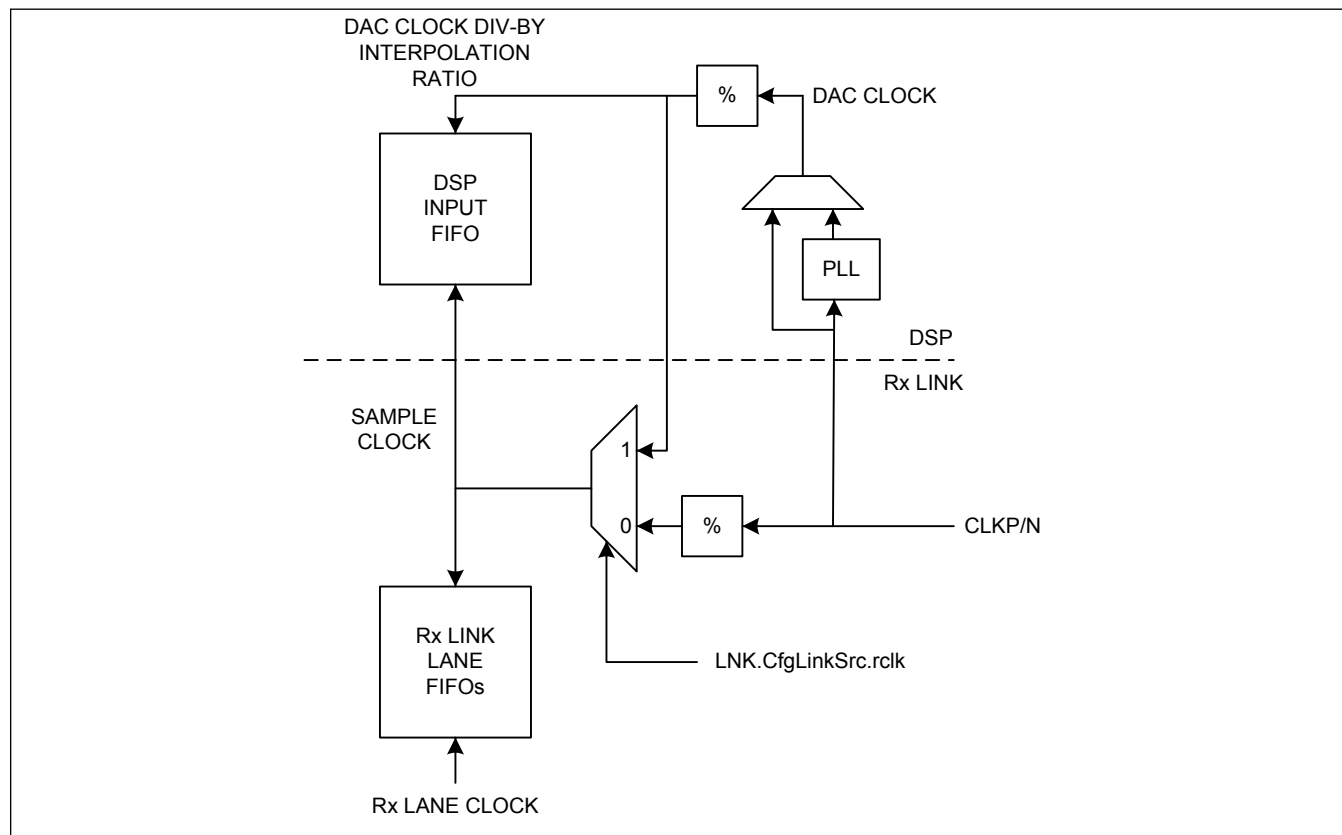
MAX5855

16-Bit, 4.9Gsps Wideband Interpolating  
and Modulating RF DAC with JESD204B Interface

| BIT         | 7                               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------------------|---|---|---|---|---|---|---|
| Field       | <a href="#">AGCInit_D2[7:0]</a> |   |   |   |   |   |   |   |
| Reset       | 0x82                            |   |   |   |   |   |   |   |
| Access Type | Write, Read                     |   |   |   |   |   |   |   |

| BITFIELD   | BITS | DESCRIPTION                           |
|------------|------|---------------------------------------|
| AGCInit_D3 | 15:8 | Quarter-rate AGC initialization value |
| AGCInit_D2 | 7:0  | Half-rate AGC initialization value    |

## JESD204B LINK and DSP Clocking



1. Program the DAC PLL registers (DSP.CfgPLL)
2. Program the Rx LINK device clock divide factor (RLinkRegs.CfgRLinkSet.Ddiv)
3. Set the interpolation mode and then reset the input FIFO (DSP.CfgDSP.R[3:0], DSP.CfgDSP.RstFIFO)
4. Remove the DSP input FIFO reset (DSP.CfgDSP.RstFIFO)

## Typical Configuration

The MAX5855 includes setting up the clocking as described in the following sections and setting all other configurations before or after that. Configuration registers other than the clocking includes the DSP, JESD204B CMU, SerDes and LNK registers.

### Enabling the DAC Output from Power-up

The following is the overall flowchart from power-up to DAC output enable. Some of the intermediate steps are mode-specific and are described in [Figure 32](#).



Figure 32. DAC Power-Up Sequence

**Power Up:** Ramp up power for all supplies, this does not require any particular order.

**Chip Reset:** Assert chip reset (RESETB) for 1 $\mu$ s. After reset is release, either monitor the INTB pin for a high-to-low transition or poll the DSP.STATUS.TRDY bit for a set (logic-high) state. These indicate that trimming is complete and the device is ready for configuration.

**Clock Setup:** Clock setup includes configuring the clock sources for internal blocks such as the DAC, the DSP, and the JESD204B functions. The JESD configuration must also include the subclass mode since that configuration determines how the FIFOs are initialized. The Clock Setup sequence must include the following:

1. DAC PLL usage
2. Device Clock availability for JESD204B function
3. DSP interpolation rate

Depending on the source used for generating the sample clock, [Figure 33](#) shows the JESD204B setups sequences required for Subclass-0 operation.

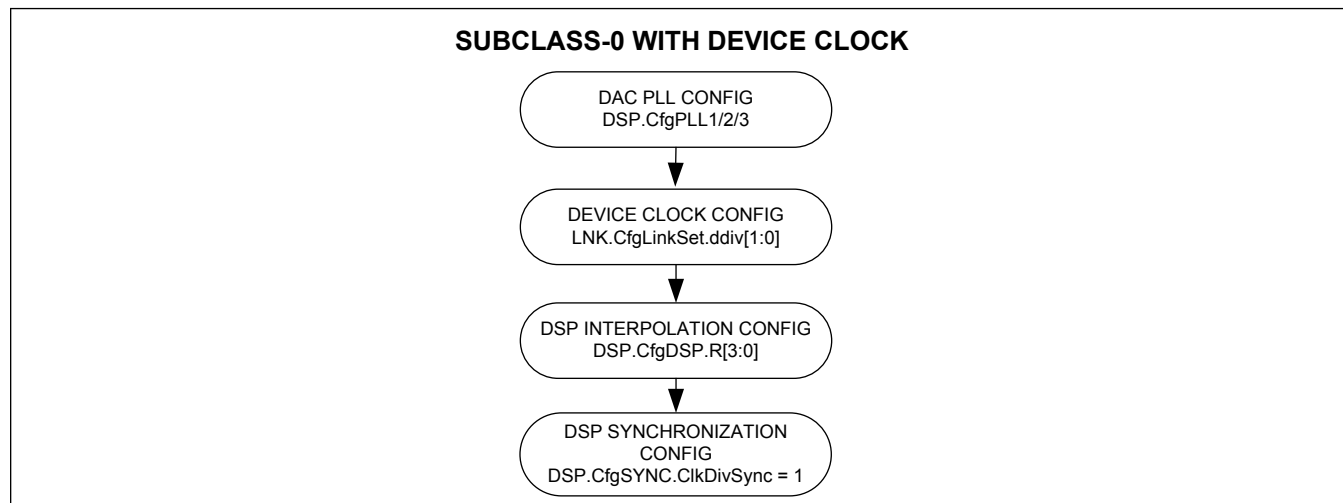


Figure 33. DAC Configuration Sequence

**FIFO Resets:** After the clock modes are configured and after a sufficient wait time has passed to allow the DAC PLL to lock, the DSP clock divider needs to be reset. Next the Rx LINK and DSP FIFOs need to be centered through the configuration process of Subclass-0 mode. Depending on the sample clock source, the setups shown in [Figure 34](#) are used for Subclass-0.

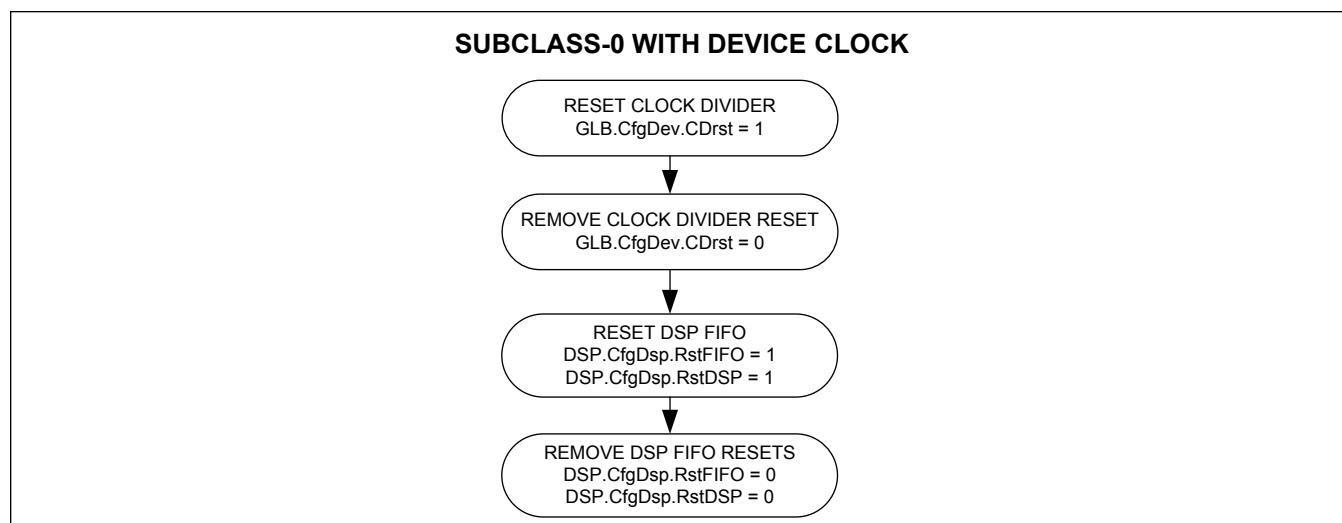


Figure 34. DAC Reset Sequence

**Mode Setup:** Setup device modes other than DAC PLL, clocking, synchronization and resets.

**Interrupt/Mute Enables:** Enable internal DAC mute and interrupt-enable bits in the JESD204B RxLink and DSP registers.

**Start Data:** Start the JESD204B LINK carrying the digital data streams.

**Clear and Check Statuses:** Clear all the latched status bits which were previously enabled for internal DAC mute and interrupt.

**Unmute DAC:** Clear the DAC mute register bit (DSP.CfgChipOM.Mute) to enable the DAC output.

## Applications Guidelines

### Power Sequence

The MAX5855 does not require a specific power sequence. However, it is recommended that all the supplies are powered up simultaneously.

### Power Supply AVCLK

Power for AVCLK is the most sensitive supply due to the sensitivity of the internal clock circuitry. To achieve the specified DAC performance, AVCLK should not be shared with other 1.0V supplies. In particular, the AVCLK supply must not be shared with digital  $V_{DD}$  1.0V supply.

### Power-On RESETB and SPI Configuration

During the initial power-on, the RESETB pin should be held low. The RESETB pin has an internal 32k $\Omega$  pulldown resistor and it should be pulled high only after all power supplies have stabilized at their nominal levels.

An alternative method for power-on-reset is to cycle the RESETB pin (transition high-to-low-to-high) after the power supplies are fully stabilized at their nominal levels.

There is a delay time required after the RESETB is set high, before SPI configuration can be initiated. The delay time allows the device to finish its initialization process. The delay is directly related to the CLKP/CLKN frequency, requiring about 370k clock cycles or about 301 $\mu$ s when using a device clock frequency of 1.2288GHz.

A series of specific SPI writes must be performed each time the device is powered-up. These writes perform initialization of specific internal blocks and ensure consistent performance after every power cycle. These writes are generated by the configuration script described in the **Configuration Script Tool** section and should include the following command sequence:

```

Write 0x0206, 0x18
Write 0x0211, 0x8C
Write 0x0213, 0x40
Wait 100us
Write 0x0213, 0x00
Write 0x0206, 0x0
Write 0x0211, 0x0
Wait 100us

```

### Delay Time $t_{D-DivRst}$ Estimation

Adding proper delay time before resetting the internal divider is important to ensure the divider starts with a stable clock. This allows the DAC PLL (or external CLKP/CLKN) to fully lock and settle. The minimum delay time is estimated as:

$$t_{D-DivRst} \approx \frac{220}{f_{PFD}} \quad (9)$$

where,

$f_{PFD}$  is the input frequency of the DAC PLL Phase Frequency Detector, when in PLL-on mode.

For example, when the CLKP/CLKN frequency is at 983.04MHz and the reference divider RVAL is set to 1/4,  $f_{PFD} = 983.04/4 = 245.76\text{MHz}$ . The  $t_{D-DivRst}$  is estimated to be 0.9 $\mu\text{s}$ .

For the Configuration Script Tool output, a default delay of 20ms is used.

### Pin DACREF Consideration

The 960 $\Omega$  resistor from FSADJ (B2) should connect directly to DACREF (B1). This should be placed on the same side of the printed circuit board (PCB) as the MAX5855 package itself, and as close as possible to those pins. The 1 $\mu\text{F}$  capacitors which are connected to REFIO (A1) and CSBP (A2) should be connected to DACREF, **not GND**. These capacitors should also be placed on the same layer of the PCB as the DAC, avoiding vias on all these traces if possible. DACREF is internally connected to AGND. **DO NOT CONNECT DACREF TO EXTERNAL GROUND.**

### DAC PLL Consideration

The PLL\_COMP (A12) and VCOBYP (B11) connections form the loop filter for the PLL (see Figure 29). Place these external components on the PCB layer opposite the CLK and OUTPUT circuits (bottom versus top of the board) to prevent crosstalk coupling. The recommended filter between PLL\_COMP (A12) and VCOBYP (B11) is a 2.7k $\Omega$  resistor in series with a 430pF capacitor. The C1 capacitor reduces noise from GND (A11) to VCOBYP (B11). Place C1 directly under the balls/vias of the package to make the physical loop (trace length) as small as possible. The exact values of C1 and C2 will vary depending on PCB layout and they may not be required for optimal performance.

### Pin SDO Consideration

In 4-wire SPI interface mode, SDO is used as a serial data output. When connecting multiple SDOs together using CSB to access the MAX5855, it is recommended to have a 10k $\Omega$  pullup resistor on the input of FPGA or ASIC to prevent floating. When SDO is not selected, it remains high-impedance.

### Clock Requirement

The MAX5855 is operated with the internal DAC PLL. Care should always be taken to design the system using a low phase noise, low jitter clock source.

With the DAC PLL on, the DAC PLL bandwidth is set to around 1MHz (based on the loop filter components). This means that any phase noise or jitter of the reference clock at frequency offsets higher than 1MHz should be filtered out by the PLL loop; therefore, any impact on the DAC performance will be minimized.

However, within the sub-1MHz band, the reference clock phase noise will dominate the PLL performance. In either case, the reference clock phase noise will be translated to the DAC output phase noise according to the formula:

$$PN_{OUT} = PN_{REF} + 20 \times \log\left(\frac{f_C}{f_{REF}}\right) \quad (12)$$

where,

$PN_{OUT}$  [dBc/Hz] is the DAC output phase noise,  $PN_{REF}$  [dBc/Hz] is the PLL reference clock phase noise,  $f_C$  is the DAC output frequency, and  $f_{REF}$  is the PLL reference clock frequency.

In addition to the reference clock phase noise and jitter, the maximum allowable spur level in the clock spectrum should be limited based on target performance standards such as DOCSIS 3.1.

Additional details on the DAC clock requirements and derivation of the equations noted above are available upon request.

### NCO Frequency

The NCO frequency is subject to two types of errors resulting from the NCO and DAC clock frequencies. The first error stems from the NCO itself and is a result of using finite word lengths for calculating the various frequency control factors, as established in the **Quadrature Modulator and NCO** section.

The second error to the NCO frequency is related to DAC input sampling clock. The NCO synthesizes a frequency based on an exact fraction of the DAC core clock frequency. That fractional value can be calculated using the equation found in the **Quadrature Modulator and NCO** section. Any percentage error in the DAC input clock will result in the same percentage error at the NCO output. For example, if the DAC input clock has a tolerance of 10ppm, the NCO output frequency will also have a tolerance of 10ppm.

The DAC PLL does not introduce any frequency error once it is locked. The PLL output frequency is exactly equal to the input reference frequency multiplied by the selected PLL multiplication factor.

### Latency

There are two types of latencies in the MAX5855: DAC conversion latency and JESD204B data latency. The DAC latency is given in the [Electrical Characteristics](#) table with units of DAC Clock Cycles. The JESD204B Rx LINK layer includes the transmit link latency, the channel latency, and the lane processing latency.

The RLinkRegs.CfgRLinkMFrame.ILADly register will need to be adjusted by the user in the final application environment. This frame clock count for the FIFO read start is dependent on a number of external factors such as FPGA/ASIC transmit delays, overall trace lengths, lane mismatch, and board parasitics. The RxLink latency will have an uncertainty of up to 20 bit clock periods after a reset state. The lane processing delay portion of the JESD204B Rx LINK is 200 SerDes bit clocks.

### PRBS Sequence

PRBS7 and PRBS23 are supposed to be inverted according to Table 3 in [http://www.xilinx.com/support/documentation/application\\_notes/xapp884\\_PRBS\\_GeneratorChecker.pdf](http://www.xilinx.com/support/documentation/application_notes/xapp884_PRBS_GeneratorChecker.pdf)

The MAX5855 Rx PHY has an option to invert the data by setting PHY.MISC\_REG2.Rx\_parallel\_data\_invert (bit 4). Contact the factory for additional information on using the PRBS pattern checking capabilities of the MAX5855 JESD interface.

### DAC Output Impedance Model and Matching Network

A DAC output impedance model is available in an s-parameter file which can be used for the design of an output matching network. When designing the PCB, the following best engineering practices may help:

- OUP and OUTN trace routes to the matching network should be as short as possible. Similarly, the trace routes from the matching network to any filter should also be as short as possible.
- The OUP and OUTN traces should be routed symmetrically to reduce any mismatch.

- The environment around OUTP and OUTN pins should be symmetrical. This means that the parasitic environment "seen" by one signal should match environment "seen" by the other signal.
- If OUTP and OUTN cannot use short trace routes, those traces should have matched lengths with mirror symmetry and they should use a differential 50Ω routed impedance.
- When crossing other signals/supplies routed on other layers, OUTP and OUTN should cross at a 90-degree angle to these signals/supplies.
- OUTP and OUTN should be routed on an outer board layer and should be kept away from supply decoupling components and traces.
- The AVCLK network **should not** be placed nor routed in proximity to OUTP and OUTN network.

### Thermal Considerations

The use of component-layer, ground plane "pour" is highly recommended for the PCB design. For improved thermal performance, the system design should incorporate direct-contact heatsinking to the device when possible. The thermal resistance values provided in the Absolute Maximum Ratings section are based on JEDEC standard 51-12. The application of thermal modeling is highly recommended at the time of system design and a Delphi model is available for system thermal simulations.

### Ordering Information

| PART NUMBER  | TEMP RANGE     | PIN-PACKAGE |
|--------------|----------------|-------------|
| MAX5855EXE+  | -40°C to +85°C | 144-FCCSP   |
| MAX5855EXE+T | -40°C to +85°C | 144-FCCSP   |

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

MAX5855

16-Bit, 4.9Gbps Wideband Interpolating  
and Modulating RF DAC with JESD204B Interface

## Revision History

| REVISION<br>NUMBER | REVISION<br>DATE | DESCRIPTION                       | PAGES<br>CHANGED |
|--------------------|------------------|-----------------------------------|------------------|
| 0                  | 9/18             | Initial release                   | —                |
| 1                  | 4/19             | Updated Pin Configuration diagram | 17               |

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