MAX5098A

Dual 2.2MHz Buck or Boost Converter with 80V Load-Dump Protection

General Description

The MAX5098A is a dual-output, high-switching-frequency DC-DC converter with integrated n-channel switches that can be used either in high-side or low-side configuration. Each output can be configured either as a buck converter or a boost converter. In the buck configuration, this device delivers up to 2A from converter 1 and 1A from converter 2. The MAX5098A also integrates a load-dump protection circuitry that is capable of handling load-dump transients up to 80V for industrial applications. The load-dump protection circuit utilizes an internal charge pump to drive the gate of an external n-channel MOSFET. When an overvoltage or load-dump condition occurs, the series protection MOSFET absorbs the high-voltage transient to prevent damage to lower-voltage components.

The DC-DC converters operate over a wide operating voltage range from 4.5V to 19V. The MAX5098A operates 180° out-of-phase with an adjustable switching frequency to minimize external components while allowing the ability to make trade-offs between the size, efficiency, and cost.

This device utilizes voltage-mode control for stable operation and external compensation; thus, the loop gain is tailored to optimize component selection and transient response. This device can be synchronized to an external clock fed at the SYNC input. Also, a clock output (CKO) allows a master-slave connection of two devices with a four-phase synchronized switching sequence. Additional features include internal digital soft-start, individual enable for each DC-DC regulator (EN1 and EN2), open-drain power-good outputs (PGOOD1 and PGOOD2), and a shutdown input (ON/OFF).

Other features of the MAX5098A include overvoltage protection, short-circuit (hiccup current limit), and thermal protection. The MAX5098A is available in a thermally enhanced, exposed pad, 5mm x 5mm, 32-pin TQFN package and is fully specified over the -40°C to +125°C temperature range.

Applications

- Industrial

Pin Configuration appears at end of data sheet.

Features

- Wide 4.5V to 5.5V or 5.2V to 19V Input Voltage Range (with Up to 80V Load-Dump Protection)
- Dual-Output DC-DC Converter with Integrated Power MOSFETs
- Each Output Configurable in Buck or Boost Mode
- Adjustable Outputs from 0.8V to 0.85V_{IN} Buck Configuration) and from V_{IN} to 28V (Boost Configuration)
- I_{OUT1} and I_{OUT2} of 2A and 1A (Respectively) in Buck Configuration
- Switching Frequency Programmable from 200kHz to 2.2MHz
- Synchronization Input (SYNC)
- Clock Output (CKO) for Four-Phase Master-Slave Operation
- Individual Converter Enable Input and Power-Good Output
- Low-I_Q (7µA) Standby Current (ON/OFF)
- Internal Digital Soft-Start and Soft-Stop
- Short-Circuit Protection on Outputs and Maximum Duty-Cycle Limit
- Overvoltage Protection on Outputs with Auto Restart
- Thermal Shutdown
- Thermally Enhanced 32-Pin TQFN Package Dissipates Up to 2.7W at +70°C

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5098AATJ+	-40°C to +125°C	32 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

19-4111; Rev 1; 10/14

maxim integrated™

Absolute Maximum Ratings

V+ to SGND .....-0.3V to +25V
V+ to IN_HIGH .....-19V to +6V
IN_HIGH to SGND .....-0.3V to +19V
IN_HIGH Maximum Input Current 60mA
BYPASS to SGND.....-0.3V to +2.5V
GATE to V+ .....-0.3V to +12V
GATE to SGND .....-0.3V to +36V
SGND to PGND_.....-0.3V to +0.3V
V_L to SGND.....-0.3V to the Lower of +6V or (V+ + 0.3V)
VDRV to SGND.....-0.3V to +6V
BST1/VDD1, BST2/VDD2, DRAIN_, PGOOD_ to SGND.....-0.3V to +30V
ON/OFF to SGND .....-0.3V to (IN_HIGH + 0.3V)
BST1/VDD1 to SOURCE1, BST2/VDD2 to SOURCE2.....-0.3V to +6V
SOURCE_ to SGND.....-0.6V to +25V
SOURCE_ to PGND_..... -1V for 50ns
EN_ to SGND.....-0.3V to +6V
OSC, FSEL_1, COMP_, SYNC, FB_ to SGND.....-0.3V to (V_L + 0.3V)
CKO to SGND .....-0.3V to (VDRV + 0.3V)
SOURCE1, DRAIN1 Peak Current .....5A for 1ms
SOURCE2, DRAIN2 Peak Current .....3A for 1ms
V_L, BYPASS to SGND Short Circuit ..... Continuous, Internally Limited
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN-EP (derate 34.5mW/°C above +70°C) ...2759mW
Operating Temperature Range..... -40°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA}) .....29.0°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....1.7°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specifications. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(VDRV = V_L, V+ = V_L = IN_HIGH = 5.2V or V+ = IN_HIGH = 5.2V to 19V, EN_ = V_L, SYNC = GND, I_{VL} = 0mA, PGND_ = SGND, C_{BYPASS} = 0.22µF (low ESR), C_{VL} = 4.7µF (ceramic), C_{V+} = 1µF (low ESR), C_{IN_HIGH} = 1µF (ceramic), R_{IN_HIGH} = 3.9kΩ, R_{OSC} = 10kΩ, T_J = -40°C to +125°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SYSTEM SPECIFICATIONS							
Input Voltage Range	V+	V+ = IN_HIGH		5.2		19	V
		VL = V+ = IN_HIGH (Note 3)		4.5		5.5	
V+ Operating Supply Current	IQ	VL unloaded, no switching			4.2		mA
V+ Standby Supply Current	IV+STBY	VEN_ = 0V, PGOOD_ unconnected, V+ = VIN_HIGH = 14V			0.75	1.1	mA
Efficiency	η	(VOUT1 = 5V at 1.5A, VOUT2 = 3.3V at 0.75A, fSW = 1.85MHz	V+ = VL = 5.2V		78		%
			V+ = 12V		76		
			V+ = 16V		70		
OVERVOLTAGE PROTECTOR							
IN_HIGH Clamp Voltage	IN_HIGH	ISINK = 10mA		19	20	21	V
IN_HIGH Clamp Load Regulation		1mA < ISINK < 50mA			160		mV
IN_HIGH Supply Current	IIN_HIGH	VEN_ = VPGOOD_ = VGATE = 0V, VIN_HIGH = VON/OFF = 14V			270	600	µA

Electrical Characteristics (continued)

(VDRV = V_L, V+ = V_L = IN_HIGH = 5.2V or V+ = IN_HIGH = 5.2V to 19V, EN_ = V_L, SYNC = GND, I_{VL} = 0mA, PGND_ = SGND, C_{BYPASS} = 0.22µF (low ESR), C_{VL} = 4.7µF (ceramic), C_{V+} = 1µF (low ESR), C_{IN_HIGH} = 1µF (ceramic), R_{IN_HIGH} = 3.9kΩ, R_{OSC} = 10kΩ, T_J = -40°C to +125°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN_HIGH Standby Supply Current	$I_{IN\_HIGHSTBY}$	$V_{ON/OFF}$ = 0V, PGOOD_ = V+ = unconnected, V_{IN_HIGH} = 14V, T_A = -40°C to +85°C		7	9	µA
V+ to IN_HIGH Overvoltage Clamp	V_{OV}	V_{OV} = V+ - V_{IN_HIGH}, I_{GATE} = 0mA (sinking)	1.2	1.85	2.5	V
IN_HIGH Startup Voltage	IN_HIGH UVLO	Rising, ON/OFF = IN_HIGH, GATE rising		3.6	4.1	V
		Falling, ON/OFF = IN_HIGH, GATE falling		3.45		
GATE Charge Current	I_{GATE_CH}	V_{IN_HIGH} = $V_{ON/OFF}$ = 14V, V_{GATE} = V+ = 0V	20	45	80	µA
GATE Output Voltage	V_{GATE} – V_{IN_HIGH}	V+ = V_{IN_HIGH} = $V_{ON/OFF}$ = 4.5V, I_{GATE} = 1µA, sourcing	4.0	5.3	7.5	V
		V+ = V_{IN_HIGH} = $V_{ON/OFF}$ = 14V, I_{GATE} = 1µA, sourcing		9		
GATE Turn-Off Pulldown Current	I_{GATE_PD}	V_{IN_HIGH} = 14V, $V_{ON/OFF}$ = 0V, V+ = 0V, V_{GATE} = 5V, sinking		3.6		mA
STARTUP/V_L REGULATOR						
V_L Undervoltage Lockout Trip Level	UVLO	V_L falling	3.9	4.1	4.3	V
V_L Undervoltage Lockout Hysteresis				180		mV
V_L Output Voltage	V_L	$I_{SOURCE\_}$ = 0 to 40mA, 5.5V ≤ V+ ≤ 19V	5.0	5.2	5.5	V
V_L LDO Short-Circuit Current	I_{VL_SHORT}	V+ = V_{IN_HIGH} = 5.2V		130		mA
V_L LDO Dropout Voltage	V_{LDO}	$I_{SOURCE\_}$ = 40mA, V+ = V_{IN_HIGH} = 4.5V		300	550	mV
BYPASS OUTPUT						
BYPASS Voltage	V_{BYPASS}	I_{BYPASS} = 0µA	1.98	2.00	2.02	V
BYPASS Load Regulation	ΔVBYPASS	0 < I_{BYPASS} < 100µA (sourcing)		2	5	mV
SOFT-START/SOFT-STOP						
Digital Ramp Period Soft-Start/Soft-Stop		Internal 6-bit DAC		2048		f_{SW} Clock Cycles
Soft-Start/Soft-Stop				64		Steps
VOLTAGE-ERROR AMPLIFIER						
FB_ Input Bias Current	$I_{FB\_}$				250	nA
FB_ Input Voltage Set Point	$V_{FB\_}$	-40°C ≤ T_A ≤ +85°C	0.783	0.8	0.809	V
		-40°C ≤ T_A ≤ +125°C	0.785		0.814	
FB_ to COMP_ Transconductance	gM		1.4	2.4	3.4	mS

Electrical Characteristics (continued)

(VDRV = V_L, V+ = V_L = IN_HIGH = 5.2V or V+ = IN_HIGH = 5.2V to 19V, EN_ = V_L, SYNC = GND, I_{VL} = 0mA, PGND_ = SGND, C_{BYPASS} = 0.22µF (low ESR), C_{VL} = 4.7µF (ceramic), C_{V+} = 1µF (low ESR), C_{IN_HIGH} = 1µF (ceramic), R_{IN_HIGH} = 3.9kΩ, R_{OSC} = 10kΩ, T_J = -40°C to +125°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL MOSFETs						
On-Resistance High-Side MOSFET Converter 1	R_{ON1}	I_{SWITCH} = 100mA, BST1/VDD1 to $V_{SOURCE1}$ = 5.2V		195		mΩ
		I_{SWITCH} = 100mA, BST1/VDD1 to $V_{SOURCE1}$ = 4.5V		208	355	
On-Resistance High-Side MOSFET Converter 2	R_{ON2}	I_{SWITCH} = 100mA, BST2/VDD2 to $V_{SOURCE2}$ = 5.2V		280		mΩ
		I_{SWITCH} = 100mA, BST2/VDD2 to $V_{SOURCE2}$ = 4.5V		300	520	
Minimum Converter 1 Output Current	I_{OUT1}	V_{OUT1} = 5V, V+ = 12V (Note 4)		2		A
Minimum Converter 2 Output Current	I_{OUT2}	V_{OUT2} = 3.3V, V+ = 12V (Note 4)		1		A
Converter 1/Converter 2 MOSFET DRAIN_ Leakage Current	I_{LK12}	V_{EN1} = V_{EN2} = 0V, $V_{DRAIN\_}$ = 19V, $V_{SOURCE\_}$ = 0V			20	µA
Internal Weak Low-Side Switch On-Resistance	$R_{ONLSSW\_}$	I_{LSSW} = 30mA		22		Ω
INTERNAL SWITCH CURRENT LIMIT						
Internal Switch Current-Limit Converter 1	I_{CL1}	V+ = V_{IN_HIGH} = 5.2V, V_L = VDRV = $V_{BST\_/VDD\_}$ = 5.2V	2.8	3.45	4.3	A
Internal Switch Current-Limit Converter 2	I_{CL2}	V+ = V_{IN_HIGH} = 5.2V, V_L = VDRV = $V_{BST\_/VDD\_}$ = 5.2V	1.75	2.1	2.6	A
SWITCHING FREQUENCY						
PWM Maximum Duty Cycle	D_{MAX}	SYNC = SGND, f_{SW} = 1.25MHz	82	90	95	%
Switching Frequency Range	f_{SW}		200		2200	kHz
Switching Frequency	f_{SW}	R_{OSC} = 6.81kΩ, each converter (FSEL_1 = V_L)	1.7	1.9	2.1	MHz
Switching Frequency Accuracy		5.6kΩ < R_{OSC} < 10kΩ, 1%		5		%
		10kΩ < R_{OSC} < 62.5kΩ, 1%		7		
SYNC Frequency Range	f_{SYNC}	SYNC input frequency is twice the individual converter frequency, FSEL_1 = V_L (see the *Setting the Switching Frequency* section)	400		4400	kHz
SYNC High Threshold	V_{SYNCH}		2			V
SYNC Low Threshold	V_{SYNCL}				0.8	V
SYNC Input Leakage	I_{SYNC_LEAK}				2	µA
SYNC Input Minimum Pulse Width	t_{SYNCIN}			100		ns

Electrical Characteristics (continued)

(VDRV = V_L, V+ = V_L = IN_HIGH = 5.2V or V+ = IN_HIGH = 5.2V to 19V, EN_ = V_L, SYNC = GND, I_{VL} = 0mA, PGND_ = SGND, C_{BYPASS} = 0.22µF (low ESR), C_{VL} = 4.7µF (ceramic), C_{V+} = 1µF (low ESR), C_{IN_HIGH} = 1µF (ceramic), R_{IN_HIGH} = 3.9kΩ, R_{OSC} = 10kΩ, T_J = -40°C to +125°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Output Phase Delay	CKO_{PHASE}	R_{OSC} = 62.5kΩ, with respect to converter 2/SOURCE2 waveform		40		Degrees
SYNC to Source 1 Phase Delay	$SYNC_{PHASE}$	R_{OSC} = 62.5kΩ		90		Degrees
Clock Output High Level	V_{CKOH}	V_L = 5.2V, sourcing 5mA	3.6			V
Clock Output Low Level	V_{CKOL}	V_L = 5.2V, sinking 5mA			0.6	V
FSEL_1						
FSEL_1 Input High Threshold	V_{IH}		2			V
FSEL_1 Input Low Threshold	V_{IL}				0.8	V
FSEL_1 Input Leakage	$I_{FSEL\_1\_LEAK}$				2	µA
ON/OFF						
ON/OFF Input High Threshold	V_{IH}		2			V
ON/OFF Input Low Threshold	V_{IL}				0.8	V
ON/OFF Input Leakage Current	I_{ON/OFF_LEAK}	$V_{ON/OFF}$ = 5V		0.26	2.00	µA
EN_ INPUTS						
EN_ Input High Threshold	V_{IH}	EN_ rising	1.9	2.0	2.1	V
EN_ Input Hysteresis	V_{EN_HYS}			0.5		V
EN_ Input Leakage Current	I_{EN_LEAK}		-1		+1	µA
POWER-GOOD OUTPUT (PGOOD1, PGOOD2)						
PGOOD_ Threshold	$V_{TPGOOD\_}$	Falling	90	92.5	95	% $V_{FB\_}$
PGOOD_ Output Voltage	$V_{PGOOD\_}$	I_{SINK} = 3mA			0.4	V
PGOOD_ Output Leakage Current	$I_{LKPGOOD\_}$	V+ = V_L = V_{IN_HIGH} = $V_{EN\_}$ = 5.2V, $V_{PGOOD\_}$ = 23V, $V_{FB\_}$ = 1V			2	µA
OUTPUT OVERVOLTAGE PROTECTION						
FB_ OVP Threshold Rising	V_{OVP_R}		107	114	121	% $V_{FB\_}$
FB_ OVP Threshold Falling	V_{OVP_F}			12.5		V
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}	Rising		+165		°C
Thermal Hysteresis	T_{HYST}			20		°C

Note 2: 100% tested at T_A = +25°C and T_A = +125°C. Specifications at T_A = -40°C are guaranteed by design and not production tested.

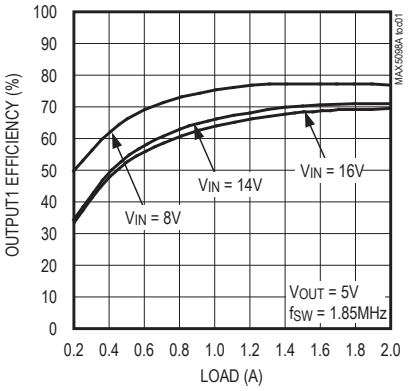
Note 3: Operating supply range (V+) is guaranteed by V_L line regulation test. Connect V+ to IN_HIGH and V_L for 5V operation.

Note 4: Output current is limited by the power dissipation of the package; see the *Power Dissipation* section in the *Applications Information* section.

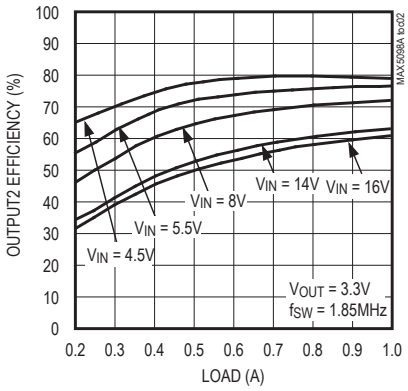
Typical Operating Characteristics

(See the *Typical Application Circuit*, unless otherwise noted. V+ = V_{IN_HIGH} = 14V, unless otherwise noted. V+ = V_{IN_HIGH} means that N1 is shorted externally.)

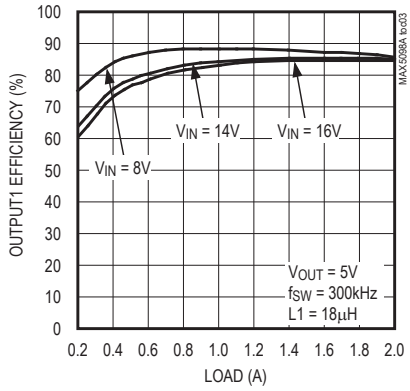
OUTPUT1 EFFICIENCY vs. LOAD CURRENT



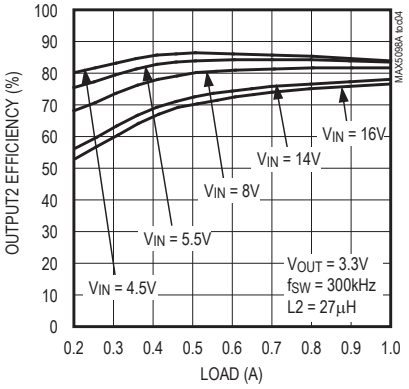
OUTPUT2 EFFICIENCY vs. LOAD CURRENT



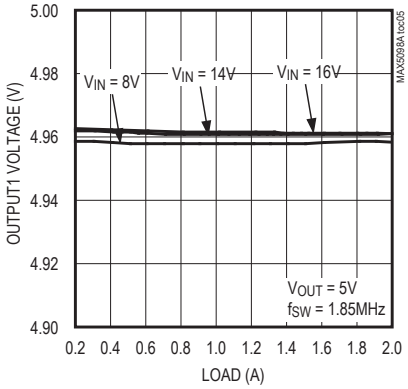
OUTPUT1 EFFICIENCY vs. LOAD CURRENT



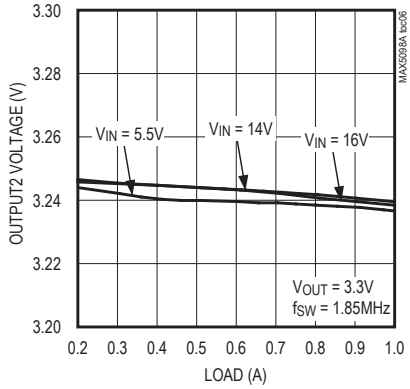
OUTPUT2 EFFICIENCY vs. LOAD CURRENT



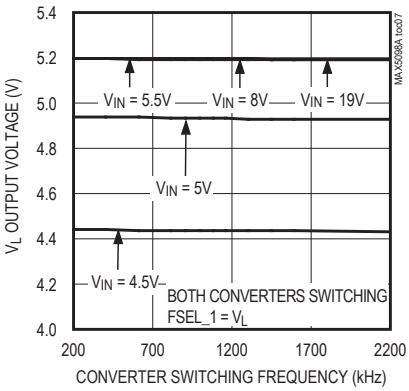
OUTPUT1 VOLTAGE vs. LOAD CURRENT



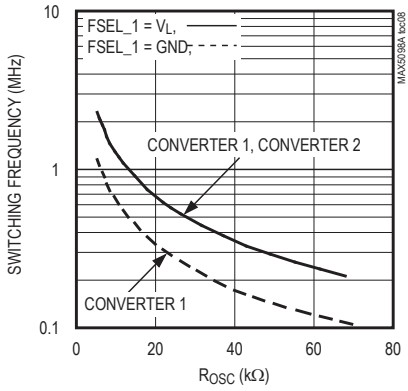
OUTPUT2 VOLTAGE vs. LOAD CURRENT



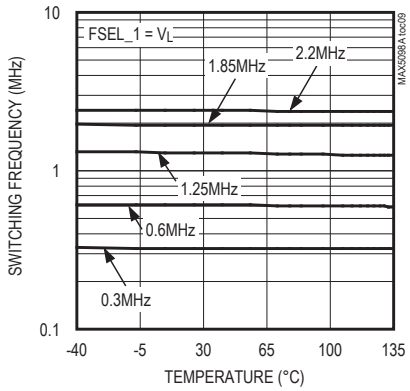
V_L OUTPUT VOLTAGE vs. CONVERTER SWITCHING FREQUENCY



EACH CONVERTER SWITCHING FREQUENCY vs. R_{OSC}



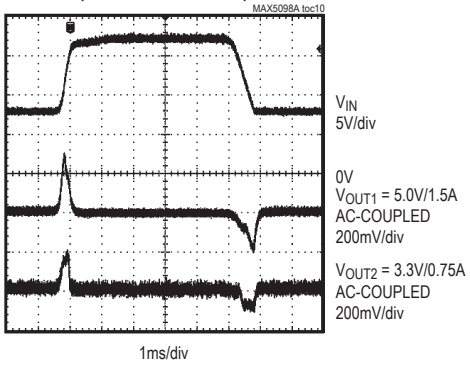
EACH CONVERTER SWITCHING FREQUENCY vs. TEMPERATURE



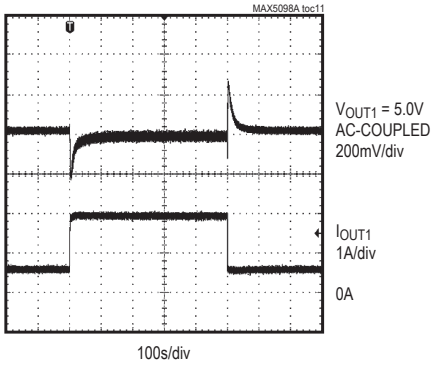
Typical Operating Characteristics (continued)

(See the *Typical Application Circuit*, unless otherwise noted. V+ = V_{IN_HIGH} = 14V, unless otherwise noted. V+ = V_{IN_HIGH} means that N1 is shorted externally.)

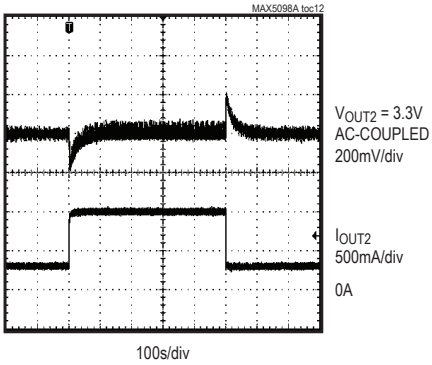
LINE-TRANSIENT RESPONSE (BUCK CONVERTER)



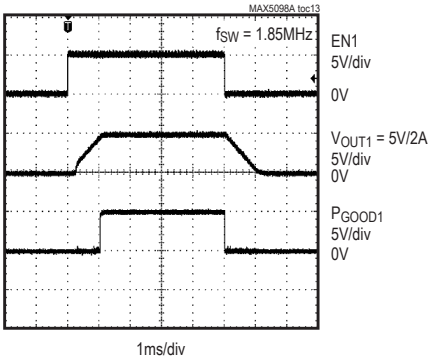
CONVERTER 1 LOAD-TRANSIENT RESPONSE



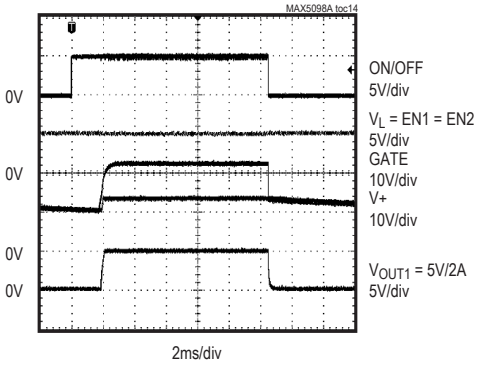
CONVERTER 2 LOAD-TRANSIENT RESPONSE



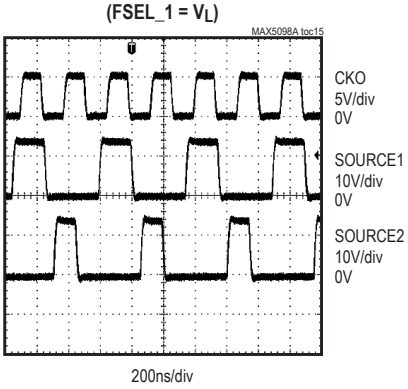
SOFT-START/SOFT-STOP FROM EN1



SOFT-START FROM ON/OFF



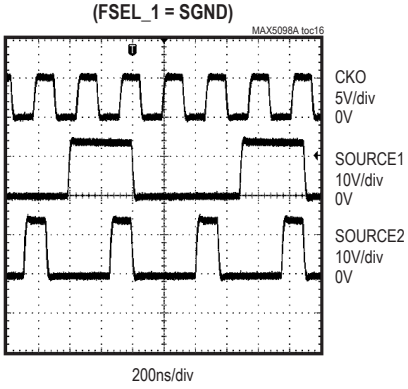
OUT-OF-PHASE OPERATION (FSEL_1 = V_L)



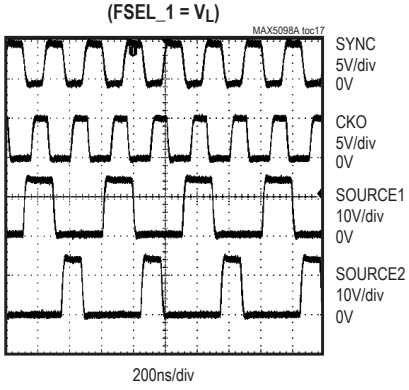
Typical Operating Characteristics (continued)

(See the *Typical Application Circuit*, unless otherwise noted. V+ = V_{IN_HIGH} = 14V, unless otherwise noted. V+ = V_{IN_HIGH} means that N1 is shorted externally.)

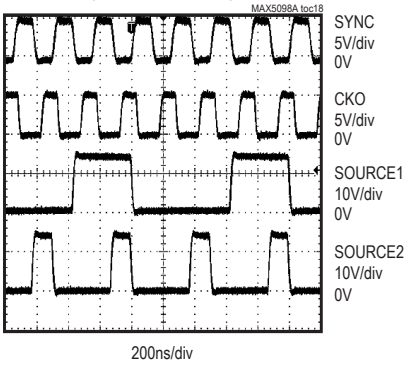
OUT-OF-PHASE OPERATION (FSEL_1 = SGND)



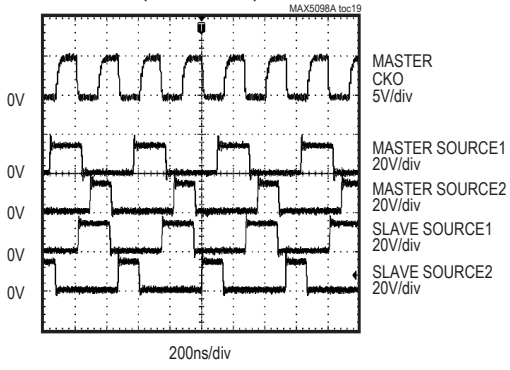
EXTERNAL SYNCHRONIZATION (FSEL_1 = V_L)



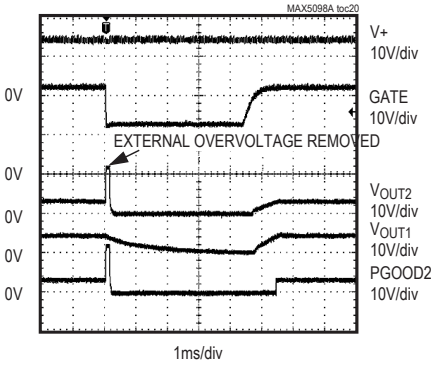
EXTERNAL SYNCHRONIZATION (FSEL_1 = SGND)



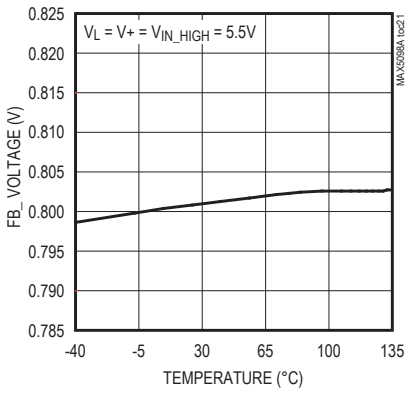
FOUR-PHASE OPERATION (FSEL_1 = V_L)



OVP BEHAVIOR



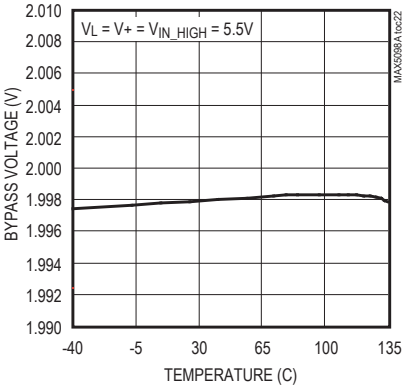
FB_ VOLTAGE vs. TEMPERATURE



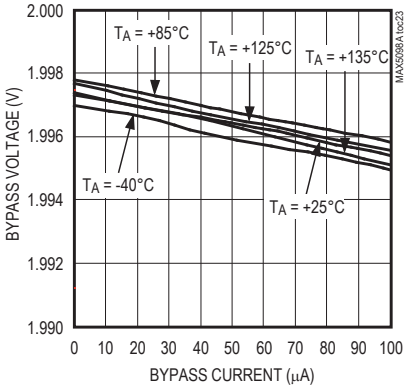
Typical Operating Characteristics (continued)

(See the *Typical Application Circuit*, unless otherwise noted. V+ = V_{IN_HIGH} = 14V, unless otherwise noted. V+ = V_{IN_HIGH} means that N1 is shorted externally.)

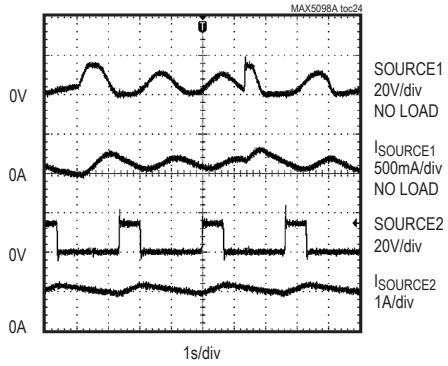
BYPASS VOLTAGE vs. TEMPERATURE



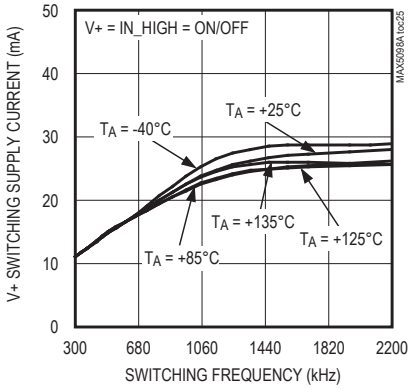
BYPASS VOLTAGE vs. BYPASS CURRENT



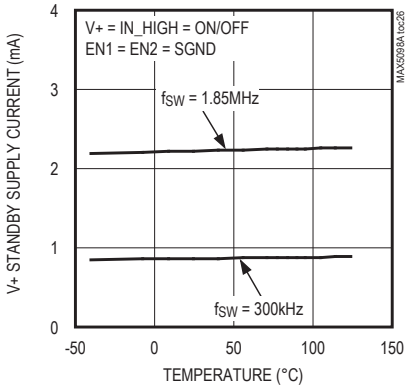
SOURCE1, SOURCE1 INDICATOR CURRENT, SOURCE2, SOURCE2 INDICATOR CURRENT



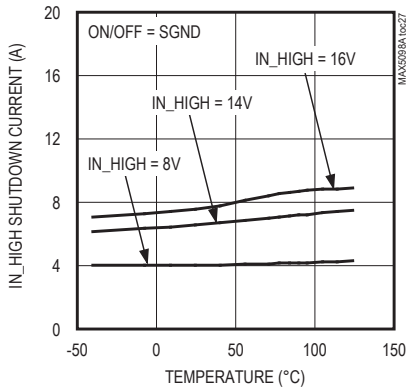
V+ SWITCHING SUPPLY CURRENT vs. SWITCHING FREQUENCY



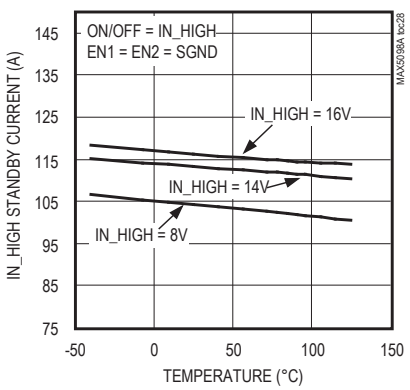
V+ STANDBY SUPPLY CURRENT vs. TEMPERATURE



IN_HIGH SHUTDOWN CURRENT vs. TEMPERATURE



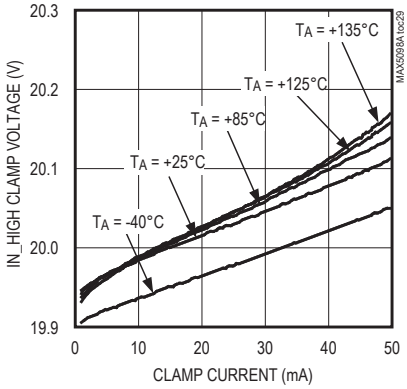
IN_HIGH STANDBY CURRENT vs. TEMPERATURE



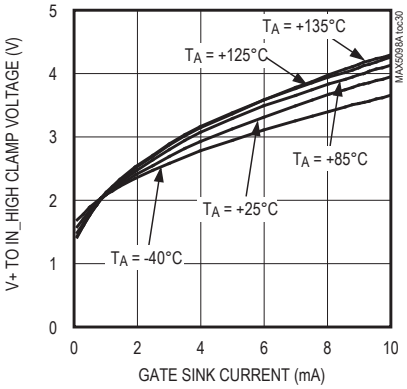
Typical Operating Characteristics (continued)

(See the *Typical Application Circuit*, unless otherwise noted. V+ = V_{IN_HIGH} = 14V, unless otherwise noted. V+ = V_{IN_HIGH} means that N1 is shorted externally.)

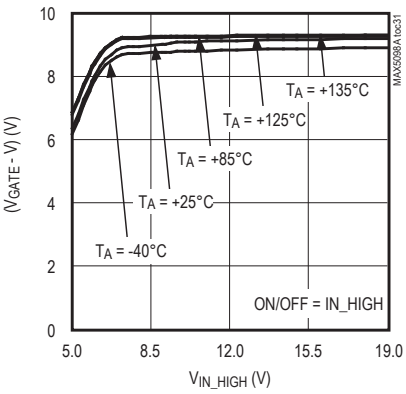
IN_HIGH CLAMP VOLTAGE vs. CLAMP CURRENT



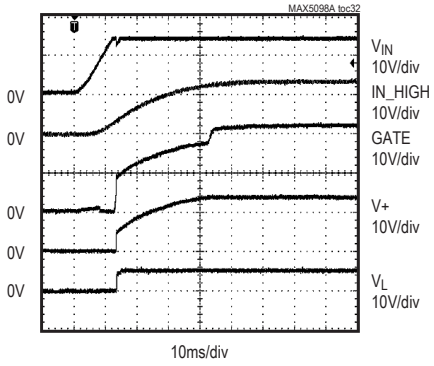
V+ TO IN_HIGH CLAMP VOLTAGE vs. GATE SINK CURRENT



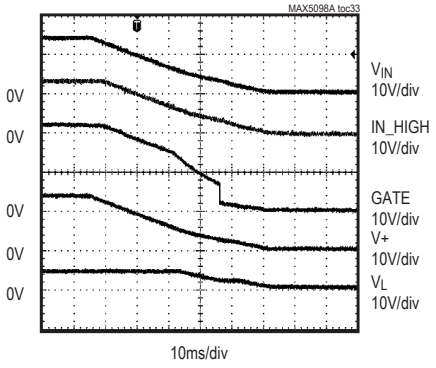
(V_{GATE} - V) vs. V_{IN_HIGH}



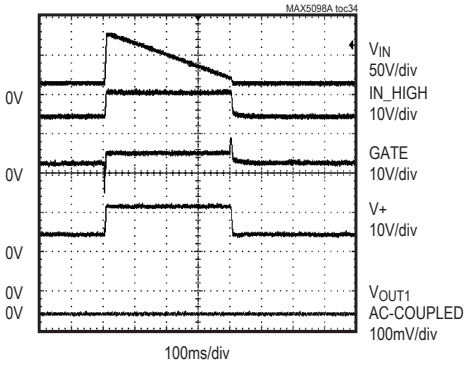
SYSTEM TURN-ON FROM BATTERY



SYSTEM TURN-OFF FROM BATTERY



SYSTEM LOAD-DUMP



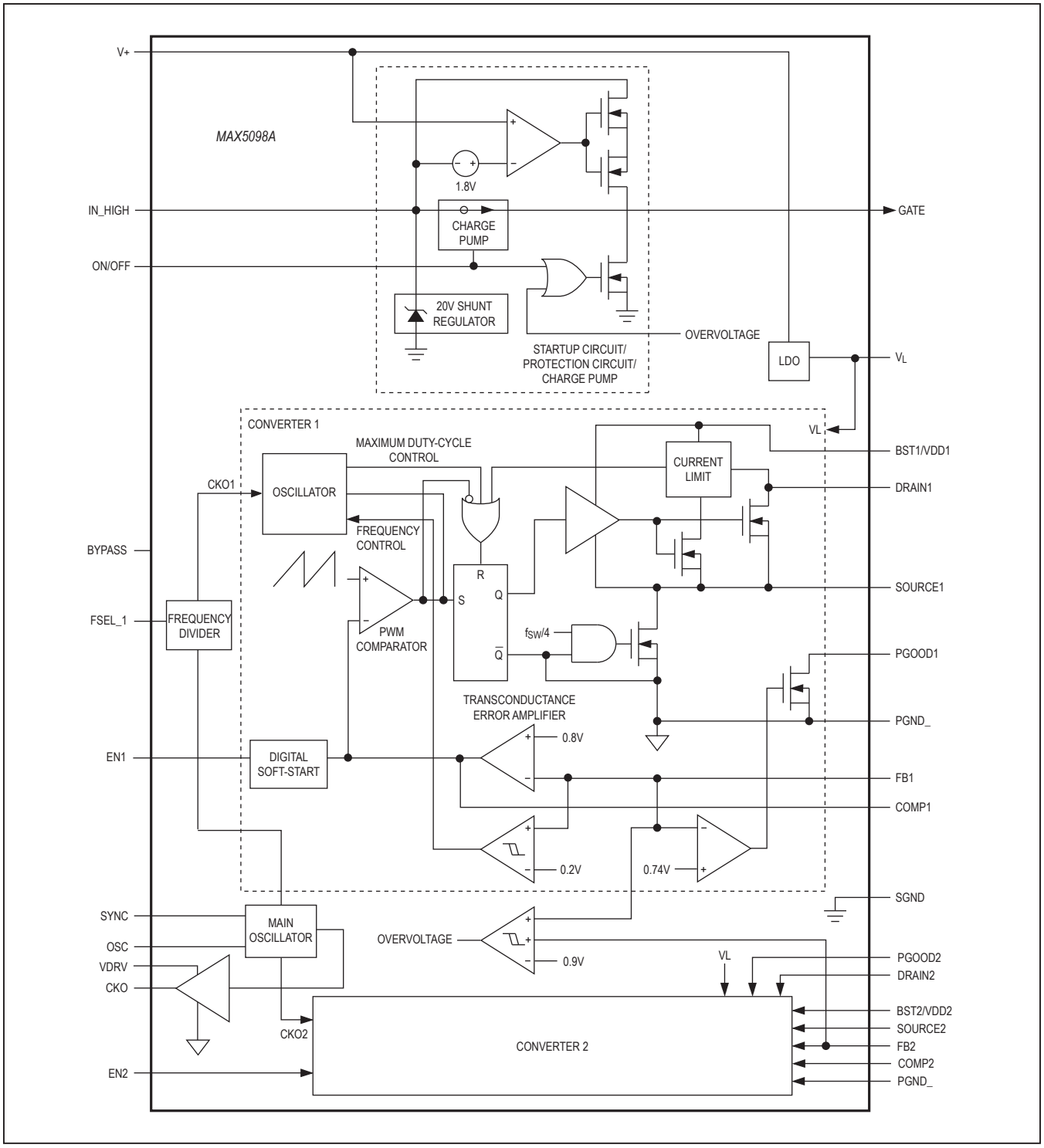
Pin Description

PIN	NAME	FUNCTION
1, 32	SOURCE2	Converter 2 Internal MOSFET Source Connection. For buck converter operation, connect SOURCE2 to the switched side of the inductor. For boost operation, connect SOURCE2 to PGND_ (Figure 6).
2, 3	DRAIN2	Converter 2 Internal MOSFET Drain Connection. For buck converter operation, use the MOSFET as a high-side switch and connect DRAIN2 to the DC-DC converters supply input rail. For boost converter operation, use the MOSFET as a low-side switch and connect DRAIN2 to the inductor and diode junction (Figure 6).
4	PGOOD2	Converter 2 Open-Drain Power-Good Output. PGOOD2 goes low when converter 2's output falls below 92.5% of its set regulation voltage. Use PGOOD2 and EN1 to sequence the converters. Converter 2 starts first.
5	EN2	Converter 2 Active-High Enable Input. Connect to V_L for always-on operation.
6	FB2	Converter 2 Feedback Input. Connect FB2 to a resistive divider between converter 2's output and SGND to adjust the output voltage. To set the output voltage below 0.8V, connect FB2 to a resistive voltage-divider from BYPASS to regulator 2's output (Figure 3). See the *Setting the Output Voltage* section.
7	COMP2	Converter 2 Internal Transconductance Amplifier Output. See the *Compensation* section.
8	OSC	Oscillator Frequency Set Input. Connect a resistor from OSC to SGND (R_{OSC}) to set the switching frequency (see the *Setting the Switching Frequency* section). Set R_{OSC} for an oscillator frequency equal to the SYNC input frequency when using external synchronization. R_{OSC} is still required when an external clock is connected to the SYNC input. See the *Synchronization (SYNC)/Clock Output (CKO)* section.
9	SYNC	External Clock Synchronization Input. Connect SYNC to a 400kHz to 4400kHz clock to synchronize the switching frequency with the system clock. Each converter frequency is 1/2 of the frequency applied to SYNC (FSEL_1 = V_L). For FSEL_1 = SGND, the switching frequency of converter 1 becomes 1/4 of the SYNC frequency. Connect SYNC to SGND when not used.
10	GATE	Gate Drive Output. Connect to the gate of the external n-channel load-dump protection MOSFET. GATE = IN_HIGH + 9V (typ) with IN_HIGH = 12V. GATE pulls to IN_HIGH by an internal n-channel MOSFET when V+ raises 2V above IN_HIGH. Leave gate unconnected if the load-dump protection is not used (MOSFET not installed).
11	ON/OFF	n-Channel Switch Enable Input. Drive ON/OFF high for normal operation. Drive ON/OFF low to turn off the external n-channel load-dump protection MOSFET and reduce the supply current to 7µA (typ). When ON/OFF is driven low, both DC-DC converters are disabled and the PGOOD_ outputs are driven low. Connect to V+ if the external load-dump protection is not used (MOSFET not installed).
12	IN_HIGH	Startup Input. IN_HIGH is protected by internally clamping to 21V (max). Connect a resistor (4kΩ max) from IN_HIGH to the drain of the protection switch. Bypass IN_HIGH with a 4.7µF electrolytic or 1µF minimum ceramic capacitor. Connect to V+ if the external load-dump protection is not used (MOSFET not installed).
13	V+	Input Supply Voltage. V+ can range from 5.2V to 19V. Connect V+, IN_HIGH, and V_L together for 4.5V to 5.5V input operation. Bypass V+ to SGND with a 1µF minimum ceramic capacitor.
14	V_L	Internal Regulator Output. The V_L regulator is used to supply the drive current at input VDRV. When driving VDRV, use an RC lowpass filter to decouple switching noise from VDRV to the V_L regulator (see the *Typical Application Circuit*). Bypass V_L to SGND with a 4.7µF minimum ceramic capacitor.
15	SGND	Signal Ground. Connect SGND to exposed pad and to the board signal ground plane. Connect the board signal ground and power ground planes together at a single point.

Pin Description (continued)

PIN	NAME	FUNCTION
16	BYPASS	Reference Output Bypass Connection. Bypass to SGND with a 0.22µF or greater ceramic capacitor.
17	FSEL_1	Converter 1 Frequency Select Input. Connect FSEL_1 to V_L for normal operation. Connect FSEL_1 to SGND to reduce converter 1's switching frequency to 1/2 of converter 2's switching frequency (Converter 1 switching frequency is 1/4 the CKO frequency). Do not leave FSEL_1 unconnected.
18	COMP1	Converter 1 Internal Transconductance Amplifier Output. See the *Compensation* section.
19	FB1	Converter 1 Feedback Input. Connect FB1 to a resistive divider between converter 1's output and SGND to adjust the output voltage. To set the output voltage below 0.8V, connect FB1 to a resistive voltage-divider from BYPASS to regulator 1's output (Figure 3). See the *Setting the Output Voltage* section.
20	EN1	Converter 1 Active-High Enable Input. Connect to V_L for an always-on operation.
21	PGOOD1	Converter 1 Open-Drain Power-Good Output. PGOOD1 output goes low when converter 1's output falls below 92.5% of its set regulation voltage. Use PGOOD1 and EN2 to sequence the converters. Converter 1 starts first.
22, 23	DRAIN1	Converter 1 Internal MOSFET Drain Connection. For buck converter operation, use the MOSFET as a high-side switch and connect DRAIN1 to the DC-DC converters supply input rail. For boost converter operation, use the MOSFET as a low-side switch and connect DRAIN1 to the inductor and diode junction (Figure 6).
24, 25	SOURCE1	Converter 1 Internal MOSFET Source Connection. For buck operation, connect SOURCE1 to the switched side of the inductor. For boost operation, connect SOURCE1 to PGND_ (Figure 6).
26	BST1/V_{DD1}	Converter 1 Bootstrap Flying-Capacitor Connection. For buck converter operation, connect BST1/V_{DD1} to a 0.1µF ceramic capacitor and diode according to the *Typical Application Circuit*. For boost converter Operation, driver bypass capacitor connection. Connect to VDRV and bypass with a 0.1µF ceramic capacitor to PGND_ (Figure 6).
27	VDRV	Low-Side Driver Supply Input. Connect VDRV to V_L through an RC filter to bypass switching noise to the internal V_L regulator. For buck converter operation, connect anode terminals of external bootstrap diodes to VDRV. For boost converter operation, connect VDRV to BST1/VDD1 and BST2/VDD2. Bypass with a minimum 2.2µF ceramic capacitor to PGND_ (see the *Typical Application Circuit*). **Do not connect to an external supply**.
28	CKO	Clock Output. CKO is an output with twice the frequency of each converter (FSEL_1 = V_L) and 90° out-of-phase with respect to converter 1. Connect CKO to the SYNC input of another MAX5098A for a four-phase converter.
29, 30	PGND1, PGND2	Power Ground. Connect both PGND1 and PGND2 together and to the board power ground plane.
31	BST2/V_{DD2}	Converter 2 Bootstrap Flying-Capacitor Connection. For buck converter operation, connect BST2/V_{DD2} to a 0.1µF ceramic capacitor and diode according to the *Typical Application Circuit*. For boost converter operation, driver bypass capacitor connection. Connect to VDRV and bypass with a 0.1µF ceramic capacitor from BST2/V_{DD2} to PGND_ (Figure 6).
—	EP	Exposed Pad. Connect EP to SGND. For enhanced thermal dissipation, connect EP to a copper area as large as possible. Do not use EP as the sole ground connection.

Functional Diagram



Detailed Description

PWM Controller

The MAX5098A dual DC-DC converter uses a pulse-width-modulation (PWM) voltage-mode control scheme. On each converter the device includes one integrated n-channel MOSFET switch and requires an external low-forward-drop Schottky diode for output rectification. The controller generates the clock signal by dividing down the internal oscillator (f_{CKO}) or the SYNC input when driven by an external clock, therefore each controller's switching frequency equals half the oscillator frequency ($f_{SW} = f_{CKO}/2$) or half of the SYNC input frequency ($f_{SW} = f_{SYNC}/2$). An internal transconductance error amplifier produces an integrated error voltage at COMP_, providing high DC accuracy. The voltage at COMP_ sets the duty cycle using a PWM comparator and a ramp generator. At each rising edge of the clock, converter 1's MOSFET switch turns on and remains on until either the appropriate or maximum duty cycle is reached, or the maximum current limit for the switch is reached. Converter 2 operates 180° out-of-phase, so its MOSFET switch turns on at each falling edge of the clock.

In the case of buck operation (see the *Typical Application Circuit*), the internal MOSFET is used in high-side configuration. During each MOSFET's on-time, the associated inductor current ramps up. During the second half of the switching cycle, the high-side MOSFET turns off and forward biases the Schottky rectifier. During this time, the SOURCE_ voltage is clamped to a diode drop (V_D) below ground. A low forward voltage drop (0.4V) Schottky diode must be used to ensure the SOURCE_ voltage does not go below -0.6V abs max. The inductor releases the stored energy as its current ramps down, and provides current to the output. The bootstrap capacitor is also recharged when the SOURCE_ voltage goes low during the high-side MOSFET off-time. The maximum duty-cycle limit ensures proper bootstrap charging at startup or low input voltages. The circuit goes in discontinuous conduction mode operation at light load, when the inductor current completely discharges before the next cycle commences. Under overload conditions, when the inductor current exceeds the peak current limit of the respective switch, the high-side MOSFET turns off quickly and waits until the next clock cycle.

In the case of boost operation, the MOSFET is a low-side switch (Figure 6). During each on-time, the inductor current ramps up. During the second half of the switching cycle, the low-side switch turns off and forward biases the Schottky diode. During this time, the DRAIN_ voltage is clamped to a diode drop (V_D) above V_{OUT}_ and the inductor provides energy to the output as well as replenishes the output capacitor charge.

ON/OFF

The MAX5098A provides an input (ON/OFF) to turn on and off the external load-dump protection MOSFET. Drive ON/OFF high for normal operation. Drive ON/OFF low to turn off the external n-channel load-dump protection MOSFET and reduce the supply current to 7µA (typ). When ON/OFF is driven low, the converter also turns off, and the PGOOD_ outputs are driven low. V+ will be self discharged through the converters output currents and the IC supply current.

Internal Oscillator/Out-of-Phase Operation

The internal oscillator generates the 180° out-of-phase clock signal required by each regulator. The switching frequency of each converter (f_{SW}) is programmable from 200kHz to 2.2MHz using a single 1% resistor at R_{OSC}. See the *Setting the Switching Frequency* section.

With dual synchronized out-of-phase operation, the MAX5098A's internal MOSFETs turn on 180° out-of-phase. The instantaneous input current peaks of both regulators do not overlap, resulting in reduced RMS ripple current and input-voltage ripple. This reduces the required input capacitor ripple current rating, allows for fewer or less expensive capacitors, and reduces shielding requirements for EMI.

Synchronization (SYNC)/ Clock Output (CKO)

The main oscillator can be synchronized to the system clock by applying an external clock (f_{SYNC}) at SYNC. The f_{SYNC} frequency must be twice the required operating frequency of an individual converter. Use a TTL logic signal for the external clock with at least 100ns pulse width. R_{OSC} is still required when using external synchronization. Program the internal oscillator frequency to have $f_{SW} = 1/2\ f_{SYNC}$. The device is properly synchronized if the SYNC frequency, f_{SYNC}, varies within ±20%.

Two MAX5098As can be connected in the master-slave configuration for four ripple-phase operation (Figure 1). The MAX5098A provides a clock output (CKO) that is 45° phase-shifted with respect to the internal switch turn-on edge. Feed the CKO of the master to the SYNC input of the slave. The effective input ripple switching frequency is four times the individual converter's switching frequency. When driving the master converter using an external clock at SYNC, set the f_{SYNC} clock duty cycle to 50% for effective 90° phase-shifted interleaved operation. When a SYNC is applied (and FSEL_1 = 0), converter 1 duty cycle is limited to 75% (max).

Input Voltage (V+)/ Internal Linear Regulator (VL)

All internal control circuitry operates from an internally regulated nominal voltage of 5.2V (V_L). At higher input voltages (V+) of 5.2V to 19V, V_L is regulated to 5.2V. At 5.2V or below, the internal linear regulator operates in dropout mode, where V_L follows V_+. Depending on the load on V_L, the dropout voltage can be high enough to reduce V_L below the undervoltage lockout (UVLO) threshold. Do not use V_L to power external circuitry.

For input voltages less than 5.5V, connect V+ and V_L together. The load on V_L is proportional to the switching frequency of converter 1 and converter 2. See the V_L Output Voltage vs. Converter Switching Frequency graph in the *Typical Operating Characteristics*. For input voltage ranges higher than 5.5V, disconnect V_L from V+.

Bypass V+ to SGND with a 1µF or greater ceramic capacitor placed close to the MAX5098A. Bypass V_L with a 4.7µF ceramic capacitor to SGND.

Undervoltage Lockout/ Soft-Start/Soft-Stop

The MAX5098A includes an undervoltage lockout with hysteresis and a power-on-reset circuit for converter turn-on and monotonic rise of the output voltage. The falling UVLO threshold is internally set to 4.1V (typ) with 180mV hysteresis. Hysteresis at UVLO eliminates “chattering” during startup. When V_L drops below UVLO, the internal MOSFET switches are turned off.

The MAX5098A digital soft-start reduces input inrush currents and glitches at the input during turn-on. When UVLO is cleared and EN_ is high, digital soft-start slowly ramps up the internal reference voltage in 64 steps. The total soft-start period is 4096 internal oscillator switching cycles.

Driving EN_ low initiates digital soft-stop that slowly ramps down the internal reference voltage in 64 steps. The total soft-stop period is equal to the soft-start period.

To calculate the soft-start/soft-stop period, use the following equation:

$$t_{SS}(ms) = \frac{4096}{f_{CKO}(kHz)}$$

where f_{CKO} is the internal oscillator and f_{CKO} is twice each converters’ switching frequency (FSEL_1 = V_L).

Enable (EN1, EN2)

The MAX5098A dual converter provides separate enable inputs, EN1 and EN2, to individually control or sequence the output voltages. These active-high enable inputs are TTL compatible. Driving EN_ high initiates soft-start of the converter, and PGOOD_ goes logic-high when the converter output voltage reaches the $V_{TPGOOD\_}$ threshold. Driving EN_ low initiates a soft-stop of the converter, and immediately forces PGOOD_ low. Use EN1, EN2, and PGOOD1 for sequencing (see Figure 2). Connect PGOOD1 to EN2 to make sure converter 1’s output is within regulation before converter 2 starts. Add an RC network from V_L to EN1 and EN2 to delay the individual converter. Sequencing reduces input inrush current and possible chattering. Connect EN_ to V_L for always-on operation.

PGOOD_

Converter 1 and converter 2 include a power-good flag, PGOOD1 and PGOOD2, respectively. Since PGOOD_ is an open-drain output and can sink 3mA while providing the TTL logic-low signal, pull PGOOD_ to a logic voltage to provide a logic-level output. PGOOD1 goes low when converter 1’s feedback FB1 drops to 92.5% ($V_{TPGOOD\_}$) of its nominal set point. The same is true for converter 2. Connect PGOOD_ to SGND or leave unconnected if not used.

Current Limit

The internal MOSFET switch current of each converter is monitored during its on-time. When the peak switch current crosses the current-limit threshold of 3.45A (typ) and 2.1A (typ) for converter 1 and converter 2, respectively, the on-cycle is terminated immediately and the inductor is allowed to discharge. The MOSFET is turned on at the next clock pulse, initiating a new switching cycle.

In deep overload or short-circuit conditions when the $V_{FB\_}$ voltage drops below 0.2V, the switching frequency is reduced to 1/4 x f_{SW} to provide sufficient time for the inductor to discharge. During overload conditions, if the voltage across the inductor is not high enough to allow for the inductor current to properly discharge, current runaway may occur. Current runaway can destroy the device in spite of internal thermal-overload protection. Reducing the switching frequency during overload conditions allows more time for inductor discharge and prevents current runaway.

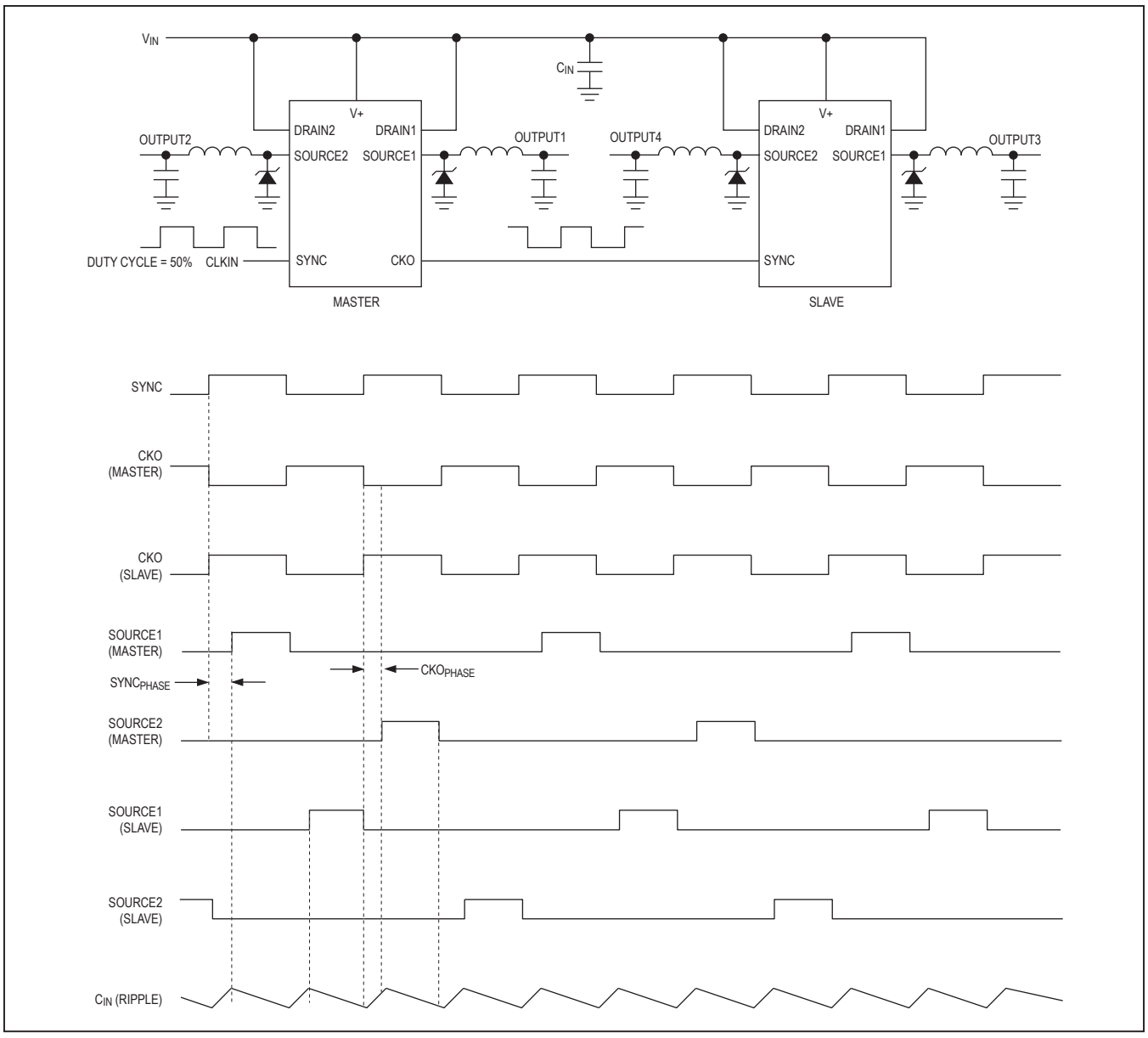


Figure 1. Synchronized Controllers

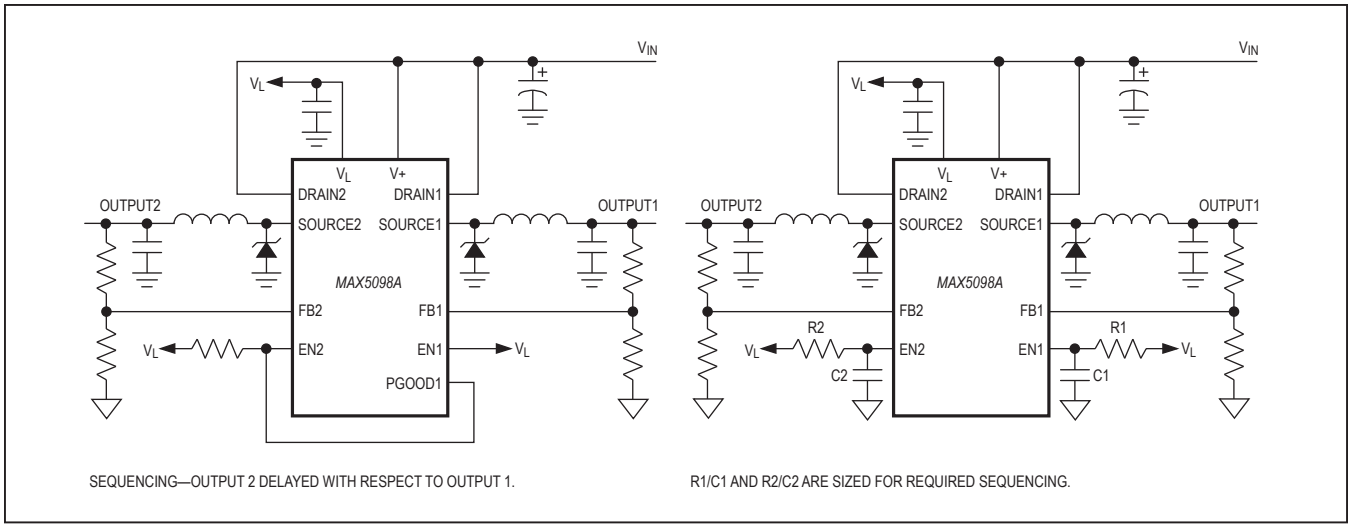


Figure 2. Power-Supply Sequencing Configurations

Output Overvoltage Protection

The MAX5098A outputs are protected from output voltage overshoots due to input transients and shorting the output to a high voltage. When the output voltage rises above the overvoltage threshold, 110% (typ) nominal FB_, the overvoltage condition is triggered. When the overvoltage condition is triggered on either channel, both converters are immediately turned off, 20Ω pulldown switches from SOURCE_ to PGND_ are turned on to help the output-voltage discharge, and the gate of the load-dump protection external MOSFET is pulled low. The device restarts as soon as both converter outputs discharge, bringing both FB_ input voltages below 12.5V of their nominal set points.

Thermal-Overload Protection

During continuous short circuit or overload at the output, the power dissipation in the IC can exceed its limit. The MAX5098A provides thermal shutdown protection with temperature hysteresis. Internal thermal shutdown is provided to avoid irreversible damage to the device. When the die temperature exceeds +165°C (typ), an on-chip thermal sensor shuts down the device, forcing the internal switches to turn off, allowing the IC to cool. The thermal sensor turns the part on again with soft-start after the junction temperature cools by +20°C. During thermal shutdown, both regulators shut down, PGOOD_ goes low, and soft-start resets. The internal 20V zener clamp from IN_HIGH to SGND is not turned off during thermal shutdown because clamping action must be always active.

Applications Information

Setting the Switching Frequency

The controller generates the clock signal by dividing down the internal oscillator f_{OSC} or the SYNC input signal when driven by an external oscillator. The switching frequency equals half the internal oscillator frequency ($f_{SW} = f_{OSC}/2$). The internal oscillator frequency is set by a resistor (R_{OSC}) connected from OSC to SGND. To find R_{OSC} for each converter switching frequency f_{SW}, use the formulas:

$$R_{OSC}(k\Omega) = \frac{10.721}{f_{SW}(MHz)^{0.920}} (f_{SW} \geq 1.25MHz)$$

$$R_{OSC}(k\Omega) = \frac{12.184}{f_{SW}(MHz)^{0.973}} (f_{SW} < 1.25MHz)$$

A rising clock edge on SYNC is interpreted as a synchronization input. If the SYNC signal is lost, the internal oscillator takes control of the switching rate, returning the switching frequency to that set by R_{OSC}. When an external synchronization signal is used, R_{OSC} must be selected such that f_{SW} = 1/2 f_{SYNC}. When f_{SYNC} clock signal is applied, f_{CKO} equals f_{SYNC} waveform, phase shifted by 180°. If the MAX5098A is running without external synchronization, f_{CKO} equals the internal oscillator frequency f_{OSC}.

Buck Converter

Effective Input Voltage Range

Although the MAX5098A converter can operate from input supplies ranging from 5.2V to 19V, the input voltage range can be effectively limited by the MAX5098A duty-cycle limitations for a given output voltage. The maximum input voltage is limited by the minimum on-time ($t_{ON(MIN)}$):

$$V_{IN(MAX)} \leq \frac{V_{OUT}}{t_{ON(MIN)} \times f_{SW}}$$

where $t_{ON(MIN)}$ is 100ns. The minimum input voltage is limited by the maximum duty cycle (D_{MAX} = 0):

$$V_{IN(MIN)} = \left[\frac{V_{OUT} + V_{DROP1}}{D_{MAX}}\right] + V_{DROP2} - V_{DROP1}$$

where V_{DROP1} is the total parasitic voltage drops in the inductor discharge path, which includes the forward voltage drop (V_D) of the rectifier, the series resistance of the inductor, and the PCB resistance. V_{DROP2} is the total resistance in the charging path that includes the on-resistance of the high-side switch, the series resistance of the inductor, and the PCB resistance.

Setting the Output Voltage

For 0.8V or greater output voltages, connect a voltage-divider from OUT_ to FB_ to SGND (Figure 3). Select R_B (FB_ to SGND resistor) to between 1kΩ and 20kΩ. Calculate R_A (OUT_ to FB_ resistor) with the following equation:

$$R_A = R_B\left[\left(\frac{V_{OUT\_}}{V_{FB\_}}\right) - 1\right]$$

where $V_{FB\_}$ = 0.8V (see the *Electrical Characteristics* table) and $V_{OUT\_}$ can range from $V_{FB\_}$ to 28V (boost operation).

For output voltages below 0.8V, set the MAX5098A output voltage by connecting a voltage-divider from OUT_ to FB_ to BYPASS (Figure 3). Select RC (FB_ to BYPASS resistor) in the 50kΩ range. Calculate R_A with the following equation:

$$R_A = R_C\left[\frac{V_{FB\_} - V_{OUT\_}}{V_{BYPASS} - V_{FB\_}}\right]$$

where $V_{FB\_}$ = 0.8V, V_{BYPASS} = 2V (see the *Electrical Characteristics* table), and $V_{OUT\_}$ can range from 0V to $V_{FB\_}$.

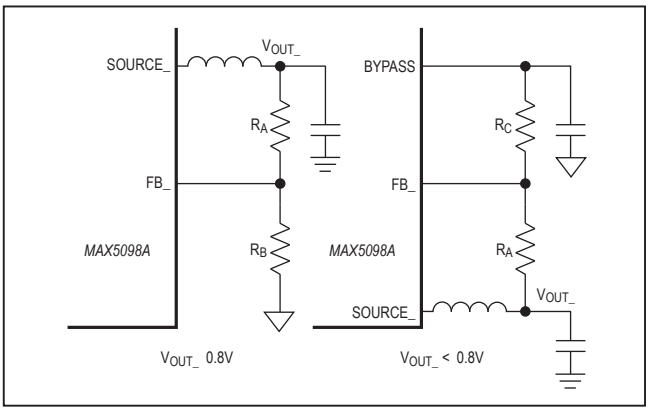


Figure 3. Adjustable Output Voltage

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX5098A: inductance value (L), peak inductor current (I_L), and inductor saturation current (I_{SAT}). The minimum required inductance is a function of operating frequency, input-to-output voltage differential and the peak-to-peak inductor current (ΔI_L). A good compromise is to choose ΔI_L equal to 30% of the full load current. To calculate the inductance, use the following equation:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

where V_{IN} and V_{OUT} are typical values (so that efficiency is optimum for typical conditions). The switching frequency is set by R_{OSC} (see the *Setting the Switching Frequency* section). The peak-to-peak inductor current, which reflects the peak-to-peak output ripple, is worse at the maximum input voltage. See the *Output Capacitor* section to verify that the worst-case output ripple is acceptable. The inductor saturation current is also important to avoid runaway current during output overload and continuous short circuit. Select the I_{SAT} to be higher than the maximum peak current limits of 4.3A and 2.6A for converter 1 and converter 2.

Input Capacitor

The discontinuous input current waveform of the buck converter causes large ripple currents at the input. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple dictate the input capacitance requirement. Note that the two converters of the MAX5098A run 180° out-of-phase, thereby effectively doubling the switching frequency at the input.

The input ripple waveform would be unsymmetrical due to the difference in load current and duty cycle between converter 1 and converter 2. The worst-case misatch is when one converter is at full load while the other converter is at no load or in shutdown. The input ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use ceramic capacitors with high ripple-current capability at the input, connected between DRAIN_ and PGND_. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

and

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

where

$$D = \frac{V_{OUT}}{V_{IN}}$$

where I_{OUT} is the maximum output current from either converter 1 or converter 2, and D is the duty cycle for that converter. The frequency of each individual converter is f_{SW}. For example, at V_{IN} = 12V, V_{OUT} = 3.3V at I_{OUT} = 2A, and with L = 3.3µH, the ESR and input capacitance are calculated for a peak-to-peak input ripple of 100mV or less, yielding an ESR and capacitance value of 20mΩ and 6.8µF for 1.25MHz frequency. At low input voltages, also add one electrolytic bulk capacitor of at least 100µF on the converters' input voltage rail. This capacitor acts as an energy reservoir to avoid possible undershoot below the undervoltage lockout threshold during power-on and transient loading.

Output Capacitor

The allowable output ripple voltage and the maximum deviation of the output voltage during step load currents determines the output capacitance and its ESR. The output ripple is comprised of ΔVQ (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic or aluminum electrolytic capacitors at the output. For aluminum electrolytic capacitors, the entire output ripple is contributed by ΔV_{ESR}. Use the ESR_{OUT} equation to calculate the ESR requirement and choose the capacitor accordingly. If using ceramic capacitors, assume the contribution to the output ripple voltage from the ESR and the capacitor discharge are equal. Calculate the output capacitance and ESR required for a specified ripple using the following equations:

$$ESR_{OUT} = \frac{\Delta V_{ESR}}{\Delta I_L}$$

$$C_{OUT} = \frac{\Delta I_L}{8 \times \Delta V_Q \times f_{SW}}$$

where

$$\Delta V_{O\_RIPPLE} \cong \Delta V_{ESR} + \Delta V_Q$$

ΔI_L is the peak-to-peak inductor current as calculated above and f_{SW} is the individual converter's switching frequency.

The allowable deviation of the output voltage during fast transient loads also determines the output capacitance and its ESR. The output capacitor supplies the step load current until the controller responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the converter. The high switching frequency of the MAX5098A allows for higher closed-loop bandwidth, reducing $t_{RESPONSE}$ and the output capacitance requirement. The resistive drop across the output capacitor ESR and the capacitor discharge causes a voltage droop during a step load. Use a combination of low-ESR tantalum or polymer and ceramic capacitors for better transient load and ripple/noise performance. Keep the maximum output voltage deviation within the tolerable limits of the electronics being powered. When using a ceramic capacitor, assume 80% and 20% contribution from the output capacitance discharge and the ESR drop, respectively. Use the following equations to calculate the required ESR and capacitance value:

$$ESR_{OUT} = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_Q}$$

where I_{STEP} is the load step and $t_{RESPONSE}$ is the response time of the controller. Controller response time depends on the control-loop bandwidth.

Boost Converter

The MAX5098A can be configured for step-up conversion since the internal MOSFET can be used as a low-side switch. Use the following equations to calculate the values for the inductor (L_{MIN}), input capacitor (C_{IN}), and output capacitor (C_{OUT}) when using the converter in boost operation.

Inductor

Choose the minimum inductor value so the converter remains in continuous mode operation at minimum output curt (I_{OMIN})

$$L_{MIN} = \frac{V_{IN}^2 \times D}{2 \times f_{SW} \times V_O \times I_{OMIN}}$$

where

$$D = \frac{V_O + V_D - V_{IN}}{V_O + V_D - V_{DS}}$$

The V_D is the forward voltage drop of the external Schottky diode, D is the duty cycle, and V_{DS} is the voltage drop across the internal MOSFET switch. Select the inductor with low DC resistance and with a saturation current (I_{SAT}) rating higher than the peak switch current limit of 4.3A (I_{CL1}) and 2.6A (I_{CL2}) of converter 1 and converter 2, respectively.

Input Capacitor

The input current for the boost converter is continuous and the RMS ripple current at the input is low. Calculate the capacitor value and ESR of the input capacitor using the following equations.

$$C_{IN} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_Q}$$

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_L}$$

where

$$\Delta I_L = \frac{(V_{IN} - V_{DS}) \times D}{L \times f_{SW}}$$

where V_{DS} is the voltage drop across the internal MOSFET switch. ΔI_L is the peak-to-peak inductor ripple current as calculated above. ΔV_Q is the portion of input ripple due to the capacitor discharge and ΔV_{ESR} is the contribution due to ESR of the capacitor.

Output Capacitor

For the boost converter, the output capacitor supplies the load current when the main switch is ON. The required output capacitance is high, especially at higher duty cycles. Also, the output capacitor ESR needs to be low enough to minimize the voltage drop due to the ESR while supporting the load current. Use the following equation to calculate the output capacitor for a specified output ripple tolerance.

$$ESR = \frac{\Delta V_{ESR}}{I_{PK}}$$

$$C_{OUT} = \frac{I_O \times D_{MAX}}{\Delta V_Q \times f_{SW}}$$

where I_{PK} is the peak inductor current as defined in the *Power Dissipation* section for the boost converter, I_O is the load current, ΔV_Q is the portion of the ripple due to

the capacitor discharge, and ΔV_{ESR} is the contribution due to the ESR of the capacitor. D_{MAX} is the maximum duty cycle at minimum input voltage.

Power Dissipation

The MAX5098A includes two internal power MOSFET switches. The DC loss is a function of the RMS current in the switch while the switching loss is a function of switching frequency and instantaneous switch voltage and current. Use the following equations to calculate the RMS current, DC loss, and switching loss of each converter. The MAX5098A is available in a thermally enhanced package and can dissipate up to 2.7W at +70°C ambient temperature. The total power dissipation in the package must be limited so that the operating junction temperature does not exceed its absolute maximum rating of +150°C at maximum ambient temperature.

For the buck converter

$$I_{RMS} = \sqrt{\left(I_{DC}^2 + I_{PK}^2 + \left(I_{DC} \times I_{PK}\right)\right) \times \frac{D_{MAX}}{3}}$$

$$P_{DC} = I_{RMS}^2 \times R_{DS(ON)MAX}$$

where

$$I_{DC} = I_O - \frac{\Delta I_L}{2}$$

$$I_{PK} = I_O + \frac{\Delta I_L}{2}$$

$$P_{SW} = \frac{V_{IN} \times I_O \times \left(t_R + t_F\right) \times f_{SW}}{4}$$

See the *Electrical Characteristics* table for the $R_{ON(MAX)}$ maximum value.

For the boost converter:

$$I_{RMS} = \sqrt{\left(I^2_{DC} + I^2_{PK} + \left(I_{DC} \times I_{PK}\right)\right) \times \frac{D_{MAX}}{3}}$$

$$I_{IN} = \frac{V_O \times I_O}{V_{IN} \times \eta}$$

$$\Delta I_L = \frac{\left(V_{IN} - V_{DS}\right) \times D}{L \times f_{SW}}$$

$$I_{DC} = I_{IN} - \frac{\Delta I_L}{2}$$

$$I_{PK} = I_{IN} + \frac{\Delta I_L}{2}$$

$$P_{DC} = I_{RMS}^2 \times R_{DS(ON)(MAX)}$$

where V_{DS} is the drop across the internal MOSFET and η is the efficiency. See the *Electrical Characteristics* table for the $R_{ON(MAX)}$ value.

$$P_{SW} = \frac{V_O \times I_{IN} \times \left(t_R + t_F\right) \times f_{SW}}{4}$$

where t_R and t_F are rise and fall times of the internal MOSFET. t_F can be measured in the actual application.

The supply current in the MAX5098A is dependent on the switching frequency. See the *Typical Operating Characteristics* to find the supply current of the MAX5098A at a given operating frequency. The power dissipation (P_S) in the device due to supply current (I_{SUPPLY}) is calculated using following equation.

$$P_S = V_{INMAX} \times I_{SUPPLY}$$

The total power dissipation P_T in the device is:

$$P_T = P_{DC1} + P_{DC2} + P_{SW1} + P_{SW2} + P_S$$

where P_{DC1} and P_{DC2} are DC losses in converter 1 and converter 2, respectively. P_{SW1} and P_{SW2} are switching losses in converter 1 and converter 2, respectively.

Calculate the temperature rise of the die using the following equation:

$$T_J = T_C \times (P_T \times \theta_{JC})$$

where θ_{JC} is the junction-to-case thermal impedance of the package equal to +1.7°C/W. Solder the exposed pad of the package to a large copper area to minimize the case-to-ambient thermal impedance. Measure the temperature of the copper area near the device at a worst-case condition of power dissipation and use +1.7°C/W as θ_{JC} thermal impedance.

Compensation

The MAX5098A provides an internal transconductance amplifier with its inverting input and its output available for external frequency compensation. The flexibility of external compensation for each converter offers wide selection of output filtering components, especially the output capacitor. For cost-sensitive applications, use aluminum electrolytic capacitors; for component size-sensitive applications, use low-ESR tantalum, polymer, or ceramic capacitors at the output. The high switching frequency of MAX5098A allows use of ceramic capacitors at the output.

Choose all the passive power components that meet the output ripple, component size, and component cost requirements. Choose the small-signal components for the error amplifier to achieve the desired closed-loop

bandwidth and phase margin. Use a simple pole-zero pair (Type II) compensation if the output capacitor ESR zero frequency is below the unity-gain crossover frequency (f_C). Type III compensation is necessary when the ESR zero frequency is higher than f_C or when compensating for a continuous mode boost converter that has a right-half-plane zero.

Use procedure 1 to calculate the compensation network components when $f_{ZERO,ESR} < f_C$.

Buck Converter Compensation Procedure 1 (See Figure 4)

1) Calculate the $f_{ZERO,ESR}$ and LC double-pole frequencies:

$$f_{ZERO,ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

$$f_{LC} = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}}$$

2) Select the unity-gain crossover frequency:

$$f_C \le \frac{f_{SW}}{20}$$

If the $f_{ZERO,ESR}$ is lower than f_C and close to f_{LC}, use a Type II compensation network where R_FC_F provides a midband zero $f_{MID,ZERO}$, and R_FC_{CF} provides a high-frequency pole.

3) Calculate modulator gain G_M at the crossover frequency.

$$G_M = \frac{V_{IN}}{V_{OSC}} \times \frac{ESR}{ESR + (2\pi \times f_C \times L_{OUT})} \times \frac{0.8}{V_{OUT}}$$

where V_{OSC} is a peak-to-peak ramp amplitude equal to 1V.

The transconductance error amplifier gain is:

$$G_{E/A} = g_M \times R_F$$

The total loop gain at f_C should be equal to 1:

$$G_M \times G_{E/A} = 1$$

or

$$R_F = \frac{V_{OSC}(ESR + 2\pi \times f_C \times L_{OUT}) \times V_{OUT}}{0.8 \times V_{IN} \times g_M \times ESR}$$

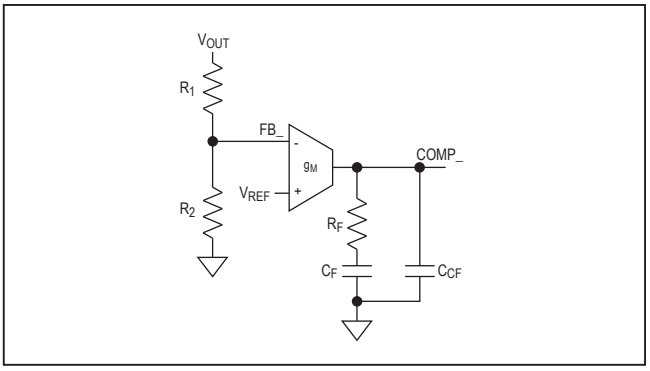


Figure 4. Type II Compensation Network

4) Place a zero at or below the LC double pole:

$$C_F = \frac{1}{2\pi \times R_F \times f_{LC}}$$

5) Place a high-frequency pole at $f_P = 0.5 \times f_{SW}$.

$$C_{CF} = \frac{C_F}{(2\pi \times 0.5 f_{SW} \times R_F \times C_F) - 1}$$

Procedure 2 (See Figure 5)

If the output capacitor used is a low-ESR ceramic type, the ESR frequency is usually far away from the targeted unity crossover frequency (f_C). In this case, Type III compensation is recommended. Type III compensation provides two-pole zero pairs. The locations of the zero and poles should be such that the phase margin peaks around f_C. It is also important to place the two zeros at or below the double pole to avoid the conditional stability issue.

1) Select a crossover frequency:

$$f_C \le \frac{f_{SW}}{20}$$

2) Calculate the LC double-pole frequency, f_{LC}:

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

3) Place a zero $f_{Z1} = \frac{1}{2\pi \times R_F \times C_F}$ at $0.75 \times f_{LC}$.

where

$$C_F = \frac{1}{2\pi \times 0.75 \times f_{LC} \times R_F}$$

and $R_F \geq 10k\Omega$.

4) Calculate C_I for a target unity crossover frequency, f_C.

$$C_I = \frac{2\pi \times f_C \times L_{OUT} \times C_{OUT} \times V_{OSC}}{V_{IN} \times R_F}$$

5) Place a pole $f_{P1} = \frac{1}{2\pi \times R_I \times C_I}$ at $f_{ZERO,ESR}$ or 5 x f_C, whichever is lower,

$$R_I = \frac{1}{2\pi \times f_{P1} \times C_I}$$

6) Place a second zero, f_{Z2}, at 0.2 x f_C or at f_{LC}, whichever is lower.

$$R1 = \frac{1}{2\pi \times f_{Z2} \times C_I} - R_I$$

7) Place a second pole at 1/2 the switching frequency.

$$C_{CF} = \frac{C_F}{(2\pi \times 0.5 \times f_{SW} \times R_F \times C_F) - 1}$$

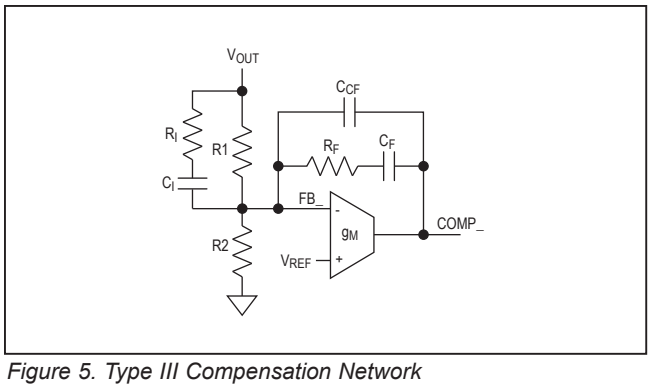


Figure 5. Type III Compensation Network

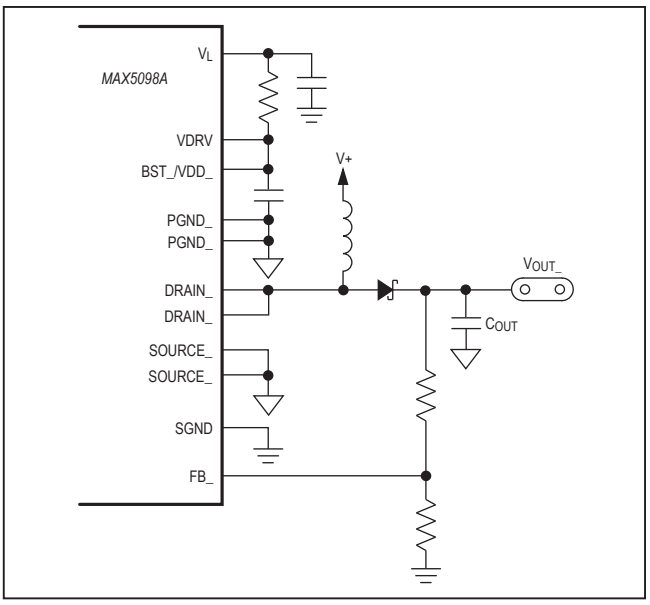


Figure 6. Boost Application

Boost Converter Compensation

The boost converter compensation gets complicated due to the presence of a right-half-plane zero $f_{ZERO,RHP}$. The right-half-plane zero causes a drop in phase while adding positive (+1) slope to the gain curve. It is important to drop the gain significantly below unity before the RHP frequency. Use the following procedure to calculate the compensation components:

1) Calculate the LC double-pole frequency, f_{LC}, and the right-half-plane-zero frequency.

$$f_{LC} = \frac{1 - D}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

$$f_{ZERO,RHP} = \frac{(1 - D)^2 R_{(MIN)}}{2\pi \times L_{OUT}}$$

where

$$D = 1 - \frac{V_{IN}}{V_{OUT}}$$

$$R_{(MIN)} = \frac{V_{OUT}}{I_{OUT(MAX)}}$$

Target the unity-gain crossover frequency for:

$$f_C \le \frac{f_{ZERO,RHP}}{5}$$

Place a zero $f_{Z1} = \frac{1}{2\pi \times R_F \times C_F}$ at $0.75 \times f_{LC}$.

where $R_F \ge 10k\Omega$.

3) Calculate C_I for a target crossover frequency, f_C:

$$C_I = \frac{V_{OSC}\left[(1-D)^2 + \omega_C{}^2 L_{OUT} C_{OUT}\right]}{\omega_C R_F V_{IN}}$$

where $\omega_C = 2\pi f_C$:

4) Place a pole $f_{P1} = \frac{1}{2\pi \times R_I \times C_I}$ at $f_{ZERO,RHP}$.

$$R_I = \frac{1}{2\pi \times f_{ZERO,RHP} \times C_I}$$

5) Place the second zero $f_{Z2} = \frac{1}{2\pi \times R1 \times C_I}$ at f_{LC}.

where

$$R1 = \frac{1}{2\pi \times f_{LC} \times C_I} - R_I$$

6) Place the second pole $f_{P2} = \frac{1}{2\pi \times R_F \times C_{CF}}$ at 1/2 the switching frequency.

$$CF = \frac{C_F}{\left(2\pi \times 0.5 \times f_{SW} \times R_F \times C_F\right) - 1}$$

Load-Dump Protection MOSFET

Select the external MOSFET with an adequate voltage rating, V_{DSS}, to withstand the maximum expected load-dump input voltage. The on-resistance of the MOSFET, $R_{DS(ON)}$, should be low enough to maintain a minimal voltage drop at full load, limiting the power dissipation of the MOSFET.

During regular operation, the power dissipated by the MOSFET is:

$$P_{NORMAL} = I_{LOAD}{}^2 \times R_{DS(ON)}$$

where I_{LOAD} is equal to the sum of both converters' input currents.

The MOSFET operates in a saturation region during load dump, with both high voltage and current applied. Choose a suitable power MOSFET that can safely operate in the saturation region. Verify its capability to support the downstream DC-DC converters input current during the load-dump event by checking its safe operating area (SOA) characteristics. Since the transient peak power dissipation on the MOSFET can be very high during the load-dump event, also refer to the thermal impedance graph given in the data sheet of the power MOSFET to make sure its transient power dissipation is kept within the recommended limits.

Improving Noise Immunity

In applications where the MAX5098A is subject to noisy environments, adjust the controller's compensation to improve the system's noise immunity. In particular, high-frequency noise coupled into the feedback loop causes jittery duty cycles. One solution is to lower the crossover frequency (see the *Compensation* section).

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. This is especially true for dual converters where one channel can affect the other. Refer to the MAX5099 Evaluation Kit data sheet for a specific layout example. Use a multilayer board whenever possible for better noise immunity. Follow these guidelines for good PCB layout:

1) For SGND, use a large copper plane under the IC and solder it to the exposed paddle. To effectively use this copper area as a heat exchanger between the PCB and ambient, expose this copper area on the top and bottom side of the PCB. Do not make a direct connection from the exposed pad copper plane to SGND underneath the IC.
2) Isolate the power components and high-current path from the sensitive analog circuitry.
3) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
4) Connect SGND and PGND_ together at a single point. Do not connect them together anywhere else (refer to the MAX5099 Evaluation Kit data sheet for more information).
5) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.
6) Ensure that the feedback connection to C_{OUT} is short and direct.
7) Route high-speed switching nodes (BST_/VDD_, SOURCE_) away from the sensitive analog areas (BYPASS, COMP_, and FB_). Use the internal PCB layer for SGND as an EMI shield to keep radiated noise away from the IC, feedback dividers, and analog bypass capacitors.

Layout Procedure

1) Place the power components first, with ground terminals adjacent (inductor, $C_{IN\_}$, and $C_{OUT\_}$). Make all these connections on the top layer with wide, copper-filled areas (2oz copper recommended).
2) Group the gate-drive components (bootstrap diodes and capacitors, and V_L bypass capacitor) together near the controller IC.
3) Make the DC-DC controller ground connections as follows:
   a) Create a small, signal ground plane underneath the IC.
   b) Connect this plane to SGND and use this plane for the ground connection for the reference (BYPASS), enable, compensation components, feedback dividers, and OSC resistor.
   c) Connect SGND and PGND_ together (this is the only connection between SGND and PGND_). Refer to the MAX5099 Evaluation Kit data sheet for more information.

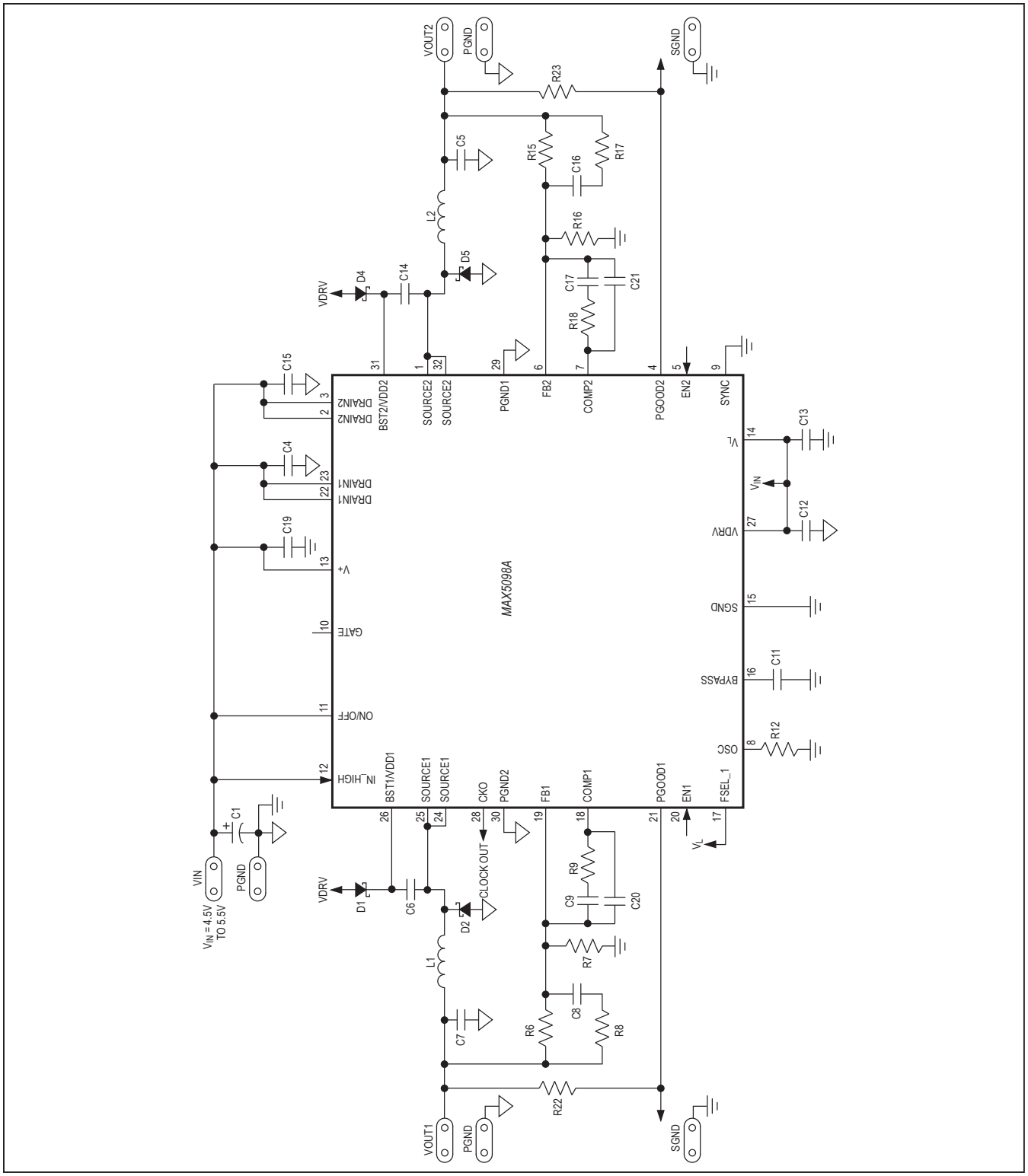
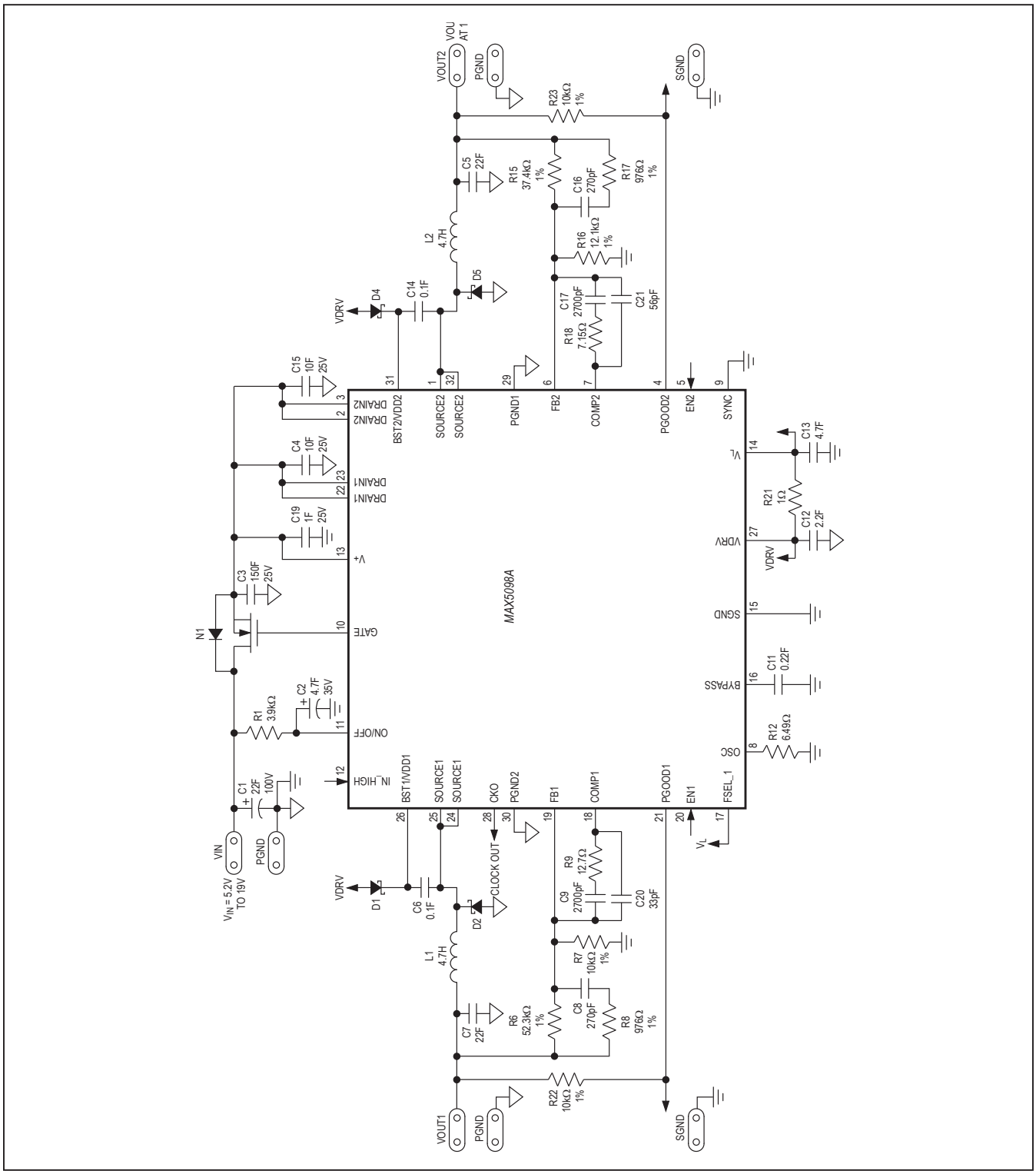
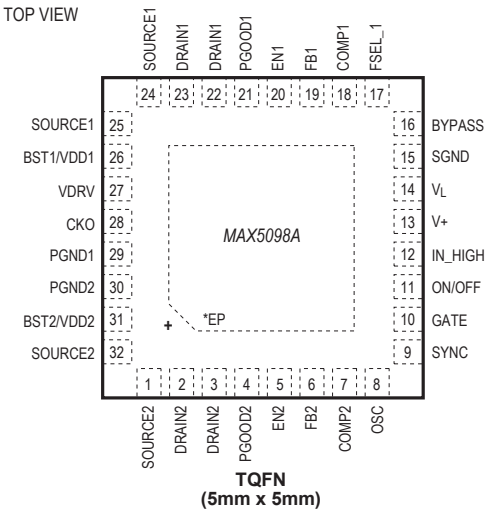


Figure 7. 4.5V to 5.5V Operation

Typical Application Circuit



Pin Configuration



TQFN
(5mm x 5mm)

*EP = EXPOSED PAD.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255+4	21-0140	90-0012

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/08	Initial release	—
1	10/14	Removed “Automotive” from the title; changed automotive references to industrial in the *General Description* and *Applications*; removed the *Load Dump Protection* section	1, 14

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