Click here for production status of specific part numbers.

MAX41460

300MHz–960MHz ASK and (G)FSK Transmitter with SPI Interface

General Description

The MAX41460 is a UHF sub-GHz ISM/SRD transmitter is designed to transmit On-Off Keying (OOK), Amplitude-Shift Keying (ASK), Frequency-Shift Keying (FSK), and Gaussian (G)FSK (or 2GFSK) data in the 286MHz to 960MHz frequency range. It integrates a fractional phase-locked-loop (PLL) so that a single, low-cost crystal can be used to generate commonly used world-wide sub-GHz frequencies. The fast response time of the PLL allows for frequency-hopping, spread spectrum protocols for increased range and security. The only frequency-dependent components required are for the external antenna-matching network.

The crystal-based architecture of the MAX41460 provides greater modulation depth, faster frequency settling, higher tolerance of the transmit frequency, and reduced temperature dependence.

The MAX41460 provides output power up to +13dBm into a 50Ω load while only drawing < 8mA for ASK (Manchester coded) and < 12mA for (G)FSK transmission at 315MHz. The output load can be adjusted to increase power up to +16dBm, and a PA boost mode can be enabled at frequencies above 850MHz to compensate for losses. The PA output power can also be controlled using programmable register settings.

The MAX41460 features single-supply operation from +1.8V to +3.6V. The device has an auto-shutdown feature to extend battery life and a fast oscillator wake-up on data activity detection. A serial programmable interface make the MAX41460 compatible with almost any microcontroller or code-hopping generator.

The MAX41460 is available in a 10-pin µMAX package and is specified over the -40°C to +105°C extended temperature range. The MAX41460 has an ESD rating of 2.5kV HBM.

Applications

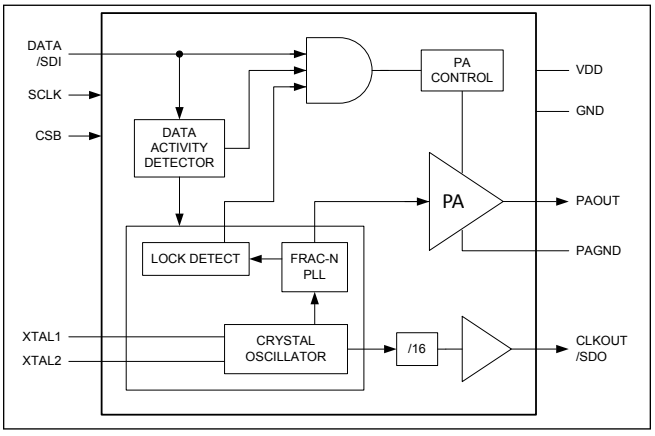
- Building Automation and Security
- Wireless Sensors and Alarms
- Remote and Passive Keyless Entry (RKE/PKE)
- Tire Pressure Monitoring Systems (TPMS)
- Automatic Meter Reading (AMR)
- Garage Door Openers (GDO)
- Radio Control Toys
- Internet of Things (IoT)

Benefits and Features

- Low Implementation Cost
  - Bits-to-RF Single-Wire Operation
  - Low Bill-of-Materials (BoM)
  - Uses Single, Low-Cost, 16MHz Crystal
  - Small 3mm x 3mm µMAX-10 Package
- Increased Range, Data Rates, and Security
  - Up to +16dBm PA Output Power
  - Fast Frequency Switching for FHSS/DSSS
  - Fast-On Oscillator: < 250µs Startup Time
  - Up to 200kbps NRZ Data Rate
- Extend Battery Life with Low Supply Current
  - < 8mA ASK Manchester Coded
  - < 12mA (G)FSK or 2GFSK at 315MHz
  - Selectable Standby and Shutdown Modes
  - Auto Shutdown at < 20nA (typ) Current
- Ease-of-Use
  - +1.8V to +3.6V Single-Supply Operation
  - Fully Programmable with SPI Interface
  - 400kHz/1MHz I²C Versions Also Available

***Ordering Information* appears at end of data sheet.**

Simplified Block Diagram



maxim integrated™

Absolute Maximum Ratings

V_{DD} to GND ..... -0.3V to +4V
All Others Pins to GND ..... -0.3V to (V_{DD} + 0.3)V
Continuous Power Dissipation (T_A = +70°C, derate 5.6mW/°C above +70°C) 444.4mW
Operating Temperature Range ..... -40°C to +105°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (reflow) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

10 µMAX (similar to 10 TSSOP)

Package Code	U10+2
Outline Number	21-0061
Land Pattern Number	90-0330
Thermal Resistance, Single-Layer Board:	
Junction-to-Ambient (θ_{JA})	180°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	36°C/W
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	113.1°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	36°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(*Typical Application Circuit*, all RF inputs and outputs are referenced to 50Ω, V_{DD} = +1.8V to +3.6V, T_A = -40°C to +105°C, P_{OUT} = +13dBm for 300MHz–450MHz or +11dBm for 863MHz–928MHz, PA_BOOST = 0, unless otherwise noted. Typical values are at V_{DD} = +3V, T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Operating Current	I_{DD}	V_{DATA} at 50% duty cycle (ASK) (Note 3, Note 4)	f_{RF} = 315MHz		7	12	mA
		V_{DATA} at 50% duty cycle (ASK) (Note 3, Note 4)	f_{RF} = 434MHz		8	12	
			f_{RF} = 863MHz–928MHz		10	19	
			f_{RF} = 315MHz, P_{OUT} = 16dBm (Note 5)		24		
			f_{RF} = 434MHz, P_{OUT} = 16dBm (Note 5)		26		
			f_{RF} = 863MHz–928MHz, P_{OUT} = 16dBm, PA_BOOST = 1 (Note 5)		45		
		V_{DATA} at 50% duty cycle (ASK), Low Phase Noise mode (Note 3, Note 4)	f_{RF} = 315MHz		9.5		
			f_{RF} = 434MHz		10.5		
			f_{RF} = 863MHz–928MHz		12.8		
		FSK (Note 2)	f_{RF} = 315MHz		12	21	
			f_{RF} = 434MHz		13	27.5	
			f_{RF} = 863MHz–928MHz		19	39	
			f_{RF} = 315MHz, P_{OUT} = 16dBm (Note 5)		28		
			f_{RF} = 434MHz, P_{OUT} = 16dBm (Note 5)		27		
			f_{RF} = 863MHz–928MHz, P_{OUT} = 16dBm, PA_BOOST = 1 (Note 5)		43		
		FSK, Low Phase Noise mode (Note 2)	f_{RF} = 315MHz		15		
			f_{RF} = 434MHz		17		
			f_{RF} = 863MHz–928MHz		20.5		
		PA off (Note 2)	f_{RF} = 315MHz		2	3	

Electrical Characteristics (continued)

(*Typical Application Circuit*, all RF inputs and outputs are referenced to 50Ω, V_{DD} = +1.8V to +3.6V, T_A = -40°C to +105°C, P_{OUT} = +13dBm for 300MHz–450MHz or +11dBm for 863MHz–928MHz, PA_BOOST = 0, unless otherwise noted. Typical values are at V_{DD} = +3V, T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			f_{RF} = 434MHz		2	3	
			f_{RF} = 863MHz–928MHz		3	4	
		PA off, Low Phase Noise mode (Note 2)	f_{RF} = 315MHz		4		
			f_{RF} = 434MHz		4		
			f_{RF} = 863MHz–928MHz		5		
Supply Voltage	V_{DD}	PA_BOOST = 0		1.8	3	3.6	V
		PA_BOOST = 1		1.8	2.7	3.0	
Standby Current	I_{STDBY}	Crystal oscillator on, everything off.	T_A = 25°C		200	500	µA
			T_A = 105°C		250		
Shutdown Current	I_{SHDN}	Everything off	T_A = 25°C		19	100	nA
MODULATION PARAMETERS							
ASK Modulation Depth		Supply current and output power are greatly dependent on board layout and PAOUT match			70		dB
FSK Frequency Deviation		Default value			±39		kHz
FSK Minimum Frequency Deviation					±1		kHz
FSK Minimum Frequency Deviation for Gaussian Shaping					±10		kHz
FSK Maximum Frequency Deviation					±100		kHz
Minimum MSK Data Rate		FSK modulation index = 0.5			4		kbps
Maximum NRZ Data Rate					200		kbps
POWER AMPLIFIER							
Output Power	P_{OUT}	f_{RF} = 300MHz–450MHz (Note 4)			13		dBm
		f_{RF} = 300MHz–450MHz (Note 4, Note 5)			17		
		f_{RF} = 863MHz–928MHz (Note 4)			11		
		f_{RF} = 863MHz–928MHz (Note 4, Note 5), PA_BOOST = 1			16		
Maximum Carrier Harmonics		PA_BOOST = 0. Supply current, output power, and harmonics are dependent on board layout and PAOUT match.			-24		dBc

Electrical Characteristics (continued)

(*Typical Application Circuit*, all RF inputs and outputs are referenced to 50Ω, V_{DD} = +1.8V to +3.6V, T_A = -40°C to +105°C, P_{OUT} = +13dBm for 300MHz–450MHz or +11dBm for 863MHz–928MHz, PA_BOOST = 0, unless otherwise noted. Typical values are at V_{DD} = +3V, T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PLL							
Frequency Range		Low Current mode (default)		286		960	MHz
		Low Phase Noise mode, LODIV = DIV12		286.7		320	
		Low Phase Noise mode, LODIV = DIV8		425		480	
		Low Phase Noise mode, LODIV = DIV4		860		960	
PLL Phase Noise		f_{RF} = 315MHz, Low Current mode (default)	f_{OFFSET} = 200kHz		-82		dBc/Hz
			f_{OFFSET} = 1MHz		-90		
		f_{RF} = 434MHz, Low Current mode (default)	f_{OFFSET} = 200kHz		-80		
			f_{OFFSET} = 1MHz		-90		
		f_{RF} = 915MHz, Low Phase Noise mode	f_{OFFSET} = 200KHz		-82		
			f_{OFFSET} = 1MHz		-104		
LO Divider Settings					4		
					8		
					12		
Minimum Synthesizer Frequency Step					$f_{XTAL}/2^{16}$		Hz
Reference Spur		f_{RF} = 315MHz	$f_{RF} \pm f_{XTAL}$		-67		dBc
		f_{RF} = 434MHz	$f_{RF} \pm f_{XTAL}$		-60		
		f_{RF} = 868MHz	$f_{RF} \pm f_{XTAL}$		-57		
		f_{RF} = 915MHz	$f_{RF} \pm f_{XTAL}$		-56		
Reference Frequency Input Level					500		mV_{P-P}
Frequency Switching Time		26MHz frequency step, 902MHz to 928MHz band, time from end of register write to frequency settled to within 5kHz of desired carrier			50		µs
Loop Bandwidth	LBW				300		kHz
LO Frequency Divider Range	N			11		72	
Turn-On Time of PLL	t_{PLL}	f_{RF} = 315MHz			30		µs
		f_{RF} = 915MHz			90		
CRYSTAL OSCILLATOR							
Crystal Frequency	f_{XTAL}	Recommended value (Note 3)		12.8	16	19.2	MHz
Crystal Oscillator Startup Time	t_{XO}	See *Preset Mode Transmission* section			243		µs
Frequency Pulling by V_{DD}					3		ppm/V

Electrical Characteristics (continued)

(*Typical Application Circuit*, all RF inputs and outputs are referenced to 50Ω, V_{DD} = +1.8V to +3.6V, T_A = -40°C to +105°C, P_{OUT} = +13dBm for 300MHz–450MHz or +11dBm for 863MHz–928MHz, PA_BOOST = 0, unless otherwise noted. Typical values are at V_{DD} = +3V, T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Crystal Input Capacitance	C_X	Internal capacitance of XTAL1 and XTAL2 pins to ground			12		pF
CMOS INPUT/OUTPUT							
Input Low Voltage	V_{IL}	SCLK/DATA/CSB	1.8V compatible			0.36	V
Input High Voltage	V_{IH}	SCLK/DATA/CSB	1.8V compatible	1.44			V
Input Current	I_{IL}/I_{IH}				±10		µA
Input Current	I_{IL}/I_{IH}	Pin CSB, internal pullup resistor				65	µA
Output Low Voltage	V_{OL}	I_{SINK} = 650µA			0.25		V
Output High Voltage	V_{OH}	I_{SOURCE} = 350µA			V_{DD} - 0.25		V
Maximum Load Capacitance at CLKOUT/SDO Pin	C_{LOAD}				10		pF
SERIAL INTERFACE (FIGURE 1)							
SCLK Frequency	f_{SCLK}	$1/t_{SCLK}$				20	MHz
SCLK to CSB Setup Time	t_{CSS}				10		ns
SCLK to CSB Hold Time	t_{CSH}				0		ns
SDI to SCLK Hold Time	t_{SDH}	Data-write			0		ns
SDI to SCLK Setup Time	t_{SDS}	Data-write			5		ns
Minimum SCLK to SDI Data Delay	t_{SDD_MIN}	Data-read, 10pF load from SDO to Ground			1.5		ns
		Data-read, 100pF load from SDO to Ground			3.5		
Maximum SCLK to SDI Data Delay	t_{SDD_MAX}	Data-read, 10pF load from SDO to Ground			8		ns
		Data-read, 100pF load from SDO to Ground			11		

Note 1: Supply current, output power and efficiency are greatly dependent on board layout and PA output match.

Note 2: 100% tested at T_A = +25°C. Limits over operating temperature and relevant supply voltage are guaranteed by design and characterization over temperature.

Note 3: Guaranteed by design and characterization. Not production tested.

Note 4: Typical values are average, peak power is 3dB higher.

Note 5: Using high output power match, see Table 2.

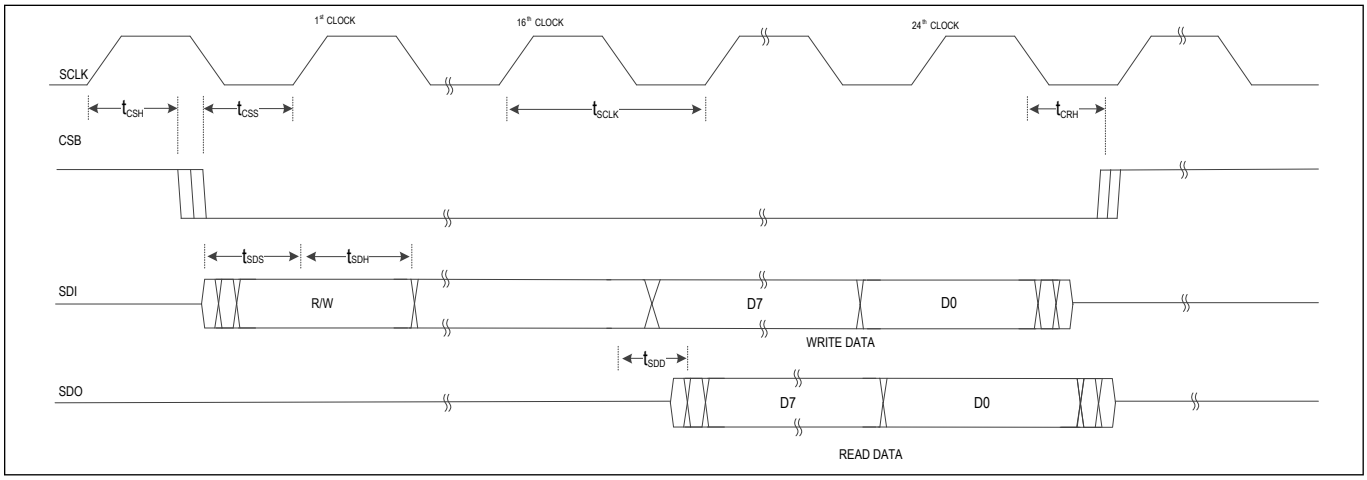
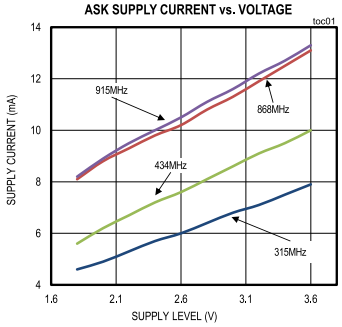


Figure 1. Serial Interface Timing Diagram

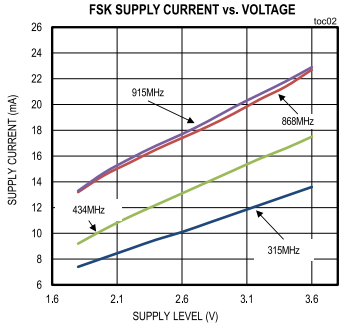
Typical Operating Characteristics

(Typical Application Circuit, RF output terminated to 50Ω. Typical values are at V_{DD} = +3V, T_A = +25°C, unless otherwise noted.)

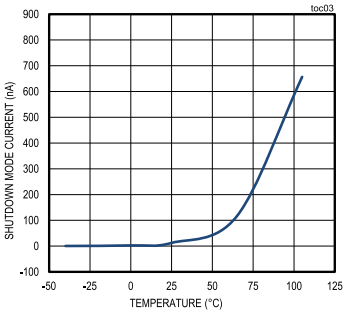
ASK SUPPLY CURRENT vs. VOLTAGE



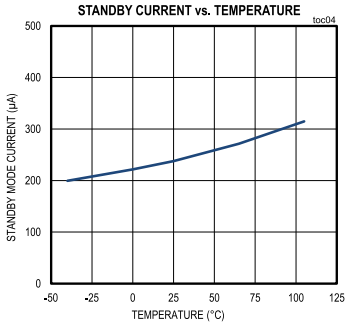
FSK SUPPLY CURRENT vs. VOLTAGE



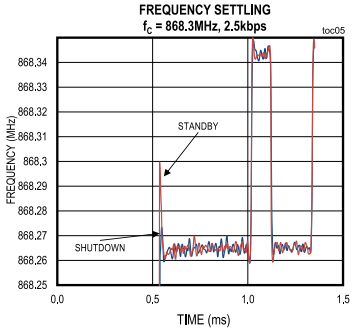
SHUTDOWN CURRENT vs. TEMPERATURE



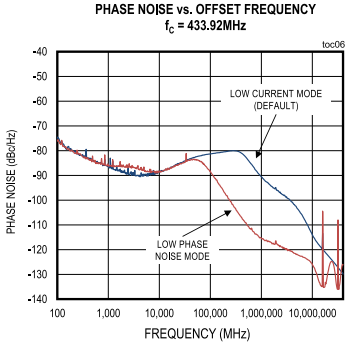
STANDBY CURRENT vs. TEMPERATURE



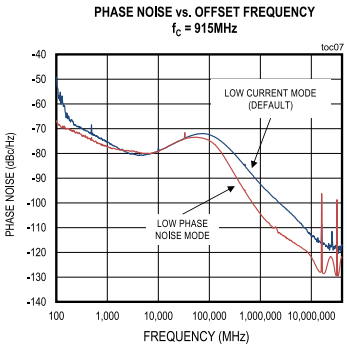
FREQUENCY SETTLING
f_C = 868.3MHz, 2.5kbps



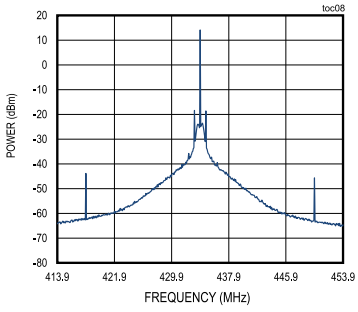
PHASE NOISE vs. OFFSET FREQUENCY
f_C = 433.92MHz



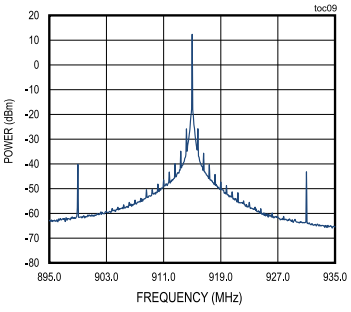
PHASE NOISE vs. OFFSET FREQUENCY
f_C = 915MHz



UNMODULATED SPECTRUM OUTPUT
f_C = 433.92MHz, RBW = 3kHz



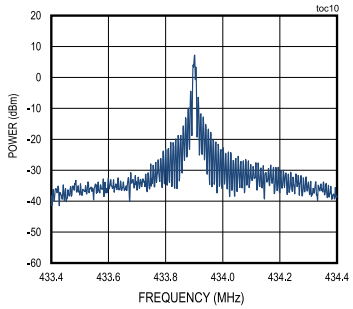
UNMODULATED SPECTRUM OUTPUT
f_C = 915MHz, RBW = 3kHz



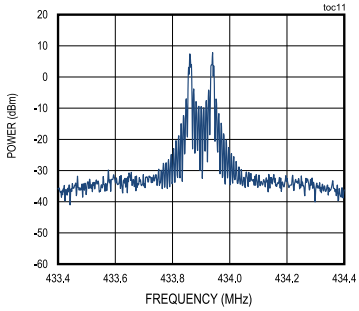
Typical Operating Characteristics (continued)

(Typical Application Circuit, RF output terminated to 50Ω. Typical values are at V_{DD} = +3V, T_A = +25°C, unless otherwise noted.)

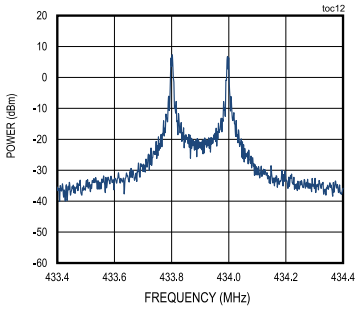
ASK MODULATED SPECTRUM OUTPUT
f_C = 433.92MHz, RBW = 3kHz



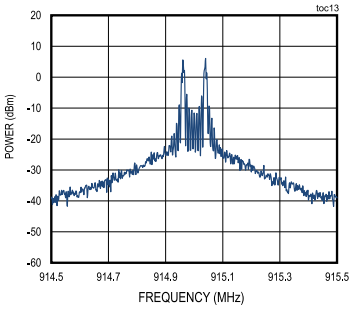
FSK ±39kHz MODULATED SPECTRUM OUTPUT
f_C = 433.92MHz, RBW = 3kHz



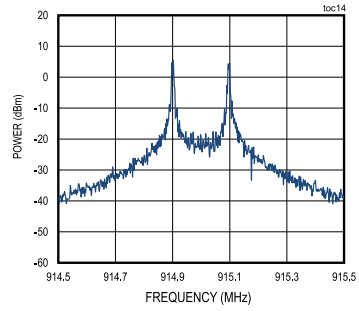
FSK ±100kHz MODULATED SPECTRUM OUTPUT
f_C = 433.92MHz, RBW = 3kHz



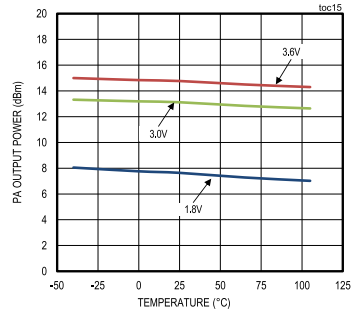
FSK ±39kHz MODULATED SPECTRUM OUTPUT
f_C = 915MHz, RBW = 3kHz



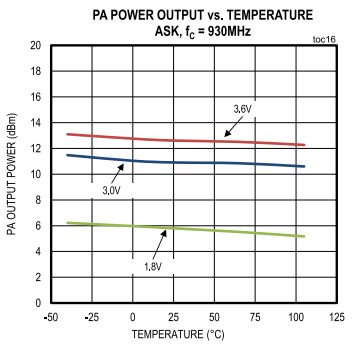
FSK ±100kHz MODULATED SPECTRUM OUTPUT
f_C = 915MHz, RBW = 3kHz



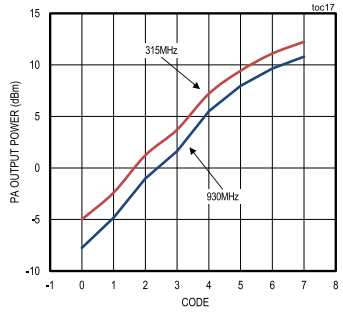
PA POWER OUTPUT vs. TEMPERATURE
FSK, f_C = 433.92MHz



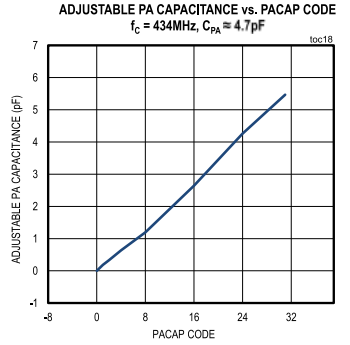
PA POWER OUTPUT vs. TEMPERATURE
ASK, f_C = 930MHz



PA OUTPUT POWER vs. PAPWR CODE



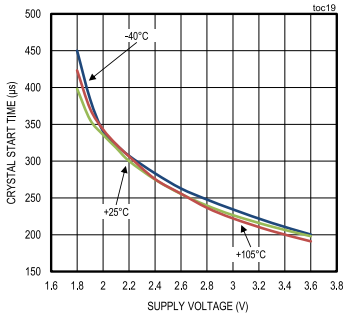
ADJUSTABLE PA CAPACITANCE vs. PACAP CODE
f_C = 434MHz, C_{PA} ≈ 4.7pF



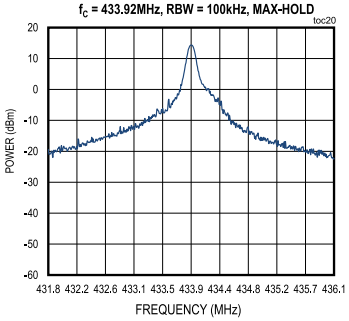
Typical Operating Characteristics (continued)

(Typical Application Circuit, RF output terminated to 50Ω. Typical values are at V_{DD} = +3V, T_A = +25°C, unless otherwise noted.)

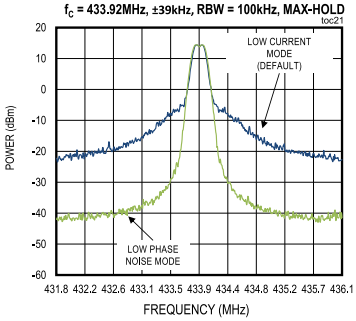
CRYSTAL STARTUP TIME vs. SUPPLY
FSK, f_C = 433.92MHz



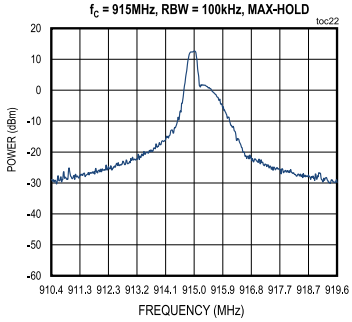
ASK SPECTRUM
LOW-CURRENT MODE
f_C = 433.92MHz, RBW = 100kHz, MAX-HOLD



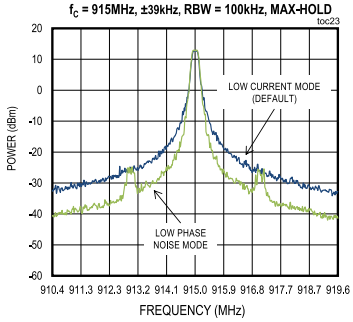
FSK SPECTRUM
LOW-CURRENT vs. LOW-PHASE NOISE MODE
f_C = 433.92MHz, ±39kHz, RBW = 100kHz, MAX-HOLD



ASK SPECTRUM
LOW-CURRENT MODE
f_C = 915MHz, RBW = 100kHz, MAX-HOLD

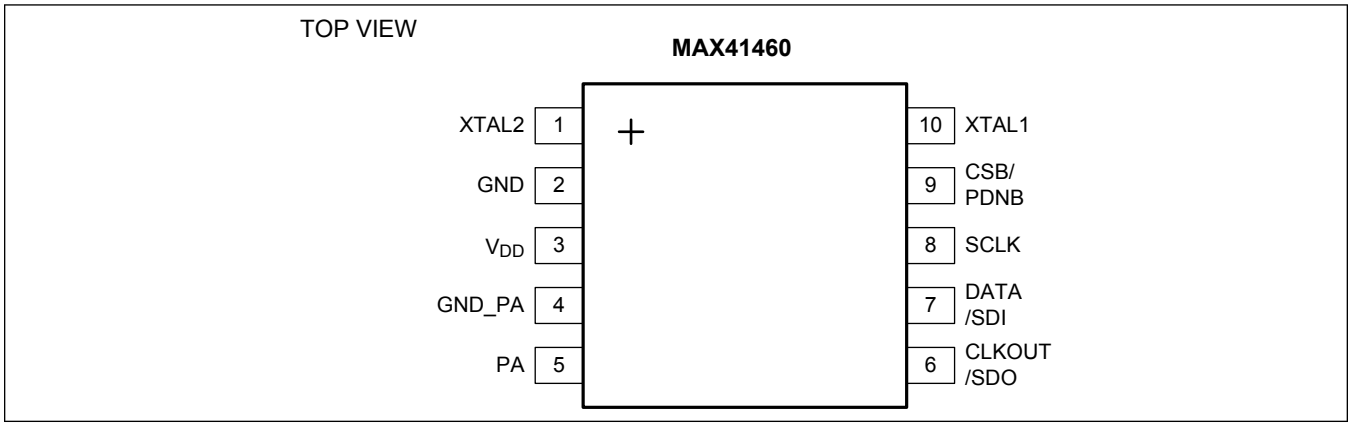


FSK SPECTRUM
LOW-CURRENT vs. LOW-PHASE NOISE MODE
f_C = 915MHz, ±39kHz, RBW = 100kHz, MAX-HOLD

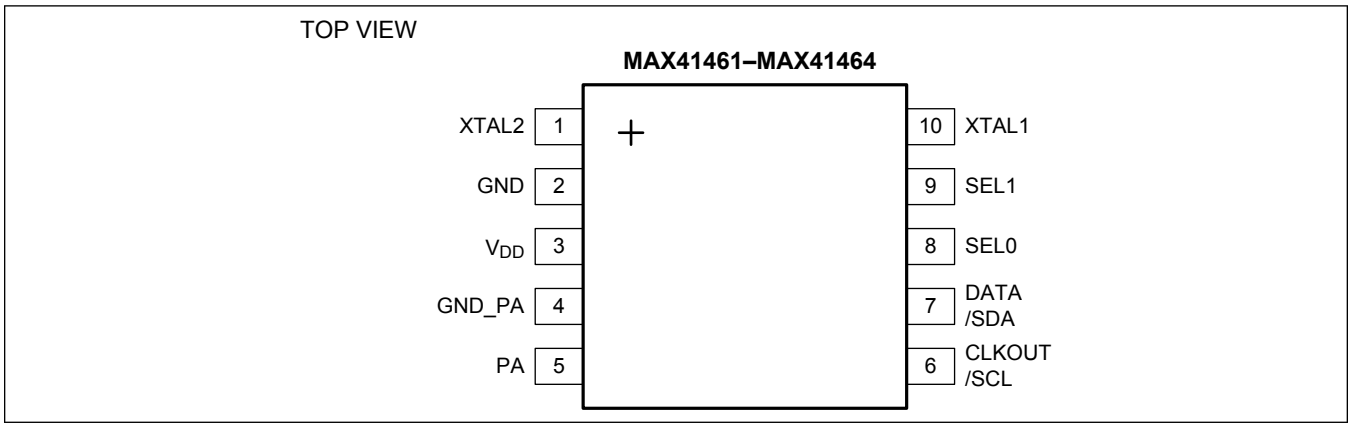


Pin Configurations

10 µMAX



10 µMAX



Pin Description

PIN		NAME	FUNCTION
MAX41460	MAX41461–MAX41464		
XTAL2	XTAL2	1	Second Crystal Input. See *Crystal Oscillator* section.
GND	GND	2	Ground. Connect to system ground.
V_{DD}	V_{DD}	3	Supply Voltage. Bypass to GND with a 100nF capacitor as close to the pin as possible.
GND_PA	GND_PA	4	Ground for the Power Amplifier (PA). Connect to system ground.
PA	PA	5	Power-Amplifier Output. The PA output requires a pullup inductor to the supply voltage, which can be part of the output-matching network to an antenna.
CLKOUT/SDO	CLKOUT/SCL	6	MAX41460: Buffered Clock Output or SPI Data Output. MAX41461–MAX41464: Buffered Clock Output. I^2C clock input for register programming when in Serial Interface Mode (SEL0 and SEL1 are unconnected or HIZ). The frequency of CLKOUT is 800kHz when not in Program mode.
DATA/SDI	DATA/SDA	7	MAX41460: Data Input. SPI bus serial data input for register programming when CSB is at logic-low. MAX41461–MAX41464: Data Input. I^2C serial data input for register programming when in Serial Interface mode (SEL0 and SEL1 are unconnected or HIZ). When not in Program mode, DATA also controls the power-up state (see the *Auto-Shutdown in Preset Mode* section in the appropriate data sheet).
SCLK	SEL0	8	MAX41460: SPI Bus Serial Clock Input. MAX41461–MAX41464: Three-state Mode Input. See *Preset Modes* section in the appropriate data sheet for details. For three-state input open, the impedance on the pin must be greater than 1MΩ.
CSB	SEL1	9	MAX41460: SPI Bus Chip Enable. Active Low. MAX41461–MAX41464: Three-state Mode Input. See *Preset Modes* section in the appropriate data sheet for details. For three-state input open, the impedance on the pin must be greater than 1MΩ.
XTAL1	XTAL1	10	First Crystal Input. See *Crystal Oscillator* section.

Detailed Description

The MAX41460 is part of the MAX4146x family of UHF sub-GHz ISM/SRD transmitters designed to transmit ASK and (G)FSK data in the 286MHz to 960MHz frequency range. The MAX4146x family is available in the following versions.

Table 1. MAX4146x Versions

VERSION	MODULATION AND INTERFACE	PRESET FREQUENCIES (MHz)
MAX41460	ASK/FSK with SPI	No presets, programmable through SPI
MAX41461	ASK (optional I²C)	315/318/319.51/345/433.42/433.92/908/915
MAX41462	ASK (optional I²C)	315/433/433.92/434/868/868.3/868.35/868.5
MAX41463	FSK (optional I²C)	315/433.42/433.92/908/908.42/908.8/915/916
MAX41464	FSK (optional I²C)	315/433.92/868.3/868.35/868.42/868.5/868.95/869.85

The MAX41460 uses an SPI programming interface. The MAX41461–MAX41464 feature an I²C interface, as well as preset modes (pin-selectable output frequencies using only one crystal frequency). No programming is required in preset modes and only a single-input data interface to an external microcontroller is needed. The MAX41460 parts are identical when put in I²C programming mode. All MAX4146x versions are fully programmable for all output frequencies, as described in the *Electrical Characteristics* table. The only frequency-dependent components required are for the the external antenna match.

The crystal-based architecture of the MAX41460 provides greater modulation depth, faster frequency settling, higher tolerance of the transmit frequency, and reduced temperature dependence. It integrates a fractional phase-locked-loop (PLL); so a single, low-cost crystal can be used to generate commonly used world-wide sub-GHz frequencies. A buffered clock-out signal make the device compatible with almost any microcontroller or code-hopping generator.

The MAX41460 provides +13dBm output power into a 50Ω load at 315MHz using an integrated high efficiency power amplifier (PA). The output load can be adjusted to increase power up to +16dBm and a PA boost mode can be enabled at frequencies above 850MHz to compensate for losses. The PA output power can also be controlled using programmable register settings. The MAX41460 feature fast oscillator wake-up upon data activity detection and has an auto-shutdown feature to extend battery life.

The MAX41460 operates at a supply voltage of +1.8V to +3.6V and is available in a 10-pin μMAX package that is specified over the -40°C to +105°C extended temperature range.

Power Amplifier

The MAX41460 PA is a high-efficiency, open-drain switching-mode amplifier. In a switching-mode amplifier, the gate of the final-stage FET is driven with a 25% duty-cycle square wave at the transmit frequency. The PA also has an internal set of capacitors that can be switched in and out to present different capacitance values at the PA output using the PACAP[4:0] register values. This allows extra flexibility for tuning the output matching network. When the matching network is tuned correctly, the output FET resonates the attached tank circuit (pullup inductor from PA to V_{DD}) with a minimum amount of power dissipated in the FET. With a proper output-matching network, the PA can drive a wide range of antenna impedances, which include a PCB trace antenna or a 50Ω antenna. The output-matching π-network suppresses the carrier harmonics and transforms the antenna impedance to an optimal impedance at the PA pin. The *Typical Application Circuit* can deliver an output power of +13dBm with a +3.0V supply. Table 2 has approximate PA load impedances for desired output powers.

The PAPWR bits in the PA1 register control the output power of the PA. This setting adjust the number of parallel drivers used, which determine the final output power (see Figure 2).

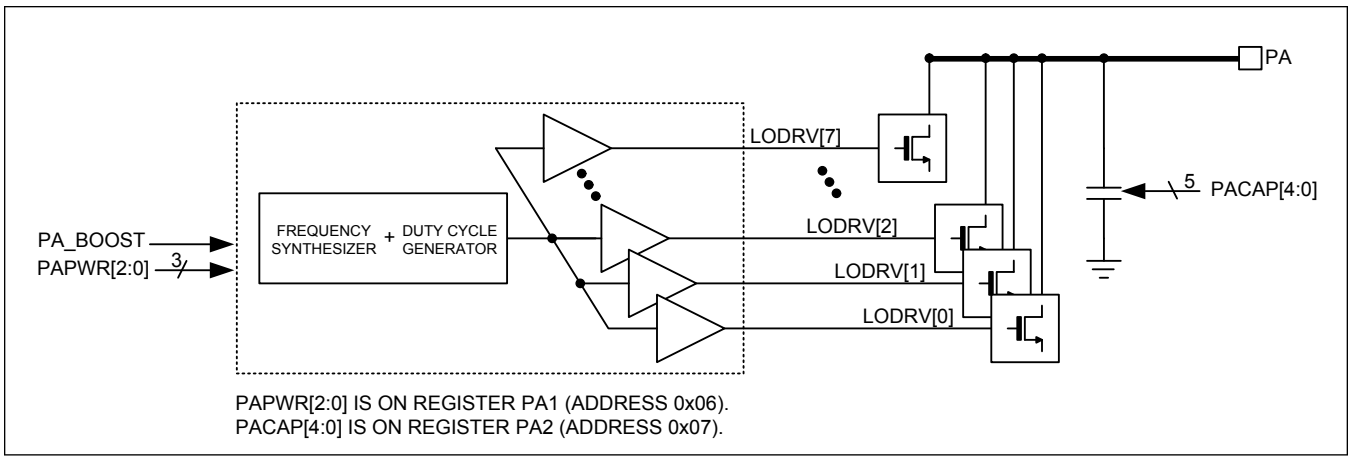


Figure 2. Power Amplifier

Boost Mode

The PA can deliver up to 16dBm of output power.

High output power can be achieved in two ways:

- Lower the load impedance for the PA by adjusting the output matching network,
- For frequencies over 850MHz, change the duty cycle of the square wave driving the PA from 25% to 50% by setting PA_BOOST = 1 in register SHDN (0x05) and adjusting the output matching network.

Note that, when using PA_BOOST = 1, the maximum supply voltage should not exceed 3V. For frequencies under 850MHz, the PA_BOOST bit should remain at 0, the output match can be adjusted to provide higher output power.

Table 2. PA Load Impedance for Desired Output Power

FREQUENCY (MHz)	OUTPUT POWER (dBm)	PA LOAD IMPEDANCE (Ω)
315	13	165
315	16 (PA_BOOST = 0)	45
434	13	180
434	16 (PA_BOOST = 0)	57
863–928	11	190
863–928	16 (PA_BOOST = 1)	34

Refer to the *MAX4146x EV Kit User's Guide* for details.

Programmable Output Capacitance

The MAX41460 has an internal set of capacitors that can be switched in and out to present different capacitor values at the PA output. The capacitors are connected from the PA output to ground. This allows changing the tuning network along with the synthesizer divide ratio each time the transmitted frequency changes, making it possible to maintain maximum transmitter power while moving rapidly from one frequency to another.

The variable capacitor is programmed through register PA2 (0x07) bits 4:0 (PACAP). The tuning capacitor has a nominal resolution of 0.18pF, from 0pF to 5.4pF. In preset mode, the variable capacitor is set to 0pF.

Transmitter Power Control

The transmitter power of the MAX41460 can be set in approximately 2.5dB steps by setting PAPWR[2:0] register bits using the SPI interface. The transmitted power (and the transmitter current) can be lowered by increasing the load impedance on the PA. Conversely, the transmitted power can be increased by lowering the load impedance.

Crystal (XTAL) Oscillator

The XTAL oscillator in the MAX41460 is designed to present a capacitance of approximately 12pF from the XTAL1 and XTAL2 pins to ground. In most cases, this corresponds to a 6pF load capacitance applied to the external crystal when typical PCB parasitics are included. It is very important to use a crystal with a load capacitance equal to the capacitance of the MAX41460 crystal oscillator plus PCB parasitics. If a crystal designed to oscillate with a different load capacitance is used, the crystal is pulled away from its stated operating frequency introducing an error in the reference frequency. The crystal's natural frequency is typically below its specified frequency. However, when loaded with the specified load capacitance, the crystal is pulled and oscillates at its specified frequency. This pulling is already accounted for in the specification of the load capacitance. Accounting for typical board parasitics, a 16MHz, 12pF crystal is recommended. Please note that adding discrete capacitance on the crystal also increases the startup time and adding too much capacitance could prevent oscillation altogether.

Additional pulling can be calculated if the electrical parameters of the crystal are known. The frequency pulling is given by:

$$f_P = \frac{C_M}{2}\left(\frac{1}{C_{CASE}+C_{LOAD}} - \frac{1}{C_{CASE}+C_{SPEC}}\right) \times 10^6$$

where:

f_P is the amount the crystal frequency pulled in ppm.

C_M is the motional capacitance of the crystal.

C_{CASE} is the case capacitance.

C_{SPEC} is the specified load capacitance.

C_{LOAD} is the load capacitance.

When the crystal is loaded as specified (i.e., $C_{LOAD} = C_{SPEC}$), the frequency pulling equals zero. For additional details on crystal pulling and load capacitance affects, refer to *Maxim Tutorial 5422 – Crystal Calculations for ISM RF Products*.

Turn-On Time of Crystal Oscillator

The turn-on time of crystal oscillator (XO), t_{XO}, is defined as elapsed time from the instant of turning on XO circuit to the first rising edge of XO divider clock output. The external microcontroller turns on the XO by,

1. Sending a wakeup pulse for MAX41461–MAX41464 in the preset mode, or
2. Writing to device I^2C address for MAX41461–MAX41464 in the I^2C mode, or
3. Pulling CSB pin low on the MAX41460.

Crystal Divider

The recommended crystal frequencies are 13.0MHz, 16.0MHz, and 19.2MHz. An internal clock of 3.2MHz±0.1MHz frequency is required. To maintain the internal 3.2MHz time base, XOCLKDIV[1:0] (register CFG1, 0x00, bit 4) must be programmed, based on the crystal frequency, as shown in Table 3.

Table 3. Required Crystal Divider Programming

CRYSTAL FREQUENCY (MHz)	Crystal Divider Ratio	XOCLKDIV[1:0]
13.0	4	00
16.0	5	01
19.2	6	10

Phase-Locked Loop (PLL)

The MAX41460 utilizes a fully integrated fractional-N PLL for its frequency synthesizer. All PLL components, including loop filter, are included on-chip. The synthesizer has a 16-bit fractional-N topology with a divide ratio that can be set from 11 to 72, allowing the transmit frequency to be adjusted in increments of $f_{XTAL}/65536$. The fractional-N architecture also allows exact FSK frequency deviations to be programmed. FSK deviations as low as ±1kHz and as high as ±100kHz can be set by programming the appropriate registers.

The internal VCO can be tuned continuously from 286MHz to 960MHz in normal mode, and from 286MHz–320MHz, 425MHz–480MHz, and 860MHz–960MHz in low phase noise mode.

Frequency Programming

The desired frequency can be programmed by setting bits FREQ in registers PLL3, PLL4, and PLL5 (0x0B, 0x0C, 0x0D). To calculate the FREQ bits, use:

$$FREQ[23:0] = ROUND\left(\frac{65536 \times f_C}{f_{XTAL}}\right)$$

See Table 4 to program the LODIV bits in register PLL1 (0x08) when choosing a LO frequency. It is recommended to leave bits CPVAL and CPLIN at factory defaults. If integer-N synthesis is desired, set bit FRACMODE = 0 in register PLL1.

Table 4. LODIV Setting

FREQUENCY RANGE (MHz)	LODIV SETTING
286–960, Low Current Mode	0x0
286–320, Low Phase Noise Mode	0x3
425–480, Low Phase Noise Mode	0x2
860–960, Low Phase Noise Mode	0x1

Fractional-N Spurs

The 16-bit fractional-N, delta-sigma modulator can produce spurious that can show up on the power amplifier output spectrum. If slight frequency offsets can be tolerated, set the LSB of FREQ (register PLL5, bit 0) to logic-high. Using an odd value (logic 1 at bit 0) of the 24-bit FREQ register will produce lower PLL spurious compared to even values (logic 0 at bit 0).

Turn-On Time of PLL

The turn-on time of PLL, t_{PLL}, is defined as the elapsed time from the instant when the XO output is available to the instant when PLL frequency acquisition is complete.

Serial Peripheral Interface (SPI)

The MAX41460 utilizes a 3-wire SPI protocol for programming its registers, configuring and controlling the operation of the whole transmitter. The register contents may be read back through the CLKOUT/SDO pin. The digital I/Os in Table 5 control the operation of the SPI.

Table 5. SPI Controls

PIN	DESCRIPTION
SCLK	SPI Clock
DATA/SDI	SPI Data Input
CSB	SPI Chip-Select Bar
CLKOUT/SDO	SPI Data Out

To help ensure the MAX41460 powers on in its low power state, an internal pullup resistor of approximately 200kΩ is connected to pin CSB. For example, if the microcontroller GPIO is high-impedance at power on, CSB will follow V_{DD} to make sure the MAX41460 does not enter the PLL ready state.

Figure 3 shows the general SPI Write transaction. Figure 4 shows the format of a 4-wire SPI Read transaction. In order to change CLKOUT to SDO, the user must set the FOURWIRE bit (register CFG6, address 0x0A, bit 0) to the value of 1.

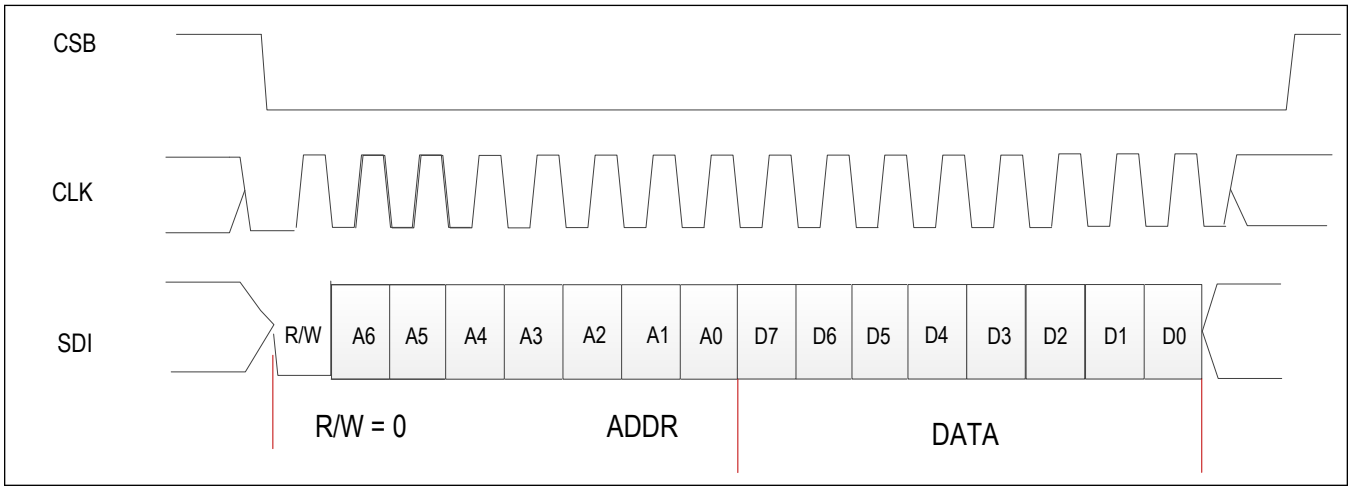


Figure 3. 3-Wire SPI Write

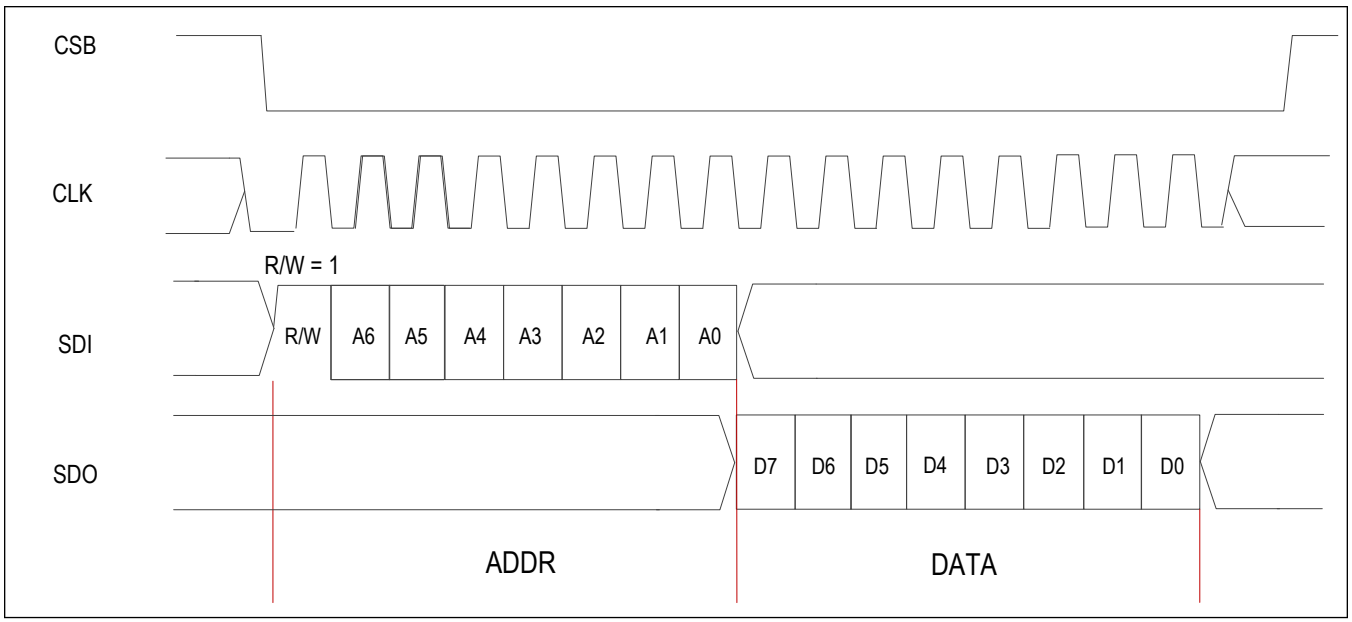


Figure 4. 4-Wire SPI Read

Asynchronous and Synchronous Transmission

The MAX41460 is configured to synchronous or asynchronous transmission mode when SYNC (register CFG1, 0x00, bit 1) is set or cleared.

In synchronous transmission mode, the MAX41460 outputs a baud-rate clock with 50% duty cycle on the CLKOUT/SDO pin. A microcontroller can use the rising edge of CLKOUT as the interrupt source for DATA generation from an interrupt service routine. The MAX41460 resamples input DATA at the falling edge of baud-rate clock to minimize jitter. The baud rate is programmable by BCLK_PREDIV[7:0] (register CFG3, 0x02, bits 7:0) and BCLK_POSTDIV[2:0] (register CFG2,, 0x01, bits 2:0) as the following expression:

$$BaudRate = \frac{f_{CLK}}{2 \times (1 + BCLK\_PREDIV) \times 2^{BCLK\_POSTDIV}}$$

where f_{CLK} is the crystal-divider output clock rate (nominally, 3.2 MHz). Valid values of BCLK_PREDIV are from 3 to 255. Valid values of BCLK_POSTDIV are from 1 to 5.

In asynchronous transmission mode (also called baud-rate transparent mode), the baud rate of data transmission is fully controlled by the microcontroller, and the DATA input is transferred to internal 3.2MHz clock domain by D-flip-flop synchronizers. The MAX41460 still provides programmable CLKOUT in asynchronous transmission mode, but the microcontroller does not have to use the CLKOUT signal.

Buffered Clock Output

The MAX41460 provides CLKOUT on pin 6 of the chip in the three-wire SPI mode. The CLKOUT frequency of MAX41460 is programmable (see the *Asynchronous and Synchronous Transmission* section).

There is no CLKOUT in the four-wire SPI mode, where pin 6 is reused as the SDO line. In four-wire SPI mode, pin 6 is disconnected (high-impedance output) when CSB is logic-high.

CLKOUT_DELAY[1:0] (register CFG2, address 0x01, bits 7:6) are not to be used in the MAX41460.

State Diagrams

The MAX41460 has four major operating states: shutdown, standby, programming, and transmitter-enabled. These states describe the power-on/power-off status of the transmitter's three primary internal circuit blocks: the crystal oscillator (XO), the PLL synthesizer, and the power amplifier (PA).

Table 6. State Descriptions

STATE	XO	PLL	PA
Shutdown	Off	Off	Off
Standby	On	Off	Off
Programming	On	On	Off
Transmitter-Enabled	On	On	On with Ramp-up

Configuration register values are retained in all states unless changed by programming, or if the device is powered off or undergoes a SOFTRESET.

Right after power-on, the MAX41460 enters the shutdown state. A falling edge on CSB (pin 9) initiates the warm-up of XO and PLL.

The device can support two types of SPI transactions: register access only, and register access followed by data transmission. The event trigger of data transmission is a rising edge on SPI_TXEN, which is a special register bit with two aliases SPI_TXEN1 (register CFG6, 0x0A, bit 1) and SPI_TXEN2 (register CFG7, 0x10, bit 1). A rising edge on SPI_TXEN can be generated by clearing SPI_TXEN1 and setting SPI_TXEN2 in a single SPI transaction.

After a rising edge of CSB, which indicates end-of-transmission, the MAX41460 refers to PWDN_MODE[1:0] (register CFG4, 0x03, bits 1:0) to enter the shutdown, standby, or programming state. The shutdown and standby states can only be entered after the transmitter-enabled state.

SPI_TXEN is automatically cleared in two cases: 1) wake-up from shutdown, 2) return to programming state from the transmitter-enabled state. In those two cases, a rising edge on SPI_TXEN can be generated by setting SPI_TXEN2 in CFG7, without explicit clearing of SPI_TXEN1.

In both shutdown and standby states, programming through the SPI interface is not allowed. The MAX41460 will leave the shutdown or standby state once a falling CSB is detected.

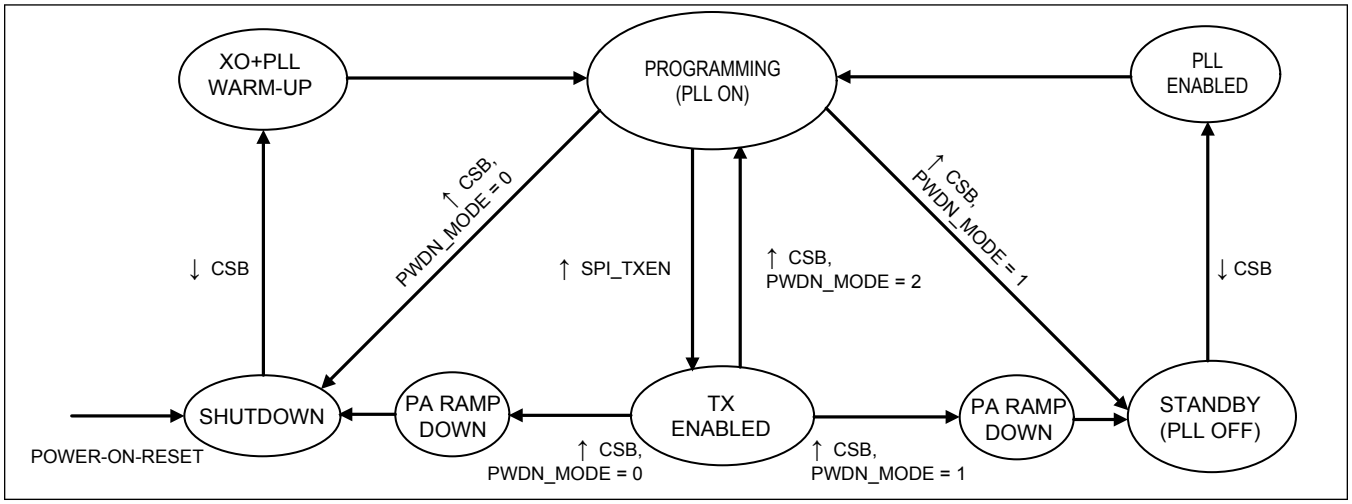


Figure 5. Simplified State Diagram of the MAX41460

Initial Programming

After turning on power supply (or after a soft reset), an SPI transaction that burst-writes 17 consecutive registers from address 0x00 to 0x10 is required to initialize the PLL frequency synthesizer.

The initial programming must clear MODMODE (register CFG1, address 0x00, bit 0), clear SPI_TXEN1 (register CFG6, address 0x0A, bit 1), configure FREQ[23:0] (register PLL3, PLL4 and PLL5) to desired frequency, and set SPI_TXEN2 (register CFG7, address 0x10, bit1).

With this process there are two timing requirements:

1) From transaction start to the SPI_TXEN bit write, the time lag must be longer than the XO turn-on time (t_{XO}).

2) From SPI_TXEN bit write to transaction end, the time lag must be longer than the PLL turn-on time (t_{PLL})

It takes 144 SCLK cycles to burst-write 17 consecutive registers. To meet requirement 1), the master device can lower the SCLK frequency or delay the start of register programming after chip select.

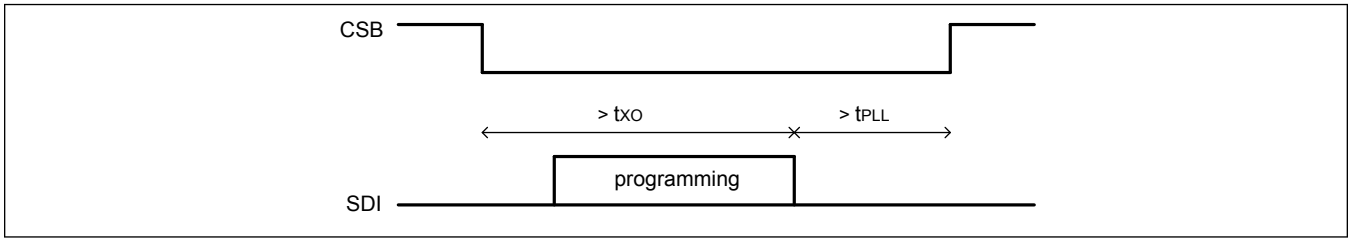


Figure 6. Initial Programming of MAX41460 by a Single SPI Transaction

After initial programming, the MAX41460 device will enter the shutdown, standby, or programming state according to the setting of PWDN_MODE[1:0] (register CFG4, address 0x03, bit[1:0]).

Startup

This section assumes that initial programming is done after power-on (or soft reset). There is no RF emission at the PA output during initial programming. Configuration register values are retained in all states, unless changed by programming, if the device is powered off, or undergoes a SOFTRESET.

Case 1: Using Two SPI Transactions, for Configuration then Transmission, from Shutdown State

The startup of the MAX41460 from the shutdown state can use two SPI transactions: one for configuration update and the other for data transmission. Note that FSK modulation can only be enabled through a configuration update because the initial programming must clear MODMODE (register CFG0, address 0x00, bit 0).

In the first SPI transaction, the master device burst-writes consecutive registers that are a portion or all of the 16 registers from address 0x00 to 0x0F. Those consecutive registers may or may not include CFG6. If CFG6 is included, the SPI_TXEN1 bit should be cleared. Otherwise, SPI_TXEN1 is automatically cleared in the wake-up from shutdown.

In the second SPI transaction, the master device can set SPI_TXEN2 (register CFG7, address 0x10, bit 1), wait for at least t_{TX} time, and then start data transmission. For applications without frequency-hopping, t_{TX} is 10µs.

The event trigger for wake-up is the falling edge of CSB of the first transaction. The event trigger for data transmission is the rising edge of SPI_TXEN that has two aliases of SPI_TXEN1 and SPI_TXEN2. The time lag between those two triggers must be longer than t_{XO} + t_{PLL}. To meet this requirement, the master device can adjust the waiting time between two SPI transactions.

The MAX41460 provides a CLKOUT signal with programmable frequency. The time lag (t_{CKO}) from transmission trigger to the first edge of CLKOUT does not vary with CLKOUT frequency.

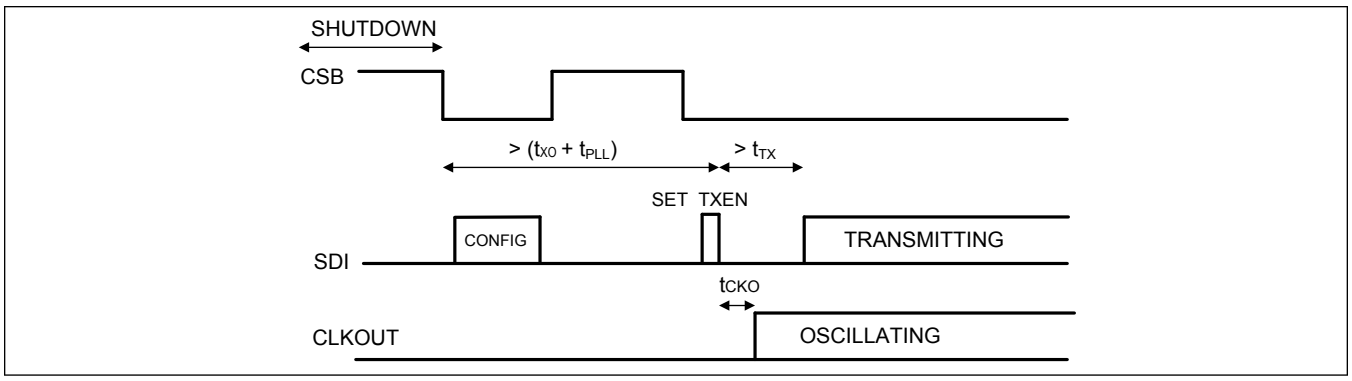


Figure 7. Using Two SPI Transactions to Start Data Transmission from the Shutdown State.

Case 2: Using a Single SPI Transaction for Configuration and Transmission, from Shutdown State

The startup of the MAX41460 from the shutdown state may also use a single SPI transaction with configuration update followed by data transmission. The master device can burst-write a number of consecutive registers, where the last register should be CFG7 to set SPI_TXEN2. The consecutive registers may or may not include CFG6. If CFG6 is included, SPI_TXEN1 should be cleared.

The event trigger for wake-up is the falling edge of CSB. The event trigger for data transmission is the rising edge of SPI_TXEN that has two aliases of SPI_TXEN1 and SPI_TXEN2. The time lag between those two triggers must be longer than $t_{XO} + t_{PLL}$. To meet this requirement, the master device can extend the SCLK period used during register programming or insert a delay between chip select and programming start. After setting SPI_TXEN2, the master device can wait for at least t_{TX} time and start data transmission.

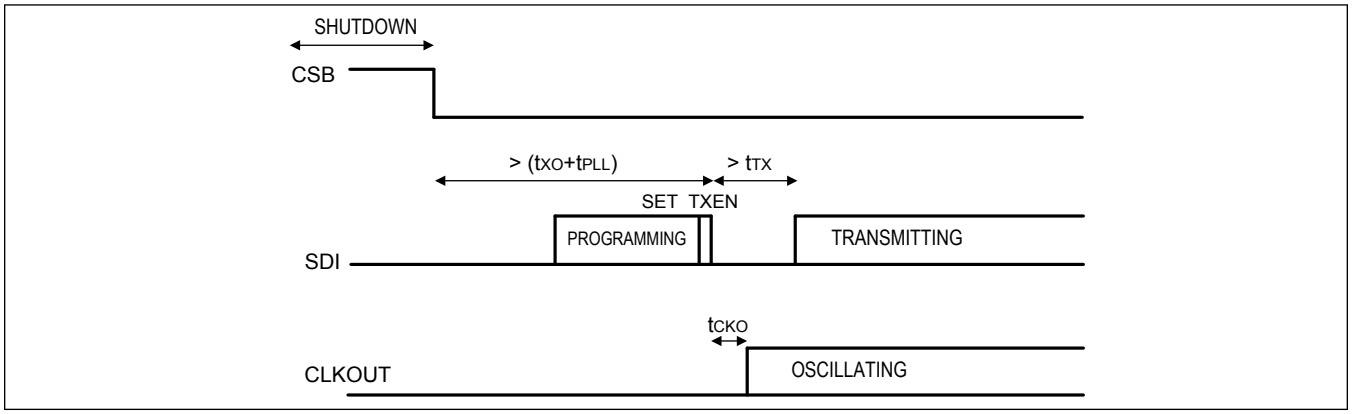


Figure 8. Using a Single SPI Transaction to Start Data Transmission from the Shutdown State.

Case 3: Using a Single SPI Transaction for Configuration and Transmission, from Standby State

The startup of the MAX41460 from the standby state can use a single SPI transaction with configuration update followed by data transmission. In the programming for configuration update, the master device should burst-write at least 7 consecutive registers, where CFG7 is the last register to write. The first register to write can be CFG6 or any register preceding CFG6. The programming should clear SPI_TXEN1 and set SPI_TXEN2.

The event trigger for wake-up is the falling edge of CSB. The event trigger for data transmission is the rising edge of

SPI_TXEN that has two aliases of SPI_TXEN1 and SPI_TXEN2. The time lag between those two triggers must be longer than t_{PLL} for startup from standby. To meet this requirement, the master device can extend the SCLK period used during register programming or insert a delay between chip select and programming start. After setting SPI_TXEN2, the master device can wait for at least t_{TX} time and start data transmission.

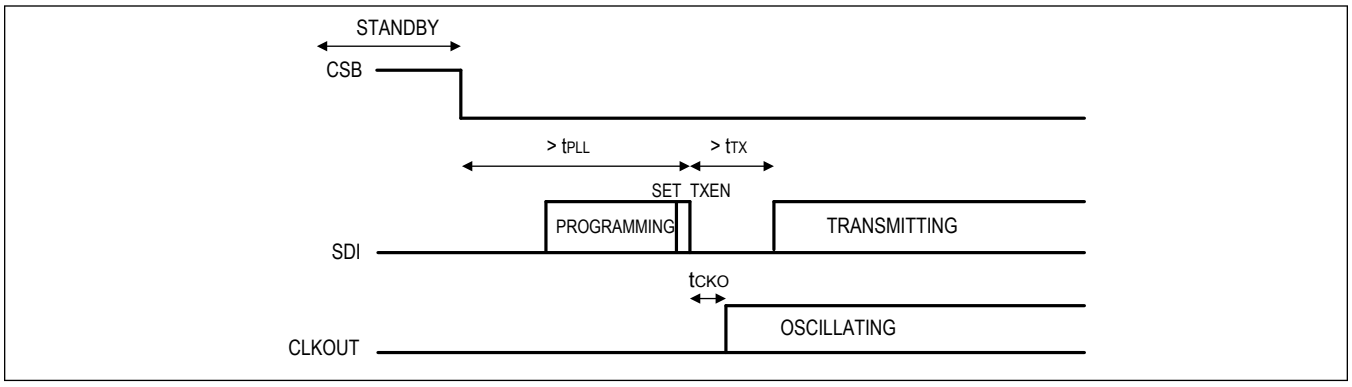


Figure 9. Using a Single SPI Transaction to Start Data Transmission from the Standby Mode.

Case 4: Using a Single SPI Transaction for Configuration and Transmission, from Programming State

The MAX41460 device can transmit a data packet each time in the transmitter-enabled state. After data transmission, the device refers to the setting of PWDN_MODE[1:0] to enter the shutdown, standby, or programming state. If the next data packet requires very fast startup, PWDN_MODE[1:0] can be configured to 0x10 so that the MAX41460 device returns to the programming state when the RF transmission is complete.

Then, the master device can use a single SPI transaction to start data transmission. There is no restrictions arising from t_{XO} and t_{PLL}. Without configuration update, the master device can write only one register CFG7 to set SPI_TXEN2. If configuration update is required, the master device should burst-write consecutive registers, where CFG7 is the last register to write. Those consecutive registers may or may not include CFG6. If CFG6 is included, the SPI_TXEN1 bit should be cleared. Otherwise, SPI_TXEN1 is automatically cleared.

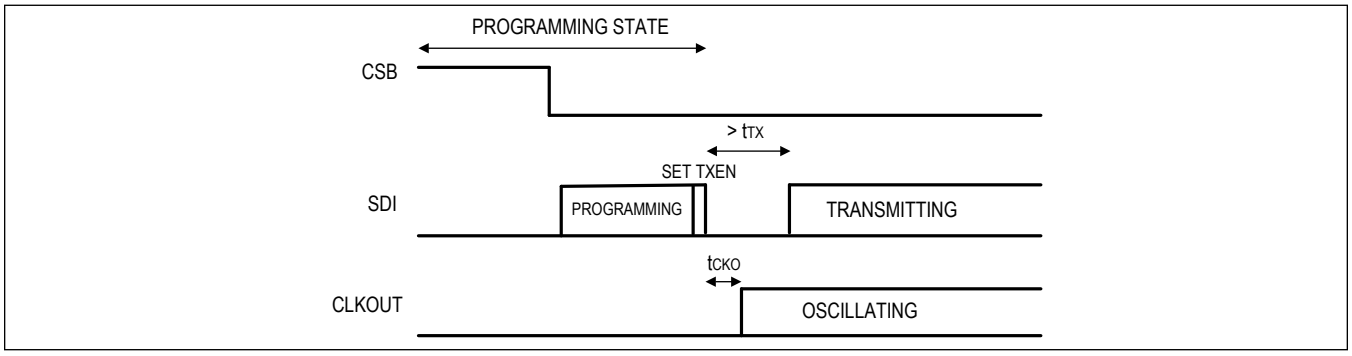


Figure 10. Using a Single SPI Transaction to Start Data Transmission from the Programming State.

Frequency-Hopping

The frequency synthesizer is initialized at a frequency in a selected ISM band by Initial Programming. After that, for the purpose of frequency dithering or frequency hopping, the FREQ[23:0] registers can be updated to a new frequency in the same selected band for each data packet to be transmitted.

Because programming is not allowed in the transmitted-enabled state (see the *State Diagrams* section), frequency configuration cannot be changed when PA is enabled. See the *Startup* section for details on how to program the device for data transmission.

After transmitting a data packet, the MAX41460 device enters the shutdown, standby, or programming state according to the setting of PWDN_MODE[1:0] register. The three options have different startup time for transmitting the the next data packet. The startup time from shutdown is at least (t_{XO} + t_{PLL} + t_{TX}), where t_{XO} is the turn-on time of crystal oscillator, t_{PLL} is the turn-on time of PLL, t_{TX} is the turn-on time of transmitter. The startup time from standby is at least (t_{PLL} + t_{TX}).

The t_{TX} time is 10µs if frequency hops are no more than 1MHz per hop. If the frequency hop is as high as 26MHz, as in the case of 902MHz~928MHz band, then the t_{TX} time is 20µs. Refer to the *Electrical Characteristics* table for typical values of t_{XO} and t_{PLL}.

Register Map

Register Map

ADDRESS	NAME	MSB							LSB
TX									
0x00	CFG1[7:0]	XOCLKDELAY[1:0]		XOCLKDIV[1:0]		–	FSKSHAPE	SYNC	MODMODE
0x01	CFG2[7:0]	CLKOUT_DELAY[1:0]		–	–	–	RESERVED[2:0]		
0x02	CFG3[7:0]	RESERVED[7:0]							
0x03	CFG4[7:0]	–	–	–	–	–	–	PWDN_MODE[1:0]	
0x04	CFG5[7:0]	–	–	TSTEP[5:0]					
0x05	SHDN[7:0]	–	–	–	–	–	RESERVED	RESERVED	PA_BOOST
0x06	PA1[7:0]	RESERVED[2:0]			–	–	PAPWR[2:0]		
0x07	PA2[7:0]	–	–	–	PACAP[4:0]				
0x08	PLL1[7:0]	CPLIN[1:0]		FRACMODE	RESERVED[1:0]		LODIV[1:0]		LOMODE
0x09	PLL2[7:0]	RESERVED	RESERVED	–	–	–	–	CPVAL[1:0]	
0x0A	CFG6[7:0]	–	–	–	–	–	RESERVED	SPI_TXEN1	FOURWIRE1
0x0B	PLL3[7:0]	FREQ[23:16]							
0x0C	PLL4[7:0]	FREQ[15:8]							
0x0D	PLL5[7:0]	FREQ[7:0]							
0x0E	PLL6[7:0]	–	DELTAF[6:0]						
0x0F	PLL7[7:0]	–	–	–	–	DELTAF_SHAPE[3:0]			
0x10	CFG7[7:0]	–	–	–	–	–	RESERVED	SPI_TXEN2	FOURWIRE2
0x17	CFG8[7:0]	–	–	–	–	–	–	–	SOFTRESET
0x18	CFG9[7:0]	RESERVED[4:0]					RESERVED	RESERVED	RESERVED
0x19	ADDL1[7:0]	RESERVED[1:0]		RESERVED[1:0]		RESERVED[1:0]		RESERVED[1:0]	
0x1A	ADDL2[7:0]	RESERVED	RESERVED[6:0]						

Register Details

CFG1 (0x00)

BIT	7	6	5	4	3	2	1	0
Field	XOCLKDELAY[1:0]		XOCLKDIV[1:0]		–	FSKSHAPE	SYNC	MODMODE
Reset	0x2		0x1		–	0b0	0b0	0b0
Access Type	Write, Read		Write, Read		–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
XOCLKDELAY	7:6	Start delay before enabling XO clock to digital block	0x0: No delay. XO clock is immediately enabled to rest of digital block 0x1: XO clock is enabled after 16 cycles to rest of digital block 0x2: XO clock is enabled after 32 cycles to rest of digital block 0x3: XO clock is enabled after 64 cycles to rest of digital block
XOCLKDIV	5:4	XO clock division ratio for digital block	0x0: Divide XO clock by 4 for digital clock 0x1: Divide XO clock by 5 for digital clock. High time is 2 cycles, low time is 3 cycles 0x2: Divide XO clock by 6 for digital clock 0x3: Divide XO clock by 7 for digital clock. High time is 3 cycles, and low time is 4 cycles
FSKSHAPE	2	Sets the state of FSK Gaussain Shaping	0x0: FSK Shaping disabled 0x1: FSK Shaping enabled
SYNC	1	Controls if clock output acts as an input. When an input, it will sample the DATA pin.	0x0 0x1
MODMODE	0	Configures modulator mode	0x0: ASK Mode 0x1: FSK Mode

CFG2 (0x01)

BIT	7	6	5	4	3	2	1	0
Field	CLKOUT_DELAY[1:0]		–	–	–	RESERVED[2:0]		
Reset	0x2		–	–	–	0x1		
Access Type	Write, Read		–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
CLKOUT_DELAY	7:6	Selects the delay when CLKOUT starts toggling upon exiting SHUTDOWN mode, in divided XO clock cycles	0x0: CLKOUT will start toggling after 64 cycles whenever moving into normal mode from shutdown mode 0x1: CLKOUT will start toggling after 128 cycles whenever moving into normal mode from shutdown mode 0x2: CLKOUT will start toggling after 256 cycles whenever moving into normal mode from shutdown mode

BITFIELD	BITS	DESCRIPTION	DECODE
			0x3: CLKOUT will start toggling after 512 cycles whenever moving into normal mode from shutdown mode
RESERVED	2:0	Write to 000 binary.	

CFG3 (0x02)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[7:0]							
Reset	0x3							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:0	Write to 00 hex.	

CFG4 (0x03)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	PWDN_MODE[1:0]	
Reset	–	–	–	–	–	–	0x0	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
PWDN_MODE	1:0	Power Down Mode Select	0x0: SHUTDOWN low power state is enabled. While entering low power state, XO, PLL, and PA are shutdown. 0x1: STANDBY low power state is enabled. While entering low power state, XO is enabled. PLL and PA are shutdown 0x2: FAST WAKEUP low power state is enabled. While entering low power state, XO and PLL are enabled. PA is shutdown. 0x3: Will revert to 0x2

CFG5 (0x04)

BIT	7	6	5	4	3	2	1	0
Field	–	–	TSTEP[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
TSTEP	5:0	Controls GFSK shaping. See Digital FSK Modulation section.

SHDN (0x05)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RESERVED	RESERVED	PA_BOOST
Reset	–	–	–	–	–	0x1	0x0	0x0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	2	Write to 1 binary.	1
RESERVED	1	Write to 0 binary.	0
PA_BOOST	0	Enables a boost in PA output power for frequencies above 850MHz. This requires a different PA match compared to normal operation.	0x0: PA Output power in normal operation. 0x1: PA Output power in boost mode for more output power.

PA1 (0x06)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			–	–	PAPWR[2:0]		
Reset	0x4			–	–	0x0		
Access Type	Write, Read			–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:5	Write to 100 binary.	100
PAPWR	2:0	Controls the PA output power by enabling parallel drivers.	0x0: Minimum, 1 driver 0x1: 2 Drivers 0x2: 3 Drivers 0x3: 4 Drivers 0x4: 5 Drivers 0x5: 6 Drivers 0x6: 7 Drivers 0x7: 8 Drivers

PA2 (0x07)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	PACAP[4:0]				
Reset	–	–	–	0x0				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PACAP	4:0	Controls shunt capacitance on PA output in fF.	0x00: 0 0x01: 175 0x02: 350 0x03: 525 0x04: 700 0x05: 875 0x06: 1050 0x07: 1225

BITFIELD	BITS	DESCRIPTION	DECODE
			0x08: 1400 0x09: 1575 0x0A: 1750 0x0B: 1925 0x0C: 2100 0x0D: 2275 0x0E: 2450 0x0F: 2625 0x10: 2800 0x11: 2975 0x12: 3150 0x13: 3325 0x14: 3500 0x15: 3675 0x16: 3850 0x17: 4025 0x18: 4200 0x19: 4375 0x1A: 4550 0x1B: 4725 0x1C: 4900 0x1D: 5075 0x1E: 5250 0x1F: 5425

PLL1 (0x08)

BIT	7	6	5	4	3	2	1	0
Field	CPLIN[1:0]		FRACMODE	RESERVED[1:0]		LODIV[1:0]		LOMODE
Reset	0x1		0x1	0x00		0x0		0b0
Access Type	Write, Read		Write, Read	Write, Read		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CPLIN	7:6	Sets the level of charge pump offset current for fractional N mode to improve close in phase noise. Set to 'DISABLED' for integer N mode.	0x0: No extra current 0x1: 5% of charge pump current 0x2: 10% of charge pump current 0x3: 15% of charge pump current
FRACMODE	5	Sets PLL between fractional-N and integer-N mode.	0x0: Integer N Mode 0x1: Fractional N Mode
RESERVED	4:3	Write to 00 binary.	00
LODIV	2:1		0x0: Disabled 0x1: LC VCO divided by 4 0x2: LC VCO divided by 8 0x3: LC VCO divided by 12
LOMODE	0	Sets LO generation. For lower power, choose LOWCURRENT. For higher performance, choose LOWNOISE.	0x0: Ring Oscillator Mode 0x1: LC VCO Mode

PLL2 (0x09)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	RESERVED	–	–	–	–	CPVAL[1:0]	
Reset	0x0	0b0	–	–	–	–	0x0	
Access Type	Write, Read	Write, Read	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7	Write to 0 binary.	0
RESERVED	6	Write to 0 binary.	0
CPVAL	1:0	Sets Charge Pump Current	0x0: 5µA 0x1: 10µA 0x2: 15µA 0x3: 20µA

CFG6 (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RESERVED	SPI_TXEN1	FOURWIRE1
Reset	–	–	–	–	–	0x0	0x0	0x0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	2	Write to 0 binary.	
SPI_TXEN1	1	Transmission enable.	0x0: Transmission disabled. 0x1: Transmission enabled.
FOURWIRE1	0	Four wire readback on CLKOUT pin mode.	0x0: Four wire readback disabled. 0x1: Four wire readback enabled.

PLL3 (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	FREQ[23:16]							
Reset	0x13							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FREQ	7:0	FREQ value to PLL. LO frequency= FREQ<23:0>/2^16*fXTAL

PLL4 (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	FREQ[15:8]							
Reset	0xB0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FREQ	7:0	FREQ value to PLL

PLL5 (0x0D)

BIT	7	6	5	4	3	2	1	0
Field	FREQ[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FREQ	7:0	FREQ value to PLL

PLL6 (0x0E)

BIT	7	6	5	4	3	2	1	0
Field	–	DELTAF[6:0]						
Reset	–	0x28						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
DELTAF	6:0	For FSK mode, MODMODE=1 and FSKSHAPE=0, sets the frequency deviation from the space frequency for the mark frequency. fDELTA = DELTAF[6:0] * fXTAL/ 8192

PLL7 (0x0F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DELTAF_SHAPE[3:0]			
Reset	–	–	–	–	0x4			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
DELTAF_SHAPE	3:0	For FSK mode, MODMODE = 1 and FSKSHAPE = 1, sets the frequency deviation from the space frequency for the mark frequency. fDELTA = DELTAF_SHAPE[3:0] * fXTAL / 81920

CFG7 (0x10)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RESERVED	SPI_TXEN2	FOURWIRE2
Reset	–	–	–	–	–	0x0	0x0	0x0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	2	Write to 0 binary.	

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_TXEN2	1	0x0: Transmission disabled. 0x1: Transmission enabled.	
FOURWIRE2	0	Four wire readback on CLKOUT pin mode. Aliased address for FOURWIRE1	0x0: Four wire readback disabled. 0x1: Four wire readback enabled.

CFG8 (0x17)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	SOFTRESET
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SOFTRESET	0	Places DUT into software reset.	0x0: Deassert the reset 0x1: Resets the entire digital, until this bit is set to 0

CFG9 (0x18)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[4:0]					RESERVED	RESERVED	RESERVED
Reset	0x0					0x0	0x0	0x0
Access Type	Write, Read					Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:3	Write to 0_0000 binary.	00000
RESERVED	2	Write to 0 binary.	0
RESERVED	1	Write to 0 binary.	0
RESERVED	0	Write to 0 binary.	0

ADDL1 (0x19)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		RESERVED[1:0]		RESERVED[1:0]		RESERVED[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Write to 00 binary.	00
RESERVED	5:4	Write to 00 binary.	00
RESERVED	3:2	Write to 00 binary.	00
RESERVED	1:0	Write to 00 binary.	00

ADDL2 (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	RESERVED[6:0]						
Reset	0x1	0x0						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7	Write to 1 binary.	1
RESERVED	6:0	Write to 000_0000 binary.	0000000

Applications Information

Power-On Programming

To ensure the MAX41460 device enters the shutdown state after power on, the DATA pin must be held low at power on. If the DATA pin cannot be guaranteed low at power on, then the use of a high value pulldown resistor is recommended. After V_{DD} has settled, a logic low-high-low transition must occur on the DATA pin to properly enter the shutdown state and the CSB pin does not need to be exercised during this operation.

After turning on the power supply (or after a soft reset), a SPI transaction that burst-writes 17 consecutive registers from address 0x00 to 0x10 is required to initialize the PLL frequency synthesizer. See the *Initial Programming* section.

For example, the crystal frequency is 16MHz, the RF frequency is 315MHz, the 17 consecutive registers can be configured as:

[0x90, 0x81, 0x03, 0x00, 0x00, 0x04, 0x80, 0x80, 0x60, 0x00, 0x00, 0xC4, 0xDE, 0x98, 0x28, 0x04, 0x02].

After initial programming, the device will enter the shutdown, standby, or programming state according to the setting of PWDN_MODE[1:0] (register CFG4, address 0x03, bit[1:0]). Configuration register values are retained in all states unless changed by programming, or if the device is powered off or undergoes a SOFTRESET. See the *Startup* section for how to program the device for data transmission.

ASK Carrier Frequency

The ASK carrier frequency is set by the FREQ bits in registers 0x0B, 0x0C, and 0x0D. The user calculates the divide ratio based on the carrier frequency and crystal frequency. The following equation shows how to determine the correct value to be loaded into the FREQ registers.

$$FREQ = \left(\frac{fRF}{fXTAL}\right) \times 65536$$

For example, the desired ASK transmit frequency is 315MHz and the crystal frequency is 16MHz. 315/16 is 19.6875. 19.6875 x 65536 is 1290240. Converted into hex, the value is 0x13B000. This value is loaded into FREQ[23:0]. In the case where the value is non-integer, the value may be rounded to the nearest integer.

Digital FSK Modulation

The FSK modulation in MAX41460 is defined by the space frequency and the mark frequency. The space frequency is the lower frequency that represents a logic 0. The mark frequency is the higher frequency that represents a logic 1. The device defaults to Gaussian filtered frequency shaping to help reduce spectral emissions.

The space frequency is defined by the FREQ[23:0] bits (registers PLL3, PLL4, PLL5). To set the space frequency, use the following equation:

$$FREQ[23:0] = \frac{65536 * f_{SPACE}}{f_{XTAL}}$$

The mark frequency is defined by the space frequency plus a frequency deviation. If frequency shaping is disabled by setting FSKSHAPE = 0 (register CFG1, bit 2), the frequency deviation is defined by DELTAF[6:0] (register PLL6, bits 6:0).

$$DELTAF[6:0] = \frac{f_{\Delta} * 8192}{f_{XTAL}}$$

If frequency shaping is enabled by setting FSKSHAPE = 1 (register CFG1, bit 2), the frequency deviation is defined by DETLAF_SHAPE[3:0] (register PLL7, bits 3:0).

$$DELTAF\_SHAPE[3:0] = \frac{f_{\Delta} * 8192}{f_{XTAL} * 10}$$

When FSK shaping is enabled by setting FSKSHAPE = 1, the frequency is transitioned in 16 steps between the two

frequencies using a Gaussian filter shape. The time between each step is controlled by TSTEP[5:0] (register CFG5, bits 5:0). The time step can be adjusted based on the data rate.

$$TSTEP[5:0] = minimum\left(64, floor\left(\frac{200000}{f_{DATA\_RATE}}\right)\right) - 1$$

where $f_{DATARATE}$ has a unit of bits per second. For example, if $f_{DATARATE}$ is 47kbps, then TSTEP is floor (200000/47000) - 1 = 3.

In the preset mode, the frequency deviation is fixed at 78kHz.and TSTEP = 1.

FSK shaping supports a data rate up to 110kbps. Higher data rates is not recommended.

Tuning Capacitor Settings

The internal variable shunt capacitor, which can be used to match the PA to the antenna with changing transmitter frequency, is controlled by setting the 5-bit cap variable in the registers. This allows for 32 levels of shunt capacitance control. Since the control of these 5 bits is independent of the other settings, any capacitance value can be chosen at any frequency, making it possible to maintain maximum transmitter efficiency while moving rapidly from one frequency to another. The internal tuning capacitor adds 0 to 5.425pF to the PA output in 0.175pF steps.

Crystal Frequency Selection

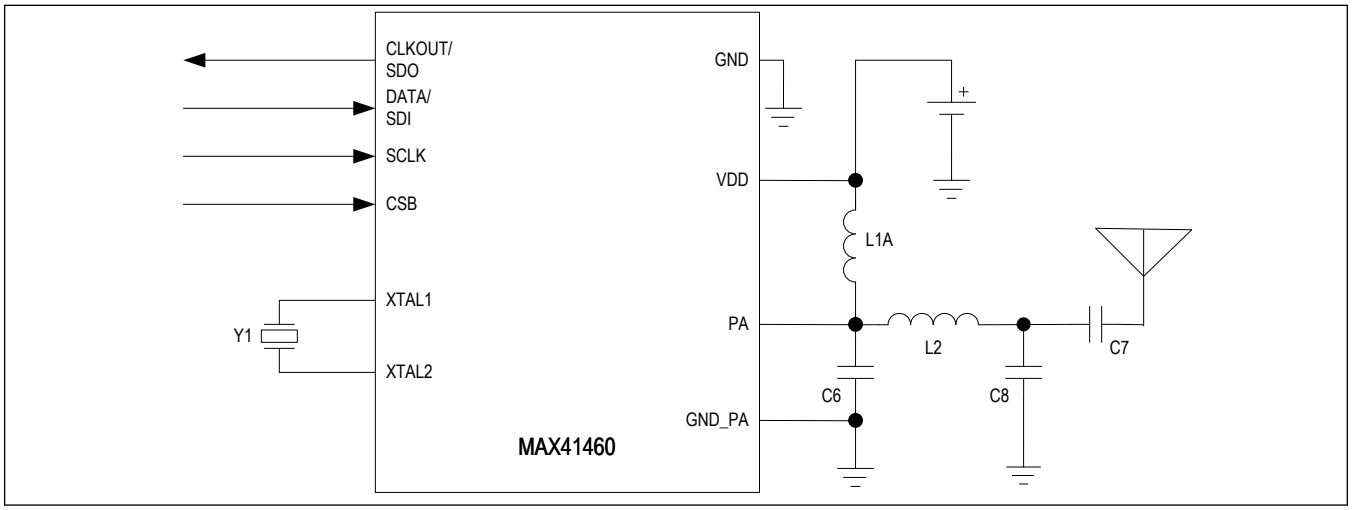
In order to avoid integer boundary spurs in fractional-N PLL synthesizers, the crystal should be selected so that the RF carrier frequency is more than 0.4 MHz apart from the nearest integer multiple of crystal frequency.

For example, the 16±0.002MHz crystals can be selected for the 433.92 MHz RF carrier, which is more than 0.4MHz apart from the nearest integer multiple of crystal frequency at 432±0.054MHz. However, the 16±0.002MHz crystals are not suitable for a RF carrier at 912MHz or 928MHz.

The crystal divider ratio should be programmed so that the divided clock frequency is 3.2±0.1MHz. In addition, the PLL synthesizer requires a reference frequency (same as crystal frequency) between 12.8MHz and 19.2MHz. Therefore, when crystal divider ratio is 4, 5, or 6, allowed range of crystal frequency is 12.8MHz~13.2MHz, 15.5MHz~16.5MHz, or 18.6MHz~19.2MHz.

In another example, desired RF frequencies are 319.5MHz, 345.0MHz and 433.92MHz, and recommended crystal selection is 13±0.002MHz so that integer boundary spurs are completely suppressed for three desired RF frequencies. Nevertheless, the 16±0.002MHz and 19.2±0.002MHz crystals are also acceptable.

Typical Application Circuit



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX41460GUB+	-40°C to +105°C	10 µMAX
MAX41460GUB+T	-40°C to +105°C	10 µMAX

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/18	Initial release	—
1	2/19	Updated Figure 3 and Figure 4	17, 18
2	3/19	Updated TSSOP references to µMAX	1, 2, 11, 13, 36

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