

# MAX3955

## 11.32Gbps Transceiver with Dual CDRs, Digital Monitors, and DC-Coupled Laser Driver

### General Description

The MAX3955 is an 11.3Gbps, highly-integrated, low-power transceiver with dual CDRs, and digital diagnostics monitoring (DDM) designed for next-generation SONET transmission systems. The receiver incorporates a limiting amplifier with loss-of-signal (LOS) circuit. The limiting amplifier features an independent 9.95Gbps to 11.32Gbps CDR. The transmitter incorporates Maxim's proprietary DC-coupled laser driver interface, an independent 9.95Gbps to 11.32Gbps CDR, and closed-loop control of average laser power.

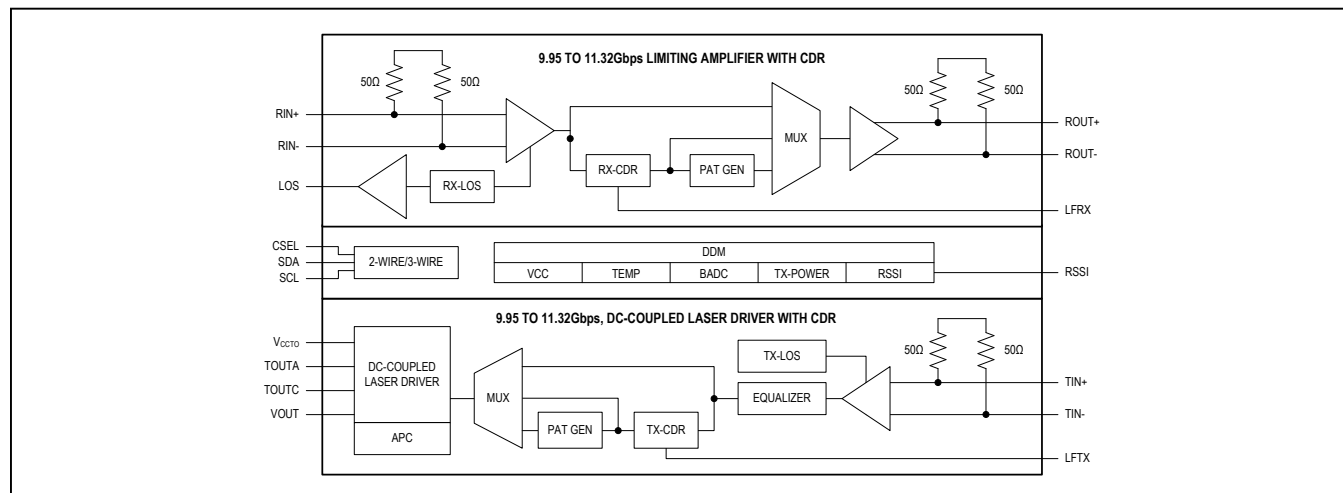
The MAX3955 supports differential AC-coupled signaling with integrated 50Ω terminations at Rx input, Rx output, and Tx input. The Tx output is a DC-coupled 25Ω laser diode interface with dedicated pins for the laser anode (TOUTA) and the laser cathode (TOUTC).

An integrated 12-bit analog-to-digital converter (ADC) is utilized to provide digital monitors of internal/external temperature,  $V_{CC}$ , and received signal strength indication (RSSI). The MAX3955's analog monitors and the use of a 2-wire or 3-wire slave interface enables configuration through either a digital-only microcontroller ( $\mu$ C) or through the DS1978 SFP+ controller (future product).

The MAX3955 operates from single +3.3V supply and over a -40°C to +95°C temperature range and is available in a standard 5mm x 5mm, 32-pin TQFN-EP package.

**Ordering Information** appears at end of data sheet.

### Simplified Block Diagram



### Benefits and Features

#### Performance

- Dual CDRs Exceeding SONET Jitter Requirements with PLL Bandwidth Setting of 7MHz
- 540mW Typical IC Power Dissipation ( $I_{LD\_MOD} = 45mA$ ,  $I_{BIAS} = 45mA$ , Both CDRs Enabled)

#### Flexibility

- Independent, Reference-less Tx and Rx CDRs
- Pattern Generator for Receive and Transmit Paths
- Signal Loop-Back Paths
- Programmable Tx Input Equalization and Rx Output Deemphasis
- Pin-Compatible with MAX3956 11.3Gbps Transceiver

#### Safety and Monitoring

- Integrated Eye Safety Features with Maskable Fault and Interrupt Signal Generation
- Analog Monitors with Integrated 12-Bit ADC, Fully Supporting SFF-8472 DDM with Digital-Only  $\mu$ C
- High-Accuracy Temperature,  $V_{CC}$ , and RSSI Monitors
- Auxiliary ADC Input at BADC for General Use

### Applications

- OC-192 XFP and SFP+ Optical Transceivers

For related parts and recommended products to use with this part, refer to [www.maximintegrated.com/MAX3955.related](http://www.maximintegrated.com/MAX3955.related).

## Absolute Maximum Ratings

Voltage at  $V_{CCX}$ ,  $V_{CCRO}$ ,  $V_{CCT}$ ,  $V_{CCTO}$  ..... -0.3V to +4.0V  
 Voltage at REGFILT ..... -0.3V to +2.0V  
 Current into  $V_{CCTO}$  ..... -15mA to +180mA  
 Current into REGFILT ..... -15mA to +15mA  
 Current into TOUTA and TOUTC ..... 150mA  
 Current into VOUT ..... -2mA to +90mA  
 Current into TIN+, TIN-, RIN+ and RIN- ..... -15mA to +15mA  
 Current into ROUT+ and ROUT- ..... -30mA to +30mA  
 Voltage at TIN+, TIN-, RIN+, RIN-, LOS,  
 DISABLE, MDIN, RSSI, I.C., FAULT,  
 SCL, SDA, INTRPT, and CSEL ..... -0.3V to ( $V_{CCX} + 0.3V$ )  
 Voltage at TSNS and TGND ..... -0.3V to +1.2V

Voltage at BADC ..... -0.3V to +2V  
 Voltage at TOUTA ..... ( $V_{CCTO} - 1.3V$ ) to ( $V_{CCTO} + 1.3V$ )  
 Voltage at TOUTC and VOUT ..... 0.3V to ( $V_{CCTO} - 0.4V$ )  
 Voltage at LFRX and LFTX ..... -0.3V to +2.5V  
 Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )  
     TQFN (derate 34.5mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ) ..... 2759mW  
 Junction Temperature .....  $+150^\circ\text{C}$   
 Storage Temperature Range .....  $-55^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Lead Temperature (soldering, 10s) .....  $+300^\circ\text{C}$   
 Soldering Temperature (reflow) .....  $+260^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Thermal Characteristics (Note 1)

TQFN

Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ ) .....  $29^\circ\text{C/W}$

Junction-to-Case Thermal Resistance ( $\theta_{JC}$ ) .....  $1.7^\circ\text{C/W}$

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

( $V_{CCX} = V_{CCRO} = V_{CCT} = 2.85V$  to  $3.47V$ ,  $V_{CCTO} = 2.97V$  to  $3.47V$ ,  $V_{GND} = 0V$ ,  $T_A = -40^\circ\text{C}$  to  $+95^\circ\text{C}$ . Typical values are at  $V_{CCX} = V_{CCRO} = V_{CCT} = V_{CCTO} = 3.3V$ ,  $14\Omega$  single-ended load for  $T_{OUTC}/T_{OUTA}$  and  $T_A = +25^\circ\text{C}$ , unless otherwise noted. See [Figure 1](#) for electrical setup.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Current	$I_{CC}$	Excludes output current through the external pullup inductors, $I_{LD\_MOD} = 60\text{mA}$ , $I_{LD\_DC} = 40\text{mA}$ , $SET\_CML[4:0] = 3d$ , both CDRs disabled (Note 3)		105	130	mA
		Same conditions as above except both CDRs enabled		165	185	
Power-On-Reset (Enable Part)	$V_{POR\_DE}$	(Note 4)		2.5		V
Power-On-Reset (Disable Part)	$V_{POR\_AS}$	(Note 4)		2.4		V
<b>RX INPUT SPECIFICATION</b>						
Input Sensitivity for BER<10 <sup>-12</sup>	$V_{RIN\_MIN}$	2 <sup>31</sup> -1 PRBS at 11.32Gbps		3		mV <sub>P-P</sub>
Differential Input Resistance	$R_{RIN}$			100		$\Omega$
<b>RX OUTPUT SPECIFICATION (SET_RXDE[2:0] = 0xx)</b>						
Differential Output Voltage Programming Range	$V_{ROUT}$	See Table 6 for more information	450		800	mV <sub>P-P</sub>
Differential Output Voltage when Squelched	$V_{ROUT}$	SQ_EN = 1		5		mV <sub>P-P</sub>
Differential Output Resistance	$R_{ROUT}$			100		$\Omega$
Deterministic Jitter	DJ	10.3125Gbps (Notes 4, 5, and 6)		4.6	10	ps <sub>P-P</sub>
		11.32Gbps (Notes 4, 5, and 6)		5.6	11	

**Electrical Characteristics (continued)**

( $V_{CCX} = V_{CCRO} = V_{CCT} = 2.85V$  to  $3.47V$ ,  $V_{CCTO} = 2.97V$  to  $3.47V$ ,  $V_{GND} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+95^{\circ}C$ . Typical values are at  $V_{CCX} = V_{CCRO} = V_{CCT} = V_{CCTO} = 3.3V$ ,  $14\Omega$  single-ended load for  $T_{OUTC}/T_{OUTA}$  and  $T_A = +25^{\circ}C$ , unless otherwise noted. See [Figure 1](#) for electrical setup.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Random Jitter	RJ	$V_{RIN} = 60mV_{P-P}$ at 10.3Gbps, 11111 00000 pattern, SET_CML[4:0] = 10d, CDR disabled (Note 4)		0.25	0.4	ps <sub>RMS</sub>
ROUT Rise/Fall Time	$t_R/t_F$	20% to 80%, 11111 00000 pattern (Notes 4 and 6)		27	35	ps
<b>RX CDR CHARACTERISTICS SPECIFICATION (Notes 4 and 17)</b>						
CDR Lock-in Range			9.95		11.32	Gbps
Input Sinusoidal Jitter Tolerance		RX_CDR_BW[4:0] = 0Dh, 0.15UI of cable-induced input DJ	f = 400kHz	1.72	2.25	UI <sub>P-P</sub>
			f = 4MHz	0.52	0.75	
			f = 40MHz	0.51	0.6	
Jitter Transfer Bandwidth Setting Range		Minimum recommended setting, RX_CDR_BW[4:0] = 03h		2		MHz
		Nominal setting, RX_CDR_BW[4:0] = 0Dh		7		
		Maximum recommended setting, RX_CDR_BW[4:0] = 1Fh		16		
Jitter Transfer Peaking		RX_CDR_BW[4:0] = 0Dh		0.02		dB
Jitter Generation		20kHz < frequency ≤ 80MHz, RX_CDR_BW[4:0] = 0Dh		3.5	5.5	mUI <sub>RMS</sub>
		4MHz < frequency ≤ 80MHz, RX_CDR_BW[4:0] = 0Dh		2.5		
Lock Acquisition Time		From XCVR_EN set to RX_LOL = 0		0.85	1	ms
<b>RX OMA BASED LOSS-OF-SIGNAL (LOS) SPECIFICATION (Notes 4 and 8)</b>						
Assert/Deassert Time		(Note 7)	2.3		80	μs
LOS Low Level Setting		SET_LOS[6:0] = 8d	Assert level	6	10	mV <sub>P-P</sub>
			Deassert level	12	16.7	
LOS Medium Level Setting		SET_LOS[6:0] = 38d	Assert level		48	mV <sub>P-P</sub>
			Deassert level		78	
LOS High Level Setting		SET_LOS[6:0] = 101d	Assert level		121	mV <sub>P-P</sub>
			Deassert level		197	
LOS Output Masking Time Range		LOS_MASKTIME = 0d		0		ms
		LOS_MASKTIME = 127d		4.6		
LOS Output Masking Time Setting Resolution		(Note 9)		36		μs

**Electrical Characteristics (continued)**

( $V_{CCX} = V_{CCRO} = V_{CCT} = 2.85V$  to  $3.47V$ ,  $V_{CCTO} = 2.97V$  to  $3.47V$ ,  $V_{GND} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+95^{\circ}C$ . Typical values are at  $V_{CCX} = V_{CCRO} = V_{CCT} = V_{CCTO} = 3.3V$ ,  $14\Omega$  single-ended load for  $T_{OUTC}/T_{OUTA}$  and  $T_A = +25^{\circ}C$ , unless otherwise noted. See [Figure 1](#) for electrical setup.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>TX INPUT SPECIFICATION</b>						
Differential Input Resistance	$R_{TIN}$			100		$\Omega$
<b>LASER DC CURRENT GENERATOR (Note 10)</b>						
Maximum DC-ON Current	$I_{DC\_MAX}$	Current into VOUT pin	57			mA
Minimum DC-ON Current	$I_{DC\_MIN}$	Current into VOUT pin		0.7	1	mA
Maximum DC-OFF Current	$I_{DC\_OFF}$	Laser current into VOUT pin when Tx output disabled			0.1	mA
<b>LASER MODULATOR OUTPUT (TX_EQ[1:0] = 00) (Note 11)</b>						
Maximum Modulation ON-Current	$I_{LD\_MOD\_MAX}$	Current into TOUTC, external $10\Omega$ differential load	85			mA
Minimum Modulation ON-Current	$I_{LD\_MOD\_MIN}$	Current into TOUTC, external $10\Omega$ differential load			10	mA
Modulation Output Termination	$R_{TOUT}$	Single-ended resistance		25		$\Omega$
Maximum Modulation OFF-Current	$I_{LD\_MOD\_OFF}$	Current into TOUTC pin when Tx output disabled			0.1	mA
Modulation Current DAC Stability		$10mA < I_{LD\_MOD} < 85mA$ (Notes 4 and 12)		1.5	4	%
<b>TX CDR SPECIFICATION (Notes 4 and 17)</b>						
CDR Lock-in Range			9.95		11.32	Gbps
Input Sinusoidal Jitter Tolerance		TX_CDR_BW[4:0] = 0Dh, $f = 400kHz$	1.66	2.15		UI <sub>P-P</sub>
		0.15UI of cable induced input DJ, $f = 4MHz$	0.59	0.78		
		$f = 40MHz$	0.58	0.69		
Jitter Transfer Bandwidth Setting Range		Minimum recommended setting, TX_CDR_BW[4:0] = 03h		2		MHz
		Nominal setting, TX_CDR_BW[4:0] = 0Dh		7		
		Maximum recommended setting, TX_CDR_BW[4:0] = 1Fh		16		
Jitter Transfer Peaking		TX_CDR_BW[4:0] = 0Dh		0.02		dB
Jitter Generation		20kHz < frequency $\leq$ 80MHz, TX_CDR_BW[4:0] = 0Dh		3.3	5.7	mUI <sub>RMS</sub>
		4MHz < frequency $\leq$ 80MHz, TX_CDR_BW[4:0] = 0Dh		2.7		
Lock Acquisition Time		From XCVR_EN set to TX_LOL = 0		0.75	1	ms

**Electrical Characteristics (continued)**

( $V_{CCX} = V_{CCRO} = V_{CCT} = 2.85V$  to  $3.47V$ ,  $V_{CCTO} = 2.97V$  to  $3.47V$ ,  $V_{GND} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+95^{\circ}C$ . Typical values are at  $V_{CCX} = V_{CCRO} = V_{CCT} = V_{CCTO} = 3.3V$ ,  $14\Omega$  single-ended load for  $T_{OUTC}/T_{OUTA}$  and  $T_A = +25^{\circ}C$ , unless otherwise noted. See [Figure 1](#) for electrical setup.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>LASER MODULATOR OUTPUT (TX_EQ[1:0] = 00, <math>10mA &lt; I_{LD\_MOD} &lt; 85mA</math>, <math>V_{TIN} = 150</math> to <math>1000mV_{p-p}</math> differential amplitude) (Note 4)</b>						
Modulation Current Rise/Fall Time	$t_R/t_F$	20% to 80%, 11111 00000 pattern		24	35	ps
Deterministic Jitter (Note 5)	DJ	10.3125Gbps		5	11	ps <sub>P-P</sub>
		11.32Gbps		5	11	
Random Jitter	RJ	11111 00000 pattern		0.23	0.55	ps <sub>RMS</sub>
<b>APC LOOP OPERATION SPECIFICATION</b>						
MD Average Current Range	$I_{MDIN\_AVG}$	Average current sunk from MDIN pin	50		2000	$\mu A$
Initialization Time	$t_{init}$	$I_{DC} = 40mA$ , $I_{MOD} = 60mA$ , $I_{DC\_init} = 0mA$ , $ER = 9dB$ , time from restart to $I_{DC}$ and $I_{MOD}$ at 90% of steady state		0.1		ms
<b>TIMING REQUIREMENTS (Note 4)</b>						
DISABLE Assert Time	$t_{off}$	Time from rising edge of DISABLE input signal to 10% of $I_{DC}$ and $I_{MOD}$		1.5	10	$\mu s$
DISABLE Negate Time	$t_{on}$	Time from falling edge of DISABLE to $I_{DC}$ and $I_{LD\_MOD}$ at 90% of steady state when $FAULT = low$ before reset		8		$\mu s$
FAULT Reset Time	$t_{recovery}$	Time from negation of latched fault using DISABLE to $I_{LD\_MOD} + I_{DC}$ at 90% of steady state		8		$\mu s$
FAULT Assert Time	$t_{fault}$	Time from fault to $TX\_FAULT = high$ , $C_{FAULT} \leq 20pF$ , $R_{FAULT} = 4.7k\Omega$		1	3	$\mu s$
DISABLE to Reset Time		Time DISABLE must be held high to reset fault	4			$\mu s$
<b>SAFETY FEATURES</b>						
Fault Assert Threshold at $V_{OUT}$		$FAULT$ always occurs for $V_{OUT} < V_{CCTO} - 2.8V$		$V_{CCTO} - 2.8V$		V
Fault Deassert Threshold at $V_{OUT}$		$FAULT$ never occurs for $V_{OUT} \geq V_{CCTO} - 2.0V$		$V_{CCTO} - 2.0V$		V
Fault Assert Threshold at $T_{OUTC}$		$FAULT$ always occurs for $V_{TOUTC} < 0.24V$		0.24		V
Fault Deassert Threshold at $T_{OUTC}$		$FAULT$ never occurs for $V_{TOUTC} \geq 0.58V$		0.58		V
Fault Assert Threshold at $T_{OUTA}$		$FAULT$ always occurs for $V_{TOUTA} < V_{CCTO} - 1.85V$		$V_{CCTO} - 1.85V$		V
Fault Deassert Threshold at $T_{OUTA}$		$FAULT$ never occurs for $V_{TOUTA} \geq V_{CCTO} - 1.34V$		$V_{CCTO} - 1.34V$		V

**Electrical Characteristics (continued)**

( $V_{CCX} = V_{CCRO} = V_{CCT} = 2.85V$  to  $3.47V$ ,  $V_{CCTO} = 2.97V$  to  $3.47V$ ,  $V_{GND} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+95^{\circ}C$ . Typical values are at  $V_{CCX} = V_{CCRO} = V_{CCT} = V_{CCTO} = 3.3V$ ,  $14\Omega$  single-ended load for  $T_{OUTC}/T_{OUTA}$  and  $T_A = +25^{\circ}C$ , unless otherwise noted. See [Figure 1](#) for electrical setup.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>RSSI MONITOR</b>						
ADC Resolution				16		bits
LSb Size				35.5		nA
RSSI Input Current Range			1		2000	$\mu A$
RSSI Offset Current				50		nA
RSSI Offset Current Stability		(Notes 4 and 13)	-120		+150	nA
RSSI Gain Error			-4		+4	%
<b>TX POWER MONITOR</b>						
Tx Power Monitor Accuracy		Average current into MDIN pin, $50\mu A < I_{MDIN\_AVG} < 2mA$ , excluding tracking error (Note 4)	-25		+25	%
<b>BADC MONITOR</b>						
Gain Error			-2		+2	%
ADC Full Scale				1.164		V
ADC Resolution				12		bits
ADC LSb Size				284		$\mu V$
<b>SUPPLY VOLTAGE MONITOR (<math>V_{CCX}</math>, <math>V_{CCRO}</math>, and <math>V_{CCT}</math>)</b>						
Supply Voltage Monitor Accuracy		$V_{CCX} = V_{CCRO} = V_{CCT} > V_{POR\_DE}$	-2		+2	%
ADC Resolution				12		bits
ADC LSb Size				1.137		mV
<b>TEMPERATURE SENSOR</b>						
External Temperature Sensor Accuracy		Measured with single PNP device (Note 4)	-2		+2	$^{\circ}C$
<b>DIGITAL INPUTS (SDA, SCL, CSEL, DISABLE)</b>						
Minimum Input Voltage High	$V_{IH}$			1.6		V
Maximum Input Voltage High	$V_{IH}$			$V_{CC}$		V
Minimum Input Voltage Low	$V_{IL}$			0		V
Maximum Input Voltage Low	$V_{IL}$			0.8		V
Input Hysteresis	$V_{HYS}$			80		mV
Input Leakage Current High (SDA, DISABLE)	$I_{IH}$	Input connected to $V_{CCRO}$	-10		+10	$\mu A$
Input Leakage Current High (SCL, CSEL)	$I_{IH}$	Input connected to $V_{CCRO}$ , internal $75k\Omega$ pulldown	20	44	100	$\mu A$

**Electrical Characteristics (continued)**

( $V_{CCX} = V_{CCRO} = V_{CCT} = 2.85V$  to  $3.47V$ ,  $V_{CCTO} = 2.97V$  to  $3.47V$ ,  $V_{GND} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+95^{\circ}C$ . Typical values are at  $V_{CCX} = V_{CCRO} = V_{CCT} = V_{CCTO} = 3.3V$ ,  $14\Omega$  single-ended load for  $T_{OUTC}/T_{OUTA}$  and  $T_A = +25^{\circ}C$ , unless otherwise noted. See [Figure 1](#) for electrical setup.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current Low (SCL, CSEL)	$I_{IL}$	Input connected to GND	-10		+10	$\mu A$
Input Leakage Current Low (SDA)	$I_{IL}$	Input connected to GND, internal 75k $\Omega$ pullup	20	44	100	$\mu A$
Input Leakage Current Low (DISABLE)	$I_{IL}$	Input connected to GND, internal 7.5k $\Omega$ pullup	200	450	800	$\mu A$
<b>DIGITAL OPEN-DRAIN OUTPUT (SDA, LOS, and FAULT) (Note 15)</b>						
Output Low Voltage	$V_{OL}$	External pullup is between 4.7k $\Omega$ and 10k $\Omega$ to $V_{CCRO}$			0.4	V
Output High Voltage	$V_{OH}$	External pullup is between 4.7k $\Omega$ and 10k $\Omega$ to $V_{CCRO}$	$V_{CCRO} - 0.4$	$V_{CCRO}$		V
<b>DIGITAL CMOS OUTPUT (INTRPT, LOS, and FAULT) (Note 15)</b>						
Output Low Voltage	$V_{OL}$	$I_{OL} = 1mA$			0.4	V
Output High Voltage	$V_{OH}$	$I_{OH} = 1mA$	$V_{CCRO} - 0.4$			
<b>3-WIRE TIMING SPECIFICATIONS (Figure 3)</b>						
SCL Clock Frequency	$f_{SCL}$			1000		kHz
SCL Pulse-Width High	$t_{CH}$			500		ns
SCL Pulse-Width Low	$t_{CL}$			500		ns
SDA Setup Time	$t_{DS}$			100		ns
SDA Hold Time	$t_{DH}$			100		ns
SCL Rise to SDA Propagation Time	$t_D$			12		ns
CSEL Pulse-Width Low	$t_{CSW}$			500		ns
CSEL Leading Time Before the First SCL Edge	$t_L$			500		ns
CSEL Trailing Time After the Last SCL Edge	$t_T$			500		ns
SDA, SCL Load	$C_b$	Total bus capacitance on one line with 4.7k $\Omega$ pullup from SDA to $V_{CC}$		20		pF
<b>2-WIRE TIMING SPECIFICATIONS (Figure 5)</b>						
SCL Clock Frequency	$f_{SCL}$			400		kHz
Minimum SCL Pulse-Width High	$t_{CH}$			1.3		$\mu s$
Minimum SCL Pulse-Width Low	$t_{CL}$			0.6		$\mu s$
Minimum Bus Free Time Between STOP and START Condition	$t_{BUF}$			1.3		$\mu s$

**Electrical Characteristics (continued)**

( $V_{CCX} = V_{CCRO} = V_{CCT} = 2.85V$  to  $3.47V$ ,  $V_{CCTO} = 2.97V$  to  $3.47V$ ,  $V_{GND} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+95^{\circ}C$ . Typical values are at  $V_{CCX} = V_{CCRO} = V_{CCT} = V_{CCTO} = 3.3V$ ,  $14\Omega$  single-ended load for  $T_{OUTC}/T_{OUTA}$  and  $T_A = +25^{\circ}C$ , unless otherwise noted. See [Figure 1](#) for electrical setup.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum STOP Setup Time	$t_{SU\_STO}$			600		ns
Minimum START Setup Time	$t_{SU\_STA}$			600		ns
Minimum START Hold Time	$t_{HD\_STA}$			600		ns
Minimum SDA Setup Time	$t_{SU\_DAT}$			100		ns
Minimum SDA Hold Time	$t_{HD\_DAT}$	Receive		0		ns
		Transmit		300		
Minimum SCL and SDA Rise and Fall Time	$t_R, t_F$	(Note 16)		$20 + 0.1C_b$		ns
Maximum Spike Pulse Width Suppressed by Input Filter	$t_{SP}$			50		ns
Capacitance Load for Each Bus Line	$C_b$	Total bus capacitance on one line with $4.7k\Omega$ pullup from SDA to $V_{CC}$		20		pF

**Note 2:** Limits are 100% tested at  $T_A = +25^{\circ}C$  (and/or  $T_A = +95^{\circ}C$ ). Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

**Note 3:** VOUT is connected to 1.9V. TOUTA is connected to  $V_{CCTO}$  through pullup inductors, and TOUTC is connected to VOUT through pullup inductors.

**Note 4:** Guaranteed by design and characterization.

**Note 5:** A repeating  $2^7$  PRBS + 72 zeros and  $2^7$  PRBS(inverted) + 72 ones pattern is used. Deterministic jitter is defined as the arithmetic sum of pulse-width distortion (PWD) and pattern-dependent jitter (PDJ). CDR is enabled.

**Note 6:**  $V_{RIN}$  is 30mV<sub>P-P</sub> to 1.2V<sub>P-P</sub> differential amplitude, SET\_CML = 10d. Input data transition time is 21ps (20% to 80%).

**Note 7:** LOS must not assert if the input data is invalid for less than 2.3μs. The LOS must assert, if the data is invalid for more than 80μs. The signal at the input will be switched between two amplitudes Signal\_ON, and Signal\_OFF.

1) Receiver operates at sensitivity level plus 1dB power penalty

A) Signal\_OFF = 0

Signal\_ON = (+8dB) + 10log(min\_assert\_level)

B) Signal\_ON = (+1dB) + 10log(max\_deassert\_level)

Signal\_OFF = 0

2) Receiver operates at overload

Signal\_OFF = 0

Signal\_ON = 1.2V<sub>P-P</sub>

**Note 8:** LOS hysteresis ( $10 \times \log(V_{LOS-DEASSERT}/V_{LOS-ASSERT})dB$ ) is designed to be  $> 1.25dB$  for SET\_LOS DAC code from 8d to 101d. LOS is characterized with a  $2^{23}-1$  PRBS pattern.

**Note 9:** Output of a TIA in case of loss of light, see [Figure 7](#).

**Note 10:**  $I_{LD\_DC} = I_{DC} + 0.5 \times I_{MOD} \times R/(50 + R)$ , where  $I_{LD\_DC}$  is the effective laser DC current,  $I_{DC}$  is the DC DAC current,  $I_{MOD}$  is the modulation DAC current, and R is the differential laser load resistance. Example: For  $R = 5\Omega$ ,  $I_{LD\_DC} = I_{DC} + 0.045 \times I_{MOD}$ .

**Note 11:**  $I_{LD\_MOD} = I_{MOD} \times 50/(50 + R)$ , where  $I_{LD\_MOD}$  is the effective laser modulation current,  $I_{MOD}$  is the modulation DAC current, and R is the differential laser load resistance. Example: For  $R = 5\Omega$ ,  $I_{LD\_MOD} = 0.91 \times I_{MOD}$ .



### Electrical Characteristics (continued)

( $V_{CCX} = V_{CCRO} = V_{CCT} = 2.85V$  to  $3.47V$ ,  $V_{CCTO} = 2.97V$  to  $3.47V$ ,  $V_{GND} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+95^{\circ}C$ . Typical values are at  $V_{CCX} = V_{CCRO} = V_{CCT} = V_{CCTO} = 3.3V$ ,  $14\Omega$  single-ended load for  $T_{OUTC}/T_{OUTA}$  and  $T_A = +25^{\circ}C$ , unless otherwise noted. See [Figure 1](#) for electrical setup.) (Note 2)

- Note 12:** Stability is defined as  $[(I_{MEASURED}) - (I_{REFERENCE})]/(I_{REFERENCE})$  over the listed current/temperature range and  $V_{CCT} = V_{CCX} = V_{CCRO} = V_{CCREF} \pm 5\%$ ,  $V_{CCREF} = 3.3V$ . Reference current measured at  $V_{CCREF}$  and  $T_{REF} = +25^{\circ}C$ .
- Note 13:** Stability is defined as  $[(I_{MEASURED}) - (I_{REFERENCE})]$  over the listed temperature and supply range. Reference current measured at  $V_{CC} = 3.3V$  and  $T_{REF} = +25^{\circ}C$ .
- Note 14:** Calibrated at room temperature by adjusting  $TSNS\_INT\_OFS[15:0]$  ( $TSNS\_INT\_SCL[15:0]$  unchanged from default value). To reduce the effect of self-heating the Rx and Tx circuitry are disabled. To minimize the reported error over the full temperature range, calibration is set such that the reported result is  $2^{\circ}C$  above ambient at room temperature. In the application, self-heating may introduce additional variation.
- Note 15:** For open-drain configuration,  $FAULT\_PU\_EN = 0$  and  $LOS\_PU\_EN = 0$ . For CMOS output configuration,  $FAULT\_PU\_EN = 1$  and  $LOS\_PU\_EN = 1$ .
- Note 16:**  $C_b$  = total capacitance of one bus line in picofarads.
- Note 17:** With  $0.15U_{P-P}$  of cable-loss induced deterministic jitter at the input. Jitter tolerance measured with a BER threshold of  $1 \times 10^{-10}$  and a confidence level of 0.95. Input pattern is a SONET frame containing a payload of  $2^{31}-1$  PRBS at a data rate of 9.95328Gbps. The input amplitude is  $250mV_{P-P}$  differential.  $SET\_RXDE = 6$  and  $TX\_EQ = 3$ . All jitter measurements performed at 7MHz PLL bandwidth ( $RX/TX\_CDR\_BW[4:0] = 0Dh$ ).

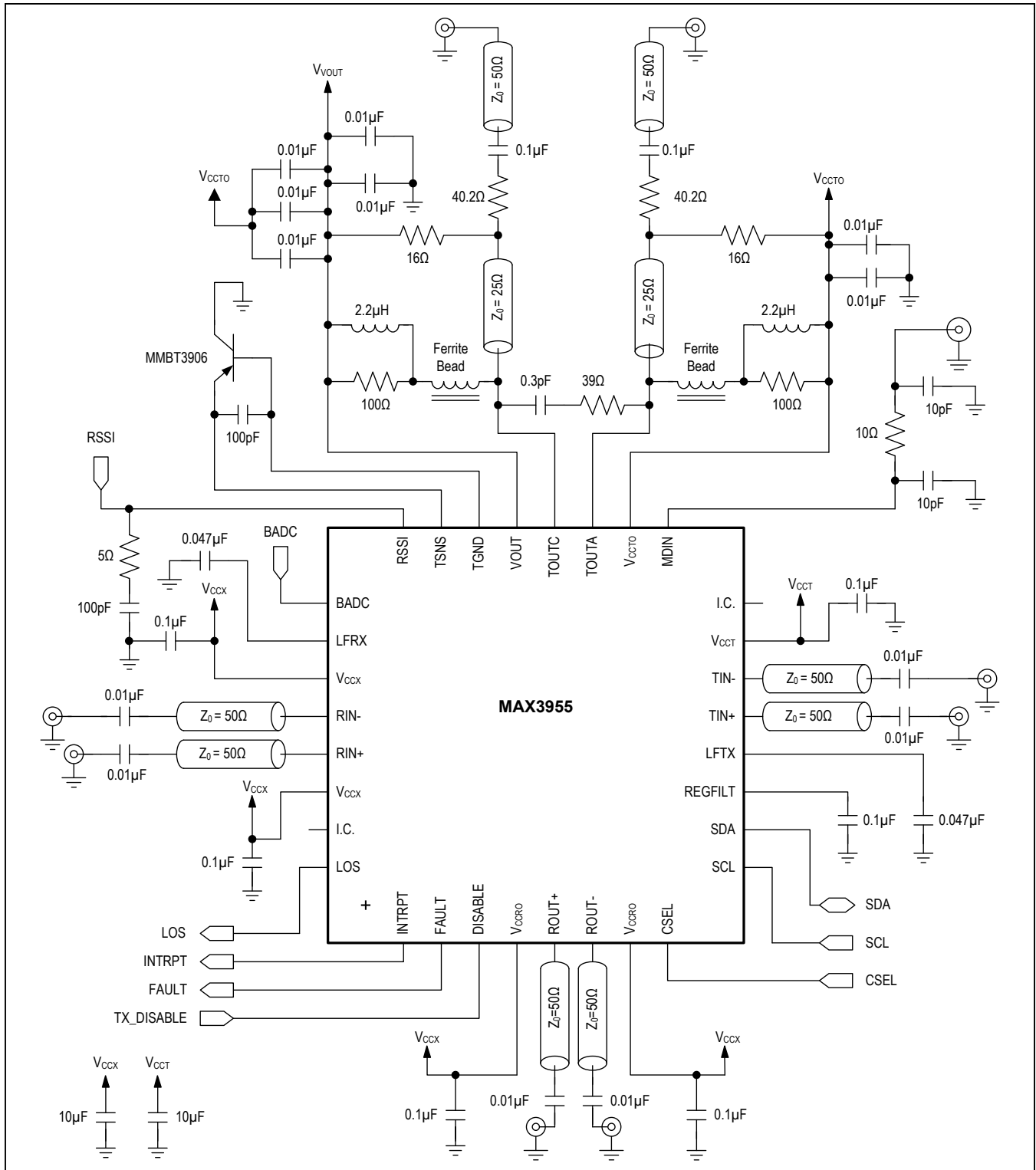
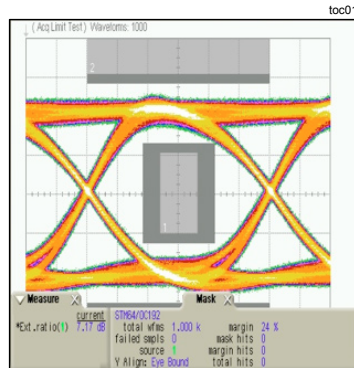


Figure 1. AC Electrical Test Schematic

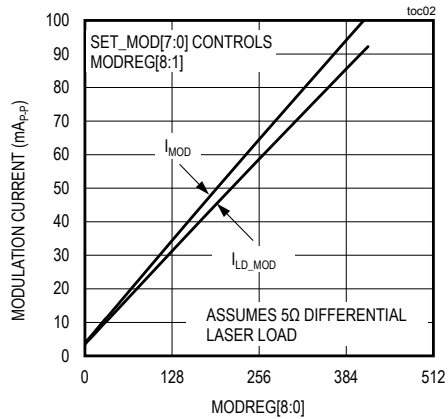
## Typical Operating Characteristics

(V<sub>CC</sub> = 3.3V, T<sub>A</sub> = +25°C, data pattern = 2<sup>31</sup>-1 PRBS, unless otherwise noted.)

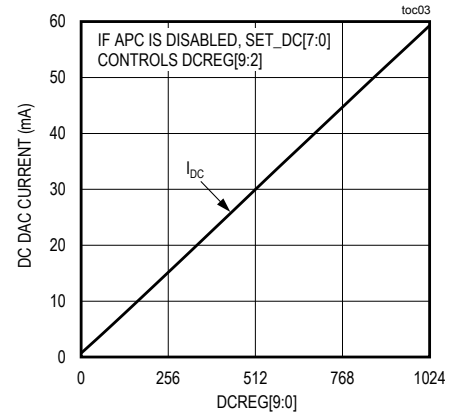
10Gbps OPTICAL EYE DIAGRAM



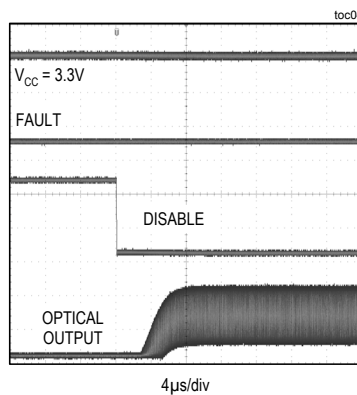
MODULATION CURRENT vs. MODREG



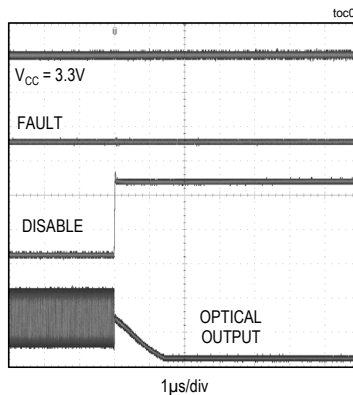
DC DAC CURRENT vs. DCREG



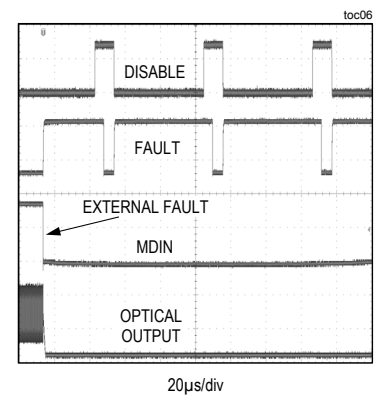
TRANSMITTER ENABLE



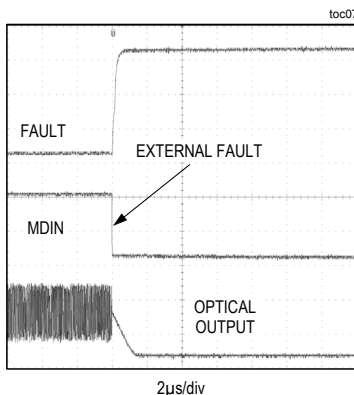
TRANSMITTER DISABLE



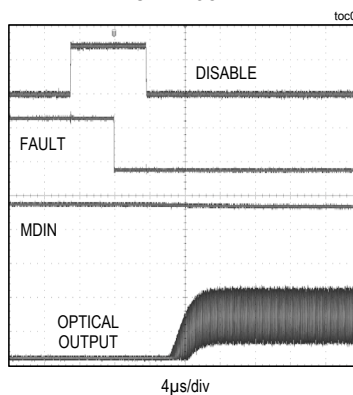
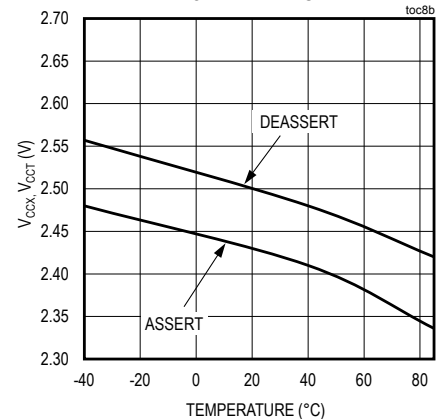
FREQUENT ASSERTION OF DISABLE



RESPONSE TO FAULT

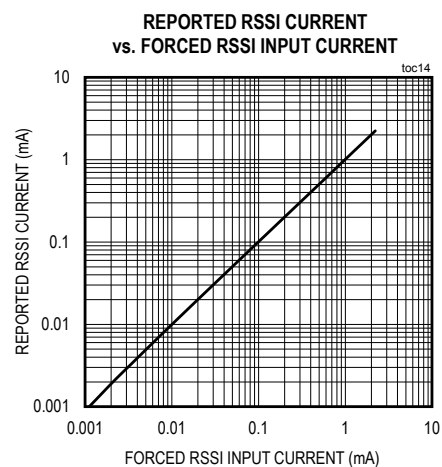
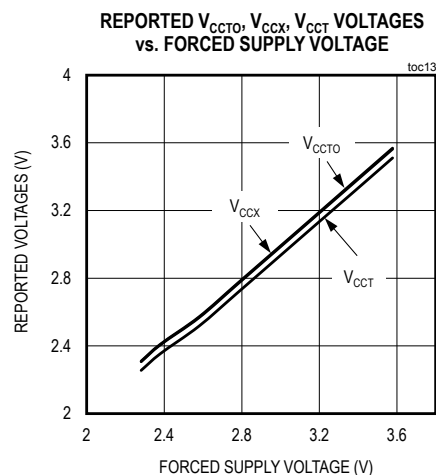
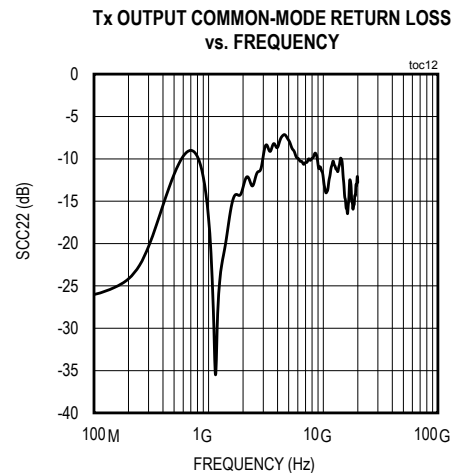
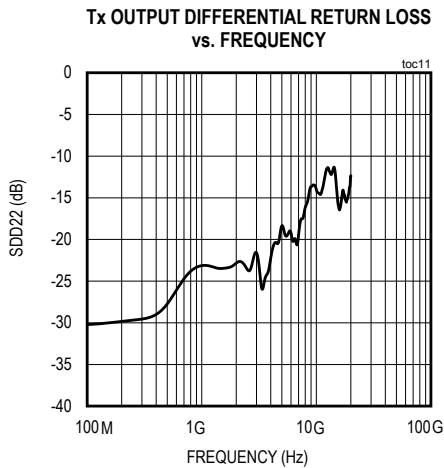
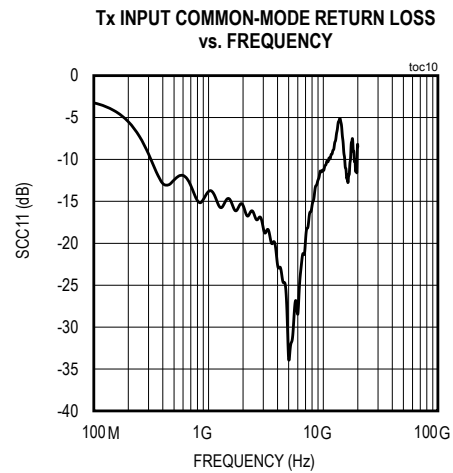
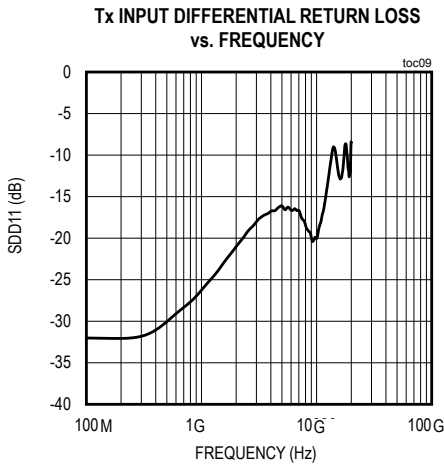


FAULT RECOVERY

POR (P3VFLAG) ASSERT/DEASSERT  
vs. TEMPERATURE

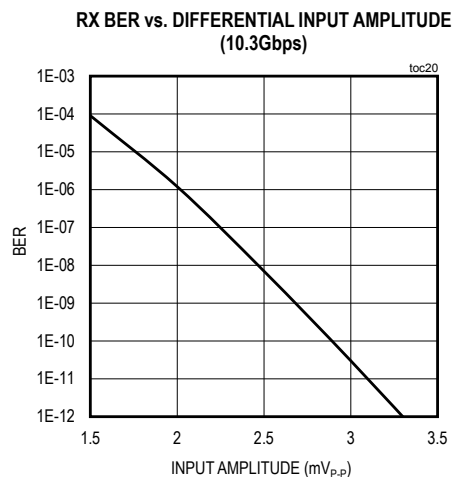
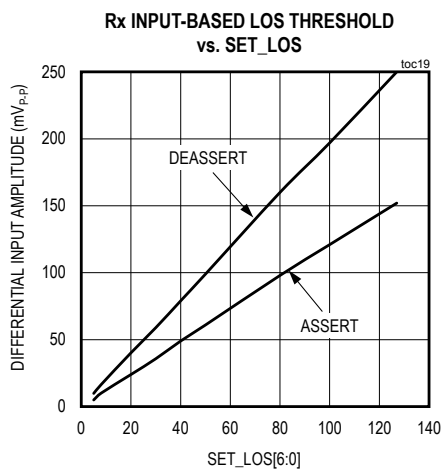
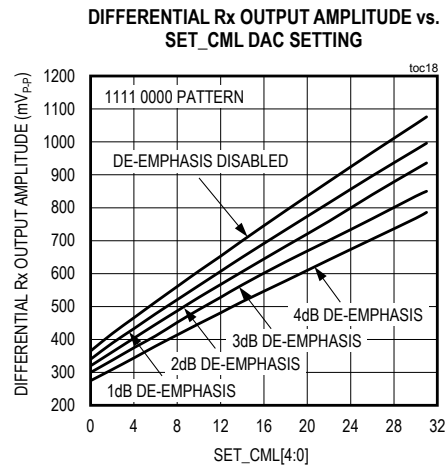
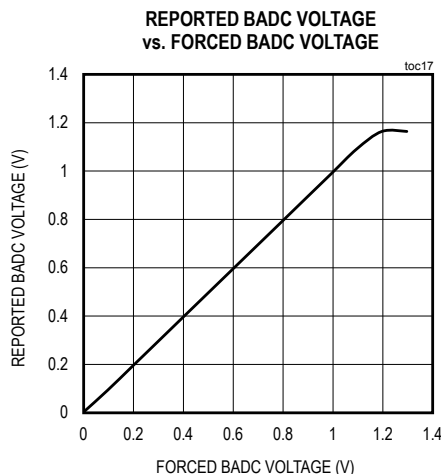
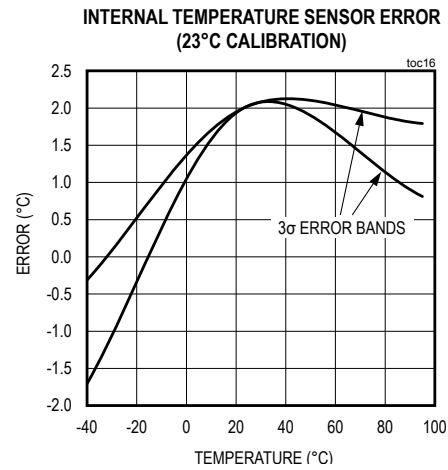
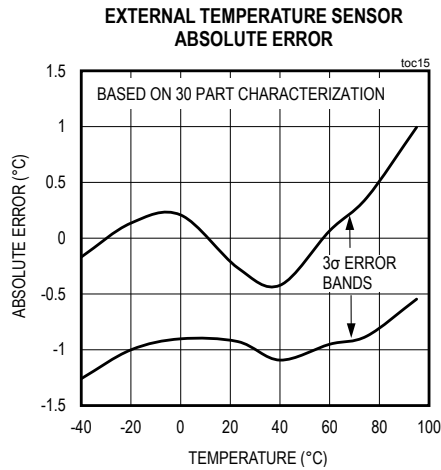
## Typical Operating Characteristics

( $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$ , data pattern =  $2^{31}-1$  PRBS, unless otherwise noted.)



## Typical Operating Characteristics

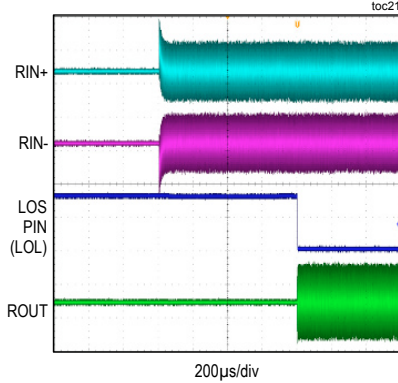
( $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$ , data pattern =  $2^{31}-1$  PRBS, unless otherwise noted.)



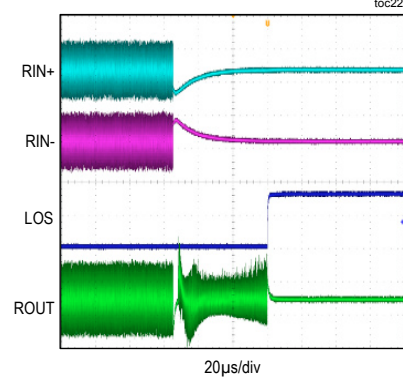
## Typical Operating Characteristics

( $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$ , data pattern =  $2^{31}-1$  PRBS, unless otherwise noted.)

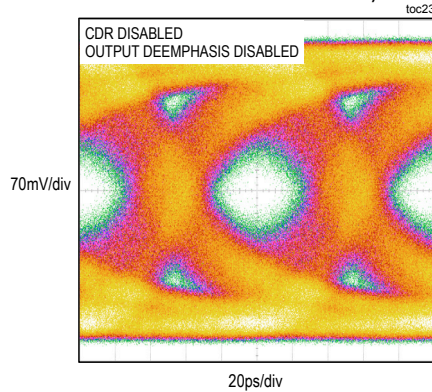
**LOL DEASSERT RESPONSE TIME**  
(SQUELCH ENABLED, LOS\_CFG[1:0] = 01)



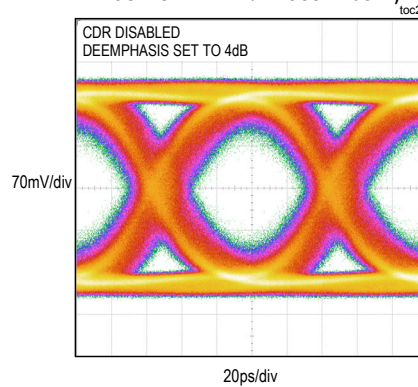
**LOL ASSERT RESPONSE TIME**  
(SQUELCH ENABLED, LOS\_CFG[1:0] = 01)



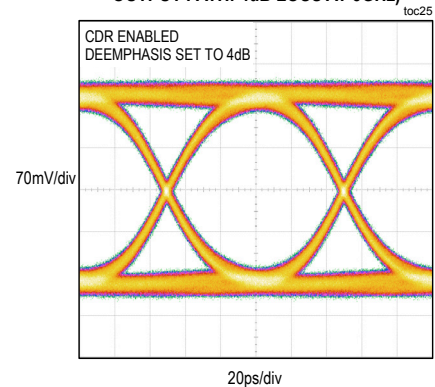
**Rx OUTPUT**  
(9.95Gbps,  $V_{RIN\pm} = 30mV_{p-p}$ , 0.40UI SOURCE DJ,  
OUTPUT: 4dB LOSS AT 5GHz)



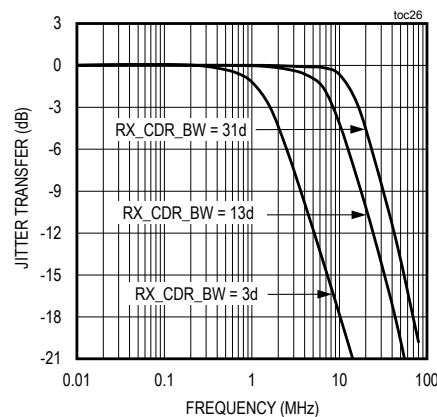
**Rx OUTPUT**  
(9.95Gbps,  $V_{RIN\pm} = 30mV_{p-p}$ , 0.40UI SOURCE DJ,  
OUTPUT PATH: 4dB LOSS AT 5GHz)



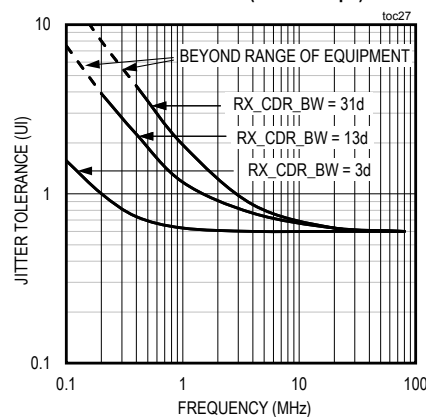
**Rx OUTPUT**  
(9.95Gbps,  $V_{RIN\pm} = 30mV_{p-p}$ , 0.40UI SOURCE DJ,  
OUTPUT PATH: 4dB LOSS AT 5GHz)



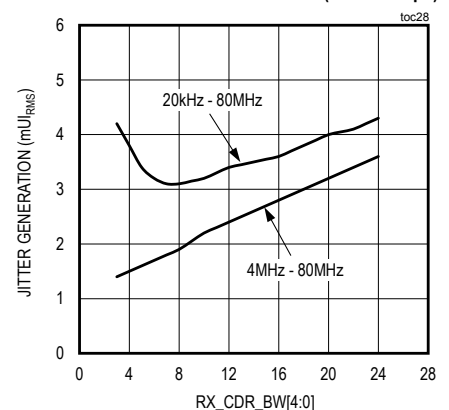
**JITTER TRANSFER**  
vs. FREQUENCY (9.95328Gbps)



**JITTER TOLERANCE**  
vs. FREQUENCY (9.95328Gbps)



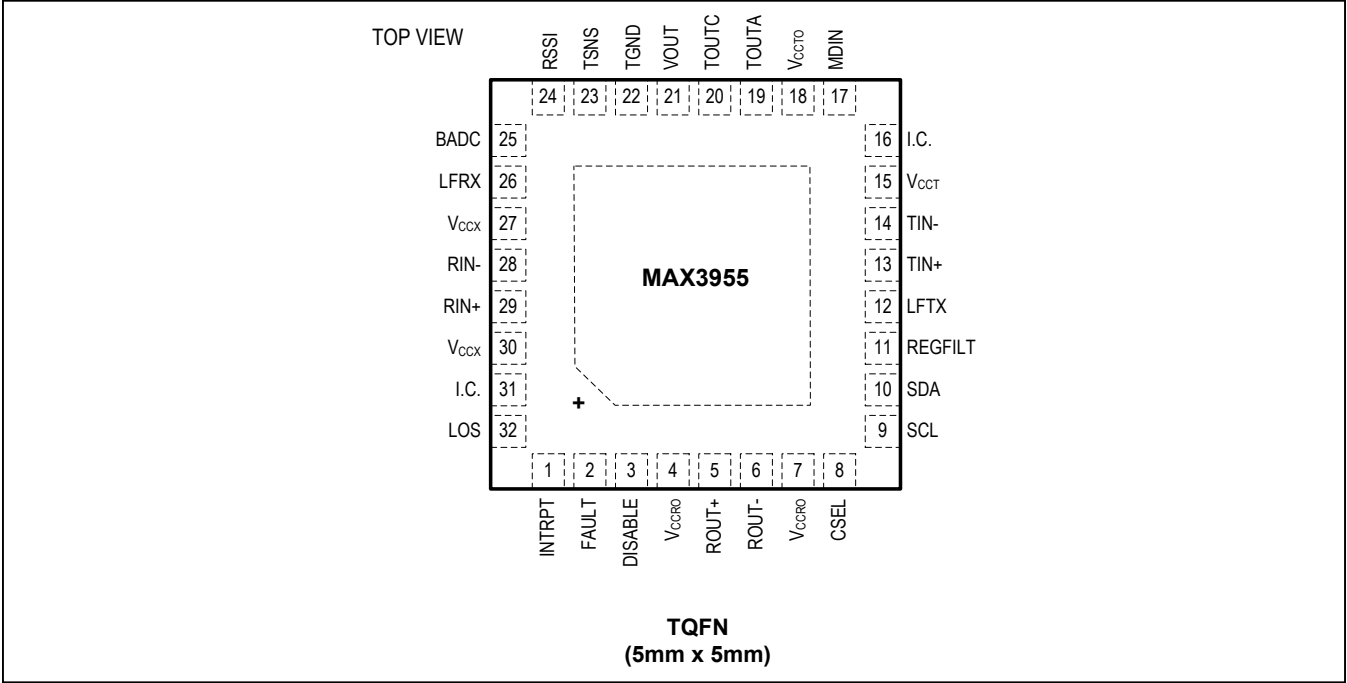
**RX JITTER GENERATION**  
vs. CDR BANDWIDTH SETTING (9.95328Gbps)



MAX3955

11.32Gbps Transceiver with Dual CDRs,  
Digital Monitors, and DC-Coupled Laser Driver

Pin Configuration



Pin Description

PIN	NAME	FUNCTION	EQUIVALENT CIRCUIT
1	INTRPT	Interrupt Output, CMOS. Programmable interrupt signal.	<p>The diagram shows the internal circuitry of the INTRPT pin. It is a CMOS output driver. The output node is connected to VCCRO through a PMOS transistor and to ground through an NMOS transistor. The output signal is labeled INTRPT. An ESD PROTECTION diode is shown connected between the output node and ground.</p>

## Pin Description (continued)

PIN	NAME	FUNCTION	EQUIVALENT CIRCUIT
2	FAULT	Transmitter Fault, Open-Drain Output. A logic-high indicates a fault condition has been detected. It remains high even after the fault condition has been removed. A logic-low occurs when the fault condition has been removed and the fault latch has been cleared by the DISABLE signal. Connect FAULT to host $V_{CC}$ via a 4.7k $\Omega$ to 10k $\Omega$ resistor. FAULT can also be configured as a CMOS output requiring no external resistor by setting the FAULT_PU_EN bit high.	
3	DISABLE	Transmitter Disable, LVTTL/CMOS Input. Set to logic-low for normal operation. Logic-high or open disables both the modulation and DC current. Internally pulled up by a 7.5k $\Omega$ resistor to $V_{CCRO}$ .	
4, 7	$V_{CCRO}$	Power Supply. Provides supply voltage to the transceiver digital core and the Rx output circuitry.	—
5	ROUT+	Differential Receiver Data Output, CML. This output has 50 $\Omega$ terminations to $V_{CCRO}$ . Polarity is set by the RX_POL bit.	
6	ROUT-		



## Pin Description (continued)

PIN	NAME	FUNCTION	EQUIVALENT CIRCUIT
8	CSEL	Chip-Select Input, CMOS. Used for 3-Wire communication. Setting CSEL to logic-high starts a cycle. Setting CSEL to logic-low ends the cycle and resets the control state machine. Internally pulled to ground by a 75k $\Omega$ resistor. Set low if using 2-wire communication.	
9	SCL	Serial-Clock Input, CMOS. Internally pulled to ground by a 75k $\Omega$ resistor.	
10	SDA	Serial-Data Bidirectional I/O, CMOS. Open-Drain Output. This pin has a 75k $\Omega$ internal pullup, but it requires an external 4.7k $\Omega$ to 10k $\Omega$ pullup to meet 3-wire timing specifications.	
11	REGFILT	Internal Filter Node. Requires 0.1 $\mu$ F decoupling capacitor to ground.	—
12	LFTX	Capacitor connection for transmitter CDR. Connect a 0.047 $\mu$ F capacitor from this pin to GND.	—

## Pin Description (continued)

PIN	NAME	FUNCTION	EQUIVALENT CIRCUIT
13	TIN+	Differential Transmitter Data Input. The polarity is set by the TX_POL bit.	
14	TIN-		
15	V <sub>CCT</sub>	Power Supply. Provides supply voltage to the transmitter core.	—
16, 31	I.C.	Internal Connection. Leave pins unconnected.	—
17	MDIN	Monitor Diode Input. Connect this pin to the cathode of the monitor diode. For transmitter power monitoring MDIN needs to be connected even for open-loop operation. External filtering on this pin should be optimized for each TOSA configuration. The Thevenin equivalent input of this pin is 40Ω to V <sub>CCT</sub> - 1.25V	—
18	V <sub>CCTO</sub>	Power Supply. Provides power to the transmitter output and laser TOSA.	
19	TOUTA	Inverting Modulator Current Output with 25Ω Back-Termination. Connect to laser anode through 25Ω transmission line.	
20	TOUTC	Noninverting Modulator Current Output with 25Ω Back-Termination. Connect to laser cathode through 25Ω transmission line.	

## Pin Description (continued)

PIN	NAME	FUNCTION	EQUIVALENT CIRCUIT
21	VOUT	Combined Laser Cathode Current Return Path and Sinking Laser DC Current Output. The current into this pin along with a portion of the modulation current make up the average laser current.	
22	TGND	Connect to an external temperature sensor (cathode). If using the internal temperature sensor, this pin can be left open.	
23	TSNS	Connect to an external temperature sensor (anode). If using the internal temperature sensor, this pin can be left open.	
24	RSSI	Current Input to Main ADC For Receive-Signal-Strength-Indication (RSSI). The voltage at this pin is regulated internally to 1.62V.	
25	BADC	Auxiliary ADC Input (1.164V Full-Scale)	—
26	LFRX	Capacitor Connection For Receiver CDR. Connect a 0.047μF capacitor from this pin to GND.	—

## Pin Description (continued)

PIN	NAME	FUNCTION	EQUIVALENT CIRCUIT
27, 30	V <sub>CCX</sub>	Power Supply. Provides supply voltage to the receiver core.	—
28	RIN-	Differential Receiver Data Input. Contains 50Ω terminations On-Chip. Connect these inputs to the TIA outputs using coupling capacitors.	
29	RIN+		
32	LOS	Receiver Loss-of-Signal (LOS) Output, Open Drain. This output goes to a logic-high when the level of the input signal drops below the SET_LOS register threshold. Polarity is set by LOS_POL register. The LOS circuitry can be disabled by setting LOS_EN = 0. Pull this pin to Host V <sub>CC</sub> via a 4.7kΩ to 10kΩ resistor. LOS can also be configured as a CMOS output requiring no external resistor by setting the LOS_PU_EN bit high.	
—	EP	Exposed Pad. Ground. This is the only electrical connection to ground and must be soldered to circuit board ground for proper thermal and electrical performance (see the <i>Exposed-Pad Package and Thermal Considerations</i> section).	—

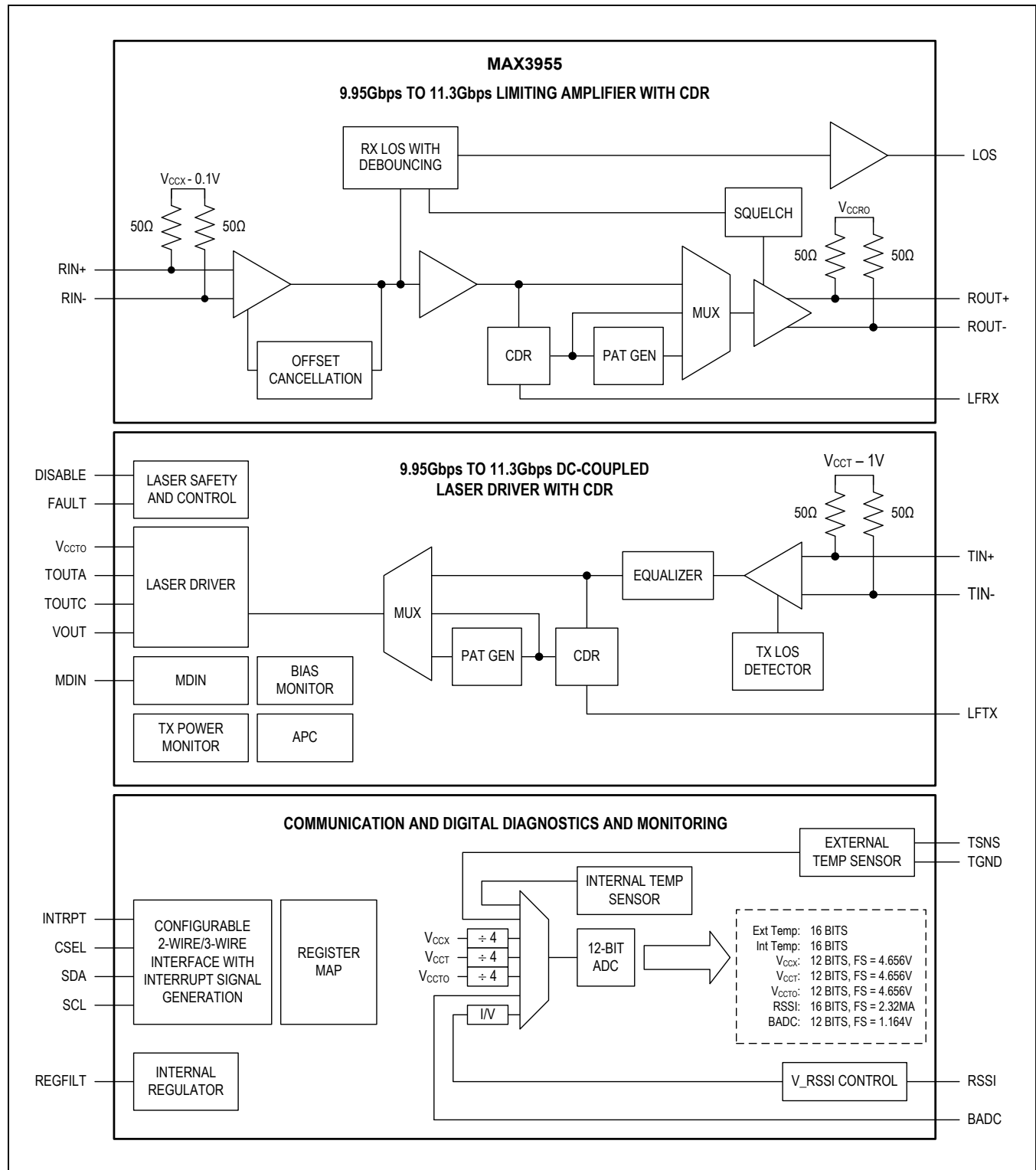


Figure 2. Functional Diagram

## Detailed Description

The MAX3955 combines a high-gain limiting amplifier, laser driver, independent Tx/Rx CDRs, Tx/Rx pattern generators, and digital diagnostics monitoring (DDM). The limiting amplifier includes offset cancellation, programmable signal detect threshold, selectable bandwidth, and deemphasis. The laser driver includes automatic power control (APC), laser current and power measurement capability, overcurrent limiting, and fault detection. A serial control interface enables an external controller to set all parameters necessary for operation and read all monitors and status indicators. The interface accepts either 2-wire or 3-wire protocol.

The features and performance are specifically designed to be compatible with low-cost microcontrollers to provide complete SFF-8472 functionality, including laser fault detection, diagnostics, and automatic power control. The MAX3955 includes all the logic required for laser protection, control loop operation, and monitor diode (MD) current measurement.

### 9.95Gbps to 11.32Gbps Limiting Amplifier Block Description

#### Limiting Amplifier

The limiting amplifier consists of a high-frequency amplifier, CDR, offset-correction circuit, loss-of-signal detector, and output buffer. Its low noise and high gain optimize optical performance. Configuration options (LOS threshold, LOS polarity, output amplitude, output deemphasis, and data polarity) enhance layout flexibility and ROSA compatibility.

#### High-Frequency Inputs

The RIN± inputs have an internal 100Ω differential termination and should be AC-coupled to the transimpedance amplifier.

#### Offset Cancellation

The offset cancellation loop compensates for pulse-width distortion at RIN± and internal offsets. The default small-signal low-frequency cutoff of the offset cancellation loop is 10kHz when AZ\_BW[1:0] is set to 01.

#### Loss-of-Signal Detector (LOS)

The loss-of-signal circuitry detects the amplitude of the incoming signal and compares it against a programmable threshold, which is controlled by SET\_LOS[6:0]. The LOS assert range is 10mV<sub>P-P</sub> to 121mV<sub>P-P</sub>. Changing the LOS threshold during operation (i.e., without executing a reset) does not cause a glitch or incorrect LOS output. The detector has 2dB of hysteresis to eliminate chatter

at the LOS output. The LOS output polarity is controlled by the LOS\_POL bit. The entire LOS circuit block can be disabled by setting LOS\_EN = 0.

#### Output Drivers

The ROUT± outputs are terminated with 50Ω to V<sub>CCRO</sub>. The differential output level is programmable between 450mV<sub>P-P</sub> and 800mV<sub>P-P</sub> by SET\_CML[4:0], and the output polarity can be inverted. The output can be disabled to its common-mode voltage either manually (RO\_EN = 0) or automatically by an LOS condition (SQ\_EN = 1 and LOS asserted).

Deemphasis can be enabled to compensate for FR4 losses. If enabled, settings of 1dB, 2dB, 3dB, and 4dB deemphasis are available.

### 9.95Gbps to 11.32Gbps Laser Driver Block Description

The laser driver consists of a high-speed differential input buffer, adjustable input equalizer, polarity switch buffer, CDR, laser modulator and DC current generator, monitor diode input buffer with adjustable gain, APC loop circuitry, eye-safety monitors, and DISABLE pin.

#### Differential High-Speed Input Buffer with Programmable Equalization

The TIN± inputs are internally biased and have a 100Ω differential termination. The first amplifier stage features a programmable equalizer, controlled by TX\_EQ, to compensate for high-frequency losses including the SFP connector. The TX\_POL bit controls the signal path polarity. The presence of an AC input signal is indicated by TIN\_LOS.

#### Laser Modulator and DC Generator

The laser modulator provides DC coupled modulation current to the laser diode. TOUTA connects to the laser anode and TOUTC to the laser cathode regardless of the polarity setting at TX\_POL. The modulation current amplitude is set by MODREG[8:0]. The modulation current DAC guarantees laser modulation amplitudes up to 85mA<sub>P-P</sub> (5Ω laser).

The VOUT pin sinks DC current from the laser cathode. The amplitude of the laser DC current is controlled by DCREG[9:0]. The DC current DAC guarantees values up to 57mA.

#### Monitor Diode Input Buffer

The MDIN input stage has adjustable gain settings, allowing a large input signal range. The MDIN\_GAIN[2:0] bits set the transimpedance gain from 156Ω to 2496Ω in octave steps.

Automatic Power Control (APC) Circuitry

The MAX3955 contains circuitry to maintain average optical power using feedback from the monitor diode. The SET\_APC register in conjunction with MDIN\_GAIN controls the set point for average laser power when APC operation is enabled.

Transmit and Receive CDRs

The MAX3955 includes optional clock and data recovery (CDR) for both the Rx and Tx signal paths. The CDRs are designed to attenuate high-frequency jitter. The CDRs can be independently locked to any data rate between 9.95Gbps and 11.32Gbps. Each CDR has a frequency detector (FD) that assists the CDR during acquisition and provides a loss-of-lock (LOL) flag which can be monitored on the internal status registers. A reference clock is not required for acquisition.

Each CDR has an independent pattern generator and loopback capability to facilitate in-system testing. The CDRs can be disabled (default setting) to save power.

DDM

Digital diagnostics monitoring is provided on the MAX3955. This includes reporting of the internal and external temperature, Tx DC-current, Tx average-current, Tx output-power, RSSI current, and internal supply voltage. The MAX3955, when combined with a digital-only  $\mu$ C, will provide compliance with SFF-8472 (Diagnostic Monitoring Interface for Optical Transceivers).

3-Wire Interface

The MAX3955 implements a proprietary 3-wire digital slave interface. The 3-wire interface consists of an SDA bidirectional data line, an SCL clock signal input, and a CSEL chip-select input (active-high). The external master initiates a data transfer by asserting the CSEL pin then generating clock and data signals. All data transfers are most significant bit (MSb) first. See Figure 3 for more information.

Protocol

Each single register operation consists of 16-bit transfers (7-bit address, 1-bit RWN, and 8-bit data). The bus master generates 16 clock cycles to SCL. The RWN bit determines if the cycle is read or write. See Table 1.

Write Mode (RWN = 0)

Writing to a register requires two transactions: a write of 12h to the MODECTRL register to enter setup mode, followed by a write to the target address. For each transaction, the master generates 16 clock cycles at SCL. It outputs a total of 16 bits (MSb first) to SDA at the falling edge of the clock. The master closes the transmission by setting CSEL to 0. Figure 3 shows the 3-wire interface timing.

Table 1. 3-Wire Digital Communication Word Structure

BIT	NAME	DESCRIPTION
15:9	Address	7-Bit Internal Register Address
8	RWN	0: Write; 1: Read
7:0	Data	8-Bit Read or Write Data

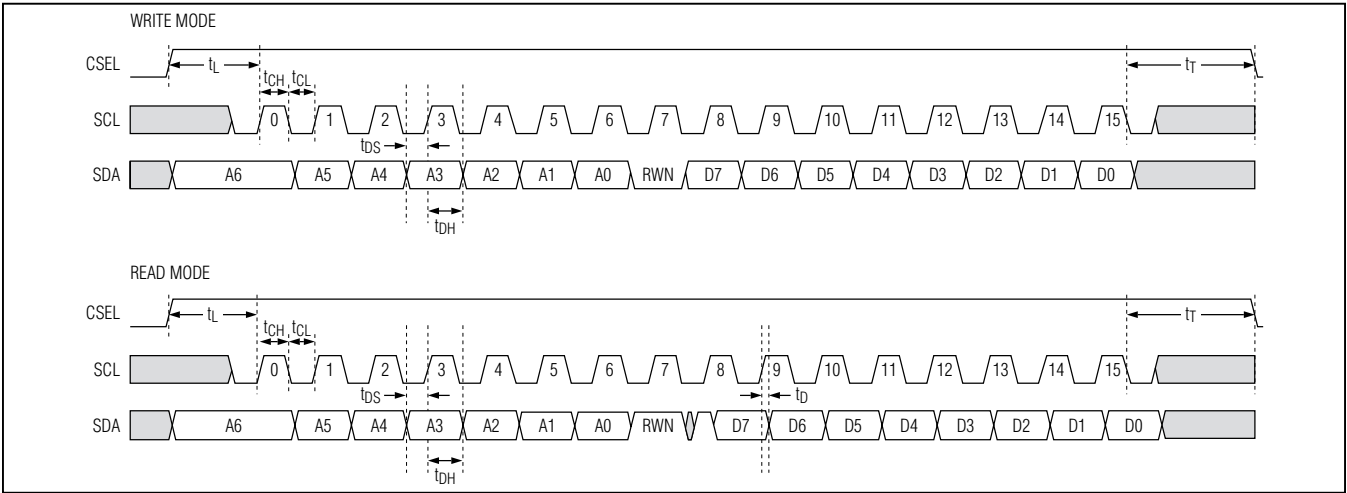


Figure 3. Timing Diagram for 3-Wire Digital Interface

### Read Mode (RWN = 1)

The master generates 16 clock cycles at SCL in total. The master outputs a total of 8 bits (MSb first) to SDA clocked by the falling edge of SCL. SDA is released after the RWN bit has been transmitted. The slave outputs 8 bits of data (MSb first) sampled by the rising edge of SCL. The master closes the transmission by setting CSEL to 0. [Figure 3](#) shows the 3-wire interface timing.

### Block Write Mode (RWN = 0)

The two different modes of operation are described in [Table 2](#).

### Block Read Mode (RWN = 1)

The master initiates the block read mode by accessing any register address and setting the RWN bit to 1. The block read mode starts by stretching the CSEL interval beyond the 16 clock cycles, and it is exited automatically when the master has set CSEL to 0.

### Mode Control

The MAX3955 contains more than 128 registers, which exceeds the addressability of a 7-bit number. Therefore it has two pages (page 0 and page 1) that contain all the

registers. To write to or read from either page, the page must first be selected by writing to the MODECTRL register: 81h to access page 0, 55h to access page 1. Once a page has been selected any further writes or reads will access that page until the MODECTRL is written to the new page. The default page upon POR is page 1.

Setup mode allows the master to write data into any register except the status registers and read-only registers. To enter the setup mode, 12h is written to the [MODECTRL](#) register. The next operation is unrestricted to any writable register. The setup mode is automatically exited after the next operation is finished. This sequence must be repeated if further register writes are necessary.

To speed up the laser control by a factor of 2, the [MODINC](#), [DCINC](#), and [APCINC](#) registers can be updated without writing setup mode to MODECTRL.

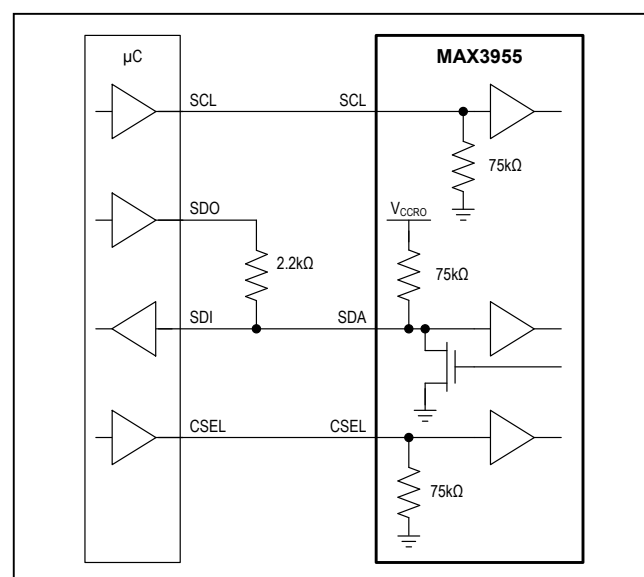
Fault-clear mode allows the clearing of the fault latch, and restarts operation of the device. It is activated by writing 68h to the [MODECTRL](#) register.

**Table 3. MODECTRL Register Settings**

CODE (hex)	CONDITION
00	Normal mode
12	Setup mode
55	Select page 1 mode
68	Fault clear mode
81	Select page 0 mode

**Table 2. Block Write Examples**

BLOCK WRITE MODE 1 (STARTS AT ADDRESS H0x01)	BLOCK WRITE MODE 2 (STARTS AT ANY ADDRESS)
Master sets CSEL to 1	Master sets CSEL to 1
ADDR H0x00 + RWN = 0	ADDR H0x00 + RWN = 0
Data 81h (page 0 access) -or- Data 55h (page 1 access)	Data 81h (page 0 access) -or- Data 55h (page 1 access)
Master sets CSEL to 0	Master sets CSEL to 0
Master sets CSEL to 1	Master sets CSEL to 1
ADDR H0x00 + RWN = 0	ADDR H0x00 + RWN = 0
Data 12h (setup mode)	Data 12h (setup mode)
Data 1 (ADDR H0x01)	Master sets CSEL to 0
Data 2 (ADDR H0x02)	Master sets CSEL to 1
Data 3 (ADDR H0x03)	ADDR H0x0N + RWN = 0
...	Data 1 (ADDR H0x0N)
Data j (ADDR H0xj)	Data 2 (ADDR H0x0N + 1)
Master sets CSEL to 0	Data 3 (ADDR H0x0N + 2)
	...
	Data i (ADDR H0xN + i - 1)
	Master sets CSEL to 0



**Figure 4. Recommended 3-Wire Implementation Using a Generic Microcontroller**



## 2-Wire Communication

### 2-Wire Definition

The following terminology is commonly used to describe 2-wire data transfers.

**Master Device:** The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

**Slave Devices:** Slave devices send and receive data at the master's request.

**Bus Idle or Not Busy:** Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states.

**START Condition:** A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low, while SCL remains high, generates a START condition. See Figure 5 for applicable timing.

**STOP Condition:** A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high, while SCL remains high, generates a STOP condition. See Figure 5 for applicable timing.

**Repeated START Condition:** The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTs are commonly used during read operations to identify a specific register address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See Figure 5 for applicable timing.

**Bit Write:** Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements (Figure 5). Data is shifted into the device during the rising edge of the SCL.

**Bit Read:** At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

**Acknowledgement (ACK and NACK):** An acknowledgement (ACK) or not-acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during

the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing for the ACK and NACK is identical to all other bit writes (Figure 5). An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

**Byte Write:** A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.

**Byte Read:** A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

**Slave Address Byte:** Each slave on the 2-wire bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/W bit in the least significant bit. The MAX3955 responds to the slave address 46h.

The part contains more than 128 registers, which exceeds the addressability of a 7-bit number. Therefore it has two pages (page 0 and page 1) that contain the registers. To write to or read from either page, the page must first be selected by writing to the MODECTRL register: 81h to access Page 0, 55h to access Page 1. Once a page has been selected any further writes or reads will access that page until MODCTRL is written to the new page. The default page upon POR is page 1.

### 2-Wire Protocol

See Figure 5 for an example of 2-wire timing and Figure 6 for an example of 2-wire protocol.

**Writing a Single Byte to the MAX3955:** The master must generate a START condition, write the slave address byte, write R/W = 0, write the MODECTRL address, write 12h (Setup), and generate a STOP condition. This transaction prepares the MAX3955 for a write. Then the master must generate a START condition, write the slave address byte, write R/W = 0, write the register address, write the byte of data, and generate a STOP condition. Remember that the master must read the slave's acknowledgement during all byte write operations.

**Writing Multiple Bytes to the MAX3955:** To write multiple bytes to a slave, the master must generate a START condition, write the slave address byte, write  $R/\overline{W} = 0$ , write the MODECTRL address, write 12h (Setup), and generate a STOP condition. Then the master must generate a START condition, write the slave address byte, write  $R/\overline{W} = 0$ , write the register address, write multiple data bytes, and generate a STOP condition. The device writes multiple bytes with this second write transaction. The MAX3955 contains an address counter that allows data to be written to consecutive addresses without transmitting a register address before each data byte is sent. The address counter limits the write to one page.

For example: A 3-byte write starts at address H0x06 and writes three data bytes (11h, 22h, and 33h) to three con-

secutive addresses. The result is that addresses H0x06, H0x07, H0x08 would contain 11h and 22h, and 33h respectively.

The APCINC, MODINC, and DCINC registers are the only registers in the device that do not require 12h (setup) to be written to MODECTRL before writing to these registers. This allows quicker adjustments of these registers.

**Writing to the APCINC, MODINC, or DCINC register:** The master must generate a START condition, write the slave address byte, write  $R/\overline{W} = 0$ , write the address, write the byte of data, and generate a STOP condition. Remember that the master must read the slave's acknowledgement during all byte write operations.

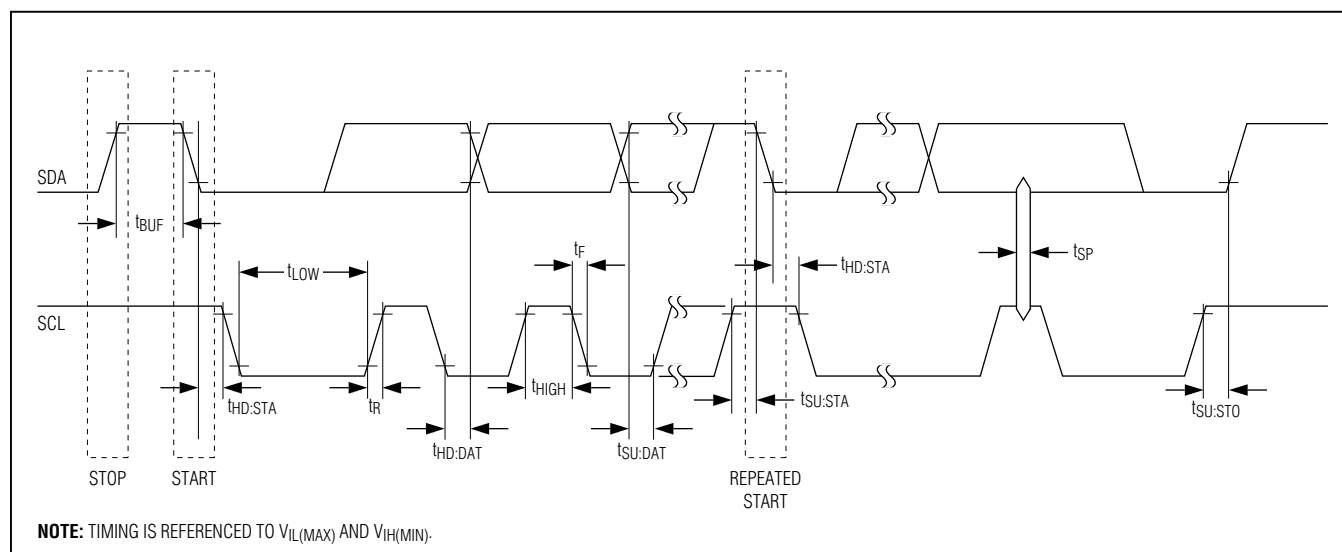


Figure 5. 2-Wire Timing Diagram

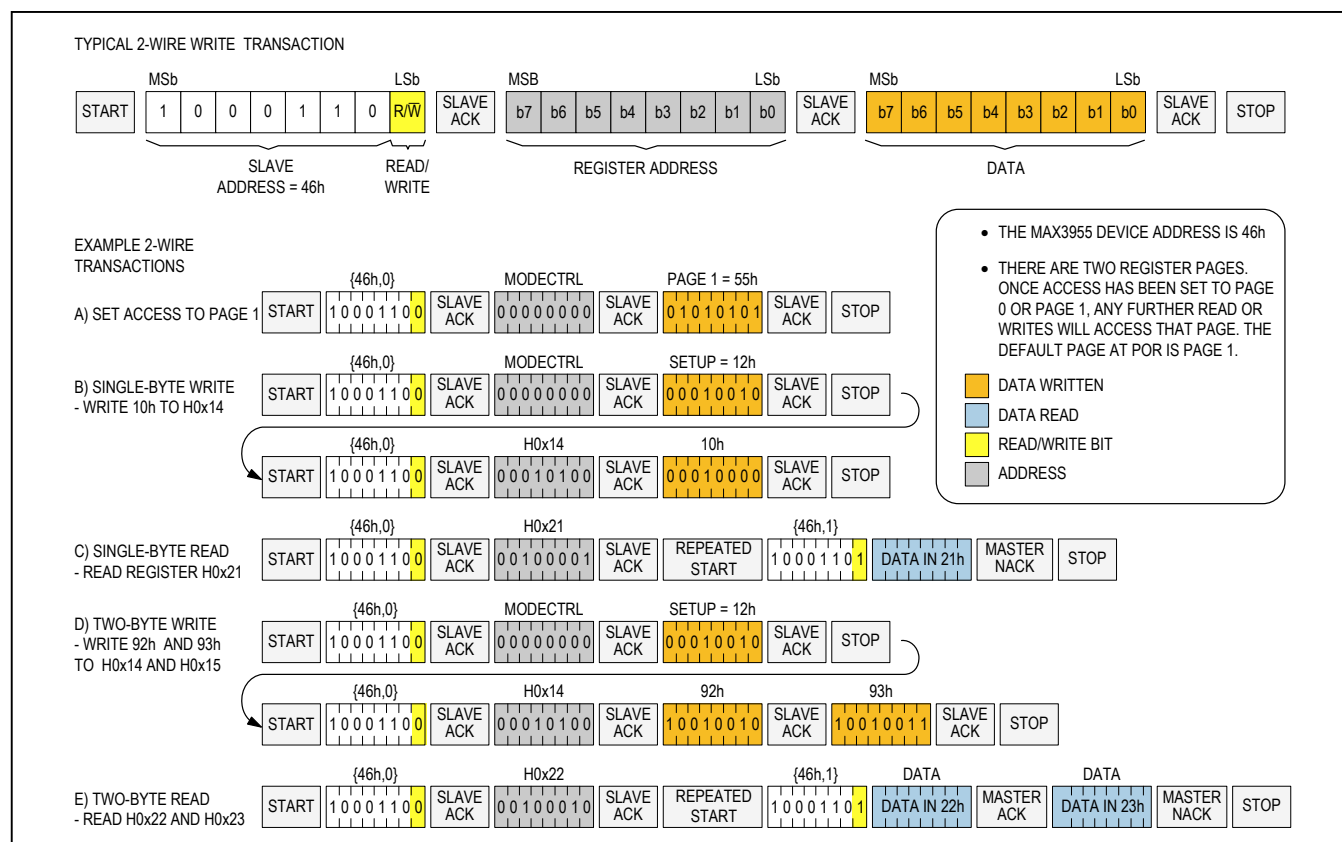


Figure 6. Example 2-Wire Protocol

## Design Procedure

### Load Factory Calibration Constants

After POR has deasserted, the microcontroller must load the individually programmed calibration constants into the calibration registers. This is accomplished by five write commands shown below (writing setup mode is not required for this operation):

WRITE: 55h to H0x00

WRITE: 34h to H0x00

WRITE: 01h to H0x7A

WRITE: 34h to H0x00

WRITE: 03h to H0x7A

**Note:** the CDRs cannot be enabled unless this procedure is performed.

### Power-On Reset (POR)

A power-on-reset circuit provides proper startup sequencing and ensures that the laser is off while the supply

voltage is ramping or below a specified threshold ( $\approx 2.5V$ ). The serial interface can also be used to command a manual reset at any time by setting `SOFT_RESET` = 1, which is identical to a power-on reset. When using `SOFT_RESET`, the MAX3955 transmitter must first be disabled, either by the `DISABLE` pin, by setting `TX_EN` = 0, or by setting `XCVR_EN` = 0. Either power-on or `SOFT_RESET` requires approximately 150 $\mu$ s to complete. POR sets all registers to their defaults. The recommended POR procedure is as follows:

- Because the POR is routed to both the `FAULT` and `INTRPT` pins, the  $\mu$ C should monitor one of these for POR detection in the case of a power-supply brown-out issue.
- If `FAULT` is used by the  $\mu$ C to detect a MAX3955 POR event, a pullup resistor should be used on this pin. This is because `FAULT` defaults to open drain upon POR.

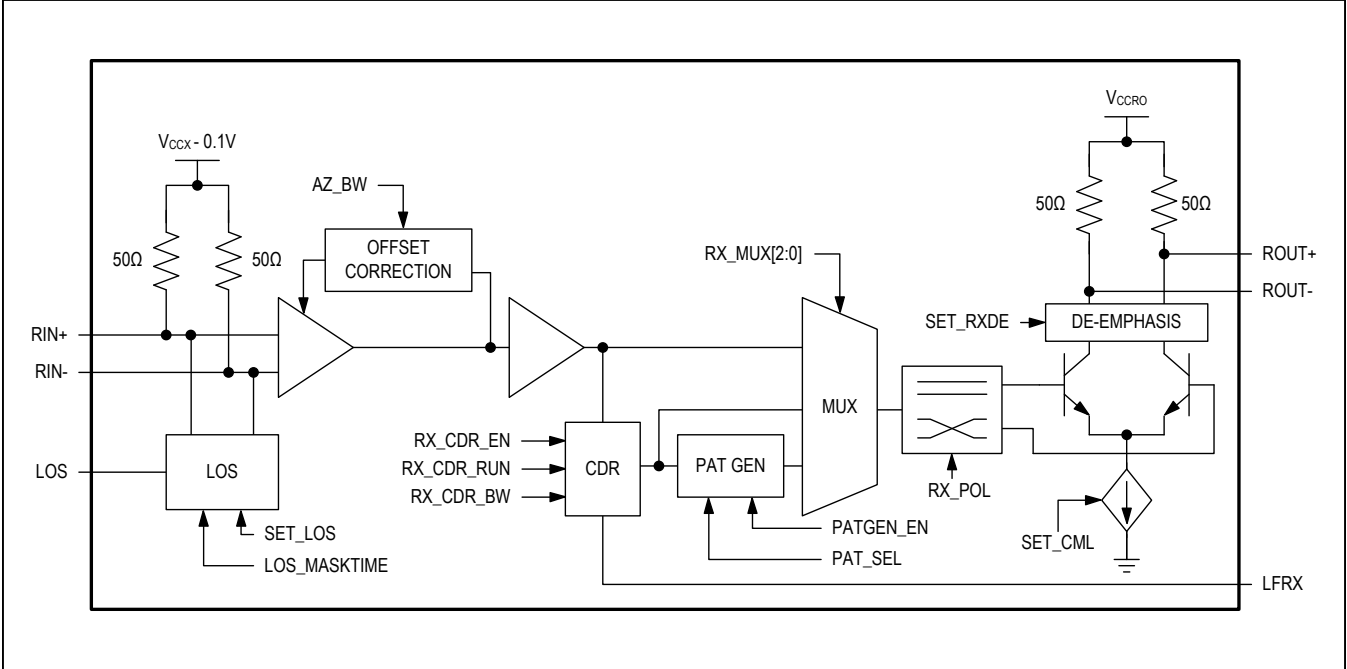


Figure 7. Limiting Amplifier Block Diagram

- Upon POR event detection, the controller initiates 2-wire or 3-wire communication with MAX3955 by repeatedly reading out the TOPSTAT register until the 1-to-0 transition occurs for both PORD and P3VFLAG.
- Once the POR flags have cleared, repeatedly read the TXSTAT1 register until the Tx status flags have cleared. Write a fault clear (68h) to the MODECTRL register to clear any startup-related faults.
- Controller writes commands to load calibration constants into calibration registers then writes/initializes all applicable registers.

11.32Gbps Receiver Details

Figure 7 is a block diagram of the MAX3955 receiver circuitry. It includes the input and output stages, offset-correction block, LOS detector, and CDR.

Offset-Correction Circuitry

The offset-correction circuitry is provided to remove PWD at RIN± and offsets caused by intrinsic mismatch within the amplifier stages. The bandwidth of the offset-correction loop is adjustable and is set by AZ\_BW[1:0]. Table 4 shows the small signal cutoff frequency for each setting.

LOS Circuitry

The LOS block detects the differential amplitude of the input signal and compares it against a threshold controlled by the 7-bit SET\_LOS register. The LOS assert

Table 4. Offset-Correction Loop Cutoff Frequency

AZ_BW[1:0]	CUTOFF FREQUENCY
00	5kHz
01	10kHz (default)
10	20kHz
11	40kHz

threshold is approximately  $1.2\text{mV}_{P-P} \times \text{SET\_LOS}[6:0]$ . The LOS de-assert level is approximately 1.6 times the assert level to avoid LOS chatter. The recommended minimum setting is SET\_LOS[6:0] = 8d.

LOS Output Masking

The LOS output masking feature masks false input signals that can occur after a loss-of-light event in a fiber optic link. These false input signals are caused by some transimpedance amplifier implementations and can corrupt the LOS output and cause system-level link diagnostic errors.

The LOS output masking time can be programmed from 0 to 4.6ms in 36μs steps using the LOS\_MASKTIME[6:0] register. The output mask timer is initiated on the first “0” to “1” LOS signal transition and prevents any further changes in the LOS output signal until the end of the

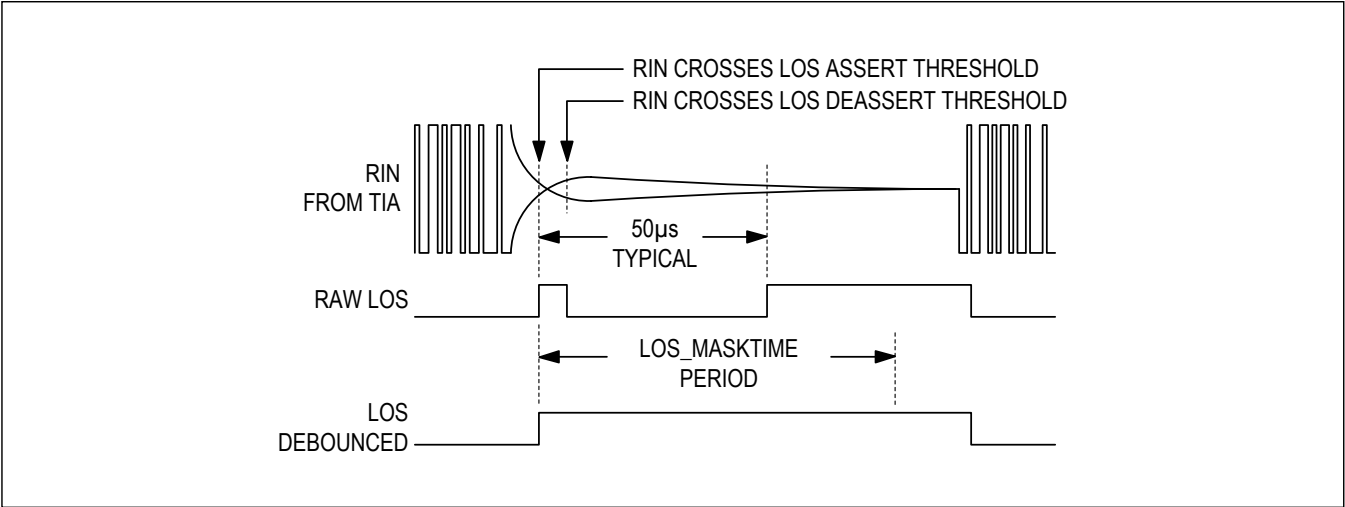


Figure 8. LOS Output Masking

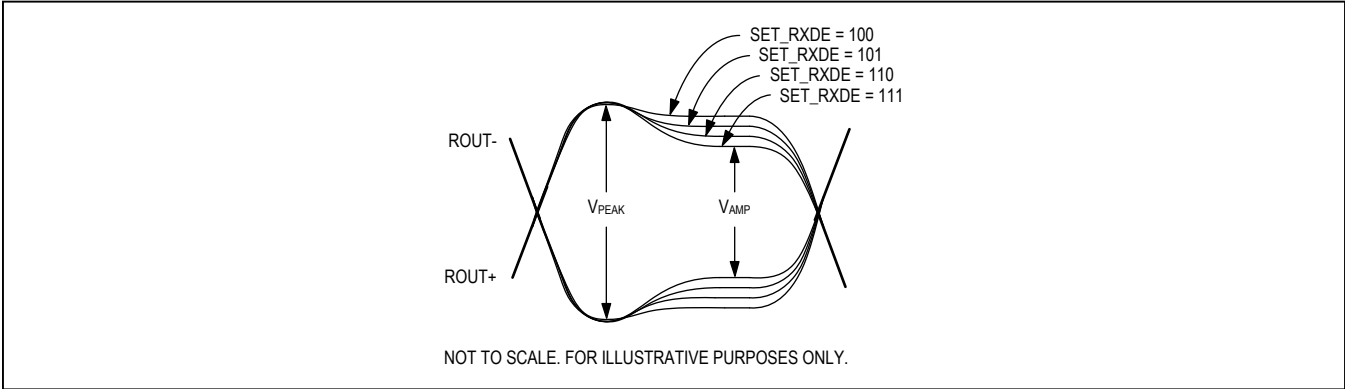


Figure 9. Deemphasis Effect on ROUT Signal

Table 5. ROUT Enable/Disable Mode

XCVR_EN	RX_EN	RO_SHDN	RO_EN	SQ_EN	ROUT MODE
0	X	X	X	X	Disabled, to V <sub>CCRO</sub>
1	0	X	X	X	Disabled, to V <sub>CCRO</sub>
1	1	1	X	X	Output disabled to V <sub>CCRO</sub> . Rx signal still available for Rx → Tx loopback
1	1	0	0	X	Output squelched, to common-mode
1	1	0	1	0	Enabled
1	1	0	1	1	Squelch mode controlled by LOS

**Table 6. ROUT Amplitude Range and Resolution (typical)**

SET_RXDE [2:0]	DIFFERENTIAL OUTPUT AMPLITUDE (mV <sub>P-P</sub> ), V <sub>AMP</sub> in Figure 9	
	SET_CML[4:0] = 12d	SET_CML[4:0] = 31d
0xx	650	1080
100	610	1000
101	570	940
110	530	850
111	480	790

**Table 7. Tx Input Equalization Control**

TX_EQ	BOOST AT 5.1GHz
00	1.5dB
01	3dB
10	4.5dB
11	5.5dB

programmed LOS timing period. The LOS output masking time should be carefully chosen to extend beyond any expected input glitch. See [Figure 8](#).

### Rx Output Stage

The CML output is optimized for a differential 100Ω load and can be squelched to its common mode voltage manually or by the internal LOS status. [Table 6](#) shows the output mode for various conditions and settings.

Deemphasis is included to compensate for FR4 losses and is set by the SET\_RXDE[2:0] bits. [Figure 9](#) illustrates the effects of deemphasis on the output waveform.

### 9.95Gbps to 11.32Gbps Laser Driver

The MAX3955 contains a DC-coupled laser driver designed to drive 5Ω to 10Ω TOSAs from 9.95Gbps to 11.32Gbps. It contains an input buffer with programmable equalization, DC current and modulation current DACs, output driver, and eye safety circuitry. A 2-wire or 3-wire digital interface is used to control these functions.

### Programmable Input Equalization

To compensate for FR4 and connector losses, the MAX3955 has adjustable input equalization as shown in [Table 7](#). When TX\_EQ ≠ 00, the equalizer has an optimized range of 190mV<sub>P-P</sub> to 700mV<sub>P-P</sub> differential at T<sub>IN</sub>±.

### Laser DC Current DAC

The DC current from the MAX3955 is optimized to provide up to 57mA of DC current into a 5Ω to 10Ω laser load with 58.5μA resolution. The current is controlled through the 2-wire or 3-wire interface using the APC loop, or by open-loop control.

Effective DC current seen by the laser (IBIAS) is actually the combination of the DC DAC current generated by the DCREG register (IDC), MODREG register (IMOD) and laser load (R). It is calculated by the formula:

$$I_{DC} = \text{DCDACCurrent}$$

$$I_{DC} = (\text{DCREG}[9:0] + 12) \times 58.5\mu\text{A}$$

$$I_{LD\_DC} = I_{DC} + I_{MOD} \times \left( \frac{R}{(50+R) \times 2} \right)$$

$$I_{BIAS} = I_{LD\_DC} + \frac{I_{LD\_MOD}}{2}$$

If the written value of DCREG[9:2] exceeds DCMAX[7:0], the warning flag is set and DCREG[9:2] remains unchanged. If an attempt is made to set the DCREG to be less than 0, an underflow warning bit DC\_UDFL will flag.

### APC Operation

The automatic power control (APC) loop automatically adjusts DC laser current to maintain constant average current at the MDIN pin. The desired average current at the MDIN pin is set by the SET\_APC register in conjunction with the MDIN\_GAIN value. The MAX3955 measures the high peak and low peak of the MDIN current which represent the P1 and P0 levels of the optical power. These levels are held in the MD1REG and MD0REG registers, respectively. The APC loop will increase/decrease DC laser current to make the following equation true:

$$\text{SET\_APC}[7:0] = \text{MD1REG}[15:8] + \text{MD0REG}[15:8]$$

When the APC loop is closed the average MDIN current is related to SET\_APC and MDIN\_GAIN by the following equation:

$$I_{MDAVG} = \text{SET\_APC}[7:0] \times \frac{1.22\text{mV}}{\text{MDIN\_GAIN}}$$

The largest step size the APC circuitry can apply to DCREG[9:0] is determined by DCINC[4:0]. So if DCINC = 1 then the APC can only increase or decrease DCREG[9:0] by 1 LSB per loop calculation. If DCINC[4:0] = 0, then the APC loop is frozen.

**Flowchart for Setting Up APC operation**

Figure 10 explains the procedure for setting up APC operation on the MAX3955 and Figure 11 shows the optical power for each step in the flowchart process.

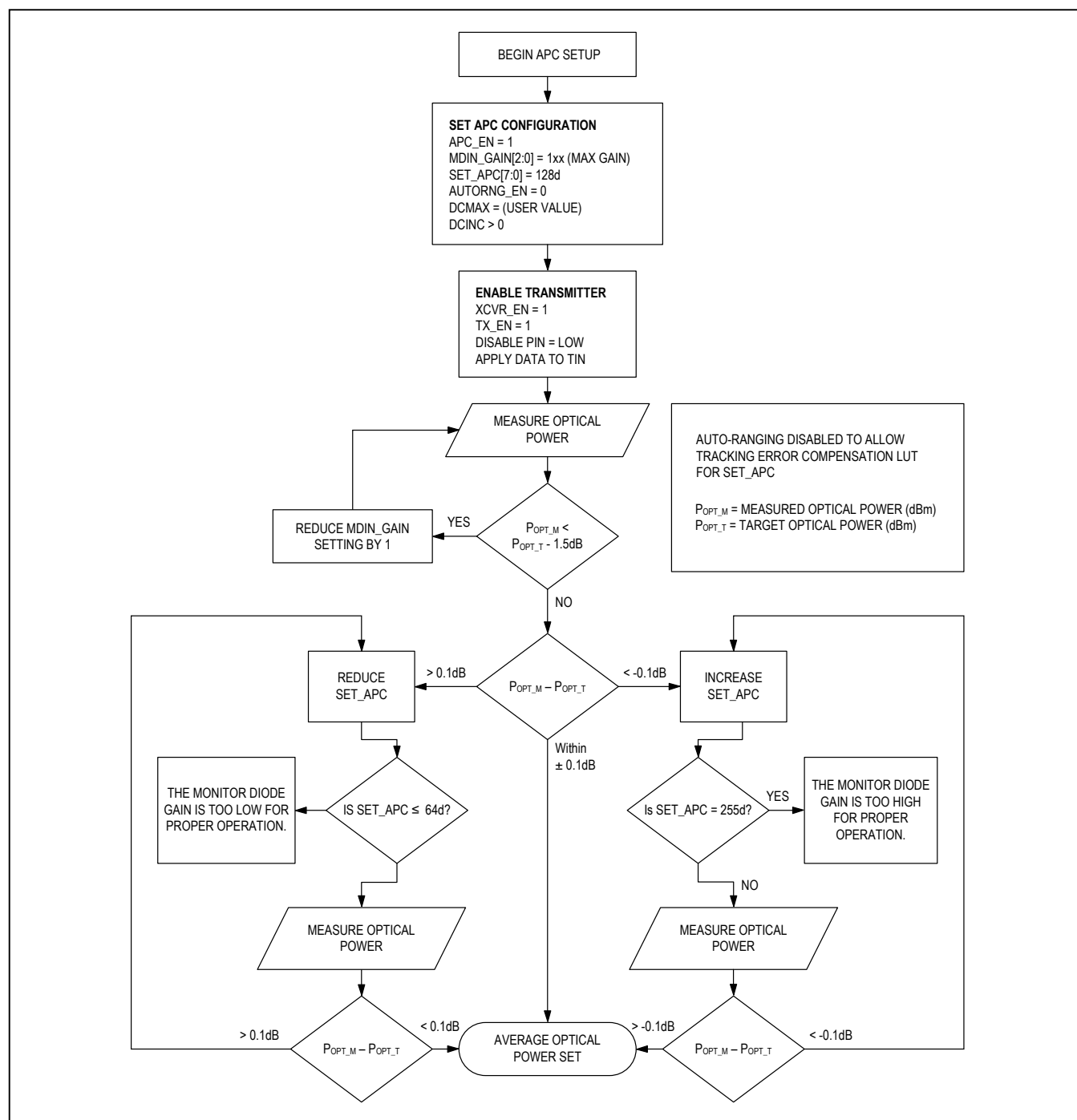


Figure 10. APC Setup Flowchart



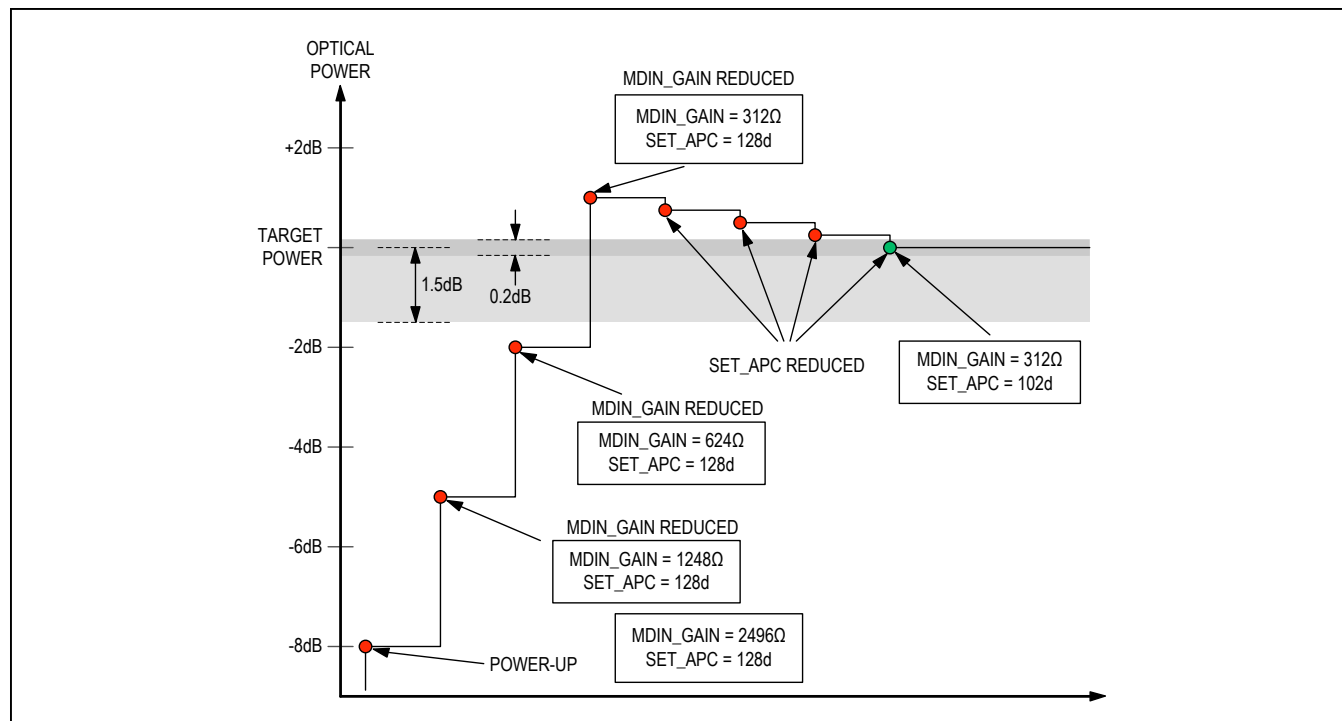


Figure 11. Example of Optical Power During APC Setup

### Open Loop Control of DC Laser Current

To control the DC DAC current manually (not using the APC loop), the APC\_EN bit must be set to 0. DCREG controls the DC DAC current. DCREG cannot be directly written to but can be adjusted by writing to DCINC or SET\_DC (if IBUPDT\_EN=1). Setting IBUPDT\_EN = 1 allows writes to SET\_DC[7:0] to automatically transfer to DCREG[9:2]. The 2 LSBs (bits 1 and 0) of DCREG are initialized to zero after POR and can be updated using the DCINC register. The DCMAX register limits the maximum DCREG[9:2] DAC code.

After initialization, the value of the DCREG register should be updated using the DCINC register. This optimizes cycle time and enhances laser safety. The DCINC[4:0] contains increment information in two's complement notation. Increment values range from -16 LSBs to +15 LSBs.

### Laser Modulation Current DAC

The modulation current from the MAX3955 is optimized to provide up to 90mA of modulation current into a 5Ω laser load with 234μA resolution. The modulation current is

controlled through the 2-wire/3-wire digital interface using the SET\_DC, MODMAX, and MODINC.

Effective modulation current seen by the laser is actually the combination of the DAC current generated by the SET\_MOD register ( $I_{MOD}$ ) and laser load ( $R$ ). It is calculated by the following formulas:

$$I_{MOD} \equiv \text{MODDAC Current}$$

$$I_{MOD} = (\text{SET\_MOD}[8:0] + 16) \times 234\mu\text{A}$$

$$I_{LD\_MOD} = I_{MOD} \times \frac{50\Omega}{R + 50\Omega}$$

### Control of Laser Modulation Current

MODREG controls the modulation DAC current and cannot be written to directly, but it can be adjusted by writing to MODINC or SET\_MOD (if IMUPDT\_EN=1). Setting IMUPDT\_EN = 1 allows writes to SET\_MOD[7:0] to automatically transfer to MODREG[8:1]. The LSB of MODREG is initialized to zero after POR and can be updated using the MODINC register. The MODMAX register limits the maximum MODREG[8:1] DAC code.



**MODINC Usage**

After initialization the value of the SET\_MOD DAC register should be updated using the MODINC register to optimize cycle time and enhance laser safety. The MODINC register is an 8-bit register where the first 5 bits contain the increment information in two's complement notation. Increment values range from -16 LSbs to +15 LSbs. If the updated value of SET\_MOD[8:1] exceeds MODMAX[7:0], the MOD\_OVFL warning flag is set and SET\_MOD[8:1] remains unchanged. If an attempt is made to set the overall modulation DAC code to be less than 0 by using a combination of SET\_MOD register and MODINC register it will cause an underflow warning bit MOD\_UDFL.

**Eye Safety and Output Control Circuitry**

There are several fault indicators associated with certain pins on the MAX3955 (see [Figure 13](#)). If the voltage at

the pin can cause an eye safety concern, then a fault is created and the TX output can be shut off. There is also a status indicator bit associated with each kind of fault condition. The MAX3955 has the capability to keep the transmitter active even if there is a fault condition by masking that fault condition. The status register bits will always flag a fault condition even if the actual fault is masked. When the fault is masked the FAULT pin voltage remains low even when there is a fault condition.

**FAULT and DISABLE Connections to Off-Module Circuitry**

The FAULT and DISABLE pins on the MAX3955 can be connected to circuitry external to the module as shown in [Figure 13](#). Pullup resistors of 4.7kΩ or greater ensure that the DISABLE and FAULT pins will tolerate the maximum difference in the host and module supply voltages.

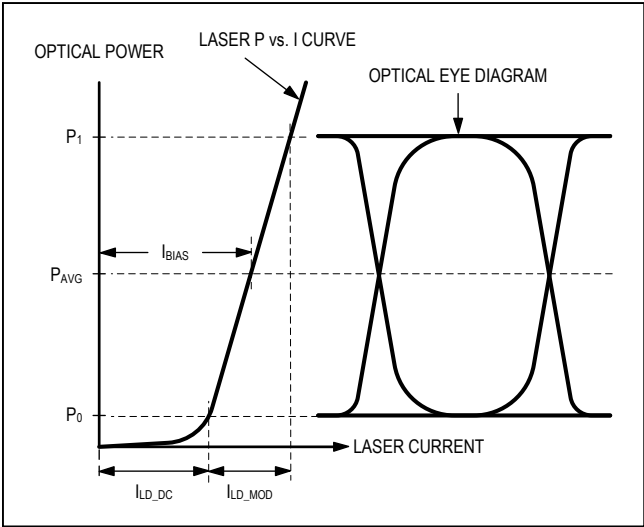


Figure 12. Laser Current Graph

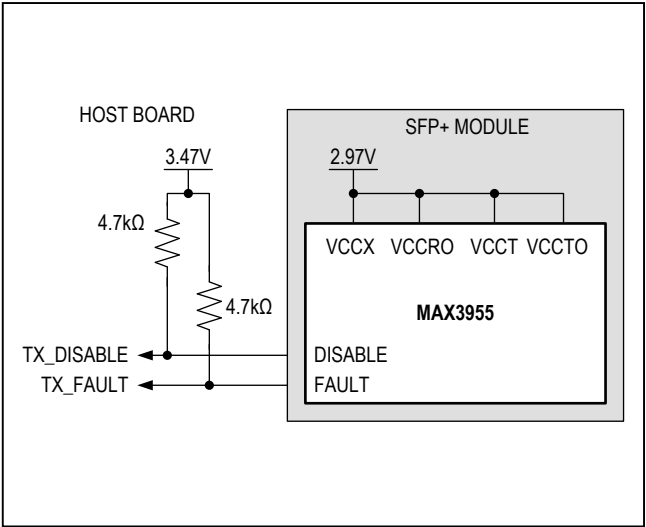


Figure 13. FAULT and DISABLE Connections to Off-Module Circuitry

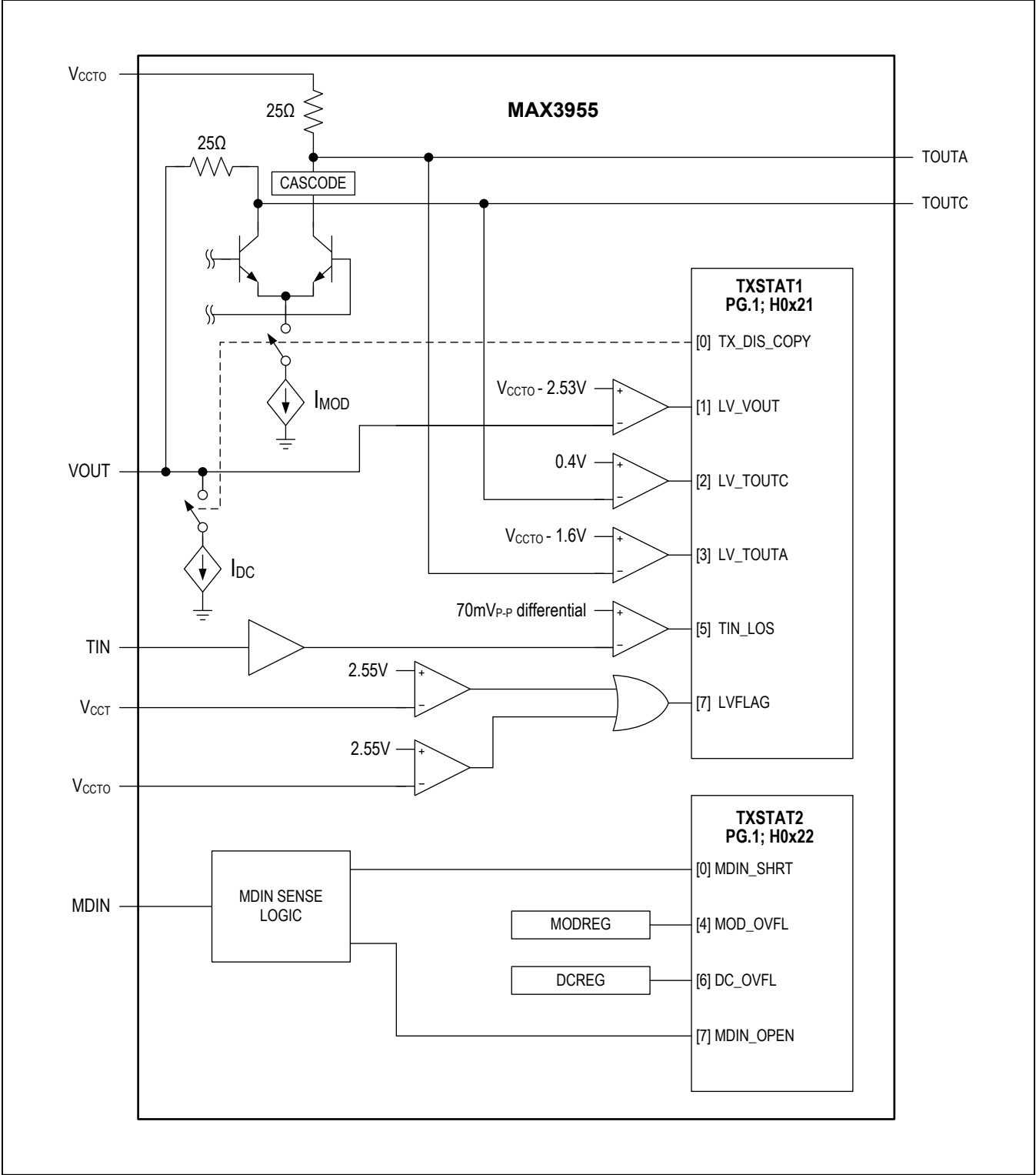


Figure 14. Eye Safety Circuitry

**Table. 8 Circuit Response to Single-Point Faults**

PIN	NAME	SHORT TO V <sub>CC</sub>	SHORT TO GND	OPEN
1	INTRPT	No effect	No effect	No effect
2	FAULT	No effect	No effect	No effect
3	DISABLE	Tx output is off if DIS_POL = 1 (default) No effect if DIS_POL = 0	No effect if DIS_POL = 1 (default) Tx output is off if DIS_POL = 0	Tx output is off if DIS_POL = 1 (default) No effect if DIS_POL = 0
4, 7	V <sub>CCRO</sub>	No effect	Board supply collapsed (Note 19)	No effect (Note 20)
5	ROUT+	No effect	No effect	No effect
6	ROUT-	No effect	No effect	No effect
8	CSEL	No effect	No effect	No effect
9	SCL	No effect	No effect	No effect
10	SDA	No effect	No effect	No effect
11	REGFILT	No effect (Note 18)	Disabled (Note 21)	No effect
12	LFTX	No effect	No effect	No effect
13	TIN+	No effect depending on TIN-amplitude (Notes 18 and 21)	No effect depending on TIN-amplitude (Notes 18 and 21)	No effect depending on TIN-amplitude (Notes 18 and 21)
14	TIN-	No effect depending on TIN+ amplitude (Notes 18 and 21)	No effect depending on TIN+ amplitude (Notes 18 and 21)	No effect depending on TIN+ amplitude (Notes 18 and 21)
15	V <sub>CCT</sub>	No effect	Board supply collapsed (Note 19)	Disabled (Note 21)
16	LFRX	No effect	No effect	No effect
17	MDIN	No effect (Note 21)	No effect (Note 21)	No effect (Note 21)
18	V <sub>CCTO</sub>	No effect	LVFLAG flag asserted, laser diode is off (Note 21)	LVFLAG flag asserted, laser diode is off (Note 21)
19	TOUTA	No effect	Disabled (Note 21)	Laser modulation current is reduced or disabled (Note 21)
20	TOUTC	Laser diode is off	Disabled (Note 21)	Laser modulation current is reduced or disabled (Note 21)
21	VOUT	I <sub>DC</sub> is on, but not delivered to laser; no fault.	Disabled (Note 21)	Disabled (Note 21)
22	TGND	No effect	No effect	No effect
23	TSNS	No effect	No effect	No effect
24	RSSI	No effect	No effect	No effect
25	BADC	No effect	No effect	No effect
26	I.C.	No effect	No effect	No effect
27, 30	V <sub>CCX</sub>	No effect	Board supply collapsed (Note 19)	No effect (Note 20)
28	RIN-	No effect	No effect	No effect
29	RIN+	No effect	No effect	No effect

Table. 8 Circuit Response to Single-Point Faults (continued)

PIN	NAME	SHORT TO V <sub>CC</sub>	SHORT TO GND	OPEN
31	I.C.	No effect	No effect	No effect
32	LOS	No effect	No effect	No effect
—	EP	Board supply collapsed (Note 19)	No effect	POR on

**Note 18:** Pin functionality might be affected, which could affect laser power/performance.

**Note 19:** Supply-shortcd current is assumed to be primarily on the circuit board (outside this device) and the main supply is collapsed by the short.

**Note 20:** Redundant path. Normal in functionality but performance could be affected.

**Note 21:** Depending on mask settings this condition can create a fault and shut down the Tx output. Default mask settings used for this table.

**Warning:** Shorted to V<sub>CC</sub> or shorted to ground on some pins can violate the Absolute Maximum Ratings.

DDM

The MAX3955 integrates the monitoring functions required to implement an SFP system, and when combined with a simple digital-only  $\mu$ C the system can comply with the SFF-8472 MSA. It may be desirable for the  $\mu$ C to implement averaging of the DDM results. [Table 9](#) indicates the ADC registers related to DDM.

Transceiver Temperature

The MAX3955 reports both the internal die temperature as well as the external board temperature (requires discrete pnp for sensing). Either may be used to support DDM reporting, however the internal die temperature is subject to self-heating. Programmable scale and offset factors allow the user to fine-tune the reported results. [Figure 15](#) shows how the scale and offset are applied to

the raw temperature data. The MAX3955 reporting format is consistent with the SFF-8472 reporting requirements.

The external temperature may be measured using a discrete PN junction (MMBT3906 pnp transistor recommended). Alternatively, a diode may be used in place of the pnp. During normal operation a current is sourced from the TSNS pin and TGND is internally shorted to ground, so that the base-emitter voltage of the pnp transistor can be measured and the temperature calculated, see [Figure 16](#). The MAX3955 automatically removes the effect of parasitic resistance in series with the sense diode, allowing flexibility in the placement of the diode.

For internal temperature sensing it is recommended to perform a single-point calibration to achieve best performance.

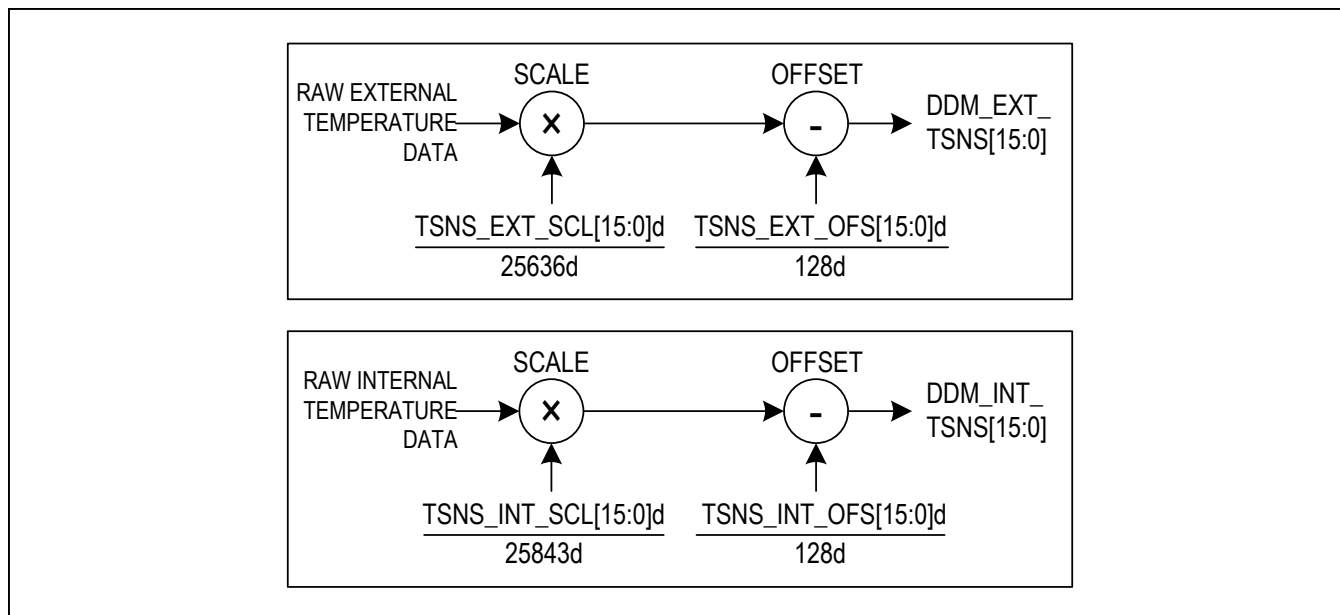


Figure 15. DDM Temperature Scale and Offset

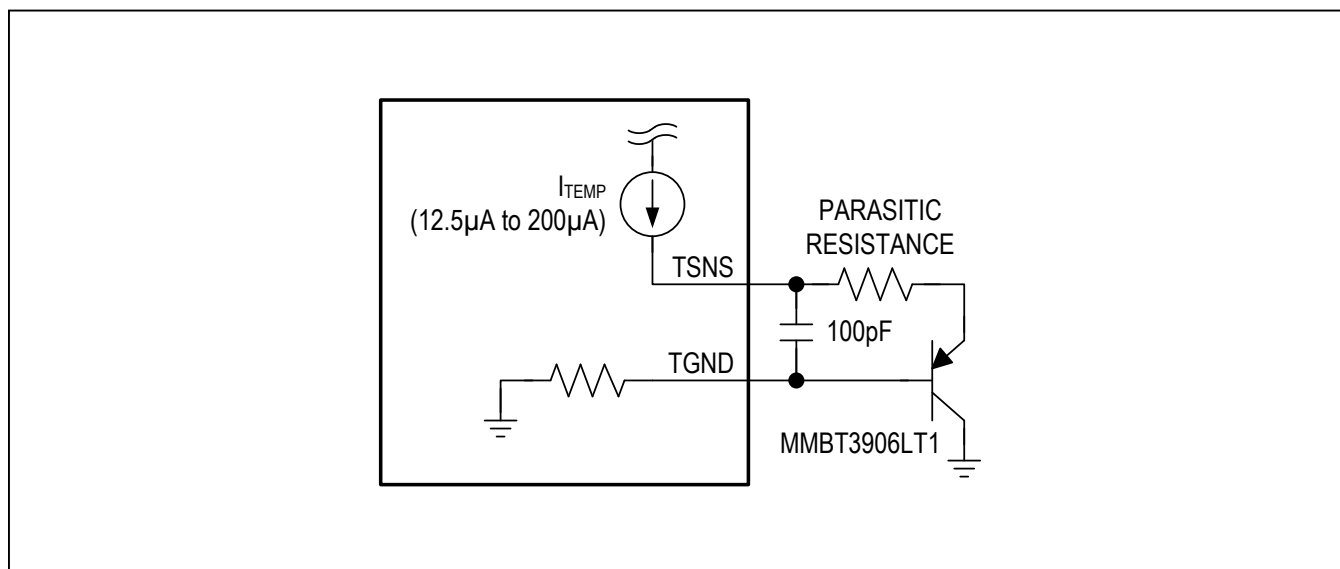


Figure 16. External Temperature Sense Circuit

### Internally Measured Supply Voltage

The MAX3955 reports the voltages of the V<sub>CCX</sub>, V<sub>CCCT</sub>, and V<sub>CCCTO</sub> pins. The result from the MAX3955 is not formatted per SFF-8472 requirements, so the  $\mu$ C must format the data.

The supply voltage results are 12 bits, with a full-scale range of 4.656V. SFF-8472 specifies that the supply voltage be reported as a 16-bit number with LSb = 100 $\mu$ V, so the result of the MAX3955 must be scaled by 1.137mV/100 $\mu$ V = 11.37 in the  $\mu$ C.

### Tx DC Current

The transmit DC value, DDM\_TXRPT[11:0], is a calculation based on the laser DC current and the laser modulation current. Due to the laser and external tuning network, a small portion of the modulation adds to the DC current. It is shown as ILD\_DC in Figure 12. This value is located in the DDM\_TXRPT[11:0] register (when DDM\_TXRPT\_SEL is set to 0) and is calculated as:

$$\text{Tx DC Current} = \text{DDM\_TXRPT}[11:0] = I_{\text{DC}} + \frac{I_{\text{MOD}}}{12.8}$$

where,

$$I_{\text{DC}} = (\text{DCREG}[9:0] + 12) \times 58.5\mu\text{A}$$

$$I_{\text{MOD}} = (\text{MODREG}[8:0] + 16) \times 234\mu\text{A}$$

The LSb size of DDM\_TXRPT[11:0] is 58.5 $\mu$ A. The maximum value of DDM\_TXRPT[11:0] is 1199d (70.1mA), while the minimum value is 17d (1mA).

**NOTE:** The register DDM\_TXRPT[11:0] can take on the value of Tx DC or Tx average. To select Tx DC, set the DDM\_TXRPT\_SEL bit to 0. When the DDM\_TX\_SHDN bit is high, the DDM\_TXRPT values (whether Tx DC or Tx average) are invalid and held at last value before the transmitter was disabled. This includes disable by means of POR, fault, DISABLE pin, TX\_EN = 0, or XCVR\_EN = 0.

### Tx Average Current

The transmit average current is a calculation based on the laser DC current and the laser modulation current. It is shown as IBIAS in Figure 12. This value is located in the DDM\_TXRPT[11:0] register (when DDM\_TXRPT\_SEL is set to 1) and calculated as:

$$\begin{aligned} \text{Tx Average Current} &= \text{DDM\_TXRPT}[11:0] \\ &= I_{\text{DC}} + (0.484 \times I_{\text{MOD}}) \end{aligned}$$

where:

$$I_{\text{DC}} = (\text{DCREG}[9:0] + 12) \times 58.5\mu\text{A}$$

$$I_{\text{MOD}} = (\text{MODREG}[8:0] + 16) \times 234\mu\text{A}$$

The LSb size of DDM\_TXRPT[11:0] is 58.5 $\mu$ A. The maximum value of DDM\_TXRPT[11:0] is 2055d (120.2mA), while the minimum value is 43d (2.5mA).

**NOTE:** The register DDM\_TXRPT[11:0] can take on the value of Tx DC or Tx average. To select Tx average, set the DDM\_TXRPT\_SEL bit to 1. When the DDM\_TX\_SHDN bit is high, the DDM\_TXRPT values (whether Tx DC or Tx average) are invalid and held at last value before the transmitter was disabled. This includes disable by means of POR, fault, DISABLE pin, TX\_EN = 0, or XCVR\_EN = 0.

### Tx Output Power

The transmit power register value, DDM\_TXP[11:0], is a measure of the monitor diode current at the MDIN pin. To convert the register value to the actual Tx Power, use the following equation:

$$P_{\text{AVG}} = \frac{\text{DDM\_TXP}[11:0] \times 977\text{nA}}{K_{\text{MD}}}$$

where  $K_{\text{MD}}$  is the laser diode to monitor diode gain in A/W.

The DDM\_TXP value is updated when the automatic power control ADC completes its averaging of 32 (MDAVG\_CNT=0) or 256 (MDAVG\_CNT=1) samples. These samples occur every 100ns while the transmitter is on, so DDM\_TXP updates occur at every 256  $\times$  100ns = 25.6 $\mu$ s when MDAVG\_CNT=1.

The maximum value of DDM\_TXP[11:0] is 4080d, while the minimum value is 32d.

### Rx Optical Power

The MAX3955 reports the RSSI input current, the conversion between RSSI current and input optical power must be handled within the  $\mu$ C. For PIN diode receivers a simple linear scaling factor may be all that is needed to convert between RSSI current and optical power.

### RSSI Interface

The RSSI pin is an ADC input used to measure RSSI current from the TIA. For optimum power-supply rejection it is recommended to connect 100pF in series with 5 $\Omega$  between the RSSI pin and GND.

The RSSI pin voltage is regulated to 1.62V as shown in Figure 17. The input stage is designed to only sink current. The RSSI will flag an interrupt (DDM\_RSSI\_LO\_FAIL) if current is pulled out of this pin.

Table 9. DDM Register Descriptions (Note 22)

RAW ADC PARAMETER	UPPER REGISTER	LOWER REGISTER	BITS	UPDATE RATE		LSB SIZE	NOTES
				DDM_AVG			
				Off (1x)	On (4x)		
VCCX	DDM_VCCX[11:8]	DDM_VCCX[7:0]	12	10ms	40ms	1.137mV	23
VCCT	DDM_VCCT[11:8]	DDM_VCCT[7:0]	12	10ms	40ms	1.137mV	23
VCCTO	DDM_VCCTO[11:8]	DDM_VCCTO[7:0]	12	10ms	40ms	1.137mV	24
BADC	DDM_BADC[11:8]	DDM_BADC[7:0]	12	10ms	40ms	284.2μV	24
RSSI	DDM_RSSI[15:8]	DDM_RSSI[7:0]	16	10ms	40ms	35.5nA	24
Internal Temperature	DDM_INT_TSNS[15:8]	DDM_INT_TSNS[7:0]	16	10ms	40ms	1/256°C	25
External Temperature	DDM_EXT_TSNS[15:8]	DDM_EXT_TSNS[7:0]	16	10ms	40ms	1/256°C	25
TX DC TX Average	DDM_TXRPT[11:8]	DDM_TXRPT[7:0]	12	26μs		58.48μA	26
TX Power	DDM_TXP[11:8]	DDM_TXP[7:0]	12	26μs		977nA	

- Note 22:** Read both the upper and lower registers in a single block read.
- Note 23:** Unsigned result.
- Note 24:** Unsigned result. Results for negative inputs will be clamped to 00h.
- Note 25:** Upper byte is signed two's complement (-128 to +127), and lower byte is unsigned fractional (0 to 255/256).
- Note 26:** The result may be toggled between Laser DC current and Laser Average current using the DDM\_TXRPT\_SEL bit.

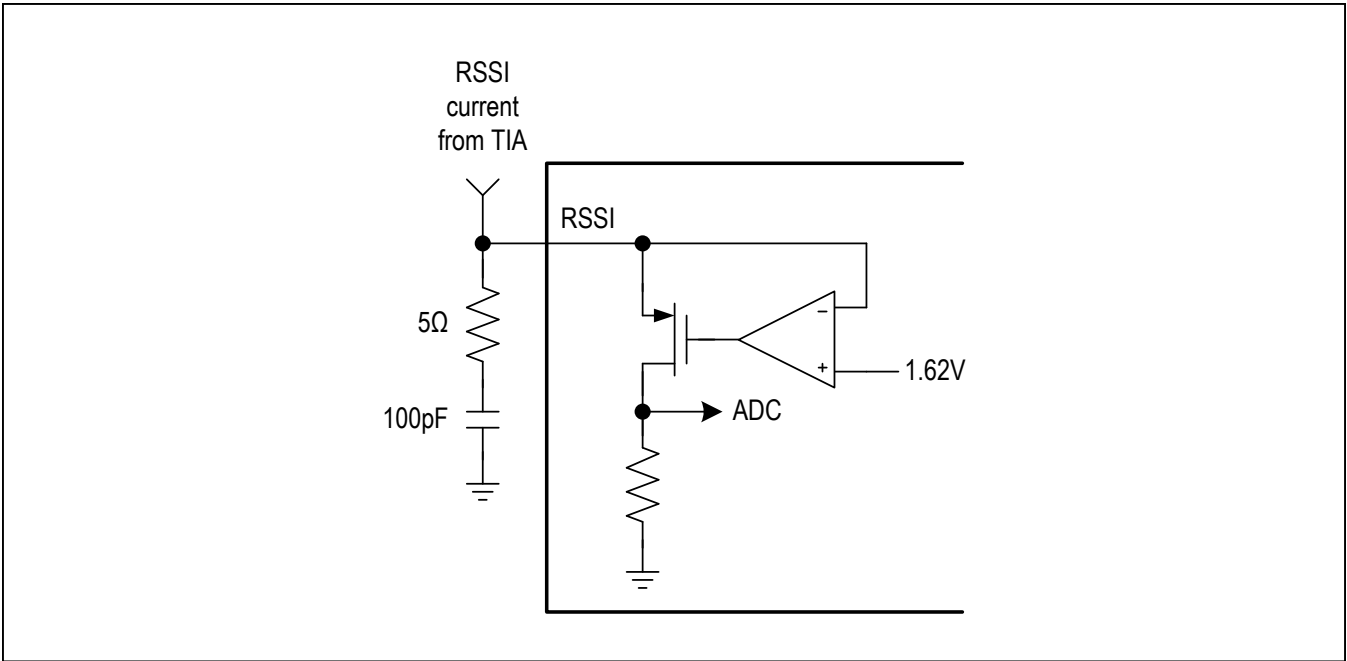


Figure 17. RSSI Circuitry

Transmit and Receive CDRs

The Tx and Rx data paths in the MAX3955 each have a CDR as is shown in [Figure 18](#). The CDRs operate independent of each other and can be individually disabled. Their operational frequency range is from 9.95Gbps to 11.32Gbps.

CDR Loop Bandwidth

The recommended CDR loop bandwidth range is from approximately 2MHz to 16MHz. The loop bandwidth is programmable in 0.5MHz steps. The RX\_CDR\_BW[4:0] bits set the loop bandwidth for the Rx CDR, and the TX\_CDR\_BW[4:0] bits set the loop bandwidth for the Tx CDR.

The loop bandwidth setting should be carefully considered in the design procedure when optimizing for jitter transfer, jitter generation, and jitter tolerance.

Increasing the loop bandwidth will improve the low frequency jitter tolerance but may degrade the total jitter at the output. Decreasing the loop bandwidth may improve the total jitter at the output but will reduce the low-frequency jitter tolerance.

External Loop Filter Capacitor

The external loop filter capacitors, connected between LFRX and GND for the Rx, and LFTX and GND for the Tx, set the damping factor of the CDRs. A capacitor with a relatively low temperature coefficient and low leakage should be used, such as X7R or better. All jitter and lock time specifications are based on an external 0.047μF capacitor with a loop bandwidth setting of RX\_CDR\_BW = TX\_CDR\_BW[4:0] = 0Dh.

Modifying the value of LFRX or LFTX changes the jitter peaking and acquisition time but not the loop bandwidth. A higher value capacitor will decrease the jitter peaking, but may increase the acquisition time. A lower value capacitor will increase the jitter peaking. If the programmed loop bandwidth is low, the capacitor may need to be increased to reduce the jitter peaking.

Table 10. Jitter Transfer Peaking vs. CDR Bandwidth Setting

CDR BANDWIDTH	RX_CDR_BW or TX_CDR_BW	LFRX LFTX	APPROXIMATE JITTER TRANSFER PEAKING
16MHz	11111	0.047μF	0.01dB
8MHz	01111	0.047μF	0.02dB
4MHz	00111	0.047μF	0.03dB
2MHz	00011	0.047μF	0.07dB
2MHz	00011	0.1μF	0.04dB
2MHz	00011	0.22μF	0.02dB



It is not advised to reduce the capacitor value below 0.047 $\mu$ F when using very low loop bandwidths as it will have a significant effect on the peaking. [Table 10](#) shows the jitter transfer peaking vs. CDR bandwidth.

The internal temperature sensor should be monitored while the pattern generators are enabled. Operating above 125°C will adversely affect the device reliability.

The CDR loss-of-lock (LOL) status can be monitored by reading RX\_LOL or TX\_LOL for the Rx and Tx circuitry. These bits can be set to assert the interrupt, and they are both sticky and maskable. The Rx LOL can also be set to control the LOS pin through the LOS\_CFG[1:0] bits.

### Signal Loopback

For testing purposes the Tx input signal can be routed to the Rx output (TIN to ROUT). Likewise, the Rx input signal can be routed to the laser output (RIN to TOUTA/TOUTC). When engaging loopback of TIN to ROUT, ensure that if Rx squelching is disabled. Similarly, if loopback of RIN to TOUT is enabled, the TIN squelch should be disabled (TX\_SQ\_MODE[1:0] = 11). See [Figure 18](#).

### Pattern Generator

The transmitter and receiver blocks contain independent pseudo-random binary sequence (PRBS) genera-

tors. Although they can be independently powered and enabled, if both are operating, they cannot be set to generate different patterns. The patterns available are 27-1 PRBS, 0011 repeating, and 0000 0000 1111 1111 repeating.

The pattern generator receives its clock signal from the CDR if an input data signal is present. If no input data signal is present then the pattern generator can be clocked by the open-loop VCO. To allow the Rx or Tx pattern generator to operate using the open-loop VCO clock, set RX\_PG\_OL or TX\_PG\_OL = 1. The VCO's open-loop frequency is adjusted by RX/TX\_VCO\_FRQ[6:0]. Any time the frequency is adjusted, the RX/TX\_CDR\_RUN bit must be toggled to 0 then to 1 to load the new frequency code. When not using the open-loop VCO mode set RX/TX\_VCO\_FRQ[6:0] = 00h.

### Transmitter Enable, Fault, Interrupt, and TOP-STAT Logic

#### Transmitter Enable Logic

The requirements for the transmitter to be enabled are shown in [Figure 19](#). "Startup complete" is a delay that allows the on-chip systems to become stable after power-up and is typically 100 $\mu$ s.

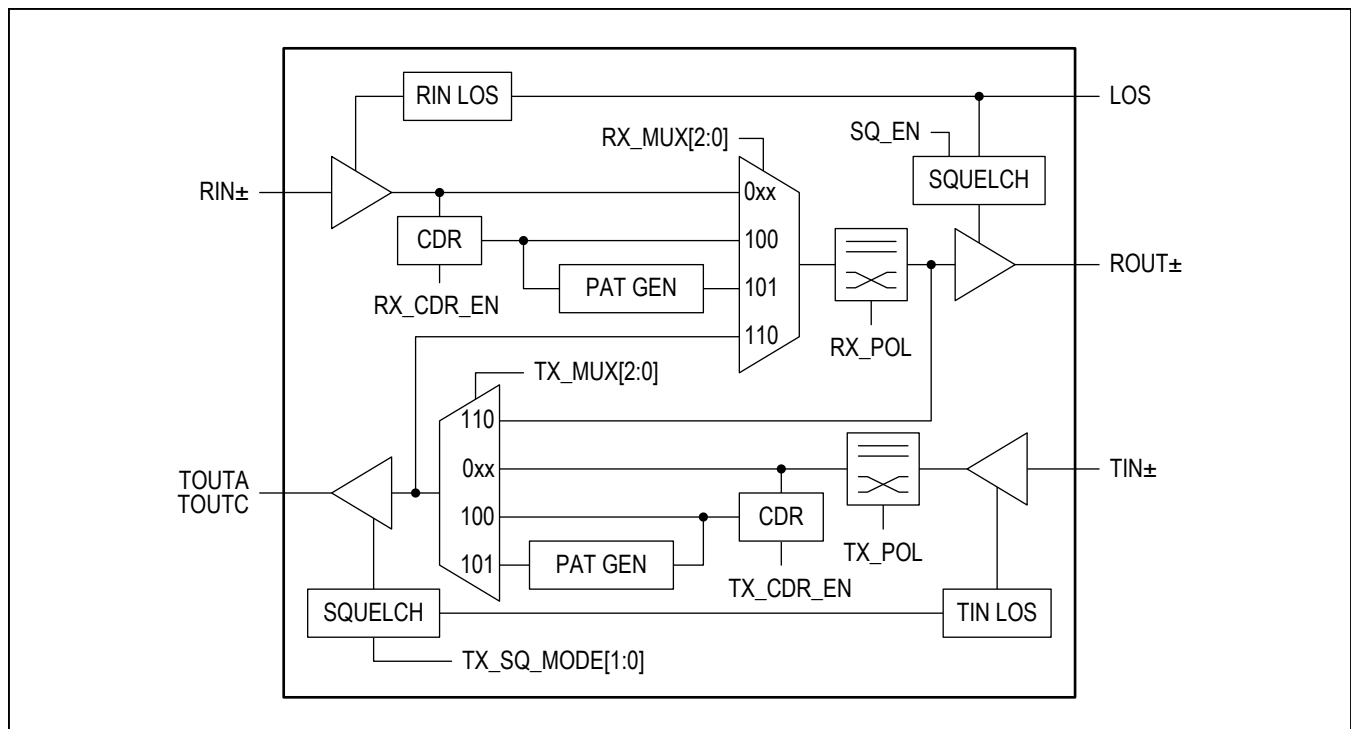


Figure 18. CDR and Loop-Back Block Diagram

### Fault Logic

The fault logic provides detection of transmitter faults with fault indication bits located in the TXSTAT1 and TXSTAT2 registers. Any of the individual faults can be masked using the FMSK1 and FMSK2 registers.

Any fault indication bit, if masked, will flag but will not create a fault condition. When a fault condition occurs and is not masked, the transmitter will shut down. To restart the transmitter after a shutdown has occurred, the source of the fault must be removed and either the DISABLE pin is toggled or the MODECTRL register has 68h written to it. The fault logic is shown in [Figure 20](#).

### Programmable Interrupt Logic

INTRPT is a programmable pin that provides a trigger for real-time monitoring of internal status bits. Status registers RXSTAT, TXSTAT1, TXSTAT2, TXSTAT3, TXSTAT4, and DDMSTAT23 contain the bits that generate interrupt signals. Each of the bits in these registers can be individually masked if desired. If masked, the bit will still flag upon detection of its flag condition but the flag will not propagate to the INTRPT pin or the TOPSTAT register. Additional interrupts are POR and Tx fault. The interrupt logic is shown in [Figure 21](#).

### TOPSTAT Logic

Status registers RXSTAT, TXSTAT1, TXSTAT2, TXSTAT3, TXSTAT4, and DDMSTAT23 feed the TOPSTAT regis-

ter along with signals Tx fault, P3V sense, and POR. TOPSTAT bits PORD and P3VFLAG is set to “1” after power-up or a POR event. These bits are “sticky” therefore need to be read to be cleared. The TOPSTAT logic diagram is shown in [Figure 22](#).

Below are the different ways for using TOPSTAT:

- 1) Using the INTRPT pin
  - a. Mask any undesired flags.
  - b. When INTRPT asserts, read TOPSTAT to narrow down the flag source. The flagged TOPSTAT bit indicates the type of interrupt flagged (APC, DDM, etc...) and which “STAT” register(s) to read to locate the source of the flag, see [Figure 22](#).
  - c. Read the register(s) that triggered the TOPSTAT bit that is flagged. The individual source of the flag will remain flagged in the STAT register until being read.
- 2) Not using the INTRPT pin
  - a. Mask any undesired flags.
  - b. Periodically read TOPSTAT to determine if any interrupts have flagged.
  - c. If a TOPSTAT bit has flagged, read the register(s) that triggered the TOPSTAT bit to determine the specific source of the flag.

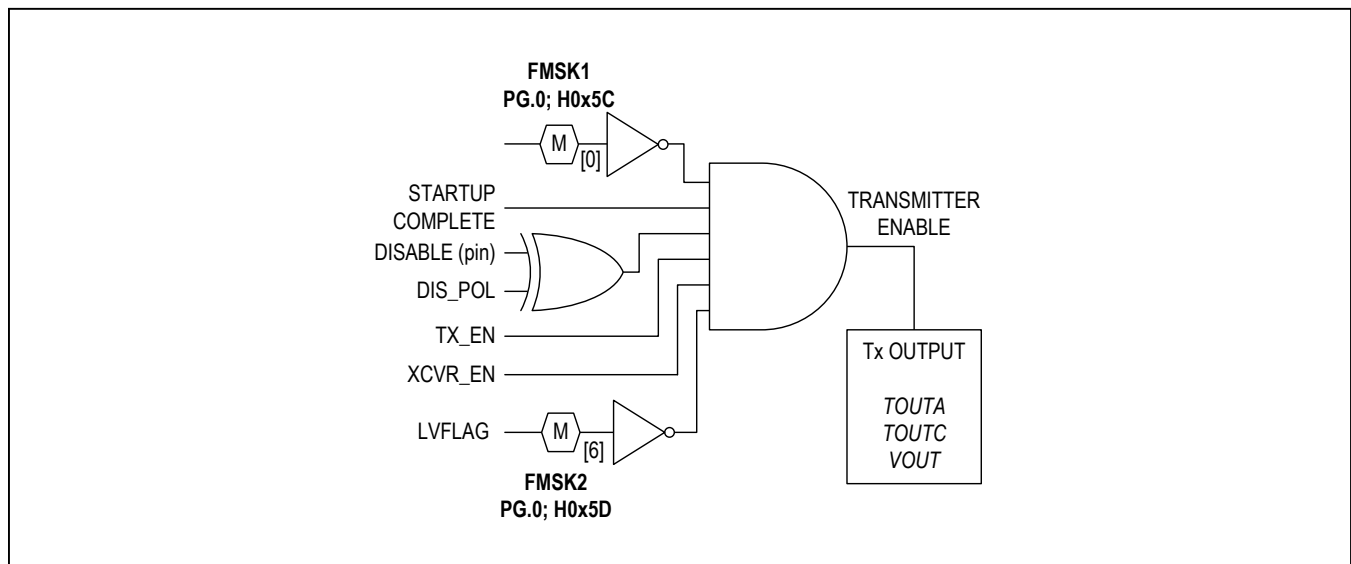


Figure 19. Transmitter Enable Logic

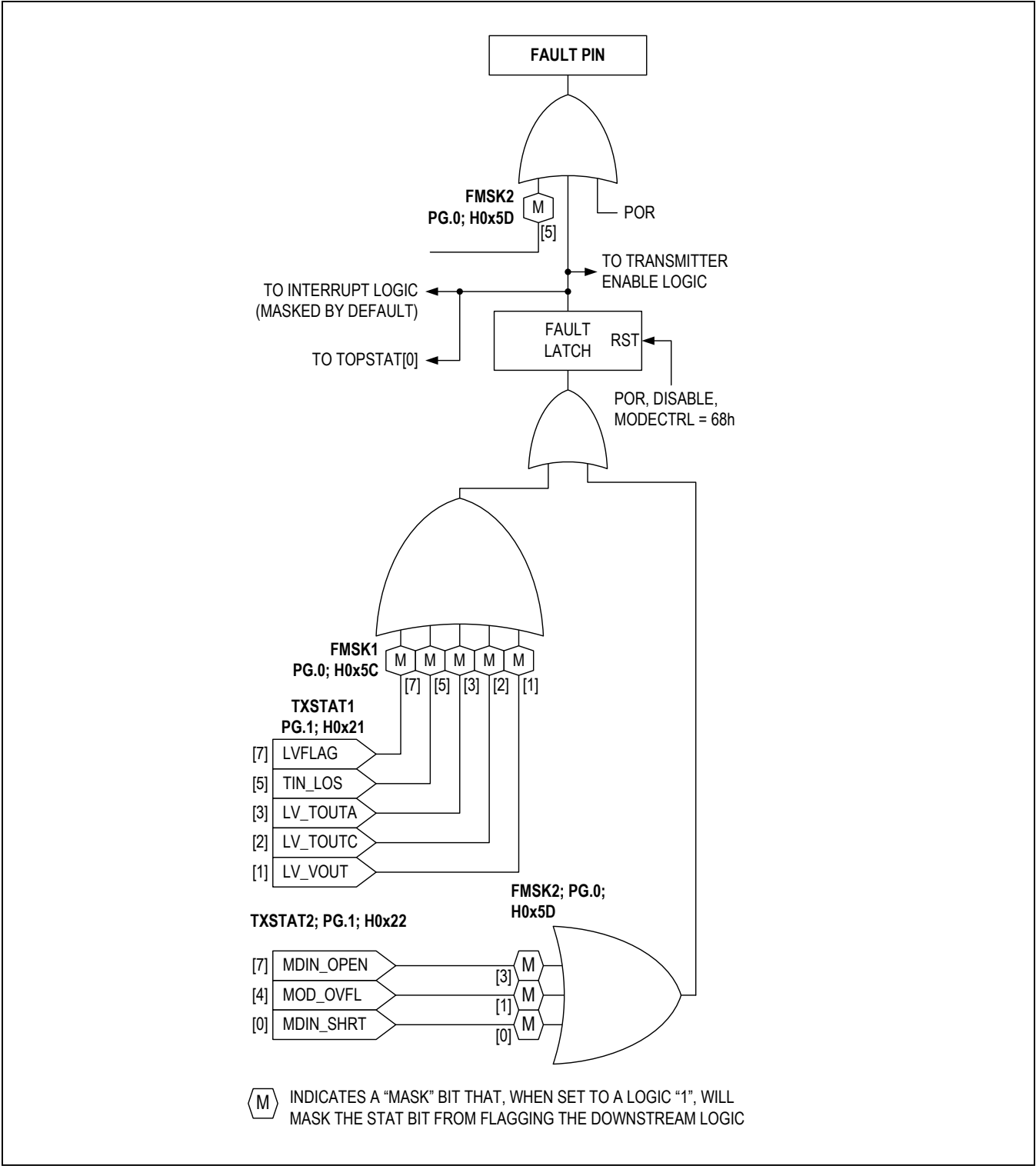


Figure 20. Fault Logic

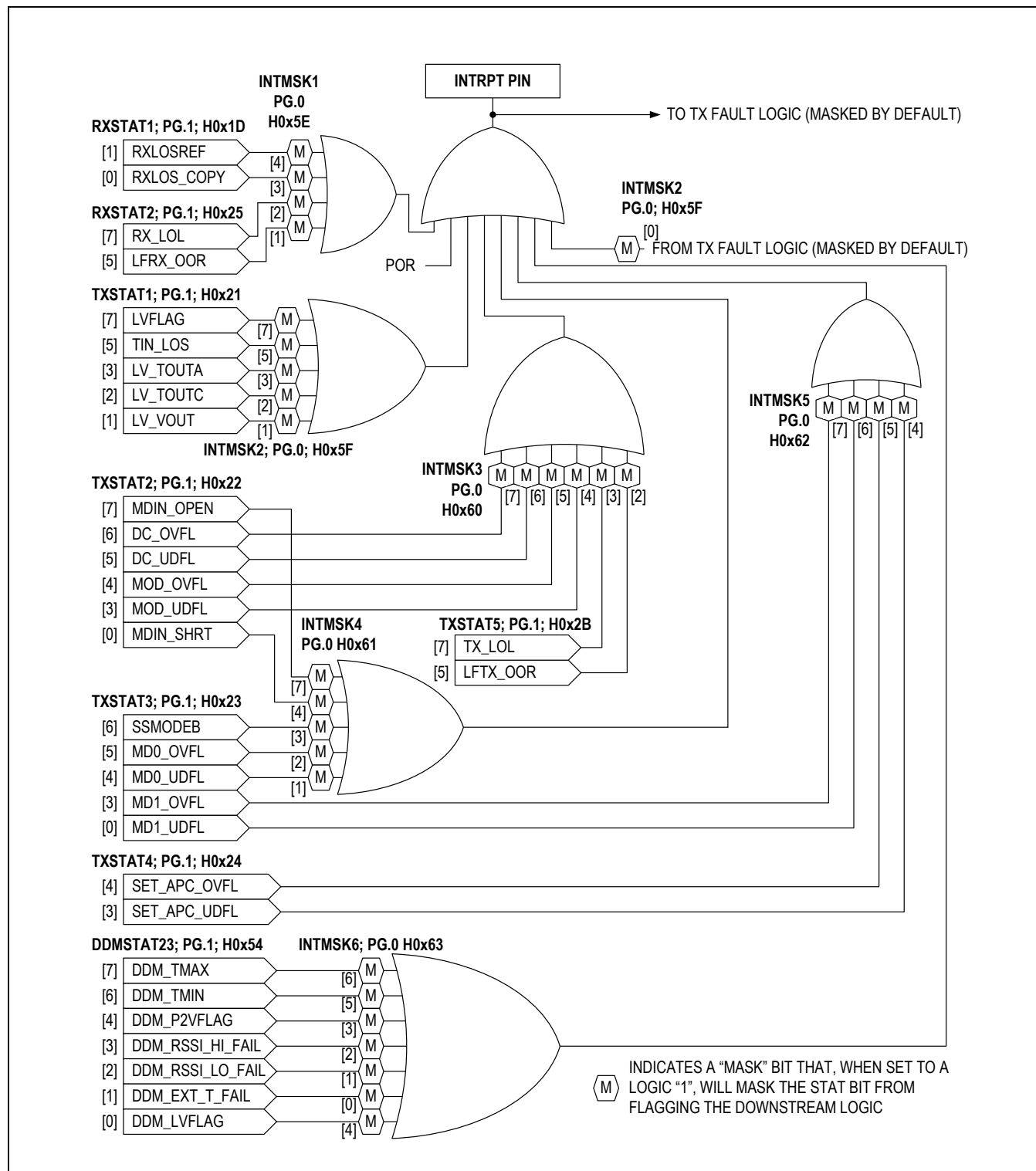


Figure 21. Interrupt Logic

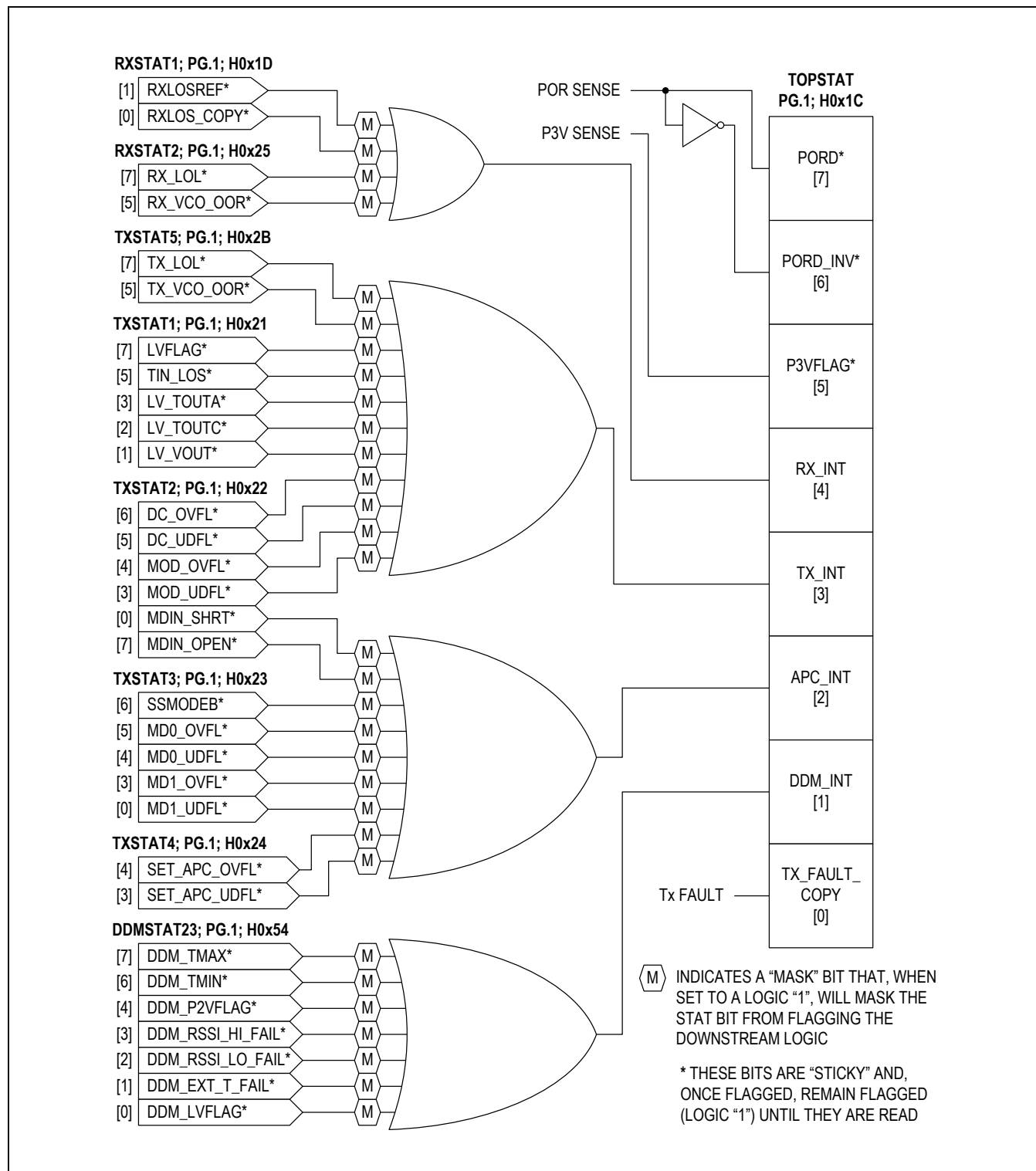


Figure 22. TOPSTAT Logic

Table 12. Registers and Addresses for Page 0

PAGE	ADDRESS	NAME	DEFAULT VALUE	FUNCTION
X	H0x00	MODECTRL	00h	Mode Control Register
0	H0x1A	RXCDRCTRL1	8Dh	Receiver CDR Control Register
0	H0x1B	RXCDRCTRL2	00h	Receiver CDR Control Register
0	H0x2D	TXCDRCTRL1	8Dh	Transmitter CDR Control Register
0	H0x2E	TXCDRCTRL2	00h	Transmitter CDR Control Register
0	H0x3C	PATGENCTRL	00h	Pattern Generator Control Register
0	H0x3F	DDMCTRL1	64h	Upper Byte of External Temp Sensor Scale Factor
0	H0x40	DDMCTRL2	24h	Lower Byte of External Temp Sensor Scale Factor
0	H0x41	DDMCTRL3	88h	Upper Byte of External Temp Sensor Offset Factor
0	H0x42	DDMCTRL4	93h	Lower Byte of External Temp Sensor Offset Factor
0	H0x43	DDMCTRL5	64h	Upper Byte of Internal Temp Sensor Scale Factor
0	H0x44	DDMCTRL6	F3h	Lower Byte of Internal Temp Sensor Scale Factor
0	H0x45	DDMCTRL7	88h	Upper Byte of Internal Temp Sensor Offset Factor
0	H0x46	DDMCTRL8	93h	Lower Byte of Internal Temp Sensor Offset Factor
0	H0x47	DDMCTRL9	80h	DDM Averaging, DC Monitor Control Register
0	H0x49	CALREG1	XXh	Calibration Constant Registers. Do not overwrite. See the <i>Load Factory Calibration Constants</i> in the <i>Design Procedure</i> section for the required calibration constants loading procedure.
0	H0x4A	CALREG2	XXh	
0	H0x4B	CALREG3	XXh	
0	H0x4C	CALREG4	XXh	
0	H0x4D	CALREG5	XXh	
0	H0x4E	RXCTRL1	61h	Receiver Control Register
0	H0x4F	RXCTRL2	E8h	Receiver Control Register
0	H0x50	RXCTRL3	4Bh	Receiver Control Register
0	H0x51	RXCTRL4	C4h	Receiver Control Register
0	H0x52	RXCTRL5	0Bh	Receiver Control Register
0	H0x53	RXCTRL6	A0h	Receiver Control Register
0	H0x55	SET_CML	09h	Receiver Output Voltage DAC
0	H0x56	SET_LOS	10h	Receiver Loss-of-Signal Threshold Setting
0	H0x58	LOS_MASKTIME	00h	LOS Output Masking Time Setting
0	H0x59	TXCTRL1	0Fh	Transmitter Control Register
0	H0x5A	TXCTRL2	12h	Transmitter Control Register
0	H0x5C	FMSK1	70h	Transmitter Fault Mask Register
0	H0x5D	FMSK2	3Fh	Transmitter Fault Mask Register

**Table 12. Registers and Addresses for Page 0 (continued)**

PAGE	ADDRESS	NAME	DEFAULT VALUE	FUNCTION
0	H0x5E	INTMSK1	7Fh	Transmitter Interrupt Mask Register
0	H0x5F	INTMSK2	FFh	Transmitter Interrupt Mask Register
0	H0x60	INTMSK3	FFh	Transmitter Interrupt Mask Register
0	H0x61	INTMSK4	FFh	Transmitter Interrupt Mask Register
0	H0x62	INTMSK5	F0h	Transmitter Interrupt Mask Register
0	H0x63	INTMSK6	7Fh	Transmitter Interrupt Mask Register
0	H0x67	TOPCTRL1	00h	Top-Level Control Register
0	H0x68	TOPCTRL2	00h	Top-Level Control Register

## Register Descriptions

### MAX3955 Mode Control Register (MODECTRL), Address: H0x00 (Page Independent)

BIT	D[7:0]	DESCRIPTION
Bit Name	MODECTRL [7:0]	00h = normal mode—read-only mode with exception of all increment registers (default) 12h = setup mode—enables write permission clears after each write operation 68h = fault clear mode—clears all faults including the fault latch at FAULT pin  There are two register address page select settings: 55h = select page-1 (default) 81h = select page-0  Read-back returns 0 when page-0 is selected and 1 when page-1 is selected
Read/Write	R/W	
POR State	00h Normal Mode and Page 0	
Reset Upon Read	No	

## Receiver CDR Control Register (RXCDRCTRL1), Address: H0x1A (Page 0)

BIT	D7	D6	D5	D[4:0]
Bit Name	RES	LOS_IGN	RES	RX_CDR_BW[4:0]
Read/Write	R/W, Write in setup mode only			
POR State	1	0	0	0 1101

BIT	NAME	DESCRIPTION
D[7]	RES	Reserved
D[6]	LOS_IGN	Rx LOS ignore. Set bit to 1 to allow CDR to acquire regardless of LOS state. 0 = CDR acquisition waits for LOS to deassert (default) 1 = CDR acquisition is active regardless of LOS state
D[5]	RES	Reserved
D[4:0]	RX_CDR_BW[4:0]	Rx CDR bandwidth setting. The total range is 0.5MHz to 16MHz in 0.5MHz steps. The recommended range is 2MHz to 16MHz. 01101 = 7MHz (default)

## Receiver CDR Control Register (RXCDRCTRL2), Address: H0x1B (Page 0)

BIT	D7	D[6:0]
Bit Name	RES	RX_VCO_FRQ[6:0]
Read/Write	R/W, Write in setup mode only	
POR State	0	000 0000
BIT	NAME	DESCRIPTION
D[7]	RES	Reserved
D[6:0]	RX_VCO_FRQ[6:0]	<p>When the Rx pattern generator is set to open-loop mode (RX_PG_OL = 1), these bits set the operating frequency for the VCO.</p> <p><b>NOTE:</b> when RX_PG_OL = 0, these bits should be set back to their default value (000 0000).</p> <p><b>NOTE:</b> when changing the VCO frequency, the RX_CDR_RUN bit must be set to 0 then back to 1 to engage the new VCO frequency setting.</p> <p>000 0000 ≈ 9.1GHz (default)  ...  100 0000 ≈ 10GHz  ...  111 1111 ≈ 11.5GHz</p>



**Transmitter CDR Control Register (TXCDRCTRL1), Address: H0x2D (Page 0)**

BIT	D[7:5]	D[4:0]
Bit Name	RES	TX_CDR_BW[4:0]
Read/Write	R/W, Write in setup mode only	
POR State	100	01101

BIT	NAME	DESCRIPTION
D[7:5]	RES	Reserved
D[4:0]	TX_CDR_BW[4:0]	Tx CDR bandwidth setting. The total range is 0.5MHz to 16MHz in 0.5MHz steps. The recommended range is 2MHz to 16MHz. 01101 = 7MHz (default)

**Transmitter CDR Control Register (TXCDRCTRL2), Address: H0x2E (Page 0)**

BIT	D7	D[6:0]
Bit Name	RES	TX_VCO_FRQ[6:0]
Read/Write	R/W, Write in setup mode only	
POR State	0	000 0000

BIT	NAME	DESCRIPTION
D[7]	RES	Reserved
D[6:0]	TX_VCO_FRQ[6:0]	<p>When the Tx pattern generator is set to open-loop mode (TX_PG_OL = 1), these bits set the operating frequency for the VCO.</p> <p><b>NOTE:</b> when TX_PG_OL = 0, these bits should be set back to their default value (000 0000).</p> <p><b>NOTE:</b> when changing the VCO frequency, the TX_CDR_RUN bit must be set to 0 then back to 1 to engage the new VCO frequency setting.</p> <p>000 0000 ≈ 9.1GHz (default)</p> <p>...</p> <p>100 0000 ≈ 10GHz</p> <p>...</p> <p>111 1111 ≈ 11.5GHz</p>

**Pattern Generator Control Register (PATGENCTRL),  
Address: H0x3C (Page 0)**

BIT	D[7:6]	D[5:4]	D[3:2]	D1	D0
Bit Name	—	PAT_SEL	RES	TX_PATGEN_EN	RX_PATGEN_EN
Read/Write	R/W, Write in setup mode only				
POR State	00	00	00	0	0

BIT	NAME	DESCRIPTION
D[5:4]	PAT_SEL	Selects the pattern for the pattern generators. 00 = 2 <sup>7</sup> -1 PRBS (default) 01 = 0011 repeating pattern 10 = 0000 0000 1111 1111 repeating pattern 11 = reserved
D[3:2]	RES	Reserved
D[1]	TX_PATGEN_EN	Powers the Tx pattern generator block 0 = unpowered (default) 1 = powered
D[0]	RX_PATGEN_EN	Powers the Rx pattern generator block 0 = unpowered (default) 1 = powered

**DDM Control Register (DDMCTRL1), Address: H0x3F (Page 0)**

BIT	D[7:0]	DESCRIPTION
Bit Name	TSNS_EXT_SCL[15:8]	This is the upper byte of the external temperature sense scale factor. This byte, along with the lower byte represents a 16-bit, unsigned value.
Read/Write	R/W Write in setup mode only	
POR State	64h	

**DDM Control Register (DDMCTRL2), Address: H0x40 (Page 0)**

BIT	D[7:0]	DESCRIPTION
Bit Name	TSNS_EXT_SCL[7:0]	This is the lower byte of the external temperature sense scale factor. This byte, along with the upper byte represents a 16-bit, unsigned value.
Read/Write	R/W Write in setup mode only	
POR State	24h	

**DDM Control Register (DDMCTRL3), Address: H0x41 (Page 0)**

BIT	D[7:0]	DESCRIPTION
Bit Name	TSNS_EXT_OFS[15:8]	This is the upper byte of the external temperature offset term. This, along with the lower byte represents a 16-bit, unsigned value. TSNS_EXT_OFS[15:0] is divided by 128 then subtracted from the scaled external-temperature data, see Figure 14.
Read/Write	R/W Write in setup mode only	
POR State	88h	

**DDM Control Register (DDMCTRL4), Address: H0x42 (Page 0)**

BIT	D[7:0]	DESCRIPTION
Bit Name	TSNS_EXT_OFS[7:0]	This is the lower byte of the external temperature offset term. This, along with the upper byte represents a 16 bit, unsigned value. TSNS_EXT_OFS[15:0] is divided by 128 then subtracted from the scaled external-temperature data, see Figure 14.
Read/Write	R/W Write in setup mode only	
POR State	93h	

**DDM Control Register (DDMCTRL5), Address: H0x43 (Page 0)**

BIT	D[7:0]	DESCRIPTION
Bit Name	TSNS_INT_SCL[15:8]	This is the upper byte of the internal temperature scale factor. This, along with the lower byte represents a 16-bit, unsigned value.
Read/Write	R/W Write in setup mode only	
POR State	64h	

**DDM Control Register (DDMCTRL6), Address: H0x44 (Page 0)**

BIT	D[7:0]	DESCRIPTION
Bit Name	TSNS_INT_SCL[7:0]	This is the lower byte of the internal temperature scale factor. This, along with the upper byte represents a 16-bit, unsigned value.
Read/Write	R/W Write in setup mode only	
POR State	F3h	

**DDM Control Register (DDMCTRL7), Address: H0x45 (Page 0)**

BIT	D[7:0]	DESCRIPTION
Bit Name	TSNS_INT_OFS[15:8]	This is the upper byte of the internal temperature offset term. This, along with the lower byte represents a 16-bit, unsigned value. TSNS_INT_OFS[15:0] is divided by 128 then subtracted from the scaled internal-temperature data, see Figure 14.
Read/Write	R/W Write in setup mode only	
POR State	88h	

**DDM Control Register (DDMCTRL8), Address: H0x46 (Page 0)**

BIT	D[7:0]	DESCRIPTION
Bit Name	TSNS_INT_OFS[7:0]	This is the lower byte of the internal temperature offset term. This, along with the upper byte represents a 16-bit, unsigned value. TSNS_INT_OFS[15:0] is divided by 128 then subtracted from the scaled internal-temperature data, see Figure 14.
Read/Write	R/W Write in setup mode only	
POR State	93h	

**DDM Control Register (DDMCTRL9), Address: H0x47 (Page 0)**

BIT	D7	D[6:3]	D2	D[1:0]
Bit Name	DDM_AVG	RES	DDM_TXRPT_SEL	RES
Read/Write	R/W, Write in setup mode only			
POR State	1	0000	0	00

BIT	NAME	DESCRIPTION
D[7]	DDM_AVG	Enables DDM averaging. 0 = no averaging 1 = 4x averaging (default)
D[6:3]	RES	Reserved
D[2]	DDM_TXRPT_SEL	Controls what the DDM_TXRPT register reports 0 = Tx DC current monitor (default) 1 = Tx average current monitor
D[1:0]	RES	Reserved

**Calibration Register (CALREG1), Address: H0x49 (Page 0)**

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RES	CAL1[6]	CAL1[5]	CAL1[4]	CAL1[3]	CAL1[2]	CAL1[1]	CAL1[0]
Read/Write	R	R/W, Write in setup mode only						
POR State	0	X	X	X	X	X	X	X

Factory calibrated register. Do not overwrite. Calibration constants must be loaded after POR. See Load Factory Calibration Constants.

**Calibration Register (CALREG2), Address: H0x4A (Page 0)**

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RES	CAL2[6]	CAL2[5]	CAL2[4]	CAL2[3]	CAL2[2]	CAL2[1]	CAL2[0]
Read/Write	R	R/W, Write in setup mode only						
POR State	0	X	X	X	X	X	X	X

Factory calibrated register. Do not overwrite. Calibration constants must be loaded after POR. See Load Factory Calibration Constants.

**Calibration Register (CALREG3), Address: H0x4B (Page 0)**

BIT	D[7:6]	D5	D4	D3	D2	D1	D0
Bit Name	RES	CAL3[5]	CAL3[4]	CAL3[3]	CAL3[2]	CAL3[1]	CAL3[0]
Read/Write	R	R/W Write in setup mode only					
POR State	00	X	X	X	X	X	X

Factory calibrated register. Do not overwrite. Calibration constants must be loaded after POR. See Load Factory Calibration Constants.

**Calibration Register (CALREG4), Address: H0x4C (Page 0)**

BIT	D[7:4]	D3	D2	D1	D0
Bit Name	RES	CAL4[3]	CAL4[2]	CAL4[1]	CAL4[0]
Read/Write	R	R/W, Write in setup mode only			
POR State	0000	X	X	X	X

Factory calibrated register. Do not overwrite. Calibration constants must be loaded after POR. See Load Factory Calibration Constants.

**Calibration Register (CALREG5), Address: H0x4D (Page 0)**

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	CAL5[7]	CAL5[6]	CAL5[5]	CAL5[4]	CAL5[3]	CAL5[2]	CAL5[1]	CAL5[0]
Read/Write	R/W, Write in setup mode only							
POR State	X	X	X	X	X	X	X	X

Factory calibrated register. Do not overwrite. Calibration constants must be loaded after POR. See Load Factory Calibration Constants.

## Receiver Control Register (RXCTRL1), Address: H0x4E (Page 0)

BIT	D7	D6	D5	D4	D3	D[2:1]	D0
Bit Name	RES	RX_EN	RX_OUT_EN	SQ_EN	RX_OUT_SHDN	RES	RX_POL
Read/Write	R	R/W, Write in setup mode only					
POR State	0	1	1	0	0	00	1

BIT	NAME	DESCRIPTION
D[7]	RES	Reserved
D[6]	RX_EN	Enables Rx core circuitry 0 = disabled – powers down the entire Rx section 1 = enabled (default)
D[5]	RX_OUT_EN	This bit directly controls the mode of the Rx output stage 0 = disabled to common-mode voltage 1 = enabled (default)
D[4]	SQ_EN	This bit enables control of the Rx output stage by means of LOS event 0 = disabled (default) 1 = enabled LOS event disables the Rx output stage to common-mode
D[3]	RX_OUT_SHDN	Powers down Rx output stage only 0 = normal (default) 1 = powered down
D[2:1]	RES	Reserved. Must be set to 00 for proper operation.
D[0]	RX_POL	Sets polarity of the Rx receiver path 0 = inverted 1 = normal (default)

## Receiver Control Register (RXCTRL2), Address: H0x4F (Page 0)

BIT	D[7:3]	D[2:0]
Bit Name	RES	SET_RXDE[2:0]
Read/Write	R/W, Write in setup mode only	
POR State	11101	000

BIT	NAME	DESCRIPTION
D[7:3]	RES	Reserved. Must be set to 11101 for proper operation.
D[2:0]	SET_RXDE[2:0]	Sets deemphasis for the Rx output stage to compensate for FR4 loss at 10Gbps 0xx = disabled (default) 100 = 1dB deemphasis 101 = 2dB deemphasis 110 = 3dB deemphasis 111 = 4dB deemphasis

## Receiver Control Register (RXCTRL3), Address: H0x50 (Page 0)

BIT	D[7:3]	D[2:1]	D0
Bit Name	RES	AZ_BW[1:0]	RES
Read/Write	R/W, Write in setup mode only		
POR State	01001	01	1

BIT	NAME	DESCRIPTION
D[7:3]	RES	Reserved
D[2:1]	AZ_BW[1:0]	Selects the auto-zero bandwidth 00 = 5kHz 01 = 10kHz (default) 10 = 20kHz 11 = 40kHz
D[0]	RES	Reserved

## Receiver Control Register (RXCTRL4), Address: H0x51 (Page 0)

BIT	D7	D6	D[5:0]
Bit Name	RES	LOS_POL	RES
Read/Write	R/W, Write in setup mode only		
POR State	1	1	000100

BIT	NAME	DESCRIPTION
D[7]	RES	Reserved
D[6]	LOS_POL	Selects the LOS polarity 0 = inverted 1 = normal (default)
D[5:0]	RES	Reserved

## Receiver Control Register (RXCTRL5), Address: H0x52 (Page 0)

BIT	D[7:6]	D[5:4]	D3	D[2:0]
Bit Name	RES	LOS_CFG[1:0]	LOS_EN	RES
Read/Write	R/W, Write in setup mode only			
POR State	00	00	1	011

BIT	NAME	DESCRIPTION
D[7:6]	RES	Reserved
D[5:4]	LOS_CFG[1:0]	LOS pin configuration 00 = LOS (default) 01 = Rx CDR LOL 1x = Rx CDR LOL or LOS
D[3]	LOS_EN	LOS enable <b>NOTE:</b> If LOS is disabled and the Rx CDR is enabled, then LOS_IGN should be set to 1 to allow the CDR to acquire lock. 0 = disabled 1 = enabled (default)
D[2:0]	RES	Reserved

**Receiver Control Register (RXCTRL6), Address: H0x53 (Page 0)**

BIT	D[7:5]	D4	D[3:0]
Bit Name	RES	LOS_PU_EN	RES
Read/Write	R/W, Write in setup mode only		
POR State	101	0	0000

BIT	NAME	DESCRIPTION
D[7:5]	RES	Reserved
D[4]	LOS_PU_EN	Enables active pullup on LOS pin. When enabled the LOS output becomes a push-pull CMOS output. 0 = disabled, open-drain output (default) 1 = enabled, push-pull CMOS output
D[3:0]	RES	Reserved

**Receiver Control Register (SET\_CML), Address: H0x55 (Page 0)**

BIT	D[7:5]	D4	D3	D2	D1	D0
Bit Name	RES	SET_CML[4]	SET_CML[3]	SET_CML[2]	SET_CML[1]	SET_CML[0]
Read/Write	R/W, Write in setup mode only					
POR State	000	0	1	0	0	1

BIT	NAME	DESCRIPTION
D[7:5]	RES	Reserved
D[4:0]	SET_CML[4:0]	Set Rx output amplitude. Amplitudes listed below are valid for SET_RXDE = 0xx 0 0000 = 370mVp-p ... 0 1001 = 600mVp-p (default) ... 1 1111 = 1.08Vp-p



## Receiver Control Register (SET\_LOS), Address: H0x56 (Page 0)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	SET_LOS [6]	SET_LOS [5]	SET_LOS [4]	SET_LOS [3]	SET_LOS [2]	SET_LOS [1]	SET_LOS [0]	RES
Read/Write	R/W, Write in setup mode only							
POR State	0	0	0	1	0	0	0	0

BIT	NAME	DESCRIPTION
D[7:1]	SET_LOS[6:0]	Set LOS threshold. Assert threshold approximately $1.2\text{mV}_{P-P} \times \text{SET\_LOS}[6:0]$ . Deassert threshold is approximately $1.6 \times$ the assert threshold to avoid LOS chatter due to noise. 00 0000 = minimum assert level ... 00 1000 = $9.6\text{mV}_{P-P}$ differential (default) ... 11 1111 = maximum assert level
D[0]	RES	Reserved

## Receiver Control Register (LOS\_MASKTIME), Address: H0x58 (Page 0)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RES	LOS_MASK TIME[6]	LOS_MASK TIME[5]	LOS_MASK TIME[4]	LOS_MASK TIME[3]	LOS_MASK TIME[2]	LOS_MASK TIME[1]	LOS_MASK TIME[0]
Read/Write	R/W, Write in setup mode only							
POR State	0	0	0	0	0	0	0	0

BIT	NAME	DESCRIPTION
D[7]	RES	Reserved
D[6:0]	LOS_MASKTIME[6:0]	Sets masking time for LOS. The LSB size is $36\mu\text{s}$ . 000 0000 = $0\mu\text{s}$ (default)

## Transmitter Control Register (TXCTRL1), Address: H0x59 (Page 0)

BIT	D7	D[6:5]	D4	D3	D[2:1]	D0
Bit Name	LOW_DC_EN	RES	FAULT_PU_EN	FAULT_POL	RES	TX_POL
Read/Write	R/W Write in setup mode only					
POR State	0	00	0	1	11	1

BIT	NAME	DESCRIPTION
D[7]	LOW_DC_EN	Enables low-DC current mode when low laser threshold current is needed 0 = disabled (default) 1 = enabled
D[6:5]	RES	Reserved
D[4]	FAULT_PU_EN	Enables active pullup on FAULT pin. When enabled the FAULT output becomes a push-pull CMOS output. 0 = disabled, open-drain output (default) 1 = enabled, push-pull CMOS output
D[3]	FAULT_POL	Sets FAULT pin polarity 0 = inverted 1 = normal (default)
D[2:1]	RES	Reserved
D[0]	TX_POL	Sets TX data path polarity 0 = inverted 1 = normal (default)

## Transmitter Control Register (TXCTRL2), Address: H0x5A (Page 0)

BIT	D[7:5]	D4	D3	D2	D1	D0
Bit Name	RES	DIS_POL	TX_EQ[1]	TX_EQ[0]	TX_SQ_MODE[1]	TX_SQ_MODE[0]
Read/Write	R/W Write in setup mode only					
POR State	000	1	0	0	1	0

BIT	NAME	DESCRIPTION
D[7:5]	RES	Reserved
D[4]	DIS_POL	Sets polarity of DISABLE pin 0 = inverse 1 = normal (default)
D[3:2]	TX_EQ[1:0]	Selects Tx input equalization 00 = 1.5dB boost at 5.1GHz (default) 01 = 3.0dB boost at 5.1GHz 10 = 4.5dB boost at 5.1GHz 11 = 5.5dB boost at 5.1GHz
D[1:0]	TX_SQ_MODE[1:0]	Tx output squelch-modes during TIN LOS event 00 = no current into TOUTC and VOUT pins (no laser current) 01 = sink current set to a mid-level corresponding to $P_{AVG}$ at current temperature 10 = modulation current is disabled but APC loop remains active (default) 11 = squelch disabled

**Fault Mask Control Register (FMSK1), Address: H0x5C (Page 0)**

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	FMSK_LVFLAG	RES	FMSK_TIN_LOS	RES	FMSK_TOUTA	FMSK_TOUTC	FMSK_VOUT	FMSK_TXFLT
Read/Write	R/W Write in setup mode only							
POR State	0	1	1	1	0	0	0	0

BIT	NAME	DESCRIPTION
D[7]	FMSK_LVFLAG	Mask LVFLAG fault condition on V <sub>CCTO</sub> pin 0 = no mask (default) 1 = mask
D[6]	RES	Reserved
D[5]	FMSK_TIN_LOS	Mask TX input LOS fault condition 0 = unmasked 1 = mask (default)
D[4]	RES	Reserved
D[3]	FMSK_TOUTA	Mask LV_TOUTA fault condition 0 = no mask (default) 1 = mask
D[2]	FMSK_TOUTC	Mask LV_TOUTC fault condition 0 = no mask (default) 1 = mask
D[1]	FMSK_VOUT	Mask LV_VOUT fault condition 0 = no mask (default) 1 = mask
D[0]	FMSK_TXFLT	Masks the FAULT latch signal, which controls the output stage on/off behavior. 0 = No mask (default) 1 = Mask When FMSK1[0] = 1, output stage behavior becomes independent of FAULT conditions.

**Fault Mask Control Register (FMSK2), Address: H0x5D (Page 0)**

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	—	FMSK_ LVFLAG_ OUTDIS	FMSK_ INTRPT_ FAULT	RES	FMSK_ MDIN_OPEN	RES	FMSK_ MOD_OVFL	FMSK_ MDIN_SHRT
Read/Write	R/W Write in setup mode only							
POR State	0	0	1	1	1	1	1	1

BIT	NAME	DESCRIPTION
D[6]	FMSK_LVFLAG_OUTDIS	Mask Tx output disable during LVFLAG event 0 = no mask (default) 1 = mask
D[5]	FMSK_INTRPT_FAULT	Mask logic OR combination of interrupt event and fault event at FAULT pin. 0 = no mask 1 = mask (default)
D[4]	RES	Reserved
D[3]	FMSK_MDIN_OPEN	Mask MDIN_OPEN fault condition 0 = no mask 1 = mask (default)
D[2]	RES	Reserved
D[1]	FMSK_MOD_OVFL	Mask MOD_OVFL fault condition. Threshold set by MODMAX register. 0 = no mask 1 = mask (default)
D[0]	FMSK_MDIN_SHRT	Mask MDIN_SHRT fault condition 0 = no mask 1 = mask (default)

**Interrupt Mask Control Register (INTMSK1), Address: H0x5E (Page 0)**

BIT	D[7:5]	D4	D3	D2	D1	D0
Bit Name	RES	INTMSK_ RXLOSREF	INTMSK_ RXLOS	INTMSK_ RX_LOL	INTMSK_ LFRX_OOR	RES
Read/Write	R/W Write in setup mode only					
POR State	011	1	1	1	1	1

BIT	NAME	DESCRIPTION
D[7:5]	RES	Reserved
D[4]	INTMSK_ RXLOSREF	Mask RXLOSREF interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[3]	INTMSK_ RXLOS	Mask RXLOS copy from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[2]	INTMSK_ RX_LOL	Mask RX_LOL from INTRPT pin 0 = no mask 1 = mask (default)
D[1]	INTMSK_ LFRX_OOR	Mask LFRX_OOR from INTRPT pin 0 = no mask 1 = mask (default)
D[0]	RES	Reserved

**Interrupt Mask Control Register (INTMSK2), Address: H0x5F (Page 0)**

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	INTMSK_ LVFLAG	RES	INTMSK_ TIN_LOS	RES	INTMSK_ TOUTA	INTMSK_ TOUTC	INTMSK_ VOUT	INTMSK_ FAULT
Read/Write	R/W Write in setup mode only							
POR State	1	1	1	1	1	1	1	1

BIT	NAME	DESCRIPTION
D[7]	INTMSK_ LVFLAG	Mask LVFLAG interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[6]	RES	Reserved
D[5]	INTMSK_ TIN_LOS	Mask TIN_LOS interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[4]	RES	Reserved
D[3]	INTMSK_ TOUTA	Mask LV_TOUTA interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[2]	INTMSK_ TOUTC	Mask LV_TOUTC interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[1]	INTMSK_ VOUT	Mask LV_VOUT interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[0]	INTMSK_ FAULT	Mask fault event from INTRPT pin 0 = no mask 1 = mask (default)

**Interrupt Mask Control Register (INTMSK3), Address: H0x60 (Page 0)**

BIT	D7	D6	D5	D4	D3	D2	D[1:0]
Bit Name	INTMSK_DC_OVFL	INTMSK_DC_UDFL	INTMSK_MOD_OVFL	INTMSK_MOD_UDFL	INTMSK_TX_LOL	INTMSK_LFTX_OOR	RES
Read/Write	R/W Write in setup mode only						
POR State	1	1	1	1	1	1	11

BIT	NAME	DESCRIPTION
D[7]	INTMSK_DC_OVFL	Mask DC_OVFL interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[6]	INTMSK_DC_UDFL	Mask DC_UDFL interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[5]	INTMSK_MOD_OVFL	Mask MOD_OVFL interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[4]	INTMSK_MOD_UDFL	Mask MOD_UDFL interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[3]	INTMSK_TX_LOL	Mask TX_LOL from INTRPT pin 0 = no mask 1 = mask (default)
D[2]	INTMSK_LFTX_OOR	Mask LFTX_OOR from INTRPT pin 0 = no mask 1 = mask (default)
D[1:0]	RES	Reserved

**Interrupt Mask Control Register (INTMSK4), Address: H0x61 (Page 0)**

BIT	D7	D[6:5]	D4	D3	D2	D1	D0
Bit Name	INTMSK_MDOPEN	RES	INTMSK_MDIN_SHRT	INTMSK_SSMODE	INTMSK_MD0OVFL	INTMSK_MD0UDFL	RES
Read/Write	R/W Write in setup mode only						
POR State	1	11	1	1	1	1	1

BIT	NAME	DESCRIPTION
D[7]	INTMSK_MDOPEN	Mask MDIN_OPEN interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[6:5]	RES	Reserved
D[4]	INTMSK_MDIN_SHRT	Mask MDIN_SHRT interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[3]	INTMSK_SSMODE	Mask SSMODE interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[2]	INTMSK_MD0OVFL	Mask MD0_OVFL interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[1]	INTMSK_MD0UDFL	Mask MD0_UDFL interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[0]	RES	Reserved



**Interrupt Mask Control Register (INTMSK5), Address: H0x62 (Page 0)**

BIT	D7	D6	D5	D4	D[3:0]
Bit Name	INTMSK_MD1OVFL	INTMSK_MD1UDFL	INTMSK_SETAPC_OVFL	INTMSK_SETAPC_UDFL	RES
Read/Write	R/W Write in setup mode only				
POR State	1	1	1	1	0000

BIT	NAME	DESCRIPTION
D[7]	INTMSK_MD1OVFL	Mask MD1_OVFL interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[6]	INTMSK_MD1UDFL	Mask MD1_UDFL interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[5]	INTMSK_SETAPC_OVFL	Mask SET_APC_OVFL interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[4]	INTMSK_SETAPC_UDFL	Mask SET_APC_UDFL interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[3:0]	RES	Reserved

## Interrupt Mask Control Register (INTMSK6), Address: H0x63 (Page 0)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RES	INTMSK_ DDMTMAX	INTMSK_ DDMTMIN	INTMSK_ DDM_ LVFLAG	INTMSK_ P2VFLAG	INTMSK_ RSSI_HI	INTMSK_ RSSI_LO	INTMSK_ EXT_TF
Read/Write	R/W Write in setup mode only							
POR State	0	1	1	1	1	1	1	1

BIT	NAME	DESCRIPTION
D[7]	RES	Reserved
D[6]	INTMSK_ DDMTMAX	Mask DDM_TMAX interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[5]	INTMSK_ DDMTMIN	Mask DDM_TMIN interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[4]	INTMSK_ DDM_ LVFLAG	Mask DDM_LVFLAG interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[3]	INTMSK_ P2VFLAG	Mask DDM_P2VFLAG interrupt (V <sub>CCX</sub> and V <sub>CCT</sub> ) from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[2]	INTMSK_ RSSI_HI	Mask DDM RSSI reading stuck high interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[1]	INTMSK_ RSSI_LO	Mask DDM RSSI reading stuck low interrupt from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)
D[0]	INTMSK_ EXT_TF	Mask DDM_EXT_T_FAIL interrupt (missing connection to external pnp) from INTRPT pin and TOPSTAT register 0 = no mask 1 = mask (default)

## Top Control Register (TOPCTRL1), Address: H0x67 (Page 0)

BIT	D7	D6	D[5:3]	D2	D1	D0
Bit Name	RES	RX_CDR_EN	RX_MUX[2:0]	RES	RX_CDR_RUN	RX_PG_OL
Read/Write	R/W Write in setup mode only					
POR State	0	0	000	0	0	0

BIT	NAME	DESCRIPTION
D[7]	RES	Reserved
D[6]	RX_CDR_EN	Receiver CDR Enable 0 = Rx CDR disabled (default) 1 = Rx CDR enabled
D[5:3]	RX_MUX[2:0]	Receiver Mux Path, see figure 18 0xx = Non-CDR path through Rx circuitry (default) 100 = CDR path through Rx circuitry 101 = Pattern generator path through Rx circuitry 110 = Loop-back path from Tx input to Rx output 111 = Reserved
D[2]	RES	Reserved
D[1]	RX_CDR_RUN	Receiver CDR run. The CDR controller is allowed to run when this bit has 1 written to it (must have XCVR_EN = 1). 0 = Rx CDR controller is reset (default) 1 = Rx CDR run
D[0]	RX_PG_OL	Clock for Rx pattern generator is based off open-loop Rx VCO clock 0 = Pattern generator clocked by closed-loop Rx CDR (default) 1 = Pattern generator clocked by open-loop Rx VCO

**Top Control Register (TOPCTRL2), Address: H0x68 (Page 0)**

BIT	D7	D6	D[5:3]	D2	D1	D0
Bit Name	RES	TX_CDR_EN	TX_MUX[2:0]	RES	TX_CDR_RUN	TX_PG_OL
Read/Write	R/W Write in setup mode only					
POR State	0	0	000	0	0	0

BIT	NAME	DESCRIPTION
D[7]	RES	Reserved
D[6]	TX_CDR_EN	Transmitter CDR Enable 0 = Tx CDR disabled (default) 1 = Tx CDR enabled
D[5:3]	TX_MUX[2:0]	Transmitter Mux Path, see figure 18 0xx = Non-CDR path through Tx circuitry (default) 100 = CDR path through Tx circuitry 101 = Pattern generator detector path through Tx circuitry 110 = Loop-back path from Rx input to Tx output 111 = Reserved
D[2]	RES	Reserved
D[1]	TX_CDR_RUN	Transmitter CDR run. The CDR controller is allowed to run when this bit has 1 written to it (must have XCVR_EN = 1). 0 = Tx CDR controller is reset (default) 1 = Tx CDR run
D[0]	TX_PG_OL	Clock for Tx pattern generator is based off open-loop Tx VCO clock 0 = Pattern generator clocked by closed-loop Tx CDR (default) 1 = Pattern generator clocked by open-loop Tx VCO

Table 13. Registers and Addresses for Page 1

PAGE	ADDRESS	NAME	DEFAULT VALUE	FUNCTION
X	H0x00	MODECTRL	00h	Mode Control Register
1	H0x01	TXCTRL3	02h	Transmitter Control Register
1	H0x02	TXCTRL4	0Ah	Transmitter Control Register
1	H0x0A	TXCTRL5	08h	Transmitter Control Register
1	H0x0B	TXCTRL6	80h	Transmitter Control Register
1	H0x0C	DCMAX	12h	Maximum DC Current Register
1	H0x0D	MODMAX	30h	Maximum Modulation Current Register
1	H0x0E	SET_DC	00h	Laser DC Current DAC Initial Value
1	H0x0F	SET_MOD	00h	Laser Modulation Current DAC Value
1	H0x10	DCINC	00h	DC Current Increment Register
1	H0x11	MODINC	00h	Modulation Current Increment Register
1	H0x12	SET_APC	80h	APC Loop Set Register
1	H0x13	APCINC	00h	APC Loop Increment Register
1	H0x14	TXCTRL7	14h	Transmitter Control Register
1	H0x15	TOPCTRL3	90h	Transceiver Control Register
1	H0x16	DCREG	00h	Laser DC Current DAC Read-Back
1	H0x17	MODREG	00h	Laser Modulation Current DAC Read-Back
1	H0x18	MD1REGH	00h	Upper Byte of Digitized Top Peak Value of MD Input Current
1	H0x19	MD1REGL	00h	Lower Byte of Digitized Top Peak Value of MD Input Current
1	H0x1A	MD0REGH	00h	Upper Byte of Digitized Bottom Peak Value of MD Input Current
1	H0x1B	MD0REGL	00h	Lower Byte of Digitized Bottom Peak Value of MD Input Current
1	H0x1C	TOPSTAT	A0h	Transceiver Status Register
1	H0x1D	RXSTAT1	10h	Receiver Status Register
1	H0x21	TXSTAT1	00h	Transmitter Status Register
1	H0x22	TXSTAT2	00h	Transmitter Status Register
1	H0x23	TXSTAT3	40h	Transmitter Status Register
1	H0x24	TXSTAT4	00h	Transmitter Status Register
1	H0x25	RXSTAT2	00h	Receiver Status Register
1	H0x2B	TXSTAT5	00h	Transmitter Status Register
1	H0x3E	DDMSTAT1	00h	Upper Byte of Digitized RSSI Value
1	H0x3F	DDMSTAT2	00h	Lower Byte of Digitized RSSI Value
1	H0x40	DDMSTAT3	00h	Upper Byte of Digitized V <sub>CCX</sub> Value
1	H0x41	DDMSTAT4	00h	Lower Byte of Digitized V <sub>CCX</sub> Value
1	H0x42	DDMSTAT5	00h	Upper Byte of Digitized V <sub>CCT</sub> Value

Table 13. Registers and Addresses for Page 1 (continued)

PAGE	ADDRESS	NAME	DEFAULT VALUE	FUNCTION
1	H0x43	DDMSTAT6	00h	Lower Byte of Digitized $V_{CCT}$ Value
1	H0x44	DDMSTAT7	00h	Upper Byte of Digitized $V_{CCTO}$ Value
1	H0x45	DDMSTAT8	00h	Lower Byte of Digitized $V_{CCTO}$ Value
1	H0x46	DDMSTAT9	00h	Upper Byte of Digitized Auxiliary Voltage Value at BADC Pin
1	H0x47	DDMSTAT10	00h	Lower Byte of Digitized Auxiliary Voltage Value at BADC Pin
1	H0x48	DDMSTAT11	00h	Upper Byte of Digitized External Temp-Sensor Value at TSNS Pin
1	H0x49	DDMSTAT12	00h	Lower Byte of Digitized External Temp-Sensor Value at TSNS Pin
1	H0x4A	DDMSTAT13	00h	Upper Byte of Digitized Internal Temp-Sensor Value
1	H0x4B	DDMSTAT14	00h	Lower Byte of Digitized Internal Temp-Sensor Value

Transmitter Control Register (TXCTRL3), Address: H0x01 (Page 1)

BIT	D7	D[6:2]	D1	D0
Bit Name	LOOP_STOP	RES	AUTORNG_EN	SOFT_RESET
Read/Write	R/W Write in setup mode only			
POR State	0	0 0000	1	0

BIT	NAME	DESCRIPTION
D[7]	LOOP_STOP	Halts the APC loop. This bit can only be changed from a 1 to a 0 by writing 1 to LOOP_RUN. 0 = no action (default) 1 = halts APC loop
D[6:2]	RES	Reserved
D[1]	AUTORNG_EN	Enables auto-ranging of MDIN_GAIN. 0 = auto-ranging disabled 1 = auto-ranging enabled. When using APCINC the MAX3955 will automatically adjust gain setting of MDIN_GAIN in order to keep SET_APC in the range of 127 to 255. (default)
D[0]	SOFT_RESET	Soft reset will reset all registers to their default (POR) values. The Tx must be disabled, via DISABLE pin or TX_EN bit, before a soft reset can occur. 0 = no action (default) 1 = soft reset

## Transmitter Control Register (TXCTRL4), Address: H0x02 (Page 1)

BIT	D[7:2]	D1	D0
Bit Name	RES	MDAVG_CNT	RES
Read/Write	R/W Write in setup mode only		
POR State	00 0010	1	0

BIT	NAME	DESCRIPTION
D[7:2]	RES	Reserved
D[1]	MDAVG_CNT	Select averaging depth for the MDIN signal 0 = 32 averaging 1 = 256 averaging (default)
D[0]	RES	Reserved

## Transmitter Control Register (TXCTRL5), Address: H0x0A (Page 1)

BIT	D7	D6	D5	D4	D[3:0]
Bit Name	RES	APC_EN	IBUPDT_EN	IMUPDT_EN	RES
Read/Write	R/W Write in setup mode only				
POR State	0	0	0	0	1000

BIT	NAME	DESCRIPTION
D[7]	RES	Reserved
D[6]	APC_EN	Enables APC loop 0 = disabled (default) 1 = enabled
D[5]	IBUPDT_EN	Sets the way DCREG[9:0] is written to:  APC enabled: 0 = maintains last value of DCREG[9:0] in initialization (default) 1 = FAULT/POR/RESTART initializes DCREG[9:2] with SET_DC[7:0]  APC off: 0 = DCREG can only be changed by writing to DCINC[4:0] (default) 1 = if IBUPDT_EN is already set to 1 a write to SET_DC[7:0] is passed to DCREG[9:2]
D[4]	IMUPDT_EN	Sets the way MODREG[8:0] is written to:  0 = MODREG can only be changed by writing to MODINC[4:0] (default) 1 = if IMUPDT_EN is already set to 1 a write to SET_MOD[7:0] is passed to MODREG[8:1]
D[3:0]	RES	Reserved

**Transmitter Control Register (TXCTRL6), Address: H0x0B (Page 1)**

BIT	D[7:1]	D0
Bit Name	RES	AUX_RESTART
Read/Write	R/W Write in setup mode only	
POR State	1000 000	0

BIT	NAME	DESCRIPTION
D[7:1]	RES	Reserved
D[0]	AUX_RESTART	Enables restarting of APC loop by means of DISABLE pin. 0 = disabled (default) 1 = enabled

**Maximum DC-Current Register (DCMAX), Address: H0x0C (Page 1)**

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	DCMAX [7]	DCMAX [6]	DCMAX [5]	DCMAX [4]	DCMAX [3]	DCMAX [2]	DCMAX [1]	DCMAX [0]
Read/Write	R/W Write in setup mode only							
POR State	0	0	0	1	0	0	1	0

BIT	NAME	DESCRIPTION
D[7:0]	DCMAX[7:0]	Programs the maximum settable DC current (limits the maximum value that can be written to the DCREG[9:2] register). Note that it only relates to the eight most significant bits of the DCREG register. $I_{DCMAX} = (DCMAX[7:0] + 3) \times 234\mu A$ 18d = 4.9mA DC current limit (default)

**Maximum Modulation-Current Register (MODMAX), Address: H0x0D (Page 1)**

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	MODMAX [7]	MODMAX [6]	MODMAX [5]	MODMAX [4]	MODMAX [3]	MODMAX [2]	MODMAX [1]	MODMAX [0]
Read/Write	sR/W Write in setup mode only							
POR State	0	0	1	1	0	0	0	0

BIT	NAME	DESCRIPTION
D[7:0]	MODMAX[7:0]	Programs the maximum settable modulation current (limits the maximum value that can be written to the MODREG[8:1] register). Note that it only relates to the eight most significant bits of the MODREG register. $I_{MODMAX} = (MODMAX[7:0] + 8) \times 468\mu A$ 48d = 26mA <sub>P-P</sub> modulation current limit (default)



## Initial or Open-Loop DC Current Register (SET\_DC), Address: H0x0E (Page 1)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	SET_DC [7]	SET_DC [6]	SET_DC [5]	SET_DC [4]	SET_DC [3]	SET_DC [2]	SET_DC [1]	SET_DC [0]
Read/Write	R/W Write in setup mode only							
POR State	0	0	0	0	0	0	0	0

BIT	NAME	DESCRIPTION
D[7:0]	SET_DC[7:0]	Programs the initial or open-loop DC current. The value in this register is sent to the DCREG[9:0] register's eight most significant bits. $I_{DC} = (\text{SET\_DC}[7:0] + 3) \times 234\mu\text{A}$ 0d = 0.7mA DC current (default)

## Modulation Current Register (SET\_MOD), Address: H0x0F (Page 1)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	SET_MOD [7]	SET_MOD [6]	SET_MOD [5]	SET_MOD [4]	SET_MOD [3]	SET_MOD [2]	SET_MOD [1]	SET_MOD [0]
Read/Write	R/W Write in setup mode only							
POR State	0	0	0	0	0	0	0	0

BIT	NAME	DESCRIPTION
D[7:0]	SET_MOD[7:0]	Programs the modulation current. The value in this register is sent to the MODREG[8:0] register's eight most significant bits. $I_{MOD} = (\text{SET\_MOD}[7:0] + 8) \times 468\mu\text{A}$ 0d = 3.7mA <sub>P-P</sub> modulation current (default)

## DC Current Increment Register (DCINC), Address: H0x10 (Page 1)

BIT	D[7:5]	D4	D3	D2	D1	D0
Bit Name	RES	DCINC[4]	DCINC[3]	DCINC[2]	DCINC[1]	DCINC[0]
Read/Write	R			R/W Write in any mode		
POR State	000	0	0	0	0	0

BIT	NAME	DESCRIPTION
D[7:5]	RES	Reserved
D[4:0]	DCINC[4:0]	<p>Mode when APC enabled:  DCINC[3:0] controls the maximum allowed step and hence influences APC loop dynamics especially during startup.  x 0000 = 0 maximum step allowed for DCREG[9:0]  x 1111 = <math>\pm 15d</math> maximum step allowed for DCREG[9:0]</p> <p>Mode when APC disabled:  Laser DC current increment/decrement applied to DCREG[9:0] upon write (two's complement number, the range is <math>\pm 15</math>).  1 0000 = subtract 16 from DCREG[9:0]  0 1111 = add 15 to DCREG[9:0]</p>

**Modulation Increment Register (MODINC), Address: H0x11 (Page 1)**

BIT	D[7:5]	D4	D3	D2	D1	D0
Bit Name	RES	MODINC[4]	MODINC[3]	MODINC[2]	MODINC[1]	MODINC[0]
Read/Write	R	R/W Write in any mode				
POR State	000	0	0	0	0	0

BIT	NAME	DESCRIPTION
D[7:5]	RES	Reserved
D[4:0]	MODINC[4:0]	Laser modulation current increment/decrement applied to MODREG[8:0] upon write (two's complement number, the range is +15/-16). 1 0000 = subtract 16 from MODREG[8:0] 0 1111 = add 15 to MODREG[8:0]

**APC Loop Set Register (SET\_APC), Address: H0x12 (Page 1)**

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	SET_APC[7]	SET_APC[6]	SET_APC[5]	SET_APC[4]	SET_APC[3]	SET_APC[2]	SET_APC[1]	SET_APC[0]
Read/Write	R/W Write in setup mode only							
POR State	1	0	0	0	0	0	0	0

BIT	NAME	DESCRIPTION
D[7:0]	SET_APC [7:0]	Sets the closed-loop MDIN target average current. This closed-loop current depends on SET_APC and MDIN_GAIN registers.

**APC Increment Register (APCINC), Address: H0x13 (Page 1)**

BIT	D[7:4]	D3	D2	D1	D0
Bit Name	RES	APCINC[3]	APCINC[2]	APCINC[1]	APCINC[0]
Read/Write	R	R/W Write in any mode			
POR State	0000	0	0	0	0

BIT	NAME	DESCRIPTION
D[7:4]	RES	Reserved
D[3:0]	APCINC[3:0]	Increments or decrements the SET_APC[7:0] value with the two's complement value from APCINC[3:0] (the range is +/-8). 1000 = subtract 8 from SET_APC[7:0] 0111 = add 7 to SET_APC[7:0]

## Transmitter Control Register (TXCTRL7), Address: H0x14 (Page 1)

BIT	D[7:3]	D2	D1	D0
Bit Name	RES	MDIN_GAIN[2]	MDIN_GAIN[1]	MDIN_GAIN[0]
Read/Write	R/W Write in setup mode only			
POR State	0 0010	1	0	0

BIT	NAME	DESCRIPTION
D[7:3]	RES	Reserved
D[2:0]	MDIN_GAIN[2:0]	Selects the transimpedance gain of the MDIN input 000 = 156Ω                      011 = 1248Ω 001 = 312Ω                      1xx = 2496Ω (default) 010 = 624Ω

## Transceiver Control Register (TOPCTRL3), Address: H0x15 (Page 1)

BIT	D7	D6	D[5:3]	D2	D1	D0
Bit Name	LOOP_RUN	LOOP_RESTART	RES	LOOP_TH	TX_EN	XCVR_EN
Read/Write	R/W Write in setup mode only					
POR State	1	0	010	0	0	0

BIT	NAME	DESCRIPTION
D[7]	LOOP_RUN	Controls the APC loop. LOOP_RUN can only be changed from a 1 to a 0 by writing a 1 to LOOP_STOP. 0 = no action 1 = APC loop will restart from last saved pre-freeze conditions (subject to IBUPDT_EN)
D[6]	LOOP_RESTART	Forces APC loop out of steady-state and enables the startup state machine 0 = no action (default) 1 = restart
D[5:3]	RES	Reserved
D[2]	LOOP_TH	Sets threshold for updating DCREG 0 = 0.125 LSb (default) 1 = 0.75 LSb
D[1]	TX_EN	Enables the Tx data path, control loop, and the DC current and modulation current DACs. 0 = Tx disabled (default) 1 = Tx enabled
D[0]	XCVR_EN	Top-level Transceiver enable 0 = disabled (default) 1 = enabled

**DC Current DAC Readback Register (DCREG), Address: H0x16 (Page 1)**

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	DCREG [9]	DCREG [8]	DCREG [7]	DCREG [6]	DCREG [5]	DCREG [4]	DCREG [3]	DCREG [2]
Read/Write	Read only							
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	No	No	No	No	No	No	No	No

BIT	NAME	DESCRIPTION
D[7:0]	DCREG[9:2]	DC Current DAC Readback. The two LSbs for this register are located at Page 1 Address: H0x24[2:1].

**Modulation Current DAC Readback Register (MODREG), Address: H0x17 (Page 1)**

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	MODREG [8]	MODREG [7]	MODREG [6]	MODREG [5]	MODREG [4]	MODREG [3]	MODREG [2]	MODREG [1]
Read/Write	Read only							
POR State	0	0	0	0	0	0	0	0

BIT	NAME	DESCRIPTION
D[7:0]	MODREG[8:1]	Modulation current DAC readback. The LSb for this register is located at Page 1 Address: H0x24[0].

**Monitor Diode Top Peak (Averaged) Register (MD1REGH), Address: H0x18 (Page 1)**

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	MD1REG [15]	MD1REG [14]	MD1REG [13]	MD1REG [12]	MD1REG [11]	MD1REG [10]	MD1REG [9]	MD1REG [8]
Read/Write	Read only							
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	No	No	No	No	No	No	No	No

BIT	NAME	DESCRIPTION
D[7:0]	MD1REG[15:8]	Stored (averaged) value for monitor-diode current peak corresponding to optical P1. MD1REGH is the upper 8 bits of the 16-bit value MD1REG[15:0].

**Monitor Diode Top Peak (Averaged) Register (MD1REGL), Address: H0x19 (Page 1)**

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	MD1REG [7]	MD1REG [6]	MD1REG [5]	MD1REG [4]	MD1REG [3]	MD1REG [2]	MD1REG [1]	MD1REG [0]
Read/Write	Read only							
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	No	No	No	No	No	No	No	No

BIT	NAME	DESCRIPTION
D[7:0]	MD1REG[7:0]	Stored (averaged) value for monitor-diode current peak corresponding to optical P1. MD1REGL is the lower 8 bits of the 16-bit value MD1REG[15:0].

**Monitor Diode Bottom Peak (Averaged) Register (MD0REGH), Address: H0x1A (Page 1)**

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	MD0REG [15]	MD0REG [14]	MD0REG [13]	MD0REG [12]	MD0REG [11]	MD0REG [10]	MD0REG [9]	MD0REG [8]
Read/Write	Read only							
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	No	No	No	No	No	No	No	No

BIT	NAME	DESCRIPTION
D[7:0]	MD0REG[15:8]	Stored (averaged) value for monitor-diode current peak corresponding to optical P0. MD0REGH is the upper 8 bits of the 16-bit value MD0REG[15:0].

**Monitor Diode Bottom Peak (Averaged) Register (MD0REGL), Address: H0x1B (Page 1)**

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	MD0REG [7]	MD0REG [6]	MD0REG [5]	MD0REG [4]	MD0REG [3]	MD0REG [2]	MD0REG [1]	MD0REG [0]
Read/Write	Read only							
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	No	No	No	No	No	No	No	No

BIT	NAME	DESCRIPTION
D[7:0]	MD0REG[7:0]	Stored (averaged) value for monitor-diode current peak corresponding to optical P0. MD0REGL is the lower 8 bits of the 16-bit value MD0REG[15:0].

**Top Level Status Register (TOPSTAT), Address: H0x1C (Page 1)**

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	PORD	PORD_INV	P3VFLAG	RX_INT	TX_INT	APC_INT	DDM_INT	TX_FAULT_COPY
Read/Write	Read only							
POR State	1	0	1	0	0	0	0	0
Reset Upon Read	Yes*	Yes*	Yes*	No	No	No	No	No

\*Sticky bit—Once flagged these registers remain flagged (logic 1) until they are read. Once read, they are reset to 0 if the source of the flag has been removed.

BIT	NAME	DESCRIPTION
D[7]	PORD	Power-on-reset of the digital core. $V_{DD}$ vs. 1.3V 0 = deasserted 1 = asserted (default)
D[6]	PORD_INV	Inverse of PORD 0 = de-asserted (default) 1 = asserted
D[5]	P3VFLAG	$V_{CCX}/V_{CCT}$ vs. 2.5V 0 = deasserted 1 = asserted (default)
D[4]	RX_INT	Interrupt/fault in Rx group. Read RXSTAT. 0 = deasserted (default) 1 = asserted
D[3]	TX_INT	Interrupt/fault in Tx group. Read TXSTAT1 and TXSTAT2. 0 = deasserted (default) 1 = asserted
D[2]	APC_INT	Interrupt/fault in APC group. Read TXSTAT2, TXSTAT3, and TXSTAT4 0 = deasserted (default) 1 = asserted
D[1]	DDM_INT	Interrupt/fault in DDM group. Read DDMSTAT23. 0 = deasserted (default) 1 = asserted
D[0]	TX_FAULT_COPY	A copy of FAULT pin value 0 = deasserted (default) 1 = asserted

## Receiver Status Register (RXSTAT), Address: H0x1D (Page 1)

BIT	D[7:2]	D1	D0
Bit Name	RES	RXLOSREF	RXLOS_COPY
Read/Write	Read only		
POR State	000100	0	0
Reset Upon Read	N/A	Yes*	Yes*

\*Sticky bit- Once flagged these registers remain flagged (logic 1) until they are read. Once read, they are reset to 0 if the source of the flag has been removed.

BIT	NAME	DESCRIPTION
D[7:2]	RES	Reserved
D[1]	RXLOSREF	Interrupt: Rx LOS block reference signal failure 0 = deasserted (default) 1 = asserted
D[0]	RXLOS_COPY	A copy of Rx LOS pin value 0 = deasserted (default) 1 = asserted

**Transmitter Status Register (TXSTAT1), Address: H0x21 (Page 1)**

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	LVFLAG	RES	TIN_LOS	RES	LV_TOUTA	LV_TOUTC	LV_VOUT	TX_DIS_COPY
Read/Write	Read only							
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	Yes*	No	Yes*	Yes*	Yes*	Yes*	Yes*	No

\*Sticky bit—Once flagged these registers remain flagged (logic 1) until they are read. Once read, they are reset to 0 if the source of the flag has been removed.

BIT	NAME	DESCRIPTION
D[7]	LVFLAG	Interrupt/fault $V_{CCT}$ or $V_{CCTO}$ undervoltage detection 0 = deasserted (default) 1 = asserted
D[6]	RES	Reserved
D[5]	TIN_LOS	Interrupt/fault Indicates TIN AC signal too low 0 = deasserted (default) 1 = asserted
D[4]	RES	Reserved
D[3]	LV_TOUTA	Interrupt/fault TOUTA open or shorted to GND. 0 = deasserted (default) 1 = asserted
D[2]	LV_TOUTC	Interrupt/fault TOUTC open or shorted to GND. 0 = deasserted (default) 1 = asserted
D[1]	LV_VOUT	Interrupt/fault VOUT fault undervoltage detection (referenced to $V_{CCTO}$ ) 0 = deasserted (default) 1 = asserted
D[0]	TX_DIS_COPY	Copy of DISABLE pin. Polarity, controlled by DIS_POL, is included in this bit.



**Transmitter Status Register (TXSTAT2), Address: H0x22 (Page 1)**

BIT	D7	D6	D5	D4	D3	D[2:1]	D0
Bit Name	MDIN_OPEN	DC_OVFL	DC_UDFL	MOD_OVFL	MOD_UDFL	RES	MDIN_SHRT
Read/Write	Read only						
POR State	0	0	0	0	0	00	0
Reset Upon Read	Yes*	Yes*	Yes*	Yes*	Yes*	No	Yes*

\*Sticky bit—Once flagged these registers remain flagged (logic 1) until they are read. Once read, they are reset to 0 if the source of the flag has been removed.

BIT	NAME	DESCRIPTION
D[7]	MDIN_OPEN	Interrupt/fault: MDIN pin open 0 = deasserted (default) 1 = asserted
D[6]	DC_OVFL	Interrupt: DCREG input over maximum warning 0 = deasserted (default) 1 = asserted
D[5]	DC_UDFL	Interrupt: DCREG input underflow warning 0 = deasserted (default) 1 = asserted
D[4]	MOD_OVFL	Interrupt/fault: MODREG input over maximum warning 0 = deasserted (default) 1 = asserted
D[3]	MOD_UDFL	Interrupt: MODREG input underflow warning 0 = deasserted (default) 1 = asserted
D[2:1]	RES	Reserved
D[0]	MDIN_SHRT	Interrupt/fault: MDIN shorted to ground or supply. 0 = deasserted (default) 1 = asserted

**Transmitter Status Register (TXSTAT3), Address: H0x23 (Page 1)**

BIT	D7	D6	D5	D4	D3	D2	D[1:0]
Bit Name	SSMODE	SSMODEB	MD0_OVFL	MD0_UDFL	MD1_OVFL	MD1_UDFL	RES
Read/Write	Read only						
POR State	0	1	0	0	0	0	00
Reset Upon Read	No	Yes*	Yes*	Yes*	Yes*	Yes*	No

\*Sticky bit—Once flagged these registers remain flagged (logic 1) until they are read. Once read, they are reset to 0 if the source of the flag has been removed.

BIT	NAME	DESCRIPTION
D[7]	SSMODE	APC steady-state mode monitor 0 = acquisition mode (default) 1 = steady-state mode
D[6]	SSMODEB	Interrupt: APC steady-state mode monitor (inverted) 0 = steady-state mode 1 = acquisition mode (default)
D[5]	MD0_OVFL	Interrupt: MD0REG input over maximum warning 0 = de-asserted (default) 1 = asserted
D[4]	MD0_UDFL	Interrupt: MD0REG input underflow warning 0 = de-asserted (default) 1 = asserted
D[3]	MD1_OVFL	Interrupt: MD1REG input over maximum warning 0 = de-asserted (default) 1 = asserted
D[2]	MD1_UDFL	Interrupt: MD1REG input underflow warning 0 = de-asserted (default) 1 = asserted
D[1:0]	RES	Reserved

**Transmitter Status Register (TXSTAT4), Address: H0x24 (Page 1)**

BIT	D[7:5]	D4	D3	D2	D1	D0
Bit Name	RES	SET_APC_OVFL	SET_APC_UDFL	DCREG[1]	DCREG[0]	MODREG[0]
Read/Write	Read only					
POR State	000	0	0	0	0	0
Reset Upon Read	No	Yes*	Yes*	No	No	No

\*Sticky bit—Once flagged these registers remain flagged (logic 1) until they are read. Once read, they are reset to 0 if the source of the flag has been removed.

BIT	NAME	DESCRIPTION
D[7:5]	RES	Reserved
D[4]	SET_APC_OVFL	Interrupt: APCINC setting attempting to overflow SET_APC register 0 = de-asserted (default) 1 = asserted
D[3]	SET_APC_UDFL	(AUTORNG_EN=1) Interrupt: SET_APC below minimum value. 0 = de-asserted (default) 1 = asserted  (AUTORNG_EN = 0) Interrupt: SET_APC below 64d. 0 = de-asserted (default) 1 = asserted
D[2:1]	DCREG[1:0]	LSbs of DCREG register
D[0]	MODREG[0]	LSb of MODREG register

**Receiver Status Register (RXSTAT2), Address: H0x25 (Page 1)**

BIT	D7	D6	D5	D[4:0]
Bit Name	RX_LOL	RES	LFRX_OOR	RES
Read/Write	Read only			
POR State	0	0	0	00000
Reset Upon Read	Yes*	—	Yes*	—

\*Sticky bit—Once flagged these registers remain flagged (logic 1) until they are read. Once read, they are reset to 0 if the source of the flag has been removed.

BIT	NAME	DESCRIPTION
D[7]	RX_LOL	Interrupt: receiver CDR loss-of-lock indicator 0 = de-asserted (default) 1 = asserted
D[6]	RES	Reserved
D[5]	LFRX_OOR	Interrupt: LFRX pin voltage out-of-range indicator 0 = de-asserted (default) 1 = asserted
D[4:0]	RES	Reserved

**Transmitter Status Register (TXSTAT5), Address: H0x2B (Page 1)**

BIT	D7	D6	D5	D[4:0]
Bit Name	TX_LOL	RES	LFTX_OOR	RES
Read/Write	Read only			
POR State	0	0	0	00000
Reset Upon Read	Yes*	—	Yes*	—

\*Sticky bit—Once flagged these registers remain flagged (logic 1) until they are read. Once read, they are reset to 0 if the source of the flag has been removed.

BIT	NAME	DESCRIPTION
D[7]	TX_LOL	Interrupt: transmitter CDR loss-of-lock indicator 0 = de-asserted (default) 1 = asserted
D[6]	RES	Reserved
D[5]	LFTX_OOR	Interrupt: LFTX pin voltage out-of-range indicator 0 = de-asserted (default) 1 = asserted
D[4:0]	RES	Reserved

**DDM Status Register (DDMSTAT1), Address: H0x3E (Page 1)**

BIT	D[7:0]	DESCRIPTION
Bit Name	DDM_RSSI [15:8]	Reports upper byte of the measured value of RSSI
Read/Write	Read only	
POR State	00h	

**DDM Status Register (DDMSTAT2), Address: H0x3F (Page 1)**

BIT	D[7:0]	DESCRIPTION
Bit Name	DDM_RSSI [7:0]	Reports lower byte of the measured value of RSSI
Read/Write	Read only	
POR State	00h	

**DDM Status Register (DDMSTAT3), Address: H0x40 (Page 1)**

BIT	D[3:0]	DESCRIPTION
Bit Name	DDM_VCCX [11:8]	Reports upper nibble of the measured value of V <sub>CCX</sub> . The DDM_VCCX[11:0] value is unsigned with full scale of 4.658V. See the Typical Operating Conditions for V <sub>CCX</sub> operational range.
Read/Write	Read only	
POR State	00h	

**DDM Status Register (DDMSTAT4), Address: H0x41 (Page 1)**

BIT	D[7:0]	DESCRIPTION
Bit Name	DDM_VCCX [7:0]	Reports lower byte of the measured value of V <sub>CCX</sub> . The DDM_VCCX[11:0] value is unsigned with full scale of 4.658V. See the Typical Operating Conditions for V <sub>CCX</sub> operational range.
Read/Write	Read only	
POR State	00h	

**DDM Status Register (DDMSTAT5), Address: H0x42 (Page 1)**

BIT	D[3:0]	DESCRIPTION
Bit Name	DDM_VCCT [11:8]	Reports upper nibble of the measured value of V <sub>CCT</sub> . The DDM_VCCT[11:0] value is unsigned with full scale of 4.658V. See the Typical Operating Conditions for V <sub>CCT</sub> operational range.
Read/Write	Read only	
POR State	00h	

**DDM Status Register (DDMSTAT6), Address: H0x43 (Page 1)**

BIT	D[3:0]	DESCRIPTION
Bit Name	DDM_VCCTO [7:0]	Reports lower byte of the measured value of V <sub>CCT</sub> . The DDM_VCCT[11:0] value is unsigned with full scale of 4.658V. See the Typical Operating Conditions for V <sub>CCT</sub> operational range.
Read/Write	Read only	
POR State	Hx00	

**DDM Status Register (DDMSTAT7), Address: H0x44 (Page 1)**

BIT	D[3:0]	DESCRIPTION
Bit Name	DDM_VCCTO [11:8]	Reports upper nibble of the measured value of $V_{CCTO}$ . The DDM_VCCTO[11:0] value is unsigned with full scale of 4.658V. See the Typical Operating Conditions for $V_{CCTO}$ operational range.
Read/Write	Read only	
POR State	Hx00	

**DDM Status Register (DDMSTAT8), Address: H0x45 (Page 1)**

BIT	D[7:0]	DESCRIPTION
Bit Name	DDM_VCCTO [7:0]	Reports lower byte of the measured value of $V_{CCTO}$ . The DDM_VCCTO[11:0] value is unsigned with full scale of 4.658V. See the Typical Operating Conditions for $V_{CCTO}$ operational range.
Read/Write	Read only	
POR State	00h	

**DDM Status Register (DDMSTAT9), Address: H0x46 (Page 1)**

BIT	D[3:0]	DESCRIPTION
Bit Name	DDM_BADC [11:8]	Reports upper nibble of the measured voltage value BADC pin. The DDM_BADC[11:0] value is unsigned with full scale of 1.164V.
Read/Write	Read only	
POR State	00h	

**DDM Status Register (DDMSTAT10), Address: H0x47 (Page 1)**

BIT	D[7:0]	DESCRIPTION
Bit Name	DDM_BADC [7:0]	Reports lower byte of the measured voltage value BADC pin. The DDM_BADC[11:0] value is unsigned with full scale of 1.164V.
Read/Write	Read only	
POR State	00h	

**DDM Status Register (DDMSTAT11), Address: H0x48 (Page 1)**

BIT	D[7:0]	DESCRIPTION
Bit Name	DDM_EXT_TSNS [15:8]	Reports upper byte of the measured value of external temperature sensor between the pins TSNS and TGND. This is the signed integer portion of the external temperature result (range: -128°C to +127°C).
Read/Write	Read only	
POR State	00h	

**DDM Status Register (DDMSTAT12), Address: H0x49 (Page 1)**

BIT	D[7:0]	DESCRIPTION
Bit Name	DDM_EXT_TSNS [7:0]	Reports lower byte of the measured voltage value of external temperature sensor between the pins TSNS and TGND. This is the fractional portion of the external temperature result (range: 0°C to 255/256°C).
Read/Write	Read only	
POR State	00h	

**DDM Status Register (DDMSTAT13), Address: H0x4A (Page 1)**

BIT	D[7:0]	DESCRIPTION
Bit Name	DDM_INT_TSNS [15:8]	Reports upper byte of the measured value of internal temperature sensor. This is the signed integer portion of the internal temperature result (range: -128°C to +127°C).
Read/Write	Read only	
POR State	00h	

**DDM Status Register (DDMSTAT14), Address: H0x4B (Page 1)**

BIT	D[7:0]	DESCRIPTION
Bit Name	DDM_INT_TSNS [7:0]	Reports lower byte of the measured voltage value of internal temperature sensor. This is the fractional portion of the internal temperature result (range: 0°C to +255/256°C).
Read/Write	Read only	
POR State	00h	

**DDM Status Register (DDMSTAT15), Address: H0x4C (Page 1)**

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RES	DDM_TX_SHDN	RES	DDM_TIN_LOS	DDM_TXRPT[11]	DDM_TXRPT[10]	DDM_TXRPT[9]	DDM_TXRPT[8]
Read/Write	Read only							
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	No	No	No	No	No	No	No	No

BIT	NAME	DESCRIPTION
D[7]	RES	Reserved
D[6]	DDM_TX_SHDN	TX status flag 0 = normal operation (default) 1 = shutdown (due to POR, FAULT, DISABLE, TX_EN = 0, or XCVR_EN = 0)
D[5]	RES	Reserved
D[4]	DDM_TIN_LOS	Loss-of-signal at TIN 0 = de-asserted (default) 1 = asserted
D[3:0]	DDM_TXRPT[11:8]	Reports the measured value of DC or average laser current. This is the upper nibble of TXB. These bits along with the lower byte in DDMSTAT16 make up the 12-bit value.

**DDM Status Register (DDMSTAT16), Address: H0x4D (Page 1)**

BIT	D[7:0]	DESCRIPTION
Bit Name	DDM_TXRPT [7:0]	Reports lower byte of DC or average laser current.
Read/Write	Read only	The DDM_TXRPT_SEL bit in DDM_CTRL9 register selects whether DC or average laser current is reported.
POR State	00h	

**DDM Status Register (DDMSTAT17), Address: H0x4E (Page 1)**

BIT	D[3:0]	DESCRIPTION
Bit Name	DDM_TXP[11:8]	Reports the measured value of the monitor diode current which represents average laser power This is the upper nibble of the 12-bit value.
Read/Write	Read only	
POR State	00h	

**DDM Status Register (DDMSTAT18), Address: H0x4F (Page 1)**

BIT	D[7:0]	DESCRIPTION
Bit Name	DDM_TXP[7:0]	Reports the measured value of the monitor diode current which represents average laser power. This is the lower byte of the 12-bit value.
Read/Write	Read only	
POR State	00h	



**DDM Status Register (DDMSTAT23), Address: H0x54 (Page 1)**

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	DDM_TMAX	DDM_TMIN	RES	DDM_P2VFLAG	DDM_RSSI_HI_FAIL	DDM_RSSI_LO_FAIL	DDM_EXT_T_FAIL	DDM_LVFLAG
Read/Write	Read only							
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	Yes*	Yes*	No	Yes*	Yes*	Yes*	Yes*	Yes*

\*Sticky bit—Once flagged these registers remain flagged (logic 1) until they are read. Once read, they are reset to 0 if the source of the flag has been removed.

BIT	NAME	DESCRIPTION
D[7]	DDM_TMAX	Interrupt: Internal temperature above +120°C. 0 = de-asserted (default) 1 = asserted
D[6]	DDM_TMIN	Interrupt: Internal temperature below -50°C. 0 = de-asserted (default) 1 = asserted
D[5]	RES	Reserved
D[4]	DDM_P2VFLAG	Interrupt: $V_{CCX}/V_{CCT}$ vs. 2.1V 0 = de-asserted (default) 1 = asserted
D[3]	DDM_RSSI_HI_FAIL	Interrupt: RSSI is stuck high. 0 = de-asserted (default) 1 = asserted
D[2]	DDM_RSSI_LO_FAIL	Interrupt: RSSI is stuck low. 0 = de-asserted (default) 1 = asserted
D[1]	DDM_EXT_T_FAIL	Interrupt: Status indicating that the external temperature sense has failed. When this condition occurs, the external temperature is forced to -128°C. 0 = de-asserted (default) 1 = asserted
D[0]	DDM_LVFLAG	Interrupt: Supply voltage too low for accurate DDM measurement. 0 = de-asserted (default) 1 = asserted

## Layout Considerations

The high-speed data inputs and outputs are the most critical paths for the device, and great care should be taken to minimize discontinuities on these transmission lines between the connector and the IC. The following are some suggestions for maximizing the device's performance:

- The data inputs should be wired directly between the connector and IC without stubs.
- The data transmission lines to the laser should be kept as short as possible, and the impedance of the transmission lines must be considered part of the laser matching network.
- Minimize capacitance on the MDIN connection.
- An uninterrupted ground plane should be positioned beneath the high-speed I/Os.
- Ground path vias should be placed close to the IC and the input/output interfaces to allow a return current path to the IC and the laser.
- Maintain 100Ω differential transmission line impedance for the RIN, ROUT, and TIN I/Os.

- The data transmission lines to the laser should be kept as short as possible, and must be designed for 50Ω differential or 25Ω single-ended characteristic impedance.
- Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk.

Refer to the schematic and board layers of the HFRD-67 reference design data sheet for more information.

## Exposed-Pad Package and Thermal Considerations

The exposed pad on the MAX3955 is the only electrical connection to ground and provides a very low-thermal resistance path for heat removal from the IC. The pad is also electrical ground on the device and must be soldered to the circuit board ground for proper thermal and electrical performance. Refer to Application Note 862: *HFRD-08.1: Thermal Considerations for QFN and Other Exposed-Paddle Packages* for additional information.

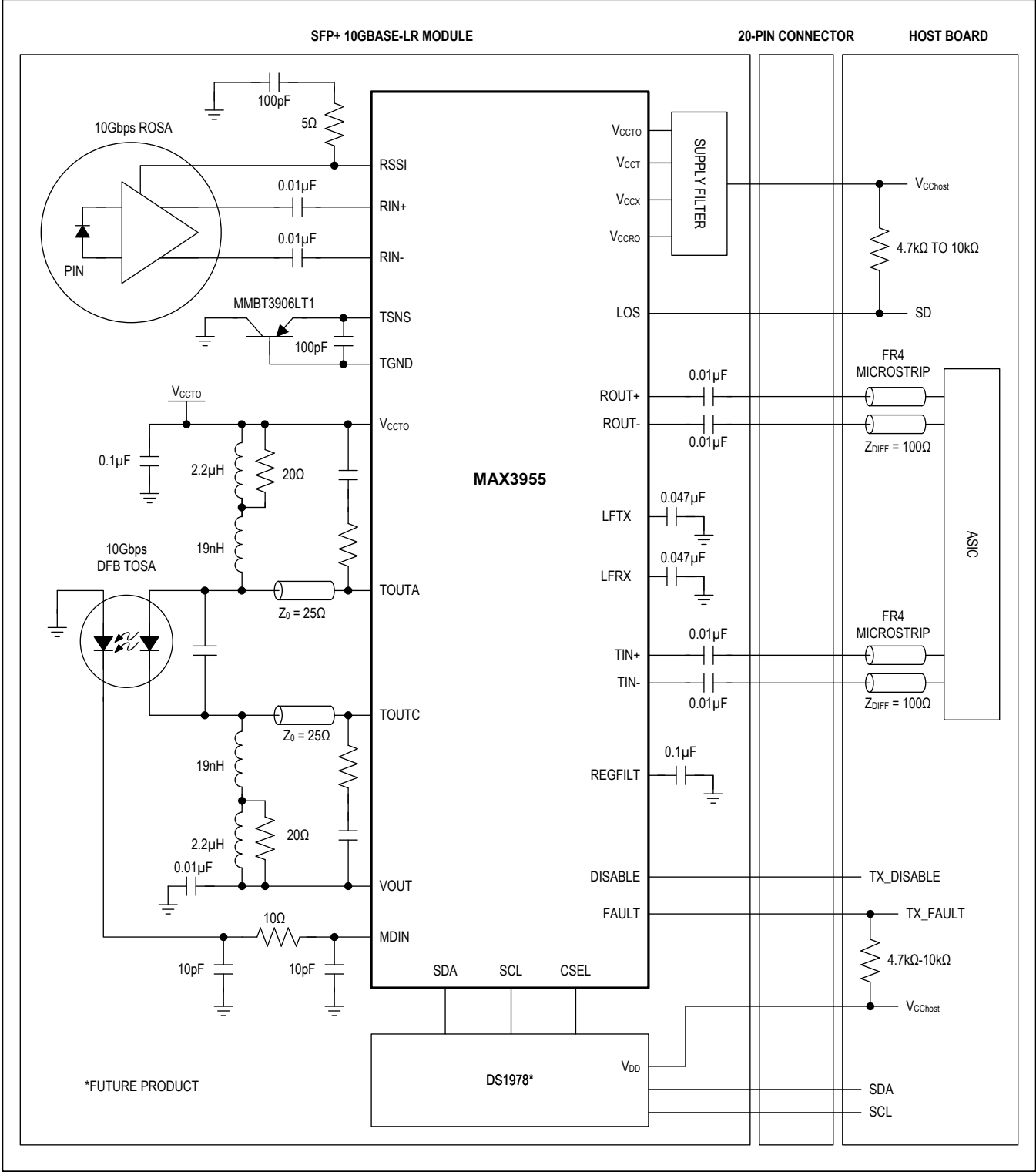
## Current Consumption

Table 14 shows the total current consumption (including all laser current) for the MAX3955 with various blocks enabled/disabled.

**Table 14. Current Consumption**

TOTAL IC PLUS LASER CURRENT (mA)	INCREMENTAL CURRENT (mA)	DESCRIPTION OF STEP
22	—	Startup, transceiver disabled
75	37	Rx Enabled (LOS disabled) (SET_CML = 8d, SET_RXDE = 000)
79	4	LOS enabled (SET_CML = 8d, SET_RXDE = 000)
104	25	Rx CDR enabled (SET_CML = 8d, SET_RXDE = 000)
107	3	Rx Deemphasis set to maximum (SET_CML = 8d, SET_RXDE = 111)
124	17	Tx Enabled (Rx settings kept same as previous row) (ILD_DC = 0mA, ILD_MOD = 0mA)
153	29	Tx CDR Enabled (ILD_DC = 0mA, ILD_MOD = 0mA)
230	77	Laser Modulation current set to 60mA <sub>P-P</sub> at 5Ω laser (ILD_DC = 0mA, ILD_MOD = 60mA <sub>P-P</sub> )
270	40	Laser DC current set to 40mA (ILD_DC = 40mA, ILD_MOD = 60mA)

Typical Application Circuit



## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3955ETJ+	-40°C to +85°C	32 TQFP-EP*

**Note:** Parts are guaranteed by design and characterization to operate over the -40°C to +95°C ambient temperature range ( $T_A$ ) and are tested up to +85°C.

+Denotes a lead(Pb)-free/RoHS-compliant package.

\*EP = Exposed pad.

## Chip Information

PROCESS: SiGe BiCMOS

## Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFP-EP	T3255+3	<a href="#">21-0140</a>	<a href="#">90-0001</a>

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/13	Initial release	—
1	9/14	Fixed data sheet errors and adjusted POR specification in <i>Electrical Characteristics</i>	2, 7, 8, 11, 27, 38, 43, 46, 47, 51, 52, 60, 81, 85, 86, 87

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