*Click **here** for production status of specific part numbers.*

# MAX32000

# High-Speed Quad Driver with Integrated DACs, Cable-Droop Compensation, Slew-Rate Control, and VHH Fourth-Level Drive

## General Description

The MAX32000 is a fully integrated, quad-channel, high-performance pin-electronics driver with built-in level-setting DACs, ideal for memory and SOC ATE systems. Each MAX32000 channel includes a four-level pin driver, programmable cable-droop compensation, five 14-bit DACs, and a comparator that is useful for AC calibration.

The driver features a wide -2V to +6V operating range and a data rate of 1200Mbps at +2V operation, and in high-voltage mode (VHH mode) offers an output voltage range of 0 to 13V. The device includes high impedance, active termination (3rd-level drive), and is highly linear even at low voltage swings. The calibration comparators and multiplexer provide a timing calibration path for each channel. A serial interface configures the device, easing PCB signal routing.

The MAX32000 is available in a 64-pin TQFP-EPR package with top-side exposed pad.

## Applications

- Memory Testers
- SOC Testers
- Digital Testers
- Discrete Component ATE
- Burn-In Testers
- Wafer Testers

## Benefits and Features

- Low Power at High-Speed Maximizes Driver Performance
  - 700mW per Channel
  - 2.57Gbps at +1V Programmed
  - 280ps Typical Rise/Fall Times at +2V (20% to 80%)
  - Very Low Timing Dispersion at 50ps Typical
  - Wide Voltage Range from -2V to +6V
  - Integrated VHH Programming Mode (4th-Level Drive) up to 13V
  - 100nA Low-Leak Mode
- Integrated Functionality Provides Value-Added Features
  - Programmable Double Time Constant Cable-Droop Compensation
  - Digital Slew-Rate Control for EMI-Sensitive Applications
  - Adjustable Output Resistance with 360mΩ Resolution
  - 22 DACs to Generate DC Voltage Levels for Control and Monitoring
  - 50MHz SPI™ Interface

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX32000CCB+ | 0°C to +70°C | 64 TQFP-EP* |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

**EP = Exposed pad.*

*SPI is a trademark of Motorola, Inc.*

*19-100695; Rev 1; 1/21*

maxim integrated™

## Absolute Maximum Ratings

$V_{CC}$ to GND ..... -0.3V to +11.0V
$V_{EE}$ to GND ..... -6.0V to +0.3V
Any $V_{CC}$ to Any $V_{EE}$ ..... +16.5V
$V_{DD}$ to DGND ..... -0.3V to +5.0V
$V_{HHP}$ to GND ..... -0.3V to +19.0V
DGND to GND ..... ±0.3V
GNDDAC__ to GND ..... ±0.3V
DGND to GNDDAC__ ..... ±0.3V
DGS to GND ..... ±1.0V
CTV, DATV_, RTV_ to GND ..... -0.3V to +5V
DATA_, NDATA_ to GND ..... ($V_{EE}$ - 0.3V) to ($V_{CC}$ + 0.3V)
RCV_, NRCV_ to GND ..... ($V_{EE}$ - 0.3V) to ($V_{CC}$ + 0.3V)
CMP, NCMP to GND ..... ($V_{CTV}$ - 1.1V) to ($V_{CTV}$ + 0.3V)
Current into CMP, NCMP ..... ±10mA
DATA_ to NDATA_, RCV_ to NRCV_ ..... ±1V
DUT_ to GND
(all modes except VHH) ..... ($V_{EE}$ - 0.3V) to ($V_{CC}$ + 0.3V)
DUT_ to GND (VHH mode) ..... -3.5V to +13.5V
DUT_ to $V_{EE}$ ..... +19V
SCLK, DIN, $\overline{CS}$, $\overline{LOAD}$, $\overline{RST}$ to DGND .... -0.3V to ($V_{DD}$ + 0.3V)
$\overline{ENVHH}$ to DGND ..... -0.3V to ($V_{DD}$ + 0.3V)
OVALARM, TALARM to DGND ..... -0.3V to ($V_{DD}$ + 0.3V)
TEMP to GND ..... ($V_{EE}$ - 0.3V) to ($V_{CC}$ + 0.3V)
REF to GND ..... -0.3V to the lower of (GNDDAC__ + 2.6V) and ($V_{CC}$ + 0.3V)
REF Current ..... ±75mA
All Digital Inputs ..... ±30mA
DUT_ Short-Circuit Duration ..... Continuous
Continuous Power Dissipation
64-Pin TQFP (derate 125mW/°C above +70°C) ..... 10.0W
Junction Temperature ..... +150°C
Operating Junction Temperature Range ..... +40°C to +100°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C
ESD, Human Body Model:
All Pins Excluding Below Pins ..... 2.000V
ESD, Human Body Model: DATA_, NDATA_ ..... 1.500V
ESD, Human Body Model: RCV_, NRCV_, DATV_, RTV_ .. 1.500V
Humidity ..... 10% to 90%

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Thermal Characteristics (Note 1)

64 TQFP-EP
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) ..... 40°C/W
Junction-to-Case Thermal Resistance ($\theta_{JC}$) ..... 1°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

## Electrical Characteristics

($V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{HHP}$ = +17.5V, $V_{DD}$ = +3.3V, $V_{DHV\_}$ = +3V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DATV\_}$ = $V_{RTV\_}$ = 0V, $V_{CTV}$ = +1.2V, $V_{CMPV}$ = +1V, $V_{VHH}$ = +10V, CDRP__ = 000b, RO_ = 1110b, SC_ = 00b, $V_{DGS}$ = $V_{GND}$ = $V_{GNDDAC\_\_}$ = 0V, specifications apply after calibration, level-setter errors included. The device is tested at $T_J$ = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at $T_J$ = +40°C and +100°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DRIVER** | | | | | | |
| **DRIVER DC CHARACTERISTICS ($R_L$ ≥ 10MΩ, unless otherwise noted, includes level-setter error)** | | | | | | |
| Output Voltage Range | $V_{DHV\_}$ | $V_{DLV\_}$ = -2.0V, $V_{DTV\_}$ = +1.5V | -1.8 | | +6.0 | V |
| | $V_{DLV\_}$ | $V_{DHV\_}$ = +6.0V, $V_{DTV\_}$ = +1.5V | -2.0 | | +5.8 | |
| | $V_{DTV\_}$ | $V_{DHV\_}$ = +6.0V, $V_{DLV\_}$ = -2.0V | -2.0 | | +6.0 | |
| Output Offset Voltage (Note 2) | $V_{DHV\_OS}$ | $V_{DHV\_}$ = +0.125V, $V_{DLV\_}$ = -2.0V, $V_{DTV\_}$ = +1.5V | | | ±2 | mV |
| | $V_{DLV\_OS}$ | $V_{DLV\_}$ = +0.125V, $V_{DHV\_}$ = +6.0V, $V_{DTV\_}$ = +1.5V | | | ±2 | |
| | $V_{DTV\_OS}$ | $V_{DTV\_}$ = +0.125V, $V_{DHV\_}$ = +6.0V, $V_{DLV\_}$ = -2.0V | | | ±2 | |

## Electrical Characteristics (continued)

($V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{HHP}$ = +17.5V, $V_{DD}$ = +3.3V, $V_{DHV\_}$ = +3V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DATV\_}$ = $V_{RTV\_}$ = 0V, $V_{CTV}$ = +1.2V, $V_{CMPV}$ = +1V, $V_{VHH}$ = +10V, CDRP__ = 000b, RO_ = 1110b, SC_ = 00b, $V_{DGS}$ = $V_{GND}$ = $V_{GNDDAC\_\_}$ = 0V, specifications apply after calibration, level-setter errors included. The device is tested at $T_J$ = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at $T_J$ = +40°C and +100°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output Voltage Temperature Coefficient (Notes 3, 4) | $V_{DHV\_TC}$ | | | ±75 | ±500 | µV/°C |
| | $V_{DLV\_TC}$ | | | ±75 | ±500 | |
| | $V_{DTV\_TC}$ | | | ±75 | ±500 | |
| Gain (Note 2) | $A_{DHV\_}$ | $V_{DLV\_}$ = -2.0V, $V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = +0.125V and +3.875V | 0.999 | 1 | 1.001 | V/V |
| | $A_{DLV\_}$ | $V_{DHV\_}$ = +6.0V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = +0.125V and +3.875V | 0.999 | 1 | 1.001 | |
| | $A_{DTV\_}$ | $V_{DHV\_}$ = +6.0V, $V_{DLV\_}$ = -2.0V, $V_{DTV\_}$ = +0.125V and +3.875V | 0.999 | 1 | 1.001 | |
| Linearity Error, -0.5V to +4.5V (Note 2, 3) | | $V_{DLV\_}$ = -2.0V, $V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = -0.5V to +4.5V | | < ±6 | | mV |
| | | $V_{DLV\_}$ = -2.0V, $V_{DHV\_}$ = +6.0V, $V_{DTV\_}$ = -0.5V to +4.5V | | < ±6 | | |
| Linearity Error, -1.75V to +5.125V (Note 2, 3) | | $V_{DLV\_}$ = -2.0V, $V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = -1.75V to +5.125V | | < ±12 | | mV |
| | | $V_{DHV\_}$ = +6.0V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = -1.75V to +5.125V | | < ±12 | | |
| | | $V_{DLV\_}$ = -2.0V, $V_{DHV\_}$ = +6.0V, $V_{DTV\_}$ = -1.75V to +5.125V | | < ±12 | | |
| Linearity Error, Full Range (Note 2, 3) | | $V_{DLV\_}$ = -2.0V, $V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = -1.8V to +6.0V | | < ±14 | | mV |
| | | $V_{DHV\_}$ = +6.0V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = -2.0V to +5.8V | | < ±14 | | |
| | | $V_{DLV\_}$ = -2.0V, $V_{DHV\_}$ = +6.0V, $V_{DTV\_}$ = -2.0V to +6.0V | | < ±14 | | |
| DHV_-to-DLV_ Crosstalk | | $V_{DLV\_}$ = -0.5V, $V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = -0.3V and +6.0V | | | ±3 | mV |
| DLV_-to-DHV_ Crosstalk | | $V_{DHV\_}$ = +4.5V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = -2.0V and +4.3V | | | ±3 | mV |
| DTV_-to-DLV_ and DHV_ Crosstalk | | $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = -2.0V and +6.0V | | | ±2 | mV |
| DHV_-to-DTV_ Crosstalk | | $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +1.6V and +3.0V | | | ±3 | mV |
| DLV_-to-DTV_ Crosstalk | | $V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V and +1.4V | | | ±3 | mV |

## Electrical Characteristics (continued)

($V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{HHP}$ = +17.5V, $V_{DD}$ = +3.3V, $V_{DHV\_}$ = +3V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DATV\_}$ = $V_{RTV\_}$ = 0V, $V_{CTV}$ = +1.2V, $V_{CMPV}$ = +1V, $V_{VHH}$ = +10V, CDRP__ = 000b, RO_ = 1110b, SC_ = 00b, $V_{DGS}$ = $V_{GND}$ = $V_{GNDDAC\_\_}$ = 0V, specifications apply after calibration, level-setter errors included. The device is tested at $T_J$ = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at $T_J$ = +40°C and +100°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Term Voltage Dependence on DATA_ | | $V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, DATA_ = high and low | | | | ±2 | mV |
| DC Power-Supply Rejection | $PSRR_{DHV}$ | $V_{DHV\_}$ = +3V, $V_{CC}$ and $V_{EE}$ independently varied full range | | 40 | | | dB |
| | $PSRR_{DLV}$ | $V_{DLV\_}$ = 0V, $V_{CC}$ and $V_{EE}$ independently varied full range | | 40 | | | |
| | $PSRR_{DTV}$ | $V_{DTV\_}$ = +1.5V, $V_{CC}$ and $V_{EE}$ independently varied full range | | 40 | | | |
| DC Drive Current Limit | | When DATA_ = high , $V_{DHV\_}$ = +6.0V and $V_{DUT\_}$ = -2V | | +65 | | +110 | mA |
| | | When DATA_ = low, $V_{DLV\_}$ = -2.0V and $V_{DUT\_}$ = +6V | | -110 | | -65 | |
| DC Output Resistance | | RO_ = 0b1000 (Note 5) | | 46 | 48 | 50 | Ω |
| DC Output Resistance Variation (Note 6) | | DATA_ = high, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1V, $I_{DUT\_}$ = 1mA, 12mA, 40mA | | | 1 | 2 | Ω |
| | | DATA_ = low, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1V, $I_{DUT\_}$ = -1mA, -12mA, -40mA | | | 1 | 2 | |
| Adjustable Output Resistance Range | $DR_O$ | RO_ = Fh vs. RO_ = 8h and RO_ = 0h vs. RO_ = 8h, resolution of 0.36I (see conditions of Note 5) | | | ±2.5 | | Ω |
| **DRIVER AC CHARACTERISTICS ($R_L$ = 50I to GND) (Note 7)** | | | | | | | |
| Dynamic Drive Current | | (Note 8) | | | ±100 | | mA |
| Drive Mode Overshoot | | Cable-droop compensation off | $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +0.1V | | 50 | | % |
| | | | $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +1V | | 12 | | |
| | | | $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +3V | | 3.3 | | |
| | | | $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +5V | | 2.0 | | |
| Drive Mode Undershoot | | Cable-droop compensation off | $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +0.1V | | 20 | | % |
| | | | $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +1V | | 5 | | |
| | | | $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +3V | | 2.3 | | |
| | | | $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +5V | | 2.0 | | |
| Cable-Droop Compensation Range, Short Time Constant | | $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +1V, CDRPS_ = 000 | | | 0 | | % |
| | | $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +1V, CDRPS_ = 111 | | | 15 | | |
| Cable-Droop Compensation Range, Long Time Constant | | $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +1V, CDRPL_ = 000 | | | 0 | | % |
| | | $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +1V, CDRPL_ = 111 | | | 15 | | |
| Driver Cable-Droop Compensation, Short Time Constant | | | | | 60 | | ps |
| Driver Cable-Droop Compensation, Long Time Constant | | | | | 1.2 | | ns |

## Electrical Characteristics (continued)

($V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{HHP}$ = +17.5V, $V_{DD}$ = +3.3V, $V_{DHV\_}$ = +3V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DATV\_}$ = $V_{RTV\_}$ = 0V, $V_{CTV}$ = +1.2V, $V_{CMPV}$ = +1V, $V_{VHH}$ = +10V, CDRP__ = 000b, RO_ = 1110b, SC_ = 00b, $V_{DGS}$ = $V_{GND}$ = $V_{GNDDAC\_\_}$ = 0V, specifications apply after calibration, level-setter errors included. The device is tested at $T_J$ = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at $T_J$ = +40°C and +100°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Settling Time (Notes 4, 9) | | To within 100mV, $V_{DHV\_}$ = +5V, $V_{DLV\_}$ = 0V | | 0.25 | 1 | ns |
| | | To within 50mV, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V | | 0.25 | 1 | |
| | | To within 25mV, $V_{DHV\_}$ = +0.5V, $V_{DLV\_}$ = 0V | | 0.25 | 1 | |
| **TIMING CHARACTERISTICS (Notes 7, 10)** | | | | | | |
| Propagation Delay, Data to Output | | $V_{DHV\_}$ = +3.0V, $V_{DLV\_}$ = 0V (Note 11) | 0.6 | 1.0 | 1.4 | ns |
| Propagation-Delay Match, $t_{LH}$ vs. $t_{HL}$ | | (Note 4) | | ±40 | ±80 | ps |
| Propagation-Delay Match, Drivers Within Package | | Same edge | | 40 | | ps |
| Propagation-Delay Temperature Coefficient | | (Note 4) | | 3 | 5 | ps/°C |
| Propagation-Delay Change vs. Pulse Width | | $V_{DHV\_}$ = +1V, $V_{DLV\_}$ = 0V, 0.85ns to 24.150ns pulse width (Note 4) | | ±25 | ±50 | ps |
| | | $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, 1.0ns to 24.0ns pulse width (Note 4) | | ±35 | ±60 | |
| | | $V_{DHV\_}$ = +5V, $V_{DLV\_}$ = 0V, 1.5ns to 23.5ns pulse width | | ±100 | | |
| Propagation-Delay Change vs. Common Mode (Note 4) | | $V_{DHV\_}$ - $V_{DLV\_}$ = +1V, $V_{DHV\_}$ = +1V to +4V (using a DC block) | | 50 | 60 | ps |
| | | $V_{DHV\_}$ - $V_{DLV\_}$ = +1V, $V_{DHV\_}$ = -1V to +6V (using a DC block) | | 50 | 100 | |
| Propagation Delay, Drive to High Impedance, High Impedance to Drive | | $V_{DHV\_}$ = +1V, $V_{DLV\_}$ = -1V (Notes 4, 12) | 1.5 | 2.2 | 2.9 | ns |
| Delay Match, Drive to High Impedance vs. High Impedance to Drive | | $V_{DHV\_}$ = +1V, $V_{DLV\_}$ = -1V (Note 13) | | ±0.35 | | ns |
| Delay Match, High Impedance vs. Data | | (Note 14) | | 1.1 | | ns |
| Propagation Delay, Drive to Term, Term to Drive | | (Notes 4, 14) | 1.7 | 2.5 | 3.4 | ns |
| Delay Match, Drive to Term vs. Term to Drive | | $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V (Note 15) | | ±1 | | ns |
| Delay Match, Terminate vs. Data | | (Note 14) | | 1.5 | | ns |

## Electrical Characteristics (continued)

($V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{HHP}$ = +17.5V, $V_{DD}$ = +3.3V, $V_{DHV\_}$ = +3V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DATV\_}$ = $V_{RTV\_}$ = 0V, $V_{CTV}$ = +1.2V, $V_{CMPV}$ = +1V, $V_{VHH}$ = +10V, CDRP__ = 000b, RO_ = 1110b, SC_ = 00b, $V_{DGS}$ = $V_{GND}$ = $V_{GNDDAC\_\_}$ = 0V, specifications apply after calibration, level-setter errors included. The device is tested at $T_J$ = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at $T_J$ = +40°C and +100°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Rise and Fall Time | | 0.2$V_{P-P}$ programmed, $V_{DHV\_}$ = +0.2V, $V_{DLV\_}$ = 0V, 20% to 80% (Note 16) | | 140 | | ps |
| | | 0.2$V_{P-P}$ programmed, $V_{DHV\_}$ = +0.2V, $V_{DLV\_}$ = 0V, 20% to 80% (Note 17) | | 150 | | |
| | | 1$V_{P-P}$ programmed, $V_{DHV\_}$ = +1.0V, $V_{DLV\_}$ = 0V, 10% to 90% (Notes 4, 16) | 200 | 270 | 400 | |
| | | 1$V_{P-P}$ programmed, $V_{DHV\_}$ = +1.0V, $V_{DLV\_}$ = 0V, 10% to 90% (Note 17) | | 350 | | |
| | | 1$V_{P-P}$ programmed, $V_{DHV\_}$ = +1.0V, $V_{DLV\_}$ = 0V, 20% to 80% (Notes 4, 16) | 140 | 190 | 275 | |
| | | 2$V_{P-P}$ programmed, $V_{DHV\_}$ = +2V, $V_{DLV\_}$ = 0V, 20% to 80% (Notes 4, 16) | 230 | 280 | 400 | |
| | | 2$V_{P-P}$ programmed, $V_{DHV\_}$ = +2V, $V_{DLV\_}$ = 0V, 20% to 80%, (Note 17) | | 300 | | |
| | | 3$V_{P-P}$ programmed, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, 10% to 90%, trim condition (Note 16) | 425 | 550 | 800 | |
| | | 3$V_{P-P}$ programmed, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, 10% to 90% (Note 17) | | 605 | | |
| | | 5$V_{P-P}$ programmed, $V_{DHV\_}$ = +5V, $V_{DLV\_}$ = 0V, 10% to 90% (Notes 4, 16) | 650 | 850 | 1050 | |
| | | 5$V_{P-P}$ programmed, $V_{DHV\_}$ = +5V, $V_{DLV\_}$ = 0V, 10% to 90% (Note 17) | | 880 | | |
| Rise and Fall Time Matching (Notes 16, 18) | | 0.2$V_{P-P}$ programmed, $V_{DHV\_}$ = +0.2V, $V_{DLV\_}$ = 0V, 20% to 80% | | ±20 | | ps |
| | | 1$V_{P-P}$ programmed, $V_{DHV\_}$ = +1.0V, $V_{DLV\_}$ = 0V, 10% to 90% (Note 4) | | ±20 | ±40 | |
| | | 2$V_{P-P}$ programmed, $V_{DHV\_}$ = +2.0V, $V_{DLV\_}$ = 0V, 20% to 80% (Note 4) | | ±20 | ±40 | |
| | | 3$V_{P-P}$ programmed, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, 10% to 90% | | ±30 | ±80 | |
| | | 5$V_{P-P}$ programmed, $V_{DHV\_}$ = +5V, $V_{DLV\_}$ = 0V, 10% to 90% | | ±50 | | |
| Slew Rate, Relative to SC1 = SC0 = 0 (Note 19) | | SC1 = 0, SC0 = 1, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, 20% to 80% | | 75 | | % |
| | | SC1 = 1, SC0 = 0, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, 20% to 80% | | 50 | | |
| | | SC1 = 1, SC0 = 1, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, 20% to 80% | | 25 | | |

## Electrical Characteristics (continued)

($V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{HHP}$ = +17.5V, $V_{DD}$ = +3.3V, $V_{DHV\_}$ = +3V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DATV\_}$ = $V_{RTV\_}$ = 0V, $V_{CTV}$ = +1.2V, $V_{CMPV}$ = +1V, $V_{VHH}$ = +10V, CDRP__ = 000b, RO_ = 1110b, SC_ = 00b, $V_{DGS}$ = $V_{GND}$ = $V_{GNDDAC\_\_}$ = 0V, specifications apply after calibration, level-setter errors included. The device is tested at $T_J$ = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at $T_J$ = +40°C and +100°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Minimum Pulse Width (Positive or Negative) | | 0.2$V_{P-P}$ programmed, $V_{DHV\_}$ = +0.2V, $V_{DLV\_}$ = 0V (Note 20) | | 400 | | ps |
| | | 1$V_{P-P}$ programmed, $V_{DHV\_}$ = +1V, $V_{DLV\_}$ = 0V (Notes 4, 20) | | 475 | 610 | |
| | | 1$V_{P-P}$ programmed, $V_{DHV\_}$ = +1V, $V_{DLV\_}$ = 0V; output reaches at least 90% of its nominal DC output level (Note 4) | | 390 | 525 | |
| | | 2$V_{P-P}$ programmed, $V_{DHV\_}$ = +2V, $V_{DLV\_}$ = 0V (Notes 4, 20) | | 665 | 833 | |
| | | 3$V_{P-P}$ programmed, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V (Notes 4, 20) | | 800 | 1000 | |
| | | 5$V_{P-P}$ programmed, $V_{DHV\_}$ = +5V, $V_{DLV\_}$ = 0V (Note 20) | | 1300 | | |
| Data Rate | | 0.2$V_{P-P}$ programmed, $V_{DHV\_}$ = +0.2V, $V_{DLV\_}$ = 0V (Note 21) | | 2500 | | Mbps |
| | | 1$V_{P-P}$ programmed, $V_{DHV\_}$ = +1V, $V_{DLV\_}$ = 0V (Notes 4, 21) | 1650 | 2100 | | |
| | | 1$V_{P-P}$ programmed, $V_{DHV\_}$ = +1V, $V_{DLV\_}$ = 0V; output reaches at least 90% of its nominal DC output level (Note 4) | 1910 | 2570 | | |
| | | 2$V_{P-P}$ programmed, $V_{DHV\_}$ = +2V, $V_{DLV\_}$ = 0V (Notes 4, 21) | 1200 | | | |
| | | 3$V_{P-P}$ programmed, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V (Notes 4, 21) | 1000 | | | |
| | | 5$V_{P-P}$ programmed, $V_{DHV\_}$ = +5V, $V_{DLV\_}$ = 0V (Note 21) | | 900 | | |
| Rise and Fall Time, Drive to Term | | $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, measured 10% to 90% of waveform (Note 22) | 250 | 700 | 1300 | ps |
| Rise and Fall Time, Term to Drive | | $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, measured 10% to 90% of waveform (Note 22) | 400 | 550 | 800 | ps |
| **COMPARATOR** | | | | | | |
| **COMPARATOR DC CHARACTERISTICS** | | | | | | |
| Input Voltage Range | | (Note 23) | -2.2 | | +6.2 | V |
| Input Offset Voltage | | $V_{DUT\_}$ = +0.125V (Note 24) | | ±1 | ±5 | mV |
| Input-Voltage Temperature Coefficient | | (Notes 24, 25) | | ±50 | | µV/°C |
| Common-Mode Rejection | CMRR | $V_{DUT\_}$ = -2.0V, +6.0V (Notes 24, 26) | 50 | 55 | | dB |

## Electrical Characteristics (continued)

($V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{HHP}$ = +17.5V, $V_{DD}$ = +3.3V, $V_{DHV\_}$ = +3V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DATV\_}$ = $V_{RTV\_}$ = 0V, $V_{CTV}$ = +1.2V, $V_{CMPV}$ = +1V, $V_{VHH}$ = +10V, CDRP__ = 000b, RO_ = 1110b, SC_ = 00b, $V_{DGS}$ = $V_{GND}$ = $V_{GNDDAC\_\_}$ = 0V, specifications apply after calibration, level-setter errors included. The device is tested at $T_J$ = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at $T_J$ = +40°C and +100°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Linearity Error (Notes 24, 27) | | -1.75V to +5.125V, $V_{DUT\_}$ = -1.75V to +5.125V | | < ±8 | | mV |
| | | Full range, $V_{DUT\_}$ = -2V to +6.0V | | < ±10 | | |
| | | Full range, $V_{DUT\_}$ = -2.2V to +6.2V | | < ±12 | | |
| Power-Supply Rejection | PSRR | $V_{DUT\_}$ = -2.0V and +6.0V (Notes 24, 28) | 50 | 60 | | dB |
| **COMPARATOR AC CHARACTERISTICS (Notes 29–32)** | | | | | | |
| Effective Comparator Bandwidth, Term Mode | | (Notes 4, 33) | 2.0 | 4.0 | | GHz |
| Effective Comparator Bandwidth, High-Impedance Mode | | (Note 34) | | 800 | | MHz |
| Minimum Pulse Width | | (Notes 4, 35) | | 0.5 | 0.65 | ns |
| Propagation Delay | | | 0.35 | 0.9 | 1.5 | ns |
| Propagation-Delay Temperature Coefficient | | | | 1.7 | | ps/°C |
| Channel-to-Channel Propagation-Delay Match, High/High vs. Low/Low | | | | 15 | | ps |
| **PROPAGATION-DELAY DISPERSIONS** | | | | | | |
| Propagation-Delay Dispersion vs. Common-Mode Input | | $V_{CM}$ = -1.9V to +5.9V (Notes 4, 36) | | 40 | 55 | ps |
| Propagation-Delay Dispersion vs. Duty Cycle | | 0.6ns to 24.4ns pulse width, relative to 12.5ns pulse width, (Notes 4, 37) | | ±25 | ±45 | ps |
| Propagation-Delay Dispersion vs. Slew Rate | | 1.0V/ns to 6.0V/ns, relative to 2.0V/ns (Note 4) | | ±30 | ±40 | ps |
| Waveform Tracking (Notes 4, 38) | | Driver in term mode, peak-to-peak within 100mV < $V_{CMPV}$ < 900mV window | | 50 | 80 | ps |
| | | Driver in term mode, peak-to-peak within 50mV < $V_{CMPV}$ < 950mV window | | 80 | 130 | |
| | | Driver in high impedance, peak-to-peak within 100mV < $V_{CMPV}$ < 900mV window | | 150 | 200 | ps |
| **LOGIC OUTPUTS CMP, NCMP (CMP, NCMP collector output, $R_L$ = 50Ω internal pullup to CTV) (Note 39)** | | | | | | |
| Termination Voltage CTV | | External termination voltage | 0 | 1.2 | 3.5 | V |
| CTV Current | | Total current for user-supplied termination voltage | | 12 | 14 | mA |
| Output High Voltage | | | $V_{CTV}$ - 0.1 | $V_{CTV}$ - 0.02 | $V_{CTV}$ + 0.05 | V |
| Output Low Voltage | | | $V_{CTV}$ - 0.45 | $V_{CTV}$ - 0.3 | $V_{CTV}$ - 0.25 | V |

## Electrical Characteristics (continued)

($V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{HHP}$ = +17.5V, $V_{DD}$ = +3.3V, $V_{DHV\_}$ = +3V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DATV\_}$ = $V_{RTV\_}$ = 0V, $V_{CTV}$ = +1.2V, $V_{CMPV}$ = +1V, $V_{VHH}$ = +10V, CDRP__ = 000b, RO_ = 1110b, SC_ = 00b, $V_{DGS}$ = $V_{GND}$ = $V_{GNDDAC\_\_}$ = 0V, specifications apply after calibration, level-setter errors included. The device is tested at $T_J$ = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at $T_J$ = +40°C and +100°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output-Voltage Swing | | | 250 | 300 | 350 | mV |
| Output Termination Resistor | | | 47 | | 53 | Ω |
| Differential Rise Time | | 10% to 90% (Notes 4, 32) | | 210 | 400 | ps |
| Differential Fall Time | | 10% to 90% (Notes 4, 32) | | 210 | 400 | ps |
| **TEMPERATURE MONITOR** | | | | | | |
| Nominal Voltage | | $T_J$ = +70°C, $R_L$ ≥ 10MΩ | | 3.43 | | V |
| Nominal Voltage Variation | | $T_J$ = +125°C, $R_L$ ≥ 10MΩ, one standard deviation | | ±50 | | mV |
| Temperature Coefficient | | | | 10 | | mV/°C |
| Output Resistance | | | | 22 | | kΩ |
| High-Impedance Leakage Current | | $V_{TMPSNS}$ = +4V, TSMUX0 = 0 | | | 1 | µA |
| **TEMPERATURE COMPARATOR/ALARM** | | | | | | |
| Comparator Hysteresis | | | | 0 | | mV |
| Alarm Threshold | | | | +125 | | °C |
| Temperature Alarm Accuracy | | | | ±5 | | °C |
| **DIGITAL I/O** | | | | | | |
| **DIFFERENTIAL CONTROL INPUTS (DATA_, NDATA_, RCV_, NRCV_)** | | | | | | |
| Input High Voltage | $V_{IH}$ | Functional test | +0.2 | | +3.5 | V |
| Input Low Voltage | $V_{IL}$ | Functional test | -0.2 | | +3.1 | V |
| Differential Input Voltage | | Functional test | ±0.15 | | ±1.0 | V |
| Differential Termination Resistance | | Differential termination between DATA_/ NDATA_ and RCV_/NRCV_, tested at ±4mA | 96 | | 104 | Ω |
| **SINGLE-ENDED INPUTS ($\overline{CS}$, SCLK, DIN, $\overline{RST}$, $\overline{LOAD}$, $\overline{ENVHH}$)** | | | | | | |
| Input High | | | 2/3 x $V_{DD}$ | | $V_{DD}$ | V |
| Input Low | | | -0.1 | | 1/3 x $V_{DD}$ | V |
| Input Bias Current | | | | | ±25 | µA |
| **SINGLE-ENDED OUTPUT (DOUT)** | | | | | | |
| High Output | $V_{OH}$ | $I_{OH}$ = 25µA | $V_{DD}$ - 0.15 | | | V |
| Low Output | $V_{OL}$ | $I_{OL}$ = -25µA | | | $V_{DGND}$ + 0.15 | V |
| **SINGLE-ENDED OPEN-DRAIN OUTPUTS (OVALARM, TALARM with external 1kΩ to $V_{DD}$)** | | | | | | |
| Voltage Range | $V_{VOC}$ | | $V_{DD}$ - 0.3 | | $V_{DD}$ + 0.3 | V |
| Low Output | $V_{OL}$ | | $V_{DGND}$ | | $V_{VOC}$ - 1.0 | V |

## Electrical Characteristics (continued)

($V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{HHP}$ = +17.5V, $V_{DD}$ = +3.3V, $V_{DHV\_}$ = +3V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DATV\_}$ = $V_{RTV\_}$ = 0V, $V_{CTV}$ = +1.2V, $V_{CMPV}$ = +1V, $V_{VHH}$ = +10V, CDRP__ = 000b, RO_ = 1110b, SC_ = 00b, $V_{DGS}$ = $V_{GND}$ = $V_{GNDDAC\_\_}$ = 0V, specifications apply after calibration, level-setter errors included. The device is tested at $T_J$ = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at $T_J$ = +40°C and +100°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **SERIAL-PORT TIMING (See Figure 3)** | | | | | | |
| SCLK Frequency | | | | | 50 | MHz |
| SCLK Pulse-Width High | $t_{CH}$ | | 10 | | | ns |
| SCLK Pulse-Width Low | $t_{CL}$ | | 10 | | | ns |
| $\overline{CS}$ Low to SCLK High Setup | $t_{CSS0}$ | | 4.25 | | | ns |
| SCLK High to $\overline{CS}$ Low Hold | $t_{CSH0}$ | | 4.25 | | | ns |
| $\overline{CS}$ High to SCLK High Setup | $t_{CSS1}$ | | 4.25 | | | ns |
| SCLK High to $\overline{CS}$ High Hold | $t_{CSH1}$ | | 4.25 | | | ns |
| DIN to SCLK High Setup | $t_{DS}$ | | 4.25 | | | ns |
| DIN to SCLK High Hold | $t_{DH}$ | | 4.25 | | | ns |
| $\overline{CS}$ High Pulse Width | $t_{CSWH}$ | | 40 | | | ns |
| $\overline{LOAD}$ Low Pulse Width | $t_{LDW}$ | | 20 | | | ns |
| $\overline{RST}$ Low Pulse Width | $t_{RST}$ | | 25 | | | ns |
| $\overline{CS}$ High to $\overline{LOAD}$ Low Hold | $t_{CSHLD}$ | | 50 | | | ns |
| SCLK to DOUT Delay | $t_{DO}$ | | | | 62.4 | ns |
| **COMMON FUNCTIONS ($V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{DD}$ = +3.3V, $V_{HHP}$ = +17.5V, unless otherwise noted)** | | | | | | |
| Operating Voltage Range | | | -2.0 | | +13 | V |
| High-Impedance Mode Leakage | $I_{DUT}$ | $V_{CMPV}$ = +6.0V, $V_{DUT\_}$ = -2.0V, CMP_EN = high | | | ±50 | µA |
| | | $V_{CMPV}$ = -2.0V, $V_{DUT\_}$ = +6.0V, CMP_EN = high | | | ±50 | |
| Low-Leak Mode Leakage | $I_{DUT}$ | $V_{DUT\_}$ = -2.0V and +6.0V (Note 40) | | | ±100 | nA |
| Combined Capacitance | | Driver in terminate mode (Note 4) | | 0.5 | 1.0 | pF |
| | | Driver in high impedance | | 3 | | |
| Low-Leak Enable Time | | $\overline{CS}$ high for setting LLEAKS_ high to $I_{DUT\_}$ specification | | 20 | | µs |
| Low-Leak Disable Time | | $\overline{CS}$ high for setting LLEAKS_ low to normal operation | | 20 | | µs |
| Low-Leak Spike, $V_{DLV\_}$/Leak | | $V_{DLV\_}$ = 0V, $Z_L$ = 10MΩ || 8pF to GND (Note 4) | -200 | | +600 | mV |
| Low-Leak Spike, $V_{DHV\_}$/Leak | | $V_{DHV\_}$ = +2V, $Z_L$ = 10MΩ || 8pF to GND (Note 4) | -200 | | +350 | mV |
| Low-Leak Spike, High-Impedance/Leak | | $R_L$ = 50Ω to GND (Note 4) | -125 | | +350 | mV |
| **DUT_ OVERVOLTAGE ALARM** | | | | | | |
| Maximum Programmable OVHV | | | 6.7 | 7.0 | | V |
| Minimum Programmable OVLV | | | | -3.0 | -2.7 | V |

## Electrical Characteristics (continued)

($V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{HHP}$ = +17.5V, $V_{DD}$ = +3.3V, $V_{DHV\_}$ = +3V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DATV\_}$ = $V_{RTV\_}$ = 0V, $V_{CTV}$ = +1.2V, $V_{CMPV}$ = +1V, $V_{VHH}$ = +10V, CDRP__ = 000b, RO_ = 1110b, SC_ = 00b, $V_{DGS}$ = $V_{GND}$ = $V_{GNDDAC\_\_}$ = 0V, specifications apply after calibration, level-setter errors included. The device is tested at $T_J$ = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at $T_J$ = +40°C and +100°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Voltage Accuracy | | Includes gain, offset, and linearity errors over full alarm range, $V_{OVHV}$ = +6.7V and $V_{OVLV}$ = -2.7V | | | 150 | mV |
| Comparator Delay | | With 50mV overdrive on DUT_ signal | | 390 | | ns |
| Comparator Hysteresis | | | | 7 | | mV |
| Minimum Alarm Setting Voltage | $V_{OVHV}$ - $V_{OVLV}$ | | | 2 | | V |
| **POWER SUPPLIES** | | | | | | |
| Positive Supply | $V_{CC}$ | | 9.0 | 9.25 | 10.0 | V |
| Negative Supply | $V_{EE}$ | | -5.35 | -5.25 | -4.75 | V |
| Logic Supply | $V_{DD}$ | | 2.3 | 3.3 | 3.6 | V |
| High Voltage Supply | $V_{HHP}$ | | 17 | 17.5 | 18 | V |
| Positive Supply Current | $I_{CC}$ | (Note 41) | | 180 | 230 | mA |
| Negative Supply Current | $I_{EE}$ | (Note 41) | | 210 | 270 | mA |
| Logic Supply Current | $I_{DD}$ | (Note 41) | | 11 | 20 | mA |
| High-Voltage Supply Current | $I_{HH}$ | (Note 41) | | 2.0 | 4.0 | mA |
| | | VHH mode, all channels enabled (Note 41) | | 60 | 70 | |
| Power Dissipation | | $V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{DD}$ = +3.3V, $V_{HHP}$ = +17.5V, LLEAKS_ = 0, CMP_EN = 0, $\overline{ENVHH}$ = high, ENVHHS_ = 0 | | 0.7 | 0.8 | W/Ch |
| | | $V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{DD}$ = +3.3V, $V_{HHP}$ = +17.5V, LLEAKS_ = 0, CMP_EN = 1, $\overline{ENVHH}$ = high, ENVHHS_ = 0 | | 0.74 | 0.90 | |
| **ANALOG INPUTS (DUT_ ground sense)** | | | | | | |
| Input Range | $V_{DGS}$ | Relative to GNDDAC__, under the full DAC range (Note 42) | | <±250 | | mV |
| | | Relative to GNDDAC__, under the limited DAC range of -1.5V to +5.5V, for VHH the DAC range is limited to 0.5V to 12.25V (Note 43) | | <±750 | | mV |
| Input Bias Current | | $V_{DGS}$ = 0V | -10 | | +10 | µA |
| Gain | | DGS gain for DHV_, DLV_, DTV_, CMPV | | 1±2% | | V/V |
| | | DGS gain for VHH | | 1±3% | | |
| **2.5V REFERENCE** | | | | | | |
| Nominal Voltage | $V_{REF}$ | | | 2.5 | | V |
| Input Bias Current | | | -10 | | +10 | µA |

## Electrical Characteristics (continued)

($V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{HHP}$ = +17.5V, $V_{DD}$ = +3.3V, $V_{DHV\_}$ = +3V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DATV\_}$ = $V_{RTV\_}$ = 0V, $V_{CTV}$ = +1.2V, $V_{CMPV}$ = +1V, $V_{VHH}$ = +10V, CDRP__ = 000b, RO_ = 1110b, SC_ = 00b, $V_{DGS}$ = $V_{GND}$ = $V_{GNDDAC\_\_}$ = 0V, specifications apply after calibration, level-setter errors included. The device is tested at $T_J$ = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at $T_J$ = +40°C and +100°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DRIVER VHH DC CHARACTERISTICS** | | | | | | |
| Output Voltage Range | $V_{VHH}$ | DGS = AGND; for DGS ≠ AGND, refer to the DGS gain specification | 0 | | 13 | V |
| DC Output Voltage | | $V_{VHH}$ = +13V, $I_{DUT}$ = 10mA | | 12.45 | | V |
| | | $V_{VHH}$ = 0V, $I_{DUT}$ = -10mA | | 0.55 | 0.75 | |
| Current Limit | | $V_{VHH}$ = +13V, $V_{DUT}$ = 0V and $V_{VHH}$ = 0V, $V_{DUT\_}$ = +13V | ±12 | | ±27 | mA |
| Offset Voltage | | $V_{VHH}$ = +7.75V | | | ±30 | mV |
| Output-Voltage Temperature Coefficient | $V_{VHH\_TC}$ | (Note 3) | | ±75 | ±500 | µV/°C |
| Normalized Gain | | $V_{VHH}$ = +7.75V, +12.75V | 0.998 | 1.000 | 1.002 | V/V |
| Linearity Relative to +7.75V, +12.75V | | $V_{VHH}$ = +7.0 to +13.0V | | | ±14 | mV |
| Linearity Relative to +1.5V, +12.75V | | $V_{VHH}$ = 0.0V to +13.0V | | | ±30 | mV |
| Output Resistance | | $I_{DUT}$ = ±2mA, $V_{VHH}$ = +1V | 45 | 55 | 75 | Ω |
| Power-Supply Rejection Ratio | | $V_{CC}$, $V_{EE}$, $V_{HHP}$ independently varied over their allowed ranges | | 20 | | mV/V |
| **DRIVER VHH AC CHARACTERISTICS ($R_L$ ≥ 10MΩ, $C_{DUT\_}$ = 100pF)** | | | | | | |
| VHH Rise/Fall Times | | $V_{DHV\_}$ = +3V, $V_{VHH}$ = +13V, 10% to 90% | | | 250 | ns |
| VHH Overshoot | | $V_{DHV\_}$ = +3V, $V_{VHH}$ = +13V (Note 3) | | | 180 | mV |
| **LEVEL DACs** | | | | | | |
| Settling Time | | Full-scale transition to within 5mV | | 20 | | µs |
| Differential Nonlinearity | | All levels not shown below, 1 LSB = 610µV | | < ±1 | | mV |
| | | VHH | | < ±2 | | |
| | | OVHV, OVLV | | < ±39 | | |

**Note 2:** $V_{DHV\_}$, $V_{DLV\_}$, and $V_{DTV\_}$ levels are calibrated for gain at +0.125V and +3.875V and are calibrated for offset at +0.125V; relative to straight line between +0.125V and +3.875V.

**Note 3:** Change in level over operating range. Includes both gain and offset temperature effects. Simulated over entire +40°C to +100°C junction operating range. Verified at worst-case points, which are at the endpoints $V_{DHV\_}$ - $V_{DLV\_}$ R 200mV.

**Note 4:** Guaranteed by design and characterization.

**Note 5:** DATA_ = high, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, $I_{OUT}$ = ±30mA. Nominal target value is 48Ω.

**Note 6:** Resistance measurements are made using ±2.5mA current changes in the loading instrument about the noted value. Absolute value of the difference in measured resistance over the specified range, tested separately for each current polarity. Test conditions at $I_{DUT}$ are ±1mA, ±12mA, and ±40mA, respectively.

**Note 7:** Rise time of the differential inputs DATA_ and RCV_ is 150ps (10% to 90%). SC1 = SC0 = 0, 40MHz, unless otherwise specified.

**Note 8:** Current supplied for a minimum of 10ns. Verified to be greater than or equal to DC drive current by design and characterization.

**Note 9:** Measured from the 90% point of the driver output (relative to its final value) to the waveform settling to within the specified limit.

**Note 10:** Propagation delays are measured from the crossing point of the differential input signals to the 50% point of expected output swing.

**Note 11:** Average of the two measurements for propagation delay, $t_{LH}$ and $t_{HL}$.

**Note 12:** Average of the four measurements in propagation delay, drive to high impedance, and high impedance to drive ($t_{LZ}$, $t_{HZ}$, $t_{ZL}$, and $t_{ZH}$). Measured from crossing point of RCV_/NRCV_ to 50% point of the output waveform.

## Electrical Characteristics (continued)

($V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{HHP}$ = +17.5V, $V_{DD}$ = +3.3V, $V_{DHV\_}$ = +3V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DATV\_}$ = $V_{RTV\_}$ = 0V, $V_{CTV}$ = +1.2V, $V_{CMPV}$ = +1V, $V_{VHH}$ = +10V, CDRP__ = 000b, RO_ = 1110b, SC_ = 00b, $V_{DGS}$ = $V_{GND}$ = $V_{GNDDAC\_\_}$ = 0V, specifications apply after calibration, level-setter errors included. The device is tested at $T_J$ = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at $T_J$ = +40°C and +100°C, unless otherwise noted.)

**Note 13:** Four measurements are made: $V_{DHV\_}$ to high impedance, $V_{DLV\_}$ to high impedance, high impedance to $V_{DHV\_}$, and high impedance to $V_{DLV\_}$ ($t_{LZ}$, $t_{HZ}$, $t_{ZL}$, and $t_{ZH}$). The worst-case difference is calculated.

**Note 14:** Average of the four measurements in propagation delay, drive to term, and term to drive ($t_{LT}$, $t_{HT}$, $t_{TL}$, and $t_{TH}$) . Measured from the crossing point of RCV_/NRCV_ to the 50% point of the output waveform.

**Note 15:** Four measurements are made: $V_{DHV\_}$ to $V_{DTV\_}$, $V_{DLV\_}$ to $V_{DTV\_}$, $V_{DTV\_}$ to $V_{DHV\_}$, and $V_{DTV\_}$ to $V_{DLV\_}$ ($t_{LT}$, $t_{HT}$, $t_{TL}$, and $t_{TH}$). The worst-case difference is calculated.

**Note 16:** Cable-droop compensation disabled. Measured as close as possible to DUT_ using a high-bandwidth cable.

**Note 17:** Cable-droop compensation enabled. Measured at end of 2m RG174 cable.

**Note 18:** There should not be a systemic mismatch in rise vs. fall time or $t_{LH}$ vs. $t_{HL}$.

**Note 19:** Functionally tested during production.

**Note 20:** At this pulse width, the output reaches at least 95% of its nominal (DC) amplitude. The pulse width is measured at the DATA_ (input) pins.

**Note 21:** Maximum data rate in transitions/second. A waveform that reaches at least 95% of its programmed amplitude can be generated at one-half of this frequency.

**Note 22:** This specification is indicative of switching speed from $V_{DHV\_}$ or $V_{DLV\_}$ to $V_{DTV\_}$ and $V_{DTV\_}$ to $V_{DHV\_}$ or $V_{DLV\_}$ when $V_{DLV\_}$ < $V_{DTV\_}$ < $V_{DHV\_}$. If $V_{DTV\_}$ < $V_{DLV\_}$ or $V_{DTV\_}$ > $V_{DHV\_}$, switching speed is degraded by roughly a factor of 3.

**Note 23:** The comparator tolerates the VHH level produced by the driver, but the specifications only apply for the -2.2V to +6.2V input voltage range.

**Note 24:** Measured by using a servo to locate comparator thresholds.

**Note 25:** Change in offset at any voltage over operating range. Includes both gain (CMRR) and offset temperature effects. Simulated over entire operating range. Verified at worst-case points, which are at the endpoints.

**Note 26:** Change in offset voltage over input range.

**Note 27:** Relative to straight line between +0.125V and +3.875V.

**Note 28:** Change in offset voltage with power supplies independently varied over their full range.

**Note 29:** All propagation delays measured from $V_{DUT\_}$ crossing calibrated $V_{CMPV}$ threshold to crossing point of differential outputs.

**Note 30:** All AC specifications are measured with the DUT_ pin (comparator input) as the reference.

**Note 31:** 40MHz, 0 to +2V input to comparator, $V_{CMPV}$ reference = +1.0V , 50% duty cycle 1ns rise/fall time, Zs = 50Ωs, driver in term mode with $V_{DTV\_}$ = +1.0V, unless otherwise noted.

**Note 32:** Use calibration comparator per channel and avoid any transition on deselected channel. If transitions cannot be avoided, keep deselected channels in low-leak mode to minimize coupling during calibration.

**Note 33:** Input rise/fall time = 45ps. 0 to 1.0V, 50% duty cycle.

**Note 34:** Input rise/fall time = 150ps. 0 to 1.0V, 50% duty cycle.

**Note 35:** At this pulse width, the output reaches at least 90% of its nominal peak-to-peak swing. The pulse width is measured at the crossing points of the differential outputs. 500ps rise/fall time. Timing specifications are not guaranteed.

**Note 36:** $V_{DUT\_}$ = 200m$V_{P-P}$, rise/fall time = 250ps, overdrive = 100mV, $V_{DTV\_}$ = $V_{CM}$. Valid for a common-mode range where the signal does not exceed the operating range. This specification is the worst-case (slowest to fastest) over the specified range.

**Note 37:** 0 to +1V input to comparator, $V_{CMPV}$ reference = +0.5V, input rise/fall time = 250ps.

**Note 38:** Input to comparator is 40MHz at 0 to +1.0V, 50% duty cycle, 1ns rise/fall time.

**Note 39:** Unless otherwise specified, comparator outputs are terminated with 50Ω to +1.2V and $V_{CTV}$ = +1.2V.

**Note 40:** While device is in low-leak mode, care must be taken to never present a voltage greater than $V_{CC}$ to the DUT_ node, as this can damage the part.

**Note 41:** At nominal supply voltages. Nominal values are $V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, and $V_{VHH}$ = +17.5V. Production tests are performed with worst-case supply conditions for each specification. Supply conditions are either min $V_{CC}$ and max $V_{EE}$ or max $V_{CC}$ and min $V_{EE}$. Some tests could require both conditions. Total current for device. $R_L$ ≥ 10MΩ.

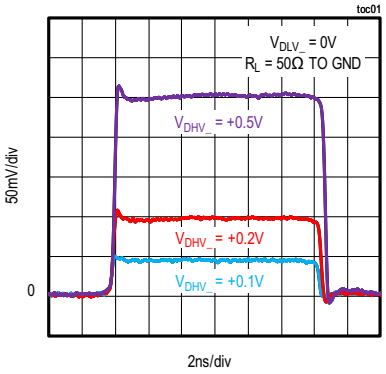
**Note 42:** Increasing DGS beyond 0V requires a proportional increase in the minimum supply levels. Specified ranges for all levels are defined with respect to DGS.

**Note 43:** Increasing DGS beyond 0V requires a proportional increase in the minimum supply levels. Limited range of -1.5V to +5.5V for all levels are defined with respect to DGS.

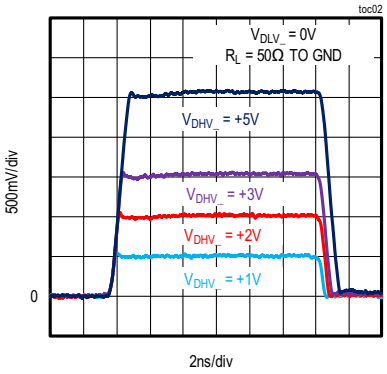
## Typical Operating Characteristics

($V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{HHP}$ = +17.5V, $V_{DD}$ = +3.3V, $V_{DHV\_}$ = +3V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DATV\_}$ = $V_{RTV\_}$ = GND, $V_{CTV}$ = +1.2V, $V_{CMPV\_}$ = +1V, $V_{VHH}$ = +10V, CDRP__ = 000b, RO_ = 1110b, SC = 00b, $V_{DGS}$ = $V_{GND}$ = $V_{GNDDAC\_\_}$ = 0V, specifications apply after calibration, level-setter errors included, $T_J$ = +70°C, temperature coefficients are measured at $T_J$ = +40°C and +100°C, unless otherwise noted.)

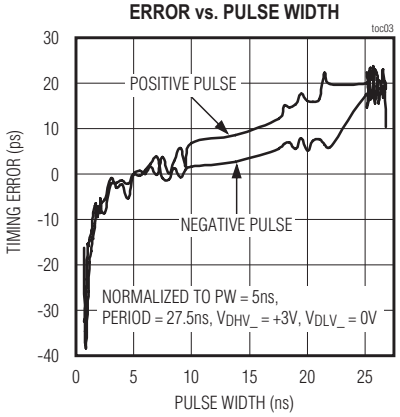
**DRIVER SMALL-SIGNAL RESPONSE**



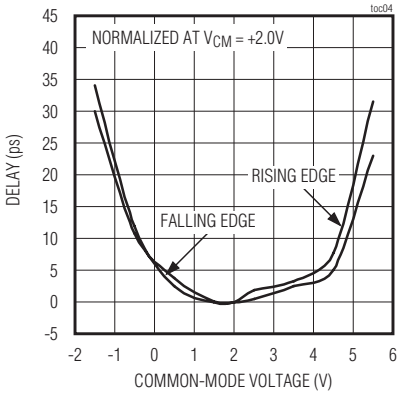

**DRIVER LARGE-SIGNAL RESPONSE**



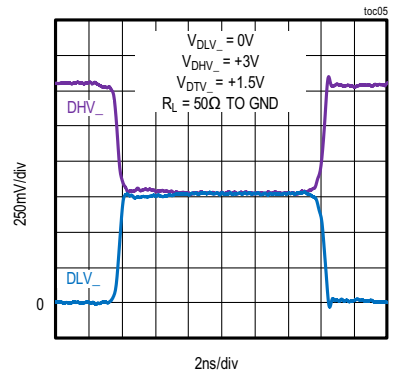

**DRIVER TRAILING-EDGE ERROR vs. PULSE WIDTH**



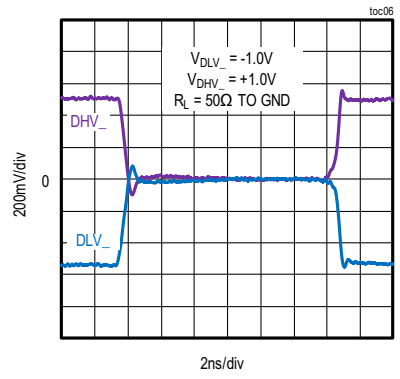

**DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE**




**DRIVER-TO-TERM TRANSITION**



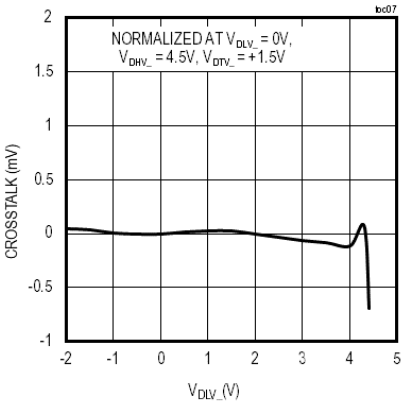

**DRIVER -TO-HIGH IMPEDANCE TRANSITION**



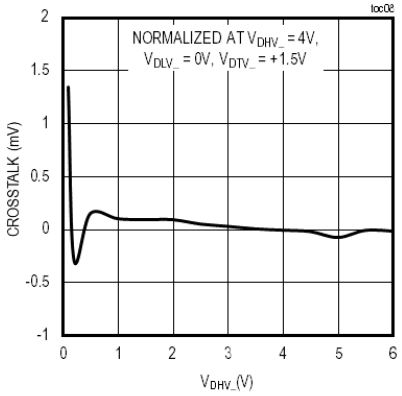
## Typical Operating Characteristics (continued)

($V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{HHP}$ = +17.5V, $V_{DD}$ = +3.3V, $V_{DHV\_}$ = +3V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DATV\_}$ = $V_{RTV\_}$ = GND, $V_{CTV}$ = +1.2V, $V_{CMPV\_}$ = +1V, $V_{VHH}$ = +10V, CDRP__ = 000b, RO_ = 1110b, SC = 00b, $V_{DGS}$ = $V_{GND}$ = $V_{GNDDAC\_\_}$ = 0V, specifications apply after calibration, level-setter errors included, $T_J$ = +70°C, temperature coefficients are measured at $T_J$ = +40°C and +100°C, unless otherwise noted.)

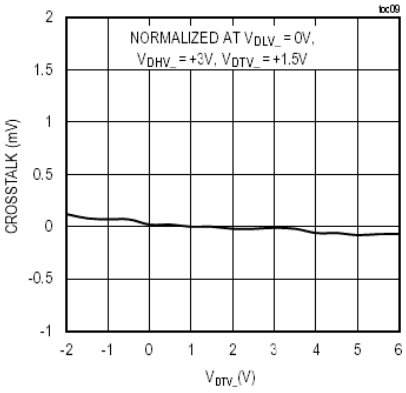
CROSSTALK TO DUT_
FROM DLV_ WITH DUT_ = DHV_



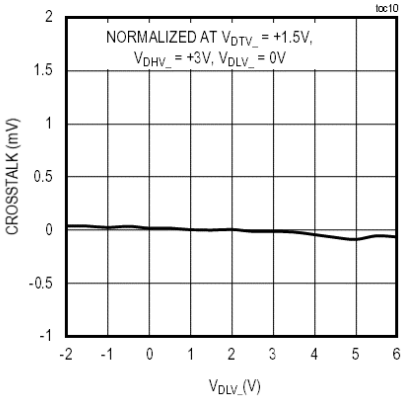

CROSSTALK TO DUT_
FROM DHV_ WITH DUT_ = DLV_



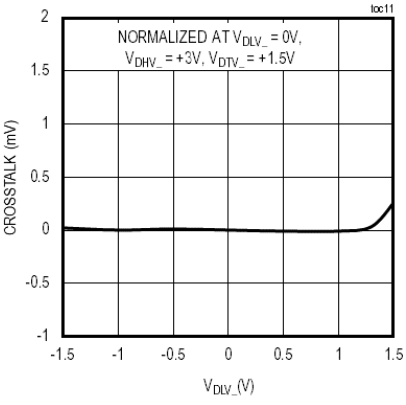

CROSSTALK TO DUT_
FROM DTV_ WITH DUT_ = DHV_



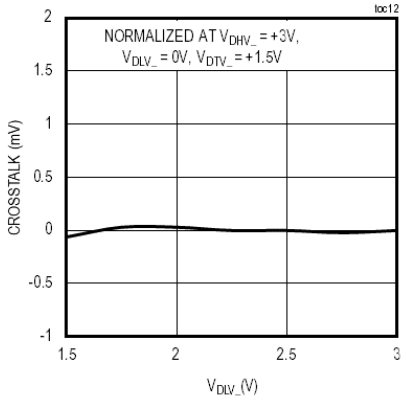

CROSSTALK TO DUT_
FROM DTV_ WITH DUT_ = DLV_




CROSSTALK TO DUT_
FROM DLV_ WITH DUT_ = DHV_



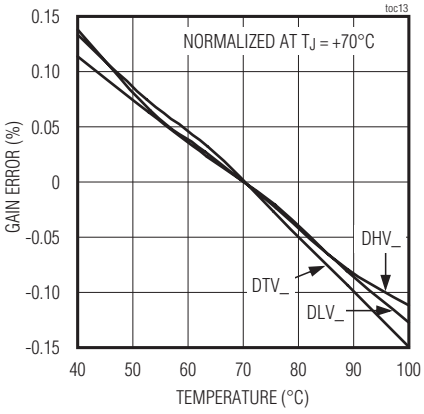

CROSSTALK TO DUT_
FROM DHV_ WITH DUT_ = DTV_



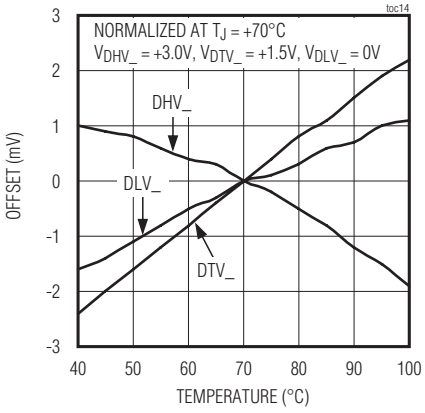
## Typical Operating Characteristics (continued)

($V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{HHP}$ = +17.5V, $V_{DD}$ = +3.3V, $V_{DHV\_}$ = +3V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DATV\_}$ = $V_{RTV\_}$ = GND, $V_{CTV}$ = +1.2V, $V_{CMPV\_}$ = +1V, $V_{VHH}$ = +10V, CDRP__ = 000b, RO_ = 1110b, SC = 00b, $V_{DGS}$ = $V_{GND}$ = $V_{GNDDAC\_\_}$ = 0V, specifications apply after calibration, level-setter errors included, $T_J$ = +70°C, temperature coefficients are measured at $T_J$ = +40°C and +100°C, unless otherwise noted.)

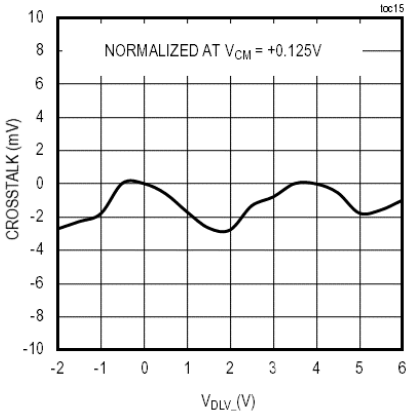
**DRIVER GAIN ERROR vs. TEMPERATURE**



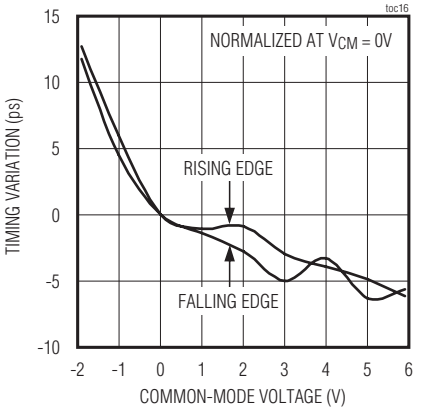

**DRIVER OFFSET vs. TEMPERATURE**



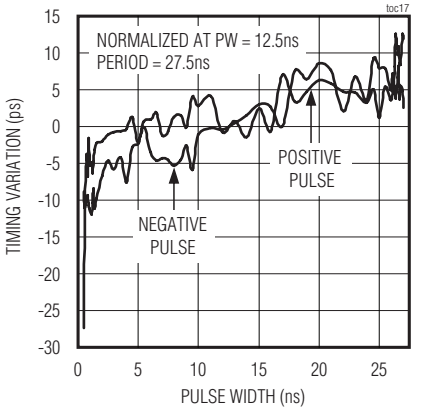

**COMPARATOR OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE**



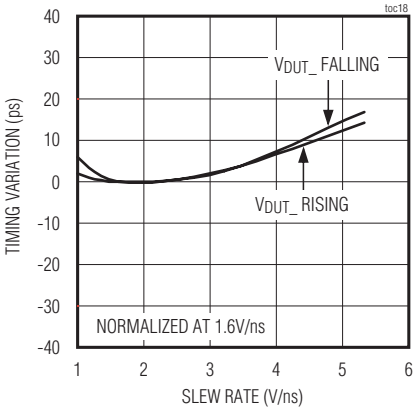

**COMPARATOR TIMING VARIATION vs. COMMON-MODE VOLTAGE**




**COMPARATOR TRAILING-EDGE TIMING VARIATION vs. PULSE WIDTH**



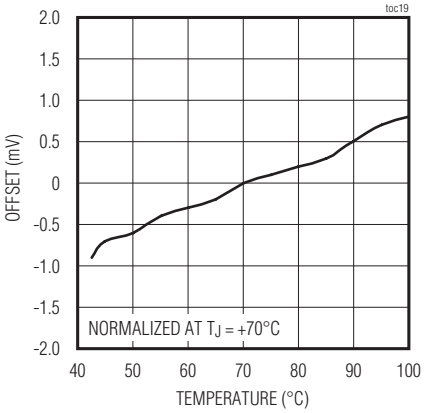

**COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE**



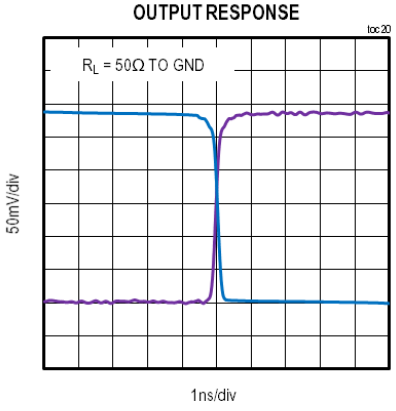
## Typical Operating Characteristics (continued)

($V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{HHP}$ = +17.5V, $V_{DD}$ = +3.3V, $V_{DHV\_}$ = +3V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DATV\_}$ = $V_{RTV\_}$ = GND, $V_{CTV}$ = +1.2V, $V_{CMPV\_}$ = +1V, $V_{VHH}$ = +10V, CDRP__ = 000b, RO_ = 1110b, SC = 00b, $V_{DGS}$ = $V_{GND}$ = $V_{GNDDAC\_\_}$ = 0V, specifications apply after calibration, level-setter errors included, $T_J$ = +70°C, temperature coefficients are measured at $T_J$ = +40°C and +100°C, unless otherwise noted.)

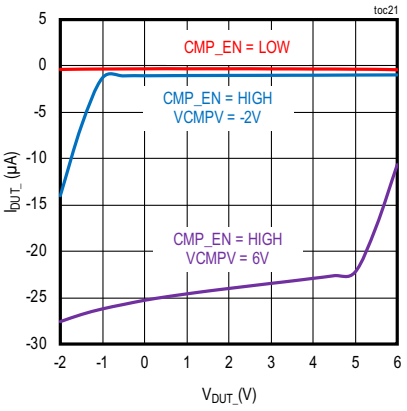
**COMPARATOR OFFSET vs. TEMPERATURE**



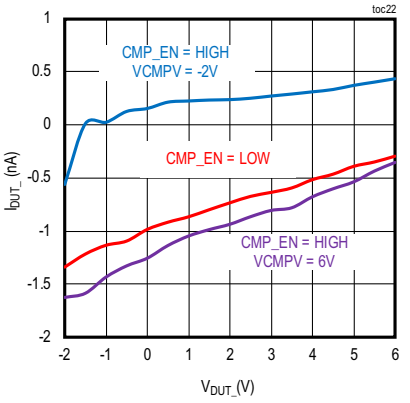

**COMPARATOR DIFFERENTIAL OUTPUT RESPONSE**



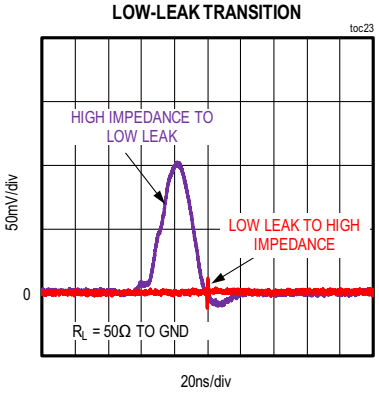

**HIGH IMPEDANCE LEAKAGE CURRENT vs. DUT_VOLTAGE**



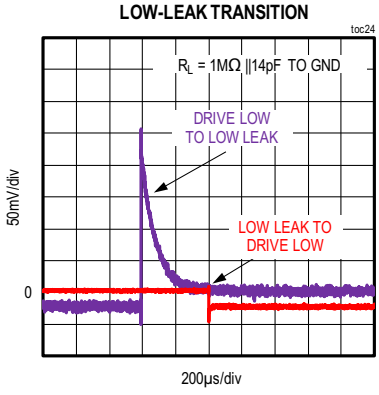

**LOW LEAKAGE CURRENT vs. DUT_VOLTAGE**




**HIGH IMPEDANCE TO LOW-LEAK TRANSITION**



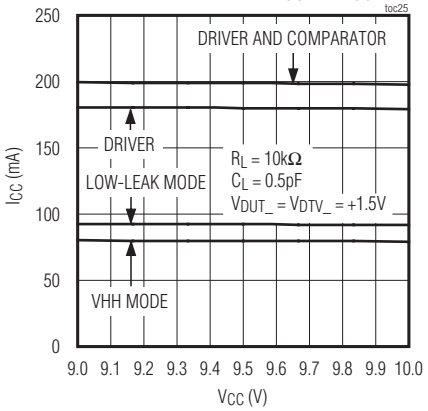

**DRIVE LOW TO LOW-LEAK TRANSITION**



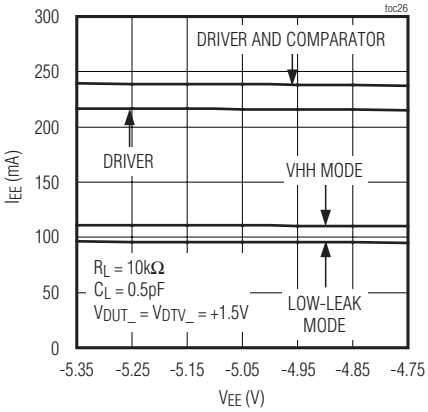
## Typical Operating Characteristics (continued)

($V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{HHP}$ = +17.5V, $V_{DD}$ = +3.3V, $V_{DHV\_}$ = +3V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DATV\_}$ = $V_{RTV\_}$ = GND, $V_{CTV}$ = +1.2V, $V_{CMPV\_}$ = +1V, $V_{VHH}$ = +10V, CDRP__ = 000b, RO_ = 1110b, SC = 00b, $V_{DGS}$ = $V_{GND}$ = $V_{GNDDAC\_\_}$ = 0V, specifications apply after calibration, level-setter errors included, $T_J$ = +70°C, temperature coefficients are measured at $T_J$ = +40°C and +100°C, unless otherwise noted.)

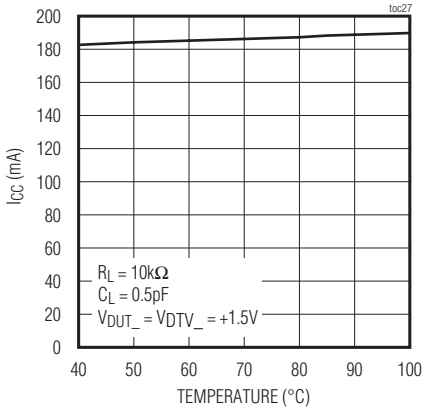
**SUPPLY CURRENT $I_{CC}$ vs. $V_{CC}$**



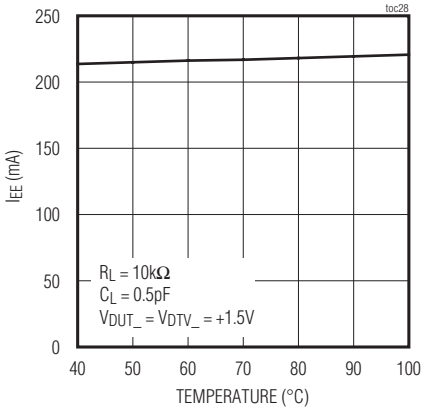

**SUPPLY CURRENT $I_{EE}$ vs. $V_{EE}$**



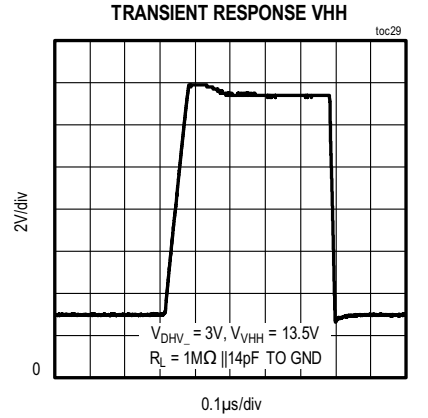

**SUPPLY CURRENT $I_{CC}$ vs. TEMPERATURE**



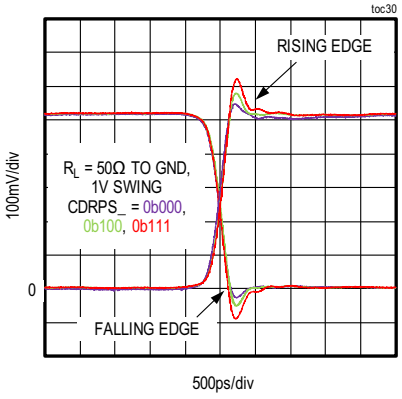

**SUPPLY CURRENT $I_{EE}$ vs. TEMPERATURE**




**TRANSIENT RESPONSE VHH**



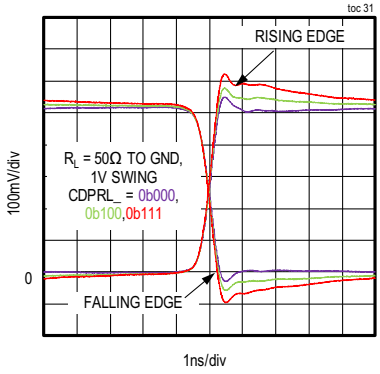

**DRIVER CABLE-DROOP COMPENSATION SHORT TIME**



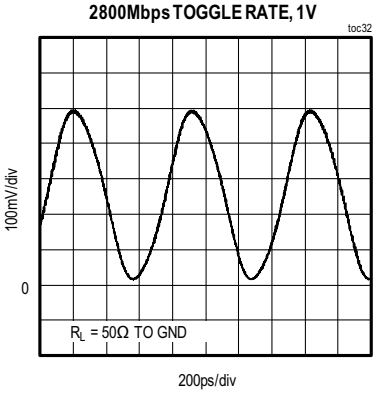
## Typical Operating Characteristics (continued)

($V_{CC}$ = +9.25V, $V_{EE}$ = -5.25V, $V_{HHP}$ = +17.5V, $V_{DD}$ = +3.3V, $V_{DHV\_}$ = +3V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DATV\_}$ = $V_{RTV\_}$ = GND, $V_{CTV}$ = +1.2V, $V_{CMPV\_}$ = +1V, $V_{VHH}$ = +10V, CDRP__ = 000b, RO_ = 1110b, SC = 00b, $V_{DGS}$ = $V_{GND}$ = $V_{GNDDAC\_\_}$ = 0V, specifications apply after calibration, level-setter errors included, $T_J$ = +70°C, temperature coefficients are measured at $T_J$ = +40°C and +100°C, unless otherwise noted.)

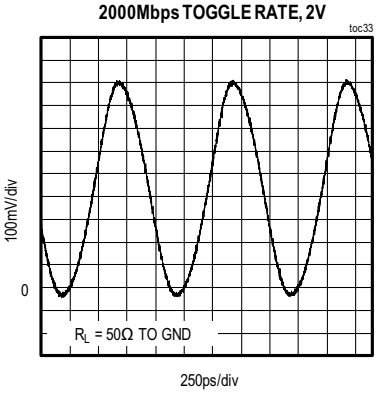
**DRIVER CABLE-DROOP COMPENSATION LONG TIME**



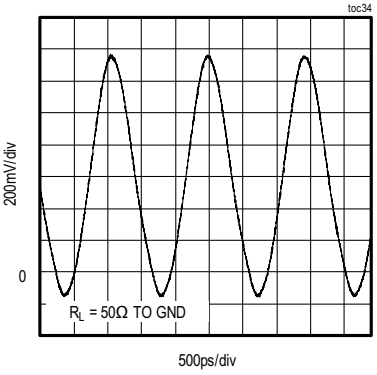

**DRIVER 2800Mbps TOGGLE RATE, 1V**



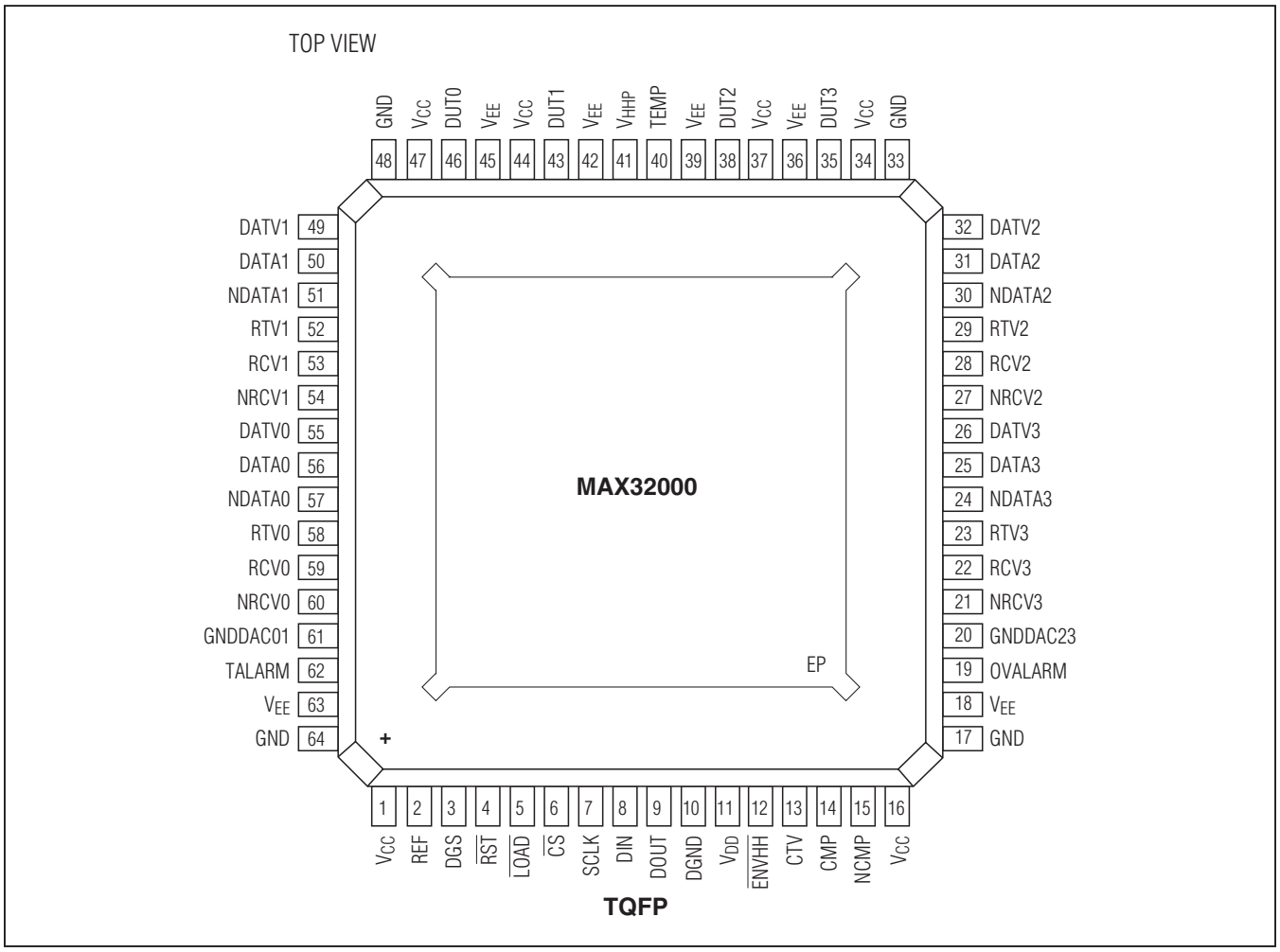

**DRIVER 2000Mbps TOGGLE RATE, 2V**




**DRIVER 1400Mbps TOGGLE RATE, 3V**



## Pin Configuration



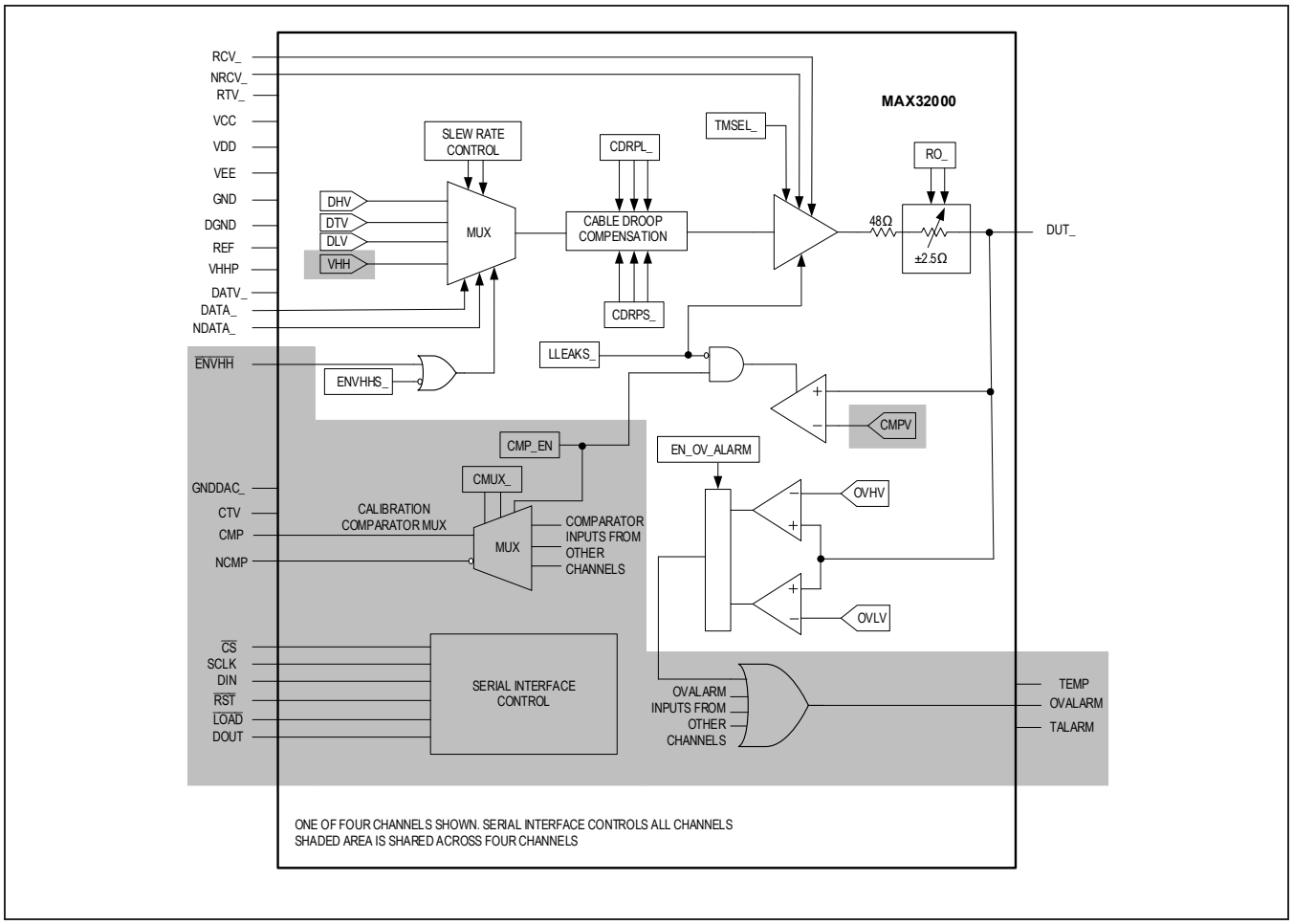
## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1, 16, 34, 37, 44, 47 | $V_{CC}$ | Positive Power Supply |
| 2 | REF | DAC 2.5V Reference Input. Set REF with respect to GNDDAC__. |
| 3 | DGS | Device Under Test Ground-Sense Input |
| 4 | $\overline{RST}$ | Active-Low Serial-Port Reset Input |
| 5 | $\overline{LOAD}$ | Active-Low Serial-Port Load Input |
| 6 | $\overline{CS}$ | Active-Low Serial-Port Chip-Select Input |
| 7 | SCLK | Serial-Port Clock Input |
| 8 | DIN | Serial-Port Data Input |
| 9 | DOUT | Serial-Port Data Output |
| 10 | DGND | Digital Ground |
| 11 | $V_{DD}$ | Logic Power Supply |
| 12 | $\overline{ENVHH}$ | Active-Low High-Voltage-Enable Input |
| 13 | CTV | Comparator Termination Voltage |
| 14 | CMP | Comparator Output |
| 15 | NCMP | Comparator-Output Complement |
| 17, 33, 48, 64 | GND | Analog Ground |
| 18, 36, 39, 42, 45, 63 | $V_{EE}$ | Negative Power Supply |
| 19 | OVALARM | Overvoltage Alarm Output |
| 20 | GNDDAC23 | Channels 2 and 3 DAC Ground |
| 21 | NRCV3 | Channel 3 Receive Input Complement |
| 22 | RCV3 | Channel 3 Receive Input |
| 23 | RTV3 | Channel 3 Receive Termination Voltage |
| 24 | NDATA3 | Channel 3 Data Input Complement |
| 25 | DATA3 | Channel 3 Data Input |
| 26 | DATV3 | Channel 3 Data Termination Voltage |
| 27 | NRCV2 | Channel 2 Receive Input Complement |
| 28 | RCV2 | Channel 2 Receive Input |
| 29 | RTV2 | Channel 2 Receive Termination Voltage |
| 30 | NDATA2 | Channel 2 Data Input Complement |
| 31 | DATA2 | Channel 2 Data Input |
| 32 | DATV2 | Channel 2 Data Termination Voltage |
| 35 | DUT3 | Channel 3 Input/Output |
| 38 | DUT2 | Channel 2 Input/Output |
| 40 | TEMP | Temperature Sensor Output |
| 41 | $V_{HHP}$ | High-Voltage Power Supply |
| 43 | DUT1 | Channel 1 Input/Output |
| 46 | DUT0 | Channel 0 Input/Output |
| 49 | DATV1 | Channel 1 Data Termination Voltage |
| 50 | DATA1 | Channel 1 Data Input |
| 51 | NDATA1 | Channel 1 Data Input Complement |

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 52 | RTV1 | Channel 1 Receive Termination Voltage |
| 53 | RCV1 | Channel 1 Receive Input |
| 54 | NRCV1 | Channel 1 Receive Input Complement |
| 55 | DATV0 | Channel 0 Data Termination Voltage |
| 56 | DATA0 | Channel 0 Data Input |
| 57 | NDATA0 | Channel 0 Data Input Complement |
| 58 | RTV0 | Channel 0 Receive Termination Voltage |
| 59 | RCV0 | Channel 0 Receive Input |
| 60 | NRCV0 | Channel 0 Receive Input Complement |
| 61 | GNDDAC01 | Channels 0 and 1 DAC Ground |
| 62 | TALARM | Temperature Alarm Output |
| — | EP | Exposed Pad. EP is internally connected to $V_{EE}$. Connect to $V_{EE}$ or leave unconnected. Do not use EP as a primary connection to $V_{EE}$. |

## Block Diagram



## Detailed Description

The MAX32000 quad-channel, pin-electronics driver integrates multiple pin-electronics functions into a single IC. Each channel includes a four-level pin driver, a shared calibration comparator, and five independent level-setting DACs (three 14-bit and two 8-bit). Additionally, each channel of the MAX32000 features programmable cable-droop compensation for the driver output, adjustable driver output resistance, and driver slew-rate adjustment.

The driver features a wide -2V to +6V high-speed operating range. In VHH mode, the output is from 0 to +13V. The MAX32000 also offers high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low-voltage swings. The driver provides high-speed differential control inputs compatible with most high-speed logic families. The calibration comparators provide extremely low timing variation over changes in slew rate, pulse width, or overdrive voltage, and provide 50Ω source outputs internally terminated to an applied voltage at CTV.

Independent low-leak control is provided for each channel. Placing the MAX32000 DUT_ output into a very low-leakage state disables the driver functions. An SPIK-compatible serial interface and external inputs configure the MAX32000.

### Integrated PE Mode Selection

The MAX32000 features two modes of operation, active and low leak. The MAX32000 enters low-leak mode when the LLEAKS_ bit is set to 1. The serial bits LLEAKS_ = 1 can be used to force the QDRV register to low-leak mode independent of other control bits. Setting LLEAKS_ to 0 is necessary to allow any other mode of operation (see *Table 1*). For SPI register bit assignments, see *Table 9*.

### Driver

The driver uses a high-speed multiplexer to select one of three DAC voltages ($V_{DHV\_}$, $V_{DLV\_}$, and $V_{DTV\_}$), high-impedance mode, or high-voltage mode (VHH). Multiplexer switching is controlled by high-speed differential inputs DATA_/NDATA_ and RCV_/NRCV_ and mode-control bits TMSEL_ and ENVHHS_ (see *Table 1*). The multiplexer output is buffered to drive DUT_. A programmable slew-rate circuit controls the slew rate of the buffer output.

In high-impedance mode, the comparator remains connected to DUT_, the DUT_ bias current is less than ±50µA, and the node continues to track high-speed signals. In low-leak mode, the bias current at DUT_ is further reduced to less than ±100nA, yet signal tracking slows down.

The nominal driver output resistance is 48Ω and features an adjustment range of ±2.5Ω through the serial interface in 360mI increments.

## Table 1. Driver Functional Overview

| LLEAKS_ (SPI BIT) | ENVHHS_* (SPI BIT) | $\overline{\text{ENVHH}}$** (EXTERNAL PIN) | TMSEL_ (SPI BIT) | RCV_ | DATA_ | DRIVER OUTPUT |
|---|---|---|---|---|---|---|
| 0 | X | 1 | X | 0 | 0 | Drive to DLV_ |
| 0 | X | 1 | X | 0 | 1 | Drive to DHV_ |
| 0 | 0 | 1 | 0 | 1 | X | High-impedance receive |
| 0 | 0 | 1 | 1 | 1 | X | Drive to DTV_ |
| 0 | 1 | X | X | 1 | X | Drive to VHH** |
| 0 | X | 0 | X | X | X | Drive to VHH** |
| 1 | X | X | X | X | X | Low leak |

*X = Don't care.*

**DHV_-to-DLV_ and DLV_-to-DHV_ transition times are not altered by the state of ENVHHS_.*

***Control of VHH is initiated either through the direct assertion of the $\overline{\text{ENVHH}}$ input, or in response to the assertion of the RCV_/NRCV_ high-speed inputs when ENVHHS_ = 1 in the QDRV register.*

***Note:** It is anticipated that the driver's VHH state is entered from one of the two drive states (DLV_ or DHV_) and not directly from the high-impedance or DTV_ states.*

### Driver Slew Control

A slew-rate circuit controls the slew rate of the buffer output. Select one of four possible slew rates according to *Table 2*. The speed of the internal multiplexer sets the 100% driver slew rate. SC1 and SC0 are set to 0 at power-up or when $\overline{RST}$ is forced low.

## Table 2. Driver Slew Control

| SC1 | SC0 | DRIVER SLEW RATE (%) |
|---|---|---|
| 0 | 0 | 100 |
| 0 | 1 | 75 |
| 1 | 0 | 50 |
| 1 | 1 | 25 |

### Driver Cable-Droop Compensation

The driver incorporates active cable-droop compensation (refer to Application Note 4338: *Cable-Loss Solutions*). At high frequencies, transmission-line effects from the tester signal delivery path (PCB trace, connectors, and cabling between the MAX32000 DUT_ output and the device under test itself) can degrade the output waveform fidelity at the DUT, resulting in a highly degraded or unusable signal. The compensation circuit counters this degradation by adding a double time-constant decaying waveform to the nominal output waveform (pre-emphasis). *Figure 1* shows a comparison between a typical driver and the MAX32000, and shows how droop compensation counters signal degradation. The maximum swing while maintaining the linear compensation of the driver cable droop is 4.4$V_{P-P}$. There are long-time-constant (1.2ns) control

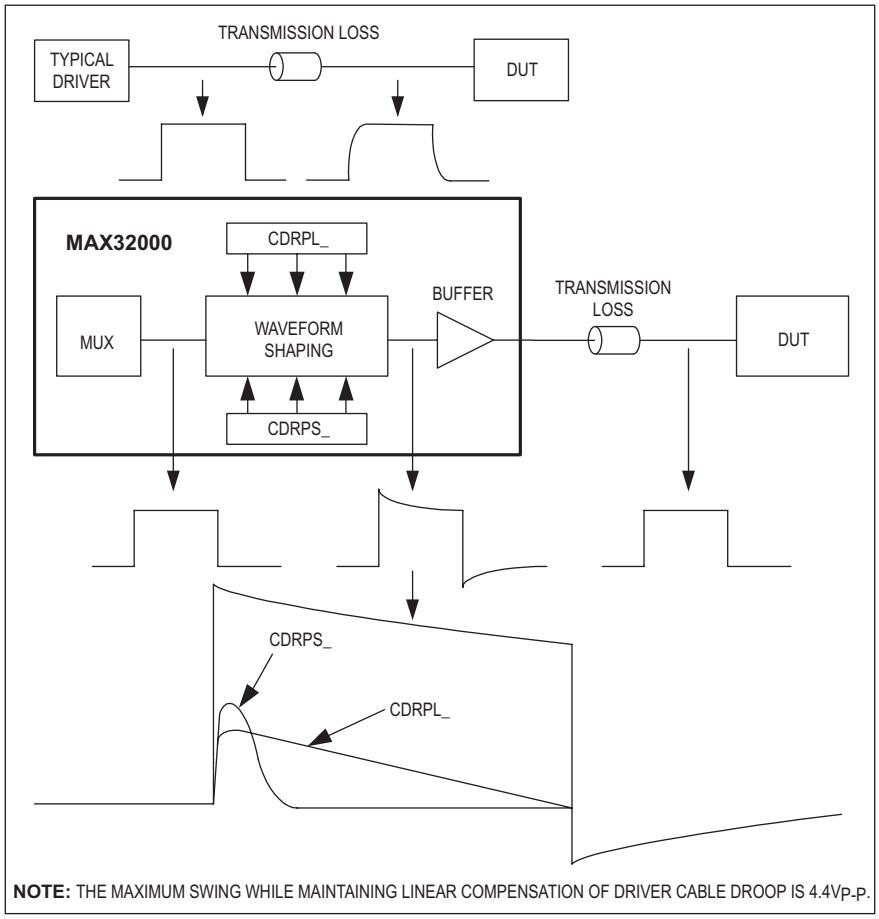



*Figure 1. Driver Cable-Droop Compensation*

bits, CDRPL[2:0], and short-time-constant (60ps) control bits, CDRPS[2:0], in the QDRV CAL register to set the amount of compensation. Control bits CDRP_[2:0] vary the amplitude of the compensation signal. *Table 3* and *Table 4* show the percent compensation as a function of control bit settings. The default power-on reset (POR) value of CDRP_[2:0] is 0b000 for zero compensation.

## Table 3. Driver Cable-Droop Compensation Short-Time-Constant Control Logic

| CDRPS2 | CDRPS1 | CDRPS0 | DROOP COMPENSATION (%) |
|---|---|---|---|
| 0 | 0 | 0 | 0.0 |
| 0 | 0 | 1 | 2.1 |
| 0 | 1 | 0 | 4.3 |
| 0 | 1 | 1 | 6.4 |
| 1 | 0 | 0 | 8.6 |
| 1 | 0 | 1 | 10.7 |
| 1 | 1 | 0 | 12.9 |
| 1 | 1 | 1 | 15.0 |

## Table 4. Driver Cable-Droop Compensation Long-Time-Constant Control Logic

| CDRPL2 | CDRPL1 | CDRPL0 | DROOP COMPENSATION (%) |
|---|---|---|---|
| 0 | 0 | 0 | 0.0 |
| 0 | 0 | 1 | 2.1 |
| 0 | 1 | 0 | 4.3 |
| 0 | 1 | 1 | 6.4 |
| 1 | 0 | 0 | 8.6 |
| 1 | 0 | 1 | 10.7 |
| 1 | 1 | 0 | 12.9 |
| 1 | 1 | 1 | 15.0 |

### Adjustable Driver Output Impedance

The MAX32000 driver output impedance is adjustable to ±2.5Ω with a 360mΩ resolution. The RO_ bits in the QDRV CAL register set the impedance value. *Table 5* shows the output-resistance control logic. The output resistance is set to RO_ + 0.0Ω (0b1000) at power-up.

### VHH Function

VHH allows DUT_ to drive voltages up to +13V. The VHH DAC, which is shared among all four channels, adjusts from 0 to +13V. Although the primary VHH level is shared, there are independent offset and gain correction circuits for each channel. *Table 1* indicates the control settings required to set DUT_ to VHH. See the *Level Transfer Functions* section for the transfer function of the VHH DAC.

Set the $\overline{\text{ENVHH}}$ pin low or set the ENVHHS_ serial bit to 1 to enable VHH mode. See *Table 1*.

## Table 5. Driver Delta $R_O$ Control

| RO3 | RO2 | RO1 | RO0 | DRIVER OUTPUT RESISTANCE (Ω) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | $R_O$ - 2.88 |
| 0 | 0 | 0 | 1 | $R_O$ - 2.52 |
| 0 | 0 | 1 | 0 | $R_O$ - 2.16 |
| 0 | 0 | 1 | 1 | $R_O$ - 1.80 |
| 0 | 1 | 0 | 0 | $R_O$ - 1.44 |
| 0 | 1 | 0 | 1 | $R_O$ - 1.08 |
| 0 | 1 | 1 | 0 | $R_O$ - 0.72 |
| 0 | 1 | 1 | 1 | $R_O$ - 0.36 |
| 1 | 0 | 0 | 0 | $R_O$ + 0.0 |
| 1 | 0 | 0 | 1 | $R_O$ + 0.36 |
| 1 | 0 | 1 | 0 | $R_O$ + 0.72 |
| 1 | 0 | 1 | 1 | $R_O$ + 1.08 |
| 1 | 1 | 0 | 0 | $R_O$ + 1.44 |
| 1 | 1 | 0 | 1 | $R_O$ + 1.80 |
| 1 | 1 | 1 | 0 | $R_O$ + 2.16 |
| 1 | 1 | 1 | 1 | $R_O$ + 2.52 |

## Table 6. Calibration Comparator Control

| CMP_EN | LLEAKS3 | LLEAKS2 | LLEAKS1 | LLEAKS0 | CMUX1 | CMUX0 | DRIVER SELECTED |
|---|---|---|---|---|---|---|---|
| 1 | X | X | X | 0 | 0 | 0 | CH0 |
| 1 | X | X | 0 | X | 0 | 1 | CH1 |
| 1 | X | 0 | X | X | 1 | 0 | CH2 |
| 1 | 0 | X | X | X | 1 | 1 | CH3 |
| 1 | 1 | 1 | 1 | 1 | X | X | * |
| 0 | X | X | X | X | X | X | * |

*X = Don't care.*
**Comp output fixed. CMP = high and NCMP = low.*

### Calibration Comparator

Set serial bit CMP_EN = 1 to enable the comparator function. The drive channel selected by the CMUX_ and LLEAKS_ bits is presented to the high-speed comparator outputs as shown in *Table 6*.

### Serial Interface

An SPI-compatible serial interface controls the MAX32000. The serial interface, detailed in *Figure 2*, operates with clock speeds up to 50MHz and includes the signals $\overline{CS}$, SCLK, DIN, $\overline{RST}$, $\overline{LOAD}$, and DOUT. Serial-interface timing is shown in *Figure 3* and timing specifications are detailed in the *Electrical Characteristics* table.

### Loading Data into the MAX32000

Load data into the 24-bit shift register from DIN on the rising edge of SCLK, while $\overline{CS}$ is low (*Figure 2*). Send the address and data bits MSB first to LSB. The MAX32000 is updated when the control and level-setting data are latched into the control and level-setting registers. The control and level-setting registers are separated from the shift register by the input and channel-select registers. Two methods allow for data to transfer from the shift register to the control and level-setting registers, depending on the state of external digital input $\overline{LOAD}$.

Holding $\overline{LOAD}$ high during the rising edge of $\overline{CS}$ allows the shift register data to transfer only into the input and channel-select registers. Force $\overline{LOAD}$ low to transfer the data into the control and level-setting registers. Changes update on the falling edge of $\overline{LOAD}$, which allows preloading of data and facilitates synchronizing updates across multiple devices. See *Figure 3* and *Figure 4*.

Holding $\overline{LOAD}$ low during the rising edge of $\overline{CS}$ forces the input and channel-select registers to become transparent and all data transfers through these registers directly to the control and level-setting registers. Changes update on the rising edge of $\overline{CS}$. *Figure 4* and *Figure 5* show how $\overline{LOAD}$ and $\overline{CS}$ function, and also the data configuration of SCLK, DIN, and DOUT. The calibration registers change on the rising edge of $\overline{CS}$, regardless of the state of $\overline{LOAD}$.

### Serial-Port Timing

Timing and arrangement of the serial-port signals are shown in *Figure 3*, *Figure 4*, and *Figure 5*.

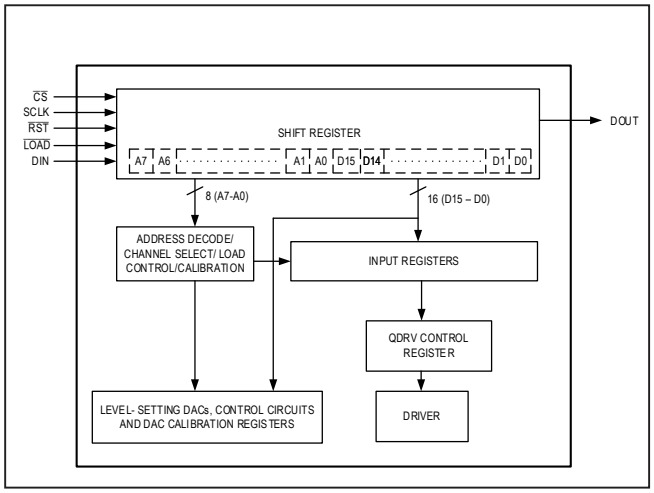



*Figure 2. Serial-Interface Block Diagram*

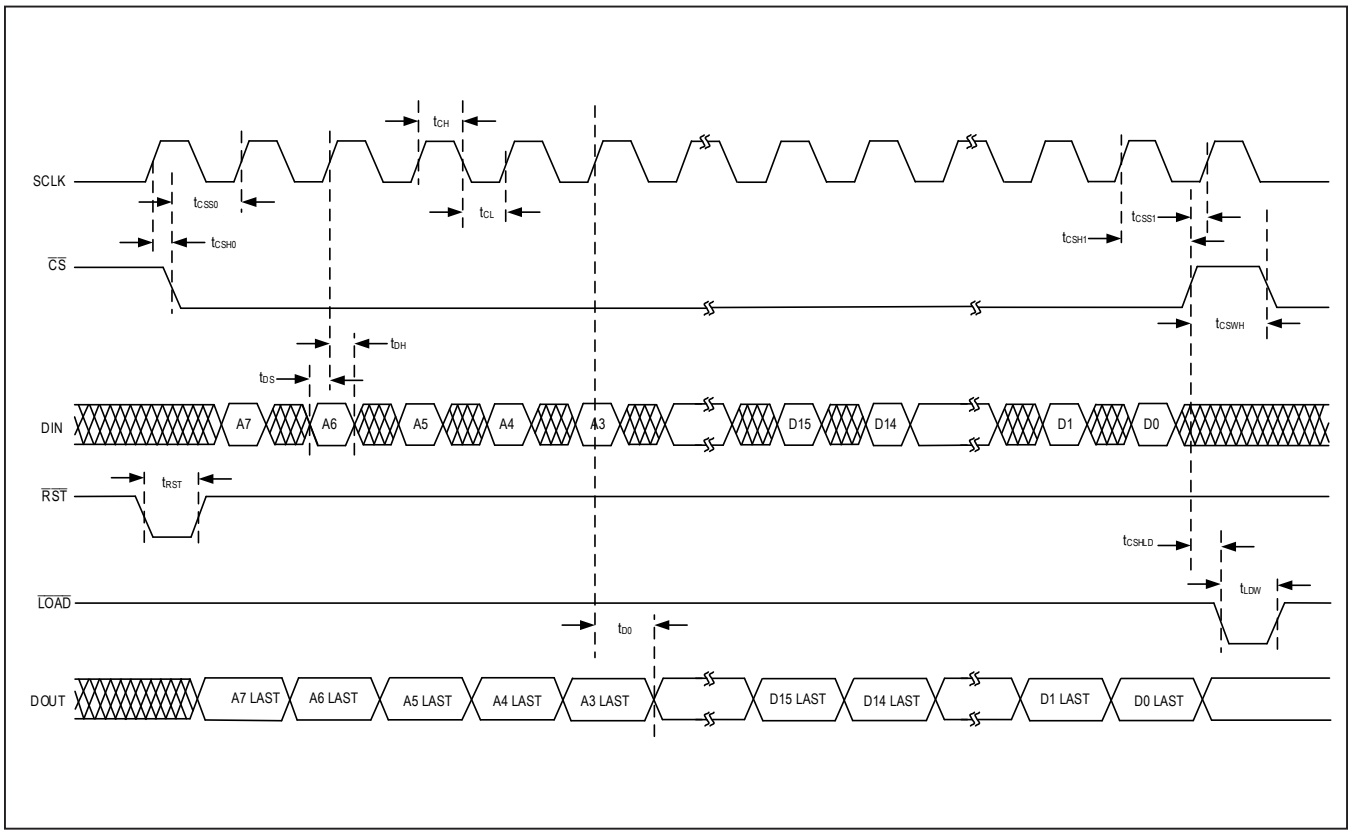



*Figure 3. Detailed Serial-Port Timing Diagram*

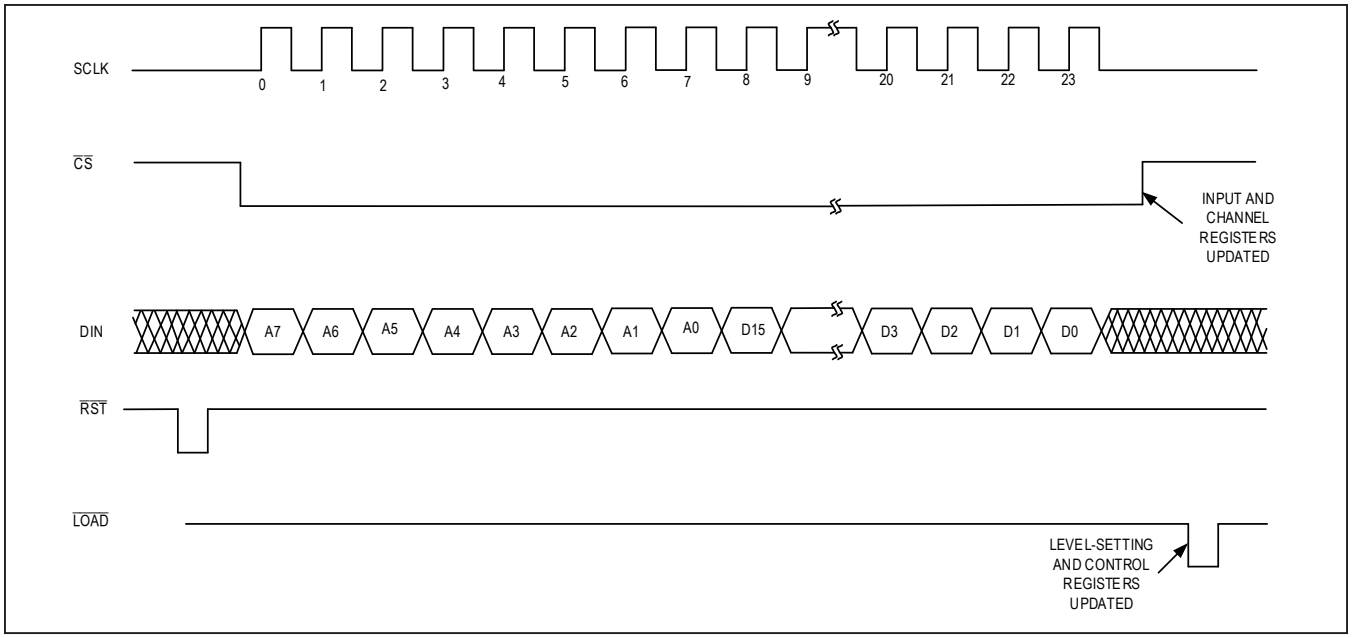



*Figure 4. Serial-Port Timing with Asynchronous Load*

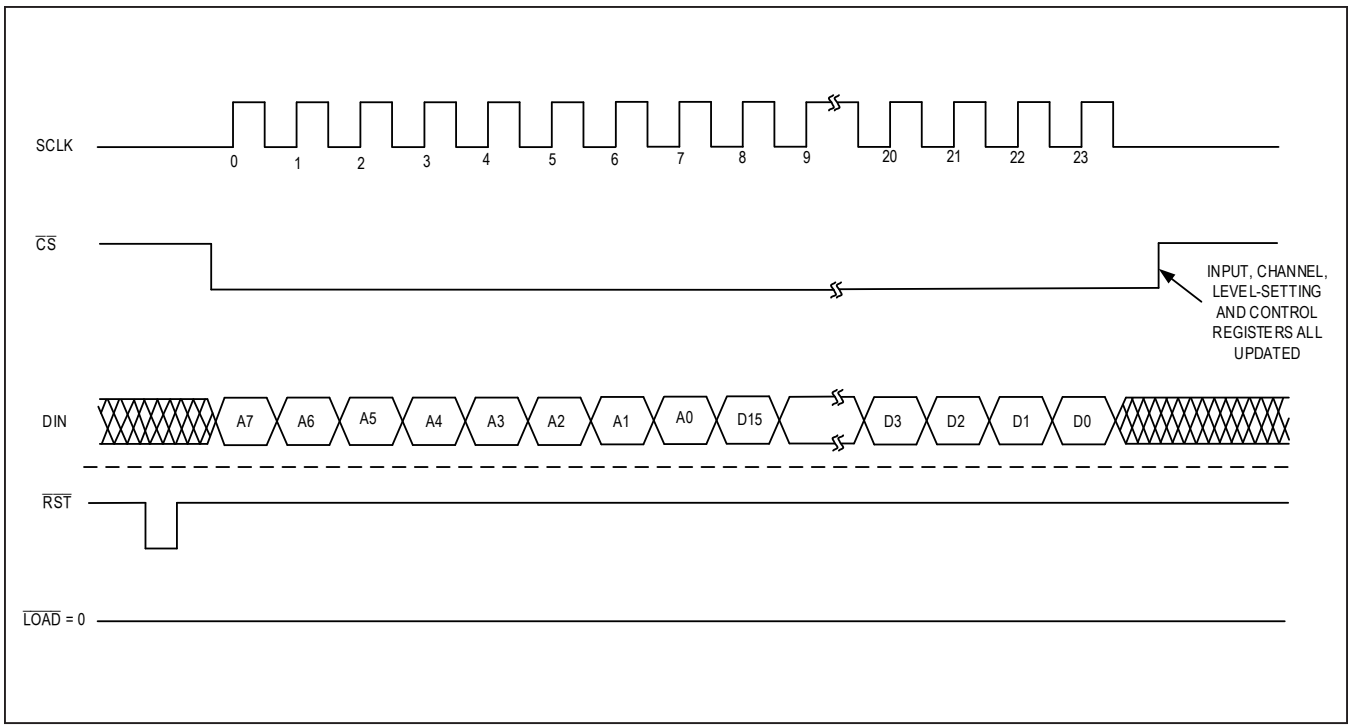



*Figure 5. Serial-Port Timing with Synchronous Load*

### Serial Interface DOUT

DOUT is a buffered version of the last bit in the serial-interface shift register. The complete contents of the shift register can be read at DOUT during the next write cycle. To shift data out without modifying any registers, perform a write with address bits A[7:0] = 0x08. Use DOUT to daisy-chain multiple devices, and/or to verify that data was properly shifted in during the previous communication. Data is shifted into the shift register on the rising edge of the SCLK, when $\overline{CS}$ is low. The shift register is 24 bits long.

### Device Control

Control and level-setting registers are selected to receive data based on the channel and mode-select bits A[7:0]. *Table 9* and *Table 10* show the control register bits and functions. Level-setting DAC data and control register data are contained in the 16 data bits D[15:0]. *Table 7*, *Table 8*, and *Table 9* detail the bit functions. Clock in bit A7 first and bit D0 last, as shown in *Figure 3*.

Bit A7 allows access to the DAC calibration registers. Use the calibration registers to adjust the gain and offset of each DAC. Set bit A7 to write to the calibration registers. See the *Level-Setter DAC and Calibration Addresses* section for more information.

## Table 7. Serial-Interface Control Bits

| DIN | FUNCTION |
|---|---|
| A7 | Calibration register write |
| A6* | Broadcast enable |
| A[5:4] | Channel address |
| A[3:0] | Register address |
| D[15:0] | Register data |

**All channels are written when the broadcast enable bit (A6) is set high and bits A[5:4] are set low.*

## Register Address Table

### Table 8. Serial-Interface Register Addresses

| ADDRESS* | | | | REGISTER | |
|---|---|---|---|---|---|
| A3 | A2 | A1 | A0 | A7 = 0, A4 AND A5 = CH | A7 = 1, A4 AND A5 = CH |
| 0 | 0 | 0 | 0 | QDRV | QDRV CAL |
| 0 | 0 | 0 | 1 | DHV_ | DHV_ CAL |
| 0 | 0 | 1 | 0 | DLV_ | DLV_ CAL |
| 0 | 0 | 1 | 1 | DTV_ | DTV_ CAL |
| 0 | 1 | 0 | 0 | TS (CH0 only) | — |
| 1 | 0 | 1 | 1 | CMPV (CH0 only) | CMPV CAL |
| 1 | 1 | 0 | 0 | VHH (CH0 only) | VHH CAL |
| 1 | 1 | 0 | 1 | OVHV | — |
| 1 | 1 | 1 | 0 | OVLV | — |
| 1 | 1 | 1 | 1 | CMP (CH0 only) | — |

**The addresses from 0b0101 to 0b1010 are not allowed.*

## Data Bit Assignments

### Table 9. Serial-Interface Data Bit Assignments

| REGISTER NAME | ADDRESS (Note 1) | | | | | DATA (Notes 1, 2) | | | | | | | | | | | | | | | | POR VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | ALL | CH3 | CH2 | CH1 | CH0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| QDRV | 0x40 | 0x30 | 0x20 | 0x10 | 0x00 | — | — | — | — | — | EN_TEMP_ALARM_ (Note 3) | EN_OV_ALARM | — | — | — | — | ENVHHS_ | TMSEL | LLEAKS_ | SC1 | SC0 | 0x004 |
| DHV_ | 0x41 | 0x31 | 0x21 | 0x11 | 0x01 | — | — | DLVL13 | DLVL12 | DLVL11 | DLVL10 | DLVL09 | DLVL08 | DLVL07 | DLVL06 | DLVL05 | DLVL04 | DLVL03 | DLVL02 | DLVL01 | DLVL00 | 0x1333 |
| DLV_ | 0x42 | 0x32 | 0x22 | 0x12 | 0x02 | — | — | DLVL13 | DLVL12 | DLVL11 | DLVL10 | DLVL09 | DLVL08 | DLVL07 | DLVL06 | DLVL05 | DLVL04 | DLVL03 | DLVL02 | DLVL01 | DLVL00 | 0x1333 |
| DTV_ | 0x43 | 0x33 | 0x23 | 0x13 | 0x03 | — | — | DLVL13 | DLVL12 | DLVL11 | DLVL10 | DLVL09 | DLVL08 | DLVL07 | DLVL06 | DLVL05 | DLVL04 | DLVL03 | DLVL02 | DLVL01 | DLVL00 | 0x1333 |
| TS | 0x44 | — | — | — | 0x04 | — | — | — | — | — | — | — | — | — | TSMUX0 | — | — | — | — | — | — | 0x0000 |

## Table 9. Serial-Interface Data Bit Assignments (continued)

| REGISTER NAME | ADDRESS (Note 1) | | | | | DATA (Notes 1, 2) | | | | | | | | | | | | | | | POR VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | ALL | CH3 | CH2 | CH1 | CH0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| CMPV | 0x4B | — | — | — | 0x0B | — | — | DLVL13 | DLVL12 | DLVL11 | DLVL10 | DLVL09 | DLVL08 | DLVL07 | DLVL06 | DLVL05 | DLVL04 | DLVL03 | DLVL02 | DLVL01 | DLVL00 | 0x1333 |
| VHH | 0x4C | — | — | — | 0x0C | — | — | DLVL13 | DLVL12 | DLVL11 | DLVL10 | DLVL09 | DLVL08 | DLVL07 | DLVL06 | DLVL05 | DLVL04 | DLVL03 | DLVL02 | DLVL01 | DLVL00 | 0x1333 |
| OVHV | 0x4D | 0x3D | 0x2D | 0x1D | 0x0D | — | — | — | — | — | — | — | — | DLVL07 | DLVL06 | DLVL05 | DLVL04 | DLVL03 | DLVL02 | DLVL01 | DLVL00 | 0x4D |
| OVLV | 0x4E | 0x3E | 0x2E | 0x1E | 0x0E | — | — | — | — | — | — | — | — | DLVL07 | DLVL06 | DLVL05 | DLVL04 | DLVL03 | DLVL02 | DLVL01 | DLVL00 | 0x4D |
| CMP | 0x4F | — | — | — | 0x0F | — | — | — | — | — | — | — | — | — | — | — | — | — | CMP_EN | CMUX1 | CMUX0 | 0x0000 |
| QDRV CAL (Note 4) | 0xC0 | 0xB0 | 0xA0 | 0x90 | 0x80 | — | — | — | — | — | — | CDRPL2 | CDRPL1 | CDRPL0 | CDRPS2 | CDRPS1 | CDRPS0 | RO3 | RO2 | RO1 | RO0 | 0x0000 |
| DHV_ CAL (Note 4) | 0xC1 | 0xB1 | 0xA1 | 0x91 | 0x81 | — | — | GCAL5 | GCAL4 | GCAL3 | GCAL2 | GCAL1 | GCAL0 | OCAL7 | OCAL6 | OCAL5 | OCAL4 | OCAL3 | OCAL2 | OCAL1 | OCAL0 | 0x2080 |
| DLV_ CAL (Note 4) | 0xC2 | 0xB2 | 0xA2 | 0x92 | 0x82 | — | — | GCAL5 | GCAL4 | GCAL3 | GCAL2 | GCAL1 | GCAL0 | OCAL7 | OCAL6 | OCAL5 | OCAL4 | OCAL3 | OCAL2 | OCAL1 | OCAL0 | 0x2080 |
| DTV_ CAL (Note 4) | 0xC3 | 0xB3 | 0xA3 | 0x93 | 0x83 | — | — | GCAL5 | GCAL4 | GCAL3 | GCAL2 | GCAL1 | GCAL0 | OCAL7 | OCAL6 | OCAL5 | OCAL4 | OCAL3 | OCAL2 | OCAL1 | OCAL0 | 0x2080 |
| CMPV CAL (Note 4) | 0xCB | 0xBB | 0xAB | 0x9B | 0x8B | — | — | GCAL5 | GCAL4 | GCAL3 | GCAL2 | GCAL1 | GCAL0 | OCAL7 | OCAL6 | OCAL5 | OCAL4 | OCAL3 | OCAL2 | OCAL1 | OCAL0 | 0x2080 |
| VHH CAL (Note 4) | 0xCC | 0xBC | 0xAC | 0x9C | 0x8C | — | — | GCAL5 | GCAL4 | GCAL3 | GCAL2 | GCAL1 | GCAL0 | OCAL7 | OCAL6 | OCAL5 | OCAL4 | OCAL3 | OCAL2 | OCAL1 | OCAL0 | 0x2080 |

**Note 1:** Em dashes (—) in the register bit table represent an unused register bit set to 0.
**Note 2:** The data bits enter the shift register in the order D[15:0].
**Note 3:** The EN_TEMP_ALARM bit is in the CH0 QDRV register only.
**Note 4:** Level-setter calibration registers and QDRV calibration registers reset only through an internally generated POR signal.

### Level-Setter DAC and Calibration Addresses

The MAX32000 contains a total of 22 DACs to generate the DC voltage levels for the various control and monitoring circuits of the 4-channel MAX32000, a total of five levels per channel, plus two shared levels. All channels share a common DAC for the CMPV and VHH; however, each channel includes independent gain and offset adjustment for CMPV and VHH. All DAC levels, with the exception of OVHV and OVLV, are set by a 14-bit code value that varies between a hex value of 0x0000 and 0x3FFF. OVHV and OVLV are set using an 8-bit code that varies between 0x00 and 0xFF.

*Table 10*, *Table 11*, and *Table 12* identify the serial-interface address of each DAC and the address of the associated calibration register. Registers can be addressed by individual channel or by utilizing a broadcast address that accesses all channels simultaneously. The level-setter output block diagram is shown in *Figure 6*.

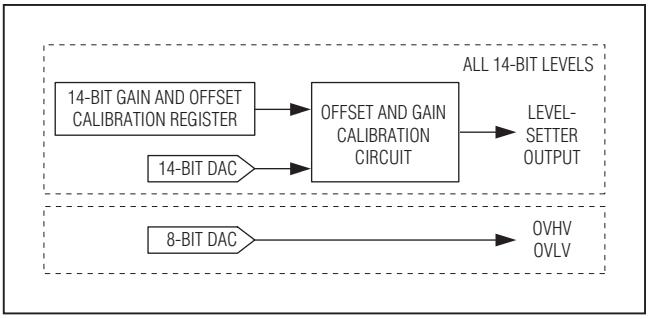



*Figure 6. Level-Setter Block Diagrams*

## Table 10. Level-Setter DAC Addressing Table

| LEVEL NAME | LEVEL DESCRIPTION | DAC REGISTER ADDRESS | | | | | RESET VALUE* |
|---|---|---|---|---|---|---|---|
| | | CH0 | CH1 | CH2 | CH3 | ALL | |
| DHV_ | Driver high | 0x01 | 0x11 | 0x21 | 0x31 | 0x41 | 0x1333 |
| DLV_ | Driver low | 0x02 | 0x12 | 0x22 | 0x32 | 0x42 | 0x1333 |
| DTV_ | Driver term | 0x03 | 0x13 | 0x23 | 0x33 | 0x43 | 0x1333 |
| CMPV** | Comparator threshold | 0x0B | — | — | — | — | 0x1333 |
| VHH** | Driver very high voltage | 0x0C | — | — | — | — | 0x1333 |
| OVHV | Overvoltage-detect high | 0x0D | 0x1D | 0x2D | 0x3D | 0x4D | 0x4D |
| OVLV | Overvoltage-detect low | 0x0E | 0x1E | 0x2E | 0x3E | 0x4E | 0x4D |

**These values are reset during a POR or with the assertion of the RST pin.*
***The VHH and CMPV levels are shared among channels 0–3. Each channel has independent calibration registers.*

## Table 11. Level-Setter DAC Calibration Address Table

| LEVEL NAME | LEVEL DESCRIPTION | CALIBRATION REGISTER ADDRESS | | | | | RESET VALUE* |
|---|---|---|---|---|---|---|---|
| | | CH0 | CH1 | CH2 | CH3 | ALL | |
| DHV_ | Driver high | 0x81 | 0x91 | 0xA1 | 0xB1 | 0xC1 | 0x2080 |
| DLV_ | Driver low | 0x82 | 0x92 | 0xA2 | 0xB2 | 0xC2 | 0x2080 |
| DTV_ | Driver term | 0x83 | 0x93 | 0xA3 | 0xB3 | 0xC3 | 0x2080 |
| CMPV** | Comparator threshold | 0x8B | 0x9B | 0xAB | 0xBB | 0xCB | 0x2080 |
| VHH** | Driver very high voltage | 0x8C | 0x9C | 0xAC | 0xBC | 0xCC | 0x2080 |

**These values are only reset during a POR. Thus, the device can be reset to a known state without requiring the reprogramming of calibration registers.*
***The VHH and CMPV levels are shared among channels 0–3. Each channel has independent calibration registers.*

## Table 12. Comparator Control Address Table

| LEVEL NAME | LEVEL DESCRIPTION | COMMON CONTROL REGISTER ADDRESS | | | | | RESET VALUE** |
|---|---|---|---|---|---|---|---|
| | | CH0 | CH1 | CH2 | CH3 | ALL | |
| CMP* | Calibration comparator mux register | 0x0F | — | — | — | — | 0x0000 |

**This register controls the common calibration multiplexer.*
***These values are reset during a POR or with the assertion of the $\overline{RST}$ pin.*

### Level-Setter Calibration Registers—Gain and Offset Codes

DAC calibration registers adjust the gain and offset of each DAC. Each DAC includes one or more calibration registers. All DAC calibration registers are programmed with a 14-bit code (*Table 9*). The codes are divided into two fields, one field each for gain (GCAL_) and offset (OCAL_). All DACs provide a 6-bit field for gain and an 8-bit field for offset.

Calibration registers are reset to default values only during a POR. Asserting the $\overline{RST}$ does not force the calibration registers to default values.

### Level Transfer Functions

Each of the MAX32000 analog DAC levels except OVHV and OVLV is set with a transfer function that includes the 14-bit DAC code setting, the gain code setting, and the offset code setting. The $V_{DAC}$ expressions below present the basic DAC transfer function. Each DAC provides a voltage output range of -3.0V to +7.0V (typ). There are five of these DACs per channel, and an additional two DACs that are shared among all channels. Each DAC is identical and generates a potential according to the equation that follows.

The transfer function for the 14-bit DACs (DHV_, DLV_, DTV_, CMPV, and VHH) is:

$$V_{DAC14} = 4 \times (DAC\_code/16{,}384) \times V_{REF} \times (1 - V_G/V_{REF}) \times (0.98 + 0.02 \times gain\ code/32) - 3V + (0.1 \times offset\_code/128 - 0.1) + V_{DGS} + 1.2 \times V_G$$

where $V_G = V_{GNDDAC\_\_} - V_{DGS}$

The transfer function for the 8-bit DACs (OVHV and OVLV) is:

$$V_{DAC8} = 4 \times (DAC\_code/256) \times V_{REF} \times (1 - V_G/V_{REF}) -3V + V_{DGS} + 1.2 \times V_G$$

where $V_G = V_{GNDDAC\_\_} - V_{DGS}$

For all DACs, the offset code is an integer value between 0 and 255, and the gain code is an integer value between 0 and 63. Offset and gain codes are based on the calibration register settings (*Table 13*).

Each channel has individual offset and gain correction for the commonly shared VHH and CMPV DACs.

## Table 13. Level-Setter Transfer Functions

| LEVEL | LEVEL TRANSFER FUNCTION |
|---|---|
| DHV_ | $V_{DAC14}$ x DHV_gain + DHV_offset |
| DLV_ | $V_{DAC14}$ x DLV_gain + DLV_offset |
| DTV_ | $V_{DAC14}$ x DTV_gain + DTV_offset |
| CMPV | $V_{DAC14}$ x CMPVgain + CMPVoffset |
| VHH | ($V_{DAC}$ - $V_{DGS}$) x 2 x VHH gain + VHH offset + $V_{DGS}$ |
| OVHV | $V_{DAC8}$ |
| OVLV | $V_{DAC8}$ |

## Applications

### Device Power-Up State

Upon power-up, the MAX32000 enters low-leak mode; the QDRV register defaults to 0x0004, the level and calibration registers default to 0x1333 and 0x2080, respectively, and OVLV and OVHV are set to 0x4D. For initial power-up values for the levels, see *Table 10*, *Table 11*, and *Table 12*. Power supplies can be powered in any sequence.

### Alarms

The MAX32000 features two fault-condition alarms. The first is a temperature sense alarm that activates when the MAX32000 internal temperature exceeds +125°C. The second fault condition activates when the voltage on DUT_ falls outside programmable voltage levels, higher than OVHV or below OVLV. The OVHV and OVLV levels are set by internal 8-bit DACs. Each channel features individual overvoltage-enable alarm bits, EN_OV_ALARM, in the QDRV register. A shared temperature-sense alarm-enable bit is in the QDRV register of channel 0 (see *Table 9* for the register map). A binary 1 must be programmed into those enable bits for the monitor circuits to assert their respective alarm outputs (TALARM, OVALARM). Alarm outputs are active low, open drain, and referenced to DGND. It is anticipated that the user implements the latch function in the ASIC/FPGA that monitors the TALARM signal. The overvoltage alarm is disabled when the driver is selected to VHH, because in most cases, VHH exceeds OVHV.

### Temperature Sensor

The MAX32000 provides a temperature sensor. The temperature-sensor function is enabled utilizing the TSMUX0 bit in the TS register. Contents of the TS register can be modified through the serial interface. *Table 14* defines the bit code necessary to enable this function. The temperature-sensor output is an analog voltage with +3.43V representing $T_J$ = +70°C and varies at ±10mV/°C.

### Power-Supply Considerations

Bypass each supply input to GND and REF to DGS with 0.1µF capacitors. Additionally, use bulk bypassing ≥ 10µF where the power-supply connections meet the circuit board.

### Exposed Pad

The exposed pad (EP) is internally connected to $V_{EE}$. Connect to $V_{EE}$ or leave unconnected. Do not use the EP as the primary connection to $V_{EE}$. Connect the EP to a large plane or heat sink to maximize thermal performance.

**Warning: Do not connect EP to ground.**

### Level-Setter Output Programming

For DHV_, DLV_, DTV_, and CMPV, the DAC output voltage is nominally:

$$(V_{REF} \times code/4096) - 3 + V_{DGS}$$

where $V_{REF}$ is nominally 2.500V.

The gain DAC pivot point is 1.0V.

For VHH, the DAC output voltage is nominally:

$$2 \times ((V_{REF} \times code/4096) - 3) + V_{DGS}$$

The gain DAC pivot point is 2.0V.

$V_{REF}$ is a precision +2.500V reference.

## Table 14. Temp Sensor Control

| TSMUX0 | TEMP PIN OUTPUT |
|---|---|
| 0 | High impedance |
| 1 | Temperature-sensor voltage |

To program a given voltage ($V_{DACx}$) for the 14-bit DAC, the voltage to code conversion is:

$$Code = 1638.4 \times (V_{DACx} + 3)$$

(for DHV_, DLV_, DTV_, and CMPV)

$$Code = 1638.4 \times ((V_{DACx}/2) + 3)$$

(for VHH)

The DAC power-up default is 0x1333 (0V nominal).

The DAC $\overline{RST}$ default is 0x1333 (0V nominal).

The DAC has 14 bits of resolution. For DAC code settings that result in $V_{DACx}$ output values that exceed the device specifications, the outputs roughly max out at the device range specification. For example, if DHV_ is programmed to code 16383 (7.5V), the driver outputs about 6.25V. More accurately, an internal diode begins to conduct, and the limiting is soft.

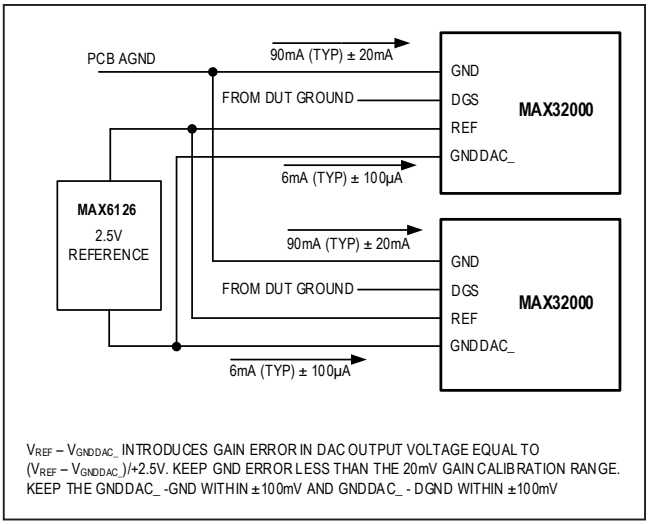



*Figure 7. Sample Connection Diagram for Two Parts per Board*

## Calibration

After mathematically determining the calibration values, shown in *Table 15* and *Table 16*, the calibrated levels need to be checked and potentially adjusted up or down because the DAC gain and offset calibration registers have a nonlinear response that could result in the gain or offset values being off by as much as Q3 LSBs, based on mathematical calculations from endpoint measurements during calibration.

### Calibration Algorithm

The user can perform a system calibration by overwriting the default values in the gain and offset registers for any DAC level. The DAC calibration points are shown in *Table 17*.

The DAC calibration algorithm is as follows:

1) Set the offset DAC to midpoint (1000 0000 = 0V nominal).
2) Set the level DAC to gain point 1 (GP1).
3) Set the gain DAC code to minimum = 00 0000.
4) Measure the output and call it $V_{GAINMINGP1}$.
5) Set the gain DAC code to maximum = 11 1111.
6) Measure the output and call it $V_{GAINMAXGP1}$.
7) Set the level DAC to gain point 2 (GP2).
8) Set the gain DAC code to minimum = 00 0000.
9) Measure the output and call it $V_{GAINMINGP2}$.
10) Set the gain DAC code to maximum = 11 1111.
11) Measure the output and call it $V_{GAINMAXGP2}$.
12) Calculate the gain code.

    The DAC is not 0V based, so there are gain differences at 0V and at 3V.

    For 63 codes, calculate the average range:

$$GAINMIN = (V_{GAINMINGP2} - V_{GAINMINGP1})/(GP2 - GP1)$$

$$GAINMAX = (V_{GAINMAXGP2} - V_{GAINMAXGP1})/(GP2 - GP1)$$

$$GAINRANGE = GAINMAX - GAINMIN$$

$$LSB = GAINRANGE/63$$

    Calculated gain code = (1 - GAINMIN)/LSB. Call it $G_{CALC}$.

13) For gain DAC codes of GCALC - 2 to GCALC + 2, measure the gain (VGP2 - VGP1)/(GP2 - GP1) at each code, where VGP_ is the output at level DAC code GP_.

## Table 15. Offset Calibration Register

| CODE | OFFSET VALUE | NOMINAL OFFSET (mV) |
|---|---|---|
| 11111111 | +FS/2 - 1 LSB | +100 |
| • • • | • • • | • • • |
| 10000001 | +1 LSB | — |
| 10000000 | 0 | 0 |
| 01111111 | -1 LSB | — |
| • • • | • • • | • • • |
| 00000000 | -FS/2 | -100 |

## Table 16. Gain Calibration Register

| CODE | OFFSET VALUE | NOMINAL GAIN (V/V) |
|---|---|---|
| 111111 | +FS/2 – 1 LSB | 1.02 |
| • • • | • • • | • • • |
| 100001 | +1 LSB | — |
| 100000 | 0 | 1 |
| 011111 | -1 LSB | — |
| • • • | • • • | • • • |
| 000000 | -FS/2 | 0.98 |

## Table 17. Calibration Points

| DAC | GAIN POINT 1 (V) (CODE) | GAIN POINT 2 (V) (CODE) | OFFSET POINT (V) (CODE) | CONDITION |
|---|---|---|---|---|
| DHV_ | 0.125 (0x1400) | 3.875 (0x2C00) | 0.125 (0x1400) | $V_{DLV\_}$ = -2V, $V_{DTV\_}$ = +1.5V |
| DLV_ | 0.125 (0x1400) | 3.875 (0x2C00) | 0.125 (0x1400) | $V_{DHV\_}$ = +6V, $V_{DTV\_}$ = +1.5V |
| DTV_ | 0.125 (0x1400) | 3.875 (0x2C00) | 0.125 (0x1400) | $V_{DLV\_}$ = -2V, $V_{DHV\_}$ = +6V |
| CMPV | 0.125 (0x1400) | 3.875 (0x2C00) | 0.125 (0x1400) | — |
| VHH | 7.75 (0x2C00) | 12.75 (0x3C00) | 7.75 (0x2C00) | — |

14) From codes GCALC - 2 to GCALC + 2, choose the code that yields a gain closest to 1.0 and program the gain DAC to that code.
15) Set the level DAC to the offset point (OP).
16) Set the offset DAC code to minimum = 0000 0000.
17) Measure the output and call it $V_{OFFSMIN}$.
18) Set the offset DAC code to maximum = 1111 1111.
19) Measure the output and call it $V_{OFFSMAX}$.
20) Calculate the offset code:

$$OFFSRANGE = V_{OFFSMAX} - V_{OFFSMIN}$$

$$LSB = OFFSRANGE/255$$

Calculated offset code = (OP - $V_{OFFSMIN}$)/LSB. Call it OCALC.

21) For offset DAC codes of OCALC - 2 to OCALC + 2, measure the offset ($V_{OP}$ - OP) at each code, where $V_{OP}$ is the output at level DAC code OP.
22) From codes OCALC - 2 to OCALC + 2, choose the code that yields an offset closest to the desired value and program the offset DAC to that code.
23) The DAC should now be calibrated.

### Calibration Example

The following is a calibration example for a DHV_ driver output high level:

1) With DHV_ = +0.125V, $V_{GAINMINGP1}$ = +0.1600V and $V_{GAINMAXGP1}$ = +0.084851V.
2) With DHV_ = +3.875V, $V_{GAINMINGP2}$ = +3.8239V and $V_{GAINMAXGP2}$ = +3.9246V.
3) GAINMIN = (3.8239V - 0.1600V)/(3.875V - 0.125V) = 0.97704.
4) GAINMAX = (3.9246V - 0.084851V)/(3.875V - 0.125V) = 1.023933.
5) GAINRANGE = 1.023933 - 0.97704 = 0.046893.
6) LSB = GAINRANGE/63 = 0.000744.
7) Gain code = (1 - 0.97704)/0.000744 = 31.
8) Remeasured +0.125V output at gain codes 29, 30, 31, 32, and 33 = +0.127601V, +0.127091V, +0.126848V, +0.126473V, and +0.126098V.
9) Remeasured +3.875V output at gain codes 29, 30, 31, 32, and 33 = +3.876120V, +3.876615V, +3.877110V, +3.877605V, and +3.878100V.
10) Gains at codes 29, 30, 31, 32, and 33 are +0.999605, +0.999837, +1.000070, +1.000302, and +1.000534.
11) Adjusted gain code = 31 (the closest to 1.0).
12) Program the gain DAC to code 31.
13) Set $V_{DHV\_}$ = +0.125V, $V_{OFFSMIN}$ = +0.0269V, and $V_{OFFSMAX}$ = +0.2180V.
14) Calculate the offset code:

$$OFFSRANGE = V_{OFFSMAX} - V_{OFFSMIN} = +0.2180V - 0.0269V = +0.1911V.$$

$$LSB = OFFSRANGE/255 = + 0.000749V.$$

Calculated offset code = (0.125V - $V_{OFFSMIN}$)/LSB = 131.

15) Offsets at codes 129, 130, 131, 132, and 133 are +0.1222V, +0.1230V, +0.1237V, +0.1245V, and +0.1252V.
16) Adjusted offset code = 133 (the closest to +0.125V).
17) Program adjusted offset code.
18) DHV_ should now be calibrated.

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 64 TQFP-EPR | C64E+9R | 21-0162 | 90-0164 |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 11/19 | Initial release | — |
| 0.1 | — | Fixed broken links in *Package Information* table | 35 |
| 0.2 | — | Fixed figure/table links | 24, 26, 28, 31 |
| 1 | 1/21 | Modified Block Diagram | 22 |

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX32000CCB+T