MAX25612/MAX25612B

Automotive Synchronous High Voltage LED Controller

General Description

The MAX25612/MAX25612B are single-channel high-brightness LED (HB LED) drivers for automotive front-light applications such as high beam, low beam, daytime running light (DRL), turn indicator, fog light and other LED lights. They can take an input voltage from 5V to 48V and can drive a string of LEDs with a maximum output voltage of 60V. The MAX25612/MAX25612B are fully synchronous and are suitable for boost, buck-boost, SEPIC, and high-side buck applications that need synchronous rectification providing efficiencies greater than 90%.

The MAX25612/MAX25612B sense output current at the high side of the LED string. High-side current sensing is required to protect against shorts from the output to the ground or battery input. It is also the most flexible scheme for driving LEDs, allowing boost, high-side buck, or buck-boost mode configurations. The PWM input provides LED dimming ratios of up to 5000:1, and the ICTRL input provides additional analog dimming capability in the MAX25612/MAX25612B. The MAX25612/MAX25612B also include a $\overline{FLT}$ flag that indicates open string, shorted string, and thermal shutdown. The MAX25612/MAX25612B have built-in spread-spectrum modulation for improved electromagnetic compatibility performance. The MAX25612/MAX25612B are available in a space-saving (4mm x 4mm), 20-pin side-wettable TQFN or a 20-pin TSSOP package and are specified to operate over the -40°C to +125°C automotive temperature range.

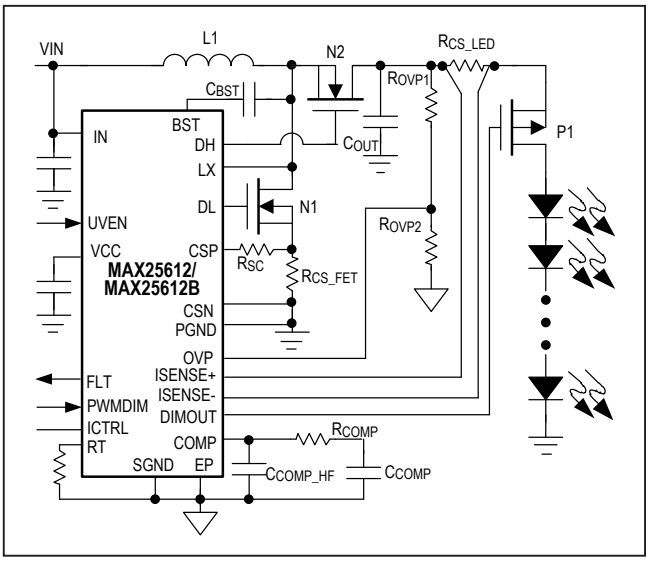
Applications

- Automotive Exterior Lighting:
  - High-Beam/Low-Beam/Signal/Position Lights
  - Daytime Running Lights (DRLs)
  - Fog Light and Adaptive Front-Light Assemblies
- Commercial, Industrial, and Architectural Lighting

Benefits and Features

- Integration Minimizes BOM and Cost
  - +5.0V to +48V Wide Input Voltage Range with a Maximum +65V Boost Output
  - Integrated pMOS Dimming FET Driver
  - ICTRL Input for Analog Dimming
  - Integrated High-Side Current-Sense Amplifier
  - 200Hz Ramp Generator Simplifies PWM Dimming
- Simple to Optimize for Efficiency, Board Space, and Input Operating Range
  - Synchronous MOSFET Driver Improves Efficiency by up to 5% for High-Current Boost, Buck-Boost, SEPIC, and High-Side Buck Applications
  - Programmable Switching Frequency (200kHz to 2.2MHz)
  - 20-Pin TSSOP Package with Exposed Pad and Thermally Enhanced 4mm x 4mm, 20-Pin Side-Wettable TQFN Packages
- Protection Features Increase System Reliability
  - Short Circuit, Overvoltage and Thermal Protection
  - Fault Diagnosis through Fault Flag
- Automotive Ready
  - -40ºC to +125ºC Operating Temperature Range
  - AEC-Q100 Qualified

Simplified Typical Operating Circuit



Ordering Information appears at end of data sheet.

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Absolute Maximum Ratings

IN, UVEN to PGND .....-0.3V to +52V
ISENSE+, ISENSE-, $\overline{DIMOUT}$ to PGND.....-0.3V to +65V
ISENSE- to ISENSE+.....-0.6V to +0.3V
BST, DH to PGND .....-0.3V to +70V
LX to PGND.....-0.3V to +65V
BST to LX .....-0.3V to +6V
DH to LX.....-0.3V to VCC+0.3V
DL to PGND .....-0.3V to VCC+0.3V
CSP, CSN to SGND .....-0.3V to VCC+0.3V
CSP-CSN .....-0.3V to +0.3V
COMP, RT to SGND.....-0.3V to Vcc+0.3V
V_{CC} to SGND.....-0.3V to +6V
SGND to PGND.....-0.3V to +0.3V
OVP, $\overline{FLT}$, ICTRL, PWMDIM to SGND.....-0.3V to +6V
Continuous Current on IN 100mA
Continuous Current on DL.....+50mA
Short Circuit Duration on V_{CC}.....Continuous
Continuous Power Dissipation (20-Pin TSSOP) (T_A = +70°C, derate 26mW/°C above +70°C.) 2122mW
Continuous Power Dissipation (20-Pin TQFN SW) (T_A = +70°C, derate 25.6mW/°C above +70°C.) 2050mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (Soldering, 10s).....+300ºC
Soldering Temperature (Reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

20-TSSOP

PACKAGE CODE	U20E+3C
Outline Number	21-100132
Land Pattern Number	90-100049
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	46ºC/W
Junction to Case (θ_{JC})	2ºC/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	37ºC/W
Junction to Case (θ_{JC})	2ºC/W

20-TQFN SW

PACKAGE CODE	T2044Y+3C
Outline Number	21-100068
Land Pattern Number	90-0037
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	59ºC/W
Junction to Case (θ_{JC})	6ºC/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	39ºC/W
Junction to Case (θ_{JC})	6ºC/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{IN} = 12V, C_{IN} = C_{VCC} = 1µF, DL = COMP = $\overline{DIMOUT}$ = PWMDIM = $\overline{FLT}$ = unconnected, V_{OVP} = V_{CS} = V_{PGND} = V_{SGND} = 0V, $V_{ISENSE+}$ = $V_{ISENSE-}$ = 45V, V_{ICTRL} = 1.40V, T_A = T_J = -40ºC to +125ºC, unless otherwise noted. Typical values are at T_A = +25ºC (Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage						
Operational Supply Voltage	V_{IN}		5		48	V
Supply Current	I_{INQ}	V_{OVP} = 1.5V, no switching		1.8	5	mA
Undervoltage Lockout						
Undervoltage Lockout Rising	V_{UVEN_THUP}	V_{UVEN} rising	1.12	1.24	1.37	V
Undervoltage Lockout Hysteresis	Hys			106		mV
V_{CC} Regulator						
Regulator Output Voltage	V_{CC}	I_{VCC} = 0.1mA to 50mA, 6V < V_{IN} < 16V	4.875	5.0	5.125	V
Undervoltage Lockout	V_{CC_UVLOR}	rising		4.0		V
Undervoltage Lockout Hysteresis				0.4		V
Oscillator (RT)						
Switching Frequency Range	f_{SW}		200		2200	kHz
Bias Voltage at RT	V_{RT}			1.25		V
Minimum OFF time		V_{COMP} = HIGH, V_{CS} = 0V		85		ns
Oscillator Frequency Accuracy		(dither disabled)	-10		+10	%
Frequency Dither	f_{DITH}	Dither enabled, f_{sw} = 200kHz to 2.2MHz		±6		%
Slope Compensation						
Slope-Compensation Current Ramp Height	I_{SLOPE}	Peak current ramp added to CS input per switching cycle	42.5	50	57.5	µA
Analog Dimming						
ICTRL Input Control Voltage Range	$ICTRL_{RNG}$		0.2		1.2	V
ICTRL Zero Current Threshold	$ICTRL_{ZC\_VTH}$	($V_{ISENSE+}$ - $V_{ISENSE-}$) < 5mV	0.16	0.18	0.2	V
ICTRL Clamp Voltage	ICTRLCLMP	ICTRL sink = 1µA	1.25	1.30	1.35	V
ICTRL Input Bias Current	$ICTRL_{IIN}$	V_{ICTRL} < = 5.5V	-500	20	500	nA
LED Current-Sense Amp						
Common-Mode Input Range			-0.2		+60	V
Differential Signal Range			0		225	mV
ISENSE+ Input Bias Current	$IB_{ISENSE+}$	($V_{ISENSE+}$ - $V_{ISENSE-}$) = 200mV, $V_{ISENSE+}$ = 60V		350	550	µA
ISENSE- Input Bias Current	$IB_{ISENSE-}$	($V_{ISENSE+}$ - $V_{ISENSE-}$) = 200mV, $V_{ISENSE-}$ = 60V		22	60	µA
Voltage Gain		($V_{ISENSE+}$ - $V_{ISENSE-}$) = 200mV, 3V < [$V_{ISENSE+}$, $V_{ISENSE-}$] < 60V	4.9	5.0	5.1	V/V

Electrical Characteristics (continued)

(V_{IN} = 12V, C_{IN} = C_{VCC} = 1µF, DL = COMP = $\overline{DIMOUT}$ = PWMDIM = $\overline{FLT}$ = unconnected, V_{OVP} = V_{CS} = V_{PGND} = V_{SGND} = 0V, $V_{ISENSE+}$ = $V_{ISENSE-}$ = 45V, V_{ICTRL} = 1.40V, T_A = T_J = -40ºC to +125ºC, unless otherwise noted. Typical values are at T_A = +25ºC (Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LED Current-Sense Regulation Voltage	V_{SENSE}	V_{ICTRL} = 1.3V, 3V < [$V_{ISENSE+}$, $V_{ISENSE-}$] < 60V	213.8	220	226.2	mV
		V_{ICTRL} = 1.2V, 3V < [$V_{ISENSE+}$, $V_{ISENSE-}$] < 60V	194	200	206	
		V_{ICTRL} = 0.4V, 3V < [$V_{ISENSE+}$, $V_{ISENSE-}$] < 60V	36	40	44	
LED Current-Sense Regulation Voltage (Low Range)	V_{SENSE}	V_{ICTRL} = 1.2V, 0V < [$V_{ISENSE+}$, $V_{ISENSE-}$] < 3V	192	200	208	mV
		V_{ICTRL} = 0.4V, 0V < [$V_{ISENSE+}$, $V_{ISENSE-}$] < 3V	35	40	45	
Common-Mode Input Range Selector	RNG_{SEL}	$V_{ISENSE+}$ rising	2.72	2.85	2.98	V
		$V_{ISENSE+}$ falling	2.48	2.6	2.72	
ERROR AMP						
Transconductance	g_M	($V_{ISENSE+}$ - $V_{ISENSE-}$) = 200mV	1170	1800	2430	µS
COMP Sink Current	$COMP_{ISINK}$	V_{COMP} = 5V		300		µA
COMP Source Current	$COMP_{ISRC}$	V_{COMP} = 0V		300		µA
PWM Comparator						
Input Offset Voltage				1		V
CS Limit Comparator						
Current-Limit Threshold	V_{CS_LIMIT}		190	210	230	mV
Gate Drivers (DH and DL)						
$R_{DS(ON)}$ Pullup pMOS				1.3		Ω
$R_{DS(ON)}$ Pulldown nMOS				0.9		Ω
PWM Dimming						
Internal Ramp Frequency	f_{RAMP}		160	200	240	Hz
External Sync Frequency Range	f_{DIM}		60		2000	Hz
External Sync Low-Level Voltage	V_{LTH}				0.4	V
External Sync High-Level Voltage	V_{HTH}		2.0			V
DIM Comparator Offset Voltage	V_{DIMOFS}		170	200	230	mV
DIM Voltage for 100% Duty Cycle			3.3			V

Electrical Characteristics (continued)

(V_{IN} = 12V, C_{IN} = C_{VCC} = 1µF, DL = COMP = $\overline{DIMOUT}$ = PWMDIM = $\overline{FLT}$ = unconnected, V_{OVP} = V_{CS} = V_{PGND} = V_{SGND} = 0V, $V_{ISENSE+}$ = $V_{ISENSE-}$ = 45V, V_{ICTRL} = 1.40V, T_A = T_J = -40ºC to +125ºC, unless otherwise noted. Typical values are at T_A = +25ºC (Note 2))

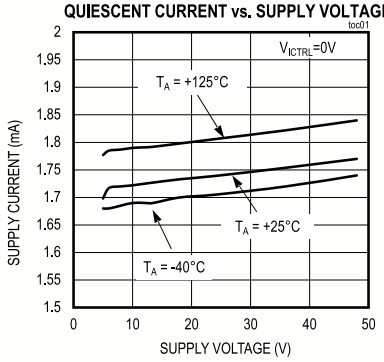
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
pMOS Gate Driver ($\overline{DIMOUT}$)						
Peak Pullup Current	$I_{DIMOUTPU}$	V_{PWMDIM} = 0V, ($V_{ISENSE+}$ - $V_{\overline{DIMOUT}}$) = 7V	40	73	120	mA
Peak Pulldown Current	$I_{DIMOUTPD}$	($V_{ISENSE+}$ - $V_{\overline{DIMOUT}}$) = 0V	15	35	65	mA
$\overline{DIMOUT}$ Low Voltage with Respect to ISENSE+			-8.4	-7.4	-6.1	V
Overvoltage Protection (OVP)						
OVP Threshold Rising	V_{OVP}	Output rising	1.17	1.23	1.29	V
Hysteresis				70		mV
Input Bias Current	I_{BOVP}	V_{OVP} = 1.235V	-500		+500	nA
Short-Circuit Hiccup Mode						
Short-Circuit Threshold	$V_{SHORT-HIC}$	($V_{ISENSE+}$ - $V_{ISENSE-}$)	369	398	427	mV
Hiccup Time	T_{HICCUP}			8192		Clock Cycles
Buck-Boost Short Detect						
Buck-Boost Short Detect Threshold (MAX25612 only)	$V_{SHORT-VOUT}$	($V_{ISENSE+}$ - V_{IN}) falling, V_{IN} = 12V	1.15	1.55	1.95	V
Open-Drain Fault ($\overline{FLT}$)						
Output Voltage Low	$V_{OL-\overline{FLT}}$	V_{IN} = 4.75V, V_{OVP} = 2V, I_{SINK} = 5mA		68.6	200	mV
Thermal Shutdown						
Thermal Shutdown Temperature	T_{SHDN}	Temperature rising		165		ºC
Thermal Shutdown Hystersis				10		ºC

Note 1: All devices are 100% tested at T_A = +25ºC. Limits over temperature are guaranteed by design

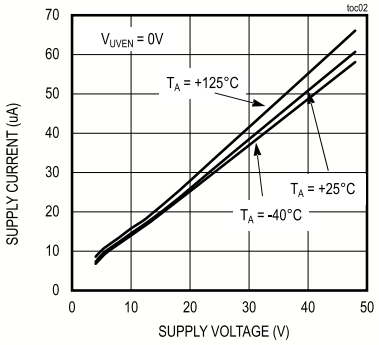
Typical Operating Characteristics

(V_{IN} = 13.5V, T_A = 25ºC unless otherwise noted.)

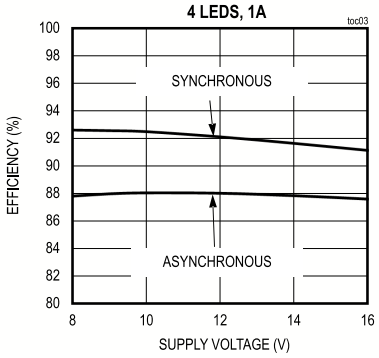
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



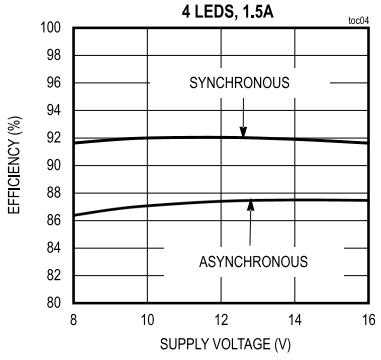
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



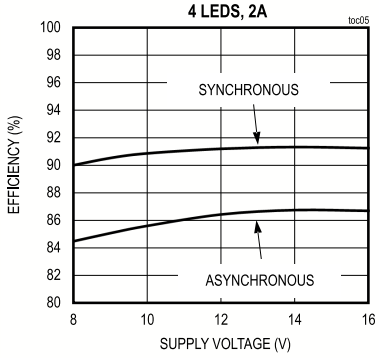
EFFICIENCY
BUCK-BOOST CONFIGURATION
4 LEDS, 1A



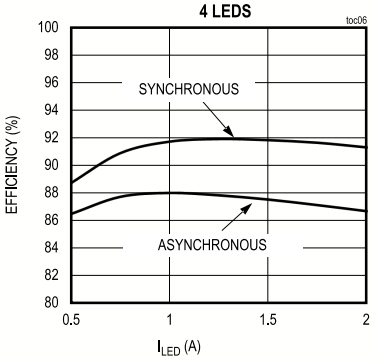
EFFICIENCY
BUCK-BOOST CONFIGURATION
4 LEDS, 1.5A



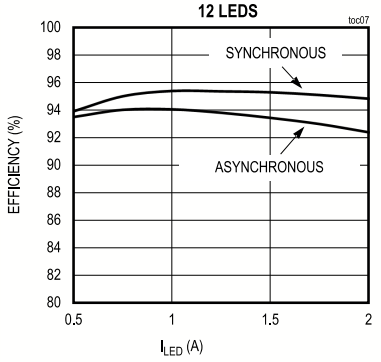
EFFICIENCY
BUCK-BOOST CONFIGURATION
4 LEDS, 2A



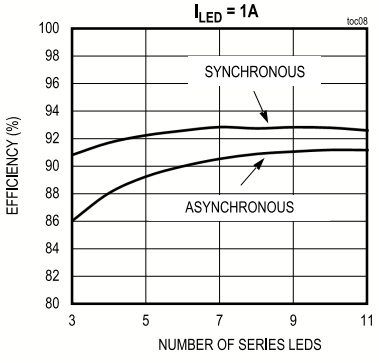
EFFICIENCY vs. LED CURRENT
BUCK-BOOST CONFIGURATION
4 LEDS



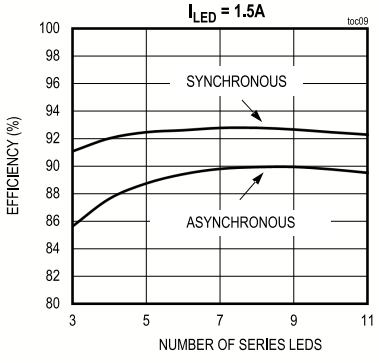
EFFICIENCY vs. LED CURRENT
BOOST CONFIGURATION
12 LEDS



EFFICIENCY vs. NUMBER OF SERIES LEDS
BUCK-BOOST CONFIGURATION
I_{LED} = 1A



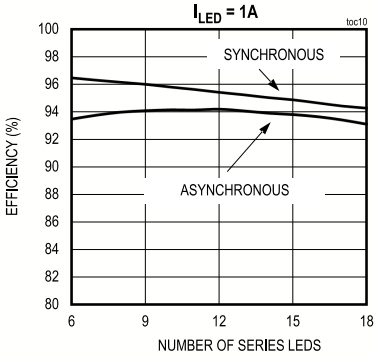
EFFICIENCY vs. NUMBER OF SERIES LEDS
BUCK-BOOST CONFIGURATION
I_{LED} = 1.5A



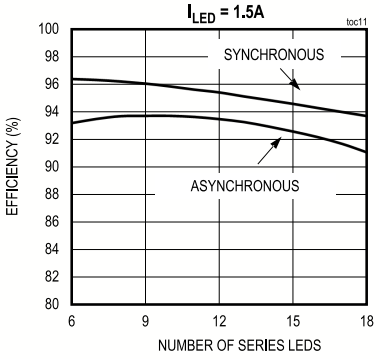
Typical Operating Characteristics (continued)

(V_{IN} = 13.5V, T_A = 25ºC unless otherwise noted.)

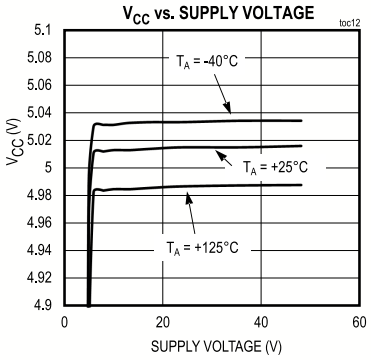
EFFICIENCY vs. NUMBER OF SERIES LEDS
BOOST CONFIGURATION
I_{LED} = 1A



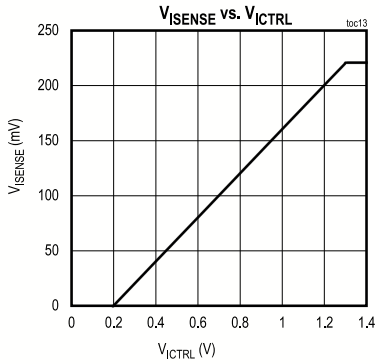
EFFICIENCY vs. NUMBER OF SERIES LEDS
BOOST CONFIGURATION
I_{LED} = 1.5A



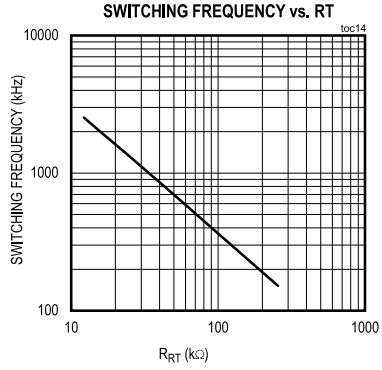
V_{CC} vs. SUPPLY VOLTAGE



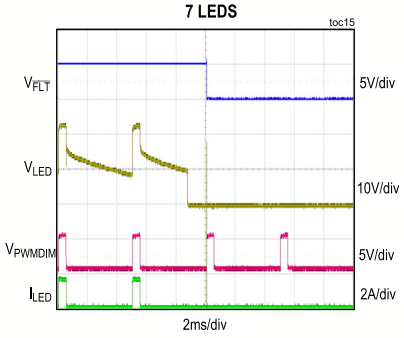
V_{ISENSE} vs. V_{ICTRL}



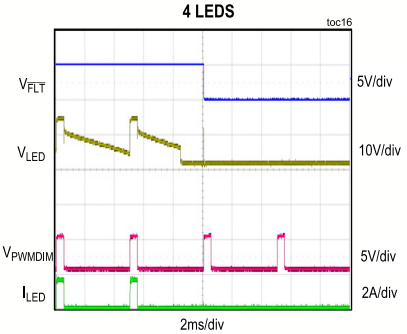
SWITCHING FREQUENCY vs. RT



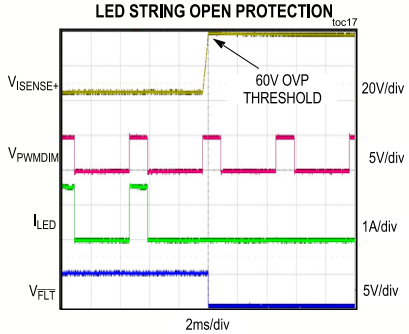
LED STRING SHORT PROTECTION
BOOST CONFIGURATION
7 LEDS



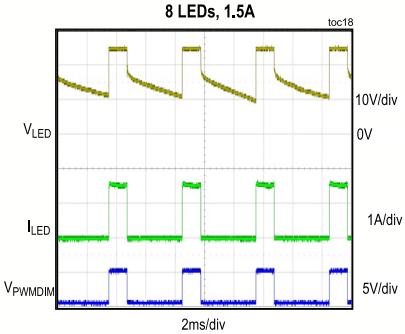
LED STRING SHORT PROTECTION
BUCK-BOOST CONFIGURATION
4 LEDS



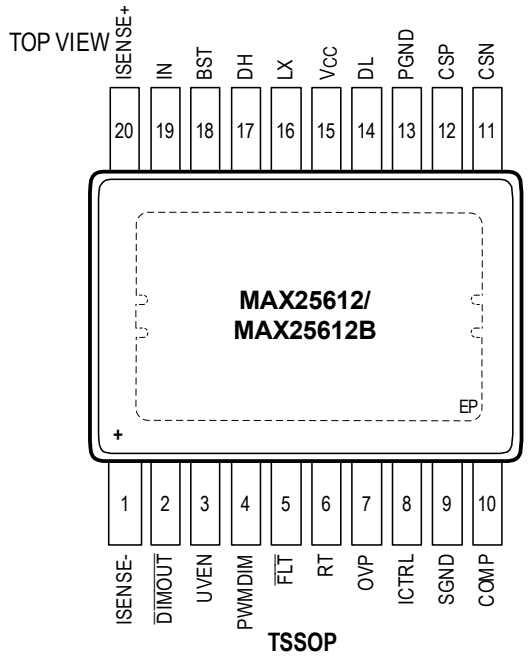
LED STRING OPEN PROTECTION



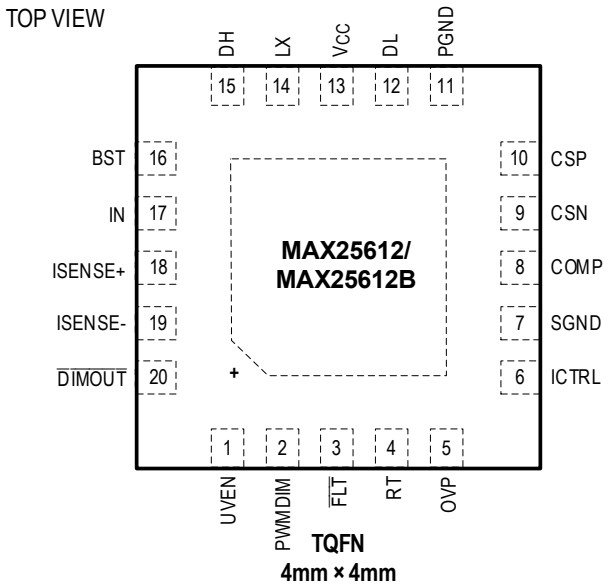
PWM DIMMING
BOOST CONFIGURATION
8 LEDs, 1.5A



Pin Configurations



TSSOP

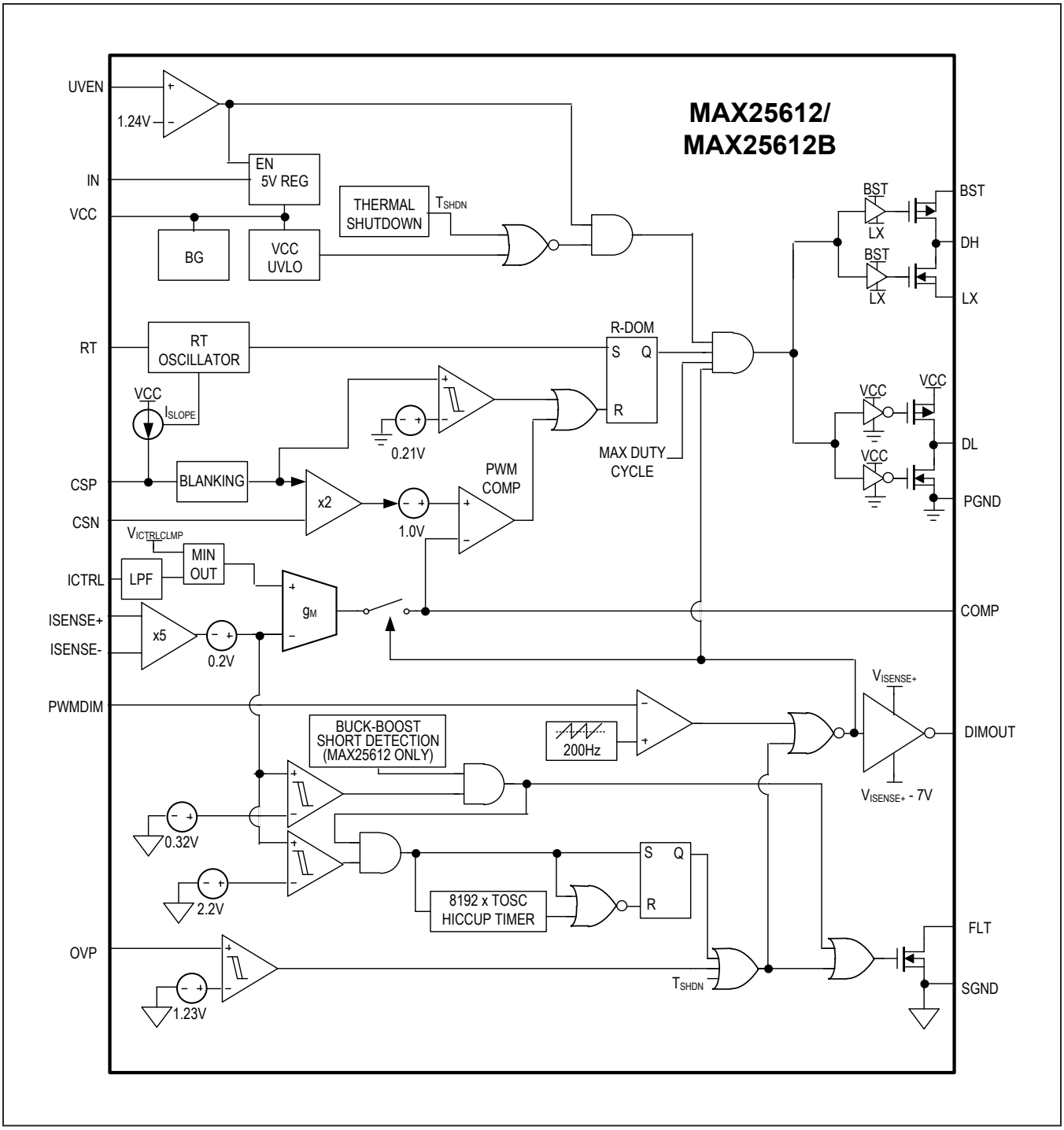


TQFN
4mm × 4mm

Pin Description

PIN		NAME	FUNCTION
TSSOP	TQFN		
1	19	ISENSE-	Negative LED Current-Sense Input. A 100Ω resistor is recommended to be placed in series with ISENSE- input and the negative terminal of the LED current-sense resistor.
2	20	$\overline{DIMOUT}$	External Dimming pMOS Gate Driver
3	1	UVEN	Undervoltage-Lockout (UVLO) Threshold/Enable Input. UVEN is a dual-function adjustable UVLO threshold input with an enable feature. Connect UVEN to V_{IN} through a resistive voltage-divider to program the UVLO threshold. Observe the absolute maximum value for this pin.
4	2	PWMDIM	Dimming Control Input. Connect PWMDIM to an external PWM signal for PWM dimming. For analog-voltage-controlled PWM dimming, connect PWMDIM to V_{CC} through a resistive voltage-divider. The dimming frequency is 200Hz under these conditions. Connect PWMDIM to SGND to turn off the LEDs.
5	3	$\overline{FLT}$	Active-Low, Open-Drain Fault Indicator Output. See the Fault Indicator ($\overline{FLT}$) section.
6	4	RT	PWM Switching Frequency Programming. Connect a resistor (R_{RT}) from RT to SGND to set the internal clock frequency.
7	5	OVP	Overvoltage Protection Input. Connect a resistive divider between the converter output, OVP, and ground. When the voltage on OVP exceeds 1.23V, a fast-acting comparator immediately stops PWM switching. This comparator has hysteresis of 70mV.
8	6	ICTRL	Analog Dimming Control Input. The voltage at ICTRL sets the LED current level when V_{ICTRL} < 1.25V. This voltage reference can be set using a resistor-divider from V_{CC} to SGND. For V_{ICTRL} > 1.25V, the internal reference sets the LED current.
9	7	SGND	Signal Ground
10	8	COMP	Compensation Network Connection. For proper compensation connect a suitable RC network from COMP to SGND.
11	9	CSN	Current-Sense Amplifier Negative Input for the Switching Regulator
12	10	CSP	Current-Sense Amplifier Positive Input for the Switching Regulator. Add a series resistor from CSP to the switching MOSFET current-sense resistor terminal for programming the slope compensation.
13	11	PGND	Power Ground
14	12	DL	Low-Side nMOS Gate Driver Output
15	13	VCC	5V Low-Dropout Voltage Regulator Output. V_{CC} supplies the bias current for the gate drive and internal control logic. Bypass V_{CC} to GND with a 4.7µF and a 0.1µF ceramic capacitor.
16	14	LX	Switch Node of the Converter
17	15	DH	High-Side nMOS Gate Driver Output
18	16	BST	Bootstrap Supply Input for the High-Side Driver
19	17	IN	Positive Power-Supply Input. Bypass with a 1µF ceramic capacitor to PGND.
20	18	ISENSE+	Positive LED Current-Sense Input. The voltage between ISENSE+ and ISENSE- is proportionally regulated to the lesser of (V_{ICTRL}, 1.23V).
-	-	EP	Exposed Pad. Connect EP to the ground plane for heatsinking. Do not use EP as the only electrical connection to ground

Functional Diagrams



Detailed Description

The MAX25612/MAX25612B are single-channel HBLED drivers for automotive front-light applications such as high beam, low beam, daytime running light (DRL), turn indicator, fog light, and other LED lights. They can take an input voltage from 5V to 48V and can drive a string of LEDs with a maximum output voltage of 60V. The MAX25612/MAX25612B feature both low- and high-side nMOS drivers for synchronous rectification. Synchronous rectification greatly improves efficiency compared to asynchronous switching converters, especially in high-current applications. Reverse recovery losses of the synchronous MOSFET will increase at higher output voltages; therefore, the efficiency benefit may be reduced when driving large numbers of LEDs. Refer to the *Typical Operating Characteristics* section for comparisons of synchronous and asynchronous switching efficiency with different currents and voltages.

The MAX25612/MAX25612B sense output current at the high side of the LED string. High-side current sensing is required to protect against shorts from the output to the ground or battery input. It is also the most flexible scheme for driving LEDs, allowing boost, high-side buck, SEPIC, or buck-boost mode configurations. The PWMDIM input provides LED dimming ratios of up to 5000:1, and the ICTRL input provides additional analog dimming capability in the MAX25612/MAX25612B. The MAX25612/MAX25612B also include a $\overline{FLT}$ flag that indicates open string, shorted string and thermal shutdown. The MAX25612/MAX25612B have built-in spread-spectrum modulation for improved electromagnetic compatibility performance.

Functional Operation

The operation of the MAX25612/MAX25612B is best understood by referring to the block diagram of the device. The devices are enabled when the UVEN pin goes above 1.24V. In addition to the UVEN input, the 5V regulator input also needs to be above its respective UVLO limit before switching on DL and DH can start. The MAX25612/MAX25612B are constant-frequency, current-mode controllers with low-side and high-side NMOS gate drivers for synchronous switching. Switching is initiated when PWM goes high. The RT oscillator can be programmed from 200kHz to 2.2MHz by the resistor between RT and SGND. Spread-spectrum dithering is added to the oscillator to alleviate EMI problems in the LED driver. The RT oscillator is synchronized to the positive edge of the PWM pulse. This means that the DL pulse goes high at the same instant as the positive pulse on PWMDIM. Synchronizing the RT oscillator to the PWMDIM pulse also guarantees that the switching frequency variation over a period of a PWMDIM pulse is the same from one PWMDIM pulse to the next. This prevents flicker during PWM dimming when spread spectrum is added to the RT oscillator.

Once PWMDIM transitions high, the external low-side switching MOSFET is turned on. A current flows through the low-side MOSFET, and this current is sensed by the voltage across the current-sense resistor from the source of the external low-side MOSFET to PGND. The MOSFET source is connected to the CSP input of the MAX25612/MAX25612B through a slope-compensation resistor (R_{SC}). See the *Typical Application Circuits* section. The ground side of the current-sense resistor is connected to the CSN input. The slope-compensation current flows out of CSP and through the R_{SC} resistor. The differential voltage across CSP and CSN is the voltage across the current-sense resistor (R_{CS_FET}) + (slope-compensation current x R_{SC}). Slope compensation prevents sub-harmonic oscillation when the duty cycle exceeds 50%. Current in the external inductor increases steadily when the external low-side MOSFET is on. The differential voltage across CSP and CSN is fed to the input of the current-limit comparator. This current-limit comparator is used to protect the external low-side switch from overcurrent and will cause switching to stop for that particular cycle if (V_{CSP} - V_{CSN}) exceeds 0.21V. The differential current-sense voltage signal is amplified by a gain factor of two. The output of the amplifier has a 1.0V offset added before being applied to the positive input of a PWM comparator. The negative input of this comparator is a control voltage from the error amplifier that regulates the LED current. When the positive input of the PWM comparator exceeds the control voltage from the error amplifier, the switching is stopped for that particular cycle and the external low-side nMOS stays off until the next switching cycle. The inductor current decays when the low-side nMOS is turned off. The inductor current starts ramping back up when the next switching cycle starts and the external low-side MOSFET turns back on. Through this repetitive action, the PWM control

algorithm establishes a switch duty cycle to regulate the current in the LED load.

When PWMDIM transitions high, the external dimming MOSFET that is driven by $\overline{DIMOUT}$ is also turned on. This external dimming MOSFET is a p-channel MOSFET and is connected on the high side of the LED load. The source of this pMOS is connected to ISENSE- and the gate is connected to $\overline{DIMOUT}$. The drain of this MOSFET is connected to the anode of the external LED string. In certain applications it is not necessary to use this dimming MOSFET, and in these cases the $\overline{DIMOUT}$ output is left open. The external pMOS is turned on when PWMDIM is high and is turned off when PWMDIM is low. During normal operation when PWMDIM is high, the voltage across the resistor from ISENSE+ to ISENSE- is regulated to a programmed voltage. This programmed voltage is 0.2 x (V_{ICTRL} - 0.2). The external pMOS switch is also used for fault protection. Once a fault condition is detected, $\overline{DIMOUT}$ is pulled high to turn off the pMOS switch. This isolates the LED string from the fault condition and prevents excessive voltage or current from damaging the LEDs.

Input Voltage (IN)

The input supply (IN) must be locally bypassed with a minimum of 1µF capacitance close to the pin. All the input current that is drawn by the MAX25612/MAX25612B goes through this input.

UVLO

The MAX25612/MAX25612B feature an adjustable UVLO using the undervoltage enable input (UVEN). Connect UVEN to IN through a resistive divider to set the UVLO threshold. The MAX25612/MAX25612B are enabled when V_{UVEN} exceeds the 1.24V (typ) threshold. UVEN also functions as an enable/disable input to the device. Drive UVEN low to disable the device. Drive UVEN high to enable the device.

V_{CC} Regulator

The V_{CC} supply is the low-voltage analog supply for the chip and derives power from the input voltage from IN to PGND. An internal power-on reset (POR) monitors the V_{CC} voltage and the IN voltage. The input voltage to the V_{CC} regulator is disconnected when the voltage at IN goes below the UVLO threshold. A POR is generated when V_{CC} goes below its UVLO threshold, causing the IC to reset. The chip will come out of reset state once the input voltage goes back up and the V_{CC} regulator output is back in regulation.

Dimming MOSFET Driver ($\overline{DIMOUT}$)

The IC requires an external p-channel MOSFET for PWM dimming. For normal operation, connect the gate of the MOSFET to the output of the dimming driver ($\overline{DIMOUT}$). The dimming driver can sink up to 35mA or source up to 73mA of peak current for fast charging and discharging of the p-MOSFET gate. When the PWMDIM signal is high, this driver pulls the p-MOSFET gate to 7V below $V_{ISENSE+}$ to completely turn on the p-channel dimming MOSFET. The $\overline{DIMOUT}$ output inverts and level-shifts the signal on PWMDIM to drive the gate of the external PMOS. In some applications, the dimming FET is not used. In this case, the $\overline{DIMOUT}$ output can be left open.

LED Current-Sense Inputs (ISENSE+/ISENSE-)

The differential voltage from ISENSE+ to ISENSE- is fed to an internal current-sense amplifier. This amplified signal is then connected to the negative input of the transconductance error amplifier. The voltage-gain factor of this amplifier is 5. The offset voltage for this amplifier is +1mV. A resistor is connected between ISENSE+ and ISENSE- to program the maximum LED current. The full-scale signal is 200mV. The ISENSE+ input should be connected to the positive terminal of the current-sense resistor and the ISENSE- input should be connected to the negative terminal of the current-sense resistor (LED string anode side).

Internal Oscillator (RT)

The internal oscillator of the MAX25612/MAX25612B are programmable from 200kHz to 2.2MHz using a single resistor at RT. Use the following formula to calculate the switching frequency:

$$f_{OSC}(kHz) = 34200/R_{RT}(k\Omega)$$

where R_{RT} is the resistor from RT to SGND. This equation is a linear approximation of the relationship between f_{OSC} and R_{RT}. See Table 1 and the *Typical Operating*

Characteristics section for more data points showing the relationship between R_{RT} and f_{OSC}. The MAX25612/MAX25612B have built-in frequency dithering of ±6% of the programmed frequency to alleviate EMI problems.

Spread Spectrum

The devices have an internal spread-spectrum option to optimize EMI performance. The switching frequency is varied ±6%, centered on the oscillator frequency (f_{OSC}). The modulation signal is a triangular wave with a period of 418 clocks. Therefore, f_{OSC} ramps down 6% and back to the set frequency in 418 clocks, and also ramps up 6% and back to the set frequency in another 418 clocks.

Synchronous MOSFET Switch Driver (DH and DL)

The IC drives an external high-side and low-side n-channel switching MOSFET. DH and DL can sink/source 2A of peak current, allowing the ICs to switch MOSFETs in high-power applications. The average current demanded from the supply to drive the external MOSFETs depends on the total gate charge (Q_G) and the operating frequency of the converter, f_{SW}. Use the following equation to calculate the driver supply current I_{DRIVER} required for the switching MOSFET:

$$I_{DRIVER} = Q_G \times f_{SW}$$

The low-side gate driver (DL) drives an external nMOS (N1) with either V_{CC} or V_{PGND} to turn the MOSFET on or off, respectively. The high-side gate driver (DH) drives an external nMOS (N2) with either V_{BST} or V_{LX} to turn the MOSFET on or off, respectively. During normal operation, DH will be driven high while the DL is driven low. Likewise, DH will be driven low while DL is driven high, thereby achieving synchronous switching. There is a small break-before-make delay between the transitions to prevent any shoot-through current that would occur as a result of both low- and high-side MOSFETs being turned on at the same time.

Boost Capacitor Node (BST)

The BST input is used to provide a drive voltage to the high-side switching MOSFET that is higher than LX. Connect a 0.1µF ceramic capacitor from BST to the LX switch node. Connect a diode from V_{CC} to BST. Place the capacitor as close as possible to BST.

Switching MOSFET Current-Sense Input (CSP and CSN)

CSP and CSN are part of the current-mode control loop. The switching control uses the voltage across CSP and CSN, set by R_{CS} and R_{SC}, to terminate the ON pulse width of the switching cycle, thus achieving peak current-mode control. Internal leading-edge blanking of 50ns is provided to prevent premature turn-off of the switching MOSFET in each switching cycle. Resistor R_{CS} is connected between the source of the n-channel switching MOSFET and PGND. During switching, a current ramp with a slope of $50\mu A x f_{SW}$ is sourced from the CSP input. This current ramp, along with resistor R_{SC}, programs the amount of slope compensation.

Overvoltage Protection Input (OVP)

OVP sets the overvoltage threshold limit across the LEDs. Use a resistive divider from ISENSE+ to OVP to SGND to set the overvoltage threshold limit. An internal overvoltage protection comparator senses the differential voltage across OVP and SGND. If the differential voltage is greater than 1.23V, DL goes low, DH and $\overline{DIMOUT}$ go high, and $\overline{FLT}$ asserts. When the differential voltage drops by 70mV, DL is enabled, $\overline{DIMOUT}$ goes low, and $\overline{FLT}$ deasserts.

Output Short-Circuit Protection

The MAX25612/MAX25612B feature output short-circuit protection. This feature is most useful where the LEDs are connected over long cables and there exists the possibility of shorts occurring when connectors are exposed.

For the MAX25612, short circuit is detected when the following two conditions are met:

- $V_{ISENSE+}$ is lower than V_{IN} by the V_{SHORT_VOUT} threshold, 1.55V (typ)
- The current-sense voltage across $V_{ISENSE+}$ - $V_{ISENSE-}$ exceeds the V_{SHORT_HIC} threshold, 398mV (typ)

The MAX25612B has disabled the V_{SHORT_VOUT} threshold flag for applications where ($V_{ISENSE+}$ - V_{IN}) is expected to be less than 1.55V (typ) during normal operation. In this case, the V_{SHORT_HIC} threshold is the only criteria for detecting a short circuit.

The MAX25612/MAX25612B respond by stopping DL and DH switching and pulling $\overline{DIMOUT}$ high to $V_{ISENSE+}$ to turn off the dimming FET, which disconnects the output capacitors from the shorted output. The device waits 8192 clock cycles before attempting to drive the LEDs again. The 8192-clock-cycle counter is only active while PWMDIM is HIGH.

Internal Transconductance Error Amplifier

The IC has a built-in transconductance amplifier that is used to amplify the error signal inside the feedback loop. When the dimming signal is low, COMP is disconnected from the output of the error amplifier and $\overline{DIMOUT}$ goes high. When the dimming signal is high, the output of the error amplifier is connected to COMP and $\overline{DIMOUT}$ goes low. This enables the compensation capacitor to hold the charge when the dimming signal has turned off the internal switching MOSFET gate drive. To maintain the charge on the compensation capacitor

C_{COMP}, the capacitor should be a low-leakage ceramic type. When the internal dimming signal is enabled, the voltage on the compensation capacitor forces the converter into steady state almost instantaneously. The transconductance of the amplifier is 1800µS.

Analog Dimming

The devices offer an analog dimming control input (ICTRL). The voltage at ICTRL sets the LED current level when V_{ICTRL} < 1.3V (typ). The LED current can be linearly adjusted from zero with the voltage on ICTRL. For V_{ICTRL} > 1.3V (typ), an internal reference sets the LED current. The LED current is guaranteed to be at zero when the ICTRL voltage is at or below $ICTRL_{ZC\_VTH(MIN)}$. The LED current can be linearly adjusted from zero to full scale for the ICTRL voltage in the range of 0.2V to 1.2V.

Pulse-Dimming Input

The PWMDIM input of the MAX25612/MAX25612B functions with either analog or PWM control signals. Once the internal pulse detector detects three successive edges of a PWM signal with a frequency between 60Hz and 2kHz, the MAX25612/MAX25612B synchronize to the external signal and pulse-width modulates the LED current at the external DIM input frequency with the same duty cycle as the DIM input. PWM dimming outside this frequency range is also possible, with the caveat that the switching clock may not be synchronized to the PWM rising edge. If an analog control signal is applied to DIM, the MAX25612/MAX25612B compare the DC input to an internally generated 200Hz ramp to pulse-width-modulate the LED current (f_{DIM} = 200Hz). The output-current duty cycle is linearly adjustable from 0% to 100% (0.2V < VDIM < 3.0V). Use the following formula to calculate the voltage, VDIM, necessary for a given output-current duty cycle D

$$V_{DIM} = (D \times 2.8) + 0.2V$$

where V_{DIM} is the voltage applied to DIM in volts.

Power Ground (PGND)

The power ground (PGND) connection acts as the ground reference for the switching power components. Connect PGND as close as possible to the negative plate of the V_{CC} decoupling capacitor.

Signal Ground (SGND)

This is the analog ground pin for all of the control circuitry of the LED driver. Connect the PGND (power ground) and the SGND together at the negative terminal of the input bypass capacitor.

Thermal Shutdown

The devices feature thermal protection. When the junction temperature exceeds +165°C, the external switching MOSFET starts operating at the minimum pulse width to reduce the power dissipation in the internal power MOSFETs. The part returns to regulation mode once the junction temperature goes below +155°C. This results in a cycled output during continuous thermal-overload conditions.

Fault Indicator ($\overline{FLT}$)

The MAX25612/MAX25612B feature an active-low, open-drain fault indicator ($\overline{FLT}$). $\overline{FLT}$ asserts when one of the following conditions occur:

1) Overvoltage across the LED string
2) Short-circuit condition across the LED string
3) Overtemperature condition

When the output voltage drops below the overvoltage set point minus the hysteresis, $\overline{FLT}$ deasserts. Similarly, during overtemperature fault, the $\overline{FLT}$ signal remains asserted until the junction temperature falls 10ºC below the thermal-shutdown threshold.

Exposed Paddle

The MAX25612/MAX25612B package features an exposed thermal pad on its underside that should be used as a heat sink. This pad lowers the package's thermal resistance by providing a direct heat-conduction path from the die to the PCB. Connect the exposed pad and GND to the system ground using a large pad or ground plane, or multiple vias to the ground plane layer.

Applications Information

V_{CC} Regulator

The internal 5V regulator is used to power the internal control circuitry inside the MAX25612/MAX25612B, as well as the low-side FET gate driver. This regulator can provide a load of 10mA to external circuitry. The 5V regulator requires an external ceramic capacitor for stable operation. A 4.7µF ceramic capacitor is adequate for most applications. Place the ceramic capacitor close to the IC to minimize trace length to the internal V_{CC} pin and also to the IC ground. Choose a 10V rated low-ESR, X7R ceramic capacitor for optimal performance.

Programming the UVLO Enable Threshold

The UVLO threshold is set by resistors R_{UVEN1} and R_{UVEN2} (see the *Typical Application Circuits* section). The MAX25612/MAX25612B turn on when the voltage across R_{UVEN2} exceeds 1.24V, the UVLO threshold. Use the following equation to set the desired UVLO enable threshold:

$$V_{UVEN} = 1.24 \times \frac{(R_{UVEN1} + R_{UVEN2})}{R_{UVEN2}}$$

where V_{UVEN} is the rising undervoltage threshold in volts. The UVEN input can also be used as a digital enable by applying an external logic signal that can turn the MAX25612/MAX25612B on and off.

Programming LED Current

Normal sensing of the LED current should be done on the high side where the LED current-sense resistor is connected to the anode of the LED string. The LED current is programmed using the resistor R_{CS_LED} (see the *Typical Application Circuits* section). When ICTRL is connected to a voltage greater than 1.3V, the internal reference regulates the voltage across R_{CS_LED} to 220mV. The current is given by:

$$I_{LED} = \frac{0.22}{R_{CS\_LED}}$$

The LED current can also be programmed by adjusting the voltage on ICTRL when $V_{ICTRL} \leq 1.2V$ (analog dimming). The current is given by:

$$I_{LED} = \frac{(V_{ICTRL} - 0.2)}{(5 \times R_{CS\_LED})}$$

Programming the Switching Frequency

The internal oscillator of the MAX25612/MAX25612B is programmable from 200kHz to 2.2MHz using a single resistor at RT. Use the following formula to calculate the value of the resistor R_{RT}:

$$R_{RT}\,(k\Omega) = \frac{34200}{f_{OSC}}$$

where f_{OSC} is the desired switching frequency in kHz. This equation is a linear approximation of the relationship between R_{RT} and f_{OSC}. See Table 1 and the *Typical Operating Characteristics* section for more data points showing the relationship between R_{RT} and f_{OSC}.

Additional ±6% spread spectrum is added internally to the oscillator to improve EMI performance.

Setting the Overvoltage Threshold

The overvoltage threshold is set by resistors R_{OVP1} and R_{OVP2} (see the *Typical Application Circuits* section). The overvoltage circuit in the MAX25612/MAX25612B is activated when the voltage on OVP with respect to GND exceeds 1.23V. Use the following equation to set the desired overvoltage threshold:

$$V_{OVP} = 1.23 \times (R_{OVP1} + R_{OVP2})/R_{OVP2}$$

Table 1. Typical R_{RT} Programming Values

R_{RT} (kΩ)	f_{OSC} (kHz)
188	200
34.2	1000
14.7	2200

Inductor Selection

Boost Configuration

In the boost converter, the average inductor current varies with the line voltage. The maximum average current occurs at the lowest line voltage. For the boost converter, the average inductor current is equal to the input current. Calculate maximum duty cycle using the equation below:

$$D_{MAX} = (V_{LED} - V_{FET2} - V_{INMIN})/(V_{LED} + V_{FET2} - V_{FET1})$$

where V_{LED} is the forward voltage of the LED string in volts, V_{INMIN} is the minimum input supply voltage in volts, and V_{FET1} and V_{FET2} are the average drain-to source voltages of the MOSFETs N1 and N2 in volts when they are on. Use an approximate value of 0.2V initially to calculate D_{MAX}. A more accurate value of the maximum duty cycle can be calculated once the power MOSFET is selected based on the maximum inductor current. Use the following equations to calculate the maximum average inductor current IL_{AVG}, peak-to-peak inductor current ripple ΔIL, and the peak inductor current IL_P in amperes:

$$IL_{AVG} = I_{LED}/(1 - D_{MAX})$$

Allowing the peak-to-peak inductor ripple to be ΔIL, the peak inductor current is given by:

$$IL_P = IL_{AVG} + 0.5 \times \Delta IL$$

The inductance value (L) of inductor L1 in Henries (H) is calculated as:

$$L = (V_{INMIN} - V_{FET1}) \times D_{MAX}/(f_{SW} \times \Delta IL)$$

where f_{SW} is the switching frequency in Hertz, V_{INMIN} and V_{FET1} are in volts, and ΔIL is in amperes. Choose an inductor that has a minimum inductance greater than the calculated value. The current rating of the inductor should be higher than IL_P at the operating temperature.

Buck-Boost Configuration

In the buck-boost LED driver, the average inductor current is equal to the input current plus the LED current. Calculate the maximum duty cycle using the following equation:

$$D_{MAX} = (V_{LED} + VFET2)/(V_{LED} + V_{FET2} + V_{INMIN} - V_{FET1})$$

where V_{LED} is the forward voltage of the LED string in volts, V_{INMIN} is the minimum input supply voltage in volts, and V_{FET1} and V_{FET2} are the average drain-to-source voltages of the MOSFETs N1 and N2 in volts when they are on. Use an approximate value of 0.2V initially to calculate D_{MAX}. A more accurate value of maximum duty cycle can be calculated once the power MOSFET is selected based on the maximum inductor current.

Use the equations below to calculate the maximum average inductor current IL_{AVG}, peak-to-peak inductor current ripple ΔIL, and the peak inductor current IL_P in amperes:

$$IL_{AVG} = I_{LED}/(1 - D_{MAX})$$

Allowing the peak-to-peak inductor ripple to be ΔIL

$$IL_P = IL_{AVG} + 0.5 \times \Delta IL$$

where IL_P is the peak inductor current.

The inductance value (L) of inductor L1 in Henries is calculated as:

$$L = (V_{INMIN} - V_{FET1}) \times D_{MAX}/(f_{SW} \times \Delta IL)$$

where f_{SW} is the switching frequency in Hertz, V_{INMIN} and V_{FET1} are in volts, and ΔIL is in amperes. Choose an inductor that has a minimum inductance greater than the calculated value.

High-Side Buck Configuration

In the high-side buck LED driver, the average inductor current is the same as the LED current. The peak inductor current occurs at the maximum input line voltage where the duty cycle is at the minimum.

$$D_{MIN} = (VLED + V_{FET2})/(V_{INMAX} - V_{FET1})$$

where V_{LED} is the forward voltage of the LED string in volts, V_{INMAX} is the maximum input supply voltage in volts, and V_{FET1} and V_{FET2} are the average drain-to-source voltages of the MOSFETs N1 and N2 in volts when they are on. Use an approximate value of 0.2V initially to calculate D_{MIN}. The maximum peak-to-peak inductor ripple ΔIL occurs at the maximum input line. The peak inductor current is given by

$$IL_P = I_{LED} + 0.5 \times \Delta IL$$

The inductance value (L) of inductor L1 in Henries is calculated as:

$$L = (V_{INMAX} - V_{FET1} - V_{LED}) \times D_{MIN}/(f_{SW} \times \Delta IL)$$

where f_{SW} is the switching frequency in Hertz, V_{INMAX} and V_{FET1} are in volts, and ΔIL is in amperes. Choose an inductor that has a minimum inductance greater than the calculated value.

SEPIC Configuration

The SEPIC converter provides the option to use either a coupled inductor or two separate inductors (see *Typical Application Circuits*). The average L1 inductor current is equal to the input current. The average L2 inductor current is equal to the LED current. Neglecting voltage drops across the FETs, the maximum duty cycle can be calculated as follows:

$$D_{MAX} = \frac{V_{LED}}{(V_{INMIN} + V_{LED})}$$

Where V_{LED} is the LED string voltage and V_{INMIN} is the minimum input voltage. The inductor value of L1 is given by:

$$L1 = \frac{V_{INMIN} \times D_{MAX}}{f_{SW} + \Delta IL_{IN}}$$

Where ΔIL_{IN} is the desired maximum input current ripple.

The L1 peak inductor current, IL_{INPK}, is given by:

$$IL_{INPK} = I_{LED} \frac{D_{MAX}}{1 - D_{MAX}} + \frac{\Delta IL_{IN}}{2}$$

The average current in inductor L2 is the same as the LED current. The desired maximum peak-to-peak output current ripple is ΔIL_{OUT}. The value of the inductor L2 is given by:

$$L2 = \frac{V_{INMIN} \times D_{MAX}}{f_{SW} \times \Delta IL_{OUT}}$$

The L2 peak inductor current, IL_{OUTPK}, is given by:

$$IL_{OUTPK} = I_{LED} + \frac{\Delta IL_{OUT}}{2}$$

To simplify further SEPIC calculations, use the following values of L and IL_{AVG}:

$$L = \frac{L1 \times L2}{L1 + L2}$$

$$IL_{AVG} = IL1_{AVG} + IL2_{AVG}$$

choose the value of C_{SEPIC} such that the peak to peak ripple on it is less than 2% of the minimum input supply voltage. This ensures that the second□order effects created by the series resonant circuit comprising L1, C_{SEPIC}, and L2 does not affect the normal operation of the converter. Use the following equation:

$$C_{SEPIC} \geq \frac{I_{LED} \times D_{MAX}}{V_{INMIN} \times 0.02 \times f_{SW}}$$

Switching MOSFET (N1) Selection

The switching MOSFET (N1) should have a voltage rating sufficient to withstand the maximum output voltage together with the voltage drop of synchronous high-side nMOS (N2), and any possible overshoot due to ringing caused by parasitic inductances and capacitances. Use a MOSFET with a drain-to-source voltage rating higher than that calculated by the following equations:

Boost configuration:

$V_{DS\_MAX} = (V_{LED} + V_{FET2} + V_{RCS\_LED} + V_{PFET}) \times 1.2$

Buck-boost configuration:

$$V_{DS\_MAX} = (V_{LED} + V_{INMAX} + V_{FET2} + V_{RCS\_LED} + V_{PFET}) \times 1.2$$

The factor 1.2 provides 20% safety margin.

A resistor is also typically added in series with the gate of the switching MOSFET (N1) to adjust the slew rate, minimize ringing on the switch node, and improve EMI performance.

Synchronous MOSFET (N2) Selection

The synchronous MOSFET (N2) should have a similar voltage rating as N1, such that it can withstand the output voltage while N1 is on and the LX node is pulled to ground, including any possible undershoot due to ringing.

Dimming MOSFET Selection

Select a dimming MOSFET (P1) with continuous current rating at the operating temperature higher than the LED current by 30%. The drain-to-source voltage rating of the dimming MOSFET must be higher than V_{LED} by 20%.

A resistor may also be added in series with the gate of the dimming MOSFET to control the slew rate and help reduce current spikes that can occur when the dimming FET turns on and connects the switching converter output capacitor to any capacitors at the LED load. A capacitor may be added across the gate and drain of the dimming FET to get better control of the RC time constant that controls the slew rate. Otherwise, the RC time constant is controlled by the parasitic capacitance of the chosen pMOS.

Slope Compensation

Slope compensation should be added to converters with peak current-mode-control operating in continuous-conduction mode with more than 50% duty cycle to avoid current-loop instability and subharmonic oscillations. The minimum amount of slope compensation required for stability is given by the following equation:

$V_{SLOPE(MIN)}$ = 0.5 x (inductor current downslope - inductor current upslope) x R_{CS_FET}

In the MAX25612/MAX25612B, the slope-compensating ramp is added to the current-sense signal before it is fed to the PWM comparator. Connect a resistor (R_{SC}) from CSP to the switch current-sense resistor terminal for programming the amount of slope compensation.

The devices generate a current ramp with a slope of 50µA/t_{OSC} for slope compensation. The current-ramp signal is forced into an external resistor (R_{SC}) connected between CSP and the source of the external MOSFET, thereby adding a programmable slope-compensating voltage (V_{SLOPE}) at the current-sense input CSP. Therefore:

$$dV_{SLOPE}/dt = (R_{SLOPE} \times 50\mu A)/t_{OSC}$$

The slope-compensation voltage that needs to be added to the current signal at minimum line voltage, with margin of 1.2x, is given by the following equation:

Boost configuration:

$$V_{SLOPE} = D_{MAX}\frac{\left(V_{LED} - 2 \times V_{INMIN}\right) \times R_{CS\_FET}}{\left(2 \times L \times f_{SW}\right)} \times 1.2$$

Buck-boost and SEPIC configuration:

$$V_{SLOPE} = D_{MAX}\frac{\left(V_{LED} - V_{INMIN}\right) \times R_{CS\_FET}}{\left(2 \times L \times f_{SW}\right)} \times 1.2$$

High-side buck configuration:

$$V_{SLOPE} = D_{MAX}\frac{\left(2 \times V_{LED} - V_{INMIN}\right) \times R_{CS\_FET}}{\left(2 \times L \times f_{SW}\right)} \times 1.2$$

MOSFET Current-Sense Resistor

The minimum value of the peak current-limit comparator is 0.19V. The current-sense resistor value is given by:

$$R_{CS\_FET} = (0.19 - D_{MAX} \times V_{SLOPE})/IL_{PK}$$

where IL_{PK} is the peak inductor current that occurs at low line in the boost and buck-boost configurations.

For boost configuration:

$$R_{CS\_FET} = \frac{0.19}{\left[IL_{PK} + 0.75D_{MAX}\frac{\left(V_{LED} - 2V_{INMIN}\right)}{L \times f_{SW}}\right]}$$

For buck-boost configuration:

$$R_{CS\_FET} = \frac{0.19}{\left[IL_{PK} + 0.75D_{MAX}\frac{\left(V_{LED} - V_{INMIN}\right)}{L \times f_{SW}}\right]}$$

For SEPIC configuration:

$$R_{CS_{FET}} = \frac{0.19}{\left[IL1_{PK} + IL2_{PK} + 0.75D_{MAX}\frac{\left(V_{LED} - V_{INMIN}\right)}{L \times f_{SW}}\right]}$$

For high-side buck configuration:

$$R_{CS_{FET}} = \frac{0.19}{\left[IL1_{PK} + 0.75D_{MAX}\frac{\left(2V_{LED} - V_{INMIN}\right)}{L \times f_{SW}}\right]}$$

Input Capacitor Selection

The input-filter capacitor bypasses the ripple current drawn by the converter and reduces the amplitude of high-frequency current conducted to the input supply.

The ESR, ESL, and bulk capacitance of the input capacitor contribute to the input ripple. Use a low-ESR input capacitor that can handle the maximum input RMS ripple current from the converter. For the boost configuration, the input current is the same as the inductor current. For buck-boost configuration, the input current is the inductor current minus the LED current. However, for both configurations, the ripple current that the input filter capacitor has to supply is the same as the inductor ripple current with the condition that the output filter capacitor should be connected to ground for buck-boost configuration. This reduces the size of the input capacitor, as the inductor current is continuous with maximum $\Delta I_L/2$. Neglecting the effect of LED current ripple, the calculation of the input capacitor for boost, as well as buck-boost configurations is the same.

Neglecting the effect of the ESL, the ESR, and the bulk capacitance at the input contributes to the input-voltage ripple. For simplicity, assume that the contribution from the ESR and the bulk capacitance is equal. This allows 50% of the ripple for the bulk capacitance. The capacitance is given by:

$$C_{IN} \geq \frac{\Delta I_L}{\left(4 \times \Delta V_{IN} \times f_{SW}\right)}$$

where ΔI_L is in amperes, C_{IN} is in Farads, f_{SW} is in Hertz, and ΔV_{IN} is in volts. The remaining 50% of allowable ripple is for the ESR of the output capacitor.

Use X7R ceramic capacitors for optimal performance. The selected capacitor should have the minimum required capacitance at the operating voltage.

In buck mode, the input capacitor has large pulsed currents due to the current flowing in the synchronous MOSFET N2 when the switching MOSFET N1 is off. It is very important to consider the ripple-current rating of the input capacitor in this application.

Output Capacitor Selection

The function of the output capacitor is to reduce the output ripple to acceptable levels. The ESR, ESL, and bulk capacitance of the output capacitor contribute to the output ripple. In most applications, the output ESR and ESL effects can be dramatically reduced by using low-ESR ceramic capacitors. To reduce the ESL and ESR effects, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance. To minimize audible noise generated by the ceramic capacitors during PWM dimming, it may be necessary to minimize the number of ceramic capacitors on the output. In these cases, an additional electrolytic or tantalum capacitor provides most of the bulk capacitance.

Boost and Buck-Boost Configurations

The calculation of the output capacitance is the same for both boost and buck-boost configurations. The output ripple is caused by the ESR and bulk capacitance of the output capacitor if the ESL effect is considered negligible. For simplicity, assume that the contributions from ESR and bulk capacitance are equal, allowing 50% of the ripple for the bulk capacitance. The capacitance is given by:

$$C_{OUT} = \frac{I_{LED} \times 2 \times D_{MAX}}{VOUT_{RIPPLE} \times f_{SW}}$$

The remaining 50% of allowable ripple is for the ESR of the output capacitor.

Based on this, the ESR of the output capacitor is given by:

$$ESR_{COUT} = \frac{VOUT_{RIPPLE}}{IL_{PK} \times 2}$$

Feedback Compensation

The LED current-control loop comprising the switching converter, LED current amplifier, and error amplifier should be compensated for stable control of the LED current. The switching converter small-signal transfer function has a right half-plane (RHP) zero for boost, SEPIC, and buck-boost configurations, as the inductor current is in continuous-conduction mode. The RHP zero adds a 20dB/decade gain together with a 90° phase lag, which is difficult to compensate. The easiest way to avoid this zero is to roll off the loop gain to 0dB at a frequency less than 1/5 of the RHP zero frequency with a -20dB/decade slope.

The worst-case RHP zero frequency (f_{ZRHP}) is calculated as follows:

Boost configuration:

$$f_{ZRHP} = \frac{V_{LED} \times \left(1 - D_{MAX}\right)^2}{2\pi \times L \times I_{LED}}$$

Buck-boost configuration:

$$f_{ZRHP} = \frac{\left(V_{LED} + V_{INMIN}\right) \times \left(1 - D_{MAX}\right)^2}{2\pi \times L \times I_{LED}}$$

SEPIC configuration:

$$f_{ZRHP} = \frac{V_{LED}\left(1 - D_{MAX}\right)^2}{2\pi \times L \times I_{LED} \times D_{MAX}}$$

The switching converter small-signal transfer function also has an output pole for both boost and buck-boost configurations. The effective output impedance that determines the output pole frequency together with the output filter capacitance is calculated as:

Boost configuration:

$$R_{OUT} = \frac{\left(R_{LED} + R_{CS\_LED}\right) \times V_{LED}}{\left(R_{LED} + R_{CS\_LED}\right) \times I_{LED} + V_{LED}}$$

Buck-boost configuration:

$$R_{OUT} = \frac{\left(R_{LED} + R_{CS\_LED}\right) \times V_{LED}}{\left(R_{LED} + R_{CS\_LED}\right) \times I_{LED} \times D_{MAX} + V_{LED}}$$

where R_{LED} is the dynamic impedance of the LED string at the operating current.

The output pole frequency for both boost and buck-boost configurations is calculated as follows:

$$f_P = \frac{1}{2\pi R_{OUT} C_{OUT}}$$

The feedback-loop compensation is done by connecting a resistor (R_{COMP}) and capacitor (C_{COMP}) in series from COMP to SGND. R_{COMP} is chosen to set the high-frequency integrator gain for fast transient response, while C_{COMP} is chosen to set the integrator zero to maintain loop stability. For optimum performance, choose the components using the following equations:

$$f_C = 0.2 \times f_{ZRHP}$$

The value of R_{COMP} and C_{COMP} can be calculated as:

$$R_{COMP} = \frac{2 \times f_{ZRHP} \times R_{CS\_FET}}{f_C \times (1 - D_{MAX}) \times R_{CS\_LED} \times 5 \times G_M}$$

$$C_{COMP} = \frac{25}{\pi \times f_{ZRHP} \times R_{COMP}}$$

the C_{COMP_HF} capacitor will add a higher frequency pole, which helps to ensure good gain margin and stability. It is typically chosen to cancel the zero from the output capacitor ESR, or such that the pole is at one half the switching frequency, whichever is lower.

$$f_{P2} = \frac{1}{2\pi R_{COMP} C_{COMP\_HF}}$$

A large resistor, such as 499kΩ or 1MΩ, should be added from COMP to SGND in applications where the ICTRL input is supplied by a programmed voltage source, which may be less than 0.2V. For applications in which the ICTRL is connected to a fixed voltage from a resistor-divider, the COMP pulldown resistor is not needed.

High-Side Buck Compensation

The high-side buck configuration does not have a right half-plane zero to avoid, so in most cases a single capacitor from COMP to GND will suffice to compensate the loop. Calculate C_{COMP} according to the following equation:

$$C_{COMP} = \frac{G_M \times A_V \times R_{CS_{LED}}}{2\pi \times f_C \times R_{CS_{FET}}}$$

Where C_{COMP} is the compensation capacitor value in nF, G_M is the G_M amplifier transconductance in µA/V, AV is the LED current-sense voltage gain, and f_C is the desired crossover frequency in kHz. Choose a crossover frequency that is lower than $f_{SW}/15$.

The output pole is set by the dynamic resistance of the LED string and the C_{OUT} capacitor

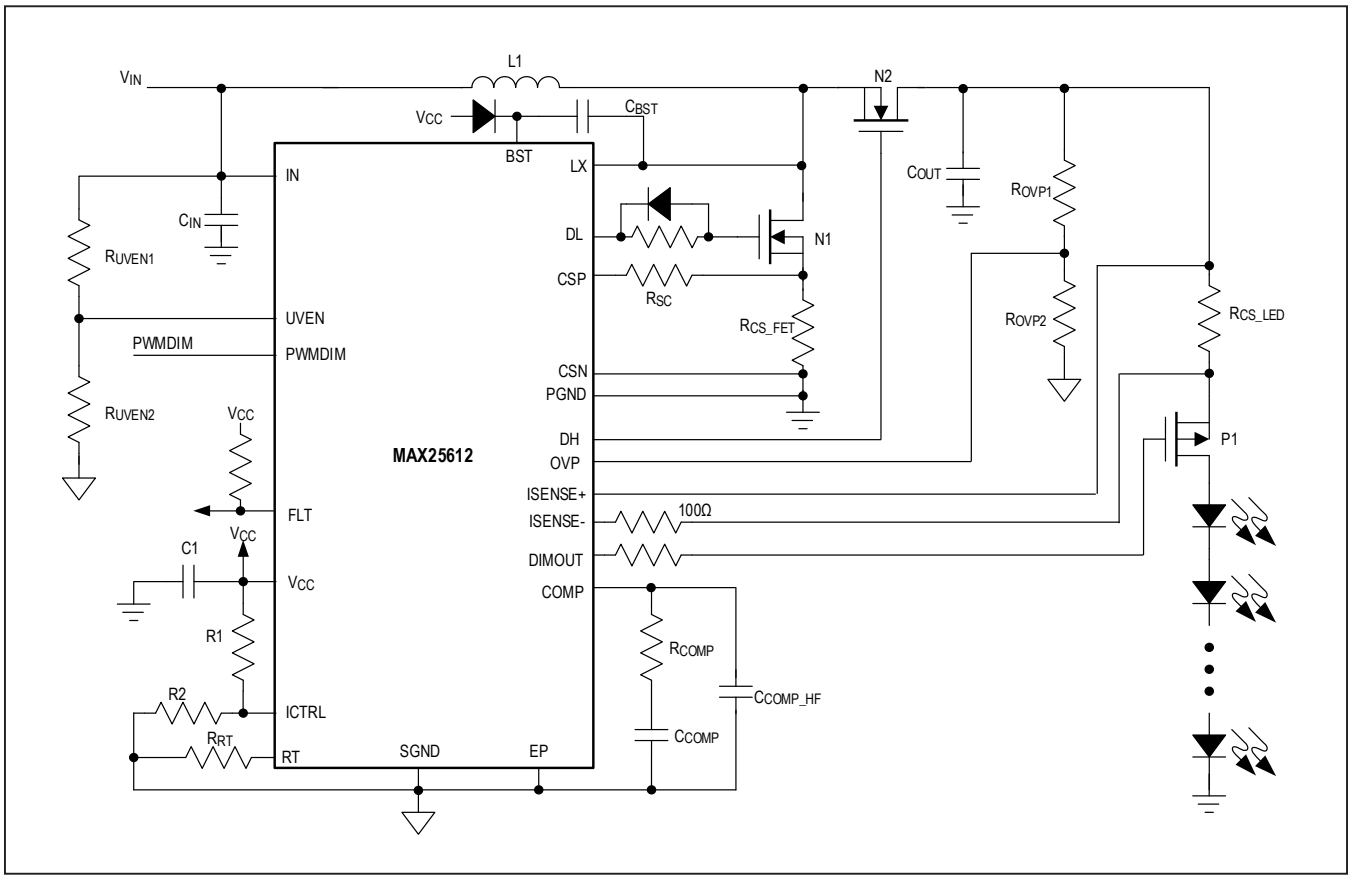
$$f_{POUT} = \frac{1}{2\pi \times R_{DYN} \times C_{OUT}}$$

If the output pole is within a decade of the crossover frequency, then it can be compensated by adding a resistor, R_{COMP}, in series with C_{COMP}.

$$R_{COMP} = \frac{C_{OUT}}{C_{COMP}} \times R_{DYN}$$

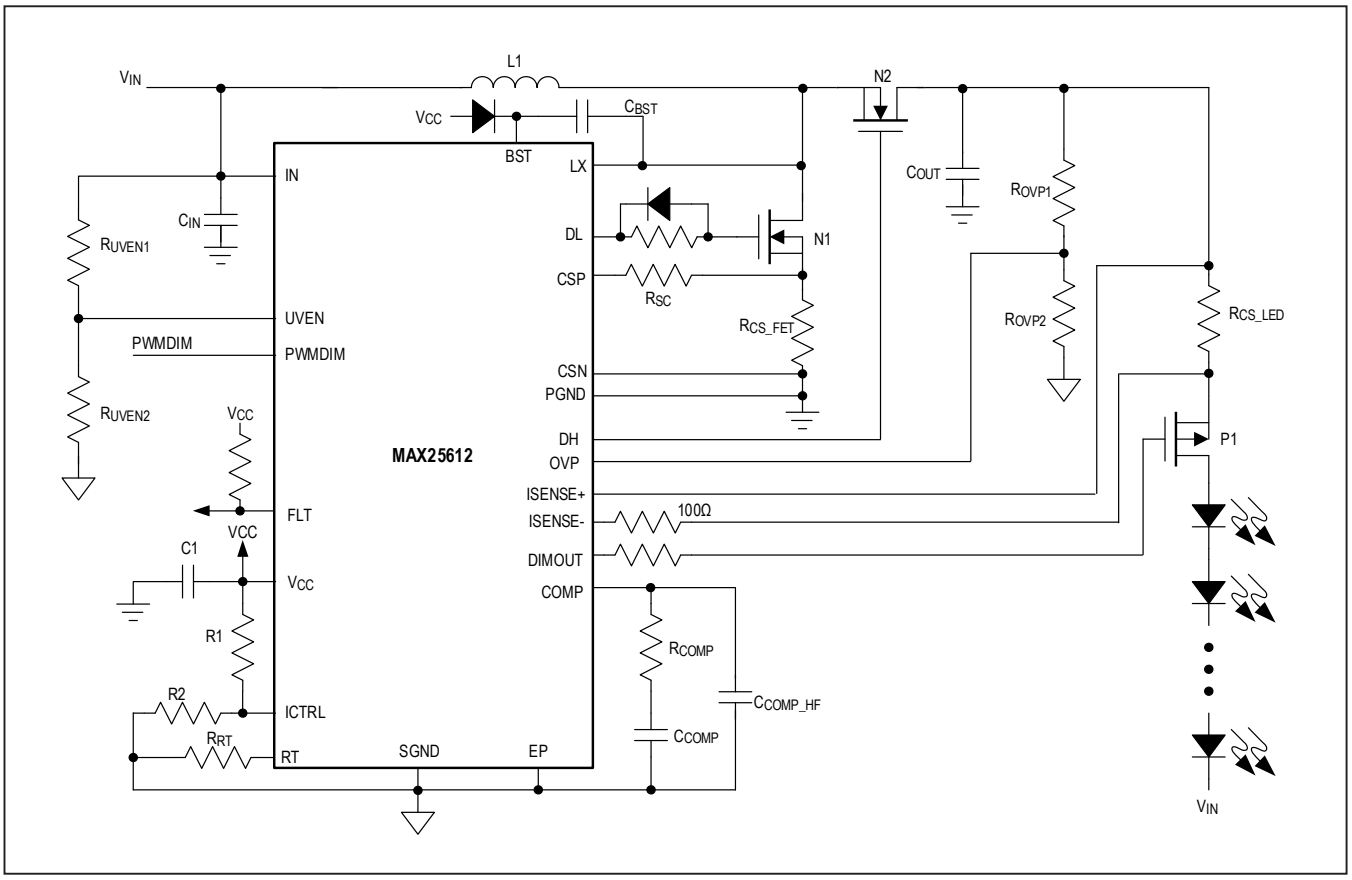
Typical Application Circuits

Boost LED Driver Using MAX25612



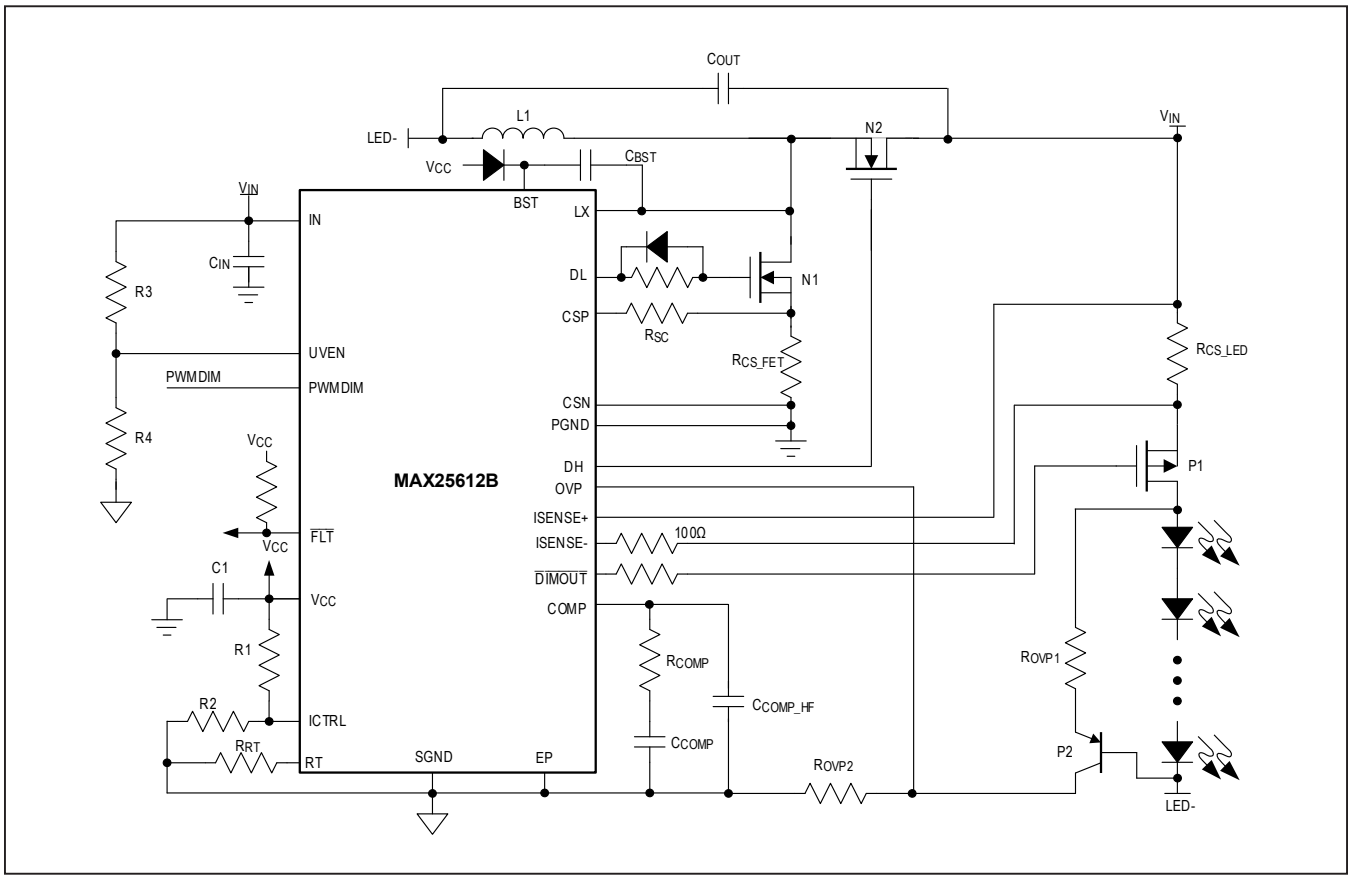
Typical Application Circuits (continued)

Buck-Boost LED Driver Using MAX25612



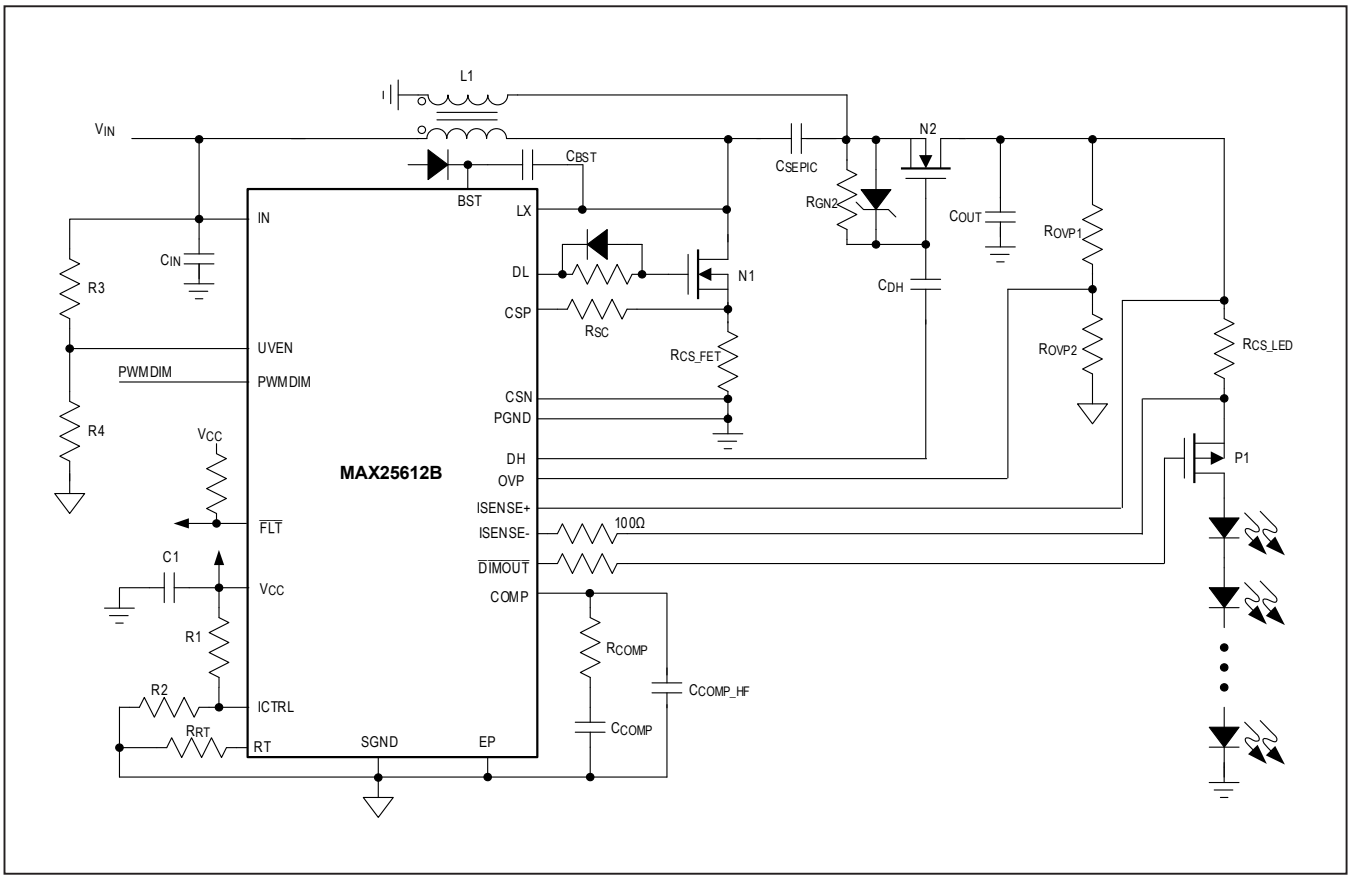
Typical Application Circuits (continued)

High-Side Buck LED Driver Using MAX25612B



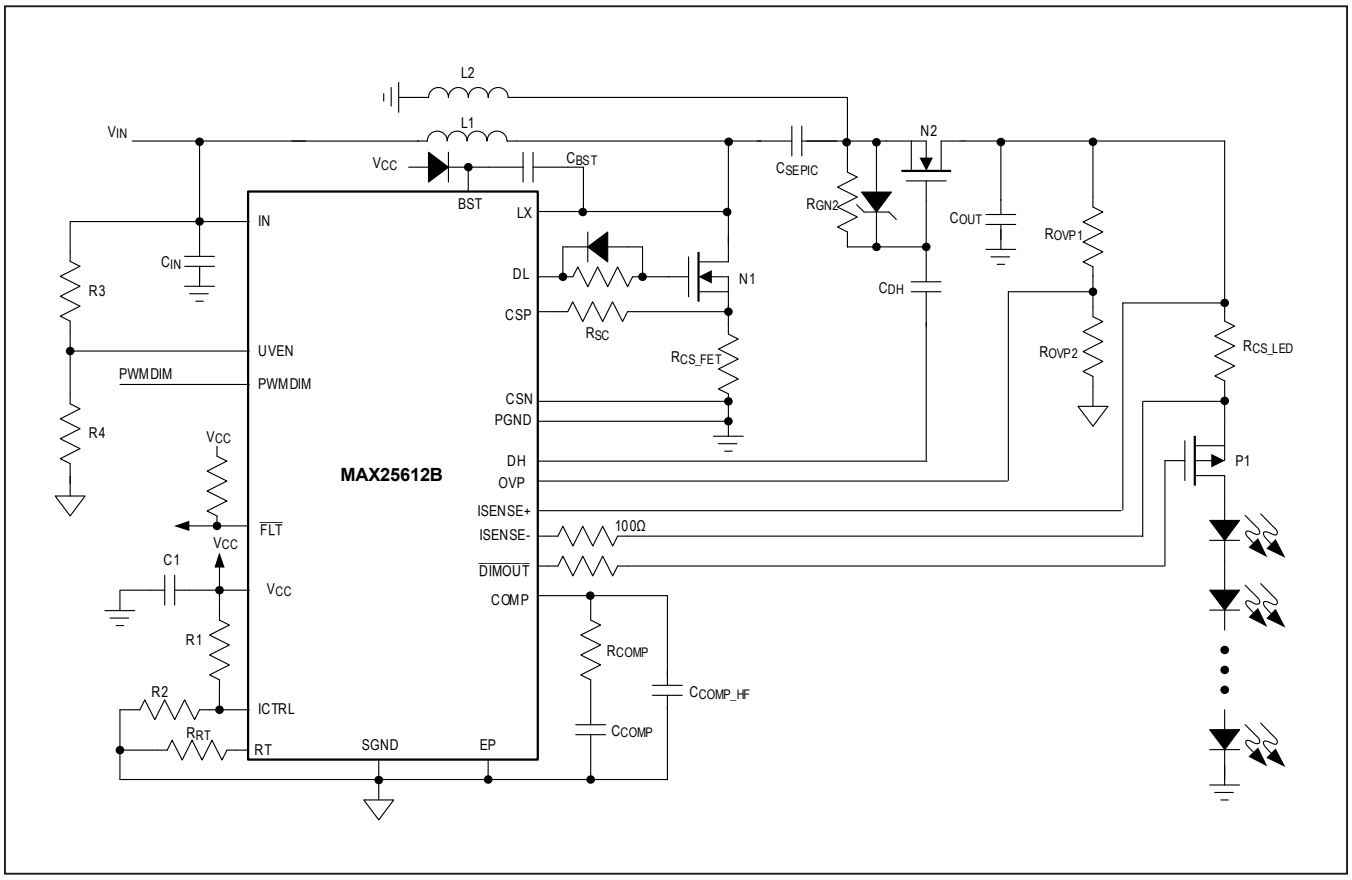
Typical Application Circuits (continued)

SEPIC01 LED Driver Using MAX25612B



Typical Application Circuits (continued)

SEPIC02 LED Driver Using MAX25612B



Ordering Information

PART	TEMPERATURE RANGE	PIN-PACKAGE
MAX25612AUP/V+	-40°C to +125°C	20-TSSOP-EP*
MAX25612ATP/VY+	-40°C to +125°C	20-TQFN-EP*
MAX25612BAUP/V+	-40°C to +125°C	20-TSSOP-EP*
MAX25612BATP/VY+	-40°C to +125°C	20-TQFN-EP*

+Denotes a lead (Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified part.
Y = Side-wettable package.
**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/19	Initial release	—
1	6/19	Added future-product notation to MAX25612ATP/VY+** in *Ordering Information*	21
2	12/19	Updated title to add MAX25612B; updated *General Description*, *Benefits and Features*, *Electrical Characteristics*, *Functional Diagrams*, *Detailed Description*, *Applications Information*, *Typical Application Circuits*, and *Ordering Information*	1–21
3	12/19	Updated *Absolute Maximum Ratings*, *Pin Configurations*, and *Applications Information*; removed future-product notation from MAX25612ATP/VY+ in *Ordering Information*	2, 8, 15, 25
4	1/20	Removed all remaining future-product notation in *Ordering Information*	25

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