*Click **here** for production status of specific part numbers.*

MAX25410 Automotive USB Power Delivery Port Protector

General Description

The MAX25410 is an automotive USB Power Delivery (USB-PD)-based Type-C protection solution for automotive radio, navigation, connectivity, and USB hub/multimedia module applications.

The device provides a one-chip automotive USB-PD protection solution for the CC1, CC2, D+, and D- signals on a USB Type-C connector. MAX25410 and MAX25410A also provide a V_{CONN} switch with advanced fault management that does not require a dedicated supply.

For ports that do not require V_{CONN} (i.e. do not support USB 3.0 or are rated at 3A or less), MAX25410B offers the designer a reduced-cost solution with the same protection level as MAX25410.

The device protection features include ±15kV IEC 61000-4-2, ISO 10605 ESD, and short-to-V_{BUS} (24V) on the protected HVCC1, HVCC2, HVD+, and HVD- pins. The device also features integrated BC1.2 charge-detection CDP, DCP, or pass-through (SDP) modes, Apple® 2.4A, Samsung® 2A, and China YD/T 1591-2009 charge-emulation support.

The MAX25410 is available in a small 4mm x 4mm 16-pin TQFN package and requires very few external components.

Applications

- Automotive Radio and Navigation
- Automotive USB Hubs
- Automotive Multimedia Box Applications

Benefits and Features

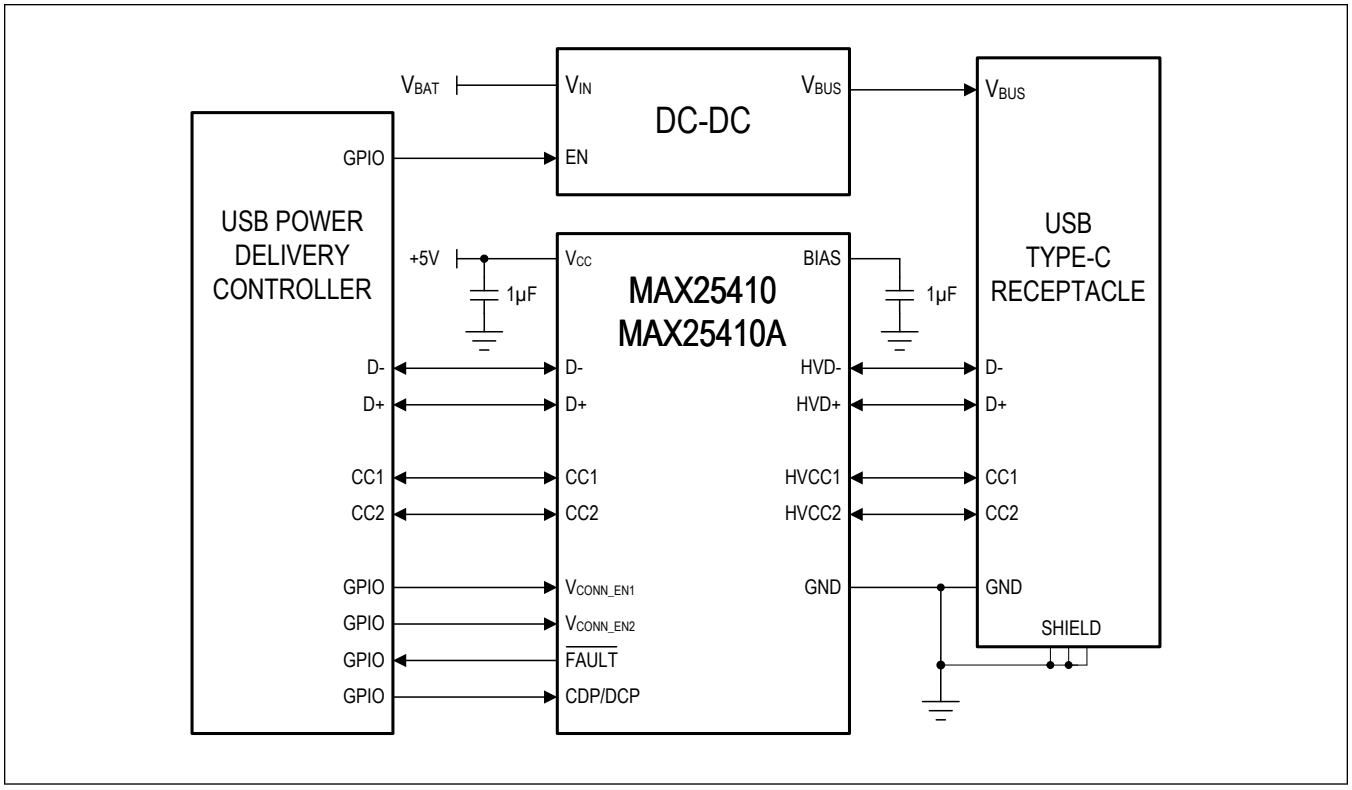
- USB Type-C CC1/CC2 Protection Switches
- Integrated 550mΩ V_{CONN} FETs with 250mA Overcurrent Protection
- USB 2.0 D+/D- Protection Switches with 1GHz Bandwidth
- 24V CC and USB 2.0 Protection against Short-to-V_{BUS}
- Automatic Fault Detection and Recovery with Industry-Compliant Reset Timings
- Integrated Apple and Samsung Dedicated Charge-Termination Resistors
  - Supports USB BC1.2 CDP and DCP Modes
  - Supports China YD/T 1591-2009
  - Compatible with USB On-the-Go Specification and Apple CarPlay
- High ESD Protection (HVD+/HVD-, HVCC1/HVCC2)
  - ±2kV Human Body Model
  - ±15kV ISO 10605 Air Gap
  - ±8kV ISO 10605 Contact
  - ±15kV IEC 61000-4-2 Air Gap
  - ±8kV IEC 61000-4-2 Contact
- 4mm x 4mm 16-Pin TQFN-EP Package
- -40°C to +105°C Operating Temperature Range
- AEC-Q100 and AEC-Q006 Qualified

Ordering Information appears at end of data sheet.

19-100679; Rev 2; 4/20

maxim integrated™

Simplified Block Diagram



Absolute Maximum Ratings

HVCC1, HVCC2 to GND (Note 1) ..... -0.3V to +24V
HVD+, HVD- to GND (Note 1) ..... -0.3V to +24V
V_{CC} to GND (Note 1) ..... -0.3V to +6.0V
CC1, CC2 to GND (Note 1) ..... -0.3V to +6.0V
D+, D- to GND (Note 1) ..... -0.3V to V_{BIAS} + 0.3V
BIAS to GND (Note 1) ..... -0.3V to +6.0V
V_{CONN_EN1}, V_{CONN_EN2} to GND ..... -0.3V to +6.0V
CDP/DCP, FAULT to GND ..... -0.3V to +6.0V

Continuous Power Dissipation (Single Layer Board) (T_A = +70°C, derate 16.9mW/°C above +70°C.) 1349.10mW
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 25mW/°C above +70°C. (Note 2)) 2000mW
Operating Temperature Range ..... -40°C to 105°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note 1: Self-protected from transient voltages exceeding these limits in circuit under normal operation.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations see http://www.maxim-ic.com/thermal-tutorial

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TQFN

Package Code	T1644+4C
Outline Number	21-0139
Land Pattern Number	90-0070
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	59.3 °C/W
Junction to Case (θ_{JC})	6°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	40°C/W
Junction to Case (θ_{JC})	6°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(T_A = -40 °C to +105 °C. Typical values are at V_{CC} = 5.0V, T_A = +25 °C, unless otherwise noted (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Supply Voltage Range	V_{CC}		4.7	5.0	5.5	V
V_{CC} Operating Current	I_{VCC}	V_{CC} = 5.0V; V_{CONN} disabled			1.5	mA
V_{CC} Undervoltage Lockout Rising	V_{CC_UVLO}	V_{CC} Rising, chip enabled	4.0	4.3	4.5	V
V_{CC} Undervoltage Lockout Hysteresis	$V_{CC\_UVLO\_HYS}$			0.1		V
BIAS Regulator						
Bias Regulator Voltage	V_{BIAS}	V_{CC} = 4.7V to 5.5V		3.15		V
BIAS Undervoltage	$V_{UV\_BIAS\_F}$	V_{BIAS} undervoltage falling threshold		2.70		V
BIAS Overvoltage	V_{OV_BIAS}	V_{BIAS} overvoltage rising threshold	3.85	4.0	4.25	V

Electrical Characteristics (continued)

(T_A = -40 °C to +105 °C. Typical values are at V_{CC} = 5.0V, T_A = +25 °C, unless otherwise noted (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIAS Undervoltage Blanking Time	$t_{BLANK\_BIAS\_UV}$	From V_{BIAS} below UV to $\overline{FAULT}$ asserted		1.8		ms
HVD+/HVD- Analog Switches						
Analog Signal Range			0		3.6	V
Data Switch ON Resistance	R_{ON_D}	V_{D+}/V_{D-} = 0V to 3.6V, I_L = 10mA		4		Ω
Data Protection Trip Threshold	V_{OV_D}	V_{HVD+}/V_{HVD-} rising	4.05	4.20	4.30	V
Data Protection OV Threshold Hysteresis	$V_{OV\_D\_HYST}$			15		mV
Data Protection Response Time	t_{FP_D}	From OV condition to switch opened		2		µs
Data Overvoltage Blanking Timeout Period	$t_{B\_OV\_D}$	From switch opened for OV to $\overline{FAULT}$ asserted		1		µs
Data Switch Differential Bandwidth	BW_{D_DIFF}	USB TEST_PACKET @ 240MHz fundamental; -3dB BW		1		GHz
ON-Resistance Match Between Channels	ΔR_{ON_SA}	I_L = 10mA, V_{D+}/V_{D-} = 1.5V to 3.0V			0.2	Ω
ON-Resistance Flatness	R_{FLATON_A}	I_L = 10mA, V_{D+}/V_{D-} = 0.0V and 0.4V			0.2	Ω
D+/D- OFF Leakage	I_{D_OFF}	V_{HVD+}/V_{HVD-} = 18V; V_{D+}/V_{D-} = 0V; D+/D- leakage to GND			1	µA
Data Switch ON Leakage	I_{D_ON}	V_{D+}/V_{D-} = 3.6V; leakage to GND			7	µA
HVD+/HVD- OFF Leakage	I_{HVD_OFF}	V_{HVD+}/V_{HVD-} = 18V; HVD+/HVD- leakage to GND		60		µA
USB2.0 Host Charge Detection						
Input Logic High	V_{IH}		2.0			V
Input Logic Low	V_{IL}				0.8	V
Data Sink Current	I_{DAT_SINK}	V_{DAT_SINK} = 0.25V to 0.4V	50	100	150	µA
Data Detection Voltage High	V_{DAT_REFH}		0.40			V
Data Detection Logic Low	V_{DAT_REFL}				0.25	V
Data Source Voltage	V_{DAT_SRC}	I_{SRC} = 200µA	0.5		0.7	V
V_{CONN} Analog Switch (MAX25410, MAX25410A)						
V_{CONN} Switch ON Resistance	R_{ON_VCONN}	100mA/200mA Load Current, V_{CC} = 5.0V		550	1150	mΩ
V_{CONN} Overcurrent Threshold (Low)	$V_{CONN\_OCP\_LOW}$	Measured on HVCC1 and HVCC2, V_{CC} from 4.7V to 5.5V	200	250	300	mA
V_{CONN} Overcurrent Threshold (High)	$V_{CONN\_OCP\_HIGH}$	Measured on HVCC1 and HVCC2, V_{CC} = 5.0V	480	600	710	mA

Electrical Characteristics (continued)

(T_A = -40 °C to +105 °C. Typical values are at V_{CC} = 5.0V, T_A = +25 °C, unless otherwise noted (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CONN} Overcurrent Protection Response Time (Low)	$t_{VCONN\_OCP\_LOW}$	Time from OC condition to V_{CONN} FET open		0.4		ms
V_{CONN} Overcurrent Protection Response Time (High)	$t_{VCONN\_OCP\_HIGH}$	Time from OC condition to V_{CONN} FET open		5		µs
V_{CONN} ON Time	t_{VCONN_ON}	Enable V_{CONN} to HVCC at 95% of V_{CC} with 25Ω//10µF load		700		µs
V_{CONN} Discharge Resistance	R_{VCONN_DIS}			3		kΩ
V_{CONN} Discharge Time	t_{VCONN_DIS}	During power-up and certain faults. See Table 1.		30		ms
V_{CONN} Diagnostic Current	I_{DIAG}	V_{CONN} enabled and before V_{CONN} main FET soft-start		60		mA
V_{CONN} Short-to-GND Comparator Rising Threshold	V_{STG_R}	Active during V_{CONN} startup only. Measured at HVCC pin		0.35		V
V_{CC} Fast UV Threshold	$V_{CC\_FAST\_UV}$	V_{CONN} enabled, measured at V_{CC}, V_{CC} falling		4.65		V
V_{CC} Fast UV Hysteresis	$V_{CC\_FAST\_UV\_HYST}$	V_{CONN} enabled		60		mV
CC Pass-Through Analog Switches						
Analog Signal Range			0		5.5	V
CC Switch ON Resistance	R_{CC_ON}	Resistance from CC1 to HVCC1 or CC2 to HVCC2, V_{CC1}/V_{CC2} = 0V to 5.5V		4		Ω
HVCC OV Protection Trip Threshold	V_{OV_HVCC}		5.65	5.85	6.05	V
HVCC Protection OV Threshold Hysteresis	$V_{OV\_HVCC\_HYST}$			75		mV
HVCC Overvoltage Blanking Timeout Period	t_{FP_HVCC}	From OV condition to switch opened		2		µs
	$t_{B\_OV\_HVCC}$	From switch opened due to OV to $\overline{FAULT}$ asserted		1		
CC Switch Single-End Capacitance	C_{ON_CC}			100		pF
CC Switch ON Leakage	$I_{CC\_ON\_LKG}$	CC switch ON, V_{CC1}/V_{CC2} = 5.5V, CC1/CC2 pin leakage			5	µA
$\overline{FAULT}$ Pin						
$\overline{FAULT}$ Output Low Voltage	V_{OL}	1mA forced into $\overline{FAULT}$ pin			0.5	V
$\overline{FAULT}$ Leakage Current	I_{FAULTB_LKG}	$\overline{FAULT}$ Pin = 3.3V or 5.0V			1	µA
$\overline{FAULT}$ Retry Timer	t_{RCV}	See Table 1.		16		ms
V_{CONN_EN1}, V_{CONN_EN2} Pins (MAX25410, MAX25410A)						
Input Logic High	$V_{VCONN\_EN\_IH}$		1.6			V

Electrical Characteristics (continued)

(T_A = -40 °C to +105 °C. Typical values are at V_{CC} = 5.0V, T_A = +25 °C, unless otherwise noted (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Logic Low	$V_{VCONN\_EN\_IL}$				0.5	V
Input Leakage Current	$I_{VCONN\_IN\_LKG}$				20	µA
CDP/DCP Pin						
Input Logic High	$V_{CDPDCP\_EN\_IH}$		1.6			V
Input Logic Low	$V_{CDPDCP\_EN\_IL}$				0.5	V
Input Leakage Current	$I_{CDPDCP\_IN\_LKG}$				5	µA
Thermal Shutdown						
Thermal Shutdown Temperature	T_{SHDN}	T_J Rising		165		ºC
Thermal Shutdown Hysteresis	T_{SHDN_HYS}			10		ºC
ESD Protection - HVCC1/HVCC2/HVD+/HVD- Pins						
ESD Protection Level	V_{ESD}	Human Body Model		±2		kV
ESD Protection Level (Note 4)	V_{ESD}	ISO 10605 Air Gap (330pF, 2kΩ)		±15		KV
		ISO 10605 Contact (330pF, 2kΩ)		±8		kV
		IEC 61000-4-2 Air Gap (150pF, 330Ω)		±15		
		IEC 61000-4-2 Contact (150pF, 330Ω)		±8		

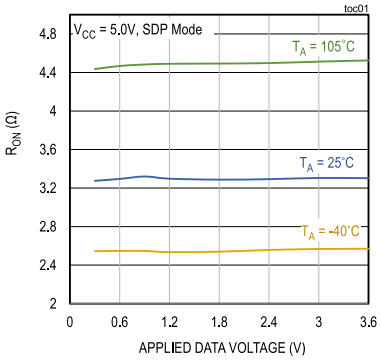
Note 3: Specification with minimum and maximum limits are 100% production tested at T_A = 25ºC and are guaranteed over the operating temperature range by design and characterization. Actual typical values may vary and are not guaranteed.

Note 4: Tested on EV kit.

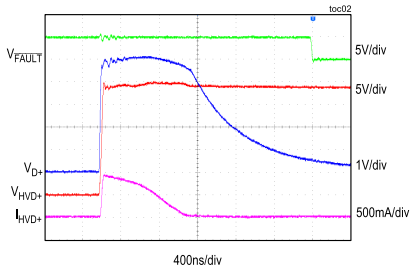
Typical Operating Characteristics

(VCC = 5.0V; T_A = 25ºC unless otherwise noted)

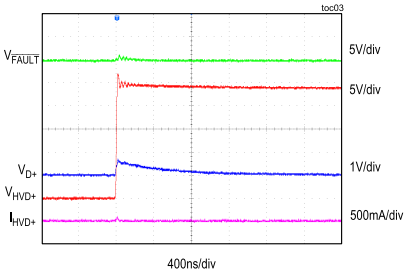
DATA SWITCH R_{ON} vs. APPLIED DATA VOLTAGE



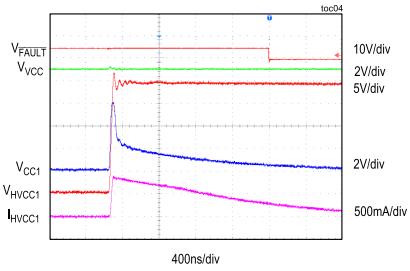
HVD± SHORT-TO-V_{BUS} 24V (POWERED)



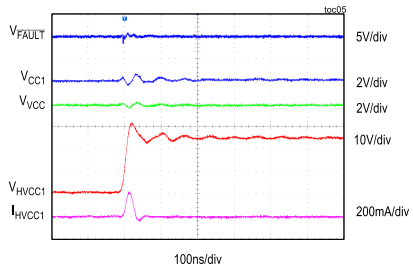
HVD± SHORT-TO-V_{BUS} 24V (UNPOWERED)



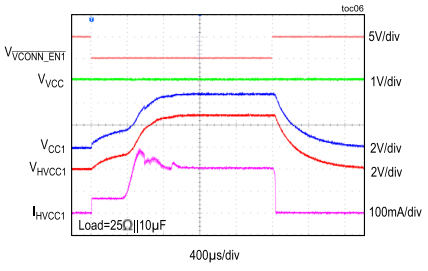
HVCC SHORT-TO-V_{BUS} 24V (POWERED)



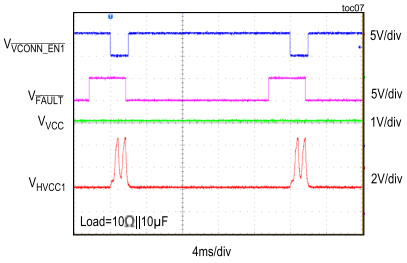
HVCC SHORT-TO-V_{BUS} 24V (UNPOWERED)



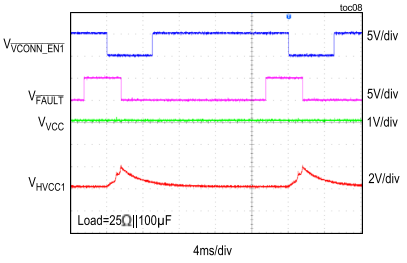
V_{CONN} ENABLED INTO COMPLIANT LOAD



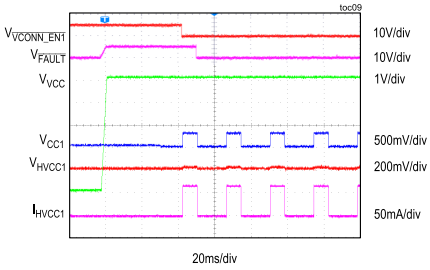
V_{CONN} ENABLED INTO NON-COMPLIANT LOAD



V_{CONN} ENABLED INTO NON-COMPLIANT LOAD



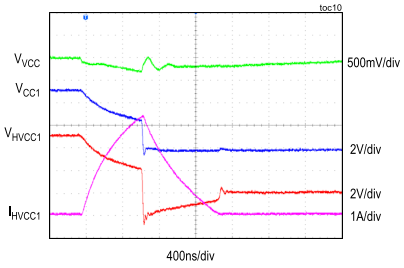
V_{CONN} ENABLED INTO SHORT-TO-GROUND AUTORETRY RESPONSE



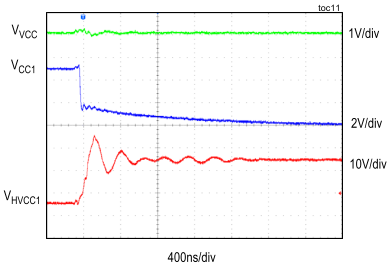
Typical Operating Characteristics (continued)

(VCC = 5.0V; T_A = 25ºC unless otherwise noted)

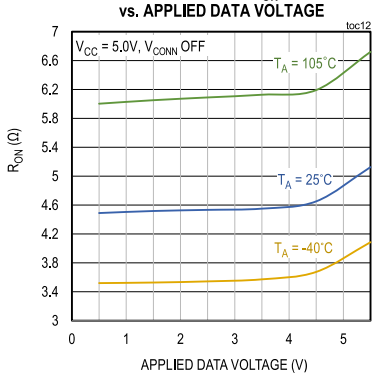
V_{CONN} SHORT-TO-GROUND RESPONSE



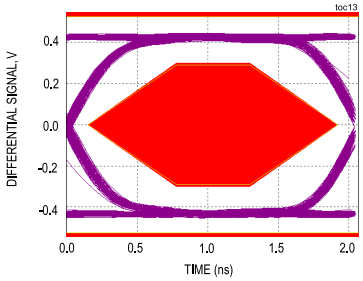
V_{CONN} SHORT-TO-VBUS 24V RESPONSE



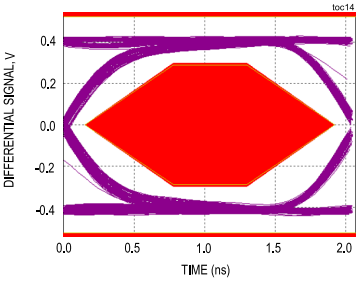
CC SWITCH R_{ON} vs. APPLIED DATA VOLTAGE



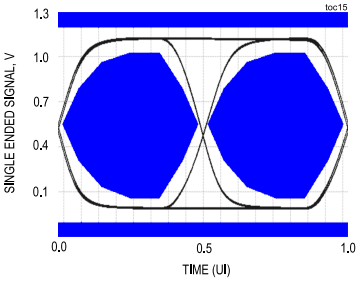
USB 2.0 EYE DIAGRAM TRANSMITTER ONLY



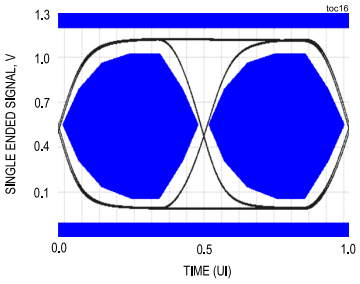
USB 2.0 EYE DIAGRAM WITH MAX25410 (UNTUNED)



BMC EYE DIAGRAM TRANSMITTER ONLY

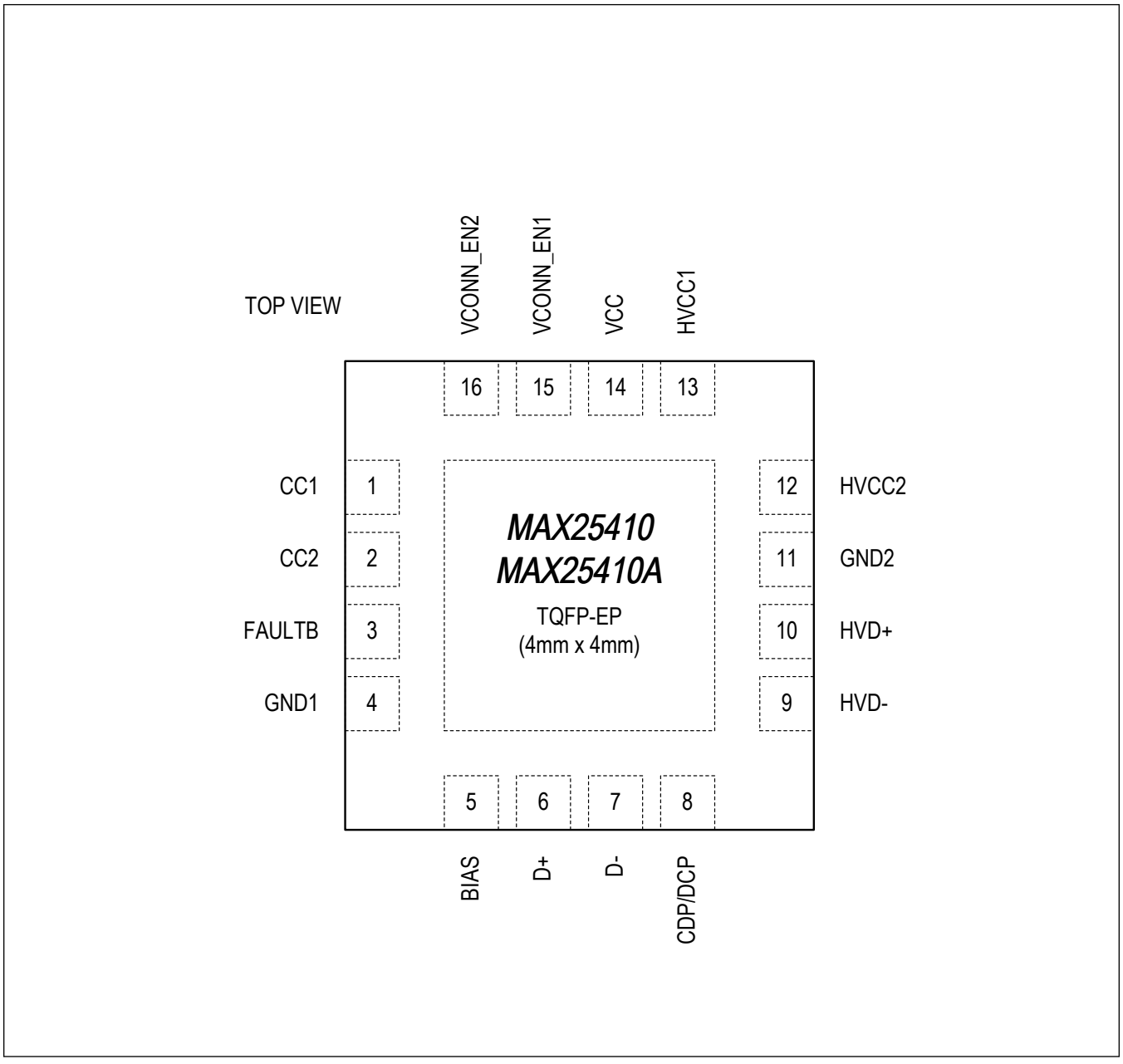


BMC EYE DIAGRAM WITH MAX25410

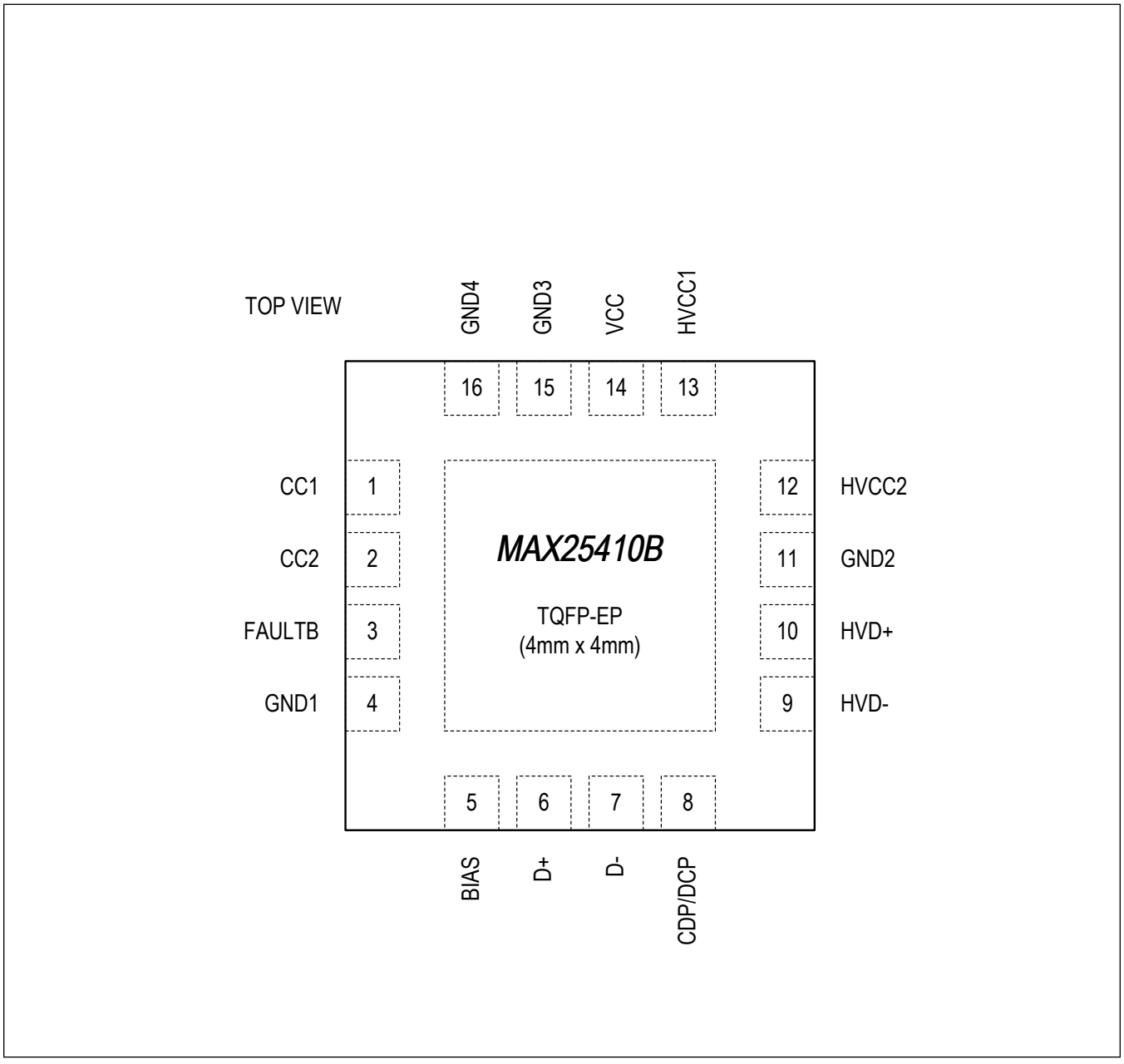


Pin Configurations

MAX25410, MAX25410A



MAX25410B

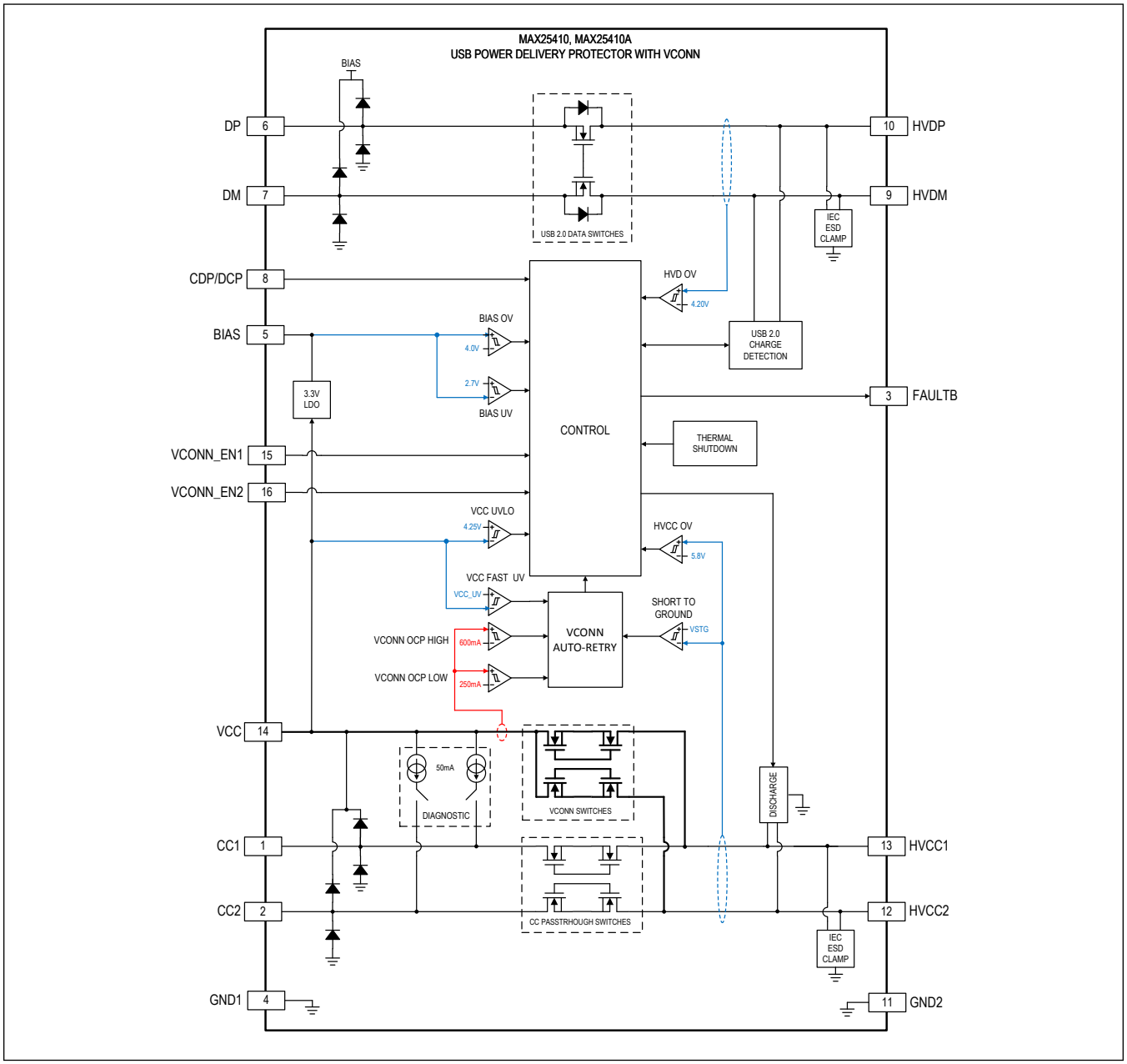

TOP VIEW
GND4
GND3
VCC
HVCC1
16
15
14
13
CC1
1
CC2
2
FAULTB
3
GND1
4
MAX25410B
TQFP-EP
(4mm x 4mm)
12
HVCC2
11
GND2
10
HVD+
9
HVD-
5
6
7
8
BIAS
D+
D-
CDP/DCP

Pin Description

PIN		NAME	FUNCTION
MAX25410, MAX25410A	MAX25410B		
1	1	CC1	Upstream CC1 Connection to USB-PD Host/Controller
2	2	CC2	Upstream CC2 Connection to USB-PD Host/Controller
3	3	$\overline{\text{FAULT}}$	Open-Drain Fault Output. Activation indicates that fault condition is present. Connect to host microcontroller, Type-C/PD port controller, or hub controller.
4	4	GND1	GND pin. Connect directly to GND; tie to GND pour underneath IC.
5	5	BIAS	BIAS Regulator Output. Connect 1µF ceramic decoupling capacitor from BIAS to GND.
6	6	D+	Upstream D+ or SBU Connection to Low-Voltage USB Transceiver
7	7	D-	Upstream D- or SBU Connection to Low-Voltage USB Transceiver
8	8	CDP/DCP	Data Switch Mode Select. This pin selects between the two default modes of data switch operation. The default modes are defined in the Table 5.
9	9	HVD-	Protected HVD- Connection to Downstream USB Type-C Connector or Captive Cable
10	10	HVD+	Protected HVD+ Connection to Downstream USB Type-C Connector or Captive Cable
11	11	GND2	GND Pin. Connect directly to GND; tie to GND pour underneath IC. Low GND connection impedance is critical for USB system performance.
12	12	HVCC2	Protected CC2 Connection to Downstream USB Type-C Connector or Captive Cable
13	13	HVCC1	Protected CC1 Connection to Downstream USB Type-C Connector or Captive Cable
14	14	V_{CC}	Main IC Supply and V_{CONN} Switch Input. Connect a local 1µF ceramic capacitor from V_{CC} to GND.
15	—	V_{CONN_EN1}	V_{CC}-to-HVCC1 V_{CONN} Switch Enable Pin. Active high or low depending on variant. Refer to *Ordering Information*.
—	15	GND3	GND pin. Connect directly to GND; tie to GND pour underneath IC.
16	—	V_{CONN_EN2}	V_{CC}-to-HVCC2 V_{CONN} switch Enable Pin. Active high or low depending on variant. Refer to *Ordering Information*.
—	16	GND4	GND pin. Connect directly to GND; tie to GND pour underneath IC.
17	17	EP	Exposed Pad. Connect directly to GND

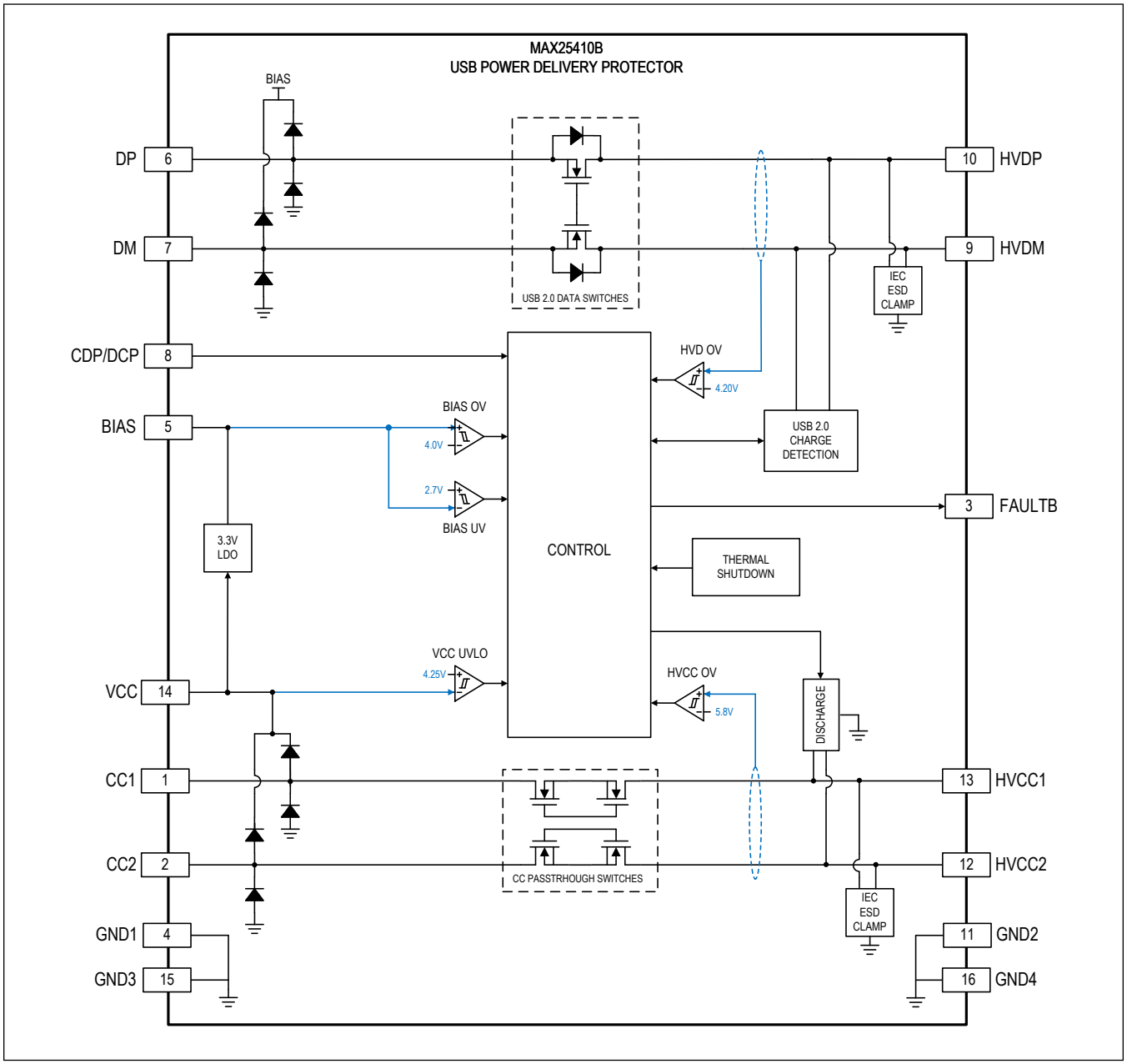
Functional Diagrams

MAX25410, MAX25410A



Functional Diagrams (continued)

MAX25410B



Detailed Description

The MAX25410 combines USB Type-C CC1/CC2 and D+/D-protection switches with an industry-leading integrated ESD and overvoltage protection. The IC is capable of delivering V_{CONN} power to the HVCC1 or HVCC2 outputs with minimal voltage drop, supports charge emulation, and supports USB LS/FS/HS communication on the D+/D- switches.

The device features automotive-grade ±15kV IEC 61000-4-2 ESD protection on all protected outputs, as well as 24V overvoltage protection on the CC and data switches. The integrated Type-C discharge switch features high-ESD protection and integrated overvoltage-detection logic.

The MAX25410 is designed for installation in USB Type-C head units/hubs/dedicated charging ports where automotive-grade ESD and overvoltage protection is required for sensitive upstream hosts.

Protection and Control

CC1/CC2 Pins

The CC1 and CC2 pins are the protected side of the CC switches and connect directly to the USB-PD controller. A 390pF capacitance to ground is recommended on both CC1 and CC2 pins, which can be the USB-PD Controller's cReceiver capacitance.

HVCC1/HVCC2 Pins

The HVCC1 and HVCC2 pins connect directly to the downstream USB Type-C port connector or captive cable. No external circuitry is needed on either HVCC pin. HVCC1 and HVCC2 are tolerant to automotive high ESD, up to 24V DC, and up to 40V voltage transients. HVCC1 and HVCC2 are automatically discharged for 30ms at power-up or after specific fault conditions (see Table 1), and for 10ms every time V_{CONN} is disabled.

D+/D- Pins

The D+ and D- pins are the protected side of the USB data switches and connect directly to the low-voltage upstream USB PHY or captive cable. No external circuitry is used on either data pin.

HVD+/HVD- Pins

The HVD+ and HVD- pins should be routed to the downstream Type-C connector or captive cable. No external circuitry is required on either pin. The HVD+ pin and HVD- pin are tolerant to automotive high ESD, up to 24V DC, and up to 40V voltage transients.

V_{CONN_EN1}/V_{CONN_EN2} Pins (MAX25410, MAX25410A)

The V_{CONN} switch allows pins to enable only one of the two V_{CONN} switches: V_{CC}-to-HVCC1 pins or V_{CC}-to-HVCC2 pins, active-high or active-low, depending on the variant. See *VCONN Switch/CC Pass Through Switch Enable Table* and the *Ordering Information* section.

$\overline{FAULT}$ Pin

The $\overline{FAULT}$ pin is an open-drain fault-indication pin that asserts upon fault detection. For faults unrelated to V_{CONN}, such as an overvoltage on HVCC or HVD pins, the $\overline{FAULT}$ pin will remain asserted continuously until the fault is no longer present.

During a V_{CONN} short-to-ground fault, the $\overline{FAULT}$ pin asserts and remains asserted until the fault is no longer present or the PD controller disables V_{CONN}.

For a non-compliant V_{CONN} load fault, the IC will attempt to retry and provide V_{CONN} automatically until the fault is no longer present or the PD controller disables V_{CONN}.

Refer to Table 1 and the V_{CONN} Auto-Retry section for additional information.

V_{CONN} Switches (MAX25410, MAX25410A)

The advantage of MAX25410 is the ability to switch power from a low-power system supply to a wide range of E-marked cables (that is, using the same supply that powers the USB-PD Controller). This essentially reduces the current budget needed for supplying V_{CONN} and therefore reduces solution cost and size.

Certain E-marked cables, however, draw currents that exceed the Type-C specification of 1W maximum shortly after V_{CONN} is sourced, which causes unwanted inrush currents and droops on the system supply, ultimately causing a module reset.

To overcome this limitation while providing the 1W V_{CONN} required by Type-C, MAX25410 implements a Fast UV comparator on V_{CC} and dual-threshold overcurrent protection with specific debounce timers. The first overcurrent threshold (OCP Low) is set at 250 mA with a debounce of 400µs, which permits exceeding the 1W limit momentarily to start up the E-marked cable circuitry. The second OCP threshold (OCP High) is set to 600 mA and has a debounce of 5 µs, which protects the system supply from non-compliant V_{CONN} loads and/or short circuits.

V_{CONN} Auto-Retry (MAX25410, MAX25410A)

Due to the V_{CC} supply being a shared supply, asynchronous system loads can occur while sourcing V_{CONN}. For this reason, a V_{CONN} Auto-Retry feature is implemented to minimize the software interaction of sourcing V_{CONN} with a shared supply.

If a V_{CONN} load (E-marked cable or VPD) tries to draw an excessive amount of current for more than the debounce time, the V_{CONN} switch will automatically open to avoid drooping the upstream power supply, then automatically retry. The USB-PD Controller can take action when the $\overline{FAULT}$ pin asserts. If $\overline{FAULT}$ de-asserts upon disabling V_{CONN}, the PD Controller can proceed without powering the non-compliant E-marked cable until a new cable is detected.

The V_{CONN} auto-retry feature is active for the following V_{CONN}-related faults:

- V_{CONN} OCP LOW
- V_{CONN} OCP HIGH
- V_{CC} FAST UV
- V_{CONN} SHORT TO GROUND

For the other faults, such as HVD and HVCC OV, VCC UVLO, BIAS OV/UV, $\overline{FAULT}$ remains asserted as long as the fault exists.

After V_{CONN} is enabled on a CC channel, the IC monitors for additional faults related to V_{CONN} operation. On the first V_{CONN} fault and after the debounce time, the V_{CONN} switch is immediately turned off, the diagnostic current is enabled on the corresponding channel, and the short-to-ground comparator is active and monitoring HVCC.

Note that during the V_{CONN} fault conditions (except V_{CONN} OV), the CC pass-through switches are always on, which allows the PD Controller to monitor V_{CONN} for further diagnostics.

Automatic Discharge (MAX25410, MAX25410A) To comply with the Type-C specification, the HVCC pins will be discharged for 10ms every time V_{CONN} is disabled (i.e., V_{CONN_EN1} goes from high to low for active-high variants, or goes from low to high for active-low variants).

Table 1. Fault Table

FAULT	COMPARATOR DEBOUNCE TIME PRIOR TAKING ACTION	ACTION TAKEN	FAULT RECOVERY
Thermal Shutdown (Die Temp >165°C (Typ))	100µs	Open CC pass-through switch, open data switches, open V_{CONN} switch, and reset BC1.2 charge detection. Assert $\overline{FAULT}$.	When the fault condition no longer exists and the 16ms retry timer has expired, release the fault, then discharge the HVCC1 and HVCC2 pins, then go to the current pin-configured state.
Bias Overvoltage	Immediate	Open CC pass-through switch, open data switches, open V_{CONN} switch, and reset BC1.2 charge detection. Assert $\overline{FAULT}$.	When the fault condition no longer exists and the 16ms retry timer has expired, release the fault, then discharge the HVCC1 and HVCC2 pins, then go to the current pin-configured state.

Table 1. Fault Table (continued)

Bias Undervoltage	1.8ms	Open CC pass-through switch, open data switches, open V_{CONN} switch, and reset BC1.2 charge detection. Assert $\overline{FAULT}$.	When the fault condition no longer exists and the 16ms retry timer has expired, release the fault, then discharge the HVCC1 and HVCC2 pins, then go to the current pin-configured state.
HVDM/ HVDP Pin Overvoltage or Short-to-V_{BUS}	Immediate	Open CC pass-through switch, open data switches, open V_{CONN} switch, and reset BC1.2 charge detection. Assert $\overline{FAULT}$.	When the fault condition no longer exists and the 16ms retry timer has expired, release the fault, then discharge the HVCC1 and HVCC2 pins, then go to the current pin-configured state.
V_{CC} UVLO	16ms	Open CC pass-through switch, open data switches, open V_{CONN} switch, and reset BC1.2 charge detection. Assert $\overline{FAULT}$.	When the fault condition no longer exists and the 16ms retry timer has expired, release the fault, then discharge the HVCC1 and HVCC2 pins, then go to the current pin-configured state.
V_{CC} Fast UV (Only when V_{CONN} is Enabled) (Note 5)	Immediate	Open V_{CONN} switch. Assert $\overline{FAULT}$.	When the fault condition no longer exists and the 16ms retry timer has expired, release the fault, then re-start the V_{CONN} switch based on the current V_{CONN_EN1} and V_{CONN_EN2} pin configuration. No HVCC1 and HVCC2 discharge for this fault; ignore CDP/DCP pin state.
HVCC1/ HVCC2 Pin Overvoltage or Short-to-V_{BUS}	Immediate	Open CC pass-through switch, open data switches, open V_{CONN} switch, and reset BC1.2 charge detection. Assert $\overline{FAULT}$.	When the fault condition no longer exists and the 16ms retry timer has expired, release the fault, then discharge the HVCC1 and HVCC2 pins, then go to the current pin-configured state.
V_{CONN} Overcurrent Threshold (Low) (Note 5)	400µs	Open V_{CONN} switch and if HVCC is below the short-to-ground threshold, then assert $\overline{FAULT}$ after 8ms. If HVCC is above the short-to-ground threshold, restart the V_{CONN} switch. Assert $\overline{FAULT}$ if retry is unsuccessful after two attempts.	When the fault condition no longer exists and the 16ms retry timer has expired, release the fault, then restart the V_{CONN} switch based on the current V_{CONN_EN1} and V_{CONN_EN2} pin configuration. No HVCC1 and HVCC2 discharge for this fault; ignore CDP/DCP pin state.
V_{CONN} Overcurrent Threshold (High) (Note 5)	5µs	Open V_{CONN} switch and if HVCC is below the short-to-ground threshold, then assert $\overline{FAULT}$ after 8ms. If HVCC is above the short-to-ground threshold, restart the V_{CONN} switch. Assert $\overline{FAULT}$ if re-try is unsuccessful after two attempts.	When the fault condition no longer exists and the 16ms retry timer has expired, release the fault, then restart the V_{CONN} switch based on the current V_{CONN_EN1} and V_{CONN_EN2} pin configuration. No HVCC1 and HVCC2 discharge for this fault; ignore CDP/DCP pin state.
V_{CONN} Overvoltage (Note 5)	Immediate	When HVCC1-to-V_{CC} or HVCC2-to-V_{CC} pin voltage exceeds 120mV (typ.) while V_{CONN} is enabled: open CC pass-through switch, open data switches, open V_{CONN} switch, and reset BC1.2 charge detection. Assert $\overline{FAULT}$.	When the fault condition no longer exists and the 16ms retry timer has expired, release the fault, then discharge the HVCC1 and HVCC2 pins, then go to the current pin-configured state.

Note 5. V_{CONN} faults actions and fault recoveries are only applicable to MAX25410 and MAX2510A.

Power up and Enabling

Supply and System Enable (V_{CC})

The V_{CC} pin is the power-supply pin and also the internal chip-enable pin. All switches (CC1, CC2, D-, D+) remain ON any time that the V_{CC} pin is above the undervoltage threshold and the $\overline{FAULT}$ pin is not asserted.

Modes of Operation

V_{CONN} Switch/CC Pass-Through Switch Enable Tables

Table 2. V_{CONN} Switch-Enable Table (MAX25410: Active-High Variants)

$V_{CC} > V_{CC\_UVLO}$	V_{CONN_EN1}	V_{CONN_EN2}	CC1/CC2 PASS-THROUGH	HVCC1 V_{CONN} SWITCH	HVCC2 V_{CONN} SWITCH
No	x	x	OFF	OFF	OFF
Yes	0	0	ON	OFF	OFF
	0	1		OFF	ON
	1	0		ON	OFF
	1	1		OFF	OFF

Table 3. V_{CONN} Switch-Enable Table (MAX25410A: Active-Low Variants)

$V_{CC} > V_{CC\_UVLO}$	V_{CONN_EN1}	V_{CONN_EN2}	CC1/CC2 PASS-THROUGH	HVCC1 V_{CONN} SWITCH	HVCC2 V_{CONN} SWITCH
No	x	x	OFF	OFF	OFF
Yes	0	0	ON	OFF	OFF
	0	1		ON	OFF
	1	0		OFF	ON
	1	1		OFF	OFF

Table 4. CC Pass-Through Switch Enable Table (MAX25410B Variants)

$V_{CC} > V_{CC\_UVLO}$	CC1/CC2 PASS-THROUGH
No	OFF
Yes	ON

USB Host Adapter Emulator

The USB protection switches integrate the latest USB-IF Battery-Charging Specification Revision 1.2 CDP and DCP circuitry, as well as 1.0A and 2.4A resistor-bias options for Apple-compliant devices. Legacy Samsung Galaxy 1.2V divider and China YD/T1591-2009 compatibility is also provided by the Auto-DCP mode.

Table 5. Data Switch Mode Truth Table

DEVICE	CDP/DCP PIN	CHARGE-DETECTION MODE
MAX25410BGTE/V+, MAX25410AGTE/V+, MAX25410GTE/V+	0	Auto-CDP
	1	Auto-DCP/Apple 2.4A
MAX25410BGTEA/V+, MAX25410AGTEA/V+, MAX25410GTEA/V+	0	Hi-Speed Pass-Through (SDP)
	1	Auto-CDP

USB On-the-Go and Dual-Role Applications

The MAX25410 is fully compatible with USB on-the-go (OTG) and dual-role applications. A negotiated role swap (HNP or Apple CarPlay) requires no software interaction with the IC. When there is no negotiation before the SoC enters peripheral mode, the MAX25410 must be in Hi-Speed pass-through (SDP mode) before and during the role swap. The MAX25410GTEA/V+, MAX25410AGTEA/V+ and MAX25410BGTEA/V+ default to SDP mode on startup if the CDP/DCP pin is logic-low. This configuration allows a role swap immediately on startup without microcontroller interaction

Timing Diagrams/Test Circuits

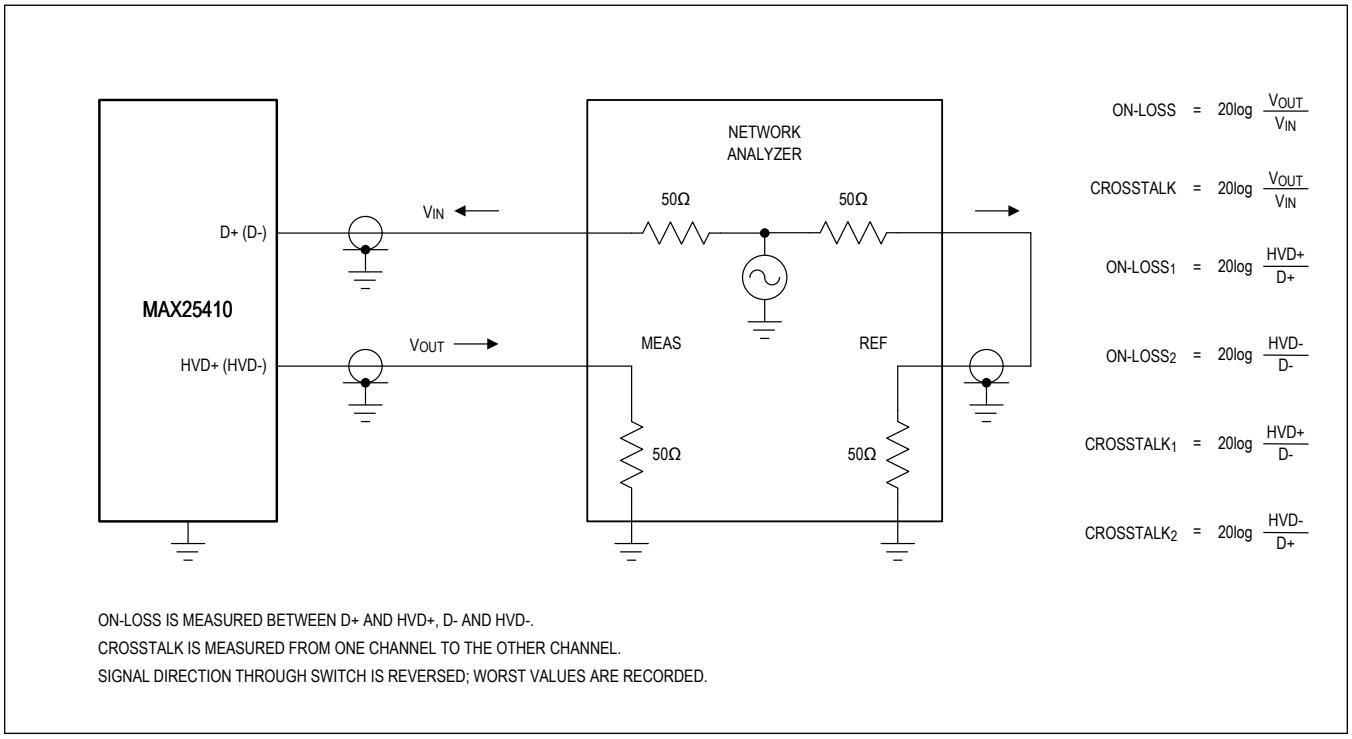


Figure 1. In-Channel -3dB Bandwidth and Crosstalk

Applications Information

V_{CC} Bypass Capacitor

V_{CC} is the main IC supply, and the V_{CONN} switch input. V_{CC} requires a minimum 1µF ceramic capacitor (X5R or better) for input supply current and V_{CONN} switch usage. The capacitor must be as close as possible to the V_{CC} pin and have a short connection to the IC exposed pad. Using vias to connect to the ground layer is recommended. For best performance, use a low-impedance path to connect the 5V system power supply to the V_{CC} pin.

BIAS Bypass Capacitor

BIAS is the output of the internal LDO and clamp rail for the USB data switches. BIAS requires a minimum 1µF ceramic capacitor (X5R or better) for decoupling and to provide an AC return path on transient events (overvoltage, ESD). The capacitor must be as close as possible to the BIAS pin and have a short connection to the IC exposed pad. Ground flood over GND1 (pin 4) is recommended.

Layout of USB Data-Line Traces

USB Hi-Speed mode requires careful PCB layout with 90Ω controlled differential impedance-matched traces of equal length. Insert tuning peaking inductors and capacitors on the D+, D-, HVD+, and HVD- pins to tune out parasitic capacitance. The values are layout dependent. Contact Maxim Applications for assistance.

Tuning of USB Data Lines

USB Hi-Speed mode requires careful PCB layout with 90Ω controlled differential impedance, with matched traces of equal length and with no stubs or test points. MAX25410 includes high-bandwidth USB data switches (1GHz). This means data-line tuning is generally not required.

However, all designs are recommended to include pads that would allow LC components to be mounted on the data lines so that tuning can easily be performed later, if necessary. Tuning components should be placed as close as possible to the IC data pins, on the same layer of the PCB as the IC. The proper configuration of the tuning components is shown in Figure 2. Tuning inductors should be high-Q wire-wound inductors. Contact Maxim's application team for assistance with the tuning process for your specific application.

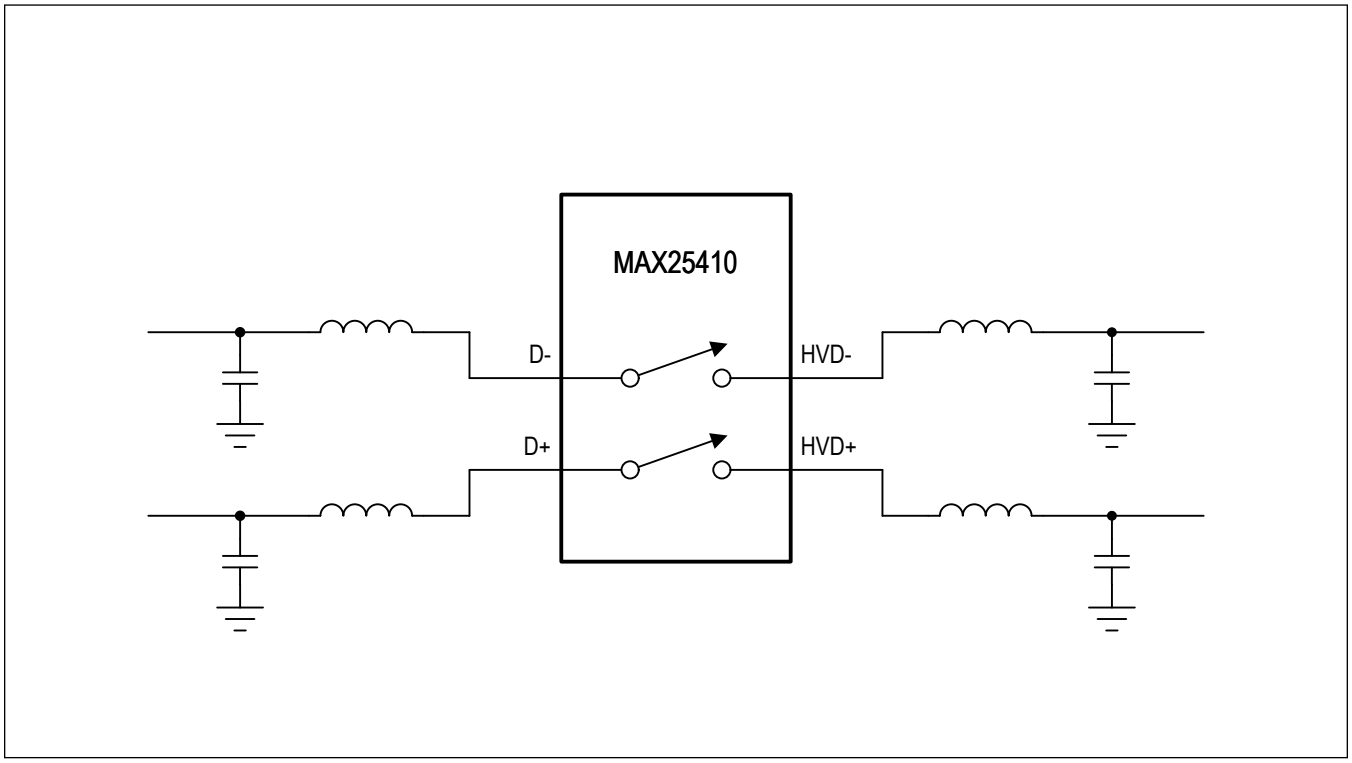


Figure 2. Tuning of Data Lines

±15kV ESD Protection

Maxim devices incorporate ESD-protection structures to protect against electrostatic discharges encountered during handling and assembly. The devices provide additional protection against static electricity. Maxim's state-of-the-art structures protect against ESD of ±15kV on HVD+, HVD-, HVCC1, and HVCC2. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. While other solutions can latch up and require the power to be cycled after an ESD event, MAX25410 devices continue to work without latchup. The devices are characterized for protection to the following limits:

1. ±2kV using the Human Body Model
2. ±15kV using the IEC 61000-4-2 Air Gap method
3. ±8kV using the IEC 61000-4-2 Contact Discharge method
4. ±15kV using the ISO 10605 Air Gap method
5. ±8kV using the ISO 10605 Contact Discharge method

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 3 shows the Human Body Model, and Figure 4 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

Human Body Test Model

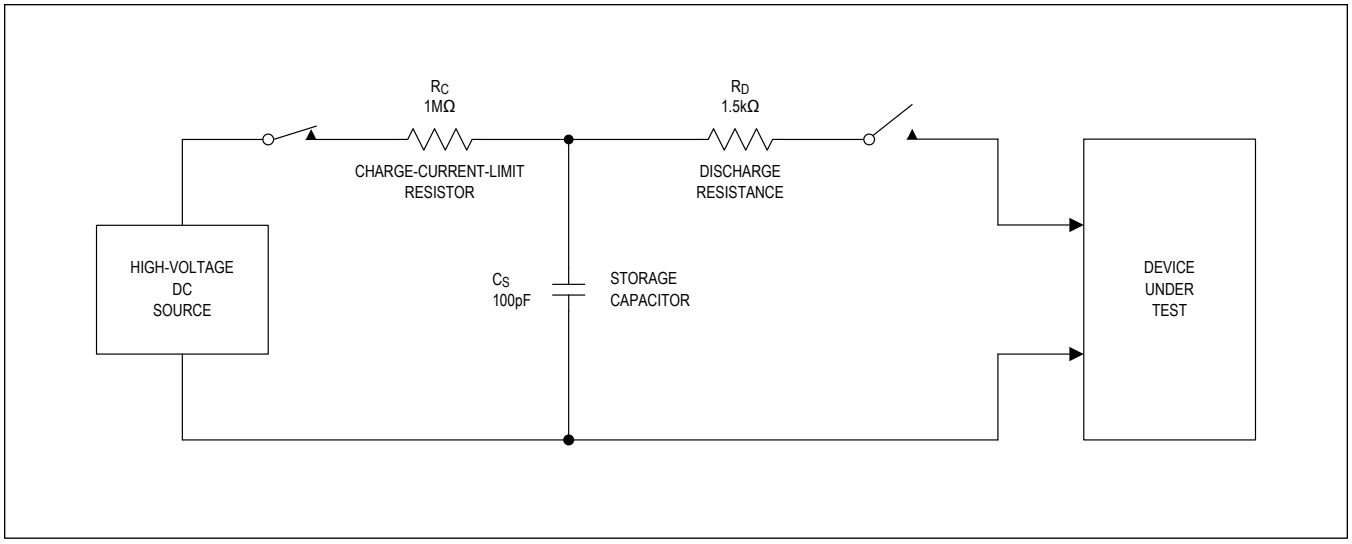


Figure 3. Human Body Test Model

Human Body Current Waveform

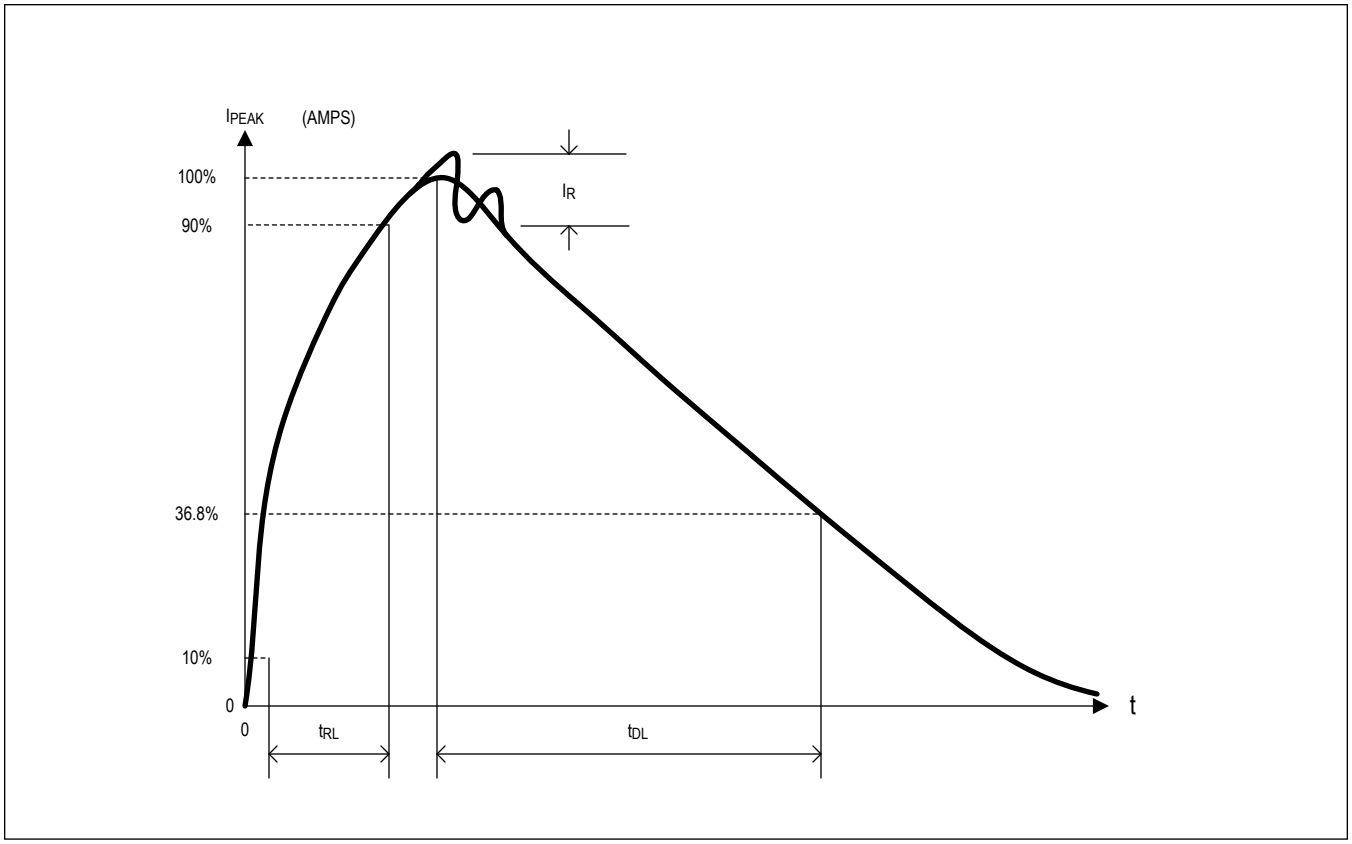


Figure 4. Human Body Current Waveform

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. The devices help users design equipment that meet Level 4 of IEC 61000-4-2. The Human Body Model testing is performed on unpowered devices, while IEC 61000-4-2 is performed while the device is powered. The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 5), the ESD-withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 6 shows the current waveform for the ±8kV, IEC 61000-4-2 Level 4, ESD Contact Discharge test. The Air Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

IEC 61000-4-2 ESD Test Model

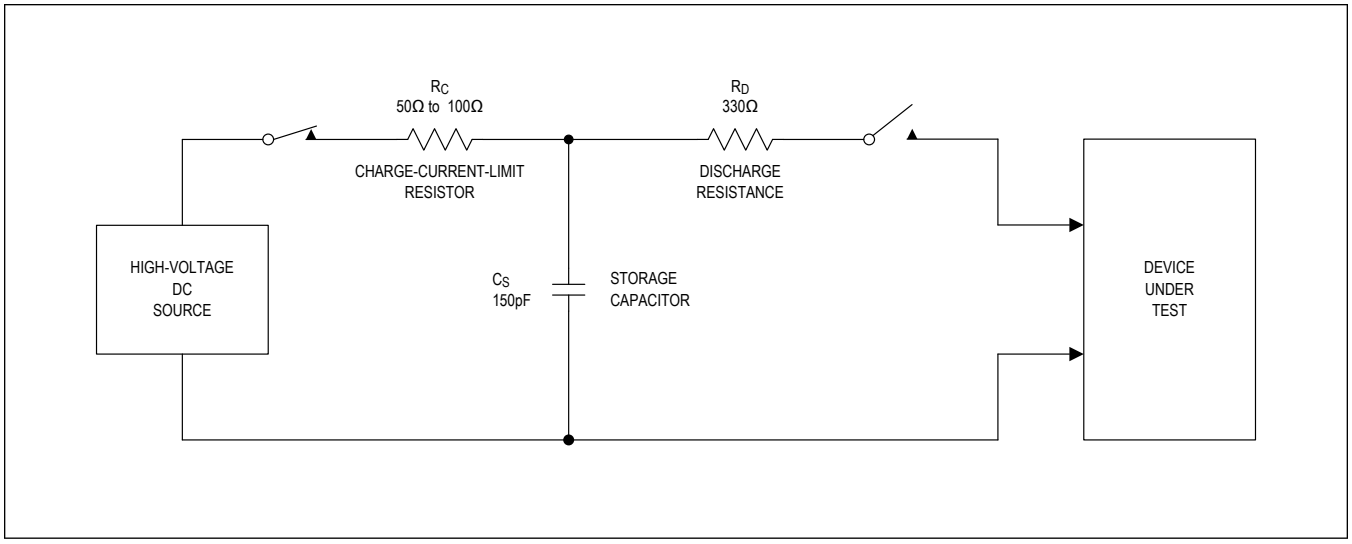


Figure 5. IEC 61000-4-2 ESD Test Model

IEC 61000-4-2 ESD Generator Current Waveform

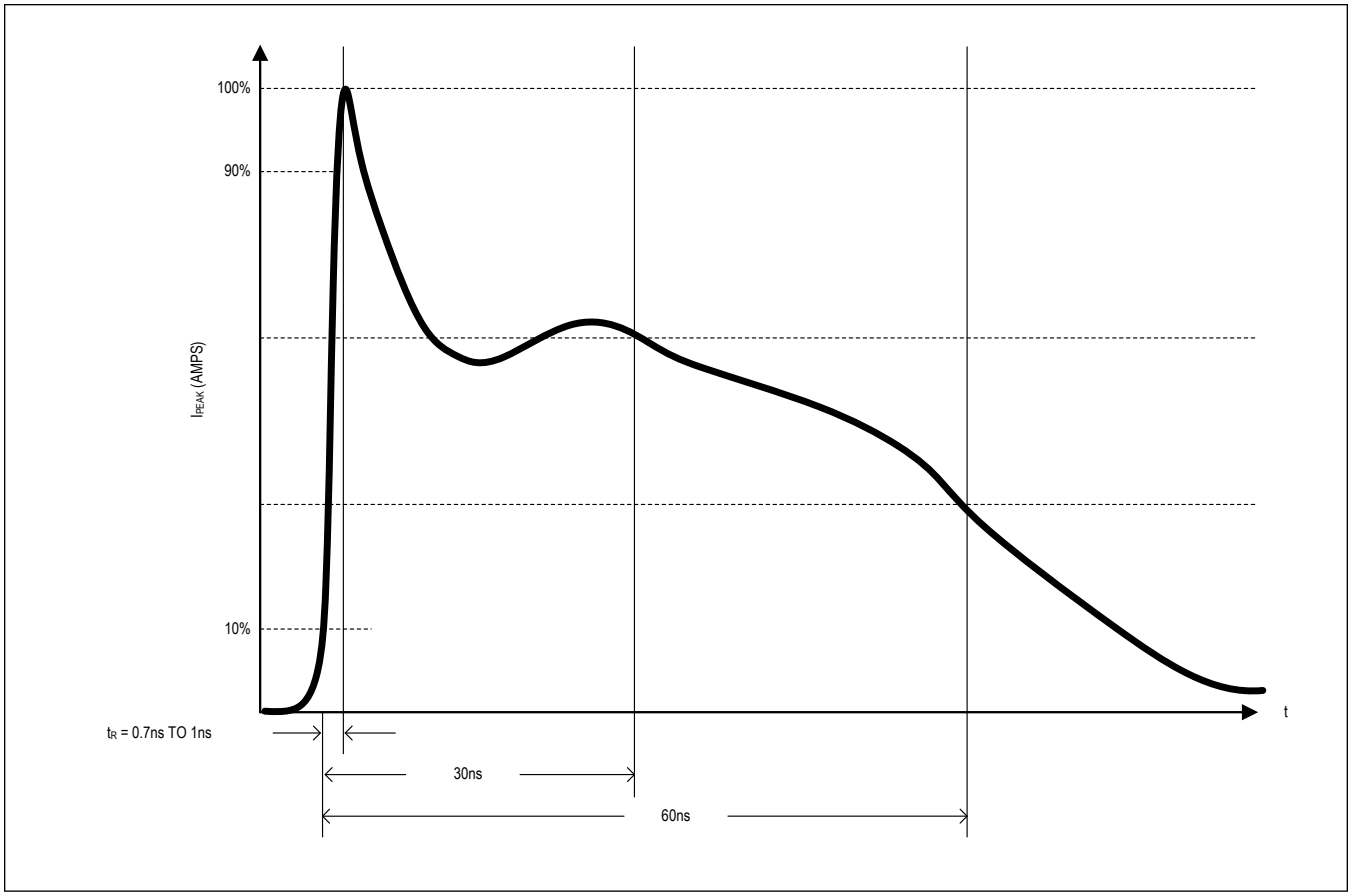
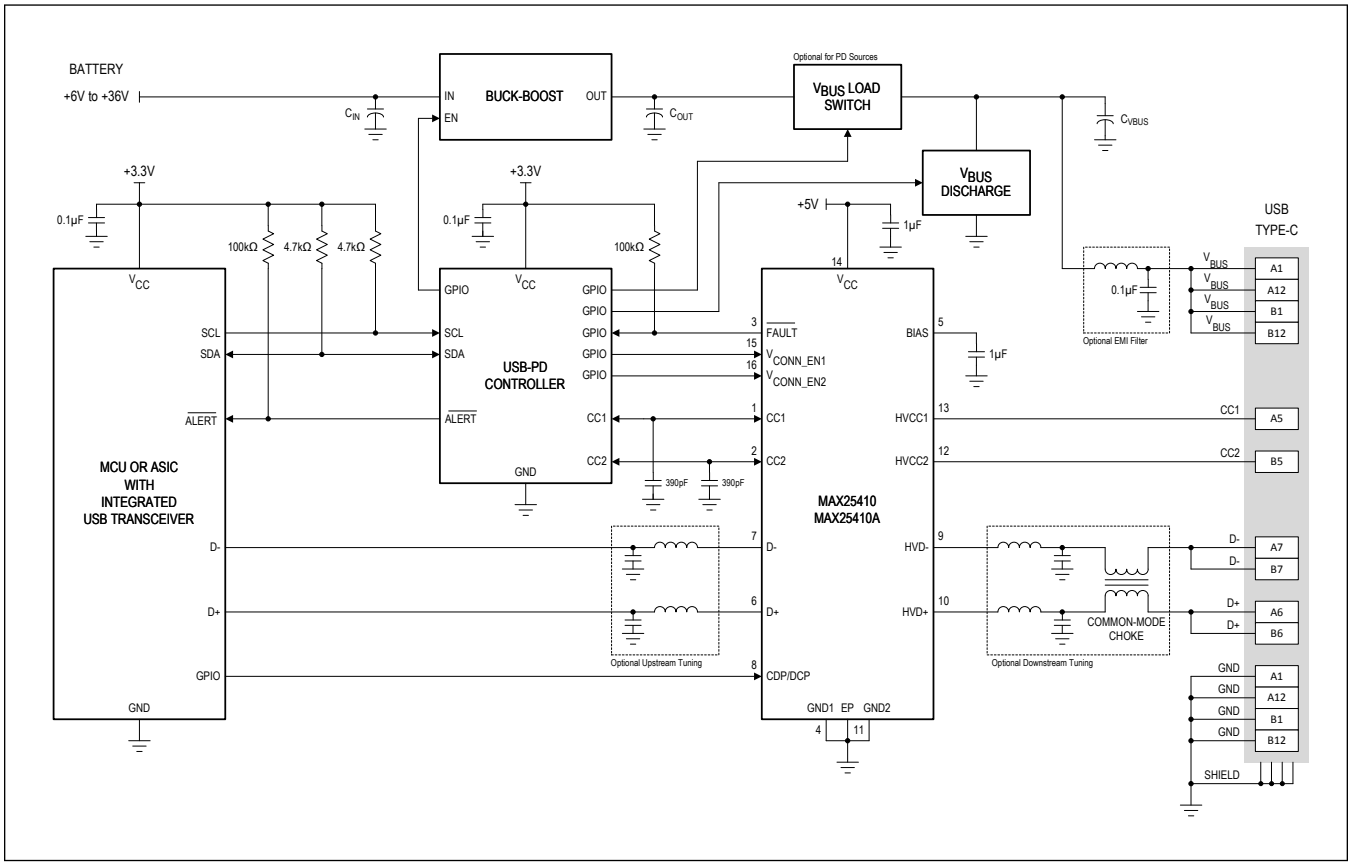


Figure 6. IEC 61000-4-2 ESD Generator Current Waveform

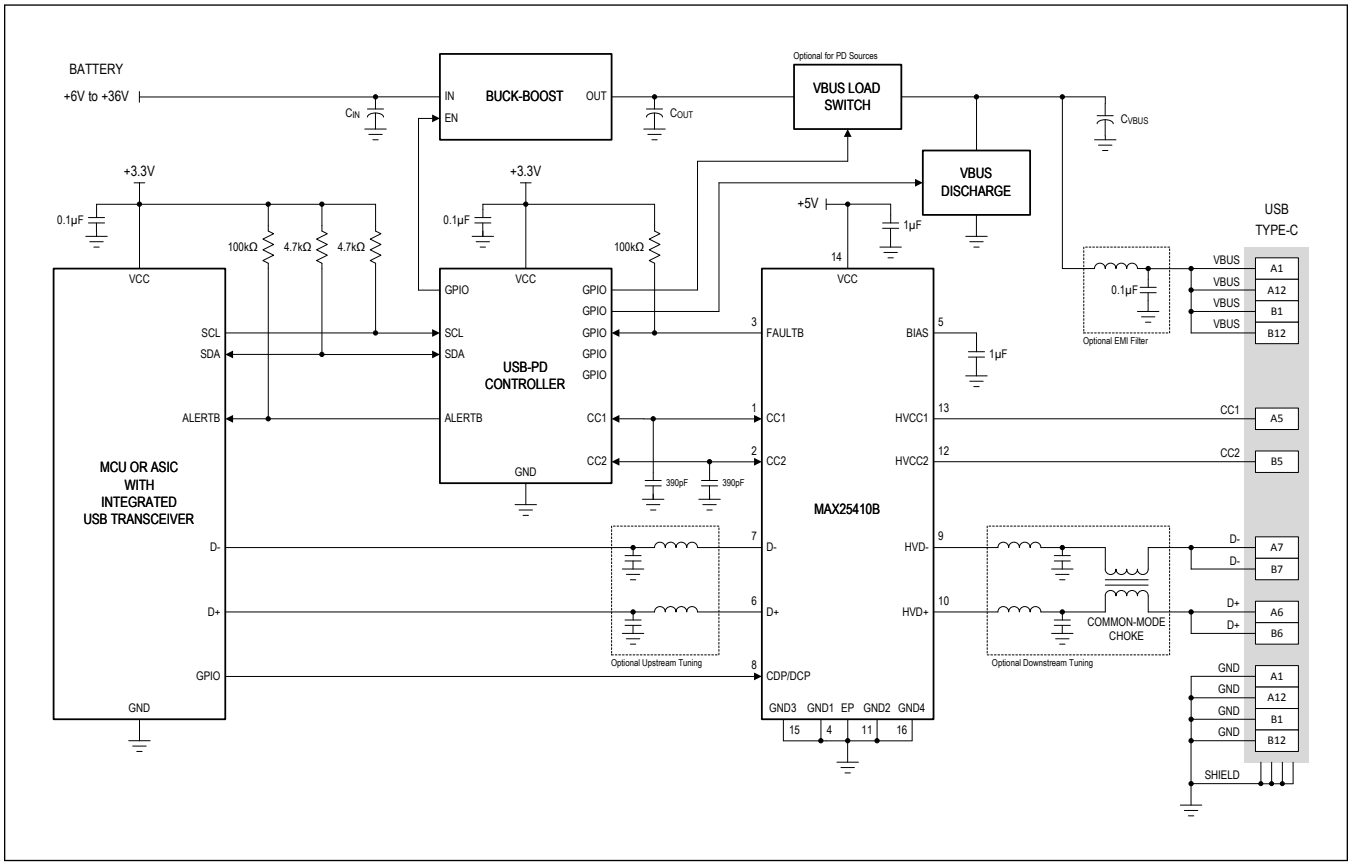
Typical Application Circuits

MAX25410, MAX25410A



Typical Application Circuits (continued)

MAX25410B



Ordering Information

PART NUMBER	V_{CONN}	V_{CONN} ENABLE POLARITY	USB MODES SUPPORTED	TEMPERATURE RANGE	PIN-PACKAGE
MAX25410AGTE/V+	Yes	Active-Low	Auto-CDP, Auto-DCP/Apple 2.4A	-40ºC to +105ºC	TQFN-EP 16-pin
MAX25410GTE/V+		Active-High			
MAX25410BGTE/V+	No	-			
MAX25410AGTEA/V+	Yes	Active-Low	Auto-CDP, SDP(Pass-Through)		
MAX25410GTEA/V+		Active-High			
MAX25410BGTEA/V+	No	-			

All devices operate over the temperature range of -40°C to +105°C and support USB CDP/HS modes.

To order Tape and Reel, suffix the part number with a T. Example: MAX25410GTE/V+T

/V denotes AEC-Q100 Automotive Qualified.

+ Denotes Lead(Pb)-Free/RoHS-compliant package.

EP denotes Exposed Pad

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/19	Initial release	—
1	10/19	Updated *Ordering Information*	25
2	4/20	Updated *General Description, Electrical Characteristics, Pin Configurations, Functional Diagrams, Detailed Description, Modes of Operation, Typical Application Circuits, Ordering Information*	1, 4, 5, 9, 10, 12–17, 25–27

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX25410GTE/V+T MAX25410AGTEA/V+ MAX25410GTEA/V+ MAX25410GTEA/V+T MAX25410AGTE/V+T MAX25410AGTEA/V+T MAX25410GTE/V+ MAX25410BGTEA/V+ MAX25410BGTEA/V+T MAX25410BGTE/V+ MAX25410BGTE/V+T