MAX25232

36V, 3A Mini Buck Converters with 3.5µA I_Q

General Description

The MAX25232 is a small, synchronous buck converter with integrated high-side and low-side switches. The device is designed to deliver up to 3A with 3.5V to 36V input voltages while using only 3.5µA quiescent current at no load.

The device provides an accurate output voltage of ±2% in FPWM mode within the normal 6V to 18V operation input range. With 65ns minimum on-time capability, the converter is capable of large input-to-output conversion ratios. Voltage quality can be monitored by observing the PGOOD signal. The device can operate in dropout by running at 99% duty cycle, making it ideal for automotive and industrial applications. The IC comes in fixed output voltage and adjustable output voltage (MAX25232ATCF and MAX25232ATCG only) options. For MAX25232ATCF and MAX25232ATCG, output voltage can be set between 3V and 10V using an external resistor-divider. Frequency is internally fixed at 2.1MHz, which allows for small external components and reduced output ripple, and guarantees no AM interference. A 400kHz option is also offered to provide minimum switching losses and maximum efficiency. The device automatically enters skip mode at light loads with ultra-low 3.5µA quiescent current at no load. The device offers pin-enabled spread-spectrum-frequency modulation designed to minimize EMI-radiated emissions due to the modulation frequency.

The MAX25232 variants are available in a small (3mm x 3mm) 12-pin TDFN package with an exposed pad, and requires very few external components.

Applications

- Automotive
- Industrial
- High-Voltage DC-DC Converters

Benefits and Features

- Synchronous DC-DC Converter with Integrated FETs
  - MAX25232ATCA/ATCB/ATCG/ATCH = 2.5A I_{OUT}
  - MAX25232ATCD/ATCE/ATCF = 3A I_{OUT}
  - 3.5µA Quiescent Current in Standby Mode
- Small Solution Size Saves Space
  - 65ns Minimum On-Time
  - 2.1MHz or 400kHz Operating Frequency
  - Fixed 5V/3.3V Output Voltage with ±2% Output Accuracy in FPWM Mode (5V/3.3V)
  - Other Fixed V_{OUT} Options Between 3V - 5.5V (in 50mV steps) Available for Precise Output Voltage Setting
  - External Resistor Divider Options to Adjust the Output Voltage Between 3V and 10V
  - Fixed 3.5ms Internal Soft-Start
  - Innovative Current-Mode-Control Architecture Minimizes Total Board Space and BOM Count
- PGOOD Output and High-Voltage EN Input Simplify Power Sequencing
- Protection Features and Operating Range Ideal for Automotive Applications
  - 3.5V to 36V Operating V_{IN} Range
  - 40V Load-Dump Protection
  - 99% Duty-Cycle Operation with Low Dropout
  - -40°C to +125°C Automotive Temperature Range
  - AEC-Q100 Qualified

***Ordering Information* appears at end of data sheet.**

19-100723; Rev 3; 4/21

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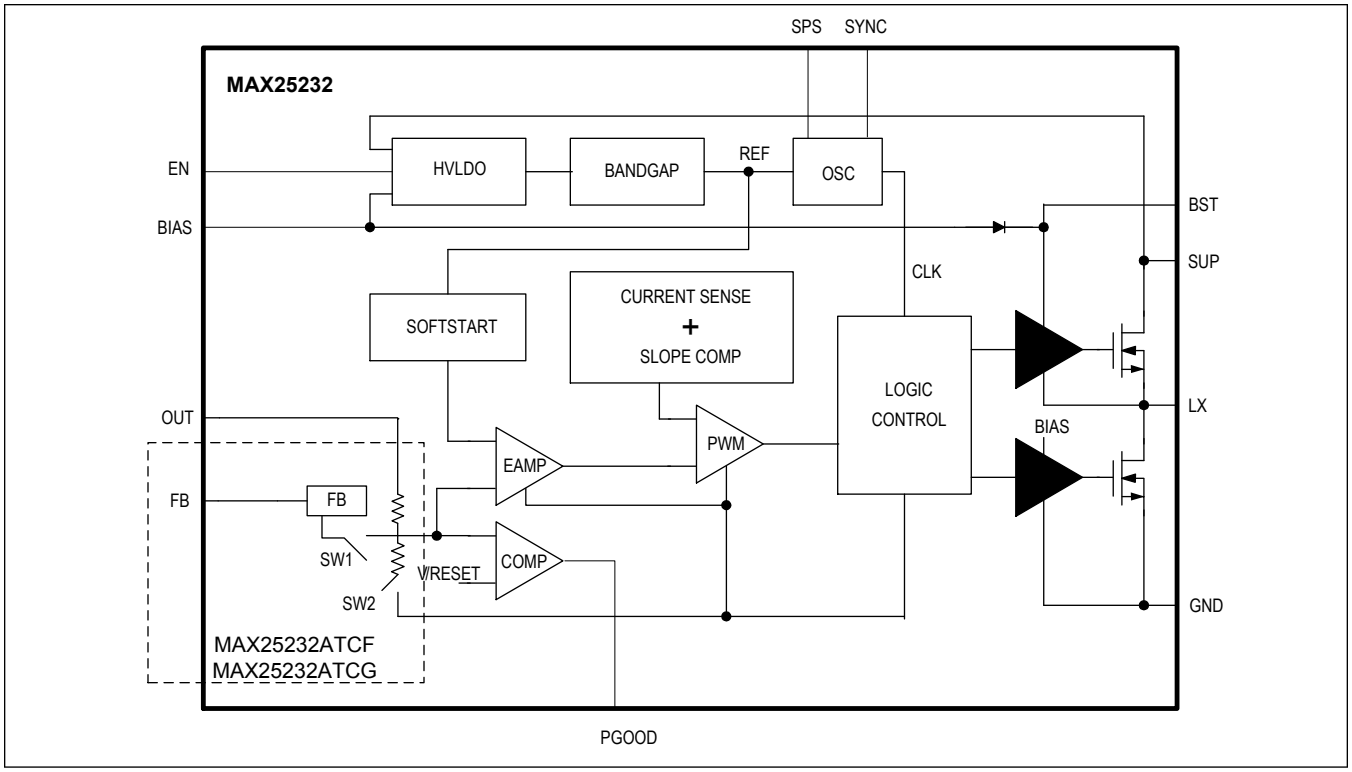
Simplified Block Diagram



Absolute Maximum Ratings

SUP ..... -0.3V to +40V
EN ..... -0.3V to +40V
BST to LX (Note 1) ..... +6V
BST ..... -0.3V to +45V
FB ..... -0.3V to V_{BIAS} + 0.3V
SYNC ..... -0.3V to V_{BIAS} + 0.3V
SPS ..... -0.3V to V_{BIAS} + 0.3V
OUT ..... -0.3V to +18V
PGOOD ..... -0.3V to +6V
PGND to AGND ..... -0.3V to +0.3V
BIAS ..... -0.3V to +6.0V
LX Continuous RMS Current 3A
OUT Short-Circuit Duration .....
ESD Protection Human Body Model ..... ±2kV
Continuous Power Dissipation (T_A = +70°C) 12-pin SWTDFN (derate 24.4mW/°C above +70°C) 1951mW
Storage Temperature Range ..... -65ºC to +150ºC
Operating Junction Temperature (Note 6) ..... -40ºC to +150ºC
Lead Temperature (Soldering, 10s) ..... +300ºC
Soldering Temperature (Reflow) ..... +260ºC

Note 1: LX has internal clamp diodes to PGND/AGND and SUP. Applications that forward bias these diodes should take care not to exceed the IC's package power-dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12 TDFN

Package Code	TD1233+2C
Outline Number	21-0664
Land Pattern Number	90-0397
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	41°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	9°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{SUP} = V_{EN}, V_{SUP} = 14V, V_{SYNC} = 0V, V_{OUT} = 5V, T_J = -40°C to +150°C, unless otherwise noted. (Notes 2 and 5))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP}			3.5		36	V
		After Start-Up		3		36	
		t < 1s				40	
Supply Current	I_{SUP}	V_{EN} = low			1	5	µA
		MAX25232ATCB, MAX25232ATCE	No load, no switching		3.5	8	
			No load (Note 3)		4.5		
		MAX25232ATCA, MAX25232ATCD, MAX25232ATCH	No load, no switching		6	10	
			No load (Note 3)		7.5		

Electrical Characteristics (continued)

(V_{SUP} = V_{EN}, V_{SUP} = 14V, V_{SYNC} = 0V, V_{OUT} = 5V, T_J = -40°C to +150°C, unless otherwise noted. (Notes 2 and 5))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LX Leakage	$I_{LX,LEAK}$	V_{SUP} = 40V, LX = 0 or 40V, T_A = +25°C		-1		+1	µA
Undervoltage Lockout	UVLO	VBIAS rising		2.53	2.73	2.93	V
		Hysteresis			0.13		
BIAS Voltage	V_{BIAS}	5.5V ≤ V_{SUP} ≤ 36V, PWM mode			5		V
BUCK CONVERTER							
Voltage Accuracy, 5V	$V_{OUT,5V}$	MAX25232ATCA, MAX25232ATCD	Skip mode (Note 3)	4.85	4.99	5.1	
			Fixed-frequency PWM mode	4.93	5	5.07	
Voltage Accuracy, 3.3V	$V_{OUT,3.3V}$	MAX25232ATCB, MAX25232ATCE	Skip mode (Note 3)	3.2	3.3	3.37	
			Fixed-frequency PWM mode	3.25	3.3	3.35	
Voltage Accuracy, 4V	$V_{OUT,4V}$	MAX25232ATCH	Skip Mode (Note 3)	3.88	4	4.12	V
			Fixed-frequency PWM mode	3.92	4	4.08	
Output Voltage Range	V_{OUT}	MAX25232ATCF, MAX25232ATCG		3		10	V
FB Voltage Accuracy	V_{FB}	MAX25232ATCF, MAX25232ATCG		0.985	1	1.015	V
FB Current	I_{FB}	MAX25232ATCF, MAX25232ATCG	VFB = 1V, TA = +25°C		0.02		µA
FB Line Regulation		MAX25232ATCF, MAX25232ATCG	V_{SUP} = 6V to 36V		0.02		%/V
High-Side Switch On-Resistance	RON,HS	V_{BIAS} = 5V, I_{LX} = 1A			70		mΩ
Low-Side Switch On-Resistance	$R_{ON,LS}$	V_{BIAS} = 5V, I_{LX} = 1A			70		mΩ
High-Side Current-Limit Threshold	I_{LIM}	MAX25232ATCA, MAX25232ATCB, MAX25232ATCG, MAX25232ATCH		3.05	3.50	3.95	A
		MAX25232ATCD, MAX25232ATCE, MAX25232ATCF		4.10	4.70	5.60	
Low-Side Negative Current-Limit Threshold	I_{NEG}				-1.2		A
Soft-Start Ramp Time (Note 4)	I_{SS}	MAX25232ATCA, MAX25232ATCB, MAX25232ATCG, MAX25232ATCH			3.5	5	ms
		MAX25232ATCD, MAX25232ATCE, MAX25232ATCF			5.5	7.5	
Minimum On-Time	t_{ON}	(Note 3)			65		ns
Maximum Duty Cycle				98	99		%
PWM Switching Frequency	f_{SW}	MAX25232ATCA, MAX25232ATCB, MAX25232ATCG, MAX25232ATCH		1.925	2.1	2.275	MHz
		MAX25232ATCD, MAX25232ATCE, MAX25232ATCF		360	400	440	kHz
Spread-Spectrum Range	SS	V_{SPS} = 5V			±3		%

Electrical Characteristics (continued)

(V_{SUP} = V_{EN}, V_{SUP} = 14V, V_{SYNC} = 0V, V_{OUT} = 5V, T_J = -40°C to +150°C, unless otherwise noted. (Notes 2 and 5))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PGOOD							
PGOOD Threshold, Rising	$V_{THR,PGD}$	V_{OUT} rising		91	93	95	%
PGOOD Threshold, Falling	$V_{THF,PGD}$	V_{OUT} falling		90	92	94	%
PGOOD Debounce Time	t_{DEB}	MAX25232ATCA, MAX25232ATCB, MAX25232ATCG, MAX25232ATCH	PWM mode		60		µs
			Skip mode		90		
		MAX25232ATCD, MAX25232ATCE, MAX25232ATCF	PWM mode		80		
			Skip mode		110		
PGOOD High-Leakage Current	$I_{LEAK,PGD}$	T_A = +25°C				1	µA
PGOOD Low Level	$V_{OUT,PGD}$	Sinking 1mA				0.4	V
LOGIC LEVELS							
EN Level, High	$V_{IH,EN}$			2.4			V
EN Level, Low	$V_{IL,EN}$					0.6	V
EN Input Current	$I_{IN,EN}$	V_{EN} = V_{SUP} = 14V, T_A = +25°C				1	µA
External Input Clock Frequency	FSYNC	MAX25232ATCA, MAX25232ATCB, MAX25232ATCG, MAX25232ATCH		1.7		2.6	MHz
		MAX25232ATCD, MAX25232ATCE, MAX25232ATCF		325		500	kHz
SYNC Threshold, High	$V_{IH,SYNC}$			1.4			V
SYNC Threshold, Low	$V_{IL,SYNC}$					0.4	V
SYNC Internal Pulldown	$R_{PD,MODE}$				1000		kΩ
SPS Threshold, High	$V_{IH,SPS}$			1.4			V
SPS Threshold, Low	$V_{IL,SPS}$					0.4	V
SPS Internal Pulldown					1000		kΩ
THERMAL PROTECTION							
Thermal Shutdown	T_{SHDN}	(Note 3)			175		°C
Thermal-Shutdown Hysteresis	$T_{SHDN.HYS}$	(Note 3)			15		°C

Note 2: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at T_A = +25°C.

Note 3: Guaranteed by design; not production tested.

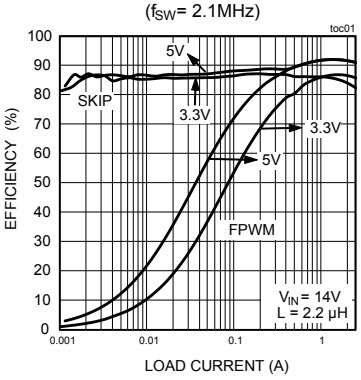
Note 4: Soft-start time is measured as the time taken from EN going high to PGOOD going high.

Note 5: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

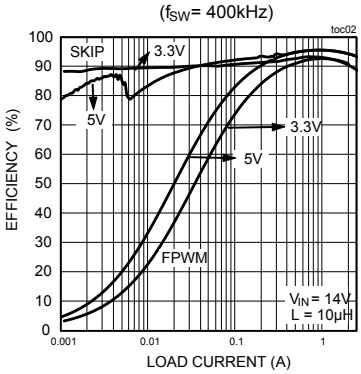
Typical Operating Characteristics

(V_{SUP} = V_{EN} = +14V, T_A = +25°C, unless otherwise noted.)

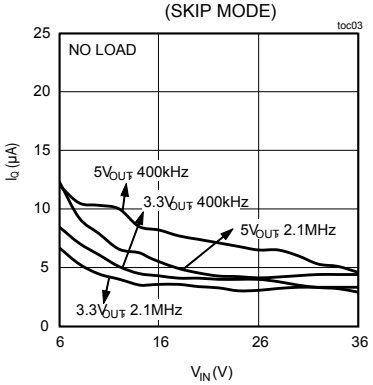
EFFICIENCY vs. LOAD
(f_{SW}= 2.1MHz)



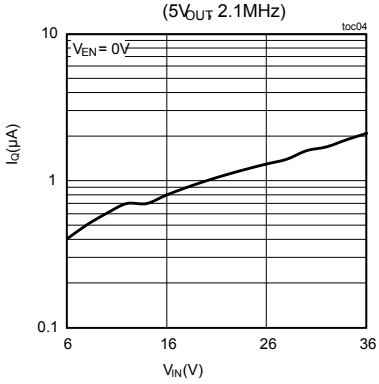
EFFICIENCY vs. LOAD
(f_{SW}= 400kHz)



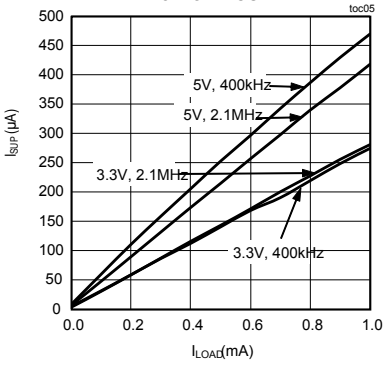
QUIESCENT SUPPLY CURRENT
vs. INPUT VOLTAGE
(SKIP MODE)



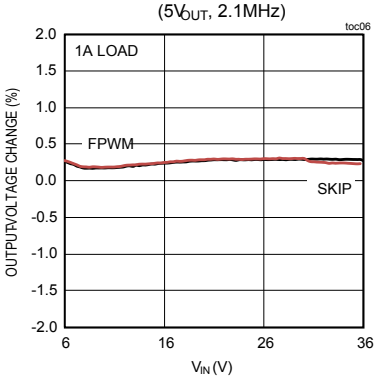
SHUTDOWN SUPPLY CURRENT
vs. INPUT VOLTAGE
(5V_{OUT}, 2.1MHz)



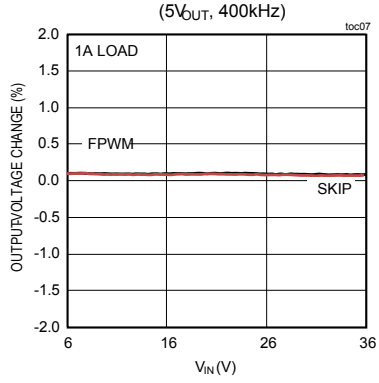
STANDBY CURRENT
vs. LOAD CURRENT



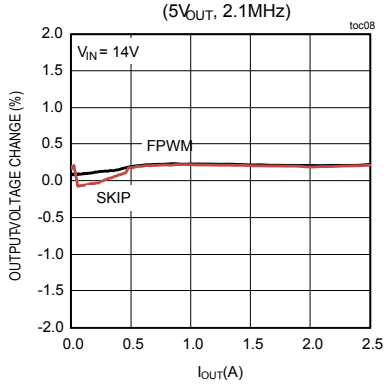
LINE REGULATION
(5V_{OUT}, 2.1MHz)



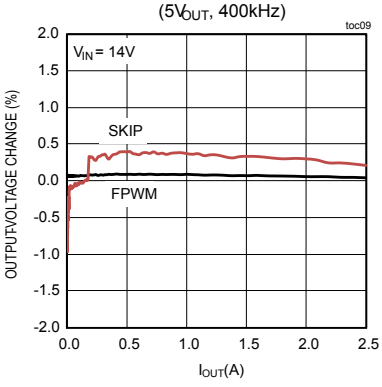
LINE REGULATION
(5V_{OUT}, 400kHz)



LOAD REGULATION
(5V_{OUT}, 2.1MHz)



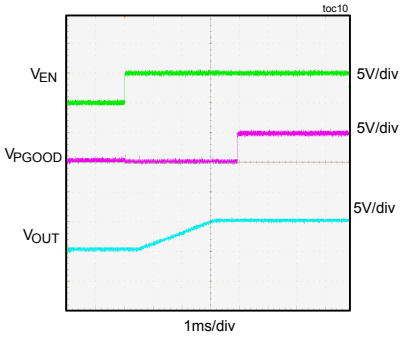
LOAD REGULATION
(5V_{OUT}, 400kHz)



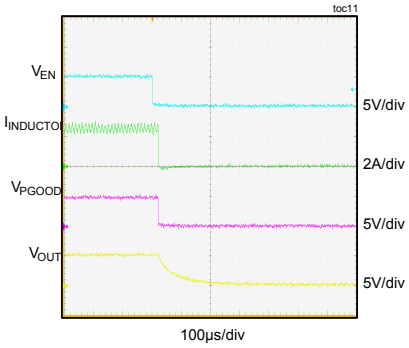
Typical Operating Characteristics (continued)

(V_{SUP} = V_{EN} = +14V, T_A = +25°C, unless otherwise noted.)

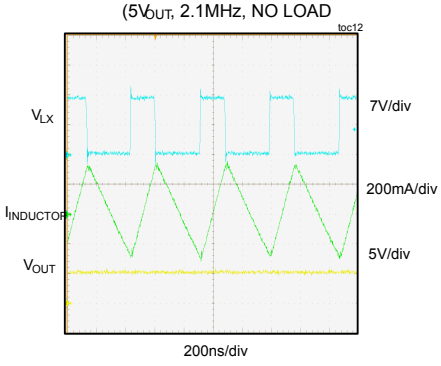
STARTUP WAVEFORM
($5V_{OUT}$, 2.1MHz)



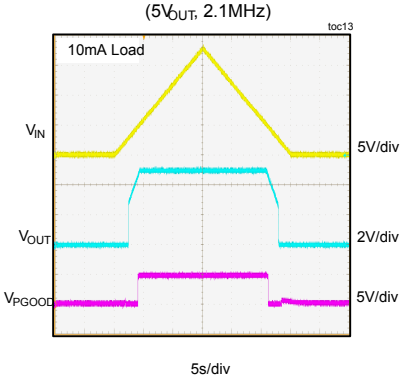
SHUTDOWN WAVEFORM
($5V_{OUT}$, 2.1MHz, 2.5A LOAD)



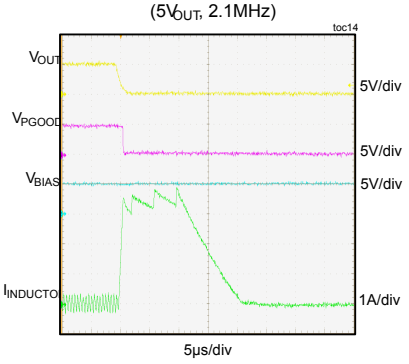
STEADY-STATE SWITCHING WAVEFORM
($5V_{OUT}$, 2.1MHz, NO LOAD



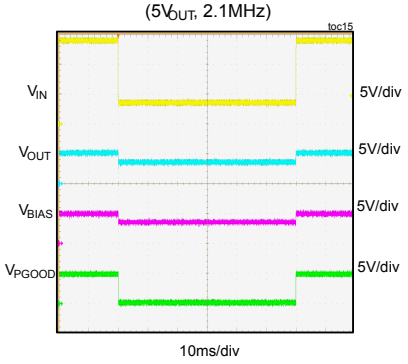
SLOW V_{IN} RAMP
($5V_{OUT}$, 2.1MHz)



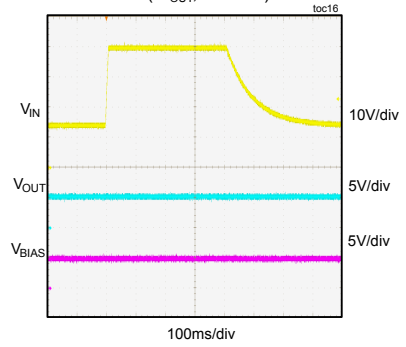
SHORT-CIRCUIT RESPONSE
($5V_{OUT}$, 2.1MHz)



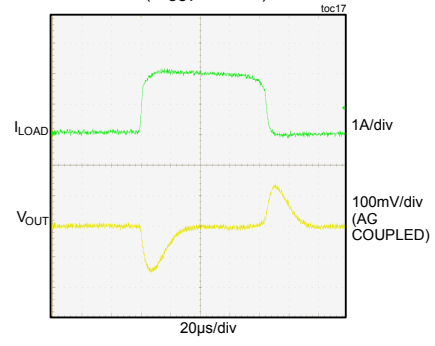
UNDERVOLTAGE PULSE
($5V_{OUT}$, 2.1MHz)



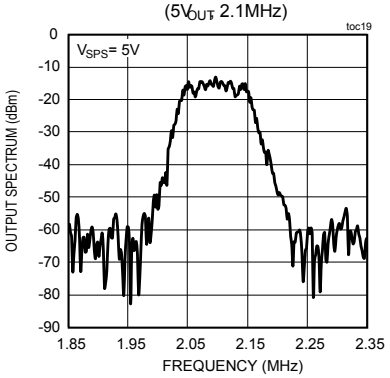
LOAD-DUMP TEST
($5V_{OUT}$, 2.1MHz)



LOAD-TRANSIENT RESPONSE
($5V_{OUT}$, 2.1MHz)

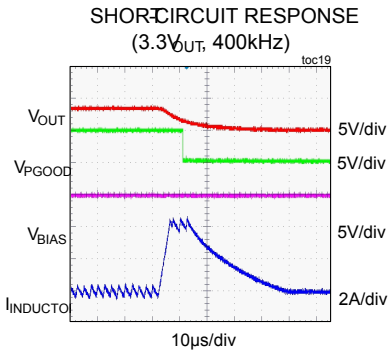


SPECTRAL ENERGY DENSITY
vs. FREQUENCY
($5V_{OUT}$, 2.1MHz)



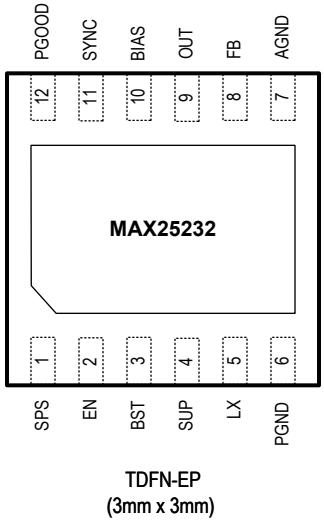
Typical Operating Characteristics (continued)

(V_{SUP} = V_{EN} = +14V, T_A = +25°C, unless otherwise noted.)



Pin Configuration

MAX25232



TDFN-EP
(3mm x 3mm)

Pin Description

PIN	NAME	FUNCTION
1	SPS	Spread-Spectrum Enable. Connect logic-high to enable spread spectrum of internal oscillator, or logic-low to disable spread spectrum. This pin has a 1MΩ internal pulldown.

Pin Description (continued)

PIN	NAME	FUNCTION
2	EN	High-Voltage-Compatible Enable Input. If this pin is low, the part is off.
3	BST	Bootstrap Pin for HS Driver. It is recommended to use 0.1µF from BST to LX.
4	SUP	Supply Input. Connect a 4.7µF ceramic capacitor from SUP to PGND.
5	LX	Buck Switching Node. Connect inductor between LX and OUT. See the Inductor Selection section. If the part is off, this node is high impedance.
6	PGND	Power Ground. Ground return path for all high-current/high-frequency noisy signals.
7	AGND	Analog Ground. Ground return path for all ‘quiet’ signals.
8	FB	Connect this pin to BIAS for fixed output voltage options. For MAX25232ATCF and MAX25232ATCG, use it as a FB pin to set the output voltage.
9	OUT	Buck Regulator Output-Voltage-Sense Input. Bypass OUT to PGND with ceramic capacitors.
10	BIAS	5V Internal Bias Supply. Connect a 1µF (min) ceramic capacitor to AGND.
11	SYNC	Sync Input. If connected to ground or open, skip-mode operation is enabled under light loads; if connected to BIAS, forced-PWM mode is enabled. This pin has a 1MΩ internal pulldown.
12	PGOOD	Open-Drain Reset Output. External pullup required.
-	EP	Exposed Pad. EP must be connected to ground plane on PCB, but is not a current-carrying path and is only needed for thermal transfer.

Detailed Description

The MAX25232 family of small, current-mode-controlled buck converters features synchronous rectification and requires no external compensation network. The devices are designed for 3A output current and can stay in dropout by running at 99% duty cycle. Each device provides an accurate output voltage of ±2% in FPWM mode within the 6V to 18V input range. Voltage quality can be monitored by observing the PGOOD signal. The devices operate at 2.1MHz (typ) frequency, which allows for small external components, reduced output ripple, and guarantees no AM band interference. The devices are also available at 400kHz (typ) for minimum switching losses and maximum efficiency.

Each device features an ultra-low 3.5µA (typ) quiescent supply current in standby mode. The device enters standby mode automatically at light loads if the high-side FET (HSFET) does not turn on for eight consecutive clock cycles. The devices operate from a 3.5V to 36V supply voltage and can tolerate transients up to 40V, making them ideal for automotive applications. The devices are available in factory-trimmed output voltages (5V, 3.3V). MAX25232ATCF and MAX25232ATCG configuration can be used to program output voltage between 3V and 10V using an external resistor-divider. For fixed-output voltages outside of 3.3V and 5V, contact factory for availability.

Enable Input (EN)

Each device is activated by driving EN high. EN is compatible from a 3.3V logic level to automotive battery levels. EN can be controlled by microcontrollers and automotive KEY or CAN inhibit signals. The EN input has no internal pullup/pulldown current to minimize the overall quiescent supply current. To realize a programmable undervoltage-lockout level, use a resistor-divider from SUP to EN to AGND.

Bias/UVLO

Each device features undervoltage lockout. When the device is enabled, an internal bias generator turns on. LX begins switching after V_{BIAS} has exceeded the internal undervoltage-lockout level, V_{UVLO} = 2.73V (typ).

Soft-Start

Each device features an internal soft-start timer. The output voltage soft-start time is 3.5ms (typ), which includes the delay in PGOOD. If a short circuit or undervoltage is encountered after the soft-start timer has expired, the device is disabled for 7ms (typ) and then reattempts soft-start again. This pattern repeats until the short circuit has been removed.

Oscillator/Synchronization and Efficiency (SYNC)

Each device has an on-chip oscillator that provides a 2.1MHz (typ) or 400kHz (typ) switching frequency. There are two operation modes, depending on the condition of SYNC. If SYNC is unconnected or at AGND, the device operates in highly efficient pulse-skipping mode. If SYNC is connected to BIAS or has a clock applied to it, the device is in forced-PWM mode (FPWM). The device can be switched during operation between FPWM mode and skip mode by switching SYNC.

Skip-Mode Operation

The devices enter skip mode when the SYNC pin is connected to ground or is unconnected and the peak load current is < 600mA (typ). In this mode, the HSFET is turned on until the inductor current ramps up to 600mA (typ) peak value and the internal feedback voltage is above the regulation voltage (1.0V, typ). At this point, both the HSFETs and low-side FETs (LSFETs) are turned off. Depending on the choice of the output capacitor and the load current, the HSFET turns on when OUT (valley) drops below the 1.0V (typ) feedback voltage. When the device is in skip mode, the internal high-voltage LDO is turned off to save current. V_{BIAS} is supplied by the output after the soft start is completed.

Achieving High Efficiency at Light Loads

Each device operates with very low-quiescent current at light loads to enhance efficiency and conserve battery life. When the device enters skip mode, the output current is monitored to adjust the quiescent current. The lowest quiescent-current standby mode is only available for factory-trimmed devices between 3.0V and 5.5V output voltages. When the output current is < approximately 5mA, the device operates in the lowest quiescent-current mode, also called standby mode. In

this mode, the majority of the internal circuitry (excluding that necessary to maintain regulation) in the device is turned off to save current. Under no load and with skip mode enabled, the device typically draws 3.5µA for the 3.3V parts, and 6µA for the 5.0V parts. For load currents > 5mA, the device enters normal skip mode and still maintains very high efficiency.

Output-Voltage Overshoot Protection

In dropout, the output voltage closely follows the input voltage, but is below the regulation point. The device runs at maximum duty cycle to satisfy the loop, and the internal error-amplifier output is railed high. When the input voltage rises above the output, the device comes out of dropout, but the internal error-amplifier output takes some time to get back to steady state. This causes an overshoot in the output voltage. To limit this overshoot, the device clamps the output of the error amplifier while coming out of dropout, causing it to discharge faster and limiting the output-voltage overshoot. The actual value of the overshoot depends on the output capacitor, inductor, and load.

Controlled EMI with Forced-Fixed Frequency

In FPWM mode, the device attempts to operate at a constant switching frequency for all load currents. For tightest frequency control, apply the operating frequency to SYNC. The advantage of FPWM is a constant switching frequency, which improves EMI performance; the disadvantage is that considerable current can be thrown away. If the load current during a switching cycle is less than the current flowing through the inductor, the excess current is diverted to AGND.

Extended Input Voltage Range

In some cases, the device is forced to deviate from its operating frequency, independent of the state of SYNC. At high input voltages above 18V (especially for 2.1MHz operation), the required on-time to regulate its output voltage may be smaller than the minimum on-time (65ns, typ). In this event, the device is forced to lower its switching frequency by skipping pulses. If the input voltage is reduced and the device approaches dropout, it continuously tries to turn on the HSFET. To maintain gate charge on the HSFET, the BST capacitor must be periodically recharged. To ensure proper charge on the BST capacitor when in dropout, the HSFET is turned off every 20µs and the LSFET is turned on for approximately 200ns. This gives an effective duty cycle of > 99%, and a switching frequency of 50kHz when in dropout.

Spread-Spectrum Option

Each device has an optional spread spectrum enabled by the SPS pin. If SPS is pulled high, the internal operating frequency varies by ±3% relative to the internally generated 2.1MHz (typ) operating frequency. Spread spectrum is offered to improve EMI performance of the device. The internal spread spectrum does not interfere with the external clock applied on the SYNC pin. It is active only when the device is running with an internally generated switching frequency.

Power-Good (PGOOD)

Each device features an open-drain power-good output. PGOOD is an active-high output that pulls low when the output voltage is below 92% (typ) of its nominal value. PGOOD is high impedance when the output voltage is above 93% (typ) of its nominal value. Connect a 20kΩ (typ) pullup resistor to an external supply, or to the on-chip BIAS output.

Overcurrent Protection

Each device limits the peak output current to 3.5A (typ) for 2.1MHz switching frequency parts and 4.7A (typ) for the 400kHz switching frequency parts. The accuracy of the current limit is ±12%, making selection of external components very easy. To protect against short-circuit events, the device shuts off when OUT is below 50% of V_{OUT} and an overcurrent event is detected. The device attempts a soft-start restart every 7ms and stays off if the short circuit has not been removed. When the current limit is no longer present, it reaches the output voltage by following the normal soft-start sequence. If the device's die reaches the thermal limit of 175°C (typ) during the current-limit event, it immediately shuts off.

Thermal-Overload Protection

Each device features thermal-overload protection. The device turns off when the junction temperature exceeds +175°C (typ). Once the device cools by 15°C (typ), it turns back on with a soft-start sequence.

Applications Information

Setting the Output Voltage

MAX25232 comes with fixed V_{OUT} options (set internally) of 5V and 3.3V. For setting the output voltage between 3V - 10V externally using resistor-dividers, chose MAX25232ATCF and MAX25232ATCG. Connect a resistor-divider from output (OUT) to FB to AGND (see Figure 1). Select R_{FB2} (FB to AGND resistor) ≤ 500kΩ. Calculate R_{FB1} (OUT to FB resistor) with the following equation:

$$R_{FB1} = R_{FB2}\left[\left[\frac{V_{OUT}}{V_{FB}}\right] - 1\right]$$

where V_{FB} = 1V (see *Electrical Characteristics*).

Other fixed-output voltage options (set internally) between 3V - 5.5V in 50mV steps are also available. Contact the factory if your application requires fixed output voltage in this range.

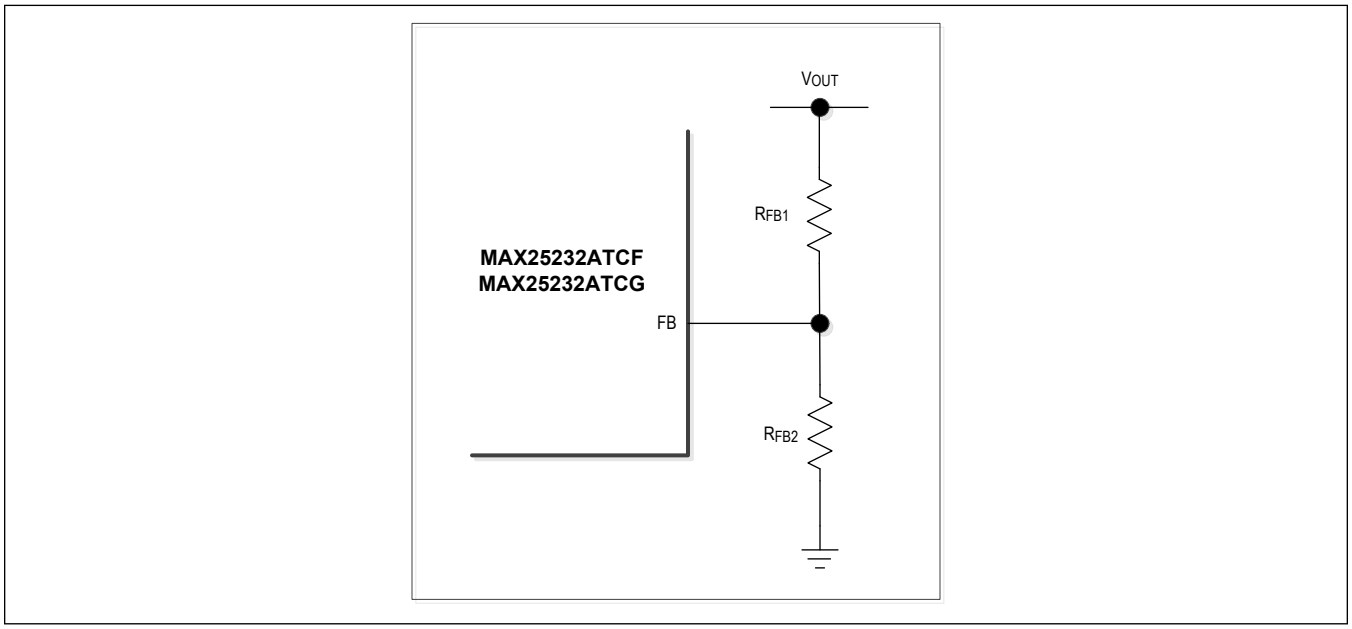


Figure 1. Setting the Output Voltage with External Resistor-Dividers

Input Capacitor

A 4.7µF low-ESR ceramic input capacitor is recommended for proper device operation. This value can be adjusted based on application input-voltage-ripple requirements.

The discontinuous input current of the buck converter causes large input-ripple current. Switching frequency, peak inductor current, and the allowable peak-to-peak input-voltage ripple dictate the input-capacitance requirement. Increasing the switching frequency or the inductor value lowers the peak-to-average current ratio, yielding a lower input-capacitance requirement. The input ripple is mainly comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the input capacitor). The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR}. Assume that input-voltage ripple from the ESR and the capacitor discharge is equal to 50% each. The following equations show the ESR and capacitor requirement for a target voltage ripple at the input:

Equation 1:

$$ESR = \frac{\Delta V_{ESR}}{I_{OUT} + (\Delta I_{P-P} / 2)}$$

$$C_{IN} = \frac{I_{OUT} \times D(1 - D)}{\Delta V_Q \times \times f_{SW}}$$

where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

and:

$$D = \frac{V_{OUT}}{V_{IN}}$$

where I_{OUT} is the output current, D is the duty cycle, and f_{SW} is the switching frequency. Use additional input capacitance at lower input voltages to avoid possible undershoot below the UVLO threshold during transient loading.

Inductor Selection

See *Table 1* for inductor selection. The nominal standard value selected should be within ±50% of the specified inductance. The specified values applies to all output voltage settings.

Table 1. Inductor Selection

PART	INDUCTANCE (µH)
For f_{SW} = 2.1MHz	2.2
For f_{SW} = 400kHz	10

Output Capacitor

For optimal phase margin (> 60 degrees, typ), the recommended output capacitances are shown in *Table 2*. Recommended values are the actual capacitances after voltage derating is taken into account.

If a lower output capacitance is required, contact the factory for recommendations. Additional output capacitance may be needed based on application-specific output-voltage-ripple requirements. The specified values applies to all output voltage settings.

Table 2. Output-Capacitance Selection

PART	OUTPUT CAPACITANCE (µF)
For f_{SW} = 2.1MHz	30
For f_{SW} = 400kHz	44

The allowable output-voltage ripple and the maximum deviation of the output voltage during step-load currents determine the output capacitance and its ESR. The output ripple comprises ΔV_Q (caused by the capacitor discharge) and ΔVESR (caused by the ESR of the output capacitor). Use low-ESR ceramic or aluminum electrolytic capacitors at the output. For aluminum electrolytic capacitors, the entire output ripple is contributed by ΔV_{ESR}. Use Equation 2 to calculate the ESR requirement and choose the capacitor accordingly. If using ceramic capacitors, assume the contribution to the output ripple voltage from the ESR and the capacitor discharge to be equal. The following equations show the output capacitance and ESR requirement for a specified output-voltage ripple.

Equation 2:

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_{P-P}}$$

$$C_{OUT} = \frac{\Delta I_{P-P}}{8 \times \Delta V_Q \times f_{SW}}$$

where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

and:

$$V_{OUT\_RIPPLE} = \Delta V_{ESR} + \Delta V_Q$$

ΔI_{P-P} is the peak-to-peak inductor current as calculated above, and f_{SW} is the converter's switching frequency. The allowable deviation of the output voltage during fast transient loads also determines the output capacitance and its ESR. The output capacitor supplies the step-load current until the converter responds with a greater duty cycle. The resistive drop across the output capacitor's ESR and the capacitor discharge causes a voltage droop during a step load. Use a combination of low-ESR tantalum and ceramic capacitors for better transient-load and ripple/noise performance. Keep the maximum output-voltage deviations below the tolerable limits of the electronics being powered. When using a ceramic capacitor, assume an 80% and 20% contribution from the output-capacitance discharge and the ESR drop, respectively. Use the following equations to calculate the required ESR and capacitance value:

Equation 3:

$$ESR_{OUT} = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$C_{OUT} \geq I_{STEP}^2 \times \frac{L}{2 \times (V_{SUP} - V_{OUT}) \times DMAX \times \Delta V_Q}$$

$$+ I_{STEP} \times \frac{t_{DELAY}}{\Delta V_Q}$$

where I_{STEP} is the load step and t_{DELAY} is the delay for the PWM mode, the worst-case delay would be (1-D) t_{SW} when the load step occurs right after a turn-on cycle. This delay is higher in skip mode.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching power losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity. Follow the guidelines below for a good PCB layout:

1. Place the input capacitor (C_{IN}) close to the device to reduce the input AC-current loop. AC current flows on the loop formed by the input capacitor and the half-bridge MOSFETs internal to the device (see Figure 2). A small loop would reduce the radiating effect of high switching currents and improve EMI functionality.
2. Solder the exposed pad to a large copper-plane area under the device. To effectively use this copper area as heat exchanger between the PCB and ambient, expose the copper area on the top and bottom side. Add a few small vias or one large via on the copper pad for efficient heat transfer.
3. Connect PGND and AGND pins directly to the exposed pad under the IC. This ensures the shortest connection path between AGND and PGND.
4. Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCB to enhance full-load efficiency and power-dissipation capability.
5. Using internal PCB layers as ground plane helps to improve the EMI functionality as ground planes act as a shield against radiated noise. Have multiple vias spread around the board, especially near the ground connections to have better overall ground connection.
6. Keep the bias capacitor (C_{BIAS}) close to the device to reduce the bias current loop. This helps to reduce noise on the bias for smoother operation.

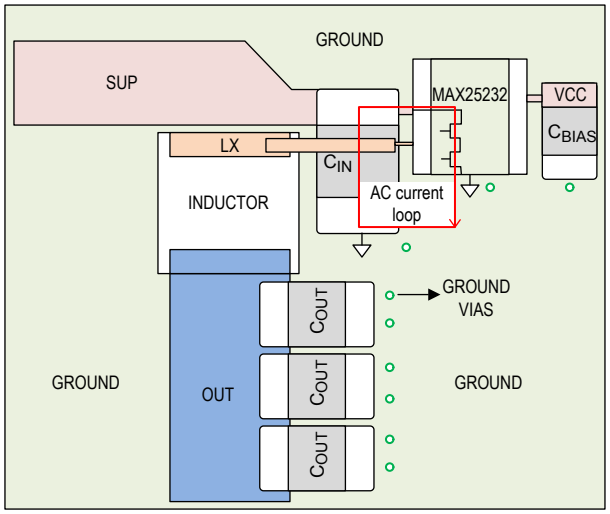


Figure 2. Recommended PCB Layout for MAX25232

Typical Application Circuits

Circuit 1

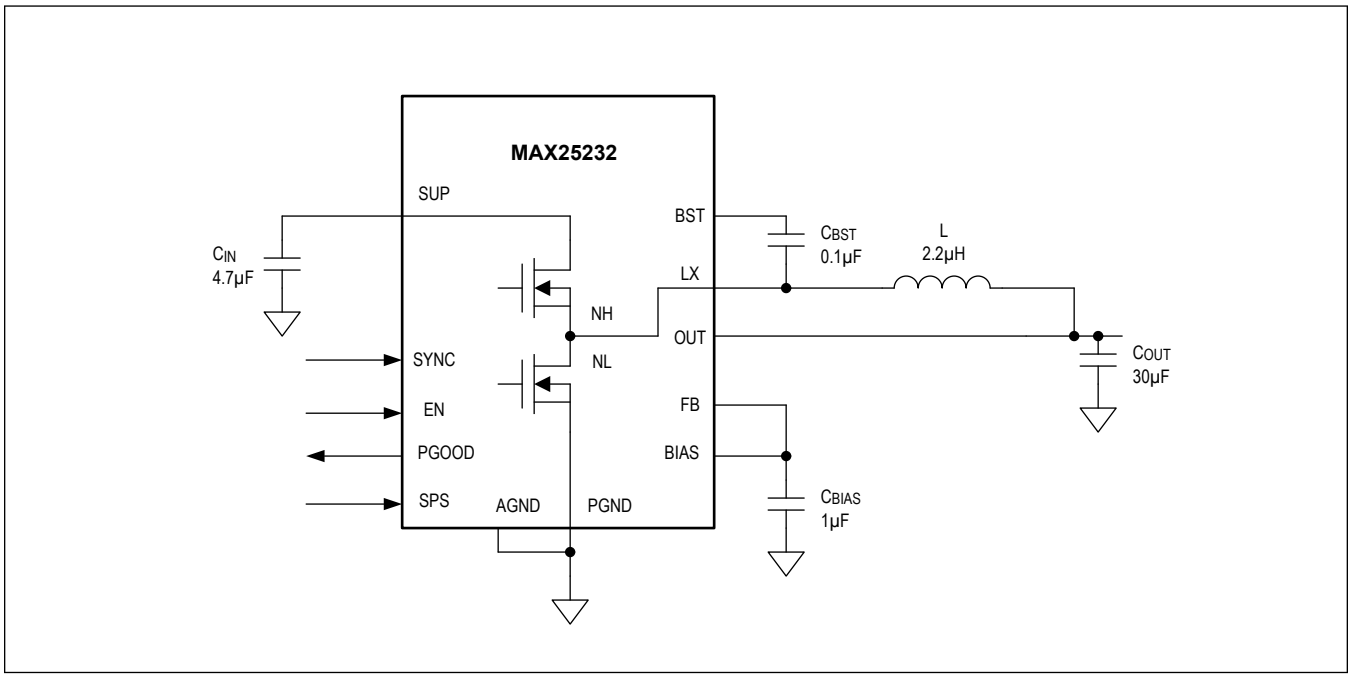


Figure 3. 2.1MHz, 5V/3.3V Fixed Output Voltage Configuration in 12-Pin TDFN Package

Typical Application Circuits (continued)

Circuit 2

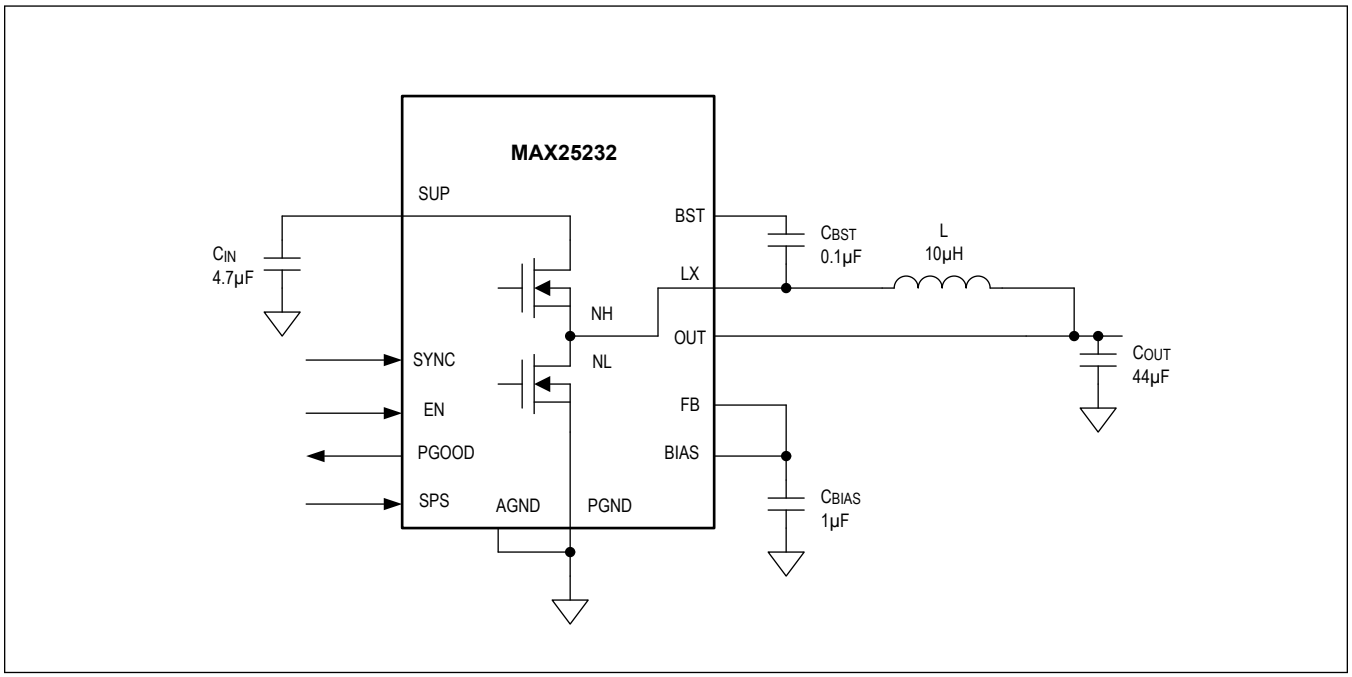


Figure 4. 400kHz, 5V/3.3V Fixed Output Voltage Configuration in 12-Pin TDFN Package

Typical Application Circuits (continued)

Circuit 3

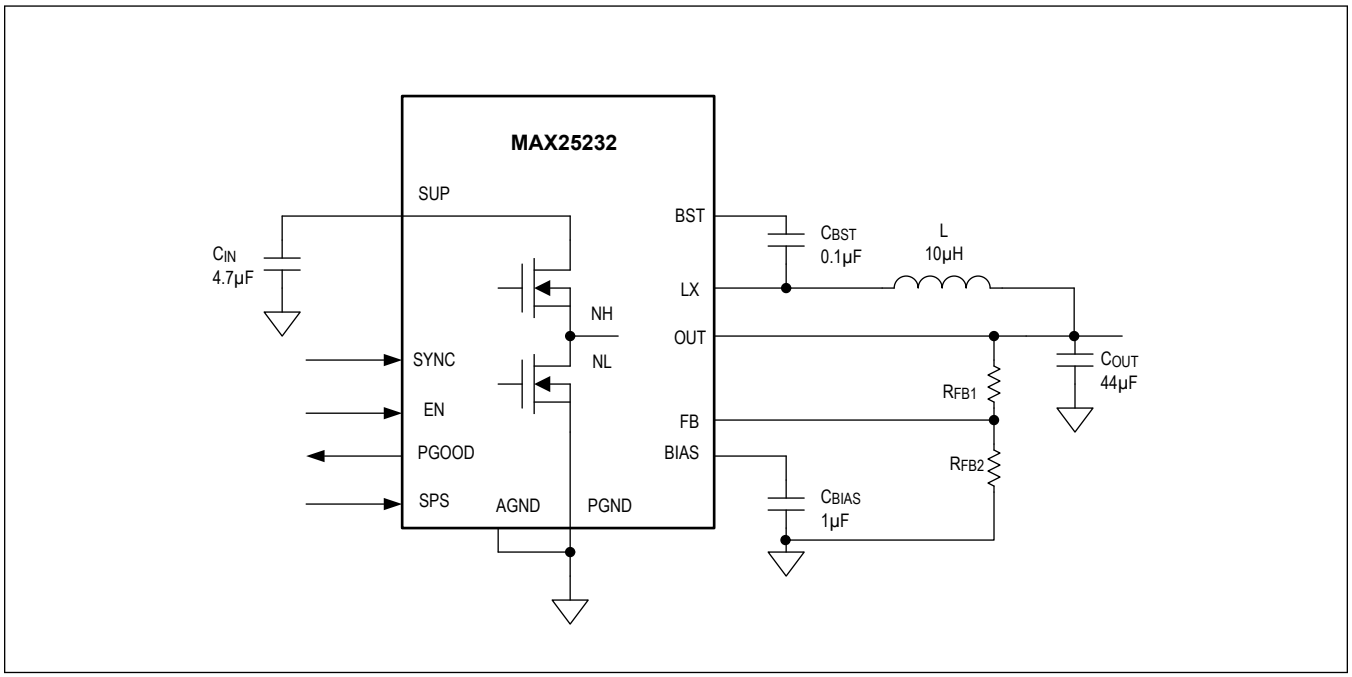


Figure 5. 400kHz, External Resistor-Divider Configuration in 12-Pin TDFN Package

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	DESCRIPTION	I_{OUT} (A)
MAX25232ATCA/V+	-40°C to +125°C	12 TDFN	2.1MHz, Fixed 5V output	2.5
MAX25232ATCB/V+	-40°C to +125°C	12 TDFN	2.1MHz, Fixed 3.3V output	2.5
MAX25232ATCD/V+	-40°C to +125°C	12 TDFN	400kHz, Fixed 5V output	3
MAX25232ATCE/V+	-40°C to +125°C	12 TDFN	400kHz, Fixed 3.3V output	3
MAX25232ATCF/V+	-40°C to +125°C	12 TDFN	400kHz, Adjustable Output Voltage Between 3V and 10V	3
MAX25232ATCG/V+	-40°C to +125°C	12 TDFN	2.1MHz, Adjustable Output Voltage Between 3V and 10V	2.5
MAX25232ATCH/V+	-40°C to +125°C	12 TDFN	2.1MHz, Fixed 4V output	2.5

Note: All parts are OTP versions, no metal mask differences.

/V Denotes an automotive-qualified part.

+ Denotes a lead(Pb)-free/RoHS-compliant package

** Future product - contact factory for availability*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/20	Initial release	—
1	10/20	Updated *Benefits and Features*, *Electrical Characteristics*, *Pin Configuration*, *Pin Description*, *Applications Information*, and *Ordering Information*	1, 4, 5, 9, 10, 14, 20
2	3/21	Updated *Absolute Maximum Ratings*, *Electrical Characteristics*, and *Ordering Information*	3, 4, 19
3	4/02	Updated Pin Configurations, Pin Description, Typical Application Circuits	8, 9, 17, 18

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