MAX25203

Dual-Phase Synchronous Boost Controller with Programmable Gate Drive and I²C

General Description

The MAX25203 automotive dual-phase synchronous boost controller enables infotainment systems to stay in regulation during cold-crank or start-stop operation all the way down to a battery input of 1.8V. It can also be used to generate backlight voltage and Class D audio amplifier voltages. This device can start with an input voltage supply from 4.5V to 42V and can operate down to 1.8V after start-up, and has a low 5µA shutdown supply current.

The MAX25203 operates at up to 2.1MHz frequency to allow small external components and reduced output ripple, and to guarantee no AM band interference. The switching frequency is resistor adjustable (220kHz to 2100kHz) or it can be synchronized on-the-fly to an external clock.

The MAX25203 has a spread-spectrum option for frequency modulation to minimize EMI interference. A 90° out-of-phase clock output enables synchronizing a second MAX25203 for quad-phase operation.

Pass-through operation has over 98% efficiency when the supply voltage exceeds the output regulation voltage. Programmable current-limit blanking handles high peak loads without oversizing the inductor.

The MAX25203 features a power-OK monitor and undervoltage lockout. Protection features include cycle-by-cycle current limit and thermal shutdown. It operates over the -40°C to +125°C automotive temperature range.

Applications

- Infotainment Systems
- Automotive Audio Amplifier

Benefits and Features

- Meets Stringent OEM Module Power Consumption and Performance Specifications
  - ±1.5% Output-Voltage Accuracy at FB
  - Output Voltage Adjustable Between 12V and 65V (70V Abs Max)
  - 5µA Shutdown Supply Current
- High Efficiency and Current Sharing
  - Pass-Through for >98% Efficiency
  - OTP Gate Drive Voltage from 6.5V to 10V Allows User to Optimize External MOSFETs and Improve Efficiency
  - Current Sharing Accuracy of ±5% Between Phases to Improve System Efficiency
  - Programmable Current-Limit Blanking Handles High Peak Loads without Oversizing Inductor
- EMI-Reduction Features Reduce Interference with Sensitive Radio Bands without Sacrificing Wide Input Voltage Range
  - Spread-Spectrum Option
  - On-the-Fly Frequency-Synchronization Input
  - Resistor-Programmable Frequency between 220kHz and 2.1MHz
  - Synchronization Output Provides 90° Out-of-Phase Clock for Quad-Phase Operation
- Integration and Thermally Enhanced Package Saves Board Space and Cost
  - Current-Mode Controllers with Forced-Continuous and Skip Modes
  - Side-Wettable, 32-Pin TQFN-EP Package
- Protection Features and I²C Diagnostics for Improved System Reliability
  - Supply Undervoltage Lockout
  - Die Temperature Monitoring through I²C
  - Short-Circuit Protection with True Shutdown™
  - Individual Phase Current Monitoring through I²C

***Ordering Information* appears at end of data sheet.**

19-101004; Rev 1; 8/21

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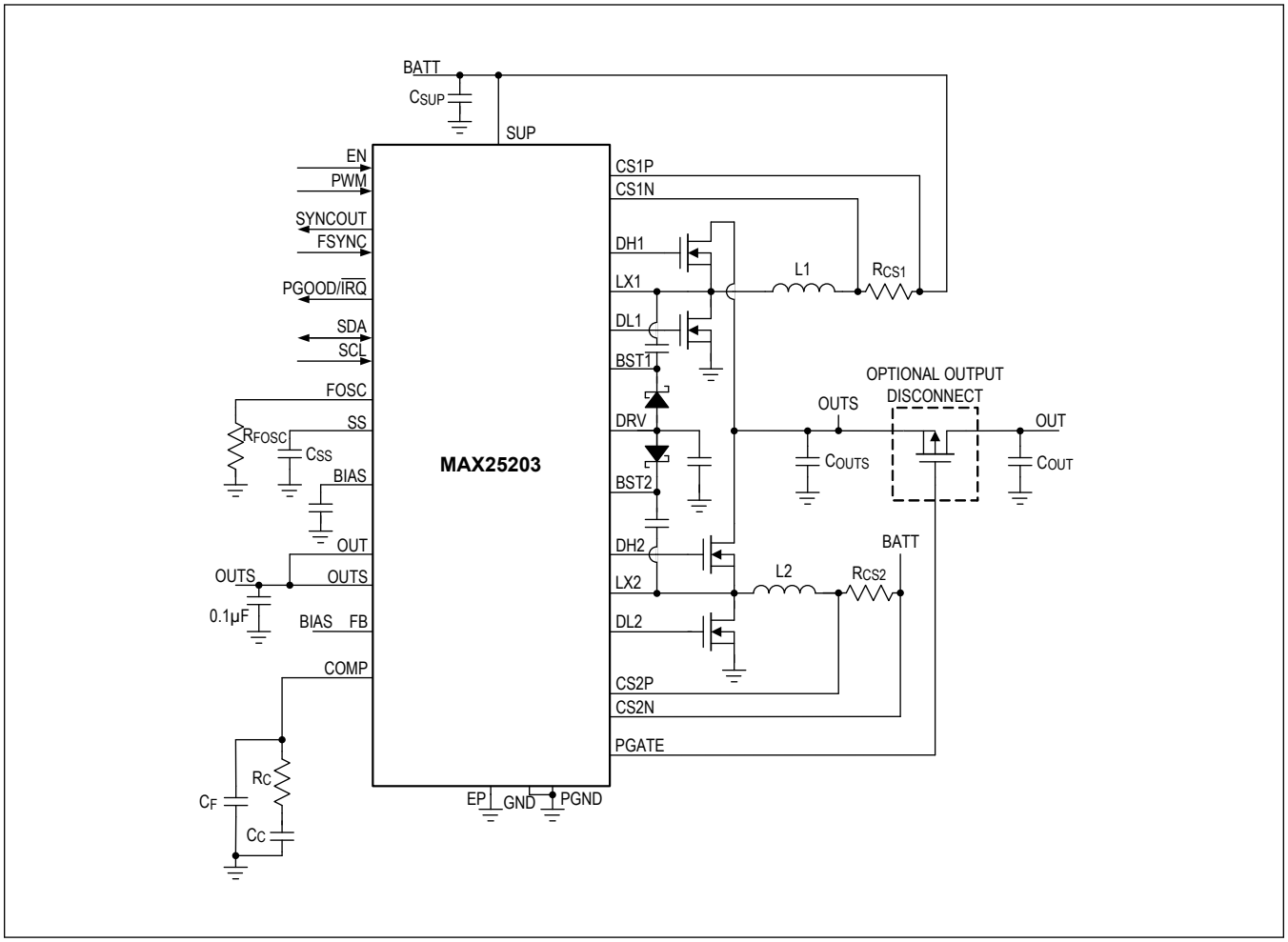
Simplified Block Diagram



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Absolute Maximum Ratings

SUP, CS_P, EN to GND ..... -0.3V to 42V
OUT, OUTS, LX_ to GND ..... -0.3V to 70V
PGATE to OUTS ..... -0.3V to 6V
CS_P to CS_N ..... -0.3V to 0.3V
BIAS, FOSC, PWM, SDA, SCL, PGOOD, SS, FB to GND ..-0.3V to 6V
SYNCOUT, FSYNC, COMP to GND ..... -0.3V to BIAS + 0.3V
BST_ to LX_ ..... -0.3V to 12V
DH_ to LX_ ..... -0.3V to BST_ + 0.3V
DRV to GND ..... -0.3V to 12V
DL_ to PGND ..... -0.3V to DRV + 0.3V
PGND to GND ..... -0.3V to 0.3V

Package Thermal Characteristics
T3255Y+4C
Continuous Power Dissipation
TQFN (derate 34.5mW/°C (*Note 1*) above +70°C) 2758.6mW
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1.7°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 29°C/W
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C
Lead Temperature (soldering, 10s) ..... +300°C
ESD Rating Human Body Model 2.5kV
ESD Rating Charged Device Model 1000V

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal consideration see *www.maxim-ic.com/thermal-tutorial*.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Ambient Temperature Range			-40 to +125	°C

Note: These limits are not guaranteed.

Package Information

SW-TQFN

Package Code	T3255Y+4C
Outline Number	21-100214
Land Pattern Number	90-100082
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	29°C/W
Junction to Case (θ_{JC})	1.7°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{SUP} = 14V, V_{EN} = 14V, V_{DRV} = 10V (MAX25203ATJA), 6.5V (MAX25203BATJA), C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, T_J = -40°C to +150°C, unless otherwise noted (*Note 2*, *Note 3*), typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNCHRONOUS STEP-UP CONTROLLER						
Supply Voltage Range	V_{SUP}	Initial startup, V_{SUP} voltage	4.5		36	V
		Bootstrap mode after initial startup condition is satisfied, V_{BAT} voltage	1.8		36	
Output Overvoltage Threshold		Detected with respect to V_{FB} rising	104	108	111	%
Supply Current	I_{SUP}	V_{EN} = V_{SUP}, V_{SUP} > V_{OUT}, no load (not including the FB divider current)		600		µA
		V_{EN} = 0V, shutdown (not including FB divider current)		5	10	
Output Voltage Adjustable Range			3.5		65	V
Regulated Feedback Voltage	V_{FB}	T_A = -40°C to +125°C	0.987	1	1.012	V
Feedback Leakage Current	I_{FB}	T_A = +25°C		0.01	0.5	µA
Feedback Line Regulation Error		V_{IN} = 3.5V to 36V, V_{FB} = 1V		0.01		%/V
Transconductance (from FB to COMP)	gm_boost	V_{FB} = 1V, V_{BIAS} = 5V (*Note 2*)	170	260	370	µS
Dead Time		DL low to DH rising		40		ns
		DH low to DL rising		30		
DH and DL Rise Time		C_{LOAD} = 3nF		20		ns
DH and DL Fall Time		C_{LOAD} = 3nF		10		ns
Minimum Off Time	t_{OFFBST}	MAX25203ATJA		200		ns
		MAX25203BATJA/VY+		85		
Switching Frequency Range	f_{SW}	Forced-PWM, resistor programmable	0.22		2.1	MHz
Switching Frequency Accuracy		R_{FOSC} = 17.5kΩ, V_{BIAS} = 5V, 3.8V	360	400	440	kHz
CS Current-Limit Voltage Threshold	V_{LIMIT}	Averaged $V_{CSP\_}$ - $V_{CSN\_}$; V_{BIAS} = 5V, V_{BATT} > 2.5V	40	50	60	mV
Current Sharing Accuracy		$V_{CSP\_}$ - $V_{CSN\_}$ > 25mV, t_{ON} > 300ns	-5		5	%
Cycle-by-Cycle CS Current-Limit Voltage Threshold	V_{LIMIT2}	Peak $V_{CSP\_}$ - $V_{CSN\_}$; V_{BIAS} = 5V, V_{BATT} > 2.5V		90		mV
Soft-Start Current	I_{SS}		8	10	12	µA
LX Leakage Current		$V_{LX\_}$ = V_{PGND} or V_{SUP}, T_A = +25°C		0.001	5	µA
PGOOD Threshold	PGOOD_H	% of FB, rising	93	95	97	%
	PGOOD_F	% of FB, falling	91	93	95	
PGOOD Leakage Current		V_{PGOOD} = 5V, T_A = +25°C			1	µA

Electrical Characteristics (continued)

(V_{SUP} = 14V, V_{EN} = 14V, V_{DRV} = 10V (MAX25203ATJA), 6.5V (MAX25203BATJA), C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, T_J = -40°C to +150°C, unless otherwise noted (*Note 2*, *Note 3*), typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PGOOD Output Low Voltage		I_{SINK} = 1mA			0.2	V
PGOOD Debounce Time		Fault detection, rising and falling		150		µs
PGOOD Timeout		Output in regulation to PGOOD high		1		ms
FSYNC INPUT						
FSYNC Input Frequency Range		Minimum sync pulse of 100ns, f_{OSC} = 2.1MHz	1.8		2.6	MHz
		Minimum sync pulse of 100ns, f_{OSC} = 400kHz	250		550	kHz
FSYNC Switching Thresholds		High threshold	1.4			V
		Low threshold			0.4	
INTERNAL LDO BIAS						
Internal BIAS Voltage		V_{IN} > 6V		5		V
BIAS UVLO Threshold		V_{BIAS} rising			4.5	V
		V_{BIAS} falling	3	3.3		
BIAS Current Capability		V_{BIAS} = 5V	10			mA
GATE DRIVE LDO						
DRV Voltage Options		Factory programmable		6.5		V
		Factory programmable		8		
		Factory programmable		10		
DRV Output Voltage	V_{DRV}	MAX25203ATJA, V_{SUP} = 14V, I_{DRV} = 1mA	9.6	10	10.3	V
		MAX25203BATJA, V_{SUP} = 14V, I_{DRV} = 150mA	6	6.5	7	
DRV Dropout Voltage		V_{SUP} = 6V, I_{DRV} = 100mA			1	V
UVLO Threshold		DRV rising			4.5	V
Hysteresis				0.85		V
PGATE DRIVER						
PGATE Turn-On Time		From turn-on to 500mA current		15		µs
PGATE Turn-Off Time		From turn-off to less than 1mA		0.1		ms
PGATE VGS Drive Voltage		V_{BIAS} > 4V		5		V
PWM VOLTAGE POSITIONING						
PWM Switching Threshold		Low threshold			0.4	V
PWM Switching Thresholds		High threshold	1.4			V
PWM Input Frequency Range		Minimum PWM pulse of 100ns	200		800	kHz

Electrical Characteristics (continued)

(V_{SUP} = 14V, V_{EN} = 14V, V_{DRV} = 10V (MAX25203ATJA), 6.5V (MAX25203BATJA), C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, T_J = -40°C to +150°C, unless otherwise noted (*Note 2*, *Note 3*), typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C-COMPATIBLE INTERFACE TIMING CHARACTERISTICS (SCL, SDA)						
SCL Clock Frequency	f_{SCL}		0		400	kHz
Bus-Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time for a Repeated START	$t_{HD;STA}$		0.6			µs
SCL Pulse Width Low	t_{LOW}		1.3			µs
SCL Pulse Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU;STA}$		0.6			µs
Data Hold Time	$t_{HD;DAT}$		0			ns
Data Setup Time	$t_{SU;DAT}$		100			ns
Data Valid Time	$t_{VD,DAT}$				900	ns
SDA and SCL Receiving Rise Time	t_R	Incoming signals (from master)	20 + CB/10		300	ns
SDA and SCL Receiving Fall Time	t_F	Incoming signals (from master)	20 + CB/10		300	ns
SDA Transmitting Fall Time	t_F		20 + CB/10		250	ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.6			µs
Bus Capacitance Allowed	C_B	2.5V ≤ V_{DDIO} ≤ 5.5V	0		900	pF
Pulse Width of a Suppressed Spike		Width of spikes that must be suppressed by the input filter of both the SDA and SCL signals		50		ns
Input High Voltage	V_{IH}		1.2			V
Input Low Voltage	V_{IL}				0.5	V
Output Low Voltage	V_{OL}	I_{SINK} = 4mA			0.2	V
THERMAL OVERLOAD						
Thermal Shutdown Temperature				170		°C
Thermal Shutdown Hysteresis				20		°C
EN LOGIC INPUT						
High Threshold		EN	1.8			V
Low Threshold		EN			0.8	V
EN Input Bias Current		EN logic inputs only, T_A = +25°C		0.01	1	µA
SPREAD SPECTRUM						
Spread Spectrum		SPS_EN = 0b1; SPS_RANGE = 0b1		f_{OSC} ± 6%		

Electrical Characteristics—MAX25203Q

(V_{SUP} = 14V, V_{EN} = 14V, V_{DRV} = 10V, C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, T_J = -40°C to +150°C, unless otherwise noted (*Note 2*, *Note 3*), typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNCHRONOUS STEP-UP CONTROLLER						
Supply Voltage Range	V_{SUP}	Initial startup, V_{SUP} voltage	4.5		36	V
		Bootstrap mode after initial startup condition is satisfied, V_{BAT} voltage	1.8		36	
Supply Current	I_{SUP}	V_{EN} = 0V, shutdown (not including FB divider current)		5	10	µA
Dead Time		DL low to DH rising		40		ns
		DH low to DL rising		30		
DH and DL Rise Time		C_{LOAD} = 3nF		20		ns
DH and DL Fall Time		C_{LOAD} = 3nF		10		ns
Minimum Off-Time	t_{OFFBST}			200		ns
CS Current-Limit Voltage Threshold	V_{LIMIT}	Averaged $V_{CSP\_}$ - $V_{CSN\_}$; V_{BIAS} = 5V, V_{BATT} > 2.5V	40	50	60	mV
Current Sharing Accuracy		$V_{CSP\_}$ - $V_{CSN\_}$ > 25mV, t_{ON} > 300ns	-5		5	%
Cycle-by-Cycle CS Current Limit Voltage Threshold	V_{LIMIT2}	Peak $V_{CSP\_}$ -$V_{CSN\_}$; V_{BIAS} = 5V, V_{BATT} > 2.5V		90		mV
LX Leakage Current		$V_{LX\_}$ = V_{PGND} or V_{SUP}, T_A = +25°C		0.001	5	µA
FSYNC INPUT						
FSYNC Input Frequency Range		Minimum sync pulse of 100ns, f_{OSC} = 2.1MHz	1.8		2.6	MHz
		Minimum sync pulse of 100ns, f_{OSC} = 400kHz	250		550	kHz
FSYNC Switching Thresholds		High threshold	1.4			V
		Low threshold			0.4	
INTERNAL LDO BIAS						
Internal BIAS Voltage		V_{IN} > 6V		5		V
BIAS UVLO Threshold		V_{BIAS} rising			4.5	V
		V_{BIAS} falling	3	3.3		
BIAS Current Capability		V_{BIAS} = 5V	10			mA
GATE DRIVE LDO						
DRV Voltage Options		Factory programmable		6.5		V
		Factory programmable		8		
		Factory programmable		10		
DRV Output Voltage	V_{DRV}	V_{SUP} = 14V, I_{DRV} = 1mA	9.6	10	10.3	V
DRV Dropout Voltage		V_{SUP} = 6V, I_{DRV} = 100mA			1	V
UVLO Threshold		DRV rising			4.5	V
Hysteresis				0.85		V
I²C-COMPATIBLE INTERFACE TIMING CHARACTERISTICS (SCL, SDA)						
SCL Clock Frequency	f_{SCL}		0		400	kHz

Electrical Characteristics—MAX25203Q (continued)

(V_{SUP} = 14V, V_{EN} = 14V, V_{DRV} = 10V, C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, T_J = -40°C to +150°C, unless otherwise noted (*Note 2*, *Note 3*), typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bus-Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time for a Repeated START	$t_{HD;STA}$		0.6			µs
SCL Pulse Width Low	t_{LOW}		1.3			µs
SCL Pulse Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU;STA}$		0.6			µs
Data Hold Time	$t_{HD;DAT}$		0			ns
Data Setup Time	$t_{SU;DAT}$		100			ns
Data Valid Time	$t_{VD;DAT}$				900	ns
SDA and SCL Receiving Rise Time	t_R	Incoming signals (from master)	20 + CB/10		300	ns
SDA and SCL Receiving Fall Time	t_F	Incoming signals (from master)	20 + CB/10		300	ns
SDA Transmitting Fall Time	t_F		20 + CB/10		250	ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.6			µs
Bus Capacitance Allowed	C_B	2.5V ≤ V_{DDIO} ≤ 5.5V	0		900	pF
Pulse Width of a Suppressed Spike		Width of spikes that must be suppressed by the input filter of both the SDA and SCL signals		50		ns
Input High Voltage	V_{IH}		1.2			V
Input Low Voltage	V_{IL}				0.5	V
Output Low Voltage	V_{OL}	I_{SINK} = 4mA			0.2	V
THERMAL OVERLOAD						
Thermal Shutdown Temperature				170		°C
Thermal Shutdown Hysteresis				20		°C
EN LOGIC INPUT						
High Threshold		EN	1.8			V
Low Threshold		EN			0.8	V
EN Input Bias Current		EN logic inputs only, T_A = +25°C		0.01	1	µA

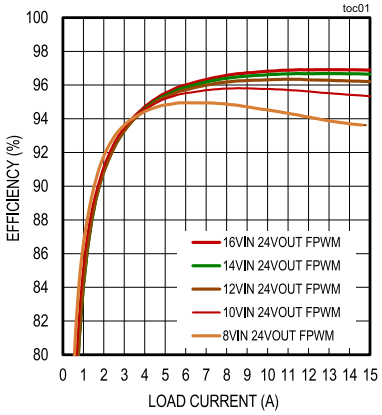
Note 2: All units are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltages are guaranteed by design and characterization.

Note 3: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

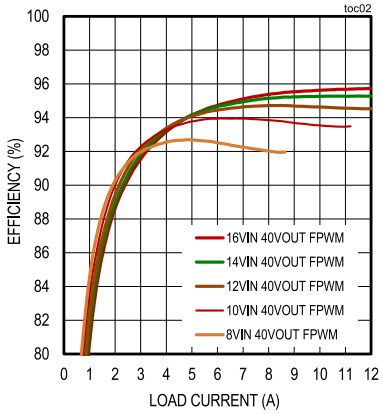
Typical Operating Characteristics

(V_{SUP} = 14V; V_{EN} = 14V; T_A = +25°C unless otherwise noted.)

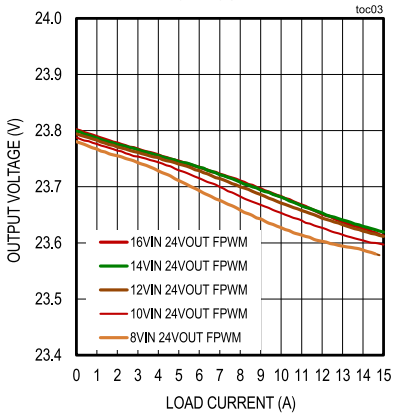
EFFICIENCY vs. LOAD CURRENT



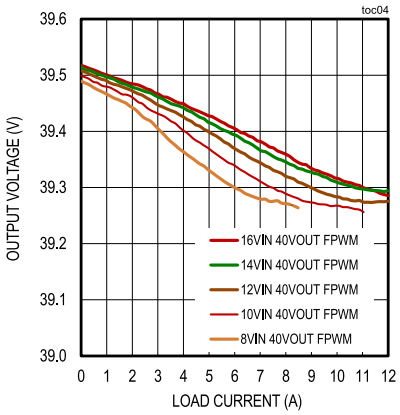
EFFICIENCY vs. LOAD CURRENT



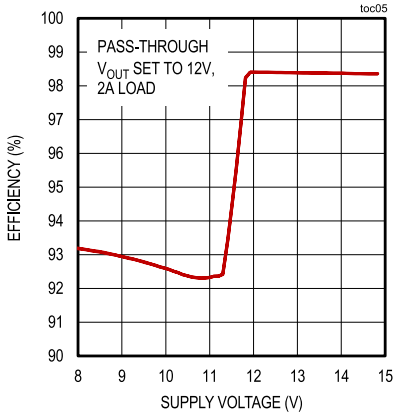
OUTPUT VOLTAGE vs. LOAD CURRENT



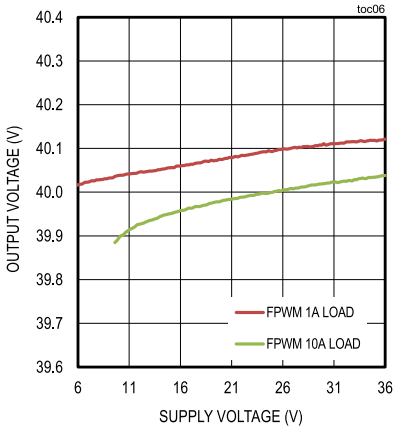
OUTPUT VOLTAGE vs. LOAD CURRENT



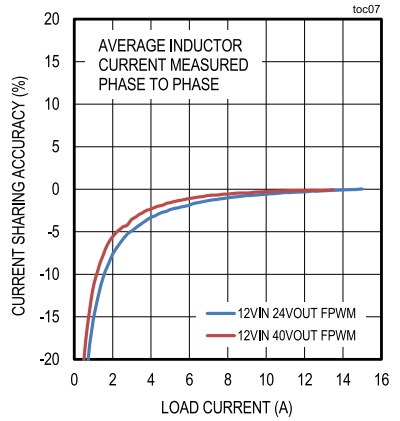
EFFICIENCY vs. SUPPLY VOLTAGE



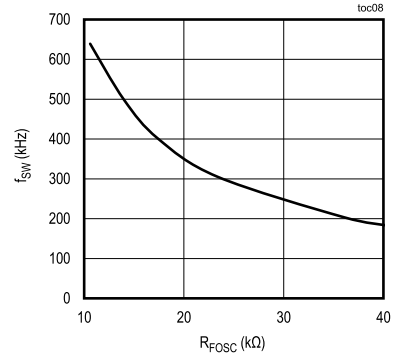
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



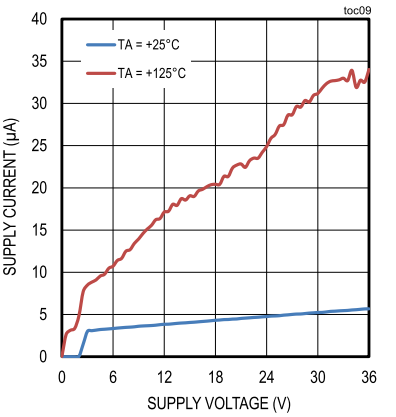
CURRENT SHARING ACCURACY vs. LOAD CURRENT



SWITCHING FREQUENCY vs. ROSC

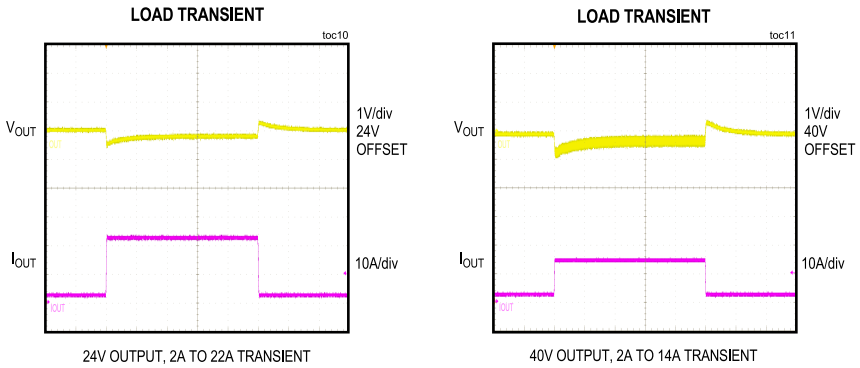


SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



Typical Operating Characteristics (continued)

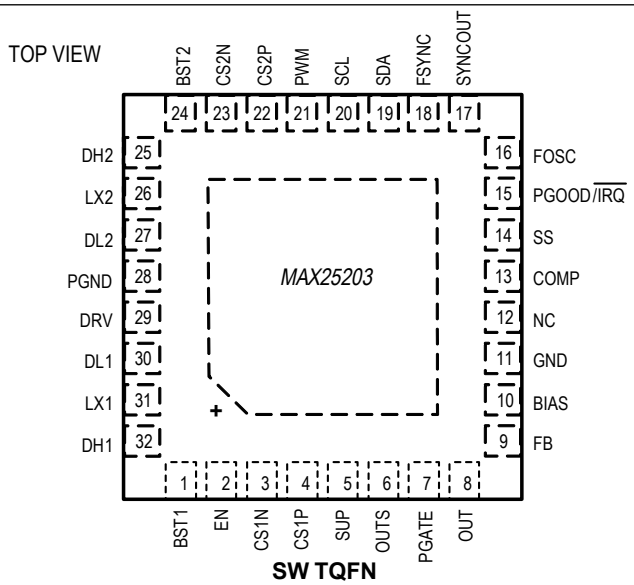
(V_{SUP} = 14V; V_{EN} = 14V; T_A = +25°C unless otherwise noted.)



24V OUTPUT, 2A TO 22A TRANSIENT

40V OUTPUT, 2A TO 14A TRANSIENT

Pin Configuration



SW TQFN
5mm x 5mm

Pin Description

PIN	NAME	FUNCTION
1	BST1	Boost Flying Capacitor Connection for High-Side Gate Voltage. Connect a high-voltage diode between DRV and BST1. Connect a ceramic capacitor between BST1 and LX1. See the *High-Side Gate-Driver Supply (BST)* section.
2	EN	High-Voltage Tolerant, Active-High Digital Enable Input for Controller. Driving EN low disables the boost controller. EN also has a very accurate threshold of ±3% for both rising and falling voltages. A resistor-divider can be used to control the turn ON and OFF of the boost controller in hardware by using a resistor-divider. When EN is low, the MAX25203 is powered off, including BIAS and I2C interface. Bring EN high to enable the MAX25203 and power up into the default state.

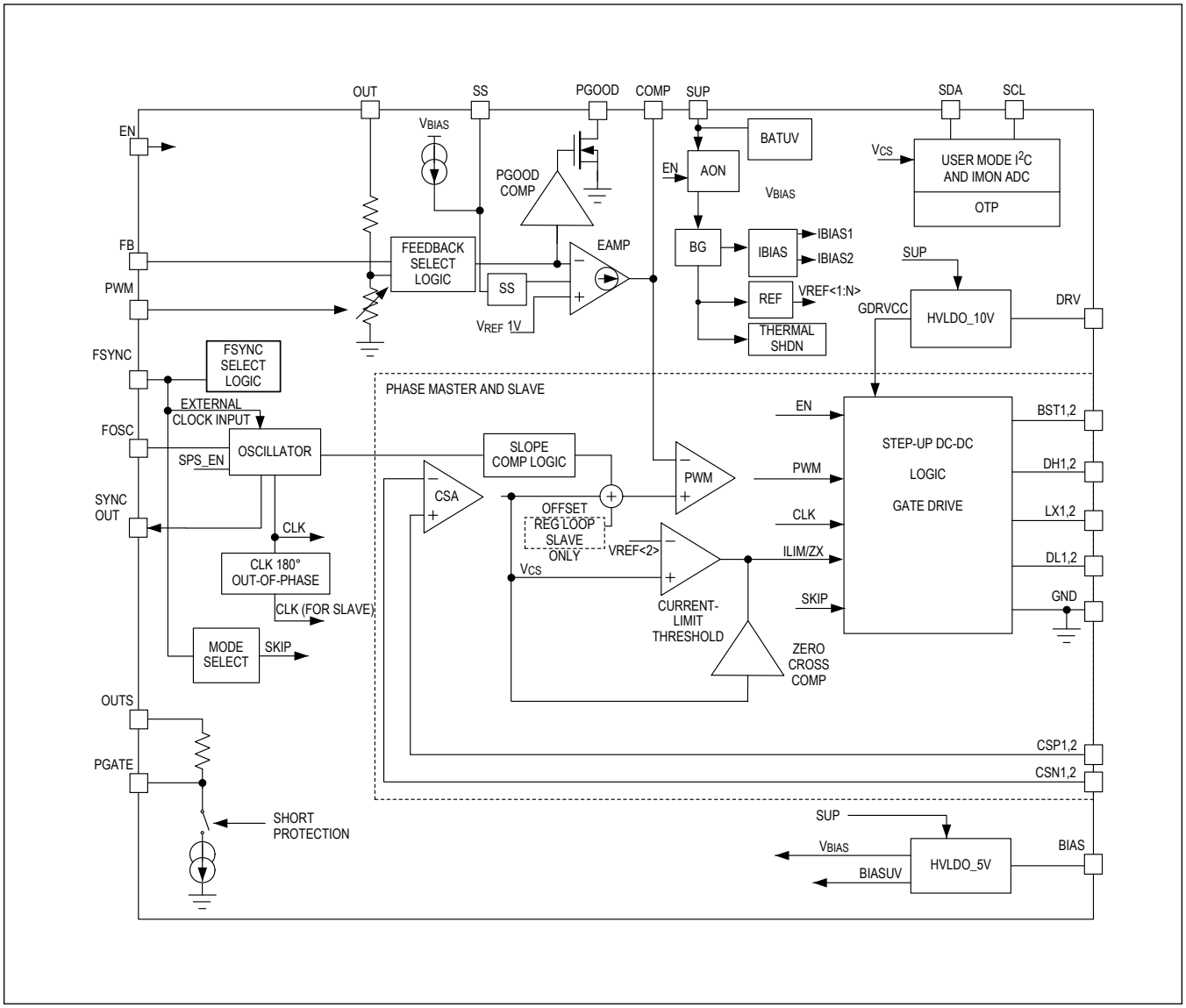
Pin Description (continued)

PIN	NAME	FUNCTION
3	CS1N	Negative Current-Sense Input for Phase 1. Connect CS1N to the negative side of the current-sense element. See the *Current Limiting and Current-Sense Inputs (SUP and CS)* section.
4	CS1P	Positive Current-Sense Input for Phase 1. Connect CS1P to the positive side of the current-sense element. See the *Current Limiting and Current-Sense Inputs (SUP and CS)* section.
5	SUP	Supply Input. Connect SUP to the main battery.
6	OUTS	True Shutdown PFET's Source Connection.
7	PGATE	External p-Channel MOSFET Gate Connection. Connect PGATE to the gate of the external p-channel output disconnect switch. Connect PGATE to GND if not used.
8	OUT	Output Voltage Sense for Internal Feedback Divider. Connect OUT to the boost output.
9	FB	Boost Converter Feedback Input. Connect FB to BIAS to use the I2C programmed output voltage or PWM voltage control. For external feedback, connect FB to the center tap of a resistor-divider between the boost regulator output. FB regulates to 1V (typ). See the *Setting and Controlling the Output Voltage* section.
10	BIAS	5V Internal Linear Regulator Output. Bypass BIAS to GND with a low-ESR ceramic capacitor of 1µF minimum value. BIAS provides the power to the internal circuitry and external loads. See the *Fixed 5V Linear Regulator (BIAS)* section.
11	GND	Ground.
12	NC	Leave this pin unconnected.
13	COMP	Boost Controller Error Amplifier Output. Connect an RC network to COMP to compensate the boost converter.
14	SS	Soft-Start. Connect a capacitor from SS to GND to set the soft-start time. See the *Soft-Start* section.
15	PGOOD/$\overline{IRQ}$	Open-Drain Power-Good Output or Interrupt Request. This pin is configured as either a power-good (PGOOD) output or interrupt request ($\overline{IRQ}$) output (see the *Ordering Information* table). To obtain a logic signal, pull up PGOOD/$\overline{IRQ}$ with an external resistor connected to a positive voltage lower than 5.5V. PGOOD pulls low when OUT is more than 93% (typ) below the normal regulation point. PGOOD is low during soft-start and in shutdown. PGOOD becomes high impedance when OUT is in regulation. $\overline{IRQ}$ pulls low when OUT is more than 93% (typ) below the normal regulation point and when a fault is reported in the FAULT register. $\overline{IRQ}$ is low during shutdown, and remains low after startup until the FAULT register has been read. $\overline{IRQ}$ becomes high impedance after reading the FAULT_STAT register when OUT is in regulation. If there is a persistent fault, $\overline{IRQ}$ pulls low again after reading FAULT, otherwise $\overline{IRQ}$ remains high until a fault occurs. See the *Output Voltage Monitor (PGOOD)* and *Interrupt Request Output ($\overline{IRQ}$)* sections for details.
16	FOSC	Frequency Setting Input. Connect a resistor to FOSC to set the switching frequency of the DC-DC converters.
17	SYNCOUT	Synchronization Clock Output. SYNCOUT outputs a clock that is 90° out-of-phase with the internal oscillator or the external FSYNC input. For the quad-phase configuration, connect SYNCOUT of the master to FSYNC of the slave.
18	FSYNC	External Clock Synchronization Input. To synchronize with an external clock, connect the clock to FSYNC. See the *Oscillator Frequency/External Synchronization* section. When not using external synchronization, connect FSYNC to BIAS for forced-PWM operation with the internal clock, or connect FSYNC to GND for skip-mode operation.
19	SDA	I2C Data Input/Output.
20	SCL	I2C Clock Input.

Pin Description (continued)

PIN	NAME	FUNCTION
21	PWM	PWM Positioning Control Input. Controls the output voltage, allowing it to track a digital duty cycle (PWM) signal. Connect PWM to GND when using an external resistor-divider to set the output voltage or if PWM is not used.
22	CS2P	Positive Current-Sense Input for Phase 2. Connect CS2P to the positive side of the current-sense element. See the *Current Limiting and Current-Sense Inputs (SUP and CS)* section.
23	CS2N	Negative Current-Sense Input for Phase 2. Connect CS2N to the negative side of the current-sense element. See the *Current Limiting and Current-Sense Inputs (SUP and CS)* section.
24	BST2	Boost Flying Capacitor Connection for High-Side Gate Voltage. Connect a high-voltage diode between DRV and BST2. Connect a ceramic capacitor between BST2 and LX2. See the *High-Side Gate-Driver Supply (BST)* section.
25	DH2	High-Side MOSFET Gate Driver Output. The DH2 output voltage swings from V_{LX2} to V_{BST2}.
26	LX2	Inductor Connection for Phase 2. Connect LX2 to the switched side of the inductor. LX2 serves as the lower supply rail for the DH2 high-side gate driver.
27	DL2	Low-Side n-Channel MOSFET Gate Driver Output for Phase 2.
28	PGND	Power Ground.
29	DRV	6.5V to 10V Preset Low-Dropout Voltage-Regulator Output. Bypass DRV to GND with a 4.7µF or greater ceramic capacitor. This voltage is used as the gate drive voltage for external MOSFETs. See the *Ordering Information* table for the factory-set DRV voltage.
30	DL1	Low-Side n-Channel MOSFET Gate Driver Output for Phase 1.
31	LX1	Inductor Connection for Phase 1. Connect LX1 to the switched side of the inductor. LX1 serves as the lower supply rail for the DH1 high-side gate driver.
32	DH1	High-Side MOSFET Gate Driver Output. The DH1 output voltage swings from V_{LX1} to V_{BST1}.
EP	EP	Exposed Pad. Connect the exposed pad to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to GND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Functional Diagram



Detailed Description

The MAX25203 automotive dual-phase synchronous boost controller enables infotainment systems to stay in regulation during cold-crank or start-stop operation all the way down to a battery input of 1.8V. It can also be used to generate backlight voltage and Class D audio amplifier voltages. This device can start with an input voltage supply from 4.5V to 42V and can operate down to 1.8V after start-up, and has a low 5µA shutdown supply current.

The MAX25203 operates at up to 2.1MHz frequency to allow small external components and reduced output ripple, and to guarantee no AM band interference. The switching frequency is resistor adjustable (220kHz to 2100kHz) or it can be synchronized on-the-fly to an external clock.

The MAX25203 has a spread-spectrum option for frequency modulation to minimize EMI interference. A 90° out-of-phase clock output enables synchronizing a second MAX25203 for quad-phase operation.

Pass-through operation has over 98% efficiency when the supply voltage exceeds the output regulation voltage. Programmable current-limit blanking handles high peak loads without oversizing the inductor.

The MAX25203 features a power-OK monitor and undervoltage lockout. Protection features include cycle-by-cycle current limit and thermal shutdown. It operates over the -40°C to +125°C automotive temperature range.

Current-Mode Control Loop

Peak current-mode control operation provides excellent load step performance and simple compensation. The inherent feed-forward characteristic is useful especially in automotive applications where the input voltage changes quickly during cold-crank and load-dump conditions. To avoid premature turn-off at the beginning of the on-cycle, the current-limit and PWM comparator inputs have leading-edge blanking.

Fixed 5V Linear Regulator (BIAS)

An internal 5V linear regulator (BIAS) is used to power the controller's internal circuitry. Connect a 1µF or greater ceramic capacitor from BIAS to GND as close to the IC pins as possible to guarantee stability under the full-load condition. If the BIAS voltage drops below the undervoltage (UVLO) threshold, the controller will shut down and all I2C register value reset to their default values.

Gate Drive LDO (DRV)

DRV is a low-dropout voltage regulator (LDO) used to supply the gate drive for external MOSFETs. The gate drive LDO output voltage is factory preset to 6.5V, 8V, or 10V; see the *Ordering Information* table for each part number's drive voltage. DRV can provide up to 150mA (typ) total. The gate drive current requirements can be estimated as follows:

$$I_{DRV} = f_{SW} (Q_{G1DL} + Q_{G1DH} + Q_{G2DL} + Q_{G2DH})$$

where f_{SW} is the switching frequency (per phase), and $Q_{G\_}$ is the low- and high-side MOSFET total gate charge (MOSFET specification at $V_{GS} = V_{DRV}$). To reduce the internal power dissipation, DRV can optionally be connected to an external 6.5V to 10V rail, bypassing the internal linear regulator.

If the DRV voltage drops below the undervoltage (UVLO) threshold switching stops, the controller is shutdown, and I2C register values are reset to default. When DRV rises above its UVLO rising threshold, the controller will begin soft-start.

Start-Up Operation/UVLO/EN

The BIAS input undervoltage lockout (UVLO) circuitry inhibits switching if the 5V bias supply (BIAS) is below its UVLO falling threshold (see the *Electrical Characteristics* table). Once the 5V bias supply (BIAS) rises above its UVLO rising threshold and EN is high, the boost controller starts switching and the output voltage begins to ramp up using soft-start. Driving EN low disables the device and reduces the standby current to less than 10µA.

Soft-Start

Soft-start ramps up the internal reference during start-up to reduce input surge current. Soft-start begins when EN is logic-high and V_{BIAS} and V_{DRV} are above the undervoltage lockout threshold. The soft-start time (t_{SS}) is set by connecting a resistor from SS to GND.

$C_{SS} = t_{SS} \times 10\ \mu\ A / V$

Oscillator Frequency/External Synchronization

The MAX25203 internal oscillator is set by a resistor connected from FOSC to GND with an adjustment range of 220kHz to 2.1MHz. High-frequency operation optimizes the application for the smallest component size, trading off efficiency to higher switching losses. Low-frequency operation offers the best overall efficiency at the expense of component size and board space. See the *Typical Operating Characteristics* section to determine the relationship between switching frequency and R_{FOSC}. For forced-PWM operation where the switching frequency matches the internal oscillator frequency, connect FSYNC to BIAS. Connect FSYNC to GND to allow skip-mode operation at light loads. With skip-mode, the output switches only as needed to supply the load, improving light-load efficiency.

The devices can also be synchronized to an external clock by connecting the external clock signal to FSYNC. For dual-phase/master controllers (see the *Ordering Information* table), the per-phase frequency is 1/4 of the applied external clock frequency. For slave controllers, FSYNC connects to SYNCOUT of the master (frequency equal to the phase frequency). The internal oscillator is synchronized on the rising edge of the external clock. See the *Electrical Characteristics* table for the FSYNC frequency range and voltage levels.

Pass-Through

When the supply voltage is higher than the output regulation voltage, switching is reduced to a 16µs period. During this period, the high-side MOSFETs are turned on in order to maximize efficiency, and the output voltage will follow the supply voltage. At the end of the 16µs period, a short switching cycle keeps the BST capacitors charged in order to maintain the high-side gate drive voltage.

Spread Spectrum

Spread spectrum is used to reduce peak emission noise at the clock frequency and its harmonics, making it easier to meet stringent EMI limits. This is done by dithering the switching frequency by a programmable percentage of the switching frequency. The amount of dithering is programmable by I2C to between 0% (disabled), ±6%, or ±9%. See the *Ordering Information* table for the default power-on spread spectrum setting. When using an external clock source (i.e., driving the FSYNC input with an external clock), spread spectrum is disabled.

MOSFET Drivers (DH and DL)

The DH high-side n-channel MOSFET driver is powered from BST while the low-side driver (DL) is powered from BIAS. Each driver has shoot-through protection that monitors the gate-to-source voltage of the external MOSFETs to prevent a MOSFET from turning on until the complementary switch is fully off. This requires a low-resistance, low-inductance path from DL and DH to the MOSFET gates for the protection circuits to work properly.

High-Side Gate-Driver Supply (BST)

The high-side MOSFET is turned on by closing an internal switch between BST and DH and transferring the bootstrap capacitor's charge (at BST) to the gate of the high-side MOSFET. This charge refreshes when the high-side MOSFET turns off and the LX voltage drops down to ground potential, taking the negative terminal of the capacitor to the same potential. At this time, the bootstrap diode recharges the positive terminal of the bootstrap capacitor.

The selected n-channel, high-side MOSFET determines the appropriate boost capacitance values according to the following equation:

$C_{BST} = Q_G/\Delta V_{BST}$

where Q_G is the total gate charge of the high-side MOSFET and ΔV_{BST} is the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose ΔV_{BST} such that the available gate-drive voltage is not significantly degraded

(e.g., ΔV_{BST} = 100mV to 300mV) when determining C_{BST}. The boost capacitor should be a low-ESR ceramic capacitor. A minimum value of 0.1µF works well in most cases. Choose a diode with low reverse current (<1µA) at maximum temperature and voltage.

p-Channel MOSFET Output Disconnect

An optional p-channel MOSFET disconnects the output from the supply when shut down and provides short-circuit protection. See the *Typical Operating Circuit* for the p-channel MOSFET connections. When this feature is not used, connect PGATE to GND.

Current Limiting and Current-Sense Inputs (SUP and CS)

The current-limit circuit uses differential current-sense inputs (CS_P and CS_N) to limit the peak inductor current. If the magnitude of the current-sense signal exceeds the current-limit threshold (V_{LIMIT} > 50mV (typ)), the PWM controller turns off the high-side MOSFET.

For the most accurate current sensing, use a current-sense resistor between the inductor and the input capacitor. Connect CS_N to the inductor side of R_{CS} and CS_P to the capacitor side. See the *Current-Sense Resistor Selection* section to determine the resistor value.

To improve efficiency, the current can also be measured directly across the inductor, eliminating the power loss from the sense resistor. However, this method is significantly less accurate and requires a filter network in the current-sense circuit. See the *Inductor DCR Current Sense* section for more information.

Output Voltage Monitor (PGOOD)

PGOOD is an open-drain output used to monitor the output voltage. PGOOD pulls low when the output voltage drops below the PGOOD threshold (see the *Electrical Characteristics* table). PGOOD is high impedance when the output voltage is in regulation. Typically a pullup resistor is connected from PGOOD to the relevant logic rail to provide a logic-level output.

Typically when changing the output voltage by I2C or PWM control, PGOOD does not pull low due to undervoltage during the transition. This is done by blanking the PGOOD output during the ramp up/down time plus the PGOOD timeout (see the *Electrical Characteristics* table). In some cases where a large output capacitance is used, the output voltage may not be able to reach the final value during blanking time. In this case, it is possible for PGOOD to briefly pull low during the transition.

Interrupt Request Output ($\overline{IRQ}$)

$\overline{IRQ}$ is the open-drain interrupt request output. This is a factory option that replaces the PGOOD output; see the *Ordering Information* table for supported parts.

$\overline{IRQ}$ pulls low when the output voltage drops below the PGOOD threshold (see the *Electrical Characteristics* table) and when a fault is flagged in the FAULT_STAT register. $\overline{IRQ}$ is high impedance when the output voltage is in regulation and no faults are flagged. Typically a pullup resistor is connected from $\overline{IRQ}$ to the relevant logic rail to provide a logic-level output. $\overline{IRQ}$ is low when disabled and during start-up remains low until soft-start is complete and the FAULT_STAT register has been read.

When a fault occurs, it it is latched in the FAULT_STAT register, so $\overline{IRQ}$ remains low until the FAULT register is read. Reading the fault register clears the flagged faults; however, if the fault persists it is immediately flagged again, and $\overline{IRQ}$ pulls low again.

Protection Features

I2C Fault Flags

The FAULT register indicates if any faults have occurred since the last time the register was read. Reading the register clears all fault flags; however, if the fault condition persists, the corresponding flag will be set again. The fault conditions reported in the FAULT register are output overvoltage, output undervoltage, input undervoltage, and overcurrent for phase 1 and phase 2. See the *Register Map* for more information.

Initially after power-up, all fault bits are set. This indicates that a reset has occurred, not that the fault corresponding to

each flag has occurred. The FAULT register should be read after power-up to clear the fault flags.

Overvoltage Protection

The devices limit the output voltage by turning off the high-side gate driver if the output voltage exceeds 105% (typ) of the nominal output voltage. The output voltage needs to come back into regulation before the device resumes switching.

Overcurrent Protection

If the inductor current exceeds the maximum current limit set by R_{CS} or inductor DCR sensing, the respective MOSFET driver turns off. If the output current is increased further, this results in shorter and shorter high-side pulses. A hard short results in a minimum on-time pulse every clock cycle. Choose the components so they can withstand the short-circuit current, if required. If an overcurrent conditions persists for the current-limit blanking time, hiccup protection is activated and the BST1_OC or BST2_OC bit in the FAULT register will be set. The hiccup protection stops switching for 100ms then attempts to soft-start. This is repeated until start-up is successful. If the sensed current exceeds the current-limit threshold by 50% or more, hiccup protection does not wait for the current-limit blanking time.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the devices. When the junction temperature exceeds +170°C (typ), an internal thermal sensor shuts down the device, allowing it to cool down. The thermal sensor turns on the devices again after the junction temperature cools by 20°C (typ).

I2C Interface

The MAX25203 feature an I2C-/SMBus-compatible, 2-wire slave serial interface consisting of a serial data line (SDA) and a serial clock line (SCL).

I2C Timing Diagram

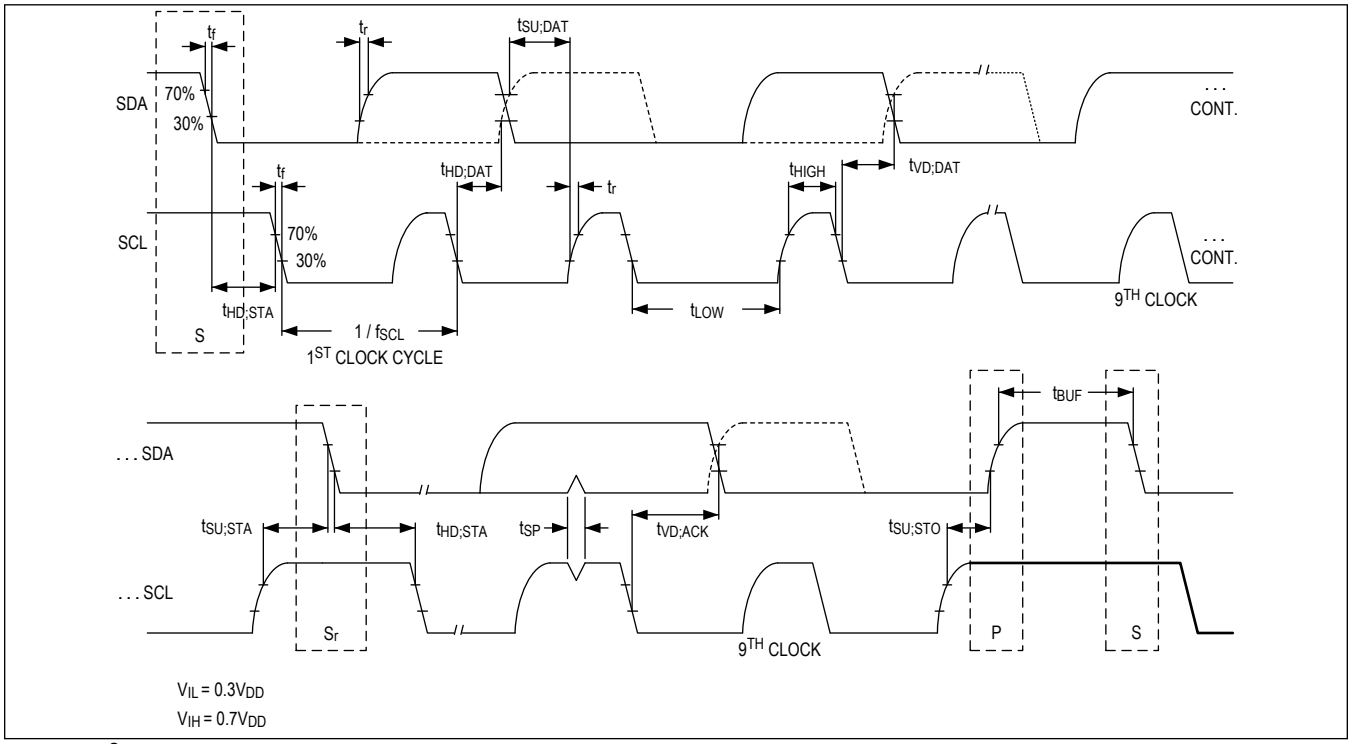


Figure 1. I2C Timing Diagram

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). SDA and SCL idle high when the I2C bus is not busy.

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changing SDA while SCL is high will result in control conditions being issued. A high-to-low transition on the SDA line while SCL is high defines a START (S) condition. A low-to-high transition on the SDA line while SCL is high defines a STOP (P) condition. START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition. The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In this respect, the START (S) and repeated START (Sr) conditions are functionally identical.

Clock Stretching

In general, the clock signal generation for the I2C bus is the responsibility of the master device. The I2C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX25203 do not use any form of clock stretching to hold down the clock line.

Slave Address

The slave address consists of 7 address bits followed by the R/W bit. Set the R/W bit to 1 to configure the devices to read mode. Set the R/W bit to 0 to configure the device to write mode. The address is the first byte of information sent to the devices after the START condition. See the *Ordering Information* table for the slave address value.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the device uses to handshake receipt each byte of data. The device pulls down SDA during the master-generated 9th clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master can reattempt communication.

Write Data Format

A write to the device includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one byte of data to the register address, one byte of data to the command register, and a STOP condition.

Read Data Format

A read from the device includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one byte of data to the register address, a restart condition, the slave address with R/$\overline{W}$ bit set to 1, one byte of data to the command register, and a STOP condition.

I2C Data Format

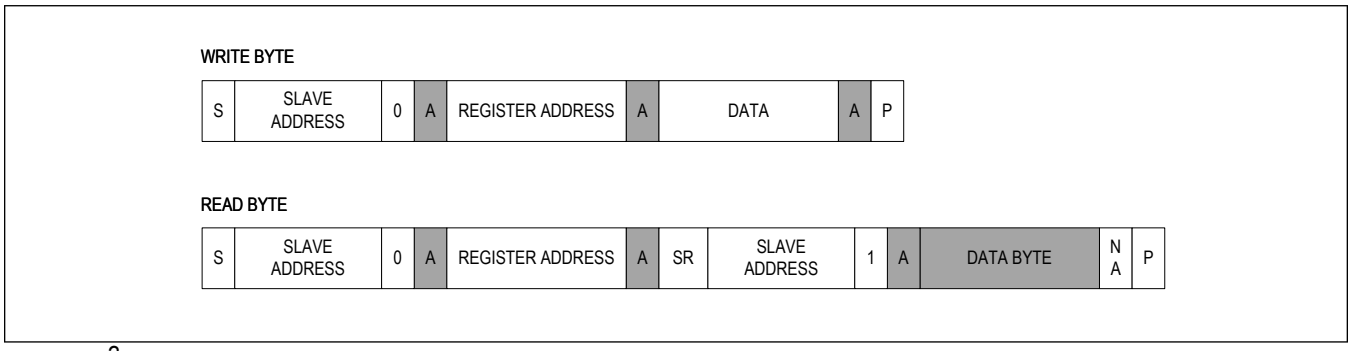


Figure 2. I2C Data Format

Register Map

MAX25203

ADDRESS	NAME	MSB							LSB
USR_REGS									
0x00	CHIP_ID_REG[7:0]	DIE_TYPE[7:0]							
0x01	BST_CTRL_0_REG[7:0]	RSVD	EN_PH2	ILIM_BLANK[1:0]		RAMP_RATE[1:0]		VIN_UV_TH[1:0]	
0x02	BST_CTRL_1_REG[7:0]	SPS_EN	SPS_RANGE	–	–	–	–	–	–
0x03	BST_CTRL_2_REG[7:0]	–	–	VOUT_THR[5:0]					
0x05	BST1_IMON_REG[7:0]	BST1_IMON[7:0]							
0x06	BST2_IMON_REG[7:0]	BST2_IMON[7:0]							
0x07	DIE_TEMP_REG[7:0]	DIE_TEMP[7:0]							
0x08	FAULT_STAT_REG[7:0]	VOUT_OV	VOUT_UV	BST1_OC	BST2_OC	VIN_UV	–	–	–
SW_RESET									
0x0F	SW_RESET_REG[7:0]	SW_RST	–	–	–	–	–	–	–

Register Details

CHIP_ID_REG (0x00)

BIT	7	6	5	4	3	2	1	0
Field	DIE_TYPE[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DIE_TYPE	7:0	Read Only. See the Ordering Information table for the fixed value of this register. This can be used to identify the IC on the I2C bus.

BST_CTRL_0_REG (0x01)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	EN_PH2	ILIM_BLANK[1:0]		RAMP_RATE[1:0]		VIN_UV_TH[1:0]	
Reset	0x1	0x1	0x01		0x0		0x0	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Set this bit to 1 when writing BST_CTRL0_REG.	
EN_PH2	6	Phase 2 Controller Enable.	0x0: Disable phase 2 controller 0x1: Enable phase 2 controller

BITFIELD	BITS	DESCRIPTION	DECODE
ILIM_BLANK	5:4	Current-Limit Blanking Time. An overcurrent condition that persists for the blanking time triggers hiccup overcurrent protection and flags in the FAULT register. Note: If the current exceeds the current limit by more than 50%, the protection is activated immediately.	0x0: 0ms 0x1: 50ms 0x2: 100ms 0x3: 20ms
RAMP_RATE	3:2	Sets the ramp time when changing the output voltage from 12V to 65V.	0x0: 8ms 0x1: 500µs 0x2: 1ms 0x3: 2ms
VIN_UV_TH	1:0	Input Undervoltage Threshold.	0x0: 5V 0x1: 6V 0x2: 7V 0x3: 8V

BST_CTRL_1_REG (0x02)

BIT	7	6	5	4	3	2	1	0
Field	SPS_EN	SPS_RANGE	–	–	–	–	–	–
Reset	OTP	OTP	–	–	–	–	–	–
Access Type	Write, Read	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
SPS_EN	7	Spread Spectrum. See the Ordering Information table for the reset value.	0x0: Spread spectrum disabled 0x1: Spread spectrum enabled
SPS_RANGE	6	Spread Spectrum Clock Setting. See the Ordering Information table for the reset value.	0x0: ±9% 0x1: ±6%

BST_CTRL_2_REG (0x03)

BIT	7	6	5	4	3	2	1	0
Field	–	–	VOUT_THR[5:0]					
Reset	–	–	OTP					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
VOUT_THR	5:0	Output Voltage Setting. Sets the output feedback threshold of the OUT pin between 12V and 65V. V_{OUT} = 12 + VOUT_THR[5:0]. Any code that is greater than the decimal 53 is reserved. See the Ordering Information table for the default voltage setting. Do not write to this register when using the PWM output voltage control.

BST1_IMON_REG (0x05)

BIT	7	6	5	4	3	2	1	0
Field	BST1_IMON[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BST1_IMON	7:0	Current-Sense Resistor Voltage ADC Measurement for Phase 1. V_{CS1} = 0.5415 x BST1_IMON - 19.0

BST2_IMON_REG (0x06)

BIT	7	6	5	4	3	2	1	0
Field	BST2_IMON[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BST2_IMON	7:0	Current-Sense Resistor Voltage ADC Measurement for Phase 2. V_{CS2} = 0.5415 x BST1_IMON - 19.0

DIE_TEMP_REG (0x07)

BIT	7	6	5	4	3	2	1	0
Field	DIE_TEMP[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DIE_TEMP	7:0	Die Temperature ADC Measurement. T_J (°C) = 2.04 x DIE_TEMP - 273

FAULT_STAT_REG (0x08)

When a fault occurs, a 1 is latched into the corresponding bit. All fault bits are cleared after reading this register. On power-up, all fault bits are set to indicate reset.

BIT	7	6	5	4	3	2	1	0
Field	VOUT_OV	VOUT_UV	BST1_OC	BST2_OC	VIN_UV	–	–	–
Reset	0x1	0x1	0x1	0x1	0x1	–	–	–
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VOUT_OV	7	Output Overvoltage Flag.	0x0: No fault. 0x1: Output exceded overvoltage threshold 108% of target.
VOUT_UV	6	Output Undervoltage Fault.	0x0: No fault. 0x1: Output dropped below the undervoltage threshold 93% of target (2% hysteresis).

BITFIELD	BITS	DESCRIPTION	DECODE
BST1_OC	5	Phase 1 Overcurrent Fault.	0x0: No fault. 0x1: Phase 1 current exceeded the overcurrent threshold.
BST2_OC	4	Phase 2 Overcurrent Fault.	0x0: No fault. 0x1: Phase 2 exceeded the overcurrent threshold.
VIN_UV	3	Supply Voltage Undervoltage Fault. VIN_UV is asserted when the supply voltage is below the value specified in VIN_UV_TH[1:0].	0x0: No fault. 0x1: The supply voltage dropped below the undervoltage threshold.

SW_RESET_REG (0x0F)

BIT	7	6	5	4	3	2	1	0
Field	SW_RST	–	–	–	–	–	–	–
Reset	0x0	–	–	–	–	–	–	–
Access Type	Write, Read, Ext	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
SW_RST	7	Write 1 to Force Software Reset. This sets all registers to their power-on default values and soft-starts the controller. Reads back 0.

Applications Information

Setting and Controlling the Output Voltage

The MAX25203 provides three methods of setting the output voltage: an external resistor-divider, I2C, and PWM input. Any one of these methods may be used to control the output voltage; however, do not change methods during operation.

External Feedback Divider

To use an external resistor-divider to set the output voltage, connect FB to the center tap of two resistors connected from the output to ground, as shown in Figure 3. When using the external divider, the output voltage range is 3.5V to 65V. The PWM input and I2C voltage setting are ignored in this configuration. PWM should be connected to GND.

Calculate the divider resistor values as follows:

$$R1 = R2\left[\frac{V_{OUT}}{V_{FB}} - 1\right]$$

where V_{FB} is the regulated feedback voltage (see the *Electrical Characteristics* table).

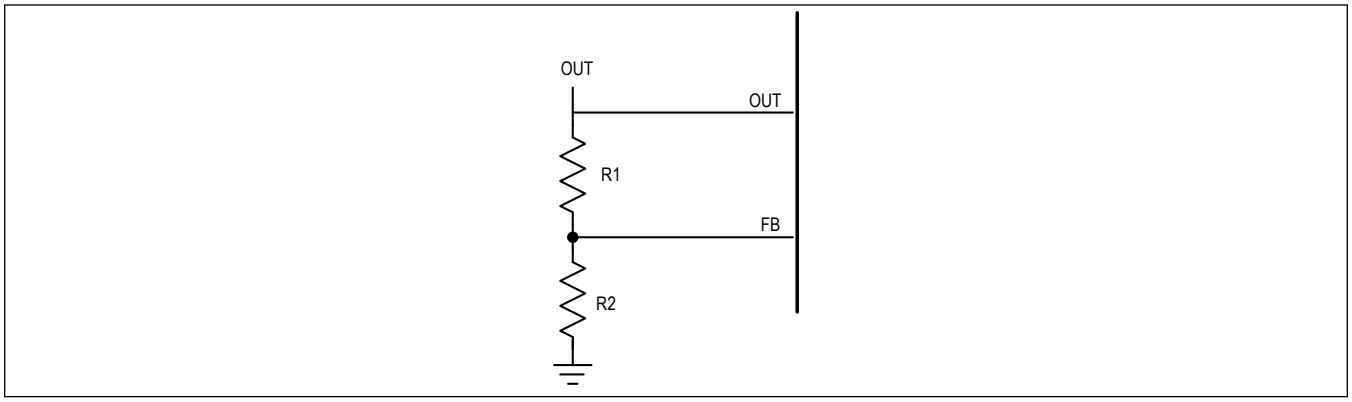


Figure 3. External Feedback Divider

I2C Voltage Setting

When using I2C to control the output voltage, connect FB to BIAS and connect PWM to GND. If FB is connected to an external divider, the register value will be ignored and the output voltage will correspond to the value set by the divider.

With configured for I2C voltage control, the MAX25203 initially powers on to the default output voltage (see the *Ordering Information* table). The output voltage can then be changed to any voltage from 12V to 65V in 1V steps by writing to VOUT_THR[5:0] in the BST_CTRL_2_REG register. Writing 0 corresponds to 12V, and decimal 53 or higher corresponds to 65V.

V_{OUT} = 12 + VOUT_THR[5 : 0] for VOUT_THR[5 : 0] ≤ 53

V_{OUT} = 65V for VOUT_THR[5 : 0] > 53

When the voltage setting is changed, the output voltage changes in 1V steps until it reaches the new value. The total time to change to the new target voltage is set in RAMP_RATE[1:0]. If VOUT_THR[5:0] is changed before reaching the previous target voltage, the output will step towards the new target voltage.

On initial power-on, the output completes soft-start to the factory default setting. If VOUT_THR[5:0] is changed during soft-start, the output will continue to the factory default setting and complete soft-start before starting to step to the new target voltage.

PWM Voltage Control

To use the PWM input to control the output voltage, FB must connect to BIAS. The PWM input does not function when

using an external resistor-divider to set the voltage.

To control the output voltage with the PWM input, apply a 400kHz (typ) PWM signal to PWM. See the *Electrical Characteristics* table for the PWM frequency range. The output can change from 12V to 65V in 1V steps, with each 1V step corresponding to a 0.8% change in duty cycle in the range 25% to 67%. A duty cycle of less than or equal to 25% corresponds to 12V output, and greater or equal to 67% corresponds to 65V output. For ICs with the maximum output limited to less than 65V, contact the factory.

The output voltage target only changes when a 0.8% or greater change in duty cycle (in the 25% to 67% range) is detected on PWM. Duty-cycle changes outside this range are ignored. If this change occurs during soft-start, the PWM setting is ignored until the PWM duty cycle changes again by at least 0.8%.

If the PWM input is low at startup, the output will go to the default output voltage (see the *Ordering Information* table). Once there is a transition on the PWM input, the PWM control takes affect. If the PWM signal is present at startup (including 100% duty cycle), the output starts up to the voltage determined by the PWM signal.

Inductor Selection

Duty cycle and frequency are important to calculate the inductor size, as the inductor current ramps up during the on-time of the switch and ramps down during its off-time. A higher switching frequency generally improves transient response and reduces component size; however, if the boost components are to be used as the input filter components during non-boost operation, a low frequency is advantageous.

The duty-cycle range of the boost converter depends on the effective input-to-output voltage ratio. In the following calculations, the duty cycle refers to the on-time of the boost MOSFET:

$$D_{MAX} = \frac{V_{OUT(MAX)} - V_{SUP(MIN)}}{V_{OUT(MAX)}}$$

The ratio of the inductor peak-to-peak AC current to DC average current must be selected first. A good initial value is a 30% peak-to-peak ripple current to average current ratio. The switching frequency, input voltage, output voltage, and selected LIR determine the inductor value as follows:

$$L[\mu H] = \frac{V_{SUP} \times D}{f_{SW}[MHz] \times LIR}$$

where:

$D = (V_{OUT} - V_{SUP})/V_{OUT}$

V_{SUP} = typical input voltage

V_{OUT} = typical output voltage

$LIR = 0.3 \times I_{OUT}/(1 - D)$

Select the inductor with a saturation current rating higher than the peak switch current limit of the converter:

$$I_{L\_PEAK} > I_{L\_MAX} + \frac{\Delta I_{L\_RIP\_MAX}}{2}$$

Running a boost converter in continuous-conduction mode introduces a right-half plane zero into the transfer function. To avoid the effect of this right-half plane zero, the crossover frequency for the control loop should be ≤ 1/3 x f_{RHP_ZERO}. If a faster bandwidth is required, a smaller inductor and higher switching frequency are recommended.

Input Capacitor Selection

The input current for the boost converter is continuous and the RMS ripple current at the input capacitor is low. Calculate the minimum input capacitor value and the maximum ESR using the following equations:

$$C_{SUP} = \frac{\Delta I_L \times D}{4 \times f_{SW} \times \Delta V_Q}$$

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_L}$$

where:

$$\Delta I_L = \frac{\left(V_{SUP} - V_{DS}\right) \times D}{L \times f_{SW}}$$

V_{DS} is the total voltage drop across the external MOSFET plus the voltage drop across the inductor ESR. ΔI_L is the peak-to-peak inductor ripple current as calculated above. ΔV_Q is the portion of input ripple due to the capacitor discharge and ΔV_{ESR} is the contribution due to ESR of the capacitor. Assume the input capacitor ripple contribution due to ESR (ΔV_{ESR}) and capacitor discharge, (ΔV_Q) are equal when using a combination of ceramic and aluminum capacitors. During the converter turn-on, a large current is drawn from the input source, especially at a high output-to-input differential.

Output Capacitor Selection

In a boost converter, the output capacitor supplies the load current when the boost MOSFET is on. The required output capacitance is high, especially at higher duty cycles. Also, the output capacitor ESR needs to be low enough to minimize the voltage drop while supporting the load current. Use the following equations to calculate the output capacitor for a specified output ripple. All ripple values are peak to peak:

$$ESR = \frac{\Delta V_{ESR}}{I_{OUT}}$$

$$C = \frac{I_{OUT} \times D_{MAX}}{\Delta V_Q \times f_{SW}}$$

where:

I_{OUT} = load current in A

f_{SW} is in MHz

C_{OUT} is in µF

ΔV_Q = portion of ripple due to capacitor discharge

ΔV_{ESR} = contribution due to capacitor ESR

D_{MAX} = maximum duty cycle at the minimum input voltage.

Use a combination of low-ESR ceramic and high-value, low-cost aluminum capacitors for lower output ripple and noise.

Current-Sense Resistor Selection

The current-sense resistor ($R_{CS\_}$) connected between the battery and the inductor sets the current limit. The CS_ input has a voltage trip level ($V_{CS\_}$) of 50mV (typ).

Set the current-limit threshold high enough to accommodate the component variations. Use the following equation to calculate the value of RCS_:

$$R_{CS} = \frac{V_{CS}}{I_{SUP(MAX)}}$$

where $I_{IN(MAX)}$ is the peak current that flows through the MOSFET at full load and a minimum V_{IN}.

$$I_{SUP(MAX)} = \frac{I_{LOAD(MAX)}}{1 - D_{MAX}}$$

When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (DL) quickly terminates the on-cycle.

Current-Sense Configurations

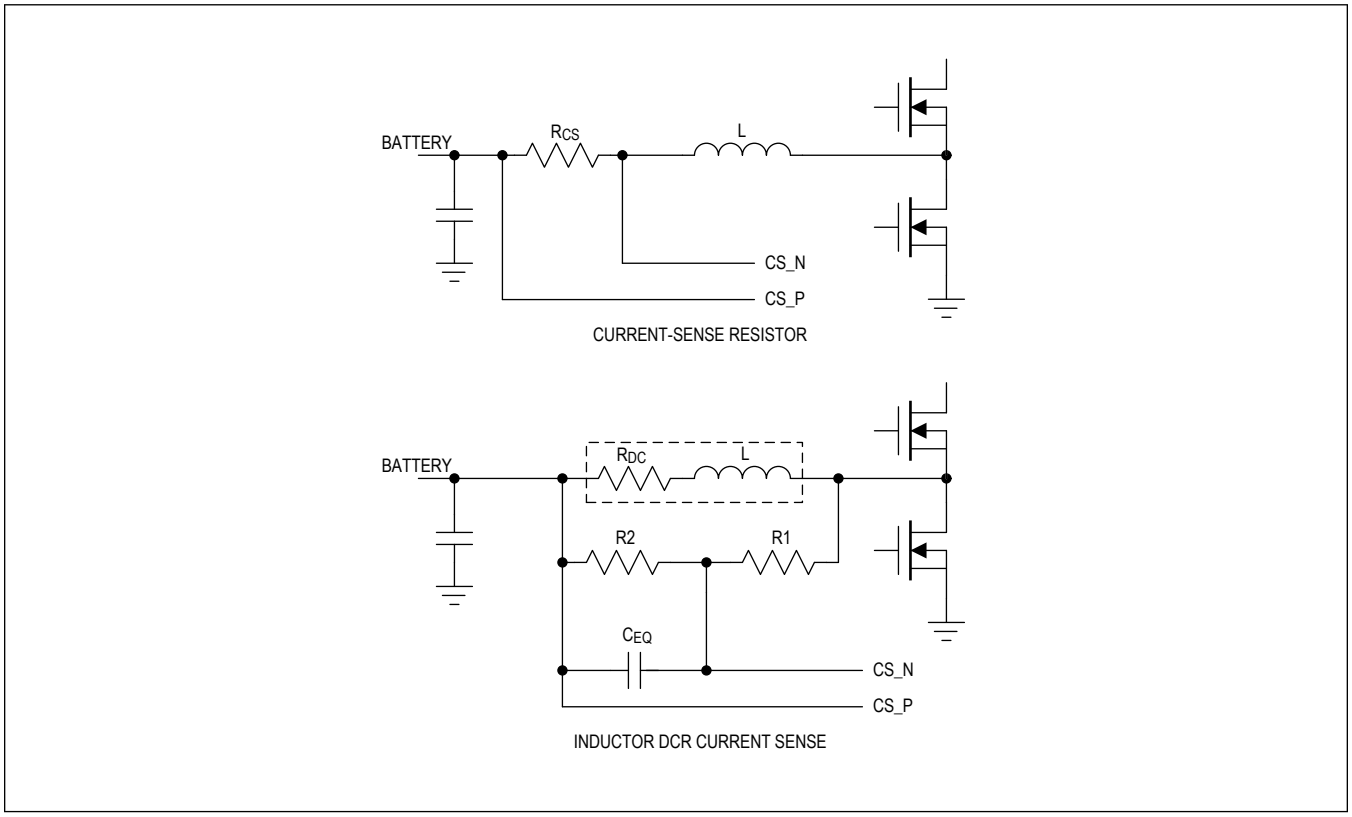


Figure 4. Current-Sense Configurations

Inductor DCR Current Sense

High-power applications that do not require accurate current sense can use the inductor's DC resistance as the current-sense element instead of the current-sense resistor. This is done by with an RC network across the inductor. The equivalent sense resistance of the network is:

$$R_{CS\_EQ} = \left(\frac{R2}{R1 + R2}\right) \times R_{DC}$$

where R_{DC} is the DC resistance of the inductor, R1 is connected from the switch side of the inductor to CS_N, and R2 is connected from the battery side of the inductor to CS_N (see Figure 4). The capacitor C_{EQ} (connected parallel to R2) is calculated as follows:

$$C_{EQ} = \frac{L}{R_{DC}}\left(\frac{1}{R1} + \frac{1}{R2}\right)$$

Boost Converter Compensation

The basic regulator loop is modeled as a power modulator, output feedback-divider, and error amplifier, as shown in Figure 4. The power modulator has a DC gain set by g_{mc} x R_{LOAD}, with a pole and zero pair set by R_{LOAD}, the output capacitor (C_{OUT}), and its ESR. The loop response is set by the following equation:

$$G_{MOD} = g_{MC} \times R_{LOAD} \times \left(\frac{1 - D}{2}\right) \times \left(\frac{1 + j\frac{f}{f_{zMOD}}}{1 + j\frac{f}{f_{pMOD}}}\right) \times \left(1 - j\frac{f}{f_{Rph\_zMOD}}\right)$$

where $R_{LOAD} = V_{OUT}/I_{LOUT(MAX)}$ in Ω, and $g_{mc} = 1/(A_{V\_CS} \times R_{DC})$ in S. A_{V_CS} is the voltage gain of the current-sense amplifier and is typically 12V/V. R_{DC} is the DC resistance of the inductor or the current-sense resistor in Ω.

In a current-mode step-down converter, the output capacitor and the load resistance introduce a pole at the following frequency:

$$f_{pMOD} = \frac{1}{\pi \times R_{LOAD} \times C_{OUT}}$$

The output capacitor and its ESR also introduce a zero at:

$$f_{zMOD} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

The right-half plane zero is at:

$$f_{Rph\_zMOD} = \frac{R_{LOAD}}{2\pi \times L} \times (1 - D) \times (1 - D)$$

When C_{OUT} is composed of "n" identical capacitors in parallel, the resulting $C_{OUT} = n \times C_{OUT(EACH)}$, and ESR = ESR(EACH)/n. Note that the capacitor zero for a parallel combination of similar capacitors is the same as for an individual capacitor.

The feedback voltage-divider has a gain of $GAIN_{FB} = V_{FB}/V_{OUT}$, where V_{FB} is 1.0V (typ).

The transconductance error amplifier has a DC gain of $GAIN_{EA(DC)} = g_{m,EA} \times R_{OUT,EA}$, where $g_{m,EA}$ is the error-amplifier transconductance, which is 370µS (max), and $R_{OUT,EA}$ is the output resistance of the error amplifier, which is 10MΩ (typ) See the *Electrical Characteristics* table for details.

A dominant pole (f_{dpEA}) is set by the compensation capacitor (CC) and the amplifier output resistance ($R_{OUT,EA}$). A zero (f_{ZEA}) is set by the compensation resistor (RC) and the compensation capacitor (CC). There is an optional pole (f_{PEA}) set by CF and RC to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C), where the loop gain equals 1 (0dB). Thus:

$$f_{pEA} = \frac{1}{2\pi \times \left(R_{OUTEA} + R_C\right) \times C_C}$$

$$f_{zEA} = \frac{1}{2\pi \times R_C \times C_C}$$

$$f_{p2EA} = \frac{1}{2\pi \times R_C \times C_F}$$

The loop gain crossover frequency (f_C) should be ≤ 1/3 of right-half plane zero frequency.

$$f_C \le \frac{f_{Rph\_zMOD}}{3}$$

At the crossover frequency, the total loop gain must be equal to 1. So:

$$GAIN_{MOD(f_C)} \times \frac{V_{FB}}{V_{OUT}} \times GAIN_{EA(f_C)} = 1$$

$$GAIN_{EA(f_C)} = g_{m,EA} \times R_C$$

$$GAIN_{MOD(f_C)} = GAIN_{MOD(dc)} \times \frac{f_{pMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(f_C)} \times \frac{V_{FB}}{V_{OUT}} \times g_{m,EA} \times R_C = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT}}{g_{m,EA} \times V_{FB} \times GAIN_{MOD(f_C)}}$$

Set the error-amplifier compensation zero formed by R_C and C_C at the f_{pMOD}. Calculate the value of C_C as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor (C_F) from COMP to GND. The value of C_F is:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

MOSFET Selection

The key selection parameters to choose the n-channel MOSFET used in the boost converter are as follows.

Threshold Voltage

The boost n-channel MOSFETs are driven with gate voltage of V_{DRV}. Make sure the on-resistance of the selected MOSFETs is specified at this gate voltage.

Maximum Drain-to-Source Voltage ($V_{DS(MAX)}$)

The MOSFET must be chosen with an appropriate V_{DS} rating to handle all V_{IN} voltage conditions.

Current Capability

The n-channel MOSFET must deliver the input current ($I_{IN(MAX)}$):

$$I_{IN(MAX)} = I_{LOAD(MAX)} \times \frac{D_{MAX}}{1 - D_{MAX}}$$

Choose MOSFETs suitable for the appropriate average current at $V_{GS} = V_{DRV}$.

Low-Voltage Operation

The devices operate down to a voltage of 4.5V or less on their SUP pins. If the system input voltage is lower than this the circuit can be operated from its own output as shown in the *Bootstrap Application Circuit*. At very low input voltages, it is important to remember that the input current will be high and the power components (inductor, MOSFET, and diode) must be specified for this higher input current.

In addition, the current-limit of the devices must be set high enough so that the limit is not reached during the on-time of the MOSFET, which would result in output power limitation and eventually entering hiccup mode. Estimate the maximum input current using the following equation:

$$I_{SUPMAX} = \left(\frac{V_{OUT} \times I_{OUT}}{\eta}\right) \Big/ V_{SUPMIN} + 0.5 \times \frac{V_{OUT} - V_{SUPMIN}}{V_{OUT}} \times \frac{V_{SUPMIN}}{f_{SW} \times L}$$

where:

I_{INMAX} = maximum input current

V_{OUT} = output voltage

I_{OUT} = output current

η = estimated efficiency (lower at low input voltages due to higher resistive losses)

V_{INMIN} = minimum value of the input voltage

f_{SW} = switching frequency

L = minimum value of the chosen inductor

Quad-Phase Operation

Two MAX25203 devices can operate together in a quad-phase master/slave configuration in order to double the output power capability. In the quad-phase configuration, each phase operates 90° out-of-phase so as to minimize the input and output ripple. Connections between the master and slave are as follows: SYNCOUT of the master connects to FSYNC of the slave, and COMP pins connect together (one COMP network shared between the two).

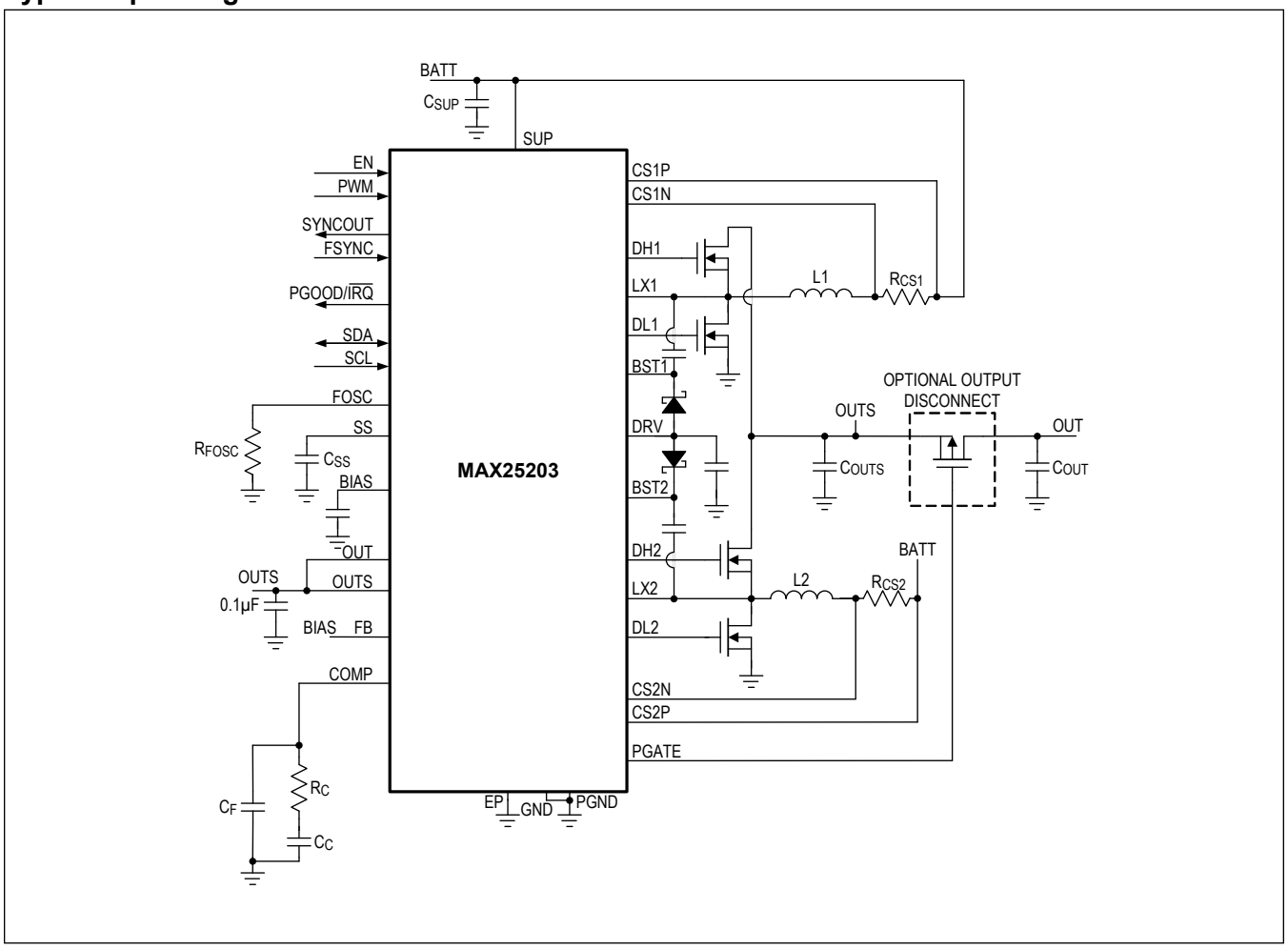
Layout Recommendations

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Layout of the switching power components requires particular attention. Follow these guidelines for good PCB layout:

- Keep high-current paths short, especially at the ground terminals.
- Minimize resistance in high-current paths by keeping the traces short and wide. Using thick (2oz vs. 1oz copper) can improve full load efficiency.
- Connect the CS and SUP connections used for current sensing directly across the sense resistor using a Kelvin sense connection.
- Route noisy switching and clock traces away from sensitive analog areas (FB, CS).

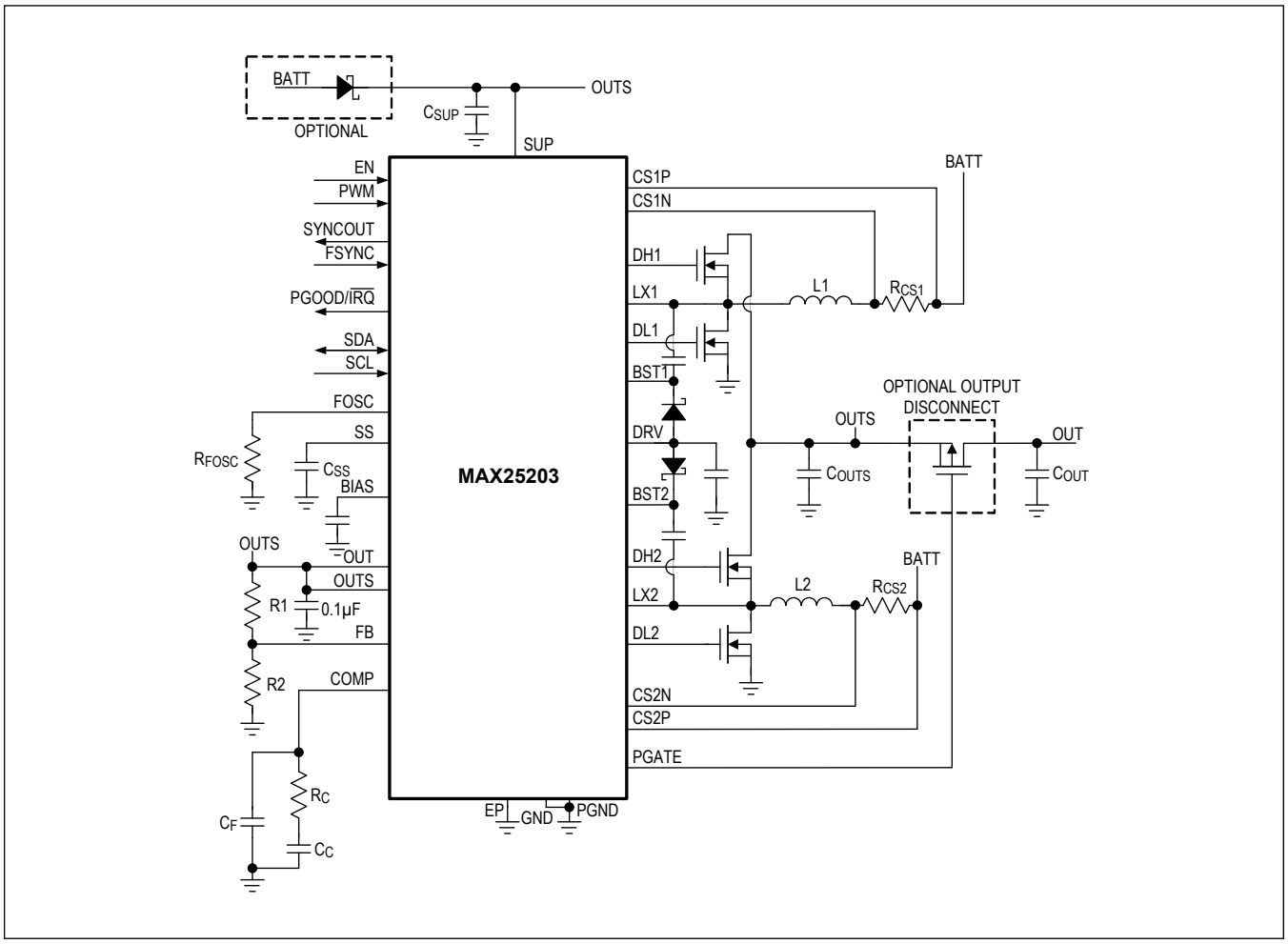
Typical Application Circuits

Typical Operating Circuit



Typical Application Circuits (continued)

Bootstrap Application Circuit



Ordering Information

PART	PIN-PACKAGE	DEFAULT SPREAD SPECTRUM	DEFAULT V_{OUT}	SLAVE ADDRESS W/ R***	CHIP_ID	PGOOD /IRQ	V_{DRV}	PHASES
MAX25203ATJA/VY+	32 SW TQFN-EP*	Off	24V	0xA8/0xA9	0x08	PGOOD	10V	Dual-phase/ quad master
MAX25203ATJB/VY+**	32 SW TQFN-EP*	Off	24V	0xA8/0xA9	0x08	PGOOD	8V	Dual-phase/ quad master
MAX25203ATJC/VY+**	32 SW TQFN-EP*	Off	24V	0xAC/0xAD	0x08	PGOOD	10V	Dual-phase/ quad master
MAX25203ATJD/VY+**	32 SW TQFN-EP*	Off	12V	0xA8/0xA9	0x08	PGOOD	10V	Dual-phase/ quad master
MAX25203ATJE/VY+**	32 SW TQFN-EP*	Off	12V	0xAC/0xAD	0x08	PGOOD	10V	Dual-phase/ quad master
MAX25203BATJA/VY+	32 SW TQFN-EP*	Off	24V	0xA8/0xA9	0x09	PGOOD	6.5V	Dual-phase/ quad master
MAX25203QATJA/VY+	32 SW TQFN-EP*	N/A	N/A	0xAA/0xAB	0x08	N/A	10V	Quad-phase slave

All parts are available in the -40°C to +125°C automotive temperature range.

**EP = Exposed pad.*

***Future product—contact factory for availability.*

****8-bit device address including R/$\overline{W}$ bit.*

/VY Denotes side-wettable automotive qualified parts.

+Denotes a lead (Pb) free/RoHS compliant package.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/21	Initial release	—
1	8/21	Updated Ordering Information	35

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX25203ATJA/VY+T MAX25203BATJA/VY+ MAX25203BATJA/VY+T MAX25203QATJA/VY+ MAX25203QATJA/VY+T