Click here to ask about the production status of specific part numbers.

MAX22000

Industrial Configurable Analog I/O

General Description

The MAX22000 is an industrial-grade configurable analog input/output device that can be configured on-the-fly in software as a voltage input or output, or current input or output. Additional inputs are available to measure other analog signals.

The device offers an 18-bit DAC with fast settling time as well as a 24-bit delta-sigma ADC. The ADC and DAC can individually choose between an internal or an external reference.

The MAX22000 supports the ADC with a low-noise programmable gain amplifier (PGA), with high-voltage and low-voltage input ranges to support RTD and thermocouple measurements. Additional auxiliary inputs are provided to measure cold junction temperatures on-board.

The MAX22000 communicates through a high speed 20MHz SPI bus for all configuration and management information as well as for conversion results. An optional 8-bit CRC enhances the reliability of the SPI interface, protecting against all 8-bit bursts as well as all double-bit errors.

The MAX22000 operates from 2.7V to 3.6V analog and digital supplies and up to \pm 24V high-voltage supplies. The device is available in a 64-pin LGA package and operates over the -40°C to +125°C industrial temperature range.

Applications

- Distributed Control Systems
- Process Control
- Programmable Logic Controllers (PLC)
- Programmable Automation Controllers (PAC)

Benefits and Features

- Accurate
 - · AOVM Mode:
 - 0.02%FSR Accuracy, Room Temp
 - 0.1%FSR Accuracy, ±50°C Temp Variation
 - 5ppm/°C Internal Reference
- Flexible
 - 6 Analog Inputs/1 Analog Output Using Software Configurable Voltage and Current
 - Two Auxiliary ADC Inputs for Cold Junction Measurements
 - RTD Input Mode in 2, 3, or 4-Wire Configurations
 - Thermocouple Input Mode
 - ±12.5V Input/Output Voltage Range
 - ±25mA or ±2.5mA Output Current Range
 - ±25V, ±2.5V, ±500mV, ±250mV, and ±125mV PGA Input Voltage Ranges
 - +24V Field Supply for Current Loop
 - Optional External Reference for ADC and/or DAC
 - Six GPIOs
 - 20MHz SPI Interface
- Robust
 - ±36V Protection on All Analog I/O Ports
 - Overcurrrent Protection
 - Thermal Shutdown
 - Undervoltage Interrupt on All High Voltage Supplies
 - CRC Detection
 - · Open Detection on All Analog Inputs
 - 2kV HBM Protection on All Pins
- -40°C to +125°C Operating Temperature Range
- Small 9mm x 9.5mm 64-Pin LGA Package

<u>Ordering Information</u> and <u>Application Block Diagram</u> appear at end of datasheet.



Industrial Configurable Analog I/O

Functional Block Diagram



Industrial Configurable Analog I/O

Absolute Maximum Ratings

AVDD to AGND	
DVDD to DGND	0.3V to +3.9V
AGND to DGND	0.3V to +0.3V
AGND_DAC to AGND	-0.3V to +0.3V
AGND_DAC to DGND	0.3V to +0.3V
AVDD to REF_DAC_EXT	0.3V to +3.9V
BYP_ADC to DGND	0.3V to +2.1V
HVDD to HVSS	0.3V to +52V
HVDDO to HVSSO	0.3V to +52V
HVDD to AGND	0.3V to +40V
HVDDO to AGND	0.3V to +40V
AGND to HVSS	0.3V to +40V
AGND to HVSSO	0.3V to +40V
HVSSO to HVSS	0.3V to +40V
AI_ to HVSS	0.3V to the lower of +52V or
	((V _{HVDD} -V _{HVSS})+0.3V)
HART_IN, FB to HVSSO	0.3 to the lower of +52V or
	((V _{HVDDO} -V _{HVSSO})+0.3V)

INT to DGND CS, SCLK, SDI, SDO, RDY, RST, SYNC, DGND0.3 to the lower of + REF_ADC, REF_DAC, AUX1, AUX REF_DAC_EXT, NR, REF_OUT, BYP_DA	-0.3V to +6V CLK, LDAC, GPIO_to 3.9V or (V _{DVDD} +0.3V) X2, REF_ADC_EXT, AC to AGND -0.3 to the
lower of +	-3.9V or (V _{AVDD} +0.3V)
AON to HVSS	0.3V to +80V
AOP to HVDDO	70V to +0.3V
AON to HVSSO	0.3V to +70V
Maximum Current into AOP, AON	±100mA
Maximum Current into Any Other Pin	± 50mA
Continuous Power Dissipation (T _A = +70°	C)
64-Pin LGA (derate 42.8mW/°C over T _A	x = +70°C)3418.8mW
Operating Temperature Range	40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

64 LGA

Package Code	L649A9M+1			
Outline Number	<u>21-100274</u>			
Land Pattern Number	<u>90-100096</u>			
Thermal Resistance, Four-Layer Board:				
Junction to Ambient (θ_{JA})	23.4°C/W			
Junction to Case (θ_{JC})	7.0			

For the latest package outline information and land patterns (footprints), go to <u>www.maximintegrated.com/packages</u>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to <u>www.maximintegrated.com/thermal-tutorial</u>.

Industrial Configurable Analog I/O

Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN TYP	MAX	UNITS
ANALOG OUTPUT VOLT	AGE MODE				
		12.5V setting, DAC full-scale range (Note 2)	±12.5		
Output Voltage Range	VOUT	12.5V setting, linear range (Notes 2, 3)	-10.5	+10.5	
		25V setting (Note 2)	+25		
Dropout Voltage		V _{HVDDO} = +13V, sourcing 25mA, measured between HVDDO and AOP, gain compression <1%		0.85	V
biopout voltage		V _{HVDDO} = -13V, sinking 25mA, measured between AON and HVSSO, gain compression <1%		0.85	v
Output Current		Output shorted to HVDDO or HVSSO, threshold current (Note 4)	50		m۵
Protection		Output shorted to HVDDO or HVSSO, average current (Note 4)	13		
AOP, AON High Impedance Leakage Current		Measured at the combined output after the external diodes		±0.5	μΑ
Offset Error	V _{OFF}	T_A = +25°C before calibration		±150	mV
Offset Calibration Range			±12.5		V
Offset Calibration Resolution			95		μV
Offset Drift		$T_A = +50^{\circ}C \pm 50^{\circ}C$ with internal reference (Note 5)	±18		μV/°C
Gain Error		T_A = +25°C before calibration	0	4	%
Gain Calibration Range			0 to 100		%
Gain Calibration Resolution			4		ppm
Gain Drift		$T_A = +50^{\circ}C \pm 50^{\circ}C$ with internal reference (Note 5)	±3.3		ppm/°C
INL Error	INL	T _A = +25°C		±300	μV
INL Drift		$T_{A} = +50^{\circ}C \pm 50^{\circ}C$ (Note 5)	±3		µV/°C
Output Noise	V _N	10kHz bandwidth	85		μV _{RMS}
Supply Rejection Ratio	PSPR	DC, 12.5V setting, V_{OUT} = 0V, V_{HVDD} = V_{HVDDO} = +5V to +24V	120		dB
		DC, 12.5V setting, V _{OUT} = 0V, V _{HVSS} = V _{HVSSO} = -24V to -5V	115		
Load Regulation		-10mA \leq I _{LOAD} \leq +10mA, measured at V _{OUT} = -10.5V and V _{OUT} = +10.5V, output change due to self-heating excluded	±0.1		mV

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AI3 Headroom		From V _{HVSS} (Note 3)	2.5			V
		From V _{HVDD} (Note 3)	2.5			
AI3 Input Current		(Note 5)			±20	nA
Settling Time		12.5V setting, resistive load from $1k\Omega$ to 10M Ω ; settling to 1% for V _{OUT} = 0V to +10.5V or 0V to -10.5V		0.2		me
		12.5V setting, capacitive load up to 1µF; settling to 1% for V _{OUT} = 0V to +10.5V or 0V to -10.5V		1		115
Bandwidth of 25V Setting		-3dB bandwidth from HART_IN to output, 25V setting, load as depicted in Figure 3		10		kHz
ANALOG OUTPUT CUR	RENT MODE					
		25mA setting, R_{SENSE} = 50Ω, DAC full- scale range (Note 6)		±25		
Output Current Bango		25mA setting, R_{SENSE} = 50Ω, linear range (Notes 3,6)	-21		+21	
Output Current Range	OUT	2.5mA setting, R_{SENSE} = 50 Ω , DAC full- scale range (Note 6)		±2.5		
		2.5mA setting, R_{SENSE} = 50 Ω , linear range (Notes 3, 6)	-2.1		+2.1	
Dropout Voltage		Sourcing 25mA, measured between HVDDO and AOP, gain compression <1%			0.85	V
		Sinking 25mA, measured between AON and HVSSO, gain compression <1%			0.85	
Offect Error	1	25mA setting, $T_A = +25^{\circ}C$ before calibration			±300	
Oliset Elloi	OFF	2.5mA setting, $T_A = +25^{\circ}C$ before calibration			±30	μA
Offset Calibration Range		25mA setting		±25		mΔ
Onset Calibration Range		2.5mA setting		±2.5		
Offset Calibration		25mA setting		200		n۸
Resolution		2.5mA setting		20		
Offset Drift		25mA setting, $T_A = +50^{\circ}C \pm 50^{\circ}C$ with internal reference (Note 5)		±36		nA/°C
		2.5mA setting, $T_A = +50^{\circ}C \pm 50^{\circ}C$, with internal reference (Note 5)		±4		
Gain Error		25mA setting, $T_A = +25^{\circ}C$ before calibration	0		4	%
Gain Calibration Range		All settings		0 to 100		%
Gain Calibration Resolution		All settings		4		ppm

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain Drift		25mA setting, $T_A = +50^{\circ}C \pm 50^{\circ}C$, with internal reference (Note 5)		±3.2		ppm/°C
INL Error	INL	25mA setting, T _A = +25°C			±600	nA
INL Drift		25mA setting, $T_A = +50^{\circ}C \pm 50^{\circ}C$ (Note 5)		±6		nA/°C
Output Noice	L.,	25mA setting, 10kHz bandwidth		270		nA _{RMS}
	I IN	2.5mA setting, 10Hz bandwidth		25		nA _{p-p}
Supply Dejection	DeD	DC, 25mA setting, V _{HVDD} = V _{HVDDO} = +5V to +24V		10		5 40/
	For	DC, 25mA setting, V _{HVSS} = V _{HVSSO} = -24V to -5V		10		
		From V _{HVSS} (Note 3)	2.5			V
AIT, AIZ Headroom		From V _{HVDD} (Note 3)	2.5			
AI1, AI2 Input Current		(Note 5)			±20	nA
Common-Mode Rejection	CMR	Al1, Al2 in CSA mode, V(Al1) = V(Al2) = V_{CM} , V_{CM} = -16V to +16V			0.5	μA/V
AI1 and AI2 Differential Input Range		AI1, AI2 in CSA mode		±1.25		V
AI1 and AI2 Differential Input Impedance		AI1, AI2 in CSA mode		100		MΩ
		Resistive load up to 250Ω ; settling to 1% for I _{OUT} = 0mA to +21mA or 0mA to -21mA		0.5		
Settling Time		Resistive load up to 750Ω ; settling to 1% for I _{OUT} = 0mA to +21mA or 0mA to -21mA		1.0		ms
		Inductive load up to 1mH; settling to 1% for I _{OUT} = 0mA to +21mA or 0mA to -21mA		0.5		
ANALOG INPUT VOLTA	GE MODE (AI1 1	FO AI4)				
Headroom		From V _{HVSS} (Note 3)	2.5			V
neaurooni		From V _{HVDD} (Note 3)	2.5			v
Input Voltage Pange	Mari	ADC full-scale range		±12.5		V
Input voltage Range	۷IN	Linear range (Note 3)	-10.5		+10.5	v
Offset Error	V _{OFF}	Before calibration			±25	mV
Offset Calibration Range				±12.5		V
Offset Calibration Resolution				3		μV
Offset Drift		$T_A = +50^{\circ}C \pm 50^{\circ}C$ with internal reference (Note 5)		±12		µV/°C
Gain Error		Before calibration			±4	%

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain Calibration Range				0 to 200		%
Gain Calibration Resolution				0.1		ppm
Gain Drift		$T_A = +50^{\circ}C \pm 50^{\circ}C$ with internal reference (Note 5)		±2.2		ppm/°C
INL Error	INL	T _A = +25°C			±600	μV
INL Drift		$T_{A} = +50^{\circ}C \pm 50^{\circ}C$ (Note 5)		±2.4		μV/°C
Input Voltage Noise	V _N	ADC sample rate is 57.6ksps, ADC mode is Continuous		85		μV _{RMS}
Input Current		(Note 5)			±20	nA
Supply Rejection Patio	DCDD	DC, V_{HVDD} = +5V to +24V		100		dB
	FORK	DC, V_{HVSS} = -24V to -5V		100		UD
50/60Hz Normal Mode		DCHNL_RATE[3:0] = 0010, 0011, 0100, 0101	87			dB
Rejection		DCHNL_RATE[3:0] = 0000, 0001	75			
Open/Short Detector		From any AI1 through AI6 to HVDD		2		MO
Resistance		From any AI1 through AI6 to AGND		2		10122
Settling Time		V _{IN} changes from 0V to +10.5V or 0V to -10.5V, digital output reaches 1% of final value, ADC sample rate is 57.6ksps, ADC mode is Continuous		100		μs
ANALOG INPUT VOLTA	GE MODE – PG	A (AI5, AI6)				
Headroom		From V _{HVSS} (Note 3)	2.5			V
neauloon		From V _{HVDD} (Note 3)	2.5			V
		25V setting, ADC full-scale range		±25		
		25V setting, linear range (Note 3)	-21		21	
		2.5V setting, ADC full-scale range		±2.5		v
		2.5V setting, linear range (Note 3)	-2.1		+2.1	
Input Voltage Pange	Max	500mV setting, ADC full-scale range		±500		
Input voltage Range	V IN	500mV setting, linear range (Note 3)	-420		+420	
		250mV setting, ADC full-scale range		±250		mV
		250mV setting, linear range (Note 3)	-210		+210	
		125mV setting, ADC full-scale range		±125		
		125mV setting, linear range (Note 3)	-105		+105	

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN TYP	MAX	UNITS
		25V setting, $T_A = +25^{\circ}C$ before calibration		±25	mV
		2.5V setting, $T_A = +25^{\circ}C$ before calibration	±300		
Offset Error	V _{OFF}	500mV setting, $T_A = +25^{\circ}C$ before calibration		±500	
		250mV setting, $T_A = +25^{\circ}C$ before calibration	±30		μν
		125mV setting, T _A = +25°C before calibration	±15		
		25V setting	±25		V
		2.5V setting	±2500		
Offset Calibration Range		500mV setting	±500		/
		250mV setting	±250		
		125mV setting	±125		
		25V setting	6		
		2.5V setting	0.6		
Offset Calibration		500mV setting	0.12		μV
Resolution		250mV setting	0.06		1
		125mV setting	0.03		
		25V setting, $T_A = +50^{\circ}C \pm 50^{\circ}C$ with internal reference (Note 5)	±12		µV/°C
Oliset Dhit		500mV setting, $T_A = +50^{\circ}C \pm 50^{\circ}C$ with internal reference (Note 5)	±600		nV/°C
Gain Error		All voltage settings, $T_A = +25^{\circ}C$ before calibration		±4	%
Gain Calibration Range			0 to 200		%
Gain Calibration Resolution			0.1		ppm
		25V setting, $T_A = +50^{\circ}C \pm 50^{\circ}C$ with internal reference (Note 5)	±2.2		/°C
Gain Drift		All other voltage settings, $T_A = +50^{\circ}C \pm 50^{\circ}C$ with internal reference (Note 5)	±1.1		ppm/ C
	INU	25V setting, T _A = +25°C		±600	μV
		500mV setting, $T_A = +25^{\circ}C$		±170	μV
		25V setting, $T_A = 25^{\circ}C \pm 50^{\circ}C$ (Note 5)	±35		µV/°C
INL Drift		500mV setting, $T_A = +50^{\circ}C \pm 50^{\circ}C$ (Note 5)	±3.5		µV/°C

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
	Max	25V setting, ADC sample rate is 57.6ksps, ADC mode is Continuous		85		μV _{RMS}
input voltage Noise	VN	500mV setting, ADC sample rate is 900sps, ADC mode is Continuous		4		μV _{P-P}
Input Common Mode		25V setting, guaranteed by CMRR (Note 7)	-6.25		+6.25	N
Range		All other voltage settings, guaranteed by CMRR (Note 7)	-1.25		+1.25	
		25V setting, V_{CM} = -6.25V to +6.25V	60			
Common Mode	CMRR	2.5V setting, V_{CM} = -1.25V to +1.25V	80			dB
Rejection Ratio		All other voltage settings, V_{CM} = -1.25V to +1.25V	92			
Supply Rejection Patio	DODD	DC, V_{HVDD} = +5V to +24V		100		dB
	FSKK	DC, V _{HVSS} = -24V to -5V		100		uВ
50/60Hz Normal Mode		DCHNL_RATE[3:0] = 0010, 0011, 0100, 0101	87			dB
Rejection		DCHNL_RATE[3:0] = 0000, 0001	75			
Input Current		(Note 5)			±20	nA
Settling Time		25V setting, V _{IN} changes from 0V to +21V or 0V to -21V, digital output reaches 1% of final value, ADC sample rate is 57.6ksps, ADC mode is Continuous		100		
		500mV setting, V _{IN} changes from 0V to +420mV or 0V to -420mV, digital output reaches 1% of final value, ADC sample rate is 57.6ksps, ADC mode is Continuous		100		μσ
AMPLIFIER INPUTS (HA	RT_IN, FB)	1				
Input Bias Voltage				±2.5		V
AUX INPUTS (AUX1, AU	X2)	1				
Headroom		From V _{HVSS} (Note 3)	2.5			v
		From V _{HVDD} (Note 3)	2.5			•
Input Voltage Range	Vin	ADC linear range, single-ended (Note 3)		+0.1 to +2.4		
	* 111	ADC linear range, differential (Note 3)		-2.3 to +2.3		
Offset Error	V _{OFF}	TA = +25°C before calibration		±0.5	±2.5	mV
Offset Calibration Range		Single-ended		0 to 2.5		v
		Differential		±2.5		
Offset Calibration Resolution				0.3		μV

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Offset Drift		$T_A = +50^{\circ}C \pm 50^{\circ}C$ with internal reference (Note 5)		±1		µV/°C
Gain Error		T_A = +25°C before calibration			±4	%
Gain Calibration Range				0 to 200		%
Gain Calibration Resolution				0.1		ppm
Gain Drift		$T_A = +50^{\circ}C \pm 50^{\circ}C$, with internal reference (Note 5)		±1		ppm/°C
INL Error	INL	T _A = +25°C		±15	±60	μV
INL Drift		T _A = +50°C ± 50°C (Note 5)		±50		nV/°C
Input Voltage Noise	V _N	ADC sample rate is 57.6ksps, ADC mode is Continuous		8		μV _{RMS}
Supply Dejection Datio	DEDD	DC, V_{HVDD} = +5V to +24V		100		dD
Supply Rejection Ratio	PSKK	DC, V _{HVSS} = -24V to -5V		100		
50/60Hz Normal Mode		DCHNL_RATE[3:0] = 0010, 0011, 0100, 0101	87			dB
Rejection		DCHNL_RATE[3:0] = 0000, 0001	75			
Input Current	I _{IN}	(Note 5)			±20	nA
Settling Time		V _{IN} changes from 0.1V to +2.4V, digital output reaches 1% of final value, ADC sample rate is 57.6ksps, ADC mode is Continuous		100		μs
DAC REFERENCE (REF	_DAC)					
REF_DAC Output Voltage	V _{REF_DAC}	Internal reference		2.5		V
Output Voltage Accuracy		Referred to $V_{REF_{DAC}}$, T_{A} = +25°C	-0.2		+0.2	%
Output Voltage Temperature Coefficient		T _A = -40°C to +125°C (Note 5)		5		ppm/°C
Line Regulation		$2.7V \le V_{AVDD} \le 3.6V$			50	μV/V
REF_DAC Bypass Capacitor				100		pF
REF_DAC_EXT Input Range		External reference		2.5		V
ADC REFERENCE (REF	_ADC)					·
REF_ADC Output Voltage	V _{REF_ADC}	Internal reference		2.5		V
Output Voltage Accuracy		Referred to V_{REF_ADC} , $T_A = +25^{\circ}C$	-0.2		+0.2	%
Output Voltage Temperature Coefficient		$T_{A} = -40^{\circ}C \text{ to } +125^{\circ}C \text{ (Note 5)}$		5		ppm/°C
Line Regulation		$2.7V \le V_{AVDD} \le 3.6V$			250	μV/V

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REF_ADC Bypass Capacitor				4.7		μF
REF_ADC_EXT Input Range		External reference		2.5		V
DIGITAL INPUTS (CS, SO	CLK, SDI, RST, S	SYNC, CLK, LDAC, GPIO0 THROUGH GPI	O5)			
Input Logic Low Voltage	V _{IL}				0.3×V _{DV} DD	V
Input Logic High Voltage	V _{IH}		0.7×V _{DV} DD			V
Input Hysteresis	V _{HYS}			200		mV
Input Leakage Current	l _{IN}		-1		+1	μA
Input Capacitance	C _{IN}			10		pF
DIGITAL OUTPUTS (SDC	D, RDY, INT, GPI	O0 THROUGH GPIO5)				
Output Logic Low Voltage	V _{OL}	I _{SINK} = 4mA			0.4	V
Output Logic High Voltage	V _{OH}	I_{Source} = 4mA, except $\overline{\text{INT}}$	0.9×V _{DV} DD			V
Three-State Leakage Current			-10		+10	μA
Three-State Output Capacitance				10		pF
POWER SUPPLIES						
Analog Supply Voltage	V _{AVDD}		2.7	3.3	3.6	V
Digital Supply Voltage	V _{DVDD}		2.7	3.3	3.6	V
Positive High Voltage Supply	V _{HVDD}		5		28	V
Negative High Voltage Supply	V _{HVSS}		-24		-5	V
High Voltage Supply	V _{HV}	V _{HVDD} - V _{HVSS}	10		48	V
Positive High Voltage Output Supply	V _{HVDDO}		5		28	V
Negative High Voltage Output Supply	V _{HVSSO}		-24		-5	V
High Voltage Output Supply	V _{HVO}	VHVDDO - VHVSSO	10		48	V
DVDD POR Threshold		Voltage rising		1.6		V
HVDD Undervoltage Threshold		Voltage rising		1.5		V

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Supply Quiescent Current		Analog output voltage mode		5.5		
		Analog output current mode		5.5		m۸
	AVDD_Q	Analog inputs AI1-AI6		5.2		IIIA
		Analog inputs and output		8		
		Analog output voltage mode		1.4		
Digital Supply Quiescent		Analog output current mode		1.4		
Current	DVDD_Q	Analog inputs AI1-AI6		2.4		ma
		Analog inputs and output		2.4		
		Analog output voltage mode, no load current		2.3		
High-Voltage Quiescent	IHV Q	Analog output current mode, no load current		3.3		mA
Current		Analog inputs AI1-AI6, AI1-AI6 at AGND		2.8		
		Analog inputs and output, AI1-AI6 at AGND, no load current		3.5		
		Analog output voltage mode, no load current, $V_{HVDD} = V_{HVDDO} = +15V$, $V_{HVSS} = V_{HVSSO} = -15V$		90		
	PQ	Analog output current mode, no load current, $V_{HVDD} = V_{HVDDO} = +15V$, $V_{HVSS} = V_{HVSSO} = -15V$		120		mW
Total Quiescent Power		Analog inputs AI1-AI6, AI1-AI6 at AGND, V _{HVDD} = V _{HVDDO} = +15V, V _{HVSS} = V _{HVSSO} = -15V		110		
		Analog inputs and output, Al1-Al6 at AGND, no load current, V _{HVDD} = V _{HVDDO} = +15V, V _{HVSS} = V _{HVSSO} = -15V		140		
PROTECTION						
Thermal Shutdown Threshold	T _{SHDN}	Temperature rising until device resets		+165		°C
Thermal Warning Threshold	T _{WARN}	Temperature rising until interrupt assertion		+145		°C
Thermal Warning Hysteresis	Twarn_Hys			10		°C
TIMING CHARACTERIST	rics					
	foour	All SPI transactions except analog output DAC register read-back			20	MH-7
	[†] SCLK	Analog output DAC register read-back, registers 0x44 through 0x47			10	111112

Electrical Characteristics (continued)

 $(V_{AVDD} = V_{DVDD} = +2.7V \text{ to } +3.6V, V_{HVDD} = V_{HVDDO} = +18.0V; V_{HVSS} = V_{HVSSO} = -18.0V, T_A = T_{MIN} \text{ to } T_{MAX}, \text{ unless otherwise noted. Typical values are at } V_{AVDD} = V_{DVDD} = 3.3V, V_{HVDD} = V_{HVDDO} = +18.0V, V_{HVSS} = V_{HVSSO} = -18.0V, T_A = +25^{\circ}C.) \text{ (Note 1)}$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCI K Clock Pariod	taa	All SPI transactions except analog output DAC register read-back	50			
SOLK CIOCK Pendu	чСР	Analog output DAC register read-back, registers 0x44 through 0x47	100			115
	t	All SPI transactions except analog output DAC register read-back	13			
	ЧСН	Analog output DAC register read-back for registers 0x44 through 0x47	40			115
SCLK Dules Width Low	4	All SPI transactions except analog output DAC register read-back	20			20
SCER Fuise Width Low	^L CL	Analog output DAC register read-back, registers 0x44 through 0x47	40	ns		
CS Fall Setup Time	t _{CSS0}	CS falling edge to first SCLK rising edge setup time	7			ns
CS Rise Setup Time	t _{CSS1}	CS rising edge to SCLK rising edge setup time	5			ns
CS Fall Hold Time	tCSH0	SCLK rising edge to $\overline{\text{CS}}$ falling edge hold time	0			ns
CS Rise Hold Time	tCSH1	SCLK falling edge to $\overline{\text{CS}}$ rising edge hold time	3			ns
CS Pulse Width High	tcsw	Minimum \overline{CS} pulse width high	150			ns
SDI Setup Time	t _{DS}	SDI setup time to SCLK rising edge	10			ns
SDI Hold Time	t _{DH}	SDI hold time after SCLK rising edge	5			ns
SDO Transition Time	^t DOT	SDO transition valid after SCLK falling edge			20	ns
SDO Hold Time	^t DOH	Output remains valid after falling edge of SCLK	1			ns
SDO Disable Time	tdod	$\overline{\text{CS}}$ rising edge to SDO disable, C _{LOAD} = 20pF			80	ns
ESD AND SURGE PROTECTION						
ESD		Human Body Model, all pins		±2		kV
IEC Surge	V _{SURGE}	IEC 61000-4-5, 1.2/50μs pulse, pins Al1-Al6, 4.75Ω series MELF resistor		±1		kV

Note 1: Maximum and minimum limits are 100% tested at T_A = +25°C, unless otherwise noted. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: The output voltage is measured at the sense voltage input (Al3). The supply voltage must fulfill the input headroom requirements as well as the output amplifier requirements. Assuming that Al1, Al2, and Al3 are connected to the output, Al1 dictates the headroom requirement. Assuming a 25mA load current, a \pm 12.5V output, and a 50 Ω sense resistor, the minimum supply voltage to fulfill the Al1 headroom requirement is the output voltage (V_{OUT}) plus the voltage drop across the sense resistor plus 2.5V, resulting in a supply voltage across the sense resistor. The minimum supply voltage requirement of \pm 16.25V. The minimum supply voltage required for the output, and the dropout voltage. For a 25mA load current, a \pm 12.5V output, a 50 Ω sense resistor, and a diode forward voltage of 750mV, the minimum supply voltage required by the output amplifier is \pm 15.35V. Overall, the minimum supply voltage is \pm 16.25V.

Note 3: Offset error, gain error, INL error, and settling times are only guaranteed in the linear range. The minimum and maximum specification of the linear range and input headroom are guaranteed through offset, gain, and INL error.

Industrial Configurable Analog I/O

- Note 4: The threshold current specifies the typical current that triggers the short circuit protection. The average current that accounts for self heating of the device is significantly smaller due to the duty cycle when OVC_CTRL is set to logic low.
- Note 5: Not production tested. Guaranteed by design and characterization.
- **Note 6:** The supply voltage must fulfill the Al1 and Al2 headroom requirements as well as the output amplifier requirements. The minimum supply voltage required to fulfill the Al1 and Al2 headroom is 2.5V plus the output current times the sum of the load and cable resistances, and the voltage across the sense resistor. The minimum supply voltage required for the output amplifier is the output current times the sum of the load and cable resistances, the voltage across the sense resistor, the diode forward voltage, and the dropout voltage. For a 25mA output current, a load resistor of 500Ω, a cable resistance of 250Ω, a 50Ω sense resistor, and a diode forward voltage of 750mV, the minimum headroom for Al1 and Al2 requires a supply voltage is ±22.5V, while the supply voltage required by the output amplifier is ±21.6V. Overall, the minimum supply voltage is ±22.5V.
- **Note 7:** The maximum allowed input common-mode range depends on the signal amplitude. The minimum and maximum values given in the <u>Electrical Characteristics</u> table apply to the maximum signal amplitude allowed for a given setting. Refer to the <u>PGA</u> <u>Input Common-Mode Range</u> section for the allowed input common-mode range for smaller signal amplitudes.



Figure 1. SPI Write Timing (N=24 when CRC is Disabled, N=32 when CRC is Enabled)



Figure 2. SPI Read Timing (N = 24 when CRC is Disabled, N = 32 when CRC is Enabled)

Industrial Configurable Analog I/O



Typical Operating Characteristics

0

TIME (ms)

0

DAC CODE STRAIGHT BINARY (decimal)

Industrial Configurable Analog I/O



Typical Operating Characteristics (continued)

UNIT (SAMPLE SIZE)

UNIT (SAMPLE SIZE)

Industrial Configurable Analog I/O

Typical Operating Characteristics (continued)















Industrial Configurable Analog I/O

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	HVDDO	Positive High-Voltage Supply for the Output Path. Bypass to AGND with a minimum $1\mu F$ ceramic capacitor as close to the device as possible.
2	AOP	Positive Transmit Output. Connect to the anode of an external diode.
3	AON	Negative Transmit Output. Connect to the cathode of another external diode.
4	HVSSO	Negative High-Voltage Supply for the Output Path. Bypass to AGND with a minimum $1\mu F$ ceramic capacitor as close to the device as possible.

Pin Description (continued)

PIN	NAME	FUNCTION	
5	HVDD	Positive High-Voltage Supply for the Input Paths. Bypass to AGND with a minimum 1µF ceramic capacitor as close to the device as possible.	
6, 19, 24, 27, 28, 54, 62	AGND	Analog Ground	
7	Al1	nalog Input 1. In analog output current mode, the positive input of the current sense feedback implifier. In all other modes, either the positive input of a current sense to the ADC with Al2, or a roltage sense to the ADC.	
8	Al2	Analog Input 2. In analog output current mode, the negative input of the current sense feedback amplifier. In all other modes, either the negative input of a current sense to the ADC with Al1, or a voltage sense to the ADC.	
9	AI3	Analog Input 3. In analog output voltage mode, the input to the voltage sense feedback amplifier. In all other modes, a high-voltage sense to the ADC.	
10	Al4	Analog Input 4. A high-voltage sense to the ADC.	
11	AI5	Analog Input 5. Along with AI6, a positive voltage input of a differential pair to the ADC.	
12, 21, 22	N.C.	Not Connected. Do not connect.	
13	Al6	Analog Input 6. Along with AI5, a negative voltage input of a differential pair to the ADC.	
14	AUX1	Auxiliary Input 1. First of two auxiliary inputs to the ADC.	
15	AUX2	Auxiliary Input 2. Second of two auxiliary inputs to the ADC.	
16	HVSS	Negative High-Voltage Supply for the Input Paths. Bypass to AGND with a minimum 1μ F ceramic capacitor to AGND.	
17	NR	Reference Noise Reduction. Connect a 0.1µF ceramic capacitor to AGND to reduce wideband noise. Leave unconnected if not used.	
18, 23, 53, 59	AVDD	Analog Power Supply. Connect a 2.7V to 3.6V source here. Bypass each pin to AGND with a minimum 1µF ceramic capacitor as close to the device as possible.	
20	REF_OUT	Voltage Reference Output. Bypass to AGND with a minimum 1μ F ceramic capacitor in parallel with a 0.1μ F ceramic capacitor as close to the device as possible.	
25	REF_ADC	ADC Buffered Reference Voltage Output. Bypass to AGND with a minimum 4.7μ F ceramic capacitor as close to the device as possible.	
26	REF_ ADC_EXT	ADC External Voltage Reference Input. If used to supply an external reference, bypass to AGND with a minimum 0.01μ F ceramic capacitor as close to the device as possible. If unused, connect to AGND.	
29	GPIO5	General Purpose Digital Input/Output 5	
30	GPIO4	General Purpose Digital Input/Output 4	
31	GPIO3	General Purpose Digital Input/Output 3	
32	GPIO2	General Purpose Digital Input/Output 2	
33	GPIO1	General Purpose Digital Input/Output 1	
34	GPIO0	General Purpose Digital Input/Output 0	
35, 42, 50, 61	DGND	Digital Ground	
36, 49, 52, 60	DVDD	Digital Power Supply. Connect a 2.7V to 3.6V source here. Bypass each pin to DGND with a minimum 1µF ceramic capacitor as close to the device as possible.	
37	BYP_ADC	ADC Regulator Bypass. Bypass to DGND with a minimum 0.22µF ceramic capacitor.	
38	CLK	External Clock Input (Optional). Use a 7.3728MHz frequency to match internal clock and to meet filter requirements. Connect to DGND if unused.	

Pin Description (continued)

PIN	NAME	FUNCTION
39	SYNC	ADC Synchronization Input. SYNC resets the ADC modulator and digital filters. If used, connect the SYNC pins of multiple MAX22000 in parallel. If unused, connect to DGND.
40	RDY	Data Ready Output. Asserts active low when a new ADC conversion result is available. Reading a sample resets $\overline{\text{RDY}}$ inactive high. $\overline{\text{RDY}}$ is always driven.
41	ĪNT	Interrupt Output. Open Drain, asserts active low. Functionality controlled by registers GEN_INT and GEN_INTEN
43	RST	Reset Input. When asserted active low, reconfigures all registers to their power-on default states, analog output goes high impedance, analog inputs power down, and ADC conversion stops.
44	SDO	SPI Serial Data Output. Three-states when \overline{CS} is inactive high. Connect to SPI MISO signal.
45	SDI	SPI Serial Data Input. Connect to SPI MOSI signal.
46	SCLK	SPI Serial Clock Input. Connect to SPI interface CLK signal.
47	CS	SPI Slave Select Input. The SPI interface responds only when \overline{CS} is active low.
48	LDAC	DAC Load Input. When asserted active low, transfers the contents of the DAC data register and updates the DAC output. LDAC is ignored while RST is active low. Connect to DGND if not used.
51	BYP_DAC	DAC Regulator Bypass. Bypass to DVDD with a minimum 1µF ceramic capacitor.
55, 56	AGND_DAC	DAC Analog Ground.
57	REF_DAC	DAC Buffered Reference Voltage Output. Bypass to AGND with a minimum 100pF ceramic capacitor as close to the device as possible.
58	REF_DAC_E XT	DAC External Voltage Reference Input. If used to supply an external reference, bypass to AGND with a minimum 0.01μ F ceramic capacitor as close to the device as possible. If unused, connect to AGND.
63	HART_IN	Highway Addressable Remote Transducer (HART) Input. Please refer to HART_IN description.
64	FB	Transmit Output Buffer Feedback. Please refer to FB pin description.
EP1 through 5	EP1 through 5	Exposed Pad. Exposed pads are on the bottom of the package. Connect to HVSS. Solder exposed pad area to HVSS with multiple vias for best thermal performance.

Industrial Configurable Analog I/O

Application Block Diagram



Detailed Description

The MAX22000 is an industrial-grade, software configurable analog input/output solution. The device offers one output that can be configured as voltage or current output, and also offers up to six analog inputs that can be configured as voltage or current inputs. Two of the analog inputs are configured as a differential programmable gain amplifier (PGA), allowing for both low- and high-voltage inputs. The other analog inputs are high-voltage single-ended inputs. The transmit path (analog output) and the receive path (analog inputs) are completely independent; thus, can be programmed for different configurations and modes of operation.

The MAX22000 provides a high-performance 18-bit DAC in the transmit path, and a 24-bit delta-sigma ADC in the receive path. A high-performance filter follows the ADC to provide 50Hz/60Hz normal mode rejection at select ADC data rates.

The device includes a high-performance 5ppm/°C (max) voltage reference on-chip. However, external references can optionally be used for either or both of the transmit and the receive path.

Modes of Operation

The MAX22000 provides 5 main modes of operation:

- Analog Output Voltage Mode (AOVM)
- Analog Output Current Mode (AOCM)
- Analog Input Voltage Mode (AIVM)
- Analog Input Current Mode (AICM)
- RTD and TC Modes

Mode selection determines which input ports, Al1 through Al6, are available as spares. Analog input conversion on available ports is independent of analog output activity.

For example, providing an analog output voltage requires only the use of Al3 for voltage feedback. If the application only needs this mode, all the other input channels are available for other uses, including the use of Al1 and Al2 as a current sense amplifier (CSA). Providing an analog output current reserves both Al1 and Al2 for current feedback. In this case, the resistor across Al1 and Al2 should be 50Ω . Al1 and Al2 can also report current when providing an analog output voltage. Here, a 50Ω resistor results in a ±25mA current measurement range.

Current measurement using AI5 and AI6 of the MAX22000 relies on an external precision resistor to effect current-tovoltage conversion. For current measurements not using differential sense, a GPIO pin can control an external analog switch to connect or disconnect the current sense resistor electronically.

Alternatively, an application requiring all 4 main modes of operation leaves only Al4, Al5, and Al6 for general use.

Besides their use as general purpose analog inputs, AI5 and AI6 can also be configured as a differential programmable gain amplifier (PGA) for either low-voltage or high-voltage inputs.

Regardless of mode of operation, ports AUX1 and AUX2 are always available for cold junction measurements.

The MAX22000 implements a safety switch, activated by the LINE_CNFG bit in the GEN_CNFG register, ensuring a feedback path whether in a 2-wire, 3-wire, or 4-wire configuration.

Input and Output Range Settings

To maintain the best accuracy, the MAX22000 provides multiple voltage and current ranges for its inputs and outputs.

<u>Table 1</u> summarizes available ranges. From narrowest to widest, the nominal range specifies the range for the intended application. The linear range encompasses the nominal range, where performance specifications such as gain error, offset error, INL, PSRR, and CMRR are still guaranteed. Even wider, the full-scale range defines the conversion limits of the data converters. This extended range guards against clipping of signals significantly beyond the nominal range of the application.

The MAX22000 sets the linear range at 105% of the nominal range, and the full-scale range at 125% of the nominal range. For example, for a \pm 10V nominal range, the MAX22000 provides a linear range of \pm 10.5V and a full-scale range of \pm 12.5V.

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To provide other ranges, manage the codes in the digital domain. For example, for applications providing a \pm 5V range, limit the provided DAC code range between negative half-scale and positive half-scale, and double the received ADC code while using \pm 10V calibration coefficients.

Table 1. Input and Output Ranges

MODE	SETTING	NOMINAL	LINEAR	FULL-SCALE
	±12.5V	±10.0V	±10.5V	±12.5V
AOVIM	+25V	N/A	N/A	+12.5V to +37.5V
	±25mA	±20mA	±21mA	±25mA
AUCIVI	±2.5mA	±2.0mA	±2.1mA	±2.5mA
AIVM	±25V (differential)	±20.0V	±21.0V	±25V
	±12.5V (single-ended)	±10.0V	±10.5V	±12.5V
	±2.5V (differential)	±2.0V	±2.1V	±2.5V
	±500mV (differential)	±400mV	±420mV	±500mV
	±250mV (differential)	±200mV	±210mV	±250mV
	±125mV (differential)	±100mV	±105mV	±125mV

PGA Input Common-Mode Range

If the signal amplitude into the PGA is known to be less than its selected full-scale range, the MAX22000 allows a greater input common-mode range than specified in the *Electrical Characteristics* tables.

For the 25V, 2.5V, 500mV, 250mV, and 125mV settings, the maximum allowed input common-mode range is calculated as follows:

$$V_{\rm CM} = V_{\rm REF} - V_{\rm PEAK} \times \frac{A}{2}$$

where,

V_{CM} = Maximum input in common-mode range

V_{REF} = Reference voltage (2.5V)

V_{PEAK} = Peak input voltage

A = Gain constant as per <u>Table 2</u>

For the 12.5V input range, the maximum input common-mode range is:

$$V_{\rm CM} = 5V_{\rm REF} - \frac{V_{\rm PEAK}}{2}$$

Table 2. Gain Setting for Various Input Voltage Ranges

INPUT	GAIN (A)
25V	1
2.5V	1
500mV	5
250mV	10
125mV	20

Analog Output Setting

<u>Table 3</u> summarizes settling performance in AOVM and AOCM modes. Settling time is defined as the time for the output to reach 1% error in response to a step of 105% of the linear range.

AOVM 25V mode setting specifies bandwidth instead, using the load circuit shown in Figure 3.

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······································				
ANALOG OUTPUT MODE	LOAD TYPE	MIN LOAD	MAX LOAD	SETTLING TIME
AOVM, 12.5V Setting	Resistive	1kΩ	10MΩ	0.1ms
	Capacitive	0µF	1µF	1.0ms
	Resistive	0Ω	250Ω	0.5ms
AOCM	Resistive	0Ω	750Ω	1.0ms
	Inductive	0mH	1mH	0.5ms

Table 3. Settling Time for Various Load Conditions



Figure 3. Load Condition for AOVM, 25V Setting

Analog Output Short-Circuit Protection

The MAX22000 provides output short-circuit protection in AOVM mode, responding to possible output overcurrent conditions in one of two ways, selectable using the OVC_CTRL bit in the GEN_CNFG register. In automatic mode, the output goes high impedance when an overcurrent condition is detected, and retries for about 300µs every 6ms until the overcurrent condition ends.

Alternatively, in host controlled mode, the output goes high-impedance and resets bits AO_CNFG[3:0] to 0b0000. The output remains high-impedance until the user writes bits AO_CNFG[3:0] with a code for a proper output configuration.

Regardless of overcurrent mode, the OVC_INT interrupt bit (in the GEN_INT register) asserts high to indicate overcurrent detection. In automatic mode, the OVC_INT bit automatically deasserts low once the MAX22000 senses that the overcurrent condition ends.

The 300 μ s dwell time ensures that completely discharged capacitive loads up to 1 μ F, charging to ±10V do not falsely trigger an overcurrent condition in AOVM mode

Power-On Reset

The AVDD and DVDD supplies are monitored by power on reset circuitry. The MAX22000 is held in a reset state until the AVDD and DVDD supplies have reached a certain threshold that allows safe operation without loss of data. Once this threshold is exceeded, the SPI interface and low-voltage circuitry is fully functional. The high-voltage supplies are also constantly monitored. The MAX22000 needs only the AVDD and DVDD supplies to communicate over the SPI interface. With AVDD and DVDD powered, loss of any high voltage supply is reported through the HVDD_INT and the HVDDO_INT bits in the GEN_INT register.

SPI Interface

An SPI interface allows communication of all important information between a microprocessor and the MAX22000.

An optional CRC enhances confidence in the data communicated to and from the MAX22000. This feature, disabled by default after hardware reset or power-up (but not a software reset), can be enabled or disabled at any time through the SPI interface. When enabled, it affects both read and write SPI transactions.

All SPI transactions without CRC are 4 bytes long. When CRC is enabled, all SPI transactions become 5 bytes long.

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For an SPI write transaction, the host appends a correct CRC, calculated from the 4 bytes of that SPI transaction. The MAX22000 checks the CRC and flags a CRC error should there be a mismatch.

During an SPI read transaction, the MAX22000 expects no CRC, so does not check for one. The MAX22000 appends a correct CRC, calculated from the first byte sent from the host (the address and R/W bit), followed by the 3 bytes of register content. It is up to the host to check the validity of this returned CRC.

SPI command format consists of a 7-bit register address, followed by a read/write bit, followed by 24 bits of data to read from or write to the register specified. The two possible SPI transaction formats are shown in <u>Table 4</u> and <u>Table 5</u>.

When enabled, the CRC uses a polynomial based on 0x31 (x8 + x5 + x4 + x0). This CRC has the following properties:

- detects all errors involving an odd number of bits
- detects all double-bit errors
- detects an error burst of up to 8 bits
- calculates and checks the CRC based on the 32-bits that would have been sent were the CRC not enabled

Refer to AN27 for more details at: https://www.maximintegrated.com/en/app-notes/index.mvp/id/27.

CRC code parameters:

- Width = 8
- Polynomial = 0x31
- Input XOR = 0x00
- Output XOR = 0x00
- Input Reflected = True
- Output Reflected = True

CRC write example: To write 0x00_0F00 to register GEN_ CHNL_CTRL, the SPI transaction from the host would be 0x06_000F_0011.

CRC read transaction example: To read the default value from register GEN_CNFG, the SPI transaction from the host would be 0x05_XXXX_XXXX. The returned value from the MAX22000 would be 0x05_1000_00CB.

Table 4. SPI Transaction Format with CRC Disabled

BITS 31:25	BIT 24	BITS 23:0
Register Address	R/W	24-bit Payload

Table 5. SPI Transaction Format with CRC Enabled

BITS 39:33	BIT 32	BITS 31:8	BITS 7:0
Register Address	R/W	24-bit Payload	CRC

Product Tracking

The MAX22000 includes a 32-bit device tracking number, unique to each device manufactured, accessible through the SPI interface.

Besides tracking individual ICs, this feature can also enable tracking of individual products incorporating the MAX22000.

Analog Output DAC

The analog output is driven by a high accuracy 18-bit, serial SPI input, digital-to-analog converter (DAC).

At power-up, the output is set to high-impedance. If subsequently programmed to switch to AOVM mode, the output goes to approximately 0V. If subsequently programmed to switch to AOCM mode, the output goes to approximately 0mA.

One of the settings, the +25V mode, is meant to support HART or to source power for a 4mA–20mA sensor. As described later, the MAX22000 supports either a signal from a HART modem through the HART_IN pin, or the DAC can generate HART modulation directly through the firmware.

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Output Correction

To ease system calibration, the MAX22000 corrects DAC codes with an 18-bit gain and an 18-bit offset adjustment, as shown in Figure 4.



Figure 4. Gain and Offset Adjustment

The DAC code written to AO_DATA_W (in the AO_DATA_ WR register) is a signed two's complement value. Thus, a code of 0x00000 results in a nominal zero voltage or current, a code of 0x20000 results in the most negative voltage or current, and a code of 0x1FFFF results in the most positive voltage or current output. Details about the code-to-output mapping can be seen in <u>Table 6</u>.

Though AO_DATA_W is always interpreted as a signed two's complement value, the 25V mode adds a fixed 25V offset to the analog output, effectively making it positive-only. In the 25V mode case, programmed voltages might be restricted due to HVDDO headroom restrictions.

The gain coefficient, AO_GAIN_W, is always an unsigned 18-bit binary code, representing a gain between 1 LSB, and one unity gain. <u>Table 7</u> summarizes the gain correction range of the MAX22000, where the last columns specify the gain as shown in <u>Figure 4</u>.

The offset coefficient, AO_OFFSET_W, is always a signed two's complement 18-bit code, representing an offset between about positive half-scale and negative half-scale. <u>Table 8</u> summarizes the offset correction range of the MAX22000.

The results of the correction calculations can saturate. Should the correction calculations result in overflow or underflow, the code clips to the appropriate level. For 25V AOVM, the saturation calculations are the same as with ±12.5V AOVM, with an additional 25V offset added after the output voltage is calculated.

Writing to any of the AO_DATA_WR, AO_GAIN_CORR_ WR, or AO_OFFSET_CORR_WR registers results in a recalculation of the corrected output code as shown in <u>Figure 4</u>, and updates the analog output once the calculations have completed.

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MODE SETTING AO_DATA_W **OUTPUT VALUE** 0x20000 12.5V 0x3FFFF 24.9999V +25V 0x00000 25.0V 0x1FFFF 37.4999V AOVM 0x20000 -12.5V 0x3FFFF -95.4µV ±12.5V 0x00000 0V 0x1FFFF 12.4999V 0x20000 -25mA 0x3FFFF -191nA ±25mA 0x00000 0mA 0x1FFFF 24.9998mA AOCM 0x20000 -2.5mA 0x3FFFF -19.1nA ±2.5mA 0x00000 0mA 0x1FFFF 2.49998mA

Table 6. Nominal Output Values vs. Code

Table 7. Gain Range Examples

RANGE	AO_GAIN_W	GAIN	AS A DECIMAL
Minimum Gain	0x00000	1/2 ¹⁸	0.000038
Quarter Gain	0x0FFFF	1/4	0.25
Half Gain	0x1FFFF	1/2	0.50
Three-Quarters Gain	0x2FFFF	3/4	.75
Maximum Gain	0x3FFFF	1	1.00

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MODE	SETTING	AO_DATA_W	OFFSET FRACTION	OUTPUT VALUE
		0x20000	-1	12.5V
	1251/	0x3FFFF	-1 / 131072	24.9999V
	+25V	0x00000	0	25.0V
		0x1FFFF	131071 / 131072	37.4999V
AUVIVI		0x20000	-1	-12.5V
		0x3FFFF	-1 / 131072	-95.4µV
	±12.5V	0x00000	0	0V
		0x1FFFF	131071 / 131072	12.4999V
		0x20000	-1	-25mA
	1.25m	0x3FFFF	-1 / 131072	-191nA
	IZJIIA	0x00000	0	0mA
AOCM		0x1FFFF	131071 / 131072	24.9998mA
AUCIVI		0x20000	-1	-2.5mA
	12 Em A	0x3FFFF	-1 / 131072	-19.1nA
	IZ.SIIIA	0x00000	0	0mA
		0x1FFFF	131071 / 131072	2.49998mA

Table 8. Offset Range Examples

Controlling the Analog Output with LDAC

The LDAC pin controls the latch between the corrected digital code and the DAC, and can help time analog output changes precisely.

If precise timing is not needed, the simplest approach would be to leave LDAC tied permanently low. Writing to AO_DATA_WR, AO_OFFSET_CORR_WR, or AO_ GAIN_CORR_WR starts a correction calculation. The MAX22000 provides a new output once these calculations complete. Likewise, transitioning LDAC from high to low after one of these registers is written, also provides a new output, even if LDAC transitions high again before correction calculations have completed.

For more precise timing control, keep LDAC high, and transition low after correction calculations have completed. The analog output updates coincide with this falling edge. To determine when the calculations have completed, either wait at least 2.5µs after completion of the SPI transaction writing one of the registers specified above, or poll the BUSY bit in the AO_STA_RD register waiting for it to read low.

Conversion Formulas

<u>Table 9</u> collects together in one place, the formulas mapping DAC data, gain, and offset codes to nominal output values. Recall that the calculation in brackets can saturate, so overflows and underflows limit to the maximum and minimum digital codes, respectively.

The MAX22000 limits digital gain correction to 1.0 or below. Commonly, applications need a small gain correction above or below unity. To allow for this, the MAX22000 output driver provides an analog gain of approximately 1.02, allowing for a small correction above 1.0 if needed.

MODE	SETTING	FORMULA
AOVM	+25V	$V_{OUT} = 12.5V \times \left[\frac{AO_DATA_W}{2^{17}} \times \frac{AO_GAIN_W + 1}{2^{18}} + \frac{AO_OFFSET_W}{2^{17}} \right] + 25V$
AOVM	±12.5V	$V_{OUT} = 12.5V \times \left[\frac{AO_DATA_W}{2^{17}} \times \frac{AO_GAIN_W + 1}{2^{18}} + \frac{AO_OFFSET_W}{2^{17}} \right]$
AOCM	±25mA	$I_{OUT} = 25 \text{mA} \times \left[\frac{\text{AO}_{DATA}W}{2^{17}} \times \frac{\text{AO}_{GAIN}W + 1}{2^{18}} + \frac{\text{AO}_{OFFSET}W}{2^{17}}\right]$
AOCM	±2.5mA	$I_{OUT} = 2.5 \text{mA} \times \left[\frac{AO_DATA_W}{2^{17}} \times \frac{AO_GAIN_W + 1}{2^{18}} + \frac{AO_OFFSET_W}{2^{17}} \right]$

Table 9. Converting from DAC Code to Analog Output

Analog Output DAC Ground

As shown in Figure 5, connect both AGND_DAC pins together. Refer remote output loads to this system ground for best performance.



Figure 5. Star Ground Connection

HART (Highway Addressable Remote Transducer) Modulation

The MAX22000 supports HART devices in two ways. First, program a microcontroller to provide DAC samples, through the SPI interface, emulating the 1.2kHz and 2.2kHz sine waves characteristic of HART, following the correct format. Read ADC samples, also through the SPI interface, to demodulate the HART signal and recover the HART data. This technique requires no additional hardware, placing the burden of the HART interface implementation in the digital domain.

Alternatively, use an external HART modem. Couple the output of that modem to the MAX22000 HART_IN pin with a DC blocking network, as shown in <u>Figure 6</u>. Ensure that the high-pass cutoff frequency is approximately 100Hz or below.



Figure 6. HART Connection

In AOVM mode, the gain from the HART_IN pin to the output is five, so a 1V peak-to-peak input results in a 5V peak-to-peak output swing.

In AOCM mode, the transconductance, assuming a 50Ω current sense resistor, is 10mA/V, so a 1V peak-to-peak input results in a 10mA peak-to-peak output swing.

Due to analog output headroom requirements, HVDD and HVDDO must be at least 26.5V. Also, HVSS and HVSSO must be -5V or more negative.



Figure 7. ADC System Calibration Data Flow

Output Driver Compensation

A passive network between the output driver and the FB pin compensates for load variations.

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Figure 8 shows a recommended compensation network offering stable performance over a wide range of resistive and capacitive loads in AOVM mode, and a wide range or resistive and inductive loads in AOCM mode.

Figure 8. Recommended Compensation Network

Analog Input ADC

The MAX22000 features a high-performance, 24-bit delta-sigma analog-to-digital (ADC) converter, achieving exceptional performance while consuming minimal power. This ADC provides a selection of sample rates from 1sps up to 115.2ksps.

The delta-sigma modulator detects overrange conditions. The DOR bit in the DCHNL_STA register reports any such condition should it occur.

Post-conversion digital SINC filters provide better than 75dB 50Hz/60Hz normal mode rejection, and also provide overflow reporting. When an overflow occurs, the code returned is either 0x7FFFFF if positive overflow occurs, or 0x800000 if negative underflow occurs.

The MAX22000 also monitors the analog signals entering the ADC, and reports an overrange condition in bit AOR in the DCHNL_STA register if the input to the ADC exceeds the full-scale range by approximately 120% or more. These conversions can result in nonsaturated digital codes, which might not meet the accuracy specifications in this data sheet.

ADC Clock

The MAX22000 incorporates a highly stable internal oscillator, providing a nominal system clock of 7.3728MHz (8.192MHz x 0.9) for both analog and digital timing. Optionally, and especially to synchronize ADC conversion using the SYNC pin, a highly stable external clock can be provided. Set the EXTCLK bit in the DCHNL_CTRL2 register to 1 to use a clock source provided on the CLK pin. Provide only a 7.3728MHz frequency to meet filter requirements. Connect CLK to DGND if unused and set the EXTCLK bit in DCHNL_CTRL2 register to 0 to select an internal clock source. Refer to the <u>ADC Conversion Synchronization</u> section for further information on use of the SYNC pin.

Analog Inputs

An internal MUX, controlled through the AI_DCHNL_ SEL[3:0] bits in the GEN_CHNL_CTRL register, selects from 11 available sources. Both single-ended and differential sources are available through this MUX, as detailed in <u>Table 13</u>.

For most MUX selections, a minimum voltage results in a converted code of 0x800000, a zero voltage results in a converted code of 0x000000, and a maximum voltage results in a converted code of 0x7FFFFF.

The exception to this are the AUX1 and AUX2 inputs, where an input of zero volts results in a converted code of 0x800000, an input of +1.25V results in a converted code of 0x000000, and an input of +2.5V results in a converted code of 0x7FFFFF.

ADC Operating Modes

The DCHNL_MODE bits in the DCHNL_CMD register control whether ADC conversions occur. By default, at power-up, the ADC is in a standby power-down mode (01b), performing no conversions and minimizing ADC power consumption.

Writing 01b to the DCHNL_MODE bits in the DCHNL_ CMD register powers down the MAX22000 ADC. If the DCHNL_PD bit of the DCHNL_CTRL1 register is set low, then the MAX22000 ADC enters a standby mode, where conversions stop, but the internal LDO and oscillator are still powered, enabling fast startup. If the DCHNL_PD bit is set high, the ADC is reset.

To convert data through the ADC, write 11b to the DCHNL_MODE bits. This triggers either a single conversion or starts a continuous series of conversions, depending on the state of the SCYCLE and CONTSC bits in the DCHNL_CTRL1 register.

Set the DCHNL_MODE bits to 01b before making any changes to ADC operation, including gain or offset corrections.

Select the conversion mode based on conversion latency and MUX usage.

If focusing on a single source of analog data with fast transients, choose continuous conversion mode. Select this mode by setting the SCYCLE bit in the DCHNL_CTRL1 register low before starting conversions. It yields the highest conversion rates possible, up to 115.2ksps. In this mode, depending on the selected conversion rate, received data has an initial filter settling of 5 samples. Refer to <u>Table 10</u> for a menu of conversion rates.

Similar to continuous conversion mode, continuous single-cycle mode provides an on-going stream of samples, but bypasses the filter settling delay. Select this mode by setting the SCYCLE bit high and the CONTSC bit also high (both in the DCHNL_CTRL1 register). It provides continuous conversions with no added latency, bypassing the pipeline delay of continuous conversion mode. Refer to <u>Table 11</u> for a menu of conversion rates.

To provide on-demand conversions, consider single-cycle mode, offering a single no-latency conversion, but otherwise similar to continuous single-cycle mode. Select this mode by setting the SCYCLE bit high and the CONTSC bit low. Refer to <u>Table 12</u> for maximum possible data rates in this mode.

When in either continuous conversion mode or continuous single-cycle mode, halt the conversions by setting the DCHNL_MODE bits in the DCHNL_CMD register to 01b. Changing the MUX selection to a different source (AI_DCHNL_SEL bits in the GEN_CHNL_CTRL register) also halts continuous conversions and switches the ADC to standby.

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DCHNL_RATE [3:0]	DATA RATE (SPS)	DCHNL_RATE [3:0]	DATA RATE (SPS)
0000b	5	1000b	900
0001b	10	1001b	1,800
0010b	15	1010b	3,600
0011b	30	1011b	7,200
0100b	50	1100b	14,400
0101b	60	1101b	28,800
0110b	225	1110b	57,600
0111b	450	1111b	115,200*

Table 10. Data Rate Choices for Continuous Conversion

* Disable all system calibrations to achieve this sampling rate.

Note: Bold represents sampling rates that provide more than 90dB of 50Hz/60Hz normal mode rejection.

Table 11. Data Rate Choices for Continuous Single-Cycle Conversion

DCHNL_RATE	DATA RATE WITH SYSTEM CALIBRATION (SPS)	DATA RATE WITHOUT SYSTEM CALIBRATION (SPS)
0000b	1 (0.9955)	1 (0.9955)
0001b	2.5	2.5
0010b	5	5
0011b	10	10
0100b	12.5	12.5
0101b	15	15
0110b	50	50
0111b	60	60
1000b	150	150
1001b	299	299
1010b	887	892
1011b	1,755	1,776
1100b	2,768	2,818
1101b	5,327	5,519
1110b	9,910	10,593
1111b	17,389	19,609

Note: Bold represents sampling rates that provide more than 90dB of 50Hz/60Hz normal mode rejection.

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DCHNL_RATE	DATA RATE WITH SYSTEM CALIBRATION (SPS)	DATA RATE WITHOUT SYSTEM CALIBRATION (SPS)
0000b	1 (0.9955)	1 (0.9955)
0001b	2.5	2.5
0010b	5	5
0011b	10	10
0100b	12.5	12.5
0101b	15	15
0110b	50	50
0111b	60	60
1000b	150	150
1001b	298	299
1010b	886	891
1011b	1,752	1,772
1100b	2,759	2,810
1101b	5,297	5,486
1110b	9,804	10,473
1111b	17,067	19,200

Table 12. Data Rate Choices for Single-Cycle Conversion

Note: Bold represents sampling rates that provide more than 90dB of 50Hz/60Hz normal mode rejection.

Data Rates

<u>Table 10</u>, <u>Table 11</u>, and <u>Table 12</u> summarize the available sampling rates of the MAX22000. Use the appropriate table depending on the conversion mode selected. In each case, the left-most column of the table indicates what to write to the DCHNL_RATE bits of the DCHNL_CMD register. In all 3 tables, the sampling rates in bold represent those that provide more than 90dB of 50Hz/60Hz normal mode rejection.

To achieve the highest possible sampling rate in <u>Table 10</u>, 115.2ksps in continuous sampling mode, system calibrations must first be disabled by setting both the NOSYSG and the NOSYSO bits in the DCHNL_CTRL2 register to 1. If either of these bits are zero, the sampling rate is instead 57.6ksps. The RATE bits in the DCHNL_STA register do not reflect this.

ADC Data Ready Output (RDY)

The RDY pin indicates the availability of an ADC conversion result. A new conversion result always triggers a falling edge on RDY. A valid read of the DCHNL_DATA register causes a rising edge on RDY if it is low. In continuous conversion mode or continuous single-cycle mode, a new conversion result might become available before the previous one had been read. In this case, the MAX22000 transitions the RDY pin high approximately 0.5µs prior to indicating that new conversion result with a falling edge.

Existing conversion results remain available until about 0.5 μ s before the next conversion result. In continuous mode, \overline{RDY} initially remains high for the first four conversion results, then goes low for the fifth result. Refer to Figure 9 for more detailed \overline{RDY} timing.



Figure 9. RDY Output Timing, a) Single-Cycle Mode, b) Continuous Single-Cycle Mode, c) Continuous Conversion Mode

ADC Conversion Synchronization

The SYNC pin—ideally in conjunction with an external clock—can be used to synchronize the data conversions to external events. Although the synchronization method also works with an internal clock, resynchronization is inevitable due to local oscillators with limited frequency accuracy. A highly stable external clock that can be shared by multiple MAX22000 devices, allows for much longer time intervals without the requirement of resynchronization.

Set bit SYNC_MODE in register DCHNL_CTRL2 to logic high to enable external synchronization mode. Optionally, set bit EXTCLK in register DCHNL_CTRL2 to logic high to use a highly accurate external clock signal.

The synchronization mode is used to detect if the current conversions are synchronized to a continuous pulse signal with a period greater than the data rate. The pulse width of the synchronization signal is not critical, as only the rising edge of the synchronization pulse is used as a timing reference. The pulse width, however, must be longer than 300ns if the internal clock source is used, and longer than twice the clock period if an external clock source is used. In addition, the low time of the SYNC signal between consecutive SYNC pulses must be longer than 300ns if the internal clock source is used, and longer than twice the clock period if an external clock source is used. In addition, the low time of the SYNC signal between consecutive SYNC pulses must be longer than 300ns if the internal clock source is used, and longer than twice the clock period if an external clock source is used. Ideally, the frequency of the synchronization signal is an integer multiple of the conversion rate. The synchronization mode records the number of ADC clock cycles between a falling edge of RDY and the rising edge of the next SYNC pulse. At the following SYNC pulse, the number of ADC clock cycles between a falling edge of RDY and the rising edge of the SYNC pulse is evaluated again and compared to the recorded value. If the new number of ADC clock cycles differs by more than one from the recorded value, the conversion in progress is stopped, the digital filter content is reset, and a new conversion starts. As the digital filter is reset, the full digital filter latency is required before valid results are available. If the new ADC clock count is within the ±1 count limit, the conversions continue uninterrupted.

<u>Figure 10</u> shows the timing relationship between the MAX22000 ADC clock and the SYNC signal. Due to startup delays, any SYNC pulses before the first falling edge of \overline{RDY} are ignored. The first rising edge on the SYNC pin after a falling edge of \overline{RDY} establishes the relationship between the SYNC signal and the conversion timing.



Figure 10. SYNC Input Timing

Analog Input System Calibration

The MAX22000 can eliminate gain and offset errors of the entire analog input signal chain, including board level components as well as internal MAX22000 circuits. The MAX22000 stores unique calibration coefficients for each of the available input channels, as selected by the AI_DCHNL_SEL bits in the GEN_CHNL_CTRL register. This simplifies calibration, as the coefficients need only be loaded once after reset or power-up. The MAX22000 automatically uses the appropriate coefficients on-the-fly. The MAX22000 supports automatic gain and offset correction in hardware for all conversion modes except for continuous conversion at 115,200 samples per second. Before this two-point calibration can take effect, the user must:

- Select two voltages near the application's full-scale maximum and minimum points for each selected channel used.
- Ensure that the calibration parameters for that channel are set to defaults.
- Apply these two voltages to the MAX22000, resulting in two codes.
- Calculate the gain and offset corrections for this channel.
- Format these for the MAX22000 gain and offset correction registers.
- Write these parameters to the appropriate registers, and repeat for any other channels being calibrated.

Select two test voltages near the application maximum and minimum. Supply them from a low noise source, and measure them with an accurate meter.

The MAX22000 employs indirect addressing to provide access to the offset and gain registers associated with each unique input channel. First, write the desired channel to the DCHNL_N_SEL register. Then, access calibration values with reads and writes to the DCHNL_N_SOC register for the offset, and the DCHNL_N_SGC for the gain.

The offset and gain values must be at their defaults when the test voltages are applied. The defaults are 0x000000 for the offset and 0xC00000 for the gain of 1.5. Also, the NOSYSG and the NOSYSO bits in the DCHNL_CTRL2 register must both be at their default 0.

As illustrated in <u>Figure 11</u>, apply two test voltages, perform a conversion on each, and record the returned codes. For V1 and V2, C1 and C2 are obtained.



Figure 11. Definition of Parameters for Two-Point Calibration

Using the appropriate full-scale range voltage in <u>Table 13</u>, calculate the gain and offset as:

$$GAIN = 1.5 \times \frac{V_1 - V_2}{\left(\frac{C_1 - C_2}{2^{23}}\right) \times V_{FS}}$$
$$OFFSET = C_2 - \frac{1.5}{GAIN} \times \frac{V_2}{V_{FS}} \times 2^{23}$$

Since 0xC00000 is a gain of 1.5 our measured gain should be near 1.5. Calculate GAIN x 2^{23} . Write the rounded value of this in the DCHNL_N_SGC register as an unsigned number. For example, A = 1.48 translates to 12,415,139 (BD70A3h) in register DCHNL_N_SGC.

OFFSET is in bits, and can be either positive or negative. Using the appropriate digital gain entry in <u>Table 13</u>, calculate OFFSET/(ADIG x 1.5). Write this value in the DCHNL_N_SOC register as a two's complement number.

DCHNL_N_SGC = GAIN ×
$$2^{23}$$

DCHNL_N_SOC = $\frac{OFFSET}{A_{DIG} \times 1.5}$

The MAX22000 now corrects all further data from this channel using these associated correction parameters.

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AI_DCHNL_SEL[3:0]	INPUT CHANNEL	FULL-SCALE RANGE (V _{FS})	DIGITAL GAIN (A _{DIG})	VALUE FOR ADC CODE 800000h	VALUE FOR ADC CODE 000000h	VALUE FOR ADC CODE 7FFFFFh
0000	None					
0001	AI1 Single Ended	12.5V	+2	-12.5v	0V	+12.5v
0010	AI2 Single Ended	12.5V	-2	-12.5v	0V	+12.5v
0011	AI1:AI2 Differential	1.25V	+2	-1.25v	0V	+1.25v
0100	AI3 Single Ended	12.5V	+2	-12.5v	0V	+12.5v
0101	Al4 Single Ended	12.5V	-2	-12.5v	0V	+12.5v
0110	AI3:AI4 Differential	25.0V	+1	-25.0V	0V	+25.0V
1001	AI5:AI6 Differential	25.0V	+1	-25.0V	0V	+25.0V
1100	AI5:AI6 Differential, AI5_DF_GAIN = 00b	2.5V	+2	-2.5V	0V	+2.5V
1100	AI5:AI6 Differential, AI5_DF_GAIN = 01b	500mV	+2	-500mV	0mV	+500mV
1100	AI5:AI6 Differential, AI5_DF_GAIN = 10b	250mV	+2	-250mV	0mV	+250mV
1100	AI5:AI6 Differential, AI5_DF_GAIN = 11b	125mV	+2	-125mV	0mV	+125mV
1101	AUX1 Single Ended	1.25V	+2	0V	+1.25V	+2.5V
1110	AUX2 Single Ended	1.25V	-2	0V	+1.25V	+2.5V
1111	AUX1:AUX2 Differential	2.5V	+1	-2.5V	0V	+2.5V

Table 13. Input Channel Conversion Parameters

The data channel conversions do not need to be stopped while accessing the offset and gain correction registers. The ADC can be running or stopped. The channel whose correction parameters are being accessed cannot be the same as the channel actively being converted. The data channel keeps converting with one exception. A write to the offset or gain correction registers for a channel currently being converted aborts that conversion. Additionally, if the ADC is in either continuous conversion mode or continuous single-cycle mode, all further conversions are halted as well.

Either offset correction, gain correction, or both can be disabled with the NOSYSG and NOSYSO bits in the DCHNL_CTRL2 register, but these bits are global, and would prohibit calibration for all channels if activated. If gain correction is disabled, the MAX22000 behaves as if DCHNL_SGC is set to 800000h. Note that this is 2/3 of the default gain correction value of C00000h. If offset correction is disabled, the MAX22000 behaves as if DCHNL_SGC is set to 80000h.

000000h.

Auxiliary ADC Inputs

The MAX22000 offers two auxiliary ADC inputs, AUX1 and AUX2. Both inputs can be used either as single-ended inputs with a 0V to 2.5V range, or as differential inputs, with a range of $\pm 2.5V$. Both inputs are high impedance, allowing for a wide range of source impedances without the need for a dedicated input buffer.

ADC Reference

The MAX22000 includes a built-in 2.5V reference, but can use external references under program control. The MAX22000 meets all electrical characteristic specifications using the internal precision reference. An external reference allows, for example, sharing one reference between multiple MAX22000.

ADC Software Reset

A software reset puts the DCHNL_ prefix registers to their default state and resets internal state machines. It does not affect the DAC.

To effect an ADC software reset:

- Write 1 to the DCHNL_PD bit in the DCHNL_CTRL1 register.
- Write 01b to the DCHNL_MODE bits in the DCHNL_CMD register.
- Poll the PDTSAT bits in the DCHNL_STA register until it reads 10b.

Hardware Reset

The MAX22000 features an active-low hardware reset. Pulse \overline{RST} low to reconfigure all registers to their power on state. The analog output goes high impedance, all analog inputs power down, any ADC conversion in progress is stopped, and the digital filters are reset.

Thermal Monitoring and Shutdown

The MAX22000 monitors its own temperature, and provides both a thermal warning and a protective thermal shutdown.

The THWRNG_INT bit is set in the GEN_INT register should the die temperature reach approximately 145°C. This bit remains set until the die temperature drops below approximately 135°C, at which point this bit clears. This high temperature warning condition can be programmed to cause an interrupt assertion on the INT pin.

Should the die temperature exceed approximately 165°C, the THSHDN_INT bit in the GEN_INT register asserts high and the INT pin asserts low, indicating a high temperature shutown condition. Note that thermal shutdown is a non-maskable interrupt. The GEN_CNFG and GEN_CHNL_CTRL registers are reset to their default state, except for the DAC_REF_SEL, the ADC_REF_SEL, and the CRC_EN bits.

Register Map

Note: In the register map the top-most line represents the MSB byte (bits 23-16, the middle line represents the middle byte (bits 15-8), and the bottom line represents the LSB byte (bits 7-0).

ADDRESS	RESET	NAME	MSB							LSB		
GEN Regist	ers											
		<u>GEN_PROD[</u> 23:16]				PROD_	_ID[7:0]					
0x00	0x2D0 000	<u>GEN_PROD[</u> 15:8]				SERIA	L[15:8]					
		<u>GEN_PROD[</u> <u>7:0]</u>				SERIA	AL[7:0]					
		<u>GEN_REV[23</u> :16]				REV_	ID[7:0]					
0x01	0x0000 00	<u>GEN_REV[15</u> :8]				SERIA	L[15:8]					
		<u>GEN_REV[7:</u> 0]				SERIA	AL[7:0]					
		<u>GEN_CNFG[2</u> 3:16]	CRC_EN	DACREF _SEL	ADCREF _SEL	LINE_C NFG		AO_CN	IFG[3:0]			
0x02	0x1000 00	<u>GEN_CNFG[1</u> <u>5:8]</u>	Al	AI1_2_CNFG[2:0] AI3_CNF AI4_CNF G G AI5_6_CNFG[5_6_CNFG[2	2:0]		
		<u>GEN_CNFG[7</u> :0]	AI5_DF_	AI5_DF_GAIN[1:0] Reserved[1:0] OVC_CT RL F					teserved[2:0]			
		GEN_CHNL_ CTRL[23:16]	AI1_TE	EST[1:0]	AI2_TE	ST[1:0]	AI3_TE	ST[1:0]	AI4_TE	ST[1:0]		
0x03	0x0000 00	<u>GEN_CHNL_</u> CTRL[15:8]	AI5_TE	EST[1:0]	AI6_TE	ST[1:0]		AI_DCHNI	L_SEL[3:0]			
		GEN_CHNL_ CTRL[7:0]				Reserv	ved[7:0]					
		<u>GEN_GPIO_</u> CTRL[23:16]	Reserv	/ed[1:0]			GPIO_	EN[5:0]				
0x04	0x0000 00	<u>GEN_GPIO_</u> CTRL[15:8]	Reserv	/ed[1:0]			GPIO_I	DIR[5:0]				
		<u>GEN_GPIO_</u> CTRL[7:0]	Reserv	/ed[1:0]			GPO_D	ATA[5:0]				
		<u>GEN_GPI_IN</u> <u>T[23:16]</u>	Reserv	/ed[1:0]		G	PI_POS_E	DGE_INT[5:	0]			
0x05	0x0000 00	<u>GEN_GPI_IN</u> T[15:8]	Reserved[1:0] GPI_NEG_EDGE_INT[5:0]									
		<u>GEN_GPI_IN</u> <u>T[7:0]</u>		Reserved[7:0]								
0x06	0x0000	<u>GEN_GPI_DA</u> TA[23:16]	Reserv	/ed[1:0]		GPI_	_POS_EDG	E_INT_STA	(5:0]			
UXUO	00	<u>GEN_GPI_DA</u> <u>TA[15:8]</u>	Reserv	/ed[1:0]		GPI_	_NEG_EDG	E_INT_STA	(5:0]			

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ADDRESS	RESET	NAME	MSB							LSB	
		<u>GEN_GPI_DA</u> <u>TA[7:0]</u>	Reserved[1:0] GPI_DATA[5:0]								
		<u>GEN_INT[23:</u> <u>16]</u>				Reserve	ed[14:7]				
0x07	0x0000 00	<u>GEN_INT[15:</u> <u>8]</u>			F	Reserved[6:0)]			PGAOV V_INT	
		GEN_INT[7:0]	HVDD_I NT	HVDDO_ INT	THSHDN _INT	THWRN G_INT	OVC_IN T	CNFG_I NT	CRC_IN T	GPI_INT	
		<u>GEN_INTEN[</u> 23:16]				Reserve	ed[14:7]				
0x08	0x0000 00	<u>GEN_INTEN[</u> <u>15:8]</u>	Reserved[6:0]							PGAOV V_INTE N	
		<u>GEN_INTEN[</u> <u>7:0]</u>	HVDD_I NTEN	HVDDO_ INTEN	Reserve d	THWRN G_INTE N	OVC_IN TEN	CNFG_I NTEN	CRC_IN TEN	GPI_INT EN	
		<u>GEN_PWR_C</u> TRL[23:16]	AODAC_ PD	Reserve d	AODAC_ RST	Reserve d	GEN_PD	Reserve d	GEN_RS T	Reserve d[16]	
0x09	0x0000 00	<u>GEN_PWR_C</u> <u>TRL[15:8]</u>		Reserved[15:8]							
		<u>GEN_PWR_C</u> <u>TRL[7:0]</u>		Reserved[7:0]							
DCHNL Reg	jisters										
		DCHNL_CMD [23:16]	Reserv	Reserved[1:0] DCHNL_MODE[1:0] DCHNL_RATE[3:0]							
0x20	0x1000 00	DCHNL_CMD [15:8]				Reserve	ed[15:8]				
		DCHNL_CMD [7:0]				Reserv	ed[7:0]				
		DCHNL_STA[23:16]				Reserv	ed[8:1]				
0x21	0x0000 08	DCHNL_STA[15:8]	Reserve d[0]	REFDET		Reserv	ed[3:0]		DOR	AOR	
		<u>DCHNL_STA[</u> <u>7:0]</u>		RATE	E[3:0]		PDSTA	AT[1:0]	MSTAT	RDY	
		DCHNL_CTR L1[23:16]	F	Reserved[2:0)]	DCHNL_ PD	Reserv	ed[1:0]	SCYCLE	CONTS C	
0x22	0x0200 00	DCHNL_CTR L1[15:8]	Reserved[15:8]								
		DCHNL_CTR L1[7:0]	Reserved[7:0]								
		DCHNL_CTR L2[23:16]	EXTCLKReserve dSYNC_M ODEReserve dNOSYS GNOSYS NOSYS OReserved[17:16]							d[17:16]	
0x23	0x0000 00	DCHNL_CTR L2[15:8]				Reserve	ed[15:8]				
		DCHNL_CTR L2[7:0]				Reserv	ed[7:0]				

Industrial Configurable Analog I/O

ADDRESS	RESET	NAME	MSB							LSB			
		DCHNL_DAT A[23:16]		DCHNL_DATA[23:16]									
0x24	0x0000 00	<u>DCHNL_DAT</u> <u>A[15:8]</u>		DCHNL_DATA[15:8]									
		<u>DCHNL_DAT</u> <u>A[7:0]</u>				DCHNL_I	DATA[7:0]						
		DCHNL_N_S EL[23:16]				Reserve	d[19:12]						
0x25	0x0000 00	DCHNL_N_S EL[15:8]		Reserved[11:4]									
		DCHNL_N_S EL[7:0]		Reserv	ed[3:0]			DCHNL_N	_SEL[3:0]				
		DCHNL_N_S OC[23:16]				DCHNL_N_	SOC[23:16]						
0x26	0x0000 00	DCHNL_N_S OC[15:8]				DCHNL_N	_SOC[15:8]						
		DCHNL_N_S OC[7:0]		DCHNL_N_SOC[7:0]									
		DCHNL_N_S GC[23:16]		DCHNL_N_SGC[23:16]									
0x27	0xC00 000	<u>DCHNL_N_S</u> <u>GC[15:8]</u>		DCHNL_N_SGC[15:8]									
		<u>DCHNL_N_S</u> <u>GC[7:0]</u>		DCHNL_N_SGC[7:0]									
AO Registe	rs												
		<u>AO_DATA_W</u> <u>R[23:16]</u>				AO_DATA	_W[17:10]						
0x40	0x0000 00	<u>AO_DATA_W</u> <u>R[15:8]</u>				AO_DAT	A_W[9:2]						
		<u>AO_DATA_W</u> <u>R[7:0]</u>	AO_DAT	A_W[1:0]			Reserv	ed[5:0]					
		AO_OFFSET _CORR_WR[23:16]				AO_OFFSE	T_W[17:10]						
0x41	0x0000 00	<u>AO_OFFSET</u> _ <u>CORR_WR[</u> <u>15:8]</u>				AO_OFFS	ET_W[9:2]						
		AO_OFFSET _CORR_WR[7:0]	AO_OFFS	NO_OFFSET_W[1:0] Reserved[5:0]									
		AO_GAIN_C ORR_WR[23: 16]		AO_GAIN_W[17:10]									
0x42	0xFFF FC0	AO_GAIN_C ORR_WR[15: 8]				AO_GAII	N_W[9:2]						
		AO_GAIN_C ORR_WR[7:0]	AO_GAI	N_W[1:0]			Reserv	ed[5:0]					

Industrial Configurable Analog I/O

ADDRESS	RESET	NAME	MSB							LSB			
		AO_CNFG_W R[23:16]		Reserv	ed[3:0]		AO_RB_ EN	Re	eserved[18:1	16]			
0x43	0x0000 00	<u>AO_CNFG_W</u> <u>R[15:8]</u>				Reserve	ed[15:8]						
		AO_CNFG_W R[7:0]				Reserv	red[7:0]						
		<u>AO_DATA_R</u> <u>D[23:16]</u>			Reserv	ed[5:0]			AO_DATA	_R[17:16]			
0x44	0x0000 00	<u>AO_DATA_R</u> <u>D[15:8]</u>				AO_DAT	A_R[15:8]						
		<u>AO_DATA_R</u> <u>D[7:0]</u>				AO_DAT	A_R[7:0]						
		AO_OFFSET _CORR_RD[2 3:16]			Reserv	ed[5:0]			AO_OFFS	SET_R[17: 6]			
0x45	0x0000 00	AO_OFFSET _CORR_RD[1 5:8]	AO_OFFSET_R[15:8]										
		AO_OFFSET _CORR_RD[7 :0]				AO_OFFS	ET_R[7:0]						
		<u>AO_GAIN_C</u> <u>ORR_RD[23:</u> <u>16]</u>			Reserv	ed[5:0]			AO_GAIN	_R[17:16]			
0x46	0x03FF FF	<u>AO_GAIN_C</u> <u>ORR_RD[15:</u> <u>8]</u>				AO_GAI	N_R[15:8]						
		<u>AO_GAIN_C</u> <u>ORR_RD[7:0]</u>				AO_GAI	N_R[7:0]						
		<u>AO_STA_RD[</u> 23:16]	Reserved[10:3]										
0x47	0x0000 00	AO_STA_RD[15:8]	Image: Market state Reserved[2:0] BUSY Reserved[11:8]										
		<u>AO_STA_RD[</u> <u>7:0]</u>				Reserv	ed[7:0]	Reserved[7:0]					

Register Details

GEN_PROD (0x00)

BIT	23	22	21	20	19	18	17	16			
Field		PROD_ID[7:0]									
Reset		0x2D									
Access Type				Read	Only						

Industrial Configurable Analog I/O

BIT	15	14	13	3 12 11 10 9 8								
Field	SERIAL[15:8]											
Reset	0x00											
Access Type		Read Only										
BIT	7	6	5	4	3	2	1	0				
Field		SERIAL[7:0]										
Reset				0x	.00							
Access Type				Read	l Only							
BITFIE	LD	BITS DESCRIPTION										
PROD_ID		23:16	2	2 Channels								
SERIAL		15:0	M	ost significant 16 t	oits of a 32-bit	code unique to	each MAX2200	00				

GEN_REV (0x01)

BIT	23	22	21	20	19	18	17	16				
Field	REV_ID[7:0]											
Reset	0x00											
Access Type		Read Only										
BIT	15	15 14 13 12 11 10 9 8										
Field		SERIAL[15:8]										
Reset		0x00										
Access Type		Read Only										
BIT	7	6	5	4	3	2	1	0				
Field		·		SERIA	L[7:0]							
Reset				0x	00							
Access Type		Read Only										
BITFIE	LD	BITS DESCRIPTION										
REV_ID		23:16	Un	que ID incremen	ted with each o	die revision of t	he MAX22000					
SERIAL		15:0	Lea	st significant 16	bits of a 32-bit	code unique to	each MAX220	00				

GEN_CNFG (0x02)

BIT	23	22	21	20	19	18	17	16	
Field	CRC_EN	DACREF_S EL	ADCREF_S EL	LINE_CNF G	AO_CNFG[3:0]				
Reset	0b0	0b0	0b0	0b1	0b0000				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read				

Industrial Configurable Analog I/O

BIT	15	14	13	12		11	10	9	8	
Field	A	1_2_CNFG[2:	0]	AI3_CNFG	Al4	_CNFG	AI5_6_CNFG[2:0]			
Reset		0b000		0b0		0b0 0b000				
Access Type	Write, Read			Write, Read	Write, Read			Write, Read		
BIT	7	6	5	4		3	2	1	0	
Field	AI5_DF_C	GAIN[1:0]	Reserv	ved[1:0]	OV	C_CTRL		Reserved[2:0]		
Reset	0b	00	0b	00		0		0b000		
Access Type	Write,	Read	Read	l Only	Wri	te, Read	Read Only			
BITFIELD	BITS		DESCRIPT	ION			D	ECODE		
CRC_EN	23	CRC genera	ator and checke	er enable:		0: CRC 1: CRC	disabled (defau enabled	lt)		
DACREF_SE L	22	DAC referer	DAC reference source:				0: DAC uses built-in voltage reference (default) 1: DAC uses reference provided on pin REF_DAC_EXT			
ADCREF_SE L	21	ADC referer	ADC reference source:				0: ADC uses built-in voltage reference (default) 1: ADC uses reference provided on pin REF_ADC_EXT Note : A write transaction that changes this bit aborts any ADC conversion in progress			
LINE_CNFG	20	Line configu	ration safety sv	witch:		0: Switc 1: Switc a feedba irrespec	 0: Switch between Al2 and Al3 is open 1: Switch between Al2 and Al3 is closed, ensuring a feedback path for analog output feedback, irrespective of the external configuration (default) 			
AO_CNFG	19:16	Analog outp	Analog output configuration:			0000: High Impedance (default) 0001: Analog output voltage mode, 25V setting 0010: Analog output voltage mode, 12.5V settir 0011: Reserved 0100: Reserved 0101: Reserved 0110: Analog output current mode, 25mA settir 0111: Reserved 1000: Analog output current mode, 2.5mA settii 1001 through 1111: Reserved. Do not use (including others not seen). Writing a value in th range leaves the contents of this register unchanged and sets the CNFG_INT bit active h to indicate an invalid write attempt				

Industrial Configurable Analog I/O

BITFIELD	BITS	DESCRIPTION	DECODE			
AI1_2_CNFG	15:13	AI1 and AI2 input configuration:	000: Both Al1 and Al2 powered down (default) 001: Al1 single-ended, Al2 powered down 010: Al1 powered down, Al2 single-ended 011: Both Al1 and Al2 single-ended 100: Al1 and Al2 differential pair (CSA) 101 through 111: Write of these bits ignored, the existing value is left unchanged, and the CNFG_INT bit is set active high to indicate an invalid write attempt Note : Selecting any current output mode in AO_CNFG [3:0] (0b0110 or 0b1000) forces Al2_2_CNFG [2:0] to be set to 0b100, and reads back as 0b100, regardless of what the write transaction specifies for these bits. Additionally, if the write transaction specifies anything other than 0b100, the CNFG_INT bit is set active high to indicate an invalid write attempt			
AI3_CNFG	12	AI3 input configuration:	0: Powered down (default) 1: Single-ended Note : Selecting any voltage output mode in AO_CNFG [3:0] (0b0001 or 0b0010) forces Al3_CNFG to be set to 0b1, and reads back as 0b1, regardless of what the write transaction specifies for this bit. Additionally, if the write transaction specifies anything other than 0b1, the CNFG_INT bit is set active high to indicate an invalid write attempt			
AI4_CNFG	11	Al4 input configuration:	0: Powered down (default) 1: Single-ended			
AI5_6_CNFG	10:8	AI5 and AI6 input configuration:	000: Powered down (default) 001: Reserved 010: Reserved 011: Reserved 100: Al5 and Al6 differential pair (PGA) 101 through 111: Write of these bits ignored, the existing value is left unchanged, and the CNFG_INT bit is set active high to indicate an invalid write attempt			
AI5_DF_GAI N	7:6	AI5 and AI6 differential input voltage range setting:	00: 12.5V setting if AI_DCHNL_SEL [3:0] is 0b1001 (default) 2.5V setting if AI_DCHNL_SEL [3] = 0b1100 (default) 01: 500mV setting 10: 250mV setting 11: 125mV setting			
Reserved	5:4	Reserved				

Industrial Configurable Analog I/O

BITFIELD	BITS	DESCRIPTION	DECODE
OVC_CTRL	3	Over-current response control, AOVM mode only:	 0: Automatic mode: an overcurrent condition sets the output high impedance, and retries every 6ms until the overcurrent condition is removed, after which it automatically returns to the output mode it was in before the overcurrent condition began (default) 1: Host-controlled mode: an overcurrent condition sets the output high impedance and resets the AO_CNFG [3:0] to 0000b; The MAX22000 output then remains high impedance until bits AO_CNFG [3:0] are written with a proper configuration.
Reserved	2:0	Reserved	

GEN_CHNL_CTRL (0x03)

BIT	23	22	21	20	19	18	17	16			
Field	AI1_TE	ST[1:0]	AI2_TE	ST[1:0]	AI3_TE	EST[1:0]	AI4_TEST[1:0]				
Reset	0b	00	0b	00	01	000	0b00				
Access Type	Write,	Read	Write,	Read	Write	, Read	Write,	Read			
BIT	15	14	13	12	11	10	9	8			
Field	AI5_TE	ST[1:0]	AI6_TE	ST[1:0]		AI_DCHNL_SEL[3:0]					
Reset	0b	00	0b	00		0>	k0				
Access Type	Write,	Read	Write,	Read		Write,	Read				
BIT	7	6	5	4	3	2	1	0			
Field	Reserved[7:0]										
Reset	0x00										
Access Type	Read Only										
BITFIELD	BITS		DESCRIPT	ION		DI	ECODE				
AI1_TEST	23:22	Al1 diagnos	tic switches:		00: diag 01: 2M 10: 2M 11: 2M	 00: diagnostic switches disabled (default) 01: 2MΩ resistor to AGND 10: 2MΩ resistor to HVDD 11: 2MΩ resistor each to HVDD and AGND 					
AI2_TEST	21:20	AI2 diagnos	tic switches:		00: diag 01: 2M 10: 2M 11: 2M	 00: diagnostic switches disabled (default) 01: 2MΩ resistor to AGND 10: 2MΩ resistor to HVDD 11: 2MΩ resistor each to HVDD and AGND 					
AI3_TEST	19:18	AI3 diagnos	tic switches:		00: diag 01: 2M 10: 2M 11: 2M	 00: diagnostic switches disabled (default) 01: 2MΩ resistor to AGND 10: 2MΩ resistor to HVDD 11: 2MΩ resistor each to HVDD and AGND 					
AI4_TEST	17:16	Al4 diagnos	tic switches:		00: diag 01: 2M 10: 2M 11: 2M	 00: diagnostic switches disabled (default) 01: 2MΩ resistor to AGND 10: 2MΩ resistor to HVDD 11: 2MΩ resistor each to HVDD and AGND 					

Industrial Configurable Analog I/O

BITFIELD	BITS	DESCRIPTION	DECODE			
AI5_TEST	15:14	AI5 diagnostic switches:	00: diagnostic switches disabled (default) 01: 2MΩ resistor to AGND 10: 2MΩ resistor to HVDD 11: 2MΩ resistor each to HVDD and AGND			
AI6_TEST	13:12	Al6 diagnostic switches:	00: diagnostic switches disabled (default) 01: 2MΩ resistor to AGND 10: 2MΩ resistor to HVDD 11: 2MΩ resistor each to HVDD and AGND			
AI_DCHNL_ SEL	11:8	Analog Input ADC channel selection:	0000: no channel selected (default) 0001: select Al1 single-ended (±12.5V conversion range) 0010: select Al2 single-ended (±12.5V conversion range) 0011: select Al1:Al2 differential (±1.25V conversion range, ±25mA if using a 50Ω resistor) 0100: select Al3 single-ended (±12.5V conversion range) 0101: select Al4 single-ended (±12.5V conversion range) 0110: select Al3:Al4 differential (±25V conversion range) 0111: Reserved 1000: Reserved 1001: Al5:Al6 differential, 12.5V setting (±25V conversion range) 1010: Reserved 1001: Al5:Al6 differential, (±2.5V through ±125mV conversion range) 1101: AUX1 single-ended (0V to +2.5V conversion range) 1111: AUX1 single-ended (0V to +2.5V conversion range) 1111: AUX2 single-ended (0V to +2.5V conversion range) 1111: AUX2 single-ended (0V to +2.5V conversion range) 1111: AUX1:AUX2 differential (±2.5V conversion range) ADC conversion to abort. If not listed: Reserved. Do not use.			
Reserved	7:0	Reserved				

GEN_GPIO_CTRL (0x04)

BIT	23	22	21	20	19	18	17	16		
Field	Reserved[1:0]		GPIO_EN[5:0]							
Reset	0)	k0	0x00							
Access Type	Read	Only	Write, Read							
BIT	15	14	13	12	11	10	9	8		
Field	Reserv	red[1:0]	GPIO_DIR[5:0]							
Reset	0	k0			0x00					
Access Type	Read	Only			Write,	Read				

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Industrial Configurable Analog I/O

BIT	7	6	5	4		3	2	1	0	
Field	Reserv	Reserved[1:0]		GPO_DATA[5:0]						
Reset	0x	(0	0x00							
Access Type	Read	Read Only			Write, Read					
BITFIELD	BITS		DESCRIPTION				D	ECODE		
Reserved	23:22	Reserved	Reserved							
GPIO_EN	21:16	GPIO port e	GPIO port enable control. For each GPIO pin:				0: corresponding GPIO pin disabled (default) 1: corresponding GPIO pin enabled			
Reserved	15:14	Reserved								
GPIO_DIR	13:8	GPIO port d pin:	GPIO port direction control. For each GPIO pin:				0: corresponding GPIO pin configured as an input (GPI) (default) 1: corresponding GPIO pin configured as an output (GPO)			
Reserved	7:6	Reserved								
GPO_DATA	5:0	GPIO data t	a bits for pins configured as outputs:			0: corresponding GPO pin drives a low, nominally DGND (default) 1: corresponding GPO pin drives high, nominally DVDD				

GEN_GPI_INT (0x05)

BIT	23	22	21	20	19	18	17	16		
Field	Reserv	ed[1:0]			GPI_POS_E	DGE_INT[5:0]	•			
Reset	0x	:0	0x00							
Access Type	Read	Only	Write, Read							
BIT	15	14	13	12	11	10	9	8		
Field	Reserv	ed[1:0]			GPI_NEG_E	DGE_INT[5:0]				
Reset	0x	0x0			0:	x00				
Access Type	Read	Read Only			Write	Write, Read				
BIT	7	6	5	4	3	2	1	0		
Field				Reserv	ved[7:0]	•	•			
Reset				0x	.00					
Access Type				Read	l Only					
BITFIELD	BITS		DESCRIPT	ION		D	ECODE			
Reserved	23:22	Reserved								
GPI_POS_E DGE_INT	21:16	Positive edg pins configu	e detection en red as inputs:	ables for GPIO	0: posit corresp 1: posit corresp	0: positive edge detection disabled on corresponding pin (default)1: positive edge detection enabled on corresponding pin				
Reserved	15:14	Reserved								

Industrial Configurable Analog I/O

BITFIELD	BITS	DESCRIPTION	DECODE
GPI_NEG_E DGE_INT	13:8	Negative edge detection enables for GPIO pins configured as inputs:	0: negative edge detection disabled on corresponding pin (default)1: negative edge detection enabled on corresponding pin
Reserved	7:0	Reserved	

GEN_GPI_DATA (0x06)

BIT	23	22	21	20	19	18	17	16			
Field	Reserv	/ed[1:0]	GPI_POS_EDGE_INT_STA[5:0]								
Reset	0x0		0x00								
Access Type	Read Only		Read Clears All								
BIT	15	14	13	12	11	10	9	8			
Field	Reserved[1:0]		GPI_NEG_EDGE_INT_STA[5:0]								
Reset	0x0		0x00								
Access Type	Read	l Only	Read Clears All								
BIT	7	6	5	4	3	2	1	0			
Field	Reserv	ved[1:0]			GPI_DA	ATA[5:0]		•			
Reset	0x0		0x00								
Access Type	Read	l Only		Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	23:22	Reserved	
GPI_POS_E DGE_INT_S TA	21:16	Positive edge detection indication for GPIO pins configured as inputs:	 0: no positive edge was detected on corresponding pin (default) 1: at least one positive edge detected on corresponding pin Note: These bits are cleared upon read
Reserved	15:14	Reserved	
GPI_NEG_E DGE_INT_S TA	13:8	Negative edge detection indication for GPIO pins configured as inputs:	 0: no negative edge was detected on corresponding pin (default) 1: at least one negative edge detected on corresponding pin Note: These bits are cleared upon read
Reserved	7:6	Reserved	
GPI_DATA	5:0	GPI data bits for pins configured as inputs:	0: logic low level detected at corresponding GPI pin 1: logic high level detected at corresponding GPI pin

Industrial Configurable Analog I/O

GEN_INT (0x07)

BIT	23	22	21 20 19 18 17					17	16		
Field				Reserve	ed[14	:7]					
Reset				0x0	000						
Access Type				Read	Only	,					
BIT	15	14	14 13 12 11 10 9						8		
Field		Reserved[6:0]									
Reset		0x0000 0b0									
Access Type				Read Only					Read Only		
BIT	7	6	5	4		3	2	1	0		
Field	HVDD_INT	HVDDO_IN T	THSHDN_I NT	THWRNG_I NT	٥v	/C_INT	CNFG_INT	CRC_INT	GPI_INT		
Reset	0b0	0b0	0b0	0b0		0b0	0b0	0b0	0b0		
Access Type	Read Only	Read Only	Read Clears All	Read Only	Read Clears All		Read Clears All	Read Clears All	Read Only		
BITFIELD	BITS		DESCRIPT	ION			D	ECODE			
Reserved	23:9	Reserved									
PGAOVV_IN T	8	PGA overvo	Itage indicatior	1:		0: voltages at AI5 and AI6 within range 1: voltages at AI5 and/or AI6 are too high, resulting in an out-of-range condition at the output of the PGA Note : When asserted active high, disconnects the inputs from the signal path					
HVDD_INT	7	HVDD/HVS	S undervoltage	indication:		0: HVDD-HVSS voltage above threshold 1: HVDD-HVSS voltage below threshold					
HVDDO_INT	6	HVDDO/HV	SSO undervolt	age indication:		0: HVDDO-HVSSO voltage above threshold 1: HVDDO-HVSSO voltage below threshold					
THSHDN_IN T	5	Thermal shu	Thermal shutdown indication:				0: die temperature low enough to permit normal operation 1: die temperature exceeds approximately 165°C, GEN_CNFG and GEN_CHNL_CTRL registers are cleared to zeroes (except for the CRC_EN, DACREF_SEL, and ADCREF_SEL bits) Note: this bit is cleared upon read				
THWRNG_IN T	4	Thermal war	rning indication	Ľ		0: die temperature within normal range 1: die temperature above approximately 145°C Note : this read-only bit warns of a potential impending thermal shutdown condition, cleared when the temperature drops below approximately 135°C					

Industrial Configurable Analog I/O

BITFIELD	BITS	DESCRIPTION	DECODE
OVC_INT	3	Overcurrent indication on the analog output:	0: current demand within acceptable range 1: current demand exceeds 50mA (typical) Note : The clearing behavior of this bit depends on the setting of the OVC_CTRL bit in the GEN_CNFG register. If OVC_CTRL is set logic low (automatic mode), OVC_INT clears once the overcurrent condition is resolved. If OVC_CTRL is set logic high (host-controlled mode), then OCV_INT clears upon read.
CNFG_INT	2	Configuration error indication:	 0: no configuration error 1: either: - AO_CONFIG is set to a value between 9h and Fh, Al_1_2_CNFG is set to a value between 5h and 0x8h, or Al_5_6_CNFG is set to a value between 0x5 and 0x8; the config bits retain their previous value, and this bit clears upon read of this register - Input buffers required for DAC mode (AO_CONFIG) not powered up; the required buffers are powered up, and the bits in the GEN_CNFG register reflect this; this bit clears on read of this register - Input buffer(s) corresponding to AI_DCHNL_SEL MUX selection not powered up; this bit remains set until the inconsistency is resolved
CRC_INT	1	CRC error detection indication:	0: no CRC error detected 1: CRC error detected Note : this clear-on-read bit never asserts unless the CRC is enabled
gpi_int	0	GPI edge detection indication:	 0: no new specified edges detected since last time this bit was read 1: At least one edge was detected at a GPI-configured pin since the last time this bit was read Note: Bit GPI_INT clears on read, and does not affect the bits in the GPI_GEN_INT register. This bit reasserts upon detection of another selected edge.

GEN_INTEN (0x08)

BIT	23	22	21	20	19	18	17	16			
Field	Reserved[14:7]										
Reset		0x0000									
Access Type		Read Only									
BIT	15	14	13	12	11	10	9	8			
Field				Reserved[6:0]		•		PGAOVV_I NTEN			
Reset	0x0000							0b0			
Access Type	Read Only										

Industrial Configurable Analog I/O

BIT	7	6	5	4		3 2 1 0			0	
Field	HVDD_INT EN	HVDDO_IN TEN	Reserved	THWRNG_I NTEN	OV	/C_INTE CNFG_INT CRC_INTE N EN N		CRC_INTE N	GPI_INTEN	
Reset	0b0	0b0	0b0	0b0		0b0	0b0	0b0	0b0	
Access Type	Write, Read	Write, Read	Read Only	Write, Read	Writ	Write, Read Write, Read Write, Read Write,				
BITFIELD	BITS		DESCRIPT	ION			DI	ECODE		
Reserved	23:9	Reserved								
PGAOVV_IN TEN	8	PGAOVV in	errupt enable:			0: corres pin (defa 1: corres	sponding interro ault) sponding interro	upt cannot asseu	ert the \overline{INT} the \overline{INT} pin	
HVDD_INTE N	7	HVDD interr	upt enable:			0: corresponding interrupt cannot assert the INT pin (default) 1: corresponding interrupt can assert the INT pin			ert the \overline{INT}	
HVDDO_INT EN	6	HVDDO inte	HVDDO interrupt enable:				sponding intern ault) sponding intern	upt cannot asso upt can assert	ert the INT the INT pin	
Reserved	5	Reserved								
THWRNG_IN TEN	4	THWRNG ir	terrupt enable:			 0: corresponding interrupt cannot assert the IN² pin (default) 1: corresponding interrupt can assert the INT pin 			ert the \overline{INT} the \overline{INT} pin	
OVC_INTEN	3	OVC interru	ot enable:			0: corres pin (defa 1: corres	sponding interri ault) sponding interri	upt cannot assoupt can assert	ert the \overline{INT} the \overline{INT} pin	
CNFG_INTE N	2	CNFG interr	CNFG interrupt enable:				sponding interri ault) sponding interri	upt cannot assoupt can assert	ert the \overline{INT} the \overline{INT} pin	
CRC_INTEN	1	CRC interru	O: corresponding interrupt cannot as CRC interrupt enable: pin (default) 1: corresponding interrupt can assert				upt cannot asso upt can assert	ert the INT the INT pin		
GPI_INTEN	0	GPI interrup	t enable:			0: corres pin (defa 1: corres	sponding interriault)	upt cannot asse	ert the \overline{INT}	

GEN_PWR_CTRL (0x09)

BIT	23	22	21	20	19	18	17	16		
Field	AODAC_PD	Reserved	AODAC_RS T	Reserved	GEN_PD	Reserved	GEN_RST	Reserved[1 6]		
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0x00000		
Access Type	Write, Read	Read Only	Write, Read	Read Only	Write, Read	Read Only	Write, Read	Read Only		
BIT	15	14	13	12	11	10	9	8		
Field				Reserve	ed[15:8]		•			
Reset	0x00000									
Access Type	Read Only									

Industrial Configurable Analog I/O

BIT	7	6	5	4	3	3 2 1 0							
Field		Reserved[7:0]											
Reset		0x00000											
Access Type		Read Only											
BITFIELD	BITS		DESCRIPT	ION		D	ECODE						
AODAC_PD	23	DAC power	down control:		0: norm 1: DAC	al operation (de powered down	efault)						
Reserved	22	Reserved											
AODAC_RS T	21	DAC softwa	re reset control	:	0: norm 1: DAC to zero	al operation (de is reset and sta	efault) ays reset until t	his bit is set					
Reserved	20	Reserved											
GEN_PD	19	General pov	0: normal operation 1: powers down all a settings in the GEN_ GEN_CHNL_CTRL subsequently writter to the state defined GEN_CHNL_CTRL and the GEN_CHL_ modifications take e with 0					operation (default) down all amplifiers irrespective of the the GEN_CNFG and the NL_CTRL registers. When GEN_PD is ntly written with 0, returns the MAX22000 te defined by the GEN_CNFG and the NL_CTRL registers. The GEN_CNFG iEN_CHL_CTRL registers can be while GEN_PD is set to 1, and these ons take effect when GEN_PD is written					
Reserved	18	Reserved											
GEN_RST	17	General soft	ware reset cor	itrol:	0: normal operation (default) 1: the GEN_CNFG and the GEN_CHNL_ registers are reset. However, the values of CRC_EN, DACREF_SEL, and ADC_REF not changed. Asserting GEN_RST also a ADC conversion in progress. Note : This bit does not reset automatical while it is set to 1, GEN_CNFG and GEN_CHNL_CTRL cannot be modified uf GEN_RST is set back to 0.								
Reserved	16:0	Reserved											

DCHNL_CMD (0x20)

BIT	23	22	21	20	19 18 17 10				
Field	Reserv	red[1:0]	DCHNL_MODE[1:0]		DCHNL_RATE[3:0]				
Reset	0b	00	0b	01	0x0				
Access Type	Read Only		Write,	Read	Write, Read				
BIT	15	14	13	12	11 10 9 8				
Field				Reserve	ed[15:8]				
Reset				0x0	000				
Access Type				Read	Only				

Industrial Configurable Analog I/O

BIT	7	6	5	4	3	2	1	0					
Field		Reserved[7:0]											
Reset		0x0000											
Access Type		Read Only											
BITFIELD	BITS		DESCRIPT	ION		D	ECODE						
Reserved	23:22	Reserved											
DCHNL_MO DE	21:20	Analog inpu	t ADC mode:		00: Res 01: pow type of 10: Res 11: con Note : If write to unless	00: Reserved. Do not use 01: power-down, see the DCHNL_PD bit for the type of power-down performed (default) 10: Reserved. Do not use 11: conversion mode Note : If an ADC conversion is in progress, an write to the DCHNL_MODE register is ignored							
DCHNL_RAT E	19:16	ADC data ra	te:		- refer to continue - refer to cycle co - refer to conversi	o Table 10 for o ous conversion o Table 11 for o onversion o Table 12 for s sion. Default is (data rate select data rate select single-cycle cor 0000b.	ion for ion for single- ntinuous					
Reserved	15:0	Reserved											

DCHNL_STA (0x21)

Note: DCHNL_STA updates coincident with the availability of a new converted ADC sample.

BIT	23	22	21	20	19)	18	17	16		
Field		Reserved[8:1]									
Reset		0x000									
Access Type		Read Only									
BIT	15	14	13	12	11	I	10	9	8		
Field	Reserved[0]	REFDET		Reserv	ed[3:0]			DOR	AOR		
Reset	0x000	0b0		0)	‹ 0			0b0	0b0		
Access Type	Read Only	Read Only		Read	Only			Read Only	Read Only		
BIT	7	6	5	4	3		2	1	0		
Field		RATI	=[3:0]	•	F	PDSTA	AT[1:0]	MSTAT	RDY		
Reset		0:	k 0			0b	10	0b0	0b0		
Access Type		Read	d Only Read Only Read Only R					Read Only			
BITFIELD	BITS		DESCRIPTION DECODE								
Reserved	23:15	Reserved									

Industrial Configurable Analog I/O

BITFIELD	BITS	DESCRIPTION	DECODE
REFDET	14	Reference voltage detection:	0: No reference voltage detected 1: Reference voltage detected Note : This bit results from a comparison of the selected ADC reference voltage, either internal or external, against a fixed threshold of approximately 350mV
Reserved	13:10	Reserved	
DOR	9	Digital overrange:	0: conversion of the most recent result is within the digital range of the ADC 1: conversion result exceeds the digital range of the ADC. The result is set to the minimum or maximum value, as appropriate Note : Updated when RDY asserts for a new sample
AOR	8	Analog overrange:	0: the most recent result is within the analog operating range of the ADC 1: the most recent result exceeds the analog operating range of the ADC, and the converted value is possibly corrupted Note : Updated when RDY asserts for a new sample
RATE	7:4	Conversion rate readback:	These bits indicate the conversion rate corresponding to the result in the DCHNL_DATA register that is about to be read. Refer to Tables 10, 11, or 12.
PDSTAT	3:2	Power down status:	00: ADC performing conversions01: Reserved. Do not use.10: ADC is in standby (default)11: ADC is in reset
MSTAT	1	ADC modular status:	0: ADC delta-sigma modulator is not converting 1: conversion in progress Note : The status update of the MSTAT bit may be delayed up to 2µs after start or completion of a conversion, which should be taken into account if polling the MSTAT bit immediately after a status change
RDY	0	Conversion result ready:	0: no new conversion result available 1: new conversion result available Note : this bit resets upon read of the DCHNL_DATA register

DCHNL_CTRL1 (0x22)

Note: Any write to the DCHNL_CTRL1 register that changes any non-don't-care bits aborts any ongoing ADC conversion.

BIT	23	22	21	20	19	18	17	16
Field	Reserved[2:0]		DCHNL_PD	Reserved[1:0]		SCYCLE	CONTSC	
Reset		0b000		0b0	0b	0b00		0b0
Access Type		Read Only		Write, Read	Read	Only	Write, Read	Write, Read

Industrial Configurable Analog I/O

BIT	15	14	13	12	11	10	9	8				
Field		Reserved[15:8]										
Reset		0x0000										
Access Type		Read Only										
BIT	7	6	5	4	3	2	1	0				
Field				Reserv	ed[7:0]							
Reset				0x0	000							
Access Type				Read	Only							
BITFIELD	BITS		DESCRIPTION DECODE									
Reserved	23:21	Reserved			0x0: Int 0x1: Int 0x2: Int 0x3: <i>Re</i>	ernal: Self-calil ernal: System ernal: System eserved. Do no	bration offset calibratio gain (full-scale t use.	on) calibration				
DCHNL_PD	20	Analog Pow	er Down State:	:	0: ADC 1: ADC	0: ADC in standby when powered down (default 1: ADC in reset when powered down						
Reserved	19:18	Reserved										
SCYCLE	17	Single-Cycle	e Conversion M	lode:	0: conti digital fi 1: single	nuous convers Itering e-cycle no-late	ion, with latend	cy due to n (default)				
CONTSC	16	Continuous	Single-Cycle M	lode:	0: single (default 1: conti Note : C	e conversion, ti) nuous single-c)nly in effect wi	hen transition t ycle conversio hen SCYCLE i	ro standby n s 1				
Reserved	15:0	Reserved										

DCHNL_CTRL2 (0x23)

Note: Any write to the DCHNL_CTRL2 register that changes any non-don't-care bits aborts any ongoing ADC conversion.

BIT	23	22	21	20	19	18	17	16		
Field	EXTCLK	Reserved	SYNC_MO DE	Reserved	NOSYSG	NOSYSO	Reserve	d[17:16]		
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0x00	0000		
Access Type	Write, Read	Read Only	Write, Read	Read Only	Write, Read	Write, Read	Read	Only		
BIT	15	14	13	12	11	10	9	8		
Field		Reserved[15:8]								
Reset				0x00	0000					
Access Type				Read	Only					
BIT	7	6	5	4	3	2	1	0		
Field				Reserv	red[7:0]					
Reset	0x00000									
Access Type		Read Only								

Industrial Configurable Analog I/O

BITFIELD	BITS	DESCRIPTION	DECODE
EXTCLK	23	External Clock Source Selection:	0: use internal oscillator for ADC clock (default) 1: use external clock source on the CLK pin for ADC
Reserved	22	Reserved	
SYNC_MOD E	21	External Synchronization Selection:	0: disabled (default) 1: enabled using the SYNC pin
Reserved	20	Reserved	
NOSYSG	19	No System Calibration Gain Correction:	 0: system calibration coefficient SGC used to correct ADC data (default) 1: behaves as if gain correction were set to 800000h Note: This global bit affects all ADC gain corrections
NOSYSO	18	No System Offset Correction:	0: system calibration coefficient SOC used to correct ADC data (default) 1: behaves as if offset correction were set to 000000h Note : This global bit affects all ADC offset corrections
Reserved	17:0	Reserved	

DCHNL_DATA (0x24)

BIT	23	22	21	20	19	18	17	16				
Field	DCHNL_DATA[23:16]											
Reset	0x000000											
Access Type	Read Only											
BIT	15	15 14 13 12 11 10 9 8										
Field				DCHNL	_DATA[15:8]							
Reset	0x00000											
Access Type	Read Only											
BIT	7	6	5	4	3	2	1	0				
Field				DCHN	L_DATA[7:0]		1					
Reset				0>	000000							
Access Type	Read Only											
BITFIE	LD	BITS			DE	SCRIPTION						
DCHNL_DATA	\	23:0		Digital result of A	DC conversion, tw	vo's compleme	ent					

DCHNL_N_SEL (0x25)

BIT	23	22	21	20	19	18	17	16		
Field		Reserved[19:12]								
Reset		0x00000								
Access Type				Read	Only					

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BIT	15	14	13	12	11	10	9	8				
Field	Reserved[11:4]											
Reset		0x00000										
Access Type			Read Only									
BIT	7	6	5	4	3	2	1	0				
Field		Reserv	red[3:0]			DCHNL_N	I_SEL[3:0]	•				
Reset		0x00	0000			0:	×0					
Access Type		Read	Only			Write,	Read					
BITFIELD	BITS		DESCRIPT	ION		D	ECODE					
Reserved	23:4	Reserved										
DCHNL_N_S EL	3:0	Data Chann Access Sele Analog input	el N Correction ection: t ADC channel	n Coefficient selection:	0000: n and DC 0001: D apply to 0010: D apply to 0010: D apply to 0100: D apply to 0101: D apply to 0110: D apply to 0111: R 1000: R 1011: R 1001: D apply to 1010: C apply to 1010: C apply to 1010: D apply to 1010: D apply to 1011: C apply to 1110: D apply to 1111: D apply to	o channel acce HNL_SGC regi CHNL_SOC ar Al1 singled-en CHNL_SOC ar Al2 single-end CHNL_SOC ar Al2 single-end CHNL_SOC ar Al3 single-end CHNL_SOC ar Al4 single-end CHNL_SOC ar Al4 single-end CHNL_SOC ar Al3:Al4 differe eserved CHNL_SOC ar Al5:Al6 differe eserved CHNL_SOC ar Al5:Al6 differe ions CHNL_SOC ar Al5:Al6 differe ions CHNL_SOC ar AL5:Al6 differe cons CHNL_SOC ar AL5:Al6 differe ions CHNL_SOC ar AUX1 single-end CHNL_SOC ar AUX1 single-end CHNL_SOC ar AUX2 single-end CHNL_SOC ar AUX2 single-end CHNL_SOC ar AUX2 single-end CHNL_SOC ar	ssed by the DC sters (default) nd DCHNL_SG ided conversion nd DCHNL_SG ied conversions nd DCHNL_SG ied conversions nd DCHNL_SG ied conversions nd DCHNL_SG intial conversion nd DCHNL_SG intial 12.5V con nd DCHNL_SG intial, 2.5V to 12 nd DCHNL_SG inded conversion nd DCHNL_SG	C contents C contents C contents C contents C contents C contents C contents C contents C contents C contents Versions C contents 25mV C contents c contents				

DCHNL_N_SOC (0x26)

BIT	23	22	21	20	19	18	17	16		
Field		DCHNL_N_SOC[23:16]								
Reset		0x000000								
Access Type		Write, Read								

Industrial Configurable Analog I/O

BIT	15	14	13	12	11	10	9	8				
Field	DCHNL_N_SOC[15:8]											
Reset		0x000000										
Access Type		Write, Read										
BIT	7	7 6 5 4 3 2 1 0										
Field		DCHNL_N_SOC[7:0]										
Reset		0x000000										
Access Type				Write,	Read							
BITFIELD	BITS		DESCRIPT	ION		D	ECODE					
DCHNL_N_S OC	23:0	Data Chann Value:	el N System O	ffset Calibratior	Accesse compler the DCH register	es the offset ca nent format, for INL_N_SEL bit	libration value, r the channel so ts in the DCHN	in two's elected by L_N_SEL				
					convers bits mat	Note : The write does not occur if an ADC conversion is in progress and the DCHNL_N_SEL bits match the AI DCHNL SEL bits						

DCHNL_N_SGC (0x27)

BIT	23	22	21	20	19	18	17	16			
Field	DCHNL_N_SGC[23:16]										
Reset				0xC0	0000						
Access Type		Write, Read									
BIT	15	15 14 13 12 11 10 9 8									
Field		DCHNL_N_SGC[15:8]									
Reset		0xC00000									
Access Type				Write,	Read						
BIT	7	6	5	4	3	2	1	0			
Field				DCHNL_N	_SGC[7:0]						
Reset		0xC00000									
Access Type				Write,	Read						

Industrial Configurable Analog I/O

BITFIELD	BITS	DESCRIPTION	DECODE
			Access the gain calibration value, in unsigned binary format, for the channel selected by the DCHNL_N_SEL bits in the DCHNL_N_SEL register. The gain is:
DCHNL_N_S GC	23:0	Data Channel N System Gain Calibration Value:	DCHNL_N_SGC 2 ²³
			Note : The write does not occur if an ADC conversion is in progress and the DCHNL_N_SEL bits match the AI_DCHNL_SEL bits

AO_DATA_WR (0x40)

BIT	23	22	22 21 20 19 18 17 16									
Field	AO_DATA_W[17:10]											
Reset	0x00000											
Access Type		Write Only										
BIT	15	14	13	12	11	10	9	8				
Field		AO_DATA_W[9:2]										
Reset		0x00000										
Access Type		Write Only										
BIT	7	6	5	4	3	2	1	0				
Field	AO_DAT	4_W[1:0]			Reser	ved[5:0]						
Reset	0x00	000			0	x00						
Access Type	Write	Only			Rea	d Only						
BITFIELD	BITS		DESCRIPT	ION		D	ECODE					
AO_DATA_ W	23:6	Analog Data	Write:		Digital Table 9	code, in two's c to map from c	omplement forn ode to output	nat, consult				
Reserved	5:0	Reserved										

AO_OFFSET_CORR_WR (0x41)

BIT	23	22	21	20	19	18	17	16			
Field	AO_OFFSET_W[17:10]										
Reset		0x00000									
Access Type		Write Only									
BIT	15	14	13	12	11	10	9	8			
Field		•		AO_OFFS	ET_W[9:2]		•				
Reset				0x00	0000						
Access Type				Write	Only						

Industrial Configurable Analog I/O

BIT	7	6	5	4	3	2	1	0			
Field	AO_OFFS	AO_OFFSET_W[1:0]		Reserved[5:0]							
Reset	0x00	0000			0x	0x00					
Access Type	Write	Only	Read Only								
BITFIELD	BITS		DESCRIPT	ION		D	ECODE				
AO_OFFSET _W	23:6	Analog Outp	out Offset Corre	ection Write:	Digital code in two's complement. Consult Table 8 to calculate offset correction.						
Reserved	5:0	Reserved									

AO_GAIN_CORR_WR (0x42)

BIT	23	22	22 21 20 19 18 17 16									
Field		AO_GAIN_W[17:10]										
Reset		0x3FFF										
Access Type		Write Only										
BIT	15	14	13	12	11	10	9	8				
Field		AO_GAIN_W[9:2]										
Reset		0x3FFFF										
Access Type		Write Only										
BIT	7	6	5	4	3	2	1	0				
Field	AO_GAIN	N_W[1:0]		•	Rese	erved[5:0]						
Reset	0x3F	FFF				0x00						
Access Type	Write	Only			Re	ad Only						
BITFIELD	BITS		DESCRIPT	ION		D	ECODE					
AO_GAIN_W	23:6	Analog Outp	nalog Output Gain Correction Write: Digital code, in unsigned binary. Consult Table 7 t calculate gain correction									
Reserved	5:0	Reserved										

AO_CNFG_WR (0x43)

BIT	23	22	21	20	19	18	17	16		
Field		Reserved[3:0]				F	Reserved[18:16]			
Reset		0>	(0		0b0		0x00000			
Access Type		Read	Only		Write Only		0x00000 Read Only 10 9 8			
BIT	15	14	13	12	11	10	9	8		
Field				Reserv	ed[15:8]					
Reset		0x00000								
Access Type				Read	I Only					

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BIT	7	6	5	4	3	2	1	0		
Field	Reserved[7:0]									
Reset		0x00000								
Access Type		Read Only								
BITFIELD	BITS		DESCRIPTION			DECODE				
Reserved	23:20	Reserved								
AO_RB_EN	19	Analog Outp	out Readback E	Enable:	0: AO_ AO_GA data 1: AO_I AO_GA	DATA_RD, AO .IN_CORR_RD DATA_RD, AO .IN_CORR_RD	_OFFSET_CON registers do no _OFFSET_CON return valid da	R_RD, and ot return valid RR_RD, and ta		
Reserved	18:0	Reserved								

AO_DATA_RD (0x44)

BIT	23	22	21	20	19	18	17	16	
Field			Reserv	red[5:0]			AO_DATA	AO_DATA_R[17:16]	
Reset			0x	00			0x0	0x00000	
Access Type		Read Only Read Only					l Only		
BIT	15	14	13	12	11	10	9	8	
Field			•	AO_DAT/	A_R[15:8]		•		
Reset		0x00000							
Access Type	Read Only								
BIT	7	6	5	4	3	2	1	0	
Field				AO_DAT	A_R[7:0]				
Reset				0x00	0000				
Access Type		Read Only							
BITFIELD	BITS		DESCRIPTION D			DECODE			
Reserved	23:18	Reserved	Reserved						
AO_DATA_R	17:0	Analog Outp	Analog Output Data Readback: Reads back the contents of the DAC output register when bit AO_RB_EN is high				output		

AO_OFFSET_CORR_RD (0x45)

BIT	23	22	21	20	19	18	17	16	
Field	Reserved[5:0]							AO_OFFSET_R[17:16]	
Reset	0x00 0x00000								
Access Type	Read Only Read Only					I Only			

Industrial Configurable Analog I/O

BIT	15	14	13	12	11	10	9	8
Field		AO_OFFSET_R[15:8]						
Reset				0x00	0000			
Access Type		Read Only						
BIT	7	6	5	4	3	2	1	0
Field		AO_OFFSET_R[7:0]						
Reset		0x00000						
Access Type				Read	Only			
BITFIELD	BITS		DESCRIPT	ION		DECODE		
Reserved	23:18	Reserved						
AO_OFFSET _R	17:0	Analog Outp	Analog Output Offset Correction Readback: Reads back the contents of the DAC offset correction register when bit AO_RB_EN is high					offset EN is high

AO GAIN CORR RD (0x46)

BIT	23	22	21	20	19	18	17	16
Field			Reserv	red[5:0]			AO_GAIN_R[17:16]	
Reset			0x	00			0x3FFFF	
Access Type		Read Only Read Only					Only	
BIT	15	14	13	12	11	10	9	8
Field				AO_GAIN	I_R[15:8]	•		
Reset		0x3FFFF						
Access Type	Read Only							
BIT	7	6	5	4	3	2	1	0
Field				AO_GAII	N_R[7:0]	•		
Reset				0x3F	FFF			
Access Type		Read Only						
BITFIELD	BITS		DESCRIPTION D				ECODE	
Reserved	23:18	Reserved						
AO_GAIN_R	17:0	Analog Ouput Gain Correction Readback: Reads back the contents of the DAC gain correction register when bit AO_RB_EN is high					gain N is high	

AO_STA_RD (0x47)

BIT	23	22	21	20	19	18	17	16
Field	Reserved[10:3]							
Reset		0x000						
Access Type				Read	Only			

Industrial Configurable Analog I/O

BIT	15	14	13	12	11	10	9	8		
Field		Reserved[2:0]		BUSY		Reserve	ed[11:8]			
Reset		0x000		0x0		0x000				
Access Type		Read Only Read Only				10 9 8 Reserved[11:8] 0x000 Read Only 2 1 0 DECODE log output circuit calculations complete, output reflects digital input log output circuit performing correction tions, changed digital input not yet refle og output		Read Only		
BIT	7	6	5	4	3	2	1	0		
Field				Reserv	red[7:0]					
Reset		0x000								
Access Type			Read Only							
BITFIELD	BITS		DESCRIPT	ION		DECODE				
Reserved	23:13	Reserved								
BUSY	12	Analog Outp	out Status:		0: Analo analog o 1: Analo calculat in analo	 0: Analog output circuit calculations complete, analog output reflects digital input 1: Analog output circuit performing correction calculations, changed digital input not yet reflected in analog output 				
Reserved	11:0	Reserved								

Applications Information

Power Supply Headroom Requirements

Analog inputs power from HVDD and HVSS, and generally need 2.5V of headroom to meet all linearity specifications. Low voltage PGA inputs ($\pm 2.5V$, $\pm 500mV$, $\pm 250mV$, and $\pm 125mV$) require at least a $\pm 5V$ supply, as long as both Al5 and Al6 meet the $\pm 2.5V$ range individually. To accept $\pm 10V$ inputs, whose full-scale range is $\pm 12.5V$, supply the MAX22000 with at least $\pm 15V$ on HVDD/HVSS.

The analog output powers from HVDDO and HVSSO. For the AOVM $\pm 12.5V$ setting, power from at least a recommended $\pm 15.2V$ supply. For the AOVM $\pm 25V$ setting, power HVDDO with at least a recommended $\pm 28V$ and HVSSO with a recommended -5V supply. For any AOCM setting, power from at least a recommended $\pm 22.5V$ supply. Depending on the application, it might be possible to use lower voltages. Refer to Notes 2 and 6 of the *Electrical Characteristics* table for further details.

Power Supply Sequencing

The four supplies, AVDD, DVDD, HVDD/HVSS, and HVDDO/HVSSO can power up in any order. It is recommended to have a minimum delay between respective pairs, such as HVDD and HVSS, HVDDO and HVSSO referenced to AGND.

The only restriction is that HVSS must always be more negative than HVSSO. Refer to the <u>Absolute Maximum Ratings</u> section for all power supply restrictions.

Any external reference voltage on the REF_DAC_EXT pin must never exceed VAVDD. A schottky diode connected between REF_DAC_EXT and AVDD can help satisfy this requirement.

Board Layout

Use proper grounding techniques such as a multilayer board with a low-inductance ground plane.

- Keep DGND separate from AGND, connecting the two at one point.
- Use ground plane shielding to improve noise immunity.
- Keep analog signal traces away from digital signal traces, especially clock traces.
- Connect the exposed pads on the bottom of the MAX22000 to HVSS.

For a detailed recommended layout, refer to the MAX22000 EV kit data sheet.

Surge Protection

With external circuitry, the input and output ports are protected against $\pm 1kV/42\Omega$ surge pulses as per IEC610004-5. Place a 36V bidirectional TVS between the output and AGND, past the AOP/AON diodes and past the current sense resistor. Place a minimum 4.7k Ω surge tolerant resistor in series with each input port at risk.

The other MAX22000 pins are rated for Human Body Model (HBM). If surge voltages can couple from the high voltage supplies (HVDD, HVDDO, HVSS, or HVSSO) to the low voltage supplies (DVDD or AVDD), place additional TVS suppressors on these power rails, or place TVS suppressors on the digital signal traces.

Typical Application Circuits

Typical Application Diagram



Ordering Information

PART NUMBER	ADC RESOLUTION	DAC RESOLUTION	TEMP. RANGE	PACKAGE
MAX22000ALB+	24 bits	18 bits	-40°C to +125°C	64 LGA
MAX22000ALB+T	24 bits	18 bits	-40°C to +125°C	64 LGA

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Industrial Configurable Analog I/O

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/19	Initial release	—
1	5/20	Updated the <i>Electrical Characteristics</i> section, updated Table 1 and Table 2, added the <i>Typical Application Circuit</i> ; fixed typos	1, 7, 23, 67
2	6/20	Replaced the Typical Application Circuit	67

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