

EVALUATION KIT
AVAILABLE

Complete Direct-Conversion L-Band Tuner

General Description

The MAX2121 low-cost, direct-conversion tuner IC is designed for satellite set-top and VSAT applications.

The device directly converts the satellite signals from the LNB to baseband using a broadband I/Q downconverter. The operating frequency range extends from 925MHz to 2175MHz.

The device includes an LNA and an RF variable-gain amplifier, I and Q downconverting mixers, and baseband lowpass filters and digitally controlled baseband variable-gain amplifiers. Together, the RF and baseband variable-gain amplifiers provide more than 80dB of gain control range.

The device includes fully monolithic VCOs, as well as a complete fractional-N frequency synthesizer. Additionally, an on-chip crystal oscillator is provided along with a buffered output for driving additional tuners and demodulators. Synthesizer programming and device configuration are accomplished with a 2-wire serial interface. The IC features a VCO autoselect (VAS) function that automatically selects the proper VCO. For multituner applications, the device can be configured to have one of two 2-wire interface addresses. A low-power standby mode is available whereupon the signal path is shut down while leaving the reference oscillator, digital interface, and buffer circuits active, providing a method to reduce power in single and multituner applications.

The device is the most advanced broadband/VSAT DBS tuner available. The low noise figure eliminates the need for an external LNA. A small number of passive components are needed to form a complete broadband satellite tuner DVB-S2 RF front-end solution. The tuner is available in a very small, 5mm x 5mm, 28-pin thin QFN package.

Applications

VSATs

Features

- ◆ 925MHz to 2175MHz Frequency Range
- ◆ Monolithic VCO
 - Low Phase Noise: -97dBc/Hz at 10kHz
 - No Calibration Required
- ◆ High Dynamic Range: -75dBm to 0dBm
- ◆ Integrated LP Filters: 123.75MHz
- ◆ Single +3.3V $\pm 5\%$ Supply
- ◆ Low-Power Standby Mode
- ◆ Address Pin for Multituner Applications
- ◆ Differential I/Q Interface
- ◆ I²C 2-Wire Serial Interface
- ◆ Very Small, 5mm x 5mm, 28-Pin TQFN Package

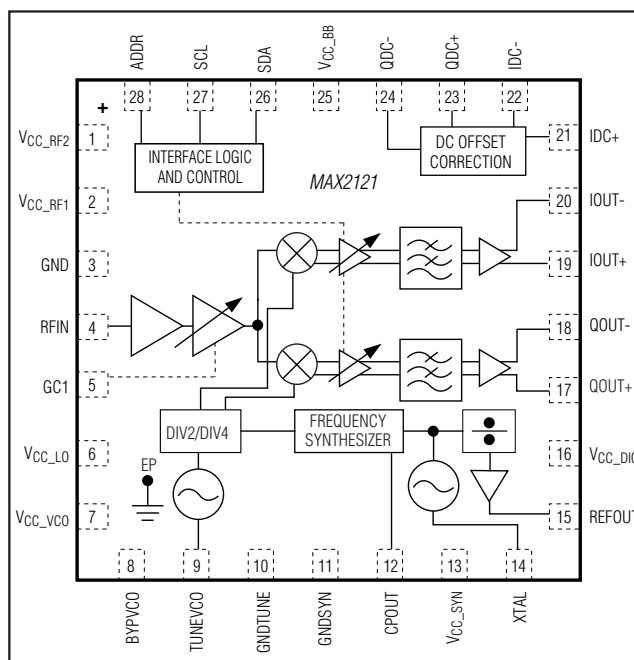
Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|-------------|----------------|-------------|
| MAX2121ETI+ | -40°C to +85°C | 28 TQFN-EP* |

*EP = Exposed pad.

+Denotes a lead(Pb)-free/RoHS-compliant package.

Functional Diagram



Complete Direct-Conversion L-Band Tuner

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND-0.3V to +3.9V
 All Other Pins to GND-0.3V to (V_{CC} + 0.3V)
 RF Input Power: RFIN+10dBm
 BYPVCO, CPOUT, XTAL, REFOUT, IOUT₋, QOUT₋, IDC₋,
 QDC₋ to GND Short-Circuit Protection10s
 Continuous Power Dissipation (T_A = +70°C)
 TQFN (derate 34.5mW/°C above +70°C)2.75W

Operating Temperature Range-40°C to +85°C
 Junction Temperature+150°C
 Storage Temperature Range-65°C to +160°C
 Lead Temperature (soldering, 10s)+300°C
 Soldering Temperature (reflow)+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(MAX2121 Evaluation Kit: V_{CC} = +3.13V to +3.47V, f_{XTAL} = 27MHz, T_A = -40°C to +85°C, V_{GC1} = +0.5V (max gain), default register settings except BBG[3:0] = 1011. No input signals at RF, baseband I/Os are open circuited. Typical values measured at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|-----------------------|------|-----------------------|-------|
| SUPPLY | | | | | |
| Supply Voltage (V _{CC}) | | 3.13 | 3.3 | 3.47 | V |
| Supply Current | Receive mode, bit STBY = 0 | | 148 | 200 | mA |
| | Standby mode, bit STBY = 1 | | 3 | | |
| ADDRESS SELECT INPUT (ADDR) | | | | | |
| Digital Input-Voltage High, V _{IH} | | 2.4 | | | V |
| Digital Input-Voltage Low, V _{IL} | | | | 0.5 | V |
| Digital Input-Current High, I _{IH} | | | | 50 | μA |
| Digital Input-Current Low, I _{IL} | | -50 | | | μA |
| ANALOG GAIN-CONTROL INPUT (GC1) | | | | | |
| Input Voltage Range | Maximum gain = 0.5V | 0.5 | | 2.7 | V |
| Input Bias Current | | -50 | | +50 | μA |
| VCO TUNING VOLTAGE INPUT (TUNEVCO) | | | | | |
| Input Voltage Range | | 0.4 | | 2.3 | V |
| 2-WIRE SERIAL INPUTS (SCL, SDA) | | | | | |
| Clock Frequency | | | | 400 | kHz |
| Input Logic-Level High | | 0.7 x V _{CC} | | | V |
| Input Logic-Level Low | | | | 0.3 x V _{CC} | V |
| Input Leakage Current | Digital inputs = GND or V _{CC} | | ±0.1 | ±1 | μA |
| 2-WIRE SERIAL OUTPUT (SDA) | | | | | |
| Output Logic-Level Low | I _{SINK} = 1mA (Note 2) | | | 0.4 | V |

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AC ELECTRICAL CHARACTERISTICS

(MAX2121 Evaluation Kit: $V_{CC} = +3.13V$ to $+3.47V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, default register settings except $BBG[3:0] = 1111$. Typical values measured at $V_{CC} = +3.3V$, $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|------|--------|----------|------------------|
| MAIN SIGNAL PATH PERFORMANCE | | | | | |
| Minimum Gain | $f_{IN} = 2175MHz$ | 72 | 78 | | dB |
| Gain Flatness | 925MHz to 2175MHz (Note 2) | | 4 | 6 | dB |
| Input Frequency Range | (Note 3) | 925 | | 2175 | MHz |
| RF Gain-Control Range (GC1) | $0.5V < V_{GC1} < 2.7V$ | 65 | 73 | | dB |
| Baseband Gain-Control Range | Bits $BBG[3:0] = 1111$ to 0000 | 11.5 | 13.5 | | dB |
| In-Band Input IP3 | (Note 4) | | +2 | | dBm |
| Out-of-Band Input IP3 | (Note 5) | | +15 | | dBm |
| Input IP2 | (Note 6) | | +40 | | dBm |
| Noise Figure | V_{GC1} is set to 0.5V (maximum RF gain) and $BBG[3:0]$ is adjusted to give a 1V _{p-p} baseband output level for a -75dBm CW input tone at 1500MHz | | 8 | | dB |
| | Starting with the same $BBG[3:0]$ setting as above, V_{GC1} is adjusted to back off RF gain by 10dB (Note 2) | | 9 | 12 | |
| Minimum RF Input Return Loss | $925MHz < f_{RF} < 2175MHz$, in 75Ω system | | 12 | | dB |
| BASEBAND OUTPUT CHARACTERISTICS | | | | | |
| Nominal Output Voltage Swing | $R_{LOAD} = 200\Omega // 5pF$ | 0.5 | 1 | | V _{P-P} |
| I/Q Amplitude Imbalance | Measured at 500kHz | | | ± 1 | dB |
| I/Q Quadrature Phase Imbalance | Measured at 500kHz | | | 3.5 | Degrees |
| Single-Ended I/Q Output Impedance | Real Z_O , from 1MHz to 140MHz | | 24 | | Ω |
| Output 1dB Compression Voltage | Differential | | 3 | | V _{P-P} |
| Baseband Highpass -3dB Frequency Corner | 47nF capacitors at IDC_{-} , QDC_{-} | | 400 | | Hz |
| BASEBAND LOWPASS FILTERS (5th-Order Butterworth with 1st-Order Group Delay Compensation) | | | | | |
| Filter Bandwidth (-3dB) | | | 123.75 | | MHz |
| Rejection Ratio | At 247.5MHz | | 31 | | dB |
| Group Delay | Up to 0.5dB bandwidth | | 1.0 | | ns |
| 3dB Bandwidth Tolerance | | | | ± 10 | % |
| FREQUENCY SYNTHESIZER | | | | | |
| RF-Divider Frequency Range | | 925 | | 2175 | MHz |
| RF-Divider Range (N) | | 19 | | 251 | |
| Reference-Divider Frequency Range | | 12 | | 30 | MHz |
| Reference-Divider Range (R) | | 1 | | 1 | |
| Phase-Detector Comparison Frequency | | 12 | | 30 | MHz |

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AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2121 Evaluation Kit: $V_{CC} = +3.13V$ to $+3.47V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, default register settings except $BBG[3:0] = 1111$. Typical values measured at $V_{CC} = +3.3V$, $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--|-----|------|------|------------------|
| VOLTAGE-CONTROLLED OSCILLATOR AND LO GENERATION | | | | | |
| Guaranteed LO Frequency Range | | 925 | | 2175 | MHz |
| LO Phase Noise | f _{OFFSET} = 10kHz | | -97 | | dBc/Hz |
| | f _{OFFSET} = 100kHz | | -100 | | |
| | f _{OFFSET} = 1MHz | | -122 | | |
| XTAL/REFERENCE OSCILLATOR INPUT AND OUTPUT BUFFER | | | | | |
| XTAL Oscillator Frequency Range f _{XTAL} | Parallel-resonance-mode crystal (Note 7) | 12 | | 30 | MHz |
| Input Overdrive Level | AC-coupled sine-wave input | 0.5 | 1 | 2.0 | V _{P-P} |
| XTAL Output-Buffer Divider Range | | 1 | | 8 | |
| XTAL Output Voltage Swing | 12MHz to 30MHz, C _{LOAD} = 10pF | 1 | 1.5 | 2 | V _{P-P} |
| XTAL Output Duty Cycle | | | 50 | | % |

Note 1: Min/max values are production tested at $T_A = +25^{\circ}C$. Min/max limits at $T_A = -40^{\circ}C$ and $T_A = +85^{\circ}C$ are guaranteed by design and characterization.

Note 2: Guaranteed by design and characterization at $T_A = +25^{\circ}C$.

Note 3: Input gain range specifications met over this band.

Note 4: In-band IIP3 test conditions: GC1 set to provide the nominal baseband output drive when mixing down a -23dBm tone at 2175MHz to 5MHz baseband ($f_{LO} = 2170MHz$). Baseband gain is set to its default value ($BBG[3:0] = 1011$). Two tones at -26dBm each are applied at 2174MHz and 2175MHz. The IM3 tone at 3MHz is measured at baseband, but is referred to the RF input.

Note 5: Out-of-band IIP3 test conditions: GC1 set to provide nominal baseband output drive when mixing down a -23dBm tone at 2175MHz to 5MHz baseband ($f_{LO} = 2170MHz$). Baseband gain is set to its default value ($BBG[3:0] = 1011$). Two tones at -20dBm each are applied at 1919MHz and 1663MHz. The IM3 tone at 5MHz is measured at baseband, but is referred to the RF input.

Note 6: Input IP2 test conditions: GC1 set to provide nominal baseband output drive when mixing down a -23dBm tone at 2175MHz to 5MHz baseband ($f_{LO} = 2170MHz$). Baseband gain is set to its default value ($BBG[3:0] = 1011$). Two tones at -20dBm each are applied at 925MHz and 1250MHz. The IM2 tone at 5MHz is measured at baseband, but is referred to the RF input.

Note 7: See Table 16 for crystal ESR requirements.

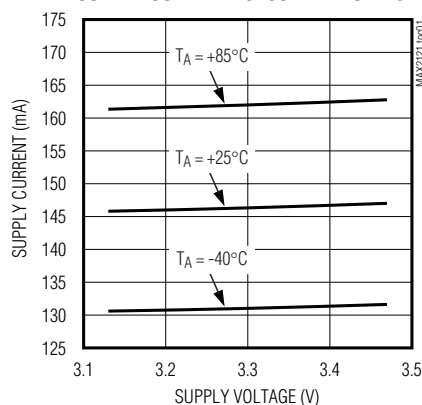
Complete Direct-Conversion L-Band Tuner

Typical Operating Characteristics

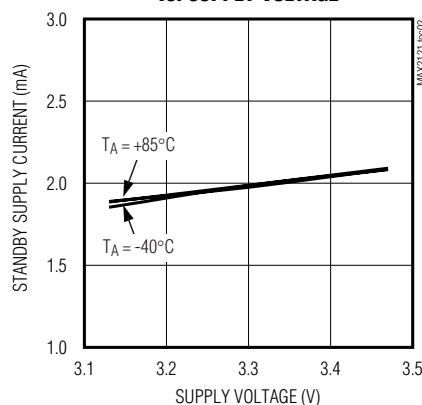
(MAX2121 Evaluation Kit: $V_{CC} = +3.3V$, $T_A = +25^\circ C$, baseband output frequency = 5MHz, $V_{GC1} = +1.2V$, default register settings except BBG[3:0] = 1011, unless otherwise noted.)

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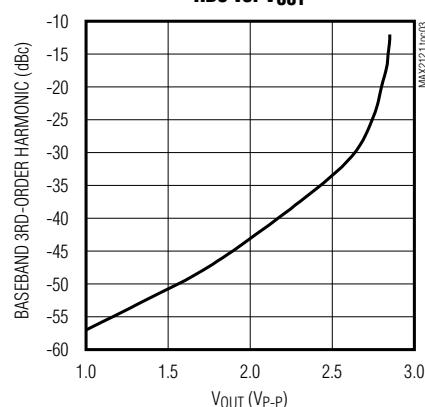
SUPPLY CURRENT vs. SUPPLY VOLTAGE



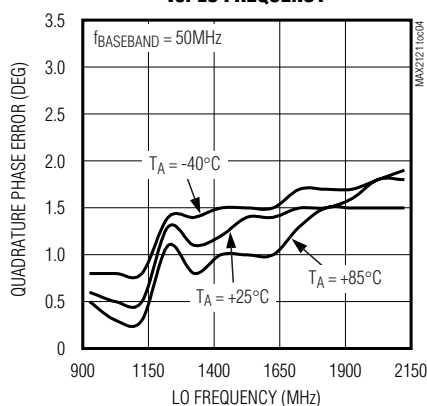
STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE



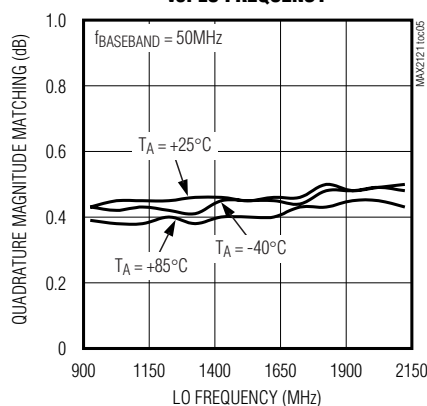
HD3 vs. VOUT



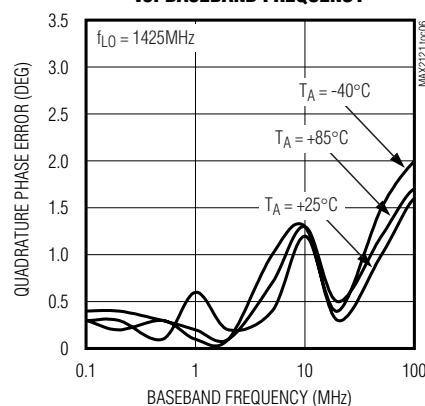
QUADRATURE PHASE ERROR vs. LO FREQUENCY



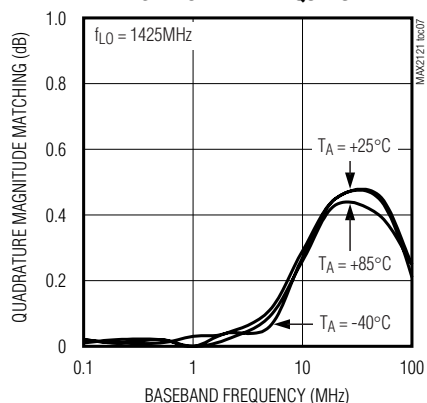
QUADRATURE MAGNITUDE MATCHING vs. LO FREQUENCY



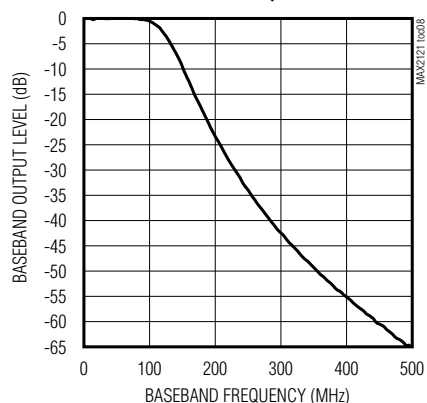
QUADRATURE PHASE ERROR vs. BASEBAND FREQUENCY



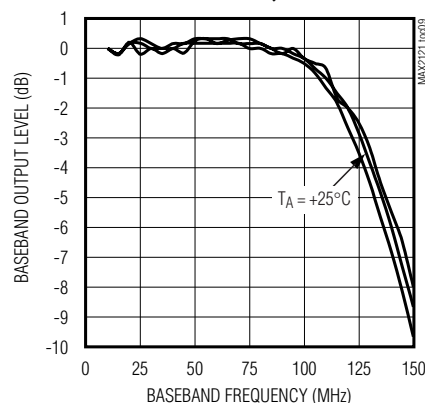
QUADRATURE MAGNITUDE MATCHING vs. BASEBAND FREQUENCY



BASEBAND FILTER FREQUENCY RESPONSE



BASEBAND FILTER FREQUENCY RESPONSE

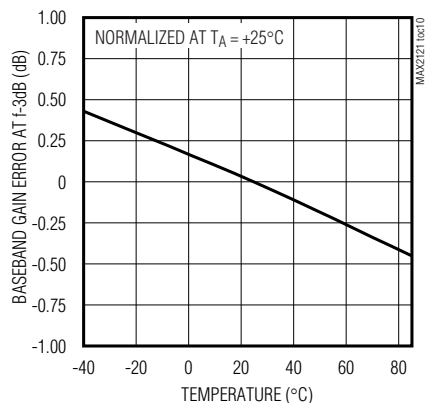


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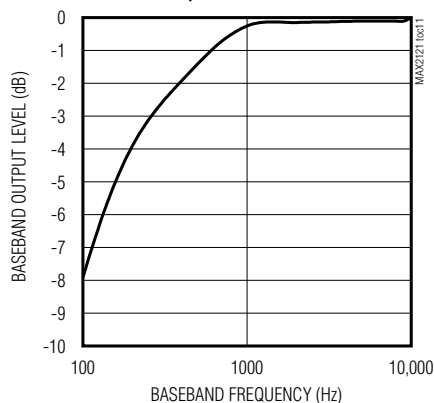
Typical Operating Characteristics (continued)

(MAX2121 Evaluation Kit: $V_{CC} = +3.3V$, $T_A = +25^\circ C$, baseband output frequency = 5MHz, $V_{GC1} = +1.2V$, default register settings except BBG[3:0] = 1011, unless otherwise noted.)

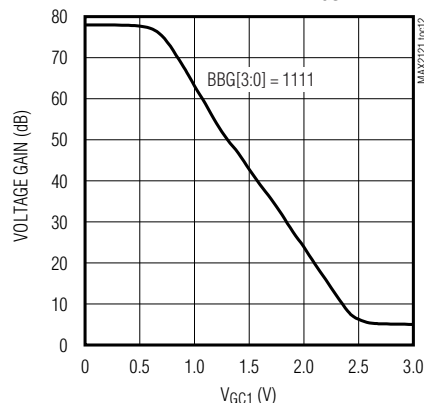
**BASEBAND FILTER 3dB FREQUENCY
vs. TEMPERATURE**



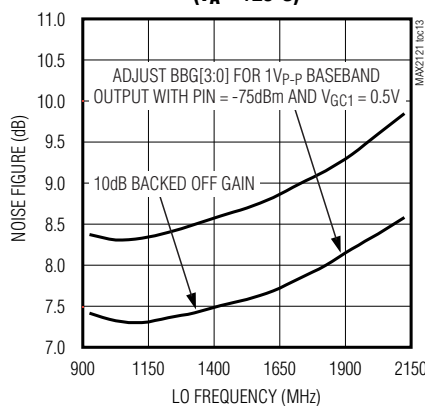
**BASEBAND FILTER HIGHPASS
FREQUENCY RESPONSE**



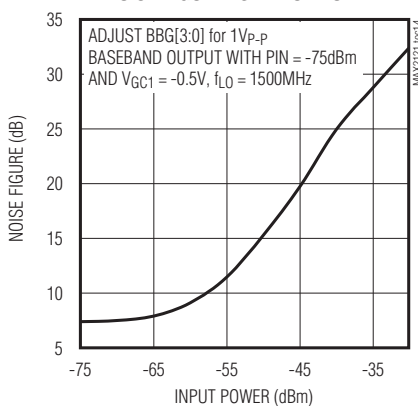
VOLTAGE GAIN vs. V_{GC1}



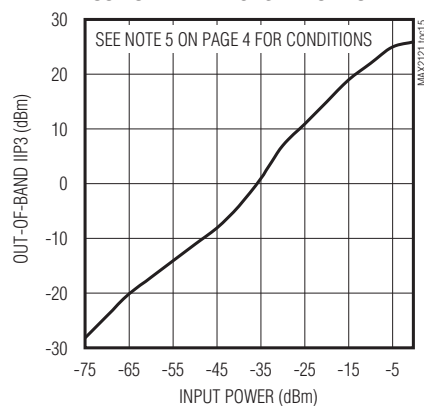
**NOISE FIGURE vs. LO FREQUENCY
($T_A = +25^\circ C$)**



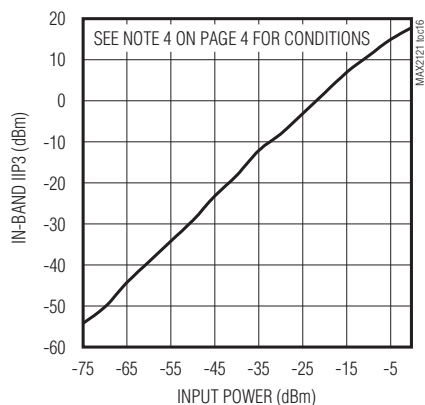
NOISE FIGURE vs. INPUT POWER



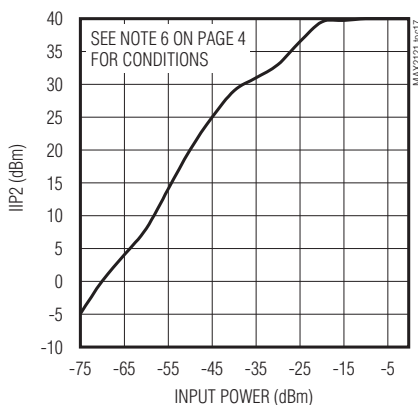
OUT-OF-BAND IIP3 vs. INPUT POWER



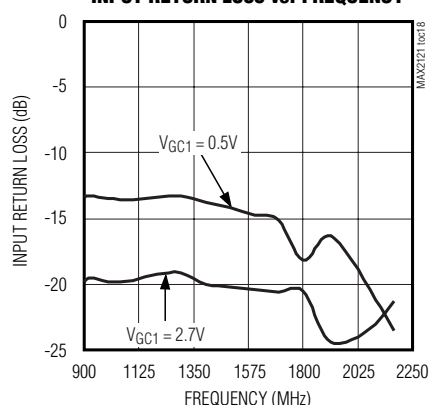
IN-BAND IIP3 vs. INPUT POWER



IIP2 vs. INPUT POWER



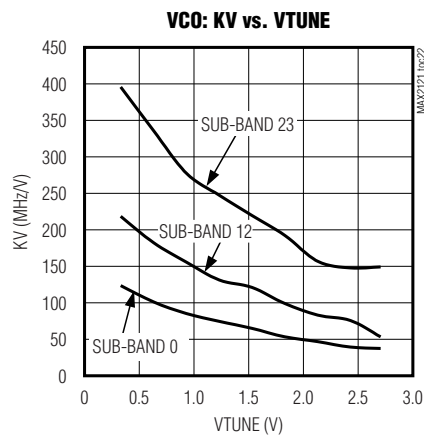
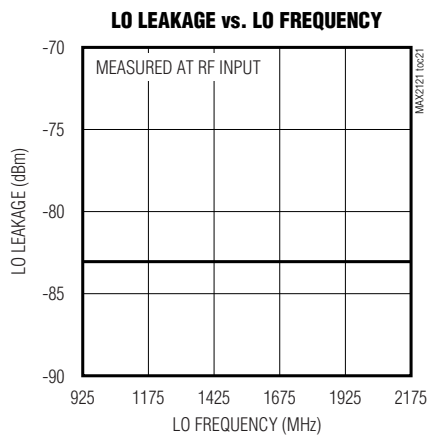
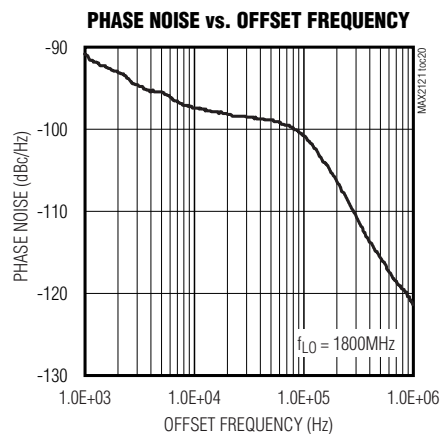
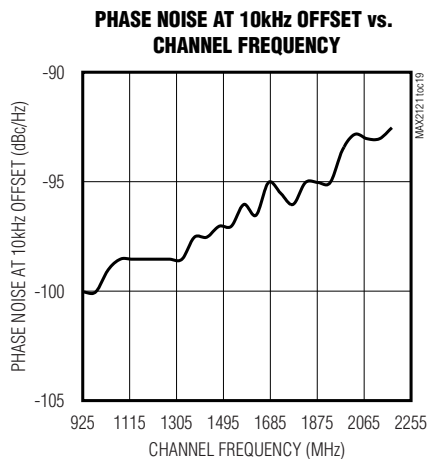
INPUT RETURN LOSS vs. FREQUENCY



Complete Direct-Conversion L-Band Tuner

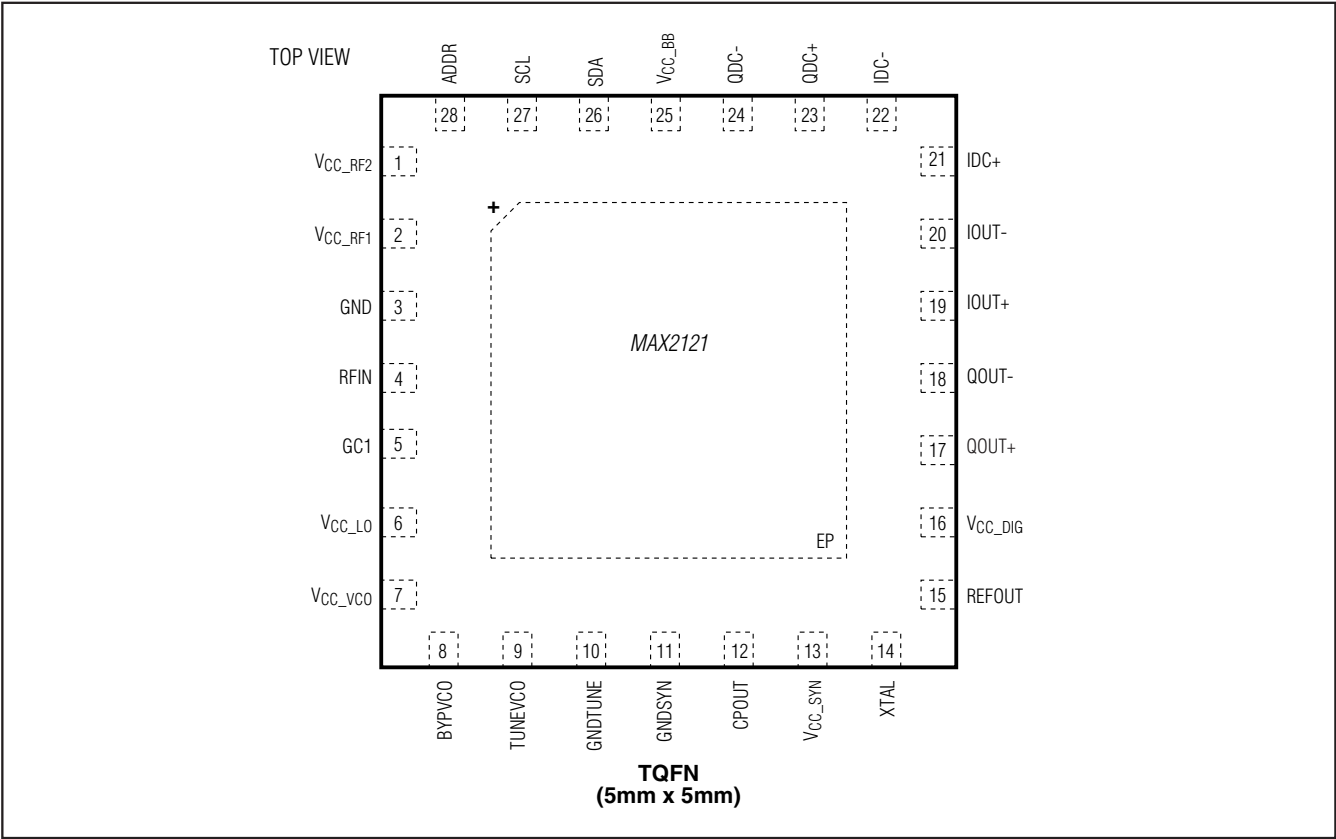
Typical Operating Characteristics (continued)

(MAX2121 Evaluation Kit: $V_{CC} = +3.3V$, $T_A = +25^\circ C$, baseband output frequency = 5MHz, $V_{GC1} = +1.2V$, default register settings except BBG[3:0] = 1011, unless otherwise noted.)



Complete Direct-Conversion L-Band Tuner

Pin Configuration



Pin Description

| PIN | NAME | FUNCTION |
|-----|---------|--|
| 1 | VCC_RF2 | DC Power Supply for LNA. Connect to a +3.3V low-noise supply. Bypass to GND with a 1nF capacitor connected as close as possible to the pin. Do not share capacitor ground vias with other ground connections. |
| 2 | VCC_RF1 | DC Power Supply for LNA. Connect to a +3.3V low-noise supply. Bypass to GND with a 1nF capacitor connected as close as possible to the pin. Do not share capacitor ground vias with other ground connections. |
| 3 | GND | Ground. Connect to board's ground plane for proper operation. |
| 4 | RFIN | Wideband 75 Ω RF Input. Connect to an RF source through a DC-blocking capacitor. |
| 5 | GC1 | RF Gain-Control Input. High-impedance analog input with a 0.5V to 2.7V operating range. V _{GC1} = 0.5V corresponds to the maximum gain setting. |
| 6 | VCC_LO | DC Power Supply for LO Generation Circuits. Connect to a +3.3V low-noise supply. Bypass to GND with a 1nF capacitor connected as close as possible to the pin. Do not share capacitor ground vias with other ground connections. |
| 7 | VCC_VCO | DC Power Supply for VCO Circuits. Connect to a +3.3V low-noise supply. Bypass to GND with a 1nF capacitor connected as close as possible to the pin. Do not share capacitor ground vias with other ground connections. |

Complete Direct-Conversion L-Band Tuner

Pin Description (continued)

MAX2121

| PIN | NAME | FUNCTION |
|-----|---------|--|
| 8 | BYPVCO | Internal VCO Bias Bypass. Bypass to GND with a 100nF capacitor connected as close as possible to the pin. Do not share capacitor ground vias with other ground connections. |
| 9 | TUNEVCO | High-Impedance VCO Tune Input. Connect the PLL loop filter output directly to this pin with as short of a connection as possible. |
| 10 | GNDTUNE | Ground for TUNEVCO. Connect to the PCB ground plane. |
| 11 | GNDSYN | Ground for Synthesizer. Connect to the PCB ground plane. |
| 12 | CPOUT | Charge-Pump Output. Connect this output to the PLL loop filter input with the shortest connection possible. |
| 13 | VCC_SYN | DC Power Supply for Synthesizer Circuits. Connect to a +3.3V low-noise supply. Bypass to GND with a 1nF capacitor connected as close as possible to the pin. Do not share capacitor ground vias with other ground connections. |
| 14 | XTAL | Crystal-Oscillator Interface. Use with an external parallel-resonance-mode crystal through a series 1nF capacitor. See the <i>Typical Application Circuit</i> . |
| 15 | REFOUT | Crystal-Oscillator Buffer Output. A DC-blocking capacitor must be used when driving external circuitry. |
| 16 | VCC_DIG | DC Power Supply for Digital Logic Circuits. Connect to a +3.3V low-noise supply. Bypass to GND with a 1nF capacitor connected as close as possible to the pin. Do not share capacitor ground vias with other ground connections. |
| 17 | QOUT+ | Quadrature Baseband Differential Output. AC-couple with 47nF capacitors to the demodulator input. |
| 18 | QOUT- | |
| 19 | IOUT+ | In-Phase Baseband Differential Output. AC-couple with 47nF capacitors to the demodulator input. |
| 20 | IOUT- | |
| 21 | IDC+ | I-Channel Baseband DC Offset Correction. Connect a 47nF ceramic chip capacitor from IDC- to IDC+. |
| 22 | IDC- | |
| 23 | QDC+ | Q-Channel Baseband DC Offset Correction. Connect a 47nF ceramic chip capacitor from QDC- to QDC+. |
| 24 | QDC- | |
| 25 | VCC_BB | DC Power Supply for Baseband Circuits. Connect to a +3.3V low-noise supply. Bypass to GND with a 1nF capacitor connected as close as possible to the pin. Do not share capacitor ground vias with other ground connections. |
| 26 | SDA | 2-Wire Serial-Data Interface. Requires $\geq 1k\ \Omega$ pullup resistor to VCC. |
| 27 | SCL | 2-Wire Serial-Clock Interface. Requires $\geq 1k\ \Omega$ pullup resistor to VCC. |
| 28 | ADDR | Address. Must be connected to either ground (logic 0) or supply (logic 1). |
| — | EP | Exposed Pad. Solder evenly to the board's ground plane for proper operation. |

Complete Direct-Conversion L-Band Tuner

Detailed Description

Register Description

The MAX2121 includes 12 user-programmable registers and two read-only registers. See Table 1 for register configurations. The register configuration of Table 1

shows each bit name and the bit usage information for all registers. Note that all registers must be written after and no earlier than 100μs after the device is powered up. The VCO autoselection circuit is triggered by writing to register 5. Thus register 5 should be the last register to be written in order to ensure proper PLL lock.

Table 1. Register Configuration

| REG NUMBER | REGISTER NAME | READ/ WRITE | REG ADDRESS | MSB | | | | | | | | LSB | |
|---------------|--|----------------|----------------|---------------|---------------|---------------|---------------|------------|-------------------|-------------------|-------------------|------|------|
| | | | | DATA BYTE | | | | | | | | D[1] | D[0] |
| | | | | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | | |
| 1 | N-Divider MSB | Write | 0x00 | FRAC 1 | N[14] | N[13] | N[12] | N[11] | N[10] | N[9] | N[8] | | |
| 2 | N-Divider LSB | Write | 0x01 | N[7] | N[6] | N[5] | N[4] | N[3] | N[2] | N[1] | N[0] | | |
| 3 | Charge Pump | Write | 0x02 | CPMP[1] 0 | CPMP[0] 0 | CPLIN[1] 0 | CPLIN[0] 1 | F[19] | F[18] | F[17] | F[16] | | |
| 4 | F-Divider MSB | Write | 0x03 | F[15] | F[14] | F[13] | F[12] | F[11] | F[10] | F[9] | F[8] | | |
| 5 | F-Divider LSB | Write | 0x04 | F[7] | F[6] | F[5] | F[4] | F[3] | F[2] | F[1] | F[0] | | |
| 6 | XTAL Buffer and Reference Divider | Write | 0x05 | XD[2] | XD[1] | XD[0] | R[4] | R[3] | R[2] | R[1] | R[0] | | |
| 7 | PLL | Write | 0x06 | D24 | CPS | ICP | X | X | X | X | X | | |
| 8 | VCO | Write | 0x07 | VCO[4] | VCO[3] | VCO[2] | VCO[1] | VCO[0] | VAS | ADL | ADE | | |
| 9 | Lowpass Filter | Write | 0x08 | 10010111 | | | | | | | | | |
| 10 | Control | Write | 0x09 | STBY | X | PWDN 0 | X | BBG[3] | BBG[2] | BBG[1] | BBG[0] | | |
| 11 | Shutdown | Write | 0x0A | X | PLL 0 | DIV 0 | VCO 0 | BB 0 | RFMIX 0 | RFVGA 0 | FE 0 | | |
| 12 | Test | Write | 0x0B | CPTST[2] 0 | CPTST[1] 0 | CPTST[0] 0 | X | TURBO 1 | LD MUX[2] 0 | LD MUX[1] 0 | LD MUX[0] 0 | | |
| 13 | Status Byte-1 | Read | 0x0C | POR | VASA | VASE | LD | X | X | X | X | | |
| 14 | Status Byte-2 | Read | 0x0D | VCOSBR[4] | VCOSBR[3] | VCOSBR[2] | VCOSBR[1] | VCOSBR[0] | ADC[2] | ADC[1] | ADC[0] | | |

X = Don't care.

0 = Set to 0 for factory-tested operation.

1 = Set to 1 for factory-tested operation.

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Table 2. N-Divider MSB Register (Address: 0x00)

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|----------|------------------------|---------|--|
| FRAC | 7 | 1 | Users must program to 1 upon powering up the device. |
| N[14:8] | 6–0 | 0000000 | Sets the most significant bits of the PLL integer-divide number (N). N can range from 19 to 251. |

Table 3. N-Divider LSB Register (Address: 0x01)

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|----------|------------------------|----------|---|
| N[7:0] | 7–0 | 00100011 | Sets the least significant bits of the PLL integer-divide number. N can range from 19 to 251. |

Table 4. Charge-Pump Register (Address: 0x02)

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|------------|------------------------|---------|---|
| CPMP[1:0] | 7–6 | 00 | Charge-pump minimum pulse width. Users must program to 00 upon powering up the device. |
| CPLIN[1:0] | 5–4 | 00 | Controls charge-pump linearity. Users must program to 01 upon powering up the device. |
| F[19:16] | 3–0 | 0010 | Sets the 4 most significant bits of the PLL fractional divide number. Default value is F = 194,180 decimal. |

Table 5. F-Divider MSB Register (Address: 0x03)

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|----------|------------------------|----------|---|
| F[15:8] | 7–0 | 11110110 | Sets the most significant bits of the PLL fractional-divide number (F). Default value is F = 194,180 decimal. |

Table 6. F-Divider LSB Register (Address: 0x04)

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|----------|------------------------|----------|--|
| F[7:0] | 7–0 | 10000100 | Sets the least significant bits of the PLL fractional-divide number (F). Default value is F = 194,180 decimal. |

Table 7. XTAL Buffer and Reference Divider Register (Address: 0x05)

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|----------|------------------------|---------|---|
| XD[2:0] | 7–5 | 000 | Sets the crystal-divider setting. 000 = Divide by 1. 001 = Divide by 2. 011 = Divide by 3. 100 = Divide by 4. 101 through 110 = All divide values from 5 (101) to 7 (110). 111 = Divide by 8. |
| R[4:0] | 4–0 | 00001 | Sets the PLL reference-divider (R) number. Users must program to 00001 upon powering up the device. 00001 = Divide by 1; other values are not tested. |

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Table 8. PLL Register (Address: 0x06)

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|----------|------------------------|---------|---|
| D24 | 7 | 1 | VCO divider setting. 0 = Divide by 2. Use for LO frequencies $\geq 1125\text{MHz}$. 1 = Divide by 4. Use for LO frequencies $< 1125\text{MHz}$. |
| CPS | 6 | 1 | Charge-pump current mode. 0 = Charge-pump current controlled by ICP bit. 1 = Charge-pump current controlled by VCO autoselect (VAS). |
| ICP | 5 | 0 | Charge-pump current. 0 = $600\mu\text{A}$ typical. 1 = $1200\mu\text{A}$ typical. |
| X | 4–0 | X | Don't care. |

Table 9. VCO Register (Address: 0x07)

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|----------|------------------------|---------|---|
| VCO[4:0] | 7–3 | 11001 | Controls which VCO is activated when using manual VCO programming mode. This also serves as the starting point for the VCO autoselection (VAS) mode. |
| VAS | 2 | 1 | VCO autoselection (VAS) circuit. 0 = Disable VCO selection must be programmed through I ² C. 1 = Enable VCO selection controlled by autoselection circuit. |
| ADL | 1 | 0 | Enables or disables the VCO tuning voltage ADC latch when the VCO autoselect mode (VAS) is disabled. 0 = Disables the ADC latch. 1 = Latches the ADC value. |
| ADE | 0 | 0 | Enables or disables VCO tuning voltage ADC read when the VCO autoselect mode (VAS) is disabled. 0 = Disables ADC read. 1 = Enables ADC read. |

Table 10. Lowpass Filter Register (Address: 0x08)

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|----------|------------------------|----------|--|
| Reserved | 7–0 | 01001011 | User must program to 10010111 (97h) upon powering up the device. |

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Table 11. Control Register (Address: 0x09)

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|----------|------------------------|---------|--|
| STBY | 7 | 0 | Software standby control. 0 = Normal operation. 1 = Disables the signal path and frequency synthesizer leaving only the 2-wire bus, crystal oscillator, XTALOUT buffer, and XTALOUT buffer divider active. |
| X | 6 | X | Don't care. |
| PWDN | 5 | 0 | Factory use only. 0 = Normal operation; other value is not tested. |
| X | 4 | X | Don't care. |
| BBG[3:0] | 3-0 | 0000 | Baseband gain setting (1dB typical per step). 0000 = Minimum gain (0dB, default). ... 1111 = Maximum gain (15dB typical). |

Table 12. Shutdown Register (Address: 0x0A)

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|----------|------------------------|---------|---|
| X | 7 | X | Don't care. |
| PLL | 6 | 0 | PLL enable. 0 = Normal operation. 1 = Shuts down the PLL. Value not tested. |
| DIV | 5 | 0 | Divider enable. 0 = Normal operation. 1 = Shuts down the divider. Value not tested. |
| VCO | 4 | 0 | VCO enable. 0 = Normal operation. 1 = Shuts down the VCO. Value not tested. |
| BB | 3 | 0 | Baseband enable. 0 = Normal operation. 1 = Shuts down the baseband. Value not tested. |
| RFMIX | 2 | 0 | RF mixer enable. 0 = Normal operation. 1 = Shuts down the RF mixer. Value not tested. |
| RFVGA | 1 | 0 | RF VGA enable. 0 = Normal operation. 1 = Shuts down the RF VGA. Value not tested. |
| FE | 0 | 0 | Front-end enable. 0 = Normal operation. 1 = Shuts down the front-end. Value not tested. |

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Table 13. Test Register (Address: 0x0B)

| BIT NAME | BIT LOCATION (0 = LSB) | DEFAULT | FUNCTION |
|------------|------------------------|---------|---|
| CPTST[2:0] | 7–5 | 000 | Charge-pump test modes. 000 = Normal operation (default). |
| X | 4 | X | Don't care. |
| TURBO | 3 | 1 | Charge-pump fast lock. Users must program to 1 after powering up the device. |
| LDMUX[2:0] | 2–0 | 000 | REFOUT output. 000 = Normal operation; other values are not tested. |

Table 14. Status Byte-1 Register (Address: 0x0C)

| BIT NAME | BIT LOCATION (0 = LSB) | FUNCTION |
|----------|------------------------|---|
| POR | 7 | Power-on reset status. 0 = Chip status register has been read with a stop condition since last power-on. 1 = Power-on reset (power cycle) has occurred. Default values have been loaded in registers. |
| VASA | 6 | Indicates whether VCO autoselection was successful. 0 = Indicates the autoselect function is disabled or unsuccessful VCO selection. 1 = Indicates successful VCO autoselection. |
| VASE | 5 | Status indicator for the autoselect function. 0 = Indicates the autoselect function is active. 1 = Indicates the autoselect process is inactive. |
| LD | 4 | PLL lock detector. TURBO bit must be programmed to 1 for valid LD reading. 0 = Unlocked. 1 = Locked. |
| X | 3–0 | Don't care. |

Table 15. Status Byte-2 Register (Address: 0x0D)

| BIT NAME | BIT LOCATION (0 = LSB) | FUNCTION |
|-------------|------------------------|--|
| VCOSBR[4:0] | 7–3 | VCO band readback. |
| ADC[2:0] | 2–0 | VAS ADC output readback. 000 = Out of lock. 001 = Locked. 010 = VAS locked. 101 = VAS locked. 110 = Locked. 111 = Out of lock. |

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2-Wire Serial Interface

The MAX2121 uses a 2-wire I²C-compatible serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX2121 and the master at clock frequencies up to 400kHz. The master initiates a data transfer on the bus and generates the SCL signal to permit data transfer. The MAX2121 behaves as a slave device that transfers and receives data to and from the master. SDA and SCL must be pulled high with external pullup resistors (1k Ω or greater) for proper bus operation. Pullup resistors should be referenced to the MAX2121's VCC.

One bit is transferred during each SCL clock cycle. A minimum of nine clock cycles is required to transfer a byte in or out of the MAX2121 (8 bits and an ACK/NACK). The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *START and STOP Conditions* section). Both SDA and SCL remain high when the bus is not busy.

START and STOP Conditions

The master initiates a transmission with a START condition (S), which is a high-to-low transition on SDA while SCL is high. The master terminates a transmission with a STOP condition (P), which is a low-to-high transition on SDA while SCL is high.

Acknowledge and Not-Acknowledge Conditions

Data transfers are framed with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX2121 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse.

To generate a not-acknowledge condition, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse, and leaves SDA high during the high period of the clock pulse. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master must reattempt communication at a later time.

Slave Address

The MAX2121 has a 7-bit slave address that must be sent to the device following a START condition to initiate communication. The slave address is internally programmed to 1100000. The eighth bit (R/W) following the 7-bit address determines whether a read or write operation occurs.

The MAX2121 continuously awaits a START condition followed by its slave address. When the device recognizes its slave address, it acknowledges by pulling the SDA line low for one clock period; it is ready to accept or send data depending on the R/W bit (Figure 1).

The write/read address is C0/C1 if ADDR pin is connected to ground. The write/read address is C2/C3 if the ADDR pin is connected to VCC.

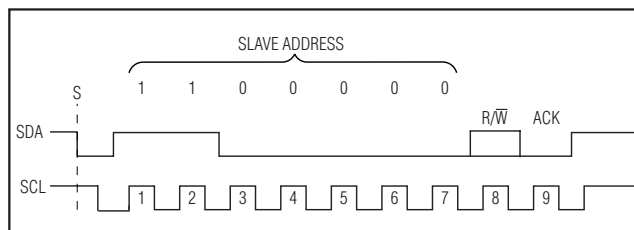


Figure 1. MAX2121 Slave Address Byte with ADDR Pin Connected to Ground

Write Cycle

When addressed with a write command, the MAX2121 allows the master to write to a single register or to multiple successive registers.

A write cycle begins with the bus master issuing a START condition followed by the seven slave address bits and a write bit ($R/\overline{W} = 0$). The MAX2121 issues an ACK if the slave address byte is successfully received. The bus master must then send to the slave the address of the first register it wishes to write to (see Table 1 for register addresses). If the slave acknowledges the address, the master can then write one byte to the register at the specified address. Data is written beginning with the most significant bit. The MAX2121 again issues an ACK if the data is successfully written to the register. The master can continue to write data to the successive internal registers with the MAX2121 acknowledging each successful transfer, or it can terminate transmission by issuing a STOP condition. The write cycle does not terminate until the master issues a STOP condition.

| START | WRITE DEVICE ADDRESS | R/ \overline{W} | ACK | WRITE REGISTER ADDRESS | ACK | WRITE DATA TO REGISTER 0x00 | ACK | WRITE DATA TO REGISTER 0x01 | ACK | WRITE DATA TO REGISTER 0x02 | ACK | STOP |
|-------|----------------------|-------------------|-----|------------------------|-----|-----------------------------|-----|-----------------------------|-----|-----------------------------|-----|------|
| | 1100000 | 0 | — | 0x00 | — | 0x0E | — | 0xD8 | — | 0xE1 | — | |

Figure 2. Example: Write Registers 0, 1, and 2 with 0x0E, 0xD8, and 0xE1, respectively.

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| START | WRITE DEVICE ADDRESS | R/ \bar{W} | ACK | READ FROM STATUS BYTE-1 REGISTER | ACK | READ FROM STATUS BYTE-2 REGISTER | ACK/ NACK | STOP |
|-------|----------------------|--------------|-----|----------------------------------|-----|----------------------------------|--------------|------|
| | 1100000 | 1 | — | — | — | — | — | |

Figure 3. Example: Receive Data from Read Registers

Read Cycle

When addressed with a read command, the MAX2121 allows the master to read back a single register, or multiple successive registers.

A read cycle begins with the bus master issuing a START condition followed by the seven slave address bits and a write bit ($R/\bar{W} = 0$). The MAX2121 issues an ACK if the slave address byte is successfully received. The bus master must then send the address of the first register it wishes to read (see Table 1 for register addresses). The slave acknowledges the address. Then, a START condition is issued by the master, followed by the seven slave address bits and a read bit ($R/\bar{W} = 1$). The MAX2121 issues an ACK if the slave address byte is successfully received. The MAX2121 starts sending data MSB first with each SCL clock cycle. At the 9th clock cycle, the master can issue an ACK and continue to read successive registers, or the master can terminate the transmission by issuing a NACK. The read cycle does not terminate until the master issues a STOP condition.

Figure 3 illustrates an example in which registers 0, 1, and 2 are read back.

Application Information

The MAX2121 downconverts RF signals in the 925MHz to 2175MHz range directly to the baseband I/Q signals.

RF Input

The RF input of the MAX2121 is internally matched to 75Ω . Only a DC-blocking capacitor is needed. See the *Typical Application Circuit*.

RF Gain Control

The MAX2121 features a variable-gain low-noise amplifier providing 73dB of RF gain range. The voltage control (VGC) range is 0.5V (minimum attenuation) to 2.7V (maximum attenuation).

Baseband Variable-Gain Amplifier

The receiver baseband variable-gain amplifiers provide 15dB of gain control range programmable in 1dB steps. The VGA gain can be serially programmed through the I²C interface by setting bits BBG[3:0] in the Control register.

Table 16. Maximum Crystal ESR Requirement

| ESR _{MAX} (Ω) | XTAL FREQUENCY (MHz) |
|---------------------------------|-------------------------|
| 80 | $12 < f_{XTAL} \leq 14$ |
| 60 | $14 < f_{XTAL} \leq 30$ |

Baseband Lowpass Filter

The MAX2121 includes an on-chip 5th-order Butterworth filter with 1st-order group delay compensation.

DC Offset Cancellation

The DC offset cancellation is required to maintain the I/Q output dynamic range. Connecting an external capacitor between IDC+ and IDC- forms a highpass filter for the I channel and an external capacitor between QDC+ and QDC- forms a highpass filter for the Q channel. Keep the value of the external capacitor less than 47nF to form a typical highpass corner of 250Hz.

XTAL Oscillator

The MAX2121 contains an internal reference oscillator, reference output divider, and output buffer. All that is required is to connect a crystal through a series 1nF capacitor. To minimize parasitics, place the crystal and series capacitor as close as possible to pin 14 (XTAL). See Table 16 for crystal (XTAL) ESR (equivalent series resistance) requirements.

Programming the Fractional N- Synthesizer

The MAX2121 utilizes a fractional-N type synthesizer for LO frequency programming. To program the frequency synthesizer, the N and F values are encoded as straight binary numbers. Determination of these values is illustrated by the following example:

f_{LO} is 2170MHz

f_{XTAL} is 27 MHz

Phase-detector comparison frequency is from 12MHz and 30MHz

R divider = R[4:0] = 1

$f_{COMP} = 27\text{MHz}/1 = 27\text{MHz}$

$D = f_{LO}/f_{COMP} = 2170/27 = 80.37470$

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Integer portion:

$N = 80$

$N[14:8] = 0$

$N[7:0] = 0101\ 0000$

Fractional portion:

$F = 0.370370 \times 2^{20} = 388,361$ (round up the decimal portion)

$F = 0101\ 1110\ 1101\ 0000\ 1001$

Note: When changing LO frequencies, all the divider registers (integer and fractional) must be programmed to activate the VAS function regardless of whether individual registers are changed.

VCO Autoselect (VAS)

The MAX2121 includes 24 VCOs. The local oscillator frequency can be manually selected by programming the VCO[4:0] bits in the VCO register. The selected VCO is reported in the Status Byte-2 register (see Table 15).

Alternatively, the MAX2121 can be set to autonomously choose a VCO by setting the VAS bit in the VCO register to logic-high. The VAS routine is initiated once the F-Divider LSB register word (register 5) is loaded.

Thus it is important to write register 5 **after** any of the following PLL related bits have been changed:

N-Divider bits (registers 1 and/or 2)

F-Divider bits (registers 3 and/or 4)

Reference Divider bits (register 6)

D24, CPS, or ICP bits (register 7)

This will ensure all intended bits have been programmed **before** the VAS is initiated and the PLL is locked. The VCO value programmed in the VCO[4:0] register serves as the starting point for the automatic VCO selection process.

During the selection process, the VASE bit in the Status Byte-1 register is cleared to indicate the autoselection function is active. Upon successful completion, bits VASE and VASA are set and the VCO selected is reported in the Status Byte-2 register (see Table 15). If the search is unsuccessful, VASA is cleared and VASE is set. This indicates that searching has ended but no good VCO has been found, and occurs when trying to tune to a frequency outside the VCO's specified frequency range.

Refer to Application Note 4256: *Extended Characterization for the MAX2112/MAX2120 Satellite Tuners*.

3-Bit ADC

The MAX2121 has an internal 3-bit ADC connected to the VCO tune pin (TUNEVCO). This ADC can be used for checking the lock status of the VCOs.

Table 17. ADC Trip Points and Lock Status

| ADC[2:0] | LOCK STATUS |
|----------|-------------|
| 000 | Out of lock |
| 001 | Locked |
| 010 | VAS locked |
| 101 | VAS locked |
| 110 | Locked |
| 111 | Out of lock |

Table 17 summarizes the ADC output bits and the VCO lock indication. The VCO autoselect routine only selects a VCO in the "VAS locked" range. This allows room for a VCO to drift over temperature and remain in a valid "locked" range.

The ADC must first be enabled by setting the ADE bit in the VCO register. The ADC reading is latched by a subsequent programming of the ADC latch bit (ADL = 1). The ADC value is reported in the Status Byte-2 register (see Table 15).

Standby Mode

The MAX2121 features normal operating mode and standby mode using the I²C interface. Setting a logic-high to the STBY bit in the Control register puts the device into standby mode, during which only the 2-wire-compatible bus, the crystal oscillator, the XTAL buffer, and the XTAL buffer divider are active.

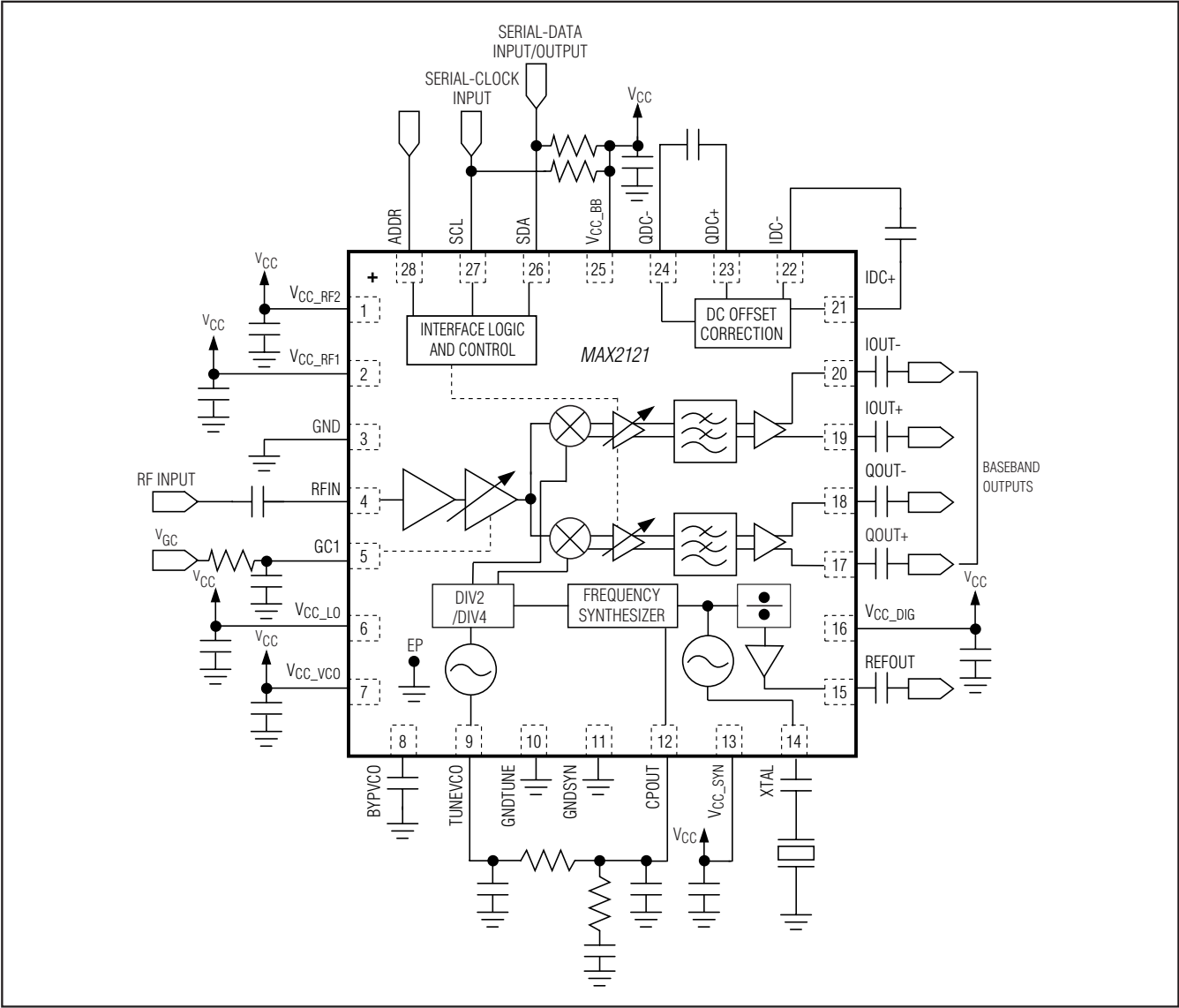
In all cases, register settings loaded prior to entering shutdown are saved upon transition back to active mode. Default register values are provided for the user's convenience only. It is the user's responsibility to load all the registers no sooner than 100μs after the device is powered up.

Layout Considerations

The MAX2121 EV kit serves as a guide for PCB layout. Keep RF signal lines as short as possible to minimize losses and radiation. Use controlled impedance on all high-frequency traces. For proper operation, the exposed paddle must be soldered evenly to the board's ground plane. Use abundant vias beneath the exposed paddle for maximum heat dissipation. Use abundant ground vias between RF traces to minimize undesired coupling. Bypass each V_{CC} pin to ground with a 1nF capacitor placed as close as possible to the pin.

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Typical Application Circuit



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-------------------------|-------------------------|
| 28 TQFN-EP | T2855+3 | 21-0140 | 90-0023 |

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Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|--------------------|------------------|---|------------------|
| 0 | 6/11 | Initial release | — |
| 1 | 7/12 | Corrected 2-tone frequencies, added new TOCs, added text to <i>Register Description</i> section, corrected incorrect symbol in Table 8, corrected <i>VCO Autoselect (VAS)</i> section | 4, 6, 10, 17 |

MAX2121

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