

## MAX20808

# Dual-Output 4A, 3MHz, 2.7V–16V Step-Down Switching Regulator

## General Description

The MAX20808/MAX20808T is a dual-output, fully integrated, highly efficient, step-down DC-DC switching regulator. The regulator is able to operate from 2.7V to 16V input supplies, and each output can be regulated from 0.5V to 5.8V, delivering up to 4A of load current per output. With the MAX20808, the two outputs can be connected in parallel as a single-output, dual-phase regulator that supports up to 8A load current.

The switching frequency of the device can be configured from 500kHz to 3MHz and provides the capability of optimizing the design in terms of solution size and performance.

The MAX20808/MAX20808T utilizes fixed-frequency, current-mode control with internal compensation. The dual-switching regulators operate 180° out-of-phase. The MAX20808/MAX20808T features a selectable advanced modulation scheme (AMS) to provide improved dynamic load transient performance. The device also features selectable discontinuous current mode (DCM) operation to improve light load efficiency. Operation settings and configurable features can be selected by connecting pin-strap resistors from the PGM\_ pins to ground.

The MAX20808/MAX20808T has an internal 1.8V low-dropout (LDO) output to power the gate drives (V<sub>CC</sub>) and internal circuitry (AVDD). The device also has an optional LDO input pin (LDOIN), allowing connection from a 2.5V to 5.5V bias input supply for optimized efficiency.

The MAX20808/MAX20808T integrates multiple protections including positive and negative overcurrent protection, output overvoltage protection, and overtemperature protection to ensure a robust design.

The MAX20808/MAX20808T is available in a compact 3.5mm x 4.6mm FC2QFN package that supports -40°C to +125°C junction temperature operation. The MAX20808 package has an open top, and MAX20808T package has a closed top.

## Applications

- Communications Equipment
- Networking Equipment
- Servers and Storage Equipment
- Point-of-Load Voltage Regulators
- μP Chipsets
- Memory V<sub>DDQ</sub>
- I/O Pins of an FPGA/DSP/MCU

## Benefits and Features

- High-Power Density with Low Component Count
  - Dual-Output or Dual-Phase Operation
  - Single-Supply Operation with Integrated LDO for Bias Generation
  - Optional 2.5V to 5.5V External Bias for Higher Efficiency
  - Compact 3.5mm x 4.6mm, 21-Pin, FC2QFN Package
  - Internal Compensation
- Wide Operating Range
  - 2.7V to 16V Input Voltage Range
  - 0.5V to 5.8V Output Voltage Range
  - 500kHz to 3MHz Configurable Switching Frequency
  - -40°C to +125°C Junction Temperature Range
  - Three Pin-Strap Programming Pins to Select Different Configurations
  - Independent Enable and Power Good for Each Output
- Optimized Performance and Efficiency
  - 92.5% Peak Efficiency with V<sub>DDH</sub> = 12V, V<sub>OUT</sub> = 1.8V, and f<sub>SW</sub> = 1MHz
  - Interleaved 180° Out-of-Phase Operation
  - Selectable AMS to Improve Load Transient
  - Selectable DCM to Improve Light Load Efficiency
  - Active Current Balancing for Dual-Phase Operation (MAX20808 only)

## Electrical and Thermal Ratings

DESCRIPTION	CURRENT RATING* (DUAL-PHASE) (A)	INPUT VOLTAGE (V)	OUTPUT VOLTAGE (V)
Electrical Rating	8	2.7 to 16	0.5 to 5.8
Thermal Rating TA = 85°C, no air flow	8	12	5.0
Thermal Rating TA = 55°C, 200LFM	8	12	5.0

\*Maximum T<sub>J</sub> = 125°C. For specific operating conditions, see the Safe Operating Area (SOA) curves in the [Typical Operating Characteristics](#) section.

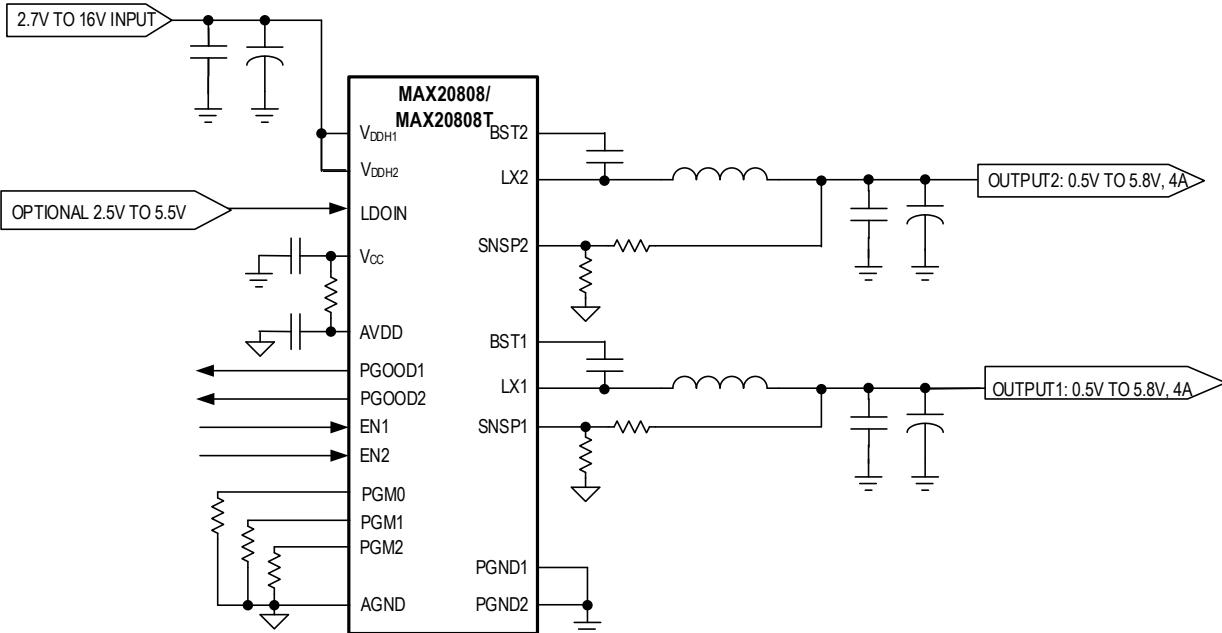
Click [here](#) for production status of specific part numbers.

MAX20808

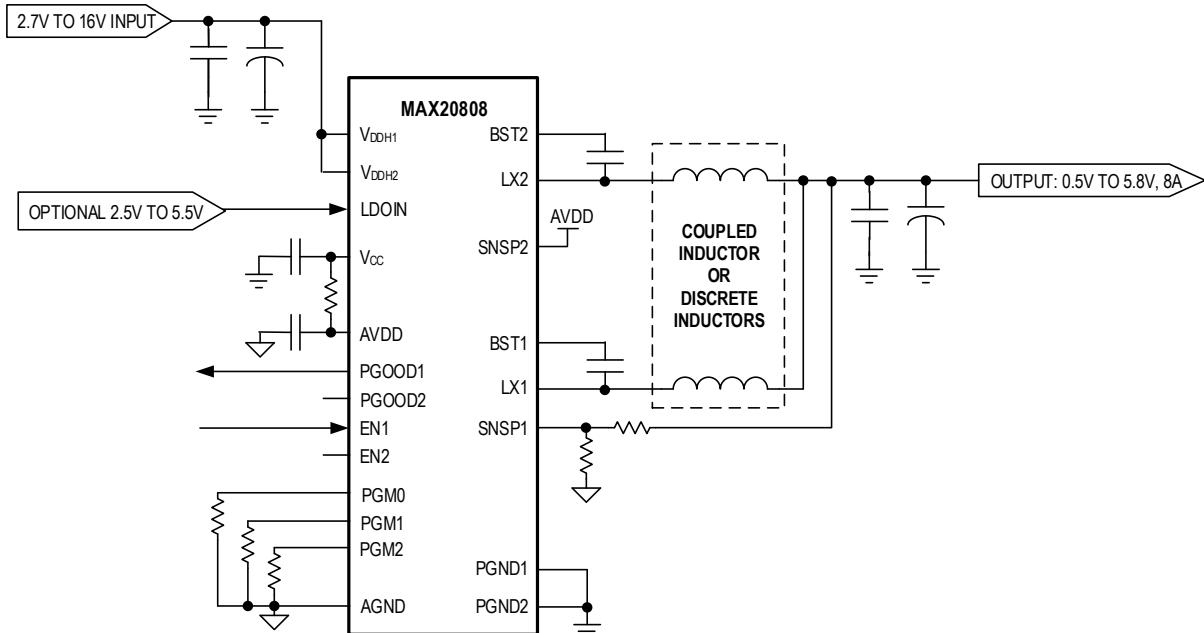
Dual-Output 4A, 3MHz, 2.7V–16V Step-Down  
Switching Regulator

## SIMPLIFIED APPLICATION CIRCUIT

### MAX20808/MAX20808T DUAL-OUTPUT APPLICATION CIRCUIT



### MAX20808 SINGLE-OUTPUT DUAL-PHASE APPLICATION CIRCUIT



**Absolute Maximum Ratings**

V <sub>DDH1</sub> , V <sub>DDH2</sub> to PGND (Note 1).....	-0.3V to +19V	PGND to AGND .....	-0.3V to +0.3V
LX1, LX2 to PGND (DC).....	-0.3V to +19V	V <sub>CC</sub> to PGND .....	-0.3V to +2.5V
LX1, LX2 to PGND (AC) (Note 2) .....	-10V to +23V	AVDD to AGND.....	-0.3V to +2.5V
V <sub>DDH1</sub> to LX1 (DC) (Note 1).....	-0.3V to +19V	EN1, EN2 to AGND.....	-0.3V to +4V
V <sub>DDH1</sub> to LX1 (AC) (Note 2) .....	-10V to +19V	PGOOD1, PGOOD2 to AGND .....	-0.3V to +4V
V <sub>DDH2</sub> to LX2 (DC) (Note 1).....	-0.3V to +19V	SNSP1, SNSP2 to AGND .....	-0.3V to AVDD+0.3V
V <sub>DDH2</sub> to LX2 (AC) (Note 2) .....	-10V to +19V	LDOIN to AGND.....	-0.3V to +6V
BST1, BST2 to PGND (DC).....	-0.3V to +21.5V	PGM0, PGM1, PGM2 to AGND .....	-0.3V to AVDD+0.3V
BST1, BST2 to PGND (AC) (Note 2) .....	-7V to +25.5V	Peak LX_ Current .....	-12A to +19A
BST1 to LX1 .....	-0.3V to +2.5V	Junction Temperature (T <sub>J</sub> ) .....	+150°C
BST2 to LX2 .....	-0.3V to +2.5V	Storage Temperature Range .....	-65°C to +150°C
		Peak Reflow Temperature Lead-Free .....	+260°C

**Note 1:** Input high-frequency (HF) capacitors placed not more than 40 mils away from the V<sub>DDH</sub> pins are required to keep inductive voltage spikes within the Absolute Maximum limits.

**Note 2:** AC is limited to 25ns.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Package Information****21 FC2QFN**

Part Number	MAX20808 (Open Top)	MAX20808T (Closed Top)
Package Code	F213A4F+1	F213A4F+2
Outline Number	<a href="#">21-100394</a>	<a href="#">21-100513</a>
Land Pattern Number	<a href="#">90-100134</a>	<a href="#">90-100184</a>
Thermal Resistance, Four Layer Board:		
Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ ) JEDEC	44.96°C/W	43.9°C/W
Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ ) on MAX20808EVKIT#	20°C/W	20°C/W
Junction-to-Case Thermal Resistance ( $\theta_{JC}$ )	0.51°C/W	10.1°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](#). Note that a "+" "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](#).

**Electrical Characteristics**

(Refer to [Typical Application Circuits](#),  $V_{DDH1} = V_{DDH2} = 12V$ ,  $V_{LDOIN} = 3.3V$ ,  $T_A = T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Specifications are production tested at  $T_A = +32^{\circ}C$ ; limits within the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>INPUT SUPPLY</b>						
Input Voltage Range	$V_{DDH}$		2.7	16		V
Input Supply Current	$I_{VDDH}$	$V_{LDOIN} = 3.3V$ , $EN_- = AGND$	0.1			mA
		$V_{LDOIN} = AVDD$ , $EN_- = AGND$	2.2			
Linear Regulator Input Voltage	$V_{LDOIN}$		2.5	5.5		V
Linear Regulator Input Current	$I_{LDOIN}$	$V_{LDOIN} = 3.3V$ , $EN_- = AGND$	2.6			mA
		$V_{LDOIN} = 3.3V$ , $EN_- = 1.8V$ , $f_{SW} = 1MHz$	22.1			
Internal LDO Regulated Output	$V_{CC}$		1.71	1.95		V
Linear Regulator Current Limit		$V_{LDOIN} = AVDD$	80			mA
		$V_{LDOIN} = 3.3V$	100			
		$V_{CC} < 1.6V$	20			
AVDD Undervoltage Lockout	$AVDD_{UVLO}$	Rising	1.65	1.67	1.70	V
AVDD Undervoltage Lockout Hysteresis				55		mV
$V_{DDH}$ Undervoltage Lockout	$V_{DDH\_UVLO}$	Rising	2.4	2.5	2.6	V
$V_{DDH}$ Undervoltage Lockout Hysteresis				100		mV
LDOIN Undervoltage Lockout	$V_{LDOIN\_UVLO}$		2.2	2.3	2.4	V
LDOIN Undervoltage Lockout Hysteresis	$V_{LDOIN\_UVLO}$			100		mV
<b>OUTPUT VOLTAGE RANGE AND ACCURACY</b>						
Internal Reference Voltage		MAX20808	0.4945	0.500	0.5055	V
		MAX20808T	0.496	0.500	0.504	
		$T_A = T_J = 0^{\circ}C$ to $+85^{\circ}C$	0.497	0.500	0.503	
Voltage Sense Leakage Current	$I_{SNSP\_}$	$T_A = T_J = +25^{\circ}C$			1	$\mu A$
<b>SWITCHING FREQUENCY</b>						
Switching Frequency	$f_{SW\_}$		500			kHz
			750			
			1000			
			1500			
			2000			
			3000			
Switching Frequency Accuracy			-10		+10	%

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Switching Regulator

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Phase Shift Between Two Outputs/Phases		$f_{SW1} = f_{SW2}$		180		°
Minimum Controllable On-Time		MAX20808, $I_{OUT} = 0A$ (Note 3)	40	47		ns
		MAX20808T, $I_{OUT} = 0A$ (Note 3)	32	40		
		MAX20808T, $I_{OUT} = 1A$ (Note 3)	27	37		
Minimum Controllable Off-Time		$I_{OUT} = 0A$ (Note 3)	100	110		ns
<b>ENABLE AND STARTUP</b>						
Initialization Time	$t_{INIT}$		800			μs
EN_ Threshold		Rising	0.9			V
		Falling		0.6		
EN_ Filtering Delay	$t_{EN\_RISING\_DELAY}$	Rising	200			μs
	$t_{EN\_FALLING\_DELAY}$	Falling	2			
Soft-Start Time	$t_{SS}$		3			ms
<b>POWER GOOD AND FAULT PROTECTIONS</b>						
PGOOD_ Output Low		$I_{PGOOD} = 4mA$		0.4		V
Output Undervoltage (UV) Threshold			-16	-13	-10	%
Output UV Deglitch Delay			4			μs
Output Overvoltage Protection (OVP) Threshold			10	13	16	%
Output OVP Deglitch Delay			2			μs
Positive Overcurrent Protection (POCP) Threshold	POCP	Inductor Peak Current, $POCP = 5.3A$	4.80	5.33	5.86	A
		Inductor Peak Current, $POCP = 4A$	3.58	4.00	4.50	
POCP Deglitch Delay			36			ns
Fast Positive Overcurrent Protection (FPOCP) Threshold	FPOCP		12.5	14.5	16.5	A
Negative Overcurrent Protection (NOCP) Threshold to POCP Threshold Ratio	NOCP	With respect to POCP threshold (typ)		-83		%
NOCP Accuracy			-20		+20	%
BST UVLO Threshold	$V_{BST}$	Rising	1.47	1.57	1.62	V
BST UVLO Threshold Hysteresis			60			mV

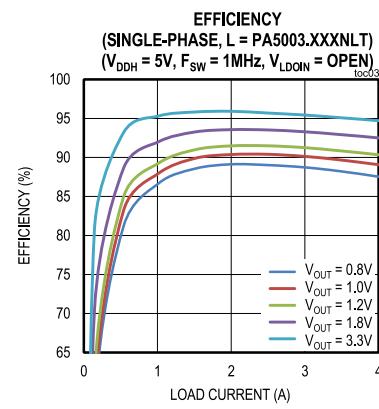
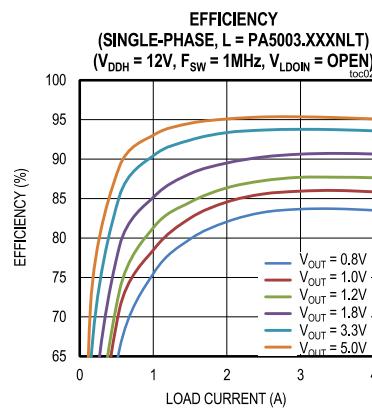
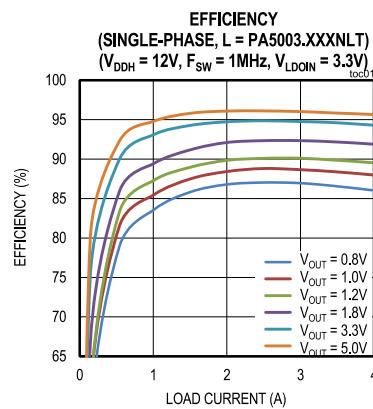
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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Overtemperature Protection (OTP) Rising Threshold	OTP			155		°C
OTP Accuracy				6		%
OTP Hysteresis				20		°C
Hiccup Protection Time	$t_{HICCUP}$			20		ms
<b>DCM OPERATION MODE</b>						
DCM Comparator Threshold to Enter DCM		POCP = 5.3A, Inductor Valley Current	-300			mA
		POCP = 4A, Inductor Valley Current	-215			
DCM Comparator Threshold to Exit DCM		Inductor Valley Current	100			mA
<b>PROGRAMMING PINS</b>						
PGM_ Pin Resistor Range	$R_{PGM\_}$		0.095	115		kΩ
PGM_ Resistor Accuracy			-1	+1		%

**Note 3:** Guaranteed by design.

## Typical Operating Characteristics

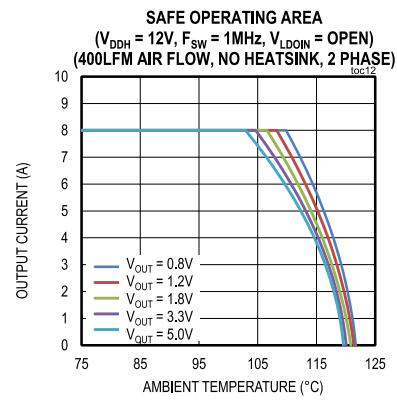
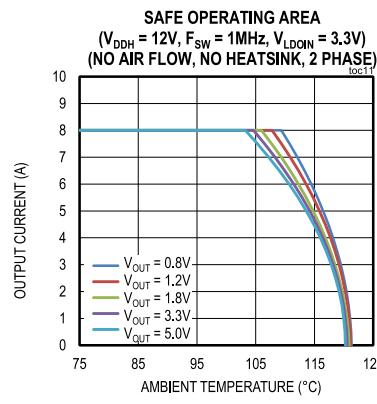
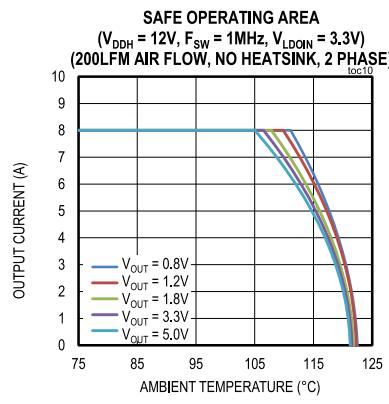
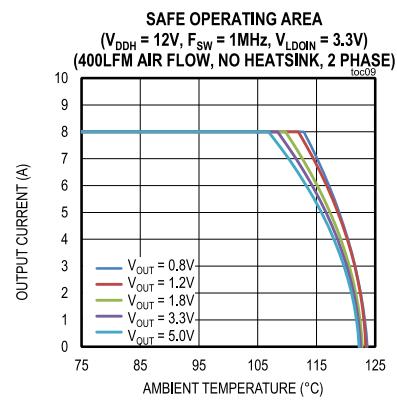
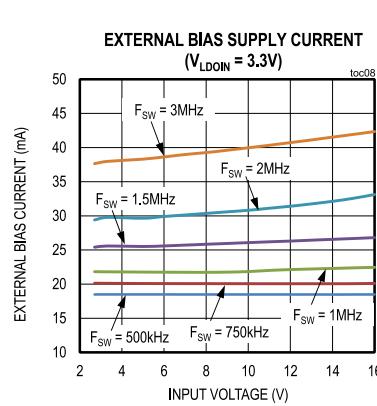
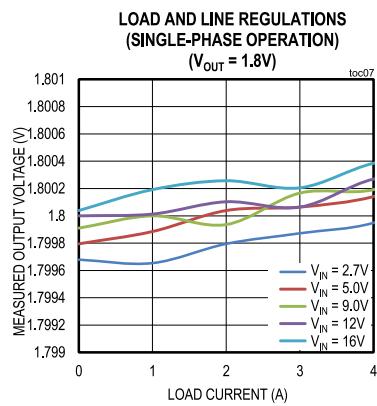
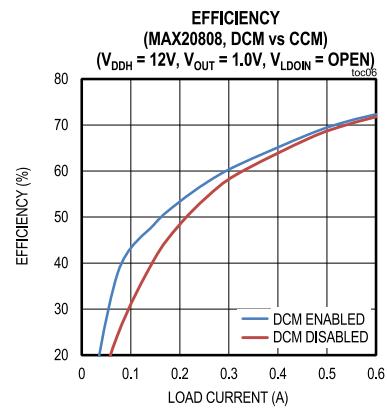
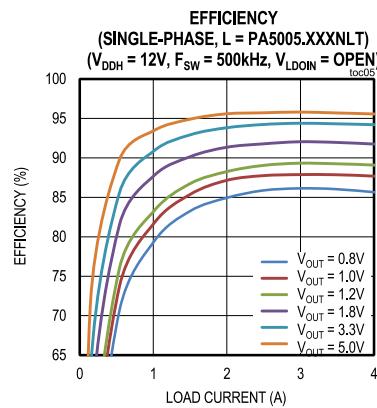
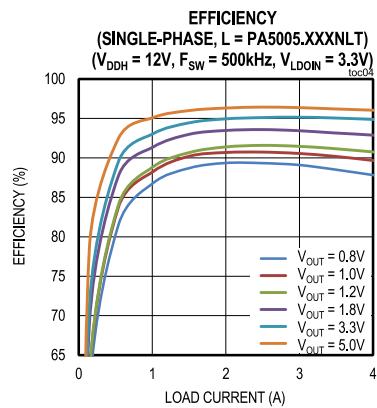
( $V_{DDH} = 12V$ , tested on MAX20808EVKIT#,  $T_A = +25^{\circ}C$ , unless otherwise noted.)



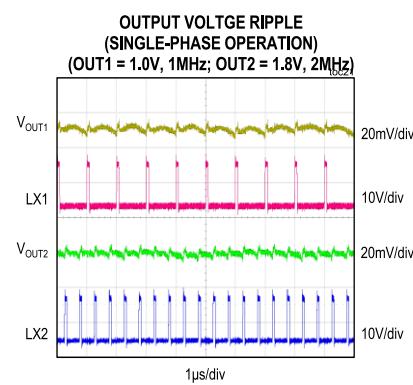
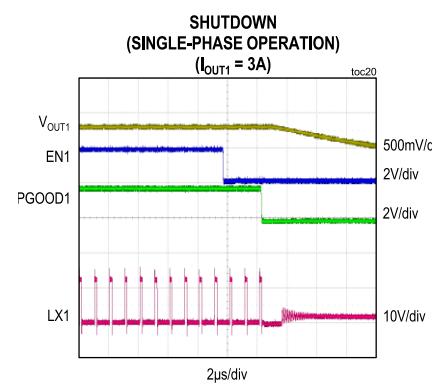
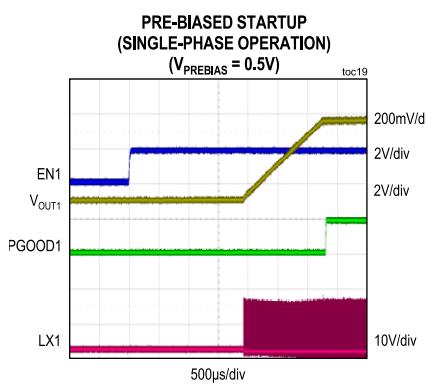
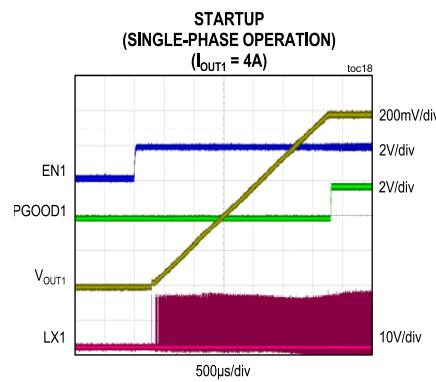
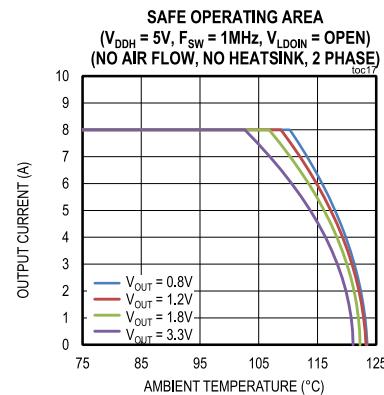
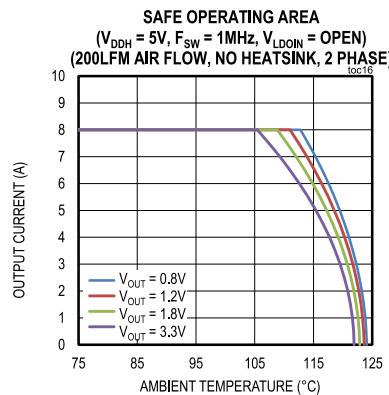
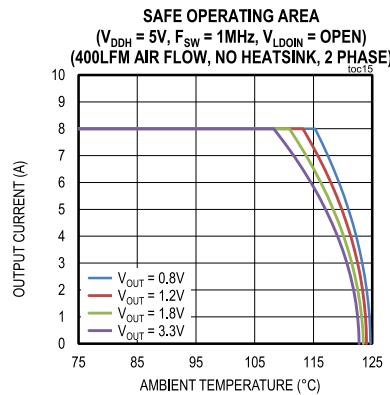
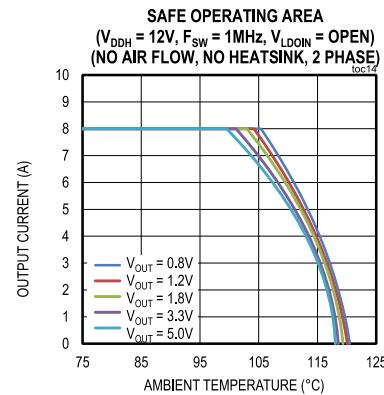
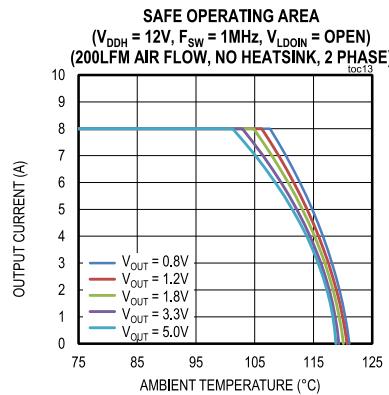
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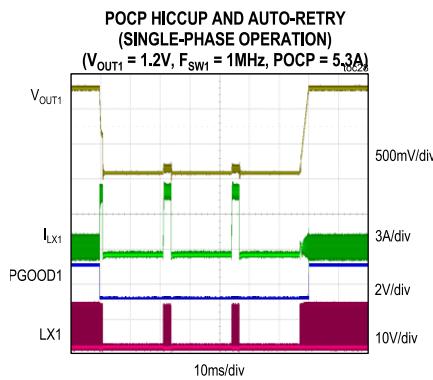
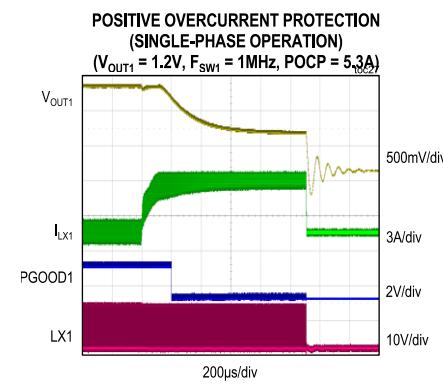
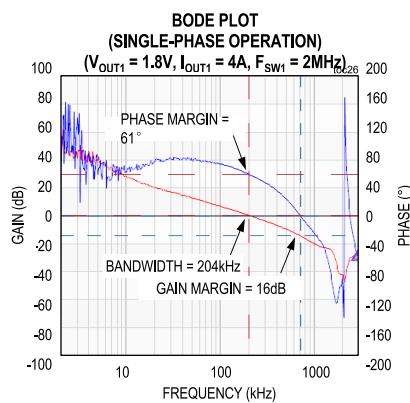
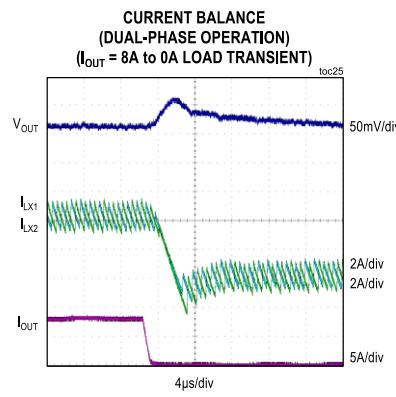
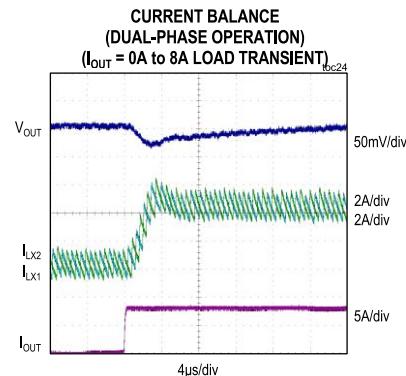
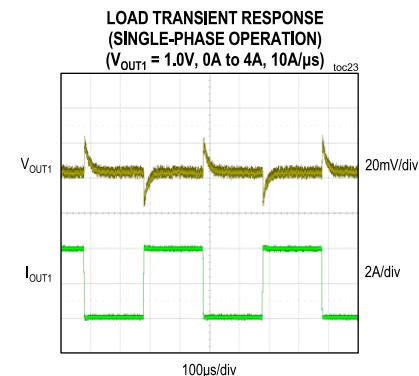
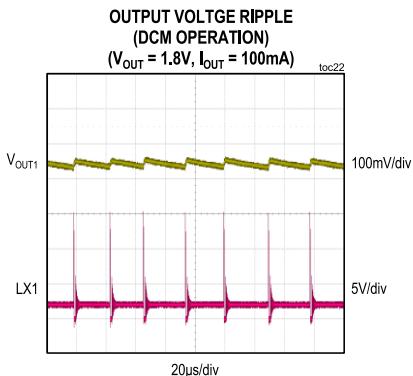
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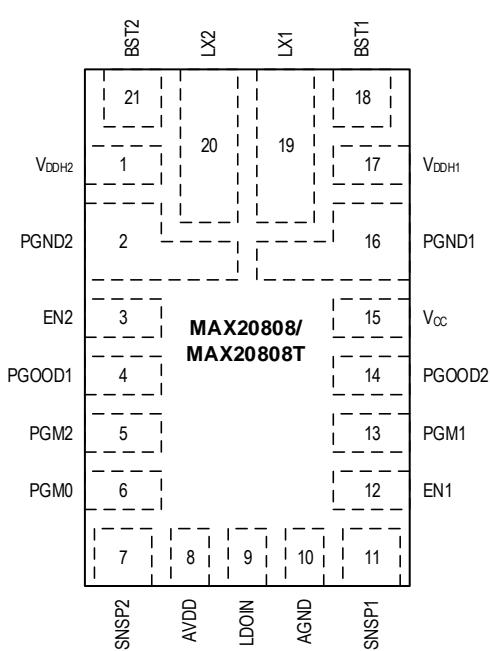
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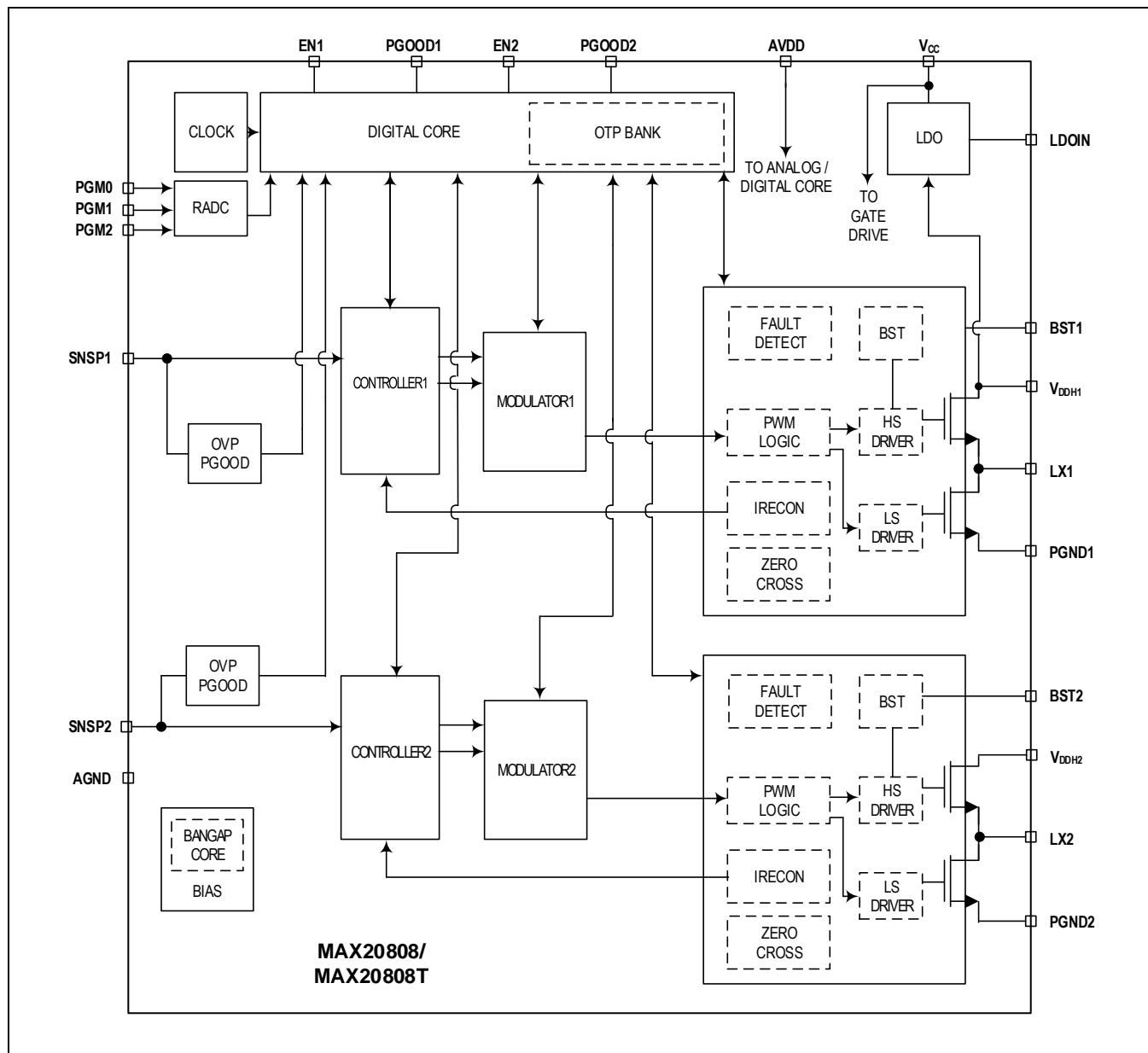
## Pin Configurations



## Pin Descriptions

PIN	NAME	FUNCTION
1	V <sub>DDH2</sub>	Regulator Input Supply for Output 2. V <sub>DDH1</sub> and V <sub>DDH2</sub> should be connected on the PCB.
2	PGND2	Power Ground. PGND1 and PGND2 should be connected on the PCB.
3	EN2	Output Enable for Output 2.
4	PGOOD1	Open-Drain Power-Good Output for Output 1.
5	PGM2	Program Input. Connect this pin to ground though a programming resistor.
6	PGM0	Program Input. Connect this pin to ground though a programming resistor.
7	SNSP2	Output 2 Voltage Sense Feedback Pin. Connect SNSP2 to V <sub>OUT2</sub> at the load. A resistive voltage-divider can be inserted between the output and SNSP2 to regulate the output above the 0.5V fixed reference voltage. Connect SNSP2 to AVDD to select dual-phase operation.
8	AVDD	1.8V Supply for Analog Circuitry. Connect a 2.2Ω to 4.7Ω resistor from AVDD to V <sub>CC</sub> . Connect a 1μF or greater ceramic capacitor from AVDD to AGND.
9	LDOIN	Optional 2.5V to 5.5V LDO Input Supply. Connect this pin to AVDD or GND, or leave this pin floating if unused.
10	AGND	Analog Ground.
11	SNSP1	Output 1 Voltage Sense Feedback Pin. Connect SNSP1 to V <sub>OUT1</sub> at the load. A resistive voltage-divider can be inserted between the output and SNSP1 to regulate the output above the 0.5V fixed reference voltage.
12	EN1	Output Enable for Output 1.

13	PGM1	Program Input. Connect this pin to ground though a programming resistor.
14	PGOOD2	Open-Drain Power-Good Output for Output 2.
15	V <sub>CC</sub>	Internal 1.8V LDO Output. Connect a 2.2 $\mu$ F or greater ceramic capacitor from V <sub>CC</sub> to PGND.
16	PGND1	Power Ground. PGND1 and PGND2 should be connected on the PCB.
17	V <sub>DDH1</sub>	Regulator Input Supply for Output 1. V <sub>DDH1</sub> and V <sub>DDH2</sub> should be connected on the PCB.
18	BST1	Bootstrap Pin for Output 1. Connect a 0.22 $\mu$ F ceramic capacitor from BST1 to LX1.
19	LX1	Switching Node of Output 1. Connect LX1 directly to the output inductor.
20	LX2	Switching Node of Output 2. Connect LX2 directly to the output inductor.
21	BST2	Bootstrap Pin for Output 2. Connect a 0.22 $\mu$ F ceramic capacitor from BST2 to LX2.

**Block Diagram****Detailed Description****Dual-Output or Dual-Phase Operation**

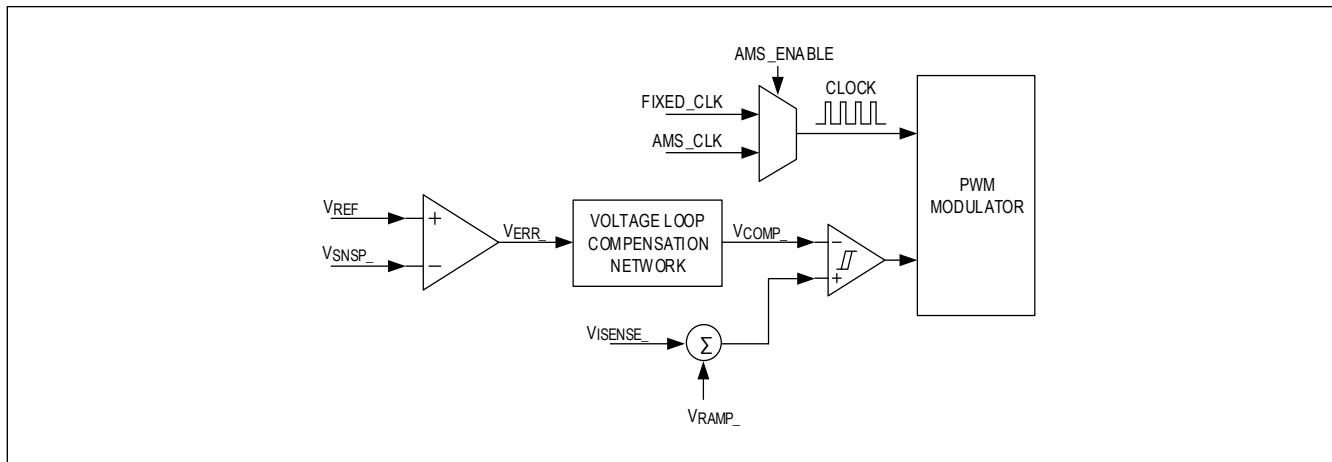
The MAX20808/MAX20808T by default is configured as dual-output step-down regulators. These devices have two independent control loops for the two outputs and the loop parameters can be independently selected.

The MAX20808 only can also be configured as a single-output, dual-phase 8A converter by connecting the SNSP2 pin to AVDD. When configured to dual-phase operation, only the control loop for OUTPUT1 works, and the control loop for OUTPUT2 is bypassed. The EN1 and PGOOD1 pins are used in dual-phase operation mode to enable the device and indicate power-good status. The EN2 and PGOOD2 pins can be disconnected.

## Control Architecture

### Fixed-Frequency, Peak Current-Mode Control Loop

The MAX20808/MAX20808T control loops are based on fixed-frequency, peak current-mode control architecture. A simplified control architecture is shown in [Figure 1](#). Each loop contains an error amplifier stage, internal voltage loop compensation network, current sense, internal slope compensation, and a PWM modulator that generates the pulse-width modulation (PWM) signals to drive high-side and low-side MOSFETs. The device has a fixed 0.5V reference voltage ( $V_{REF}$ ). The difference of  $V_{REF}$  and the sensed output voltage is amplified by the first error amplifier. Its output voltage ( $V_{ERR}$ ) is used as the input of the voltage loop compensation network. The output of the compensation network ( $V_{COMP}$ ) is fed to a PWM comparator with the current-sense signal ( $V_{ISENSE}$ ) and slope compensation ( $V_{RAMP}$ ). The output of the PWM comparator is the input of the PWM modulator. The turning on of the high-side MOSFET is aligned with an internal clock. It can either be a fixed-frequency clock or a phase-shifted clock if AMS is enabled.



*Figure 1. Simplified Control Architecture*

### Advanced Modulation Scheme

The MAX20808/MAX20808T offers a selectable AMS to provide improved dynamic load transient response. The AMS provides a significant advantage over conventional fixed-frequency PWM schemes. Enabling the AMS feature allows for modulation at both leading and trailing edges, which results in a fast-switching response during large load transients. [Figure 2](#) shows the scheme to include leading-edge modulation to the traditional trailing-edge modulation when AMS is enabled in the device. The modulation scheme allows the turn on and off with minimal delay. Since the total inductor current increases very quickly, thus satisfying the load demand, the current drawn from the output capacitors is reduced. With AMS enabled, the system closed-loop bandwidth can be extended without phase-margin penalty. As a result, the output capacitance can be minimized.

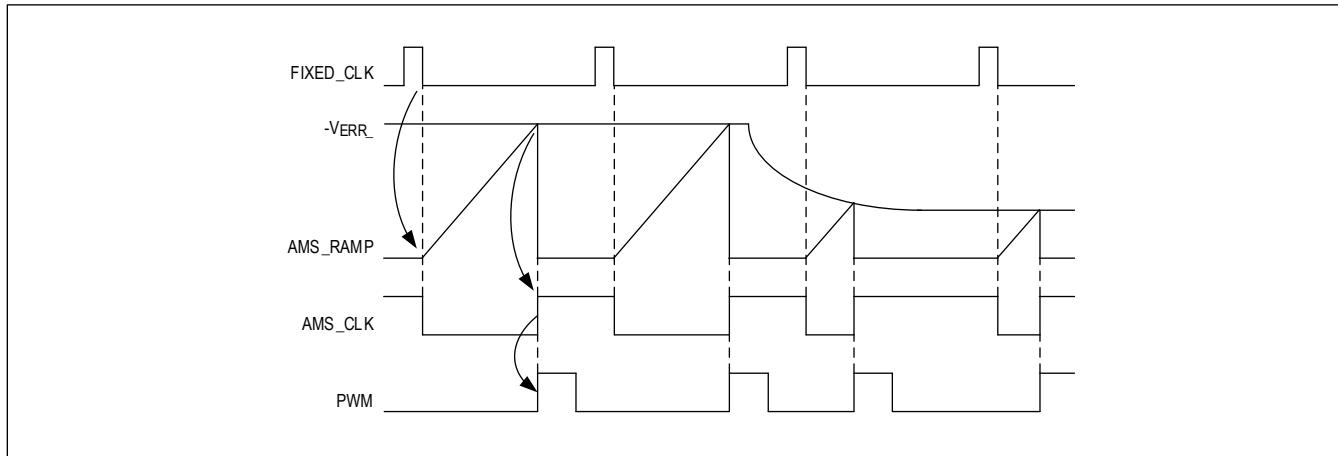


Figure 2. AMS Operation

### Discontinuous Current Mode Operation

The discontinuous current mode operation can be enabled to improve light-load efficiency. It is required that  $V_{DDH}$  is at least 2V higher than the desired  $V_{OUT}$  for the device to operate in DCM. The device has a DCM current-detection comparator to monitor the inductor valley current while operating in continuous-conduction mode (CCM). At light load, if the inductor valley current is below the DCM comparator threshold for 48 consecutive cycles, the device transitions seamlessly to DCM. Once in DCM, the switching frequency decreases as load decreases. The MAX20808/MAX20808T transitions back to CCM operation as soon as the inductor valley current is higher than 100mA.

### Active Current Balancing

When the MAX20808 is configured to dual-phase operation, the MAX20808 operates with active current balancing for enhanced dynamic-current sharing or balancing between two-phase currents. This feature maintains the current balance during load transients, even at a load-step frequency close to the switching frequency or its harmonics. The active current-balancing circuit adjusts the individual phase-current control signal in order to minimize the phase-current imbalance.

### Internal Linear Regulator

The MAX20808/MAX20808T contains an internal 1.8V linear regulator. The 1.8V voltage on  $V_{CC}$  is derived from the  $V_{DDH1}$  pin by default. To improve efficiency, it is recommended to apply an external 2.5V to 5.5V bias input supply on the LDOIN pin so that the 1.8V voltage on  $V_{CC}$  is converted from the LDOIN pin instead. The LDOIN pin can be connected to the output voltage if the output voltage falls within the 2.5V–5.5V range. The optional LDOIN bias input supply can be applied or removed anytime during regulation without affecting the regulation.

The 1.8V voltage on the  $V_{CC}$  pin supplies the current to the MOSFET drivers of both outputs. A decoupling capacitor of at least  $2.2\mu F$  must be connected between  $V_{CC}$  and PGND. The AVDD pin also requires a 1.8V supply to power the device's internal analog circuitry. A  $2.2\Omega$  to  $4.7\Omega$  resistor must be connected between AVDD and  $V_{CC}$ . A  $1\mu F$  or greater decoupling capacitor must be used between AVDD and AGND.

### Startup and Shutdown

The startup and shutdown timing is shown in **Figure 3**. When the AVDD pin voltage is above its rising UVLO threshold, the device goes through an initialization procedure. The dual-output or dual-phase operation is detected. Configuration resistors on the PGM\_ pins are read. Once initialization is complete, the device detects the  $V_{DDH}$  UVLO and EN\_ status. When both are above their rising thresholds, soft-start begins and switching is enabled. The output voltage of the enabled output starts to ramp up. The soft-start ramp time is 3ms. If there are no faults, the open-drain PGOOD\_ pin is released from being held low after the soft-start ramp is complete. The device supports smooth startup with the output prebiased.

During operation, if either  $V_{DDH}$  UVLO or  $EN_-$  falls below its threshold, switching is stopped immediately. The  $PGOOD_-$  pin is driven low. The output voltage is discharged by the load current.

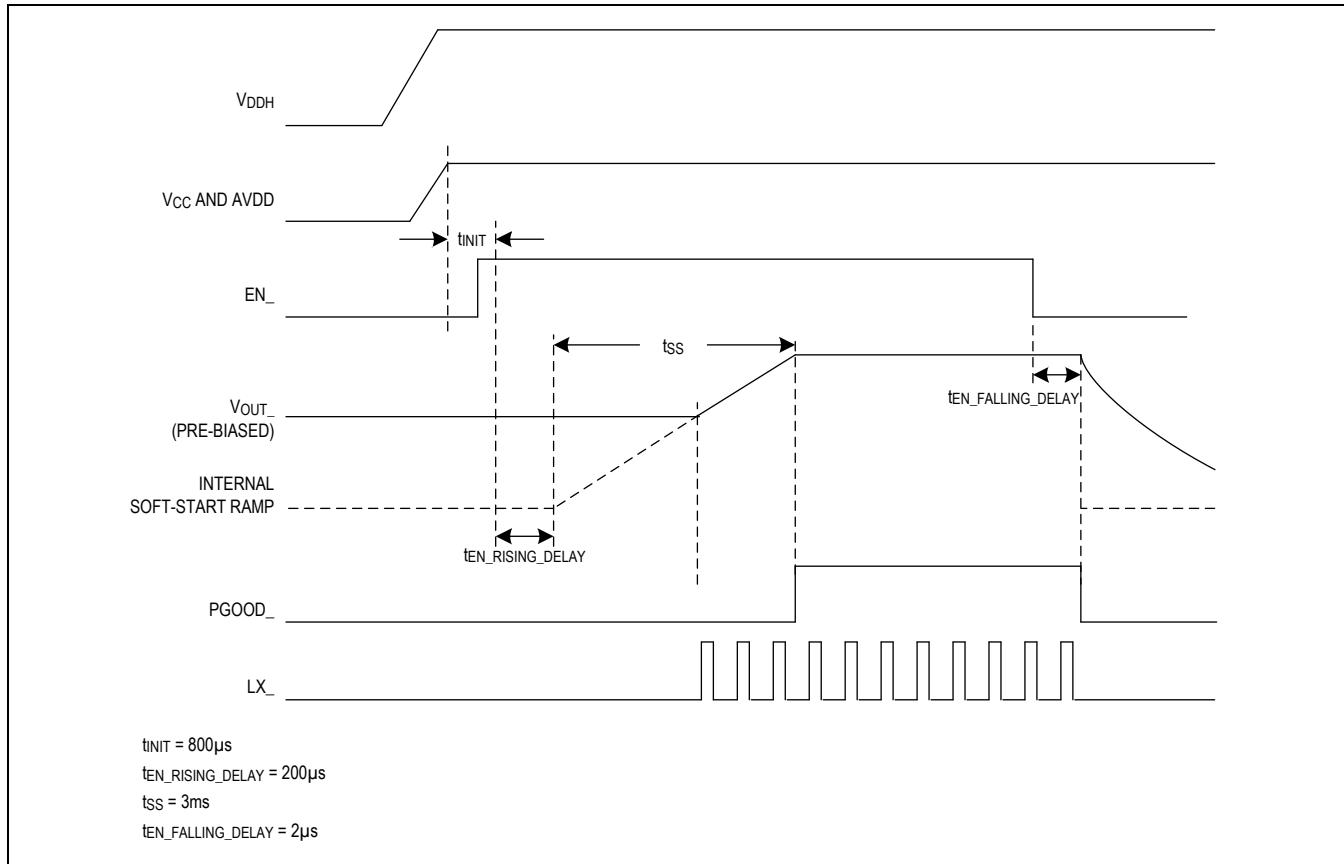


Figure 3. Startup and Shutdown Timing

## Fault Handling

### Input Undervoltage Lockout ( $V_{DDH}$ UVLO)

The MAX20808/MAX20808T internally monitors  $V_{DDH}$  with a UVLO circuit. When the input supply voltage is below the UVLO threshold, the device stops switching and drives the  $PGOOD_-$  pin low. The device restarts after 20ms hiccup protection time if the  $V_{DDH}$  UVLO status is cleared. Refer to the [Startup and Shutdown](#) section for the startup sequence.

### Output Overvoltage Protection (OVP)

The feedback voltage on  $SNSP_-$  is monitored for overvoltage once the soft-start ramp is complete. If the feedback voltage is above the OVP threshold beyond the OVP deglitch filtering delay, the device stops switching and drives the  $PGOOD_-$  pin low. The device restarts after 20ms hiccup protection time if the OVP status is cleared. When configured to dual-output operation, the OVP of one output does not affect the operation of the other output.

### Positive Overcurrent Protection (POCP)

The device's peak current mode control architecture provides inherent current limiting and short-circuit protection. The inductor current is continuously monitored while switching. The inductor peak current is limited on a cycle-by-cycle basis. In each switching cycle, once the sensed inductor current exceeds the POCP threshold, the device turns off the high-side MOSFET and turns on the low-side MOSFET to allow the inductor current to be discharged by output voltage. An up-down counter is used to accumulate the number of consecutive POCP events each switching cycle. If the counter exceeds

1024, the device stops switching and drives the PGOOD<sub>\_</sub> pin low. The device restarts after 20ms hiccup protection time. When configured to dual-output operation, the POCP of one output does not affect the operation of the other output.

The MAX20808 offers two POCP thresholds (5.3A and 4A) for each output, which can be selected by the PGM1 and PGM2 pins (refer to [Pin-Strap Programmability](#) section). Due to POCP deglitch delay, for a specific application use case, the actual POCP threshold should be higher (refer to [Output Inductor Selection](#) section).

### Negative Overcurrent Protection (NOCP)

The device also has negative overcurrent protection against inductor valley current. The NOCP threshold is -83% of the POCP threshold. In each switching cycle, once the sensed inductor current exceeds the NOCP threshold, the device turns off the low-side MOSFET and turns on the high-side MOSFET for a fixed 180ns time to allow the inductor current to be charged by input voltage. Same as the POCP, an up-down counter is used to accumulate the number of consecutive NOCP events. If the counter exceeds 1024, the device stops switching and drives the PGOOD<sub>\_</sub> pin low. The device restarts after 20ms hiccup protection time. When configured to dual-output operation, the NOCP of one output does not affect the operation of the other output.

### Overtemperature Protection (OTP)

The overtemperature protection threshold is +155°C with 20°C hysteresis. If the junction temperature reaches OTP threshold during operation, the device stops switching and drives the PGOOD<sub>\_</sub> pin low. The device restarts if the OTP status is cleared.

### Pin-Strap Programmability

The MAX20808/MAX20808T has three program pins (PGM0, PGM1, and PGM2) to set some of the key configurations of the device. A pin-strap resistor is connected from the PGM<sub>\_</sub> pin to AGND, and its value is read during startup initialization. The PGM0 selects the common settings that apply to both outputs (AMS, DCM, and switching frequencies). When the device is configured to dual-output operation, the PGM1 selects the POCP and internal compensation parameters of OUTPUT1; the PGM2 selects the POCP and internal compensation parameters of OUTPUT2. When the device is configured to dual-phase operation, the POCP and internal compensation parameters are selected only by PGM1. Refer to the [Internal Compensation Selection](#) section for information about how to select the compensation parameters for optimized control loop performance.

**Table 1. PGM0 Configurations**

PGM0 CODES	R (Ω)	AMS	DCM	f <sub>SW1</sub> (kHz)	f <sub>SW2</sub> (kHz)
0	95.3	Disable	Disable	500	500
1	200			500	1000
2	309			750	750
3	422			750	1500
4	536			1000	500
5	649			1000	1000
6	768			1000	2000
7	909			1500	750
8	1050			1500	1500
9	1210			2000	1000
10	1400			2000	2000
11	1620			3000	3000
12	1870	Enable	Enable	500	500
13	2150			500	1000
14	2490			750	750
15	2870			750	1500
16	3740			1000	500
17	8060			1000	1000
18	12400			1000	2000
19	16900			1500	750

20	21500	Enable	1500	1500
21	26100		2000	1000
22	30900		2000	2000
23	36500		3000	3000
24	42200		500	500
25	48700		500	1000
26	56200		750	750
27	64900		1000	500
28	75000		1000	1000
29	86600		1500	1500
30	100000		2000	2000
31	115000		3000	3000

**Table 2. PGM1 Configurations for OUTPUT1 or Dual-Phase Operation**

PGM1 CODES	R ( $\Omega$ )	POCP1 (A)	VOLTAGE LOOP GAIN MULTIPLIER 1	SLOPE1 ( $\mu$ A)
0	95.3	5.3	0.4	1.5
1	200			2.6
2	309			3.7
3	422			6.0
4	536			7.0
5	649			8.0
6	768		0.7	1.5
7	909			2.6
8	1050			3.7
9	1210			6.0
10	1400			7.0
11	1620			8.0
12	1870	1	1	1.5
13	2150			2.6
14	2490			3.7
15	2870			6.0
16	3740			7.0
17	8060			8.0
18	12400	1.5	1.5	1.5
19	16900			2.6
20	21500			3.7
21	26100			6.0
22	30900			7.0
23	36500	4	0.4	1.5
24	42200			2.6
25	48700			7.0
26	56200		0.7	1.5
27	64900			2.6
28	75000			7.0
29	86600	1	1	1.5
30	100000			2.6
31	115000			7.0

**Table 3. PGM2 Configurations for OUTPUT2**

PGM2 CODES	R ( $\Omega$ )	POCP2 (A)	VOLTAGE LOOP GAIN MULTIPLIER 2	SLOPE2 ( $\mu$ A)
0	95.3	5.3	0.4	1.5
1	200			2.6
2	309			3.7
3	422			6.0
4	536			7.0
5	649			8.0
6	768		0.7	1.5
7	909			2.6
8	1050			3.7
9	1210			6.0
10	1400			7.0
11	1620			8.0
12	1870		1	1.5
13	2150			2.6
14	2490			3.7
15	2870			6.0
16	3740			7.0
17	8060			8.0
18	12400		1.5	1.5
19	16900			2.6
20	21500			3.7
21	26100			6.0
22	30900			7.0
23	36500	4	0.4	1.5
24	42200			2.6
25	48700			7.0
26	56200		0.7	1.5
27	64900			2.6
28	75000			7.0
29	86600		1	1.5
30	100000			2.6
31	115000			7.0

## Reference Design Procedure

### Output Voltage Sensing

The MAX20808/MAX20808T has an internal 0.5V reference voltage. When the desired output voltage is higher than 0.5V, it is required to use resistor-dividers  $R_{FB1}$  and  $R_{FB2}$  to sense the output voltage (refer to [Typical Application Circuits](#)). It is recommended that the value  $R_{FB2}$  does not exceed 5k $\Omega$ . The resistor-divider ratio is given by the following equation:

$$V_{OUT} = V_{REF} \times \left( 1 + \frac{R_{FB1}}{R_{FB2}} \right)$$

where

$V_{OUT}$  = Output voltage

$V_{REF}$  = 0.5V fixed reference voltage

$R_{FB1}$  = Top resistor-divider

$R_{FB2}$  = Bottom resistor-divider

### Switching Frequency Selection

The MAX20808/MAX20808T offers a wide range of selectable switching frequencies from 500kHz to 3MHz. Switching frequency selection can be optimized for different applications. Higher switching frequencies are recommended for applications prioritizing solution size so that the value and size of output LC filter can be reduced. Lower switching frequencies are recommended for applications prioritizing efficiency and thermal dissipation due to reduced switching losses. The frequency must be selected so that the minimum controllable on-time and minimum controllable off-time are not violated. The maximum recommended switching frequency is calculated by the following equation:

$$f_{SWMAX} = \text{MIN} \left\{ \frac{V_{OUT}}{t_{ONMIN} \times V_{DDHMAX}}, \frac{V_{DDHMIN} - V_{OUT}}{t_{OFFMIN} \times V_{DDHMIN}} \right\}$$

where

$f_{SWMAX}$  = Maximum selectable switching frequency

$V_{DDHMAX}$  = Maximum input voltage

$V_{DDHMIN}$  = Minimum input voltage

$t_{ONMIN}$  = Minimum controllable on-time

$t_{OFFMIN}$  = Minimum controllable off-time

Due to system noise injection, even at steady-state operation, typically the LX rising and falling edges would have some random jittering noise. The selection of the switching frequency ( $f_{SW}$ ) should take into consideration the jittering and be lower than  $f_{SWMAX}$ . To improve the LX jittering, it is recommended to use smaller inductor values and lower voltage loop gain to minimize the noise sensitivity.

### Output Inductor Selection

The output inductor has an important influence on the overall size, cost, and efficiency of the voltage regulator. Since the inductor is typically one of the larger components in the system, a minimum inductor value is particularly important in space-constrained applications. Smaller inductor values also permit faster transient response, reducing the amount of output capacitance needed to maintain transient tolerance.

To improve current loop noise immunity, typically the output inductor is selected so that the inductor current ripple is at least 1A. The inductor value is calculated by the following equation:

$$L = \frac{V_{OUT}(V_{DDH} - V_{OUT})}{V_{DDH} \times I_{RIPPLE} \times f_{SW}}$$

where

$V_{DDH}$  = Input voltage

$I_{RIPPLE}$  = Inductor current ripple peak-to-peak value

The inductor should also be selected so that maximum load current delivery can be guaranteed by the selected POCP threshold. The MAX20808/MAX20808T offers two POCP thresholds (5.3A and 4A) for each output, which can be selected by the PGM1 and PGM2 pins (refer to [Pin-Strap Programmability](#) section). Due to deglitch delay from the POCP comparator tripping to the high-side MOSFET turning off, for a specific application use case, the adjusted POCP threshold should take into consideration the inductor value, input voltage, and output voltage, which can be calculated by the following equation:

$$POCP_{ADJUST} = POCP + \frac{(V_{DDH} - V_{OUT}) \times t_{POCP}}{L}$$

where

POCP<sub>ADJUST</sub> = Adjusted POCP threshold

POCP = POCP level specified in the EC table

t<sub>POCP</sub> = POCP deglitch delay (36ns, typ)

It needs to be verified that the peak inductor current in normal operation does not exceed the minimum adjusted POCP threshold:

$$\frac{I_{OUTMAX}}{N} + \frac{I_{RIPPLE}}{2} < POCP_{ADJUST(MIN)}$$

where

N = Number of phases

I<sub>OUTMAX</sub> = Maximum load current

POCP<sub>ADJUST(MIN)</sub> = Minimum adjusted POCP threshold, calculated with the minimum value of the POCP threshold.

*Table 4* shows some suitable inductor part numbers which are verified on the MAX20808/MAX20808T evaluation kit to offer optimal performance.

**Table 4. Recommended Inductors**

COMPANY	VALUE (μH)	I <sub>SAT</sub> (A)	R <sub>DC</sub> (mΩ)	FOOTPRINT (mm)	HEIGHT (mm)	PART NUMBER
TDK	0.22	9	8	2.5 × 2.0	1.2	TFM252012ALMAR22MTAA
TDK	0.33	8.4	10	3.2 × 2.5	1.2	TFM322512ALMAR33MTAA
Pulse	0.47	26	3.75	5.5 × 5.3	2.9	PA5003.471NLT
Pulse	0.56	22.2	4.05	5.5 × 5.3	2.9	PA5003.561NLT
Pulse	1.0	16.5	6.9	5.5 × 5.3	2.9	PA5003.102NLT
Pulse	2.2	10	13.2	5.5 × 5.3	2.9	PA5003.222NLT

### Output Capacitor Selection

One major factor in determining the total required output capacitance is the output-voltage ripple. To meet the output-voltage ripple requirement, the minimum output capacitance should satisfy the following equation:

$$C_{OUT} \geq \frac{I_{RIPPLE}}{8 \times N \times f_{SW} \times (V_{OUTRIPPLE} - ESR \times I_{RIPPLE})}$$

where

V<sub>OUTRIPPLE</sub> = Maximum allowed output-voltage ripple

ESR = ESR of output capacitors

The other important factors in determining the total required output capacitance are the maximum allowable output-voltage overshoot and undershoot during load transients. For a given loading or unloading current step, the minimum required output capacitance should also satisfy the following equation:

$$C_{OUT} \geq \text{MAX} \left\{ \frac{\left( \frac{\Delta I}{N} + \frac{I_{RIPPLE}}{2} \right)^2 \times L \times N}{2 \times \Delta V_{OUT} \times (V_{DDH} - V_{OUT})}, \frac{\left( \frac{\Delta I}{N} + \frac{I_{RIPPLE}}{2} \right)^2 \times L \times N}{2 \times \Delta V_{OUT} \times V_{OUT}} \right\}$$

where

C<sub>OUT</sub> = Output capacitance

ΔI = Loading or unloading current step

$\Delta V_{OUT}$  = Maximum allowed output voltage undershoot or overshoot

### Input Capacitor Selection

The input capacitance selection is determined by the input voltage ripple requirement. The  $V_{DDH1}$  and  $V_{DDH2}$  pins of the MAX20808/MAX20808T should be connected on the PCB. When configured to dual-output operation, the input capacitance is shared between the two outputs. The minimum required input capacitance is estimated by the following equation:

$$C_{IN} \geq \text{MAX} \left\{ \frac{I_{OUT1(MAX)} \times V_{OUT1}}{f_{SW1} \times V_{DDH} \times V_{INPP}}, \frac{I_{OUT2(MAX)} \times V_{OUT2}}{f_{SW2} \times V_{DDH} \times V_{INPP}} \right\}$$

where

$C_{IN}$  = Input capacitance

$I_{OUT\_}(MAX)$  = Maximum output current of  $OUTPUT\_$

$V_{OUT\_}$  = Output voltage of  $OUTPUT\_$

$f_{sw\_}$  = Switching frequency of  $OUTPUT\_$

$V_{INPP}$  = Peak-to-peak input voltage ripple

When configured to dual-phase operation, the minimum required input capacitance is estimated by the following equation:

$$C_{IN} \geq \frac{I_{OUT(MAX)} \times V_{OUT}}{2 \times f_{SW} \times V_{DDH} \times V_{INPP}}$$

Besides the minimum required input capacitance, it is also required to place 0.1 $\mu$ F and 1 $\mu$ F high-frequency decoupling capacitors next to each  $V_{DDH\_}$  pin to suppress the high-frequency switching noises.

### Internal Compensation Selection

#### Voltage Loop Gain

For stability purposes, it is recommended that the voltage loop bandwidth (BW) be lower than one-fifth of the switching frequency. Consider the case of using multilayer ceramic chip (MLCC) output capacitors that have nearly ideal impedance characteristics in the frequency range of interest with negligible equivalent series resistance (ESR) and equivalent (or effective) series inductance (ESL). The voltage loop BW can be estimated with the following equation:

$$BW = \frac{N \times \frac{R_{FB2}}{R_{FB2} + R_{FB1}} \times \frac{R_{VGA}}{10k\Omega}}{2\pi \times 20m\Omega \times C_{OUT}}$$

where

$R_{VGA}$  = Voltage loop gain resistance, which is set by the switching frequency and voltage loop gain multiplier selected by  $PGM\_$  pin resistors ([Table 5](#))

**Table 5. Voltage Loop Gain Resistance**

SWITCHING FREQUENCY (kHz)	VOLTAGE LOOP GAIN MULTIPLIER	$R_{VGA}$ (k $\Omega$ )
500	0.4	15.6
	0.7	27
	1	37
	1.5	52.2
750	0.4	22

	0.7	31
	1	44.5
	1.5	62.3
1000	0.4	22
	0.7	37
	1	52.2
	1.5	74.5
1500	0.4	27
	0.7	44.5
	1	62.3
	1.5	104.4
2000 or 3000	0.4	31
	0.7	52.2
	1	74.5
	1.5	104.4

### Slope Compensation

Slope compensation is applied to guarantee current loop stability when the duty cycle is higher than 50%. For applications where the duty cycle is smaller than 50%, it is also recommended to apply slope compensation to improve current loop noise immunity. The minimum and maximum slope compensation values are calculated by the following equation:

$$\frac{V_{OUT}}{L} \times C_{SLOPE} \times \frac{1.6\Omega}{25} \leq SLOPE \leq \frac{V_{IN} \times f_{SW} \times C_{SLOPE}}{V_{OUT}} \left[ 800mV - \left( \frac{I_{OUTMAX}}{N} + \frac{I_{RIPPLE}}{2} \right) \times \frac{1.6\Omega}{25} \right]$$

where

$$C_{SLOPE} = 5pF$$

The slope-compensation options of MAX20808/MAX20808T can be selected by resistor values on the PGM1 and PGM2 pins. A higher slope value is recommended to help reduce the duty cycle jittering and improve stability.

### Typical Reference Designs

Refer to [Typical Application Circuits](#) for examples of reference schematics. Reference design examples for some common output voltages are shown in [Table 6](#).

**Table 6. Reference Design Examples**

V <sub>OUT</sub> (V)	I <sub>OUT</sub> (A) (PER PHASE)	f <sub>SW</sub> (kHz)	R <sub>FB1</sub> (kΩ)	R <sub>FB2</sub> (kΩ)	PGM0 (kΩ)	PGM1 OR PGM2 (kΩ)	L (μH)	C <sub>IN</sub> (PER EACH V <sub>DDH</sub> PIN)	C <sub>OUT</sub>
0.8	4	750	1.82	3.01	2.49	1.05	0.47	10μF +1μF +0.1μF	2 × 47μF
0.9	4	1000	2.40	3.01	8.06	1.05	0.47	10μF +1μF +0.1μF	2 × 47μF
1.0	4	1000	3.01	3.01	8.06	1.05	0.47	10μF +1μF +0.1μF	2 × 47μF
1.2	4	1000	4.22	3.01	8.06	1.05	0.56	10μF +1μF +0.1μF	2 × 47μF
1.8	4	1500	7.87	3.01	21.5	2.49	0.56	10μF +1μF +0.1μF	2 × 47μF
3.3	4	2000	16.9	3.01	30.9	2.15	1.0	10μF +1μF +0.1μF	2 × 47μF
5.0	3	2000	22.6	2.49	30.9	100	2.2	10μF +1μF +0.1μF	1 × 47μF

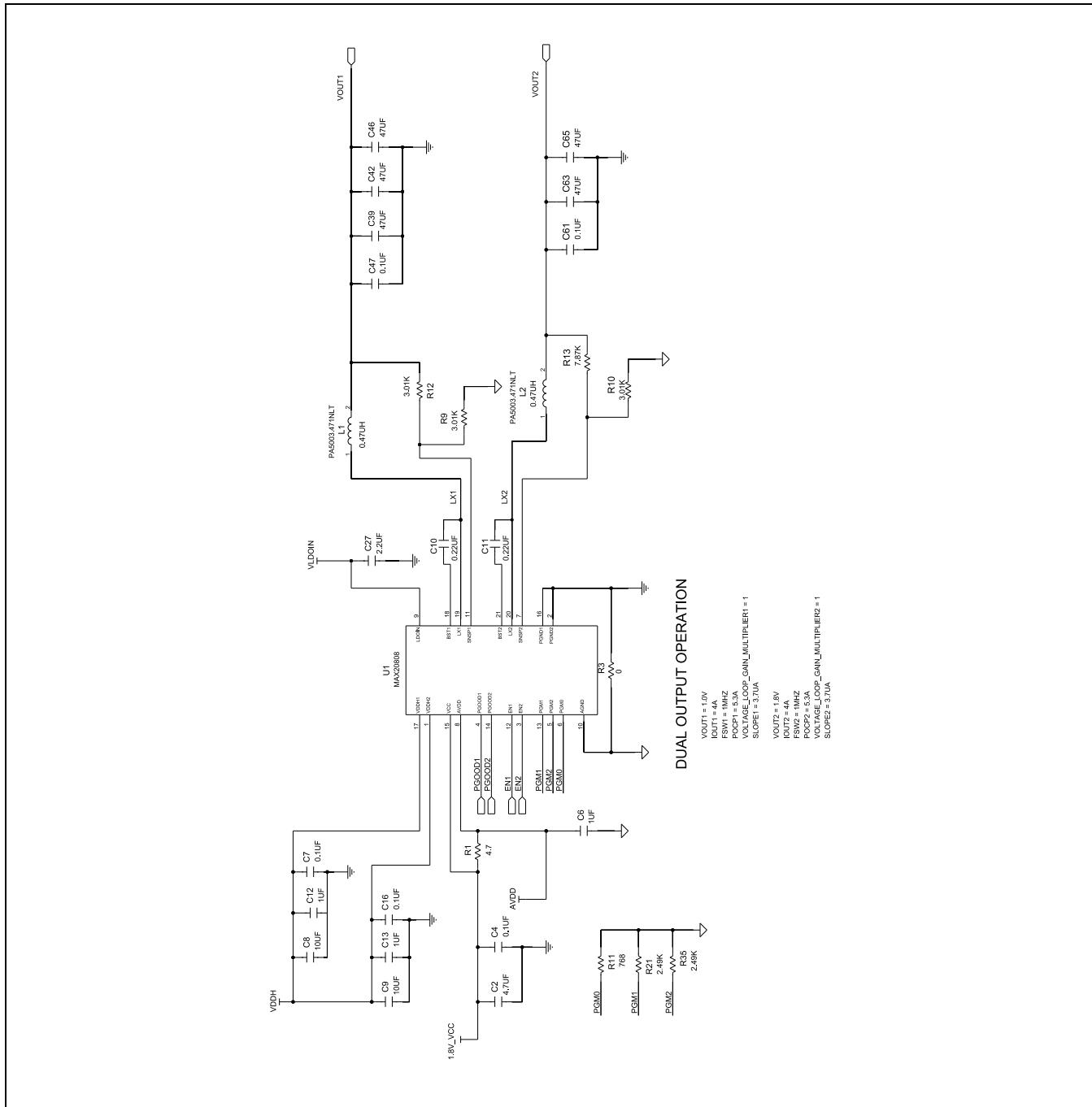
### PCB Layout Guidelines

- For electrical and thermal reasons, the second layer from the top and bottom of the PCB should be reserved for power ground (PGND) planes.

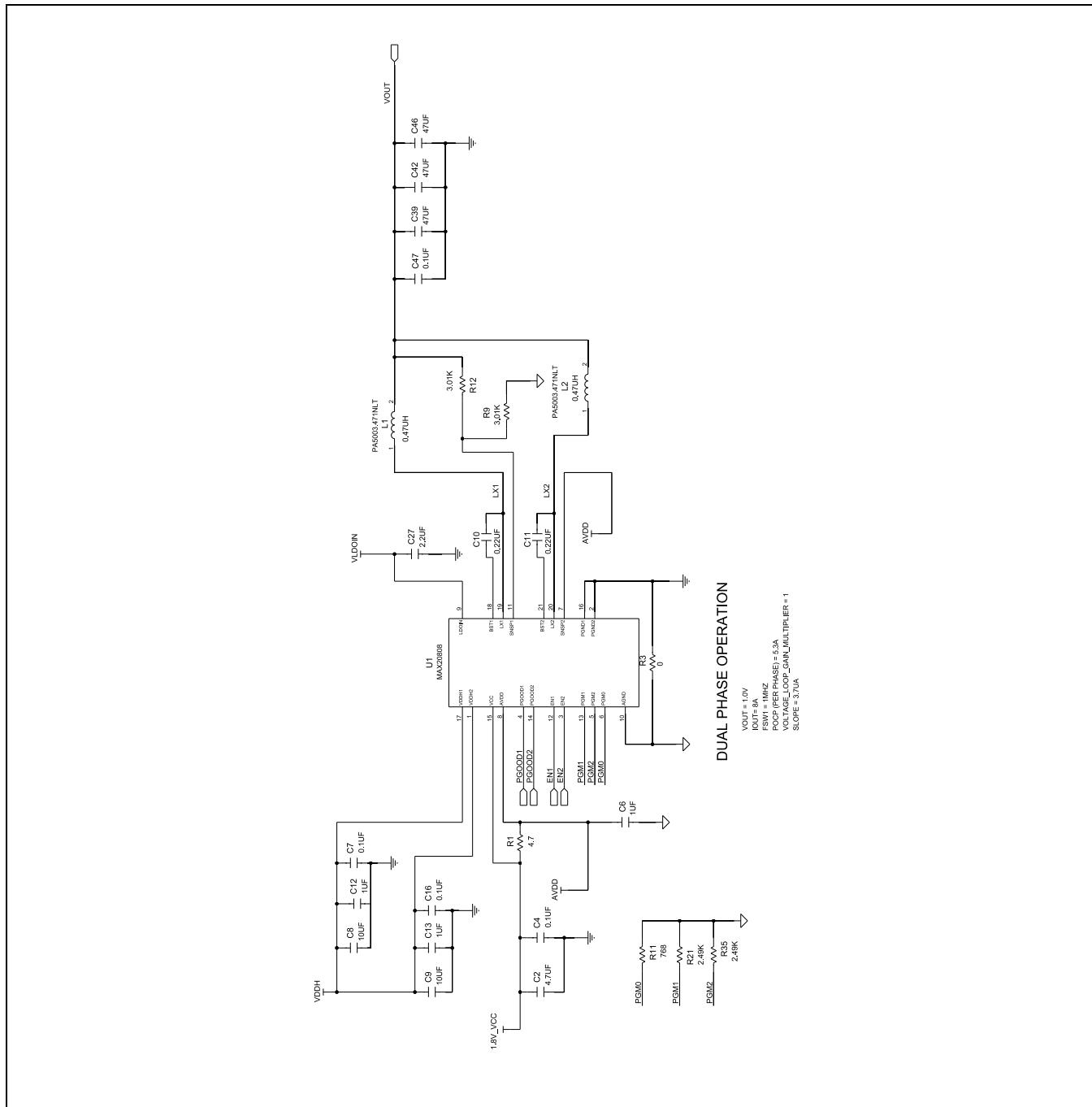
- The input decoupling capacitor should be located the closest to the IC and no more than 40mils from the  $V_{DDH\_}$  pins.
- The  $V_{CC}$  decoupling capacitors should be connected to PGND and placed as close as possible to  $V_{CC}$  pin.
- An analog ground copper polygon or island should be used to connect all analog control-signal grounds. This “quiet” analog ground copper polygon or island should be connected to the PGND through a single connection close to AGND pin. The analog ground can be used as a shield and ground reference for the control signals (PGM\_ and SNSP\_).
- The AVDD decoupling capacitors should be connected to AGND and placed as close as possible to AVDD pin.
- The boost capacitors should be placed as close as possible to LX\_ and BST\_ pins, on the same side of the PCB with the IC.
- The feedback resistor-divider and optional external compensation network should be placed close to the IC to minimize the noise injection.
- Voltage sense line should be shielded by ground plane and be kept away from switching node and the inductor.
- Multiple vias are recommended for all paths that carry high currents and for heat dissipation.
- The input capacitors and output inductors should be placed near the IC and the traces to the components should be kept as short and wide as possible to minimize parasitic inductance and resistance.

## Typical Application Circuits

## Dual-Output Operation



## Dual-Phase Operation



**Ordering Information**

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE	DUAL-PHASE OPERATION	MINIMUM CONTROLLABLE ON-TIME
MAX20808AFH+	-40°C to +125°C	21 FC2QFN (Open Top)	YES	47ns
MAX20808AFH+T	-40°C to +125°C	21 FC2QFN (Open Top)	YES	47ns
MAX20808TAFH+*	-40°C to +125°C	21 FC2QFN (Closed Top)	NO	40ns
MAX20808TAFH+T*	-40°C to +125°C	21 FC2QFN (Closed Top)	NO	40ns

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

\*Future product—contact factory for availability.

**Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	05/21	Initial release	—

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