Click here for production status of specific part numbers.

MAX20075D/MAX20076D/ MAX20076E/MAX25276D

36V, 600mA/1.2A Mini Buck Converter with 3.5µA I_Q

General Description

The MAX20075D/MAX20076D/MAX25276D are small, synchronous buck converters with integrated high-side and low-side switches. The MAX20076D/MAX25276D are designed to deliver up to 1.2A and the MAX20075D up to 0.6A, with 3.5V to 36V input voltages, while using only 3.5µA quiescent current at no load. The devices provide an accurate output voltage of ±2% within the normal operation input range of 6V to 18V. With 20ns minimum on-time capability, the converter is capable of large input-to-output conversion ratios. Voltage quality can be monitored by observing the PGOOD signal. The devices can operate in dropout by running at 99% duty cycle, making them ideal for automotive and industrial applications. The devices offer two fixed output voltages of 5V and 3.3V. In addition, the devices can be configured for 1V to 10V output voltages using an external resistor-divider. Frequency is internally fixed at 2.1MHz, which allows for small external components and reduced output ripple, and guarantees no AM interference. The devices automatically enter skip mode at light loads with ultra-low quiescent current of 3.5µA at no load. The devices offer pin-enabled spread-spectrum-frequency modulation designed to minimize EMI-radiated emissions due to the modulation frequency.

The MAX20075D/MAX20076D/MAX25276D are available in small (3mm x 3mm) 12-pin TDFN and side-wettable TDFN packages with an exposed pad, and use very few external components.

Applications

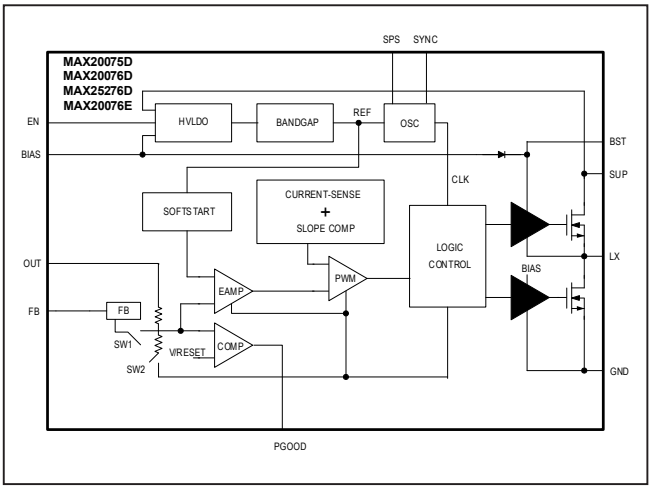
- Automotive
- Industrial
- High-Voltage DC-DC Converters

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Synchronous DC-DC Converter with Integrated FETs
  - MAX20075D = 0.6A I_{OUT}
  - MAX20076D/MAX25276D = 1.2A I_{OUT}
  - 3.5µA Quiescent Current when in Standby Mode
- 20ns Minimum On-Time Small Solution Size Saves Space
  - 2.1MHz Frequency
  - Programmable 1V to 10V Output for the Buck, or Fixed 5V/3.3V Options Available
  - Fixed 2.5ms Internal Soft-Start
  - Fixed Output Voltage with ±2% Output Accuracy (5V/3.3V), or Externally Resistor Adjustable (1V to 10V) with ±1.5% FB Accuracy
  - Innovative Current-Mode-Control Architecture Minimizes Total Board Space and BOM Count
- PGOOD Output and High-Voltage EN Input Simplify Power Sequencing
- Protection Features and Operating Range Ideal for Automotive Applications
  - 3.5V to 36V Operating V_{IN} Range
  - 40V Load-Dump Protection
  - 99% Duty-Cycle Operation with Low Dropout
  - -40°C to +125°C Automotive Temperature Range
  - AEC-Q100 Qualified

Simplified Block Diagram



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Absolute Maximum Ratings

SUP .....-0.3V to +40V
EN..... -0.3V to V_{SUP} + 0.3V
BST to LX (Note 1).....+6V
BST.....-0.3V to +45V
FB .....-0.3V to V_{BIAS} + 0.3V
SYNC.....-0.3V to V_{BIAS} + 0.3V
SPS .....-0.3V to V_{BIAS} + 0.3V
OUT .....-0.3V to +18V
PGOOD .....-0.3V to +6V
PGND to AGND.....-0.3V to +0.3V
BIAS .....-0.3V to +6.0V
OUT Short-Circuit Duration .....Continuous
ESD Protection
Human Body Model .....±2kV
Continuous Power Dissipation (T_A = +70°C)
12-pin TDFN/SW TDFN
(derate 24.4mW/°C above +70°C) 1951mW
Operating Junction Temperature (Note 5)..... -40°C to +150°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (Soldering, 10s).....+300°C
Soldering Temperature (Reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: LX has internal clamp diodes to PGND/AGND and SUP. Applications that forward bias these diodes should take care not to exceed the IC's package power-dissipation limits.

Recommended Operating Conditions

Parameter	Ambient temperature range
Conditions	-40°C to +125°C

Package Information

PACKAGE TYPE: 12 TDFN-CU	
Package Code	TD1233+2C
Outline Number	**21-0664**
Land Pattern Number	**90-0397**
PACKAGE TYPE: 12 SW TDFN	
Package Code	TD1233Y+2C
Outline Number	**21-100176**
Land Pattern Number	**90-100072**
PACKAGE TYPE: 12 SW TDFN	
Package Code	TD1233Y+3C
Outline Number	**21-100284**
Land Pattern Number	**90-100072**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	9°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{SUP} = V_{EN}, V_{SUP} = 14V, V_{SYNC} = 0V, V_{OUT} = 5V, T_J = -40°C to +150°C, unless otherwise noted.) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP}		3.5		36	V
		t < 1s			40	
		MAX25276D, after startup (Note 2)	3		36	
Supply Current	I_{SUP}	V_{EN} = low		1	5	µA
		MAX20075/76DATCB/V+, MAX20076EATCB/VY+, no load, no switching		3.5	8	
		MAX20075/76DATCB/V+, MAX20076EATCB/VY+, no load,switching (Note 3)		4.5		
		MAX20075/76DATCA/V+, no load, no switching		5.6	10	
		MAX20075/76DATCA/V+, no load, switching (Note 3)		6.6		
LX Leakage	$I_{LX,LEAK}$	V_{SUP} = 40V, LX = 0 or 40V, T_A = +25°C	-1		+1	µA
Undervoltage Lockout	UVLO	OUT rising	2.52	2.73	2.93	V
		Hysteresis		0.16		
BIAS Voltage	VBIAS	5.5V ≤ V_{SUP} ≤ 36V, FPWM mode		5		V
BUCK CONVERTER						
Voltage Accuracy, 5V	$V_{OUT,5V}$	MAX20075/76DATCA/V+ skip mode (Note 3)	4.87	5	5.08	V
		MAX20075/76DATCA/V+ fixed-frequency PWM mode	4.93	5	5.07	
Voltage Accuracy, 5.147V	$V_{OUT,5.147V}$ (Note 2)	MAX25276DATCA/VY+ skip mode (Note 3)	5.013	5.147	5.230	V
		MAX25276DATCA/VY+ fixed frequency PWM mode	5.070	5.147	5.224	
Voltage Accuracy, 3.3V	$V_{OUT,3.3V}$	MAX20075/76DATCB/V+, MAX20076DATCC/V+, MAX20076EATCB/VY+ skip mode (Note 3)	3.18	3.3	3.37	V
		MAX20075/76DATCB/V+, MAX20076DATCC/V+, MAX20076EATCB/VY+ fixed-frequency PWM mode	3.25	3.3	3.35	
Voltage Accuracy, 3.6V	$V_{OUT,\ 3.6V}$	MAX20075DATCC/V+, MAX20075DATCC/VY+ skip mode (Note 3)	3.47	3.6	3.68	V
		MAX20075DATCC/V+, MAX20075DATCC/VY+ fixed-frequency PWM mode	3.55	3.6	3.655	
Output Voltage Range	V_{OUT}	MAX20075/76DATCC/V+ and MAX20075DATCC/VY+ only	1		3.6	V
		MAX20075/76DATCA/V+, MAX20075/76DATCB/V+, and MAX20076EATCB/VY+ only	3		10	
FB Voltage Accuracy	V_{FB}		0.985	1	1.015	V

Electrical Characteristics (continued)

(V_{SUP} = V_{EN}, V_{SUP} = 14V, V_{SYNC} = 0V, V_{OUT} = 5V, T_J = -40°C to +150°C, unless otherwise noted.) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FB Current	I_{FB}	V_{FB} = 1V, T_A = +25°C			0.02		µA
FB Line Regulation		V_{SUP} = 6V to 36V			0.02		%/V
High-Side Switch On-Resistance	$R_{ON,HS}$	V_{BIAS} = 5V, I_{LX} = 1.2A			300	550	mΩ
Low-Side Switch On-Resistance	$R_{ON,LS}$	V_{BIAS} = 5V, I_{LX} = 1.2A			200	350	mΩ
High-Side Current-Limit Threshold		MAX20076D/MAX25276D		1.67	1.9	2.13	A
		MAX20075D		1.05	1.2	1.35	
Low-Side Negative Current-Limit Threshold	I_{NEG}				-0.6		A
Soft-Start Ramp Time	I_{SS}				2.5	5	ms
Minimum On-Time	t_{ON_V}	MAX20075/76DATCC/V+ and MAX20075DATCC/VY+				20	ns
Minimum On-Time	t_{ON}	MAX20075/76DATCA/V+, MAX20075/76DATCB/V+, and MAX20076EATCB/VY+			66	85	ns
Maximum Duty Cycle				98	99		%
PWM Switching Frequency	f_{SW}	Fixed		1.925	2.1	2.275	MHz
Spread-Spectrum Range	SS	V_{SPS} = 5V			±6		%
PGOOD							
PGOOD Threshold, Rising	$V_{THR,PGD}$	V_{OUT} rising	MAX20075/76DATCA/V+, MAX20075/76DATCC/V+, and 20075DATCC/VY+	90	93.5	97	%
PGOOD Threshold, Falling	$V_{THF,PGD}$	V_{OUT} falling		89.5	93	96.5	%
PGOOD Debounce Time	t_{DEB}	PWM mode, V_{OUT} falling			65		µs
		Skip mode, V_{OUT} rising			100		
		MAX20076EATCB/VY+, V_{OUT} rising		6			ms
PGOOD High-Leakage Current	$I_{LEAK,PGD}$	T_A = +25°C				1	µA
PGOOD Low Level	$V_{OUT,PGD}$	Sinking 1mA				0.4	V
LOGIC LEVELS							
EN Level, High	$V_{IH,EN}$			2.4			V
EN Level, Low	$V_{IL,EN}$					0.6	V
EN Input Current	$I_{IN,EN}$	V_{EN} = V_{SUP} = 14V, T_A = +25°C				1	µA
External Input Clock Frequency				1.7		2.6	MHz
SYNC Threshold, High	$V_{IH,SYNC}$			1.4			V

Electrical Characteristics (continued)

(V_{SUP} = V_{EN}, V_{SUP} = 14V, V_{SYNC} = 0V, V_{OUT} = 5V, T_J = -40°C to +150°C, unless otherwise noted.) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC Threshold, Low	$V_{IL,SYNC}$				0.4	V
SYNC Internal Pulldown	$R_{PD,MODE}$			1000		kΩ
SPS Threshold, High	$V_{IH,SPS}$		1.4			V
SPS Threshold, Low	$V_{IL,SPS}$				0.4	V
SPS Internal Pulldown				1000		kΩ
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}	(Note 3)		175		°C
Thermal-Shutdown Hysteresis	$T_{SHDN.HYS}$	(Note 3)		15		°C

Note 2: V_{OUT} and V_{SUP} are the only electrical characteristics that differentiate the MAX25276D from the MAX20076D (with matching subscript).

Note 3: Guaranteed by design; not production tested.

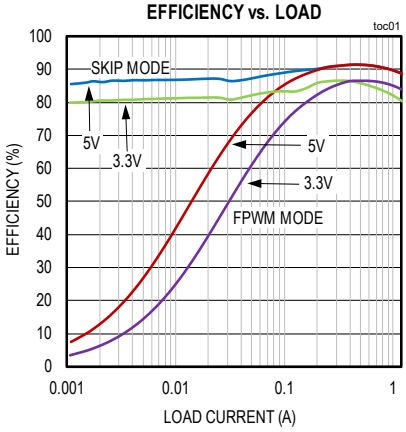
Note 4: Limits are 100% tested at T_A + +25°C. Limits over the operating range and relevant supply voltage are guaranteed by design and characterization. Typical values are at T_A = +25°C.

Note 5: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

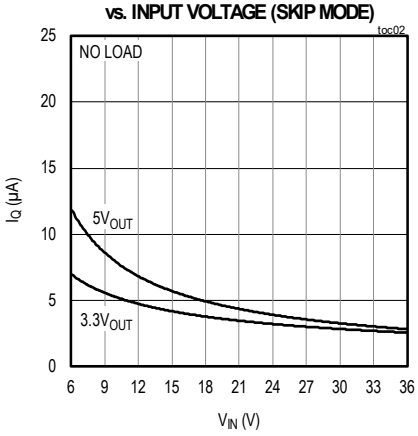
Typical Operating Characteristics

V_{SUP} = V_{EN} = +14V, (T_A = +25°C, unless otherwise noted.)

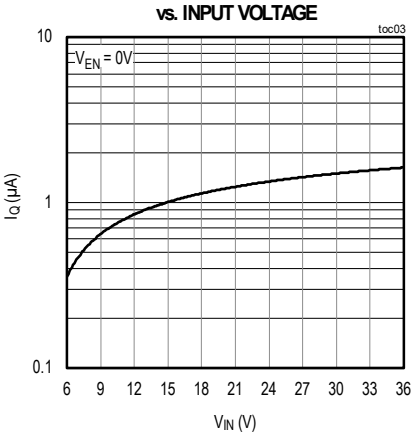
EFFICIENCY vs. LOAD



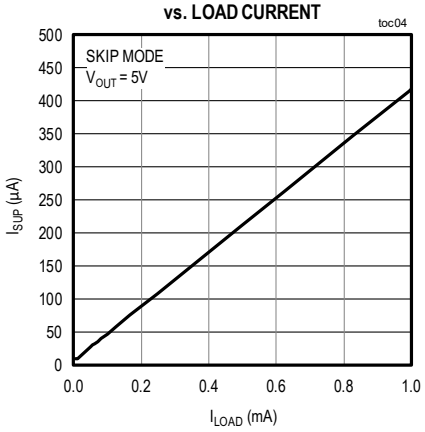
QUIESCENT SUPPLY CURRENT vs. INPUT VOLTAGE (SKIP MODE)



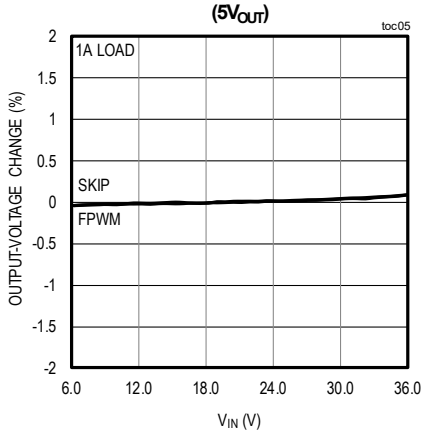
SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE



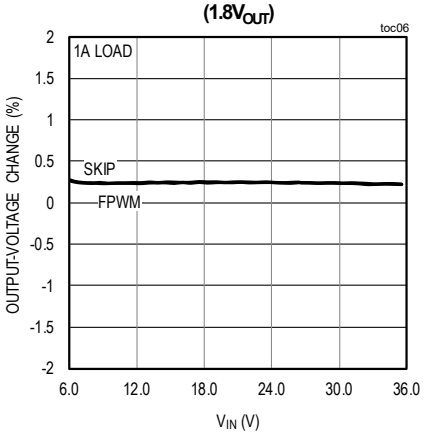
STANDBY CURRENT vs. LOAD CURRENT



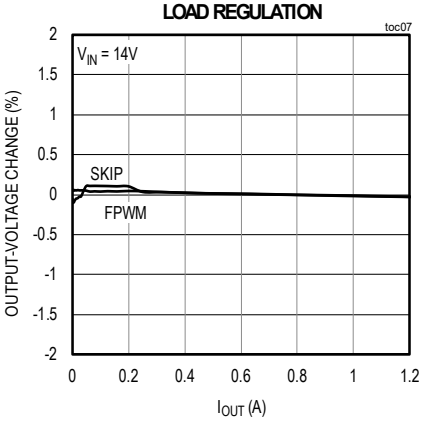
LINE REGULATION (5V_{OUT})



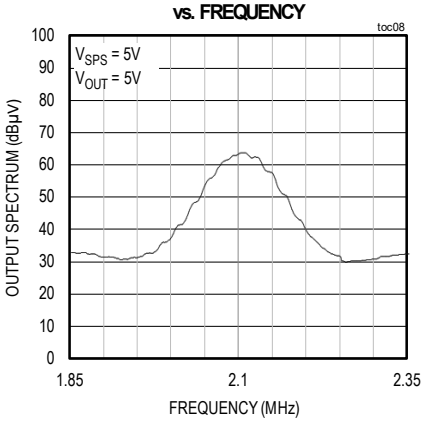
LINE REGULATION (1.8V_{OUT})



LOAD REGULATION



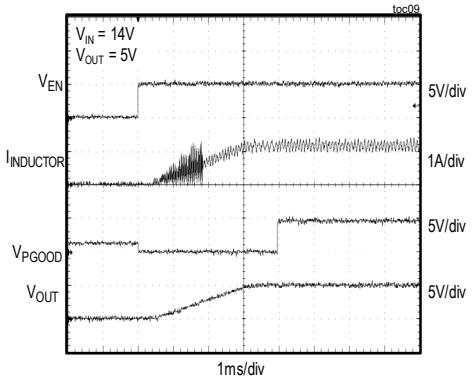
SPECTRAL ENERGY DENSITY vs. FREQUENCY



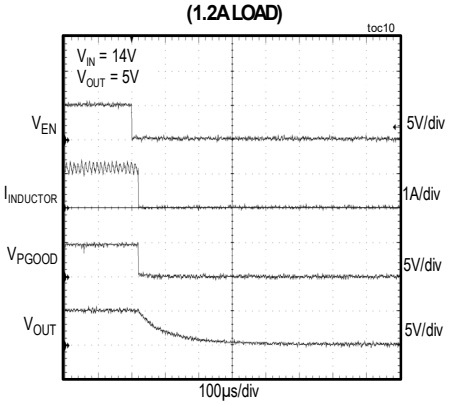
Typical Operating Characteristics (continued)

V_{SUP} = V_{EN} = +14V, (T_A = +25°C, unless otherwise noted.)

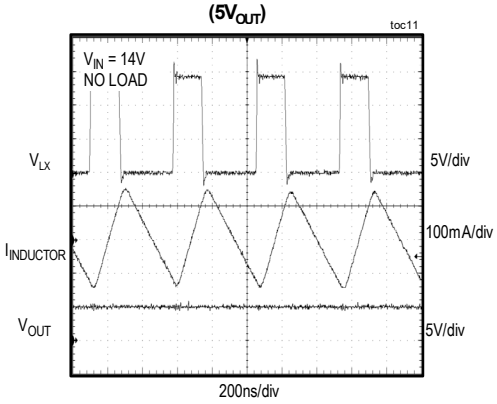
STARTUP WAVEFORM (1.2A LOAD)



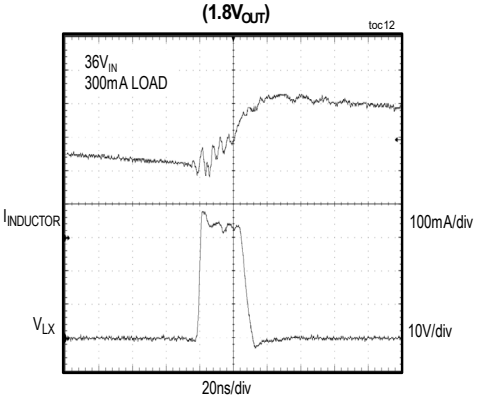
SHUTDOWN WAVEFORM (1.2A LOAD)



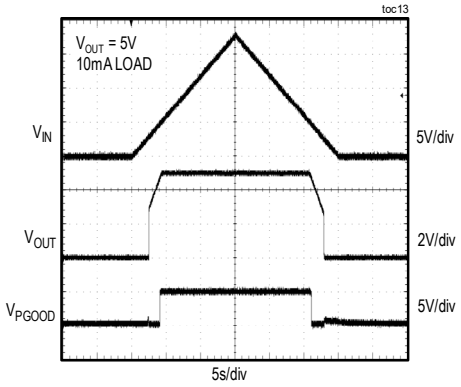
STEADY-STATE SWITCHING WAVEFORMS ($5V_{OUT}$)



MINIMUM ON-TIME ($1.8V_{OUT}$)



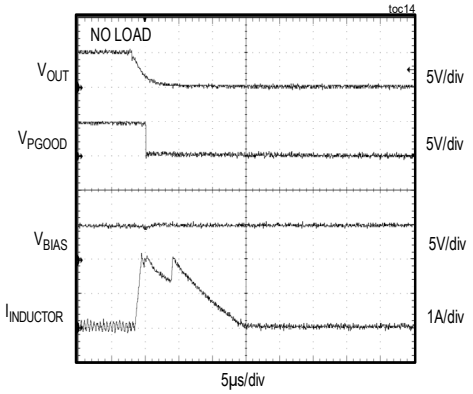
SLOW V_{IN} RAMP



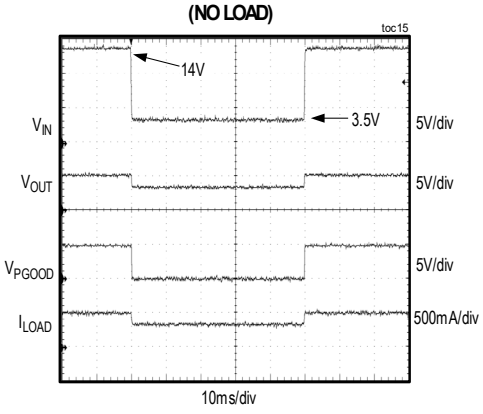
Typical Operating Characteristics (continued)

V_{SUP} = V_{EN} = +14V, (T_A = +25°C, unless otherwise noted.)

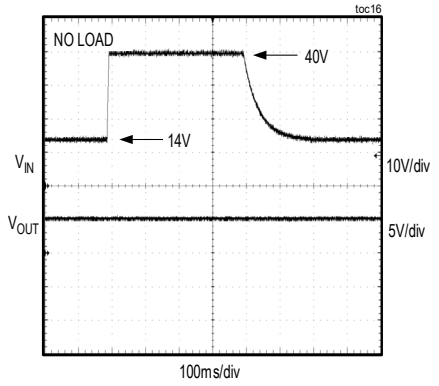
SHORT-CIRCUIT RESPONSE



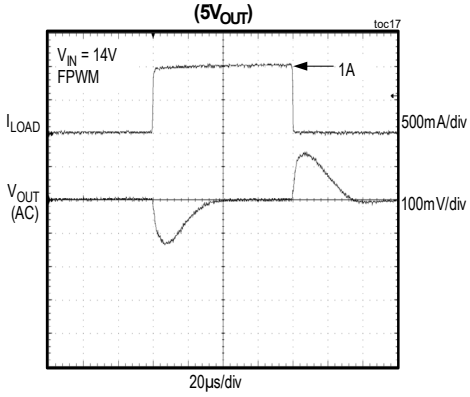
UNDERVOLTAGE PULSE (NO LOAD)



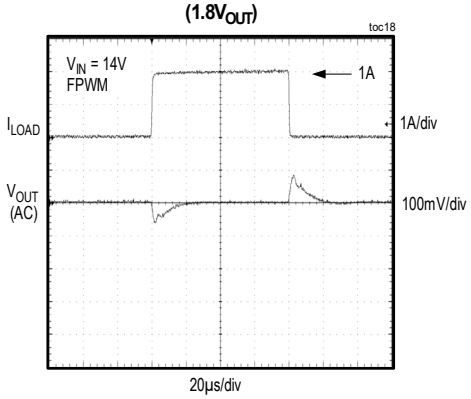
LOAD-DUMP TEST



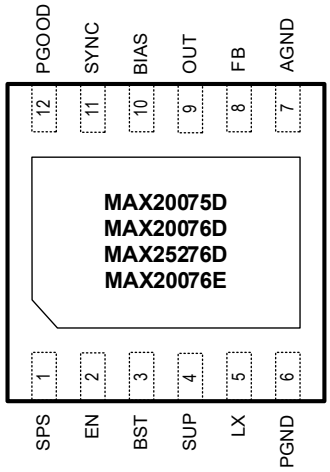
LOAD-TRANSIENT RESPONSE ($5V_{OUT}$)



LOAD-TRANSIENT RESPONSE ($1.8V_{OUT}$)



Pin Configurations



TDFN-EP
(3mm x 3mm)

Pin Description

PIN	NAME	FUNCTION
1	SPS	Spread-Spectrum Enable. Connect logic-high to enable spread spectrum of internal oscillator or logic-low to disable spread spectrum. This pin has a 1MΩ internal pulldown.
2	EN	High-Voltage-Compatible Enable Input. If this pin is low, the part is off.
3	BST	Bootstrap Pin for HS Driver. It is recommended to use 0.1µF from BST to LX.
4	SUP	Supply Input. Connect a 4.7µF ceramic capacitor from SUP to PGND.
5	LX	Buck Switching Node. High impedance when part is off. Connect a 4.7µH inductor between LX and OUT.
6	PGND	Power Ground. Ground return path for all high-current/high-frequency noisy signals.
7	AGND	Analog Ground. Ground return path for all ‘quiet’ signals.
8	FB	Feedback Pin. Connect a resistor-divider from OUT to FB to ground for external adjustment of the output voltage. Connect FB to BIAS for internal fixed voltages.
9	OUT	Buck Regulator Output-Voltage-Sense Input. Bypass OUT to PGND with 22µF ceramic capacitor.
10	BIAS	5V Internal BIAS Supply. Connect a 1µF (min) ceramic capacitor to AGND.
11	SYNC	Sync Input. If connected to ground or open, skip-mode operation is enabled under light loads; if connected to BIAS, forced-PWM mode is enabled. This pin has a 1MΩ internal pulldown.
12	PGOOD	Open-Drain Reset Output. External pullup required.
—	EP	Exposed Pad. EP **must** be connected to ground plane on PCB, but is not a current-carrying path and is only needed for thermal transfer.

Detailed Description

The MAX20075D/MAX20076D/MAX25276D family of small, current-mode-controlled buck converters features synchronous rectification and requires no external compensation network. The devices are designed for 1.2A and 0.6A output current (MAX20076D/MAX25276D and MAX20075D, respectively), and can stay in dropout by running at 99% duty cycle. They provide an accurate output voltage within the 5.5V to 18V input range. With 20ns minimum on-time the devices can regulate output voltages of < 3V directly off the car battery. This eliminates the need for traditional two-stage designs for voltage rails < 3V. Voltage quality can be monitored by observing the PGOOD signal. The devices operate at 2.1MHz (typ) frequency, which allows for small external components, reduced output ripple, and guarantees no AM band interference.

The devices feature an ultra-low 3.5µA (typ) quiescent supply current in standby mode. The devices center standby mode automatically at light loads if HSFET does not turn on for eight consecutive clock cycles. The devices operate from a 3.5V to 36V supply voltage and can tolerate transients up to 40V, making them ideal for automotive applications. The devices are available in factory-trimmed output voltages (5V, 3.3V) and are programmable with an external resistor-divider. For fixed output voltages outside of 3.3V and 5V, contact factory for availability.

Enable Input (EN)

The devices are activated by driving EN high. EN is compatible from a 3.3V logic level to automotive battery levels. EN can be controlled by microcontrollers and automotive KEY or CAN inhibit signals. The EN input has no internal pullup/pulldown current to minimize the overall quiescent supply current. To realize a programmable undervoltage-lockout level, use a resistor-divider from SUP to EN to AGND.

BIAS/UVLO

The devices feature undervoltage lockout. When the device is enabled, an internal bias generator turns on. LX begins switching after V_{BIAS} has exceeded the internal undervoltage-lockout level, V_{UVLO} = 2.73V (typ).

Soft-Start

The devices feature an internal soft-start timer. The output voltage soft-start ramp time is 2.5ms (typ). If a short circuit or undervoltage is encountered after the soft-start timer has expired, the device is disabled for 6ms (typ) and then reattempts soft-start again. This pattern repeats until the short circuit has been removed.

Oscillator/Synchronization and Efficiency (SYNC)

The devices have an on-chip oscillator that provides a 2.1MHz (typ) switching frequency. Depending on the condition of SYNC, two operation modes exist. If SYNC is unconnected or at AGND, the device operates in highly efficient pulse-skipping mode. If SYNC is at BIAS or has a clock applied to it, the device is in forced PWM mode (FPWM). The devices offer the best of both worlds. The devices can be switched during operation between FPWM mode and skip mode by switching SYNC.

Skip-Mode Operation

Skip mode is entered when the SYNC pin is connected to ground or is unconnected and the peak load current is < 150mA (typ). In this mode, the high-side FET is turned on until the current in the inductor is ramped up to 150mA (typ) peak value and the internal feedback voltage is above the regulation voltage (1.0V, typ). At this point, both the high-side and low-side FETs are turned off. Depending on the choice of the output capacitor and the load current, the high-side FET turns on when OUT (valley) drops below the 1.0V (typ) feedback voltage.

When the device is in skip mode, the internal high-voltage LDO is turned off after the startup is complete to reduce the input current. V_{BIAS} is supplied by the output in this condition.

Achieving High Efficiency at Light Loads

The devices operate with very low-quiescent current at light loads to enhance efficiency and conserve battery life. When the devices enter skip mode, the output current is monitored to adjust the quiescent current. The lowest quiescent current standby mode is only available for factory-trimmed devices between output voltages of 3.0V to 5.5V.

When the output current is < ~5mA, the devices operate in the lowest quiescent-current mode, also called the standby mode. In this mode, the majority of the internal circuitry (excluding that necessary to maintain regulation) in the devices, including the internal high-voltage LDO, is turned off to save current. Under no load and with skip mode enabled, the IC typically draws 4.5µA for the 3.3V parts, and 6.6µA for the 5.0V parts. For load currents > 5mA, the devices enter normal skip mode, still maintaining very high efficiency.

Controlled EMI with Forced-Fixed Frequency

In FPWM mode, the devices attempt to operate at a constant switching frequency for all load currents. For tightest frequency control, apply the operating frequency to SYNC. The advantage of this mode is a constant

switching frequency, which improves EMI performance; the disadvantage is that considerable current can be thrown away. If the load current during a switching cycle is less than the current flowing through the inductor, the excess current is diverted to AGND.

Extended Input Voltage Range

In some cases, the devices are forced to deviate from its operating frequency, independent of the state of SYNC. For input voltages above 18V, the required duty cycle to regulate its output may be smaller than the minimum on-time (66ns, typ). In this event, the devices are forced to lower their switching frequency by skipping pulses. If the output voltage being regulated is < 3V, then the MAX20075DATCC/VY+ and MAX20076DATCC/V+ can enable this at 2.1MHz without skipping pulses.

If the input voltage is reduced and the devices approach dropout, the devices try to turn on the high-side FET continuously. To maintain gate charge on the high-side FET, the BST capacitor must be periodically recharged. To ensure proper charge on the BST capacitor when in dropout, the high-side FET is turned off every 20µs and the low-side FET is turned on for about 200ns. This gives an effective duty cycle of > 99% and a switching frequency of 50kHz when in dropout. Since the MAX20075DATCC/VY+ and MAX20076DATCC/V+ support voltages of < 3V it does not support operation with SUP ≤ OUT.

Spread-Spectrum Option

The devices have an optional spread spectrum enabled by the SPS pin. If SPS is pulled high, then the internal operating frequency varies by ±6% relative to the internally generated operating frequency of 2.1MHz (typ). Spread spectrum is offered to improve EMI performance of the devices.

The internal spread spectrum does not interfere with the external clock applied on the SYNC pin. It is active only when the devices are running with an internally generated switching frequency.

Power-Good (PGOOD)

The devices feature an open-drain power-good output. PGOOD is an active-high output that pulls low when the output voltage is below 93% of its nominal value. PGOOD is high impedance when the output voltage is above 93.5% of its nominal value. Connect a 20kΩ (typ) pullup resistor to an external supply or the on-chip BIAS output.

Overcurrent Protection

The devices limit the peak output current to 1.9A (typ). The accuracy of the current limit is ±12%, which makes selection of external components very easy. To protect against short-circuit events, the devices shut off when OUT is below 50% of OUT voltage (25% of OUT voltage for the MAX20075DATCC/VY+ and MAX20076DATCC/V+) and an overcurrent event is detected. The devices attempt a soft-start restart every 7ms and stay off if the short circuit has not been removed. When the current limit is no longer present, it reaches the output voltage by following the normal soft-start sequence. If the devices' die reaches the thermal limit of 175°C (typ) during the current-limit event, it immediately shuts off.

Thermal-Overload Protection

The devices feature thermal-overload protection. The device turns off when the junction temperature exceeds +175°C (typ). Once the device cools by 15°C (typ), it turns back on with a soft-start sequence.

Applications Information

Setting the Output Voltage

Connect FB to BIAS for a fixed output voltage as per the setting. To set the output to other voltages between 1V and 10V, connect a resistive divider from output (OUT) to FB to AGND (Figure 1). Select R_{FB2} (FB to AGND resistor) less than or equal to 500kΩ. Calculate R_{FB1} (OUT to FB resistor) with the following equation:

$$R_{FB1} = R_{FB2} [(V_{OUT}/V_{FB})-1)]$$

where V_{FB} = 1V (see the *Electrical Characteristics* table).

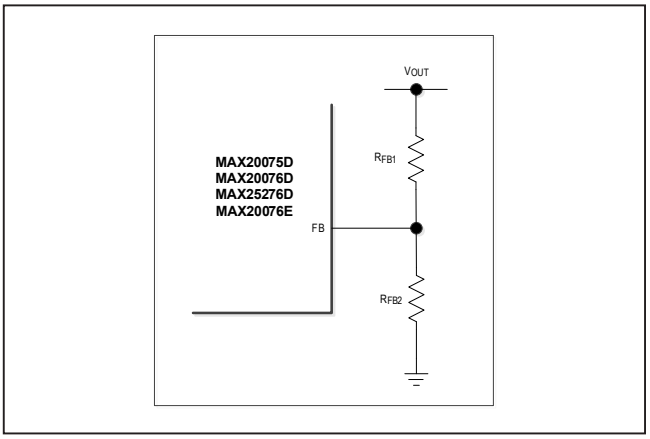


Figure 1. Connecting a Resistive Divider from Output to FB to AGND

Inductor Selection

The design is optimized with 4.7µH inductor for all input and output voltage conditions. The nominal standard value selected should be within ±50% of 4.7µH.

Input Capacitor

A low-ESR ceramic input capacitor of 4.7µF is recommended for proper device operation. This value can be adjusted based on application input-voltage ripple requirements.

The discontinuous input current of the buck converter causes large input ripple current. The switching frequency, peak inductor current, and the allowable peak-to-peak input-voltage ripple dictate the input-capacitance requirement. Increasing the switching frequency or the inductor value lowers the peak-to-average current ratio, yielding a lower input-capacitance requirement.

The input ripple comprises mainly of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the input capacitor). The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR}. Assume that input-voltage ripple from the ESR and the capacitor discharge is equal to 50% each. The following equations show the ESR and capacitor requirement for a target voltage ripple at the input:

Equation 1:

$$ESR = \frac{\Delta V_{ESR}}{I_{OUT} + (\Delta I_{P-P} / 2)}$$

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

and:

$$D = \frac{V_{OUT}}{V_{IN}}$$

where I_{OUT} is the output current, D is the duty cycle, and f_{SW} is the switching frequency. Use additional input capacitance at lower input voltages to avoid possible undershoot below the UVLO threshold during transient loading.

Output Capacitor

For optimal phase margin (> 70°, typ) with internal fixed-voltage options, a 22µF output capacitor is recommended. A lower output capacitor can be used at the expense of lower phase margin. For all other designs a minimum of 10µF output capacitor is required. Additional output capacitance may be needed based on application-specific output-voltage ripple requirements. If the total output capacitance required is > 70µF, contact the factory for an optimized solution.

The allowable output-voltage ripple and the maximum deviation of the output voltage during step-load currents determine the output capacitance and its ESR. The output ripple comprises ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the output capacitor). Use low-ESR ceramic or aluminum electrolytic capacitors at the output. For aluminum electrolytic capacitors, the entire output ripple is contributed by ΔV_{ESR}. Use the ESR_{OUT} equation to calculate the ESR requirement and choose the capacitor accordingly. If using ceramic capacitors, assume the contribution to the output ripple voltage from the ESR and the capacitor discharge to be equal. The following equations show the output capacitance and ESR requirement for a specified output-voltage ripple.

Equation 2:

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_{P-P}}$$

$$C_{OUT} = \frac{\Delta I_{P-P}}{8 \times \Delta V_Q \times f_{SW}}$$

where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

and:

$$V_{OUT\_RIPPLE} = \Delta V_{ESR} + \Delta V_Q$$

ΔI_{P-P} is the peak-to-peak inductor current as calculated above, and f_{SW} is the converter's switching frequency. The allowable deviation of the output voltage during fast transient loads also determines the output capacitance and its ESR. The output capacitor supplies the step-load current until the converter responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the converter. The high switching frequency of the devices allows for a higher closed-loop bandwidth, thus reducing $t_{RESPONSE}$ and the output-capacitance requirement. The resistive drop across the output capacitor's ESR and the capacitor discharge causes a voltage droop during a step load. Use a combination of low-ESR tantalum and ceramic capacitors for better transient load and ripple/noise performance. Keep the maximum output-voltage deviations below the tolerable limits of the electronics being powered. When

using a ceramic capacitor, assume an 80% and 20% contribution from the output-capacitance discharge and the ESR drop, respectively. Use the following equations to calculate the required ESR and capacitance value:

Equation 3:

$$ESR_{OUT} = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_Q}$$

where ISTEP is the load step and $t_{RESPONSE}$ is the response time of the converter. The converter response time depends on the control-loop bandwidth.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching power losses and clean, stable operation. Use a multi-layer board wherever possible for better noise immunity. Follow the guidelines below for a good PCB layout:

1) The input capacitor (4.7µF, see Figure 2, Figure 3, and Figure 4) should be placed right next to the SUP pin. Since the MAX20075D/MAX20076D/MAX25276D operate at 2.1MHz switching frequency, this placement is critical for effective decoupling of high-frequency noise from the SUP pins.
2) Solder the exposed pad to a large copper-plane area under the device. To effectively use this copper area as heat exchanger between the PCB and ambient, expose the copper area on the top and bottom side. Add a few small vias or one large via on the copper pad for efficient heat transfer. Connect the exposed pad to PGND, ideally at the return terminal of the output capacitor.
3) Isolate the power components and high-current paths from sensitive analog circuitry.
4) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
5) Connect PGND and AGND together, preferably at the return terminal of the output capacitor. Do not connect them anywhere else.
6) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCB to enhance full-load efficiency and power-dissipation capability.
7) Route high-speed switching nodes away from sensitive analog areas. Use internal PCB layers as PGND to act as EMI shields to keep radiated noise away from the device and analog bypass capacitor.

Typical Application Circuits

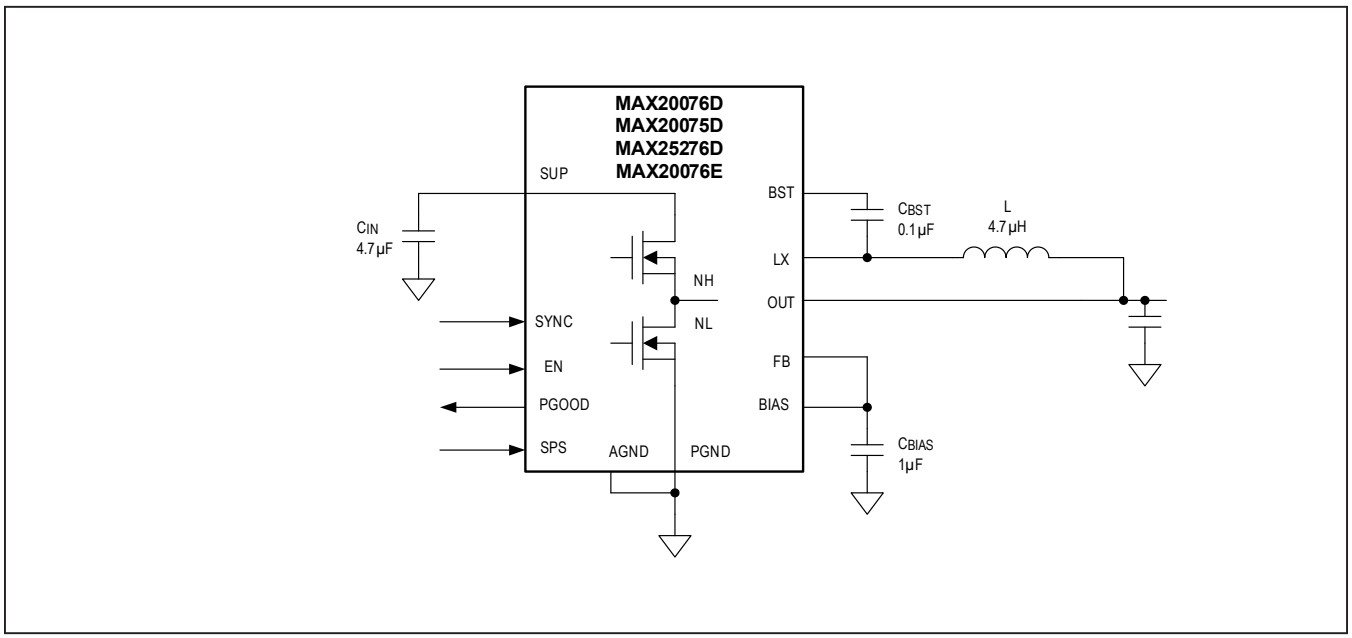


Figure 2. MAX20075D/MAX20076D/MAX20076E/MAX25276D Application Circuit with Fixed Output Voltage

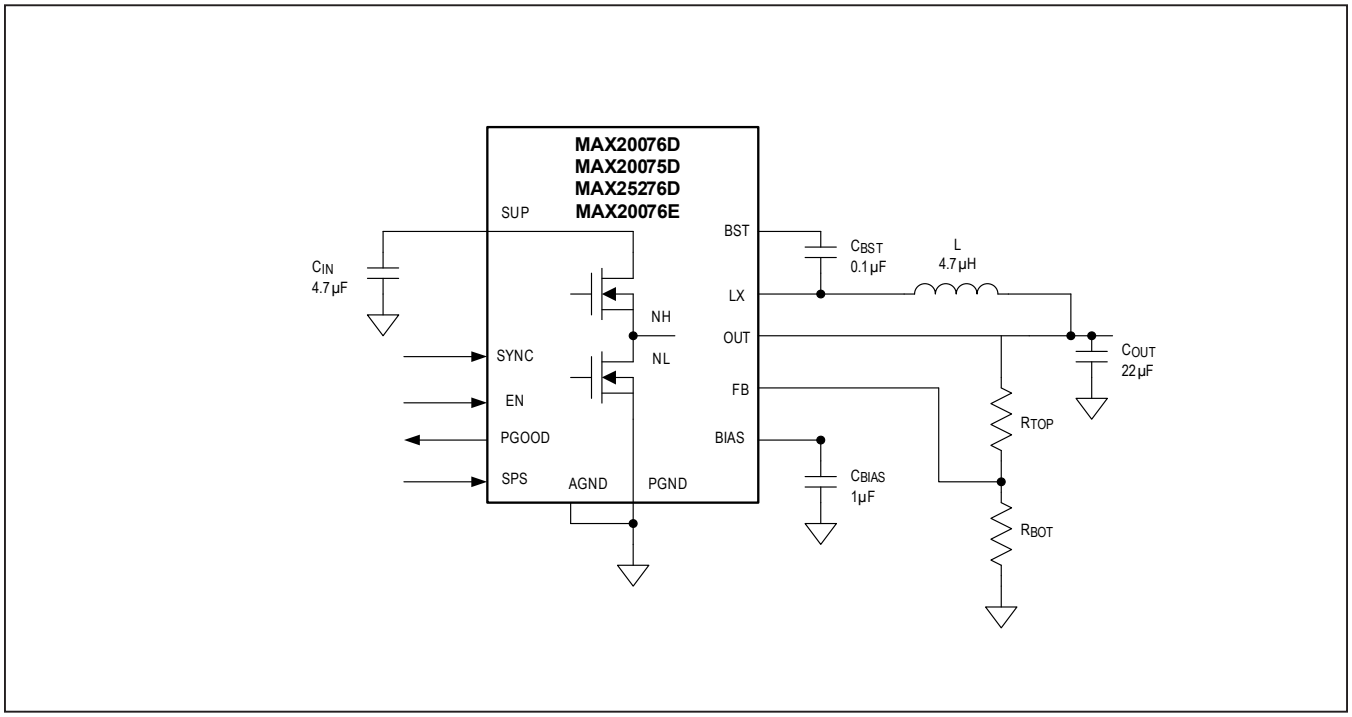


Figure 3. MAX20075D/MAX20076D/MAX20076E/MAX25276D Application Circuit with External Resistor-Divider to Set Output Voltage

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	DESCRIPTION	I_{OUT}
MAX20075DATCA/V+	-40°C to +125°C	TD1233+2C	Fixed 5V output or 3V to 10V external resistor-divider	0.6A
MAX20075DATCB/V+	-40°C to +125°C	TD1233+2C	Fixed 3.3V output or 3V to 10V external resistor-divider	0.6A
MAX20075DATCC/V+	-40°C to +125°C	TD1233+2C	Fixed 3.6V or 1V to 3.6V with external resistor-divider	0.6A
MAX20075DATCC/VY+	-40°C to +125°C	TD1233Y+2C	Fixed 3.6V or 1V to 3.6V with external resistor-divider	0.6A
MAX20076DATCA/V+	-40°C to +125°C	TD1233+2C	Fixed 5V output or 3V to 10V external resistor-divider	1.2A
MAX20076DATCA/VY+	-40°C to +125°C	TD1233Y+3C	Fixed 5V output or 3V to 10V external resistor-divider	1.2A
MAX20076DATCB/V+	-40°C to +125°C	TD1233+2C	Fixed 3.3V output or 3V to 10V external resistor-divider	1.2A
MAX20076DATCC/V+	-40°C to +125°C	TD1233+2C	Fixed 3.3V or 1V to 3.6V with external resistor-divider	1.2A
MAX20076DATCC/VY+*	-40°C to +125°C	TD1233Y+3C	Fixed 3.3V or 1V to 3.6V with external resistor-divider	1.2A
MAX20076EATCB/VY+	-40°C to +125°C	TD1233Y+2C	Fixed 3.3V output or 3V to 10V external resistor-divider with 6ms delay in PGOOD	1.2A
MAX25276DATCA/VY+	-40°C to +125°C	TD1233Y+3C	2.1MHz, fixed 5.147V output or 3V to 10V external resistor-divider	1.2A

Note: *All parts are OTP versions, no metal mask differences.*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
Y = Side-wettable package.
** Future product—contact factory for vailability*

Chip Information

PROCESS: CMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/19	Initial release	—
1	7/19	Updated *Ordering Information* to add future-product status	15
2	8/19	Added MAX20076E to title and all figures; replaced all instances of MAX20076DATCD/VY+ with MAX20076EATCB/VY+	1-15
3	8/19	Updated *Ordering Information* to remove future-product status from MAX20075DATCB/V+ and MAX25276DATCA/VY+	15
4	10/19	Updated *Ordering Information* to remove all remaining future-product notation	15
5	11/19	Updated *Ordering Information* to add MAX20076DATCA/VY+ and add future-product notation to MAX20076DATCA/V+	15
6	12/19	Updated *Ordering Information* to correct package code for MAX20076DATCA/VY+	15
7	2/20	Updated *Ordering Information* to add MAX20076DATCC/VY+* and remove future-product notation from MAX20076DATCA/V+	15

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