Click here to ask about the production status of specific part numbers.

MAX17852

14-Channel High-Voltage, ASIL D, Data-Acquisition System with Integrated Current-Sense Amplifier

General Description

The MAX17852 is a flexible data-acquisition system for the management of high-voltage and low-voltage battery modules. The system can measure 14 cell voltages, one current measurement, and a combination of four temperatures or system voltages with fully redundant measurement engines in 263µs, or perform all inputs solely with the ADC measurement engine in 156µs. There are 14 internal switches rated for > 300mA for cell-balancing, each supporting extensive built-in diagnostics. Up to 32 devices can be daisy-chained to manage 448 cells and monitor 128 temperatures.

Cell and bus-bar voltages ranging from -2.5V to +5V are measured differentially over a 65V common-mode range, with a typical accuracy of 1mV (3.6V cell, 25°C). If oversampling is enabled, up to 128 measurements per channel can be averaged internally with 14-bit resolution and combined with digital post-processing IIR filtering for increased noise immunity. The system can shut itself down in the event of a thermal overload by measuring its own die temperature.

For robust communications, the system uses Maxim's battery-management UART or SPI protocol for robust communications and supports an I^2C master interface for external device control, and is optimized to support a reduced feature set of internal diagnostics and rapid-alert communication through both embedded communication and hardware-alert interfaces to support ASIL-D and FMEA requirements.

Applications

- High-Voltage Battery Stacks
- Electric Vehicles (EVs)
- Hybrid Electric Vehicles (HEVs)
- Electric Bikes
- Battery-Backup Systems (UPS or ESS)
- Super-Cap Systems
- Battery-Powered Tools

Benefits and Features

- AECQ-100 Grade 1 Temp. Range -40°C to 125°C
- 65V Operating Voltage
- Ultra-Low-Power Operation
  - Standby Mode: 2mA
  - Shutdown Mode: 2µA
- Redundant ADC and Comparator Acquisitions
- Simultaneous Cell and Bus-Bar Voltage Acquisitions
- 14 Cell-Voltage Measurement Channels
  - 1mV Accuracy (3.6V, 25°C)
  - 2mV Accuracy (5°C to 40°C)
  - 4.5mV Accuracy (-40°C to 125°C)
- 14 Cell-Balancing Switches
  - > 300mA Software-Programmable Balancing Current
  - Optimized Driving (AUTOBALSWDIS) and Parking Balancing Modes
  - Automated Balancing with Individual Cell Timers
  - Automated Balancing by Cell Voltage
  - Emergency Discharge Mode
- Low-Noise Current-Sense Amplifier
  - 5mA resolution (Gain = 256)
- Four Configurable Auxiliary Inputs for Temperature, Voltage, or GPIO
- Integrated Die Temperature Measurement
- Automatic Thermal Protection
- Individually Configurable Safety Alert
  - Overvoltage, Undertemperature and Undervoltage, Overtemperature Faults
  - One Cell-Mismatch Alert
- Support ASIL-D Requirements for Cell Voltage, Temperature, Current, Communication
- Selectable UART, Dual UART, or SPI Interface
- Battery-Management UART Protocol
  - Daisy-Chain Up to 32 Devices
  - Capacitive Communication-Port Isolation
  - Up to 2 Mbps Baud Rate (auto-detect)
  - 1.5µs Propagation Delay (per device)
  - Packet-Error Checking (PEC)
- I^2C Master
- Configurable Hardware-Alert Interfaces
- Factory-Trimmed Oscillator (No External Crystals Required)
- 32-Bit Unique Device ID
- 64-Pin (10mm x 10mm) LQFP Package

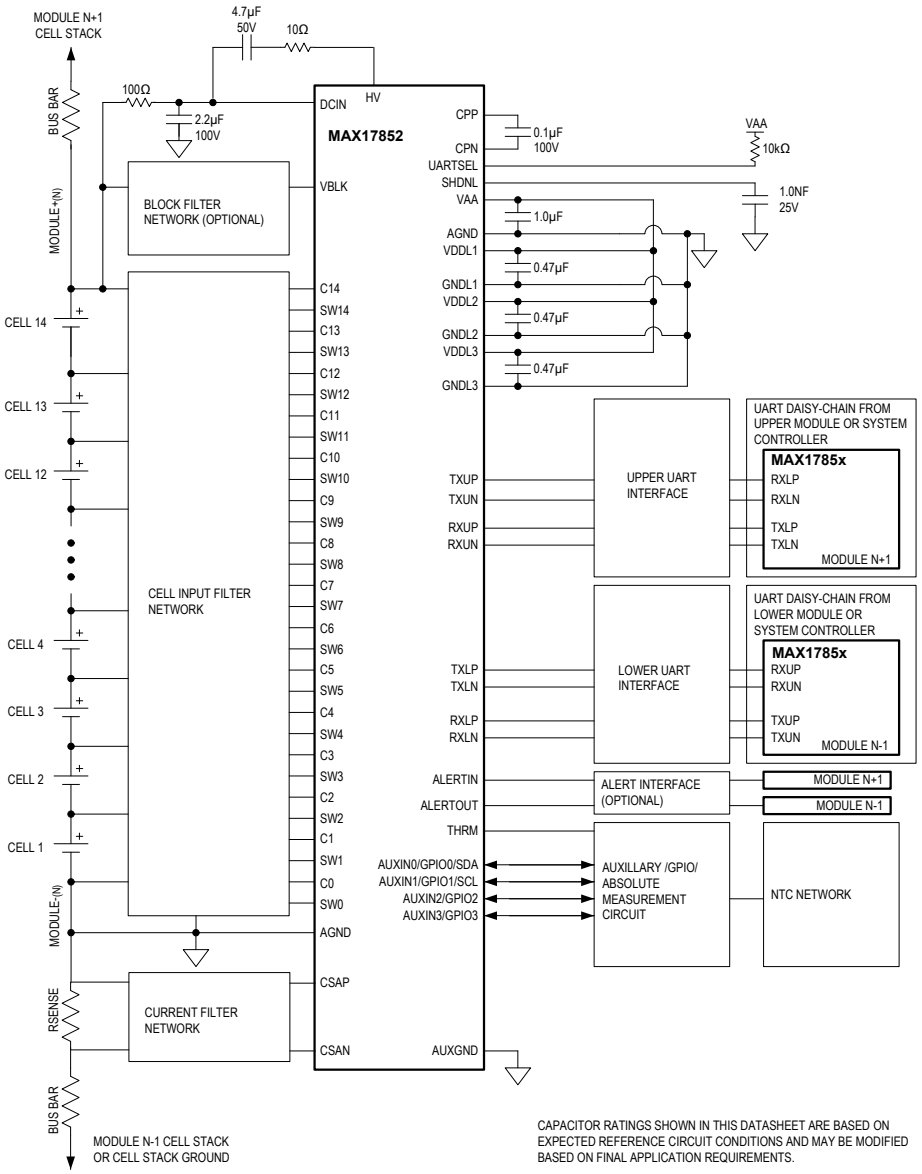
***Ordering Information* appears at end of datasheet.**

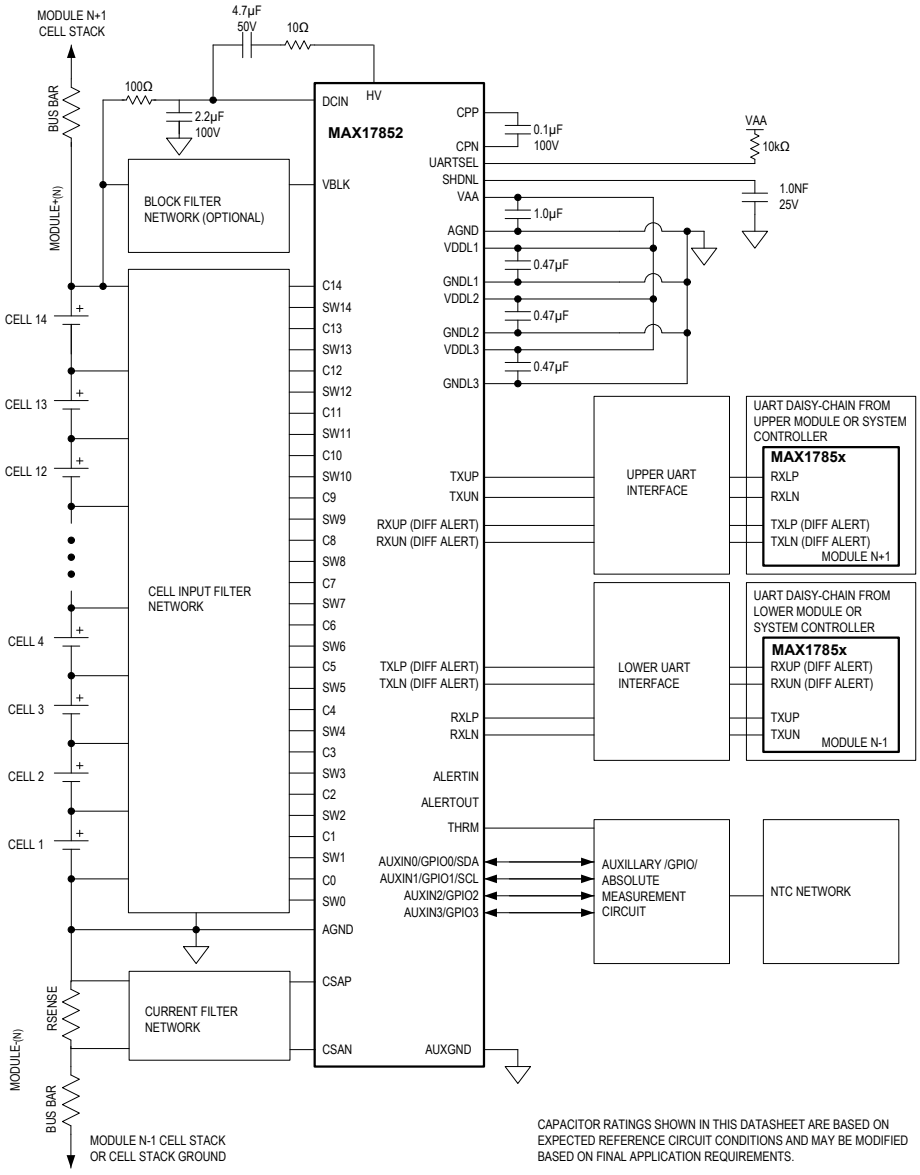
19-100902; Rev 0; 12/20

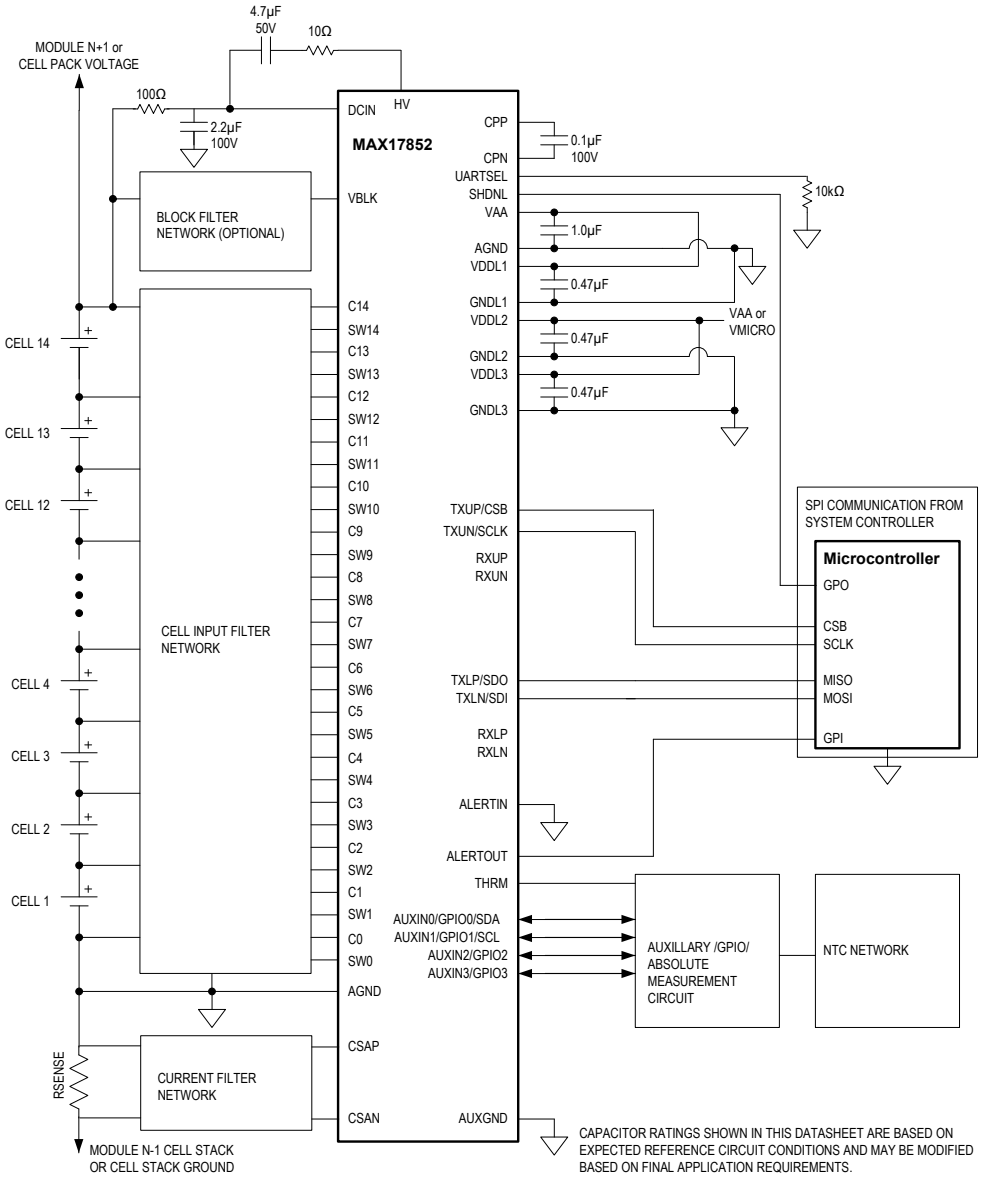
maxim integrated™

MAX17852 Simplified Application Diagrams

SPI Interface with Single-Ended Alert




MODULE N+1 CELL STACK
4.7µF
50V
10Ω
100Ω
2.2µF
100V
BUS BAR
MODULE+(N)
DCIN
HV
MAX17852
BLOCK FILTER NETWORK (OPTIONAL)
VBLK
CPP
0.1µF
100V
CPN
UARTSEL
SHDNL
VAA
10kΩ
1.0NF
25V
1.0µF
AGND
VDDL1
0.47µF
GNDL1
VDDL2
0.47µF
GNDL2
VDDL3
0.47µF
GNDL3
CELL 14
CELL 13
CELL 12
CELL 4
CELL 3
CELL 2
CELL 1
CELL INPUT FILTER NETWORK
C14
SW14
C13
SW13
C12
SW12
C11
SW11
C10
SW10
C9
SW9
C8
SW8
C7
SW7
C6
SW6
C5
SW5
C4
SW4
C3
SW3
C2
SW2
C1
SW1
C0
SW0
AGND
CSAP
CSAN
AUXGND
TXUP
TXUN
RXUP (DIFF ALERT)
RXUN (DIFF ALERT)
TXLP (DIFF ALERT)
TXLN (DIFF ALERT)
RXLP
RXLN
ALERTIN
ALERTOUT
THRM
AUXIN0/GPIO0/SDA
AUXIN1/GPIO1/SCL
AUXIN2/GPIO2
AUXIN3/GPIO3
UPPER UART INTERFACE
LOWER UART INTERFACE
UART DAISY-CHAIN FROM UPPER MODULE OR SYSTEM CONTROLLER
MAX1785x
RXLP
RXLN
TXLP (DIFF ALERT)
TXLN (DIFF ALERT)
MODULE N+1
UART DAISY-CHAIN FROM LOWER MODULE OR SYSTEM CONTROLLER
MAX1785x
RXUP (DIFF ALERT)
RXUN (DIFF ALERT)
TXUP
TXUN
MODULE N-1
AUXILLARY /GPIO/ ABSOLUTE MEASUREMENT CIRCUIT
NTC NETWORK
CURRENT FILTER NETWORK
RSENSE
MODULE-(N)
BUS BAR
MODULE N-1 CELL STACK OR CELL STACK GROUND
CAPACITOR RATINGS SHOWN IN THIS DATASHEET ARE BASED ON EXPECTED REFERENCE CIRCUIT CONDITIONS AND MAY BE MODIFIED BASED ON FINAL APPLICATION REQUIREMENTS.


MODULE N+1 or CELL PACK VOLTAGE
4.7µF 50V
10Ω
100Ω
2.2µF 100V
DCIN
HV
MAX17852
CPP
0.1µF 100V
CPN
UARTSEL
SHDNL
VAA
10kΩ
1.0µF
AGND
VDDL1
0.47µF
GNDL1
VDDL2
VAA or VMICRO
0.47µF
GNDL2
VDDL3
0.47µF
GNDL3
VBLK
BLOCK FILTER NETWORK (OPTIONAL)
CELL 14
CELL 13
CELL 12
CELL 4
CELL 3
CELL 2
CELL 1
CELL INPUT FILTER NETWORK
C14
SW14
C13
SW13
C12
SW12
C11
SW11
C10
SW10
C9
SW9
C8
SW8
C7
SW7
C6
SW6
C5
SW5
C4
SW4
C3
SW3
C2
SW2
C1
SW1
C0
SW0
AGND
CSAP
CSAN
RSENSE
CURRENT FILTER NETWORK
MODULE N-1 CELL STACK OR CELL STACK GROUND
TXUP/CSB
TXUN/SCLK
RXUP
RXUN
TXLP/SDO
TXLN/SDI
RXLP
RXLN
ALERTIN
ALERTOUT
THRM
AUXIN0/GPIO0/SDA
AUXIN1/GPIO1/SCL
AUXIN2/GPIO2
AUXIN3/GPIO3
AUXGND
SPI COMMUNICATION FROM SYSTEM CONTROLLER
Microcontroller
GPO
CSB
SCLK
MISO
MOSI
GPI
AUXILLARY /GPIO/ ABSOLUTE MEASUREMENT CIRCUIT
NTC NETWORK
CAPACITOR RATINGS SHOWN IN THIS DATASHEET ARE BASED ON EXPECTED REFERENCE CIRCUIT CONDITIONS AND MAY BE MODIFIED BASED ON FINAL APPLICATION REQUIREMENTS.

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Absolute Maximum Ratings

HV to AGND ..... -0.3V to +80V
DCIN, SWn, VBLK, Cn to AGND -0.3 V to min(V_{HV} + 0.3 or 72)V
Cn to Cn-1 ..... -72V to +72V
SWn to SWn-1 ..... -0.3V to +16V
V_{AA} to AGND ..... -0.3V to +4V
V_{DDL2}, V_{DDL3} to V_{AA} ..... -0.3V to +6.0V
V_{DDL1} to GNDL1 ..... -0.3V to +4V
V_{DDL2} to GNDL2 ..... -0.3V to +6V
V_{DDL3} to GNDL3 ..... -0.3V to +6V
V_{AA} to V_{DDL1} ..... -0.3V to +0.3V
AGND to GNDL1, GNDL2, GNDL3 ..... -0.3V to +0.3V
AGND to AUXGND ..... -0.3V
GPIOn/AUXINn ..... -0.3V to V_{DDL2} + 0.3V
THRM to AGND ..... -0.3V to V_{AA} + 0.3V
CSAP/CSAN to AGND ..... -0.3V to V_{AA} + 0.3V
SHDNL to AGND ..... -0.3V to V_{DCIN} + 0.3V
RXLP, RXLN, RXUP, RXUN, ALERTIN to AGND ... -30V to +30V
TXLP, TXLN, ALERTOUT to GNDL2 ..... -0.3V to +6V
TXUP, TXUN to GNDL3 ..... -0.3V to +6V
UARTSEL to AGND ..... -0.3V to V_{DDL1} + 0.3V
CPP to AGND ..... V_{DCIN} - 1V to V_{HV} + 1V
CPN to AGND ..... -0.3V to V_{DCIN} + 0.3V
Maximum Continuous Current into Any Pin (Note 1) ..... -20mA to +20mA
Maximum Continuous Current into SWn Pin (Note 2) . -650mA to +650mA
Maximum Average Power for ESD Diodes (Note 3) ... $14.4W/\sqrt{T}$
Package Continuous Power (Note 4) ..... mW to 2000mW
Operating Temperature Range ..... -40°C to +125°C
Storage Temperature Range ..... -55°C to +150°C
Junction Temperature (Continuous) ..... 150°C
Soldering Lead Temperature (10s maximum) ..... 300°C

Note 1: Balancing switches disabled.

Note 2: One balancing switch enabled, 60s (max).

Note 3: Average power for time period *T,* where *T* is the time constant (in µs) of the transient diode current during hot-plug event. For, example, if *T* is 330µs, the maximum average power is 0.793W. Peak current must never exceed 2A. Actual average power during hot-plug must be calculated from the diode current waveform for the application circuit and compared to the maximum rating.

Note 4: Multilayer board. For T_A > +70°C, derate 25mW/°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

LQFP

Package Code	C64+18
Outline Number	21-0083
Land Pattern Number	90-0141
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	40ºC/W
Junction to Case (θ_{JC})	8ºC/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25ºC. Operation is with the recommended application circuit. (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Supply Voltage, DCIN	V_{DCIN}		9		65	V

Electrical Characteristics (continued)

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25ºC. Operation is with the recommended application circuit. (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage, V_{DDL2}, V_{DDL3}	V_{DDL2}, V_{DDL3}		V_{AA}		5.5	V
DCIN Current, Shutdown Mode	I_{DCSHDN}	V_{SHDNL} = 0V		0.1		µA
DCIN Current, Standby Mode (Note 6)	I_{DCSTBY}	V_{SHDNL} > 1.8V, UART in idle mode; not in acquisition mode; balance switches, test current sources, and alert interface disabled	1.7	2.3	2.9	mA
DCIN Current, ADC Acquisition Mode (Note 6)	I_{DC_ADC}	All cell and auxiliary measurements enabled, OVSAMPL[2:0] = 000b. CSA disabled, CSAEN = 0b.		5.4	8.0	mA
DCIN Current, ADC Acquisition Mode with CSA (Note 6)	I_{DC_ADC}	All cells and auxiliary measurements disabled. CSA enabled, CSAEN = 1b.		6.3		mA
DCIN Current, COMP Acquisition Mode (Note 6)	I_{DC_COMP}	All cell and auxiliary measurements enabled		6	7.7	mA
DCIN Current, ADC + COMP Acquisition Mode (Note 6)	$I_{DC_ADCCOMP}$	All cell and auxiliary measurements enabled		6.8	8.4	mA
DCIN Incremental Current, SPI Communication Mode (Note 6)	I_{DCCOMM_SPI}	V_{SHDNL} > 1.8V, all channels disabled, all test current sources disabled, acquisition disabled		170	300	µA
DCIN Incremental Current, UART Communication Mode (Note 6)	I_{DCCOMM_UART}	Baud rate = 2Mbps (0% idle time preambles mode), 200pF load on TXUP and TXUN, TXL not active, not in acquisition mode, BALSWEN, CTSTEN = 0000h		170	300	µA
HV Current, ADC Acquisition Mode	I_{HVMEAS}	ADC-only acquisition, all cells and auxiliary channels enabled, V_{HV} = V_{DCIN} + 5.5V	0.9	1.1	1.3	mA
HV Current, Comparator Scan Mode	I_{HVCOMP}	COMP only acquisition, all cells and auxiliary channels enabled, V_{HV} = V_{DCIN} + 5.5V		1.8		mA
Incremental HV Current, Cell-Balancing Mode	I_{HVBAL}	V_{HV} = V_{DCIN} + 5.5V, n balancing switches enabled	(n + 1) x 5	(n + 1) x 15.5	(n + 1) x 26	µA
CELL VOLTAGE INPUTS (Cn, VBLK)						
Differential Input Range (Note 7)	V_{CELLn}	Unipolar mode	0		5	V
		Bipolar mode	-2.5		+2.5	
Common-Mode Input Range	V_{CnCM}	Not connected to SWn inputs	0		65	V
Input Leakage Current	I_{LKG_Cn}	Not in acquisition mode, V_{Cn} = 65V	-100	±10	+100	nA
VBLK Input Resistance	R_{VBLK}	V_{VBLK} = V_{DCIN} = 57.6V	4.5	10	20	MΩ

Electrical Characteristics (continued)

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25ºC. Operation is with the recommended application circuit. (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HVMUX Switch Resistance	R_{HVMUX}	CTSTDAC[3:0] = Fh	1.7	3.3	5	KΩ
CELL-BALANCING INPUTS (SWn)						
Leakage Current	I_{LKG_SW}	V_{SW0} = 0V, V_{SWn} = 5V, V_{SWn}-1 = 0V	-1.0		1.0	µA
Resistance, SWn to SWn-1	R_{SW}	BALSWEN[n-1] = 1, I_{SWn} = 100mA	0.5	1.25	2.25	Ω
Resistance, SWn to SWn-1 (Note 8)	R_{SW}	BALSWEN[n-1] =1, I_{SWn} = 300mA		1.3		Ω
Maximum Allowed Balancing Current (Note 9)	I_{BAL_MAX}	T_J = +125°C, CBMEASEN = 0x00, FLXPCKEN1/2 = 0, all even or all odd channels enabled		650		mA
AUXILIARY INPUTS (AUXINn)						
Input Voltage Range	V_{AUXIN}	V_{ADCREF} = V_{THRM} or V_{REF} based on AUXREFSEL	0		V_{ADCREF}	V
Input Leakage Current	I_{LKG_AUX}	Not in acquisition mode, V_{AUXINn} = 1.65V	-400	10	+400	nA
THRM OUTPUT						
Switch Resistance, VAA to THRM	R_{THRM}			25	70	Ω
Leakage Current	I_{LKG_THRM}	V_{THRM} = 3.3V	-1		+1	µA
CURRENT SENSE AMPLIFIER INPUTS (CSAP, CSAN)						
Input Voltage Range	V_{CSA}		-0.3		0.3	V
Gain Error, Current Sense Inputs	A_{V_CSA}	All gain settings	-0.3		0.3	%
Offset Error, Current Sense Inputs	V_{OS_CSA}	CSA gain = 256V/V, CSAP,CSAN=AGND		4		µV
		CSA gain = 4V/V, CSAP,CSAN=AGND		20		
Input Leakage Current	I_{LKG_CSA}	CSAP, CSAN = -300mV		10		nA
Input Differential Leakage Current	I_{Diff_Leak}	CSAP, CSAN = -300mV	-1		1	nA
MEASUREMENT ACCURACY						
ADC Measurement Error, HVMUX Inputs (Note 10)	$V_{CELLnERR}$	Unipolar mode,V_{CELLn} = 3.6V, SCANMODE = 0x0, 0x1		±0.45		mV
		Bipolar mode, V_{CELLn} = 1.1V, SCANMODE = 0x0, 0x1		±0.45		
	$V_{CELLnERR}$	Unipolar mode, 0.2V ≤ VCELLn ≤ 4.8V, SCANMODE = 0x0, 0x1	-4.5		+4.5	
	$V_{CELLnERR}$	Bipolar mode, -2.3V ≤ VCELLn ≤ +2.3V, SCANMODE = 0x0, 0x1	-4.5		+4.5	
		Unipolar mode, 1.9V ≤ VCELLn ≤ 4.2V, SCANMODE = 0x0, 0x1, 5°C < Temp < 40°C	-2		+2	

Electrical Characteristics (continued)

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25ºC. Operation is with the recommended application circuit. (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Measurement Error, ALTMUX Inputs (Note 10)	V_{SWnERR}	Unipolar mode,V_{CELLn} = 3.6V, SCANMODE = 0x0, 0x1		±0.45		mV
		Bipolar mode, V_{CELLn} = 1.1V, SCANMODE = 0x0, 0x1		±0.45		
		Unipolar mode, 0.2V ≤ V_{CELLn} ≤ 4.8V, SCANMODE = 0x0, 0x1	-4.5		+4.5	
		Bipolar mode, 0V ≤ VCELLn ≤ 2.3V, SCANMODE = 0x0, 0x1	-4.5		+4.5	
ADC Measurement Error, VBLK Input (Note 11)	V_{BLKERR}	9V ≤ V_{BLK} ≤ 65V, V_{DCIN} = 65V, SCANMODE = 0x0, 0x1	-110		+110	mV
		9V ≤ V_{BLK} ≤ 58.8V, V_{DCIN} = 58.8V, SCANMODE = 0x0, 0x1	-100		+100	
ADC Measurement Error, AUXIN Inputs (Note 11)	$V_{OS_AUX_RATIO}$	AUXREF[n] = 0b, SCANMODE = 0x0, 0x1	-3.5		+3.5	mV
ADC Measurement Error, AUXIN Inputs (Note 11)	$V_{OS_AUX_ABS}$	AUXREF[n] = 1b, SCANMODE = 0x0, 0x1	-2.5		+2.5	mV
Total Measurement Error, Die Temperature (Note 8)	T_{DIE_ERR}	T_J = -40°C to +125°C, OVSAMPL[2:0] = 000b	-5	0	+5	°C
Channel Noise (Note 8)	$V_{CELLNOISE}$	OVSAMPL[2:0] = 0x3h		250		μV_{RMS}
Differential Non-Linearity (Any Conversion)	DNL			±1.0		LSbs
ADC Resolution			12			bits
Level-shifting Amplifier Offset (Note 12)	V_{OS_LSAMP}	DIAGSEL[2:0] = 011b	-200	-10	+200	mV
COMPARATOR						
Comparator Accuracy	V_{OS_COMP}	0.2V ≤ VCELLn ≤ 4.8V	-20		20	mV
SHDNL INPUT AND CHARGE PUMP						
Input Low Voltage	V_{IL_SHDNL}				0.6	V
Input High Voltage	V_{IH_SHDNL}		1.8			V
Regulated Voltage	$V_{SHDNLIMIT}$	V_{DCIN} ≥ 12V	8	9.5	12	V
		V_{DCIN} = 9V		6.7		
Pulldown Resistance	$R_{FORCEPOR}$	FORCEPOR = 1	2.5	4.7	8	kΩ
Input Leakage Current	I_{LKG_SHDNL}	V_{SHDNL} = 3.3V			1	µA
		V_{SHDNL} = 65V		40	75	
Charge Pump Current - UARTL/UARTU (Note 13)	I_{SHDNL}	V_{SHDNL} < $V_{SHDNLIMIT}$, Baud rate = 2Mbps	15	117	350	µA

Electrical Characteristics (continued)

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25ºC. Operation is with the recommended application circuit. (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UARTSEL						
UARTSEL Input Low Voltage	$V_{IL_UARTSEL}$				0.3 x V_{AA}	V
UARTSEL Input High Voltage	$V_{IH_UARTSEL}$		0.7 x V_{AA}			V
UARTSEL Pullup Resistance	$R_{UARTSEL}$			100		kΩ
GENERAL-PURPOSE I/O (GPIOn)						
Input Low Voltage	V_{IL_GPIO}				0.3 x V_{DDL2}	V
Input High Voltage	V_{IH_GPIO}		0.7 x V_{DDL2}			V
Pull-down Resistance	R_{GPIO}	AUXINn/GPIOn configured as GPIO input	0.5	2	7.5	MΩ
Output Low Voltage	V_{OL_GPIO}	I_{SINK} = 3mA			0.4	V
Output High Voltage	V_{OH_GPIO}	I_{SOURCE} = 3mA	V_{DDL2} - 0.4			V
ALERTIN						
ALERTIN High Comparator Thershold	V_{CH}		-V_{AA}/2 - 0.4	-V_{AA}/2	-V_{AA}/2 + 0.4	V
ALERTIN Zero-Crossing Comparator Threshold	V_{ZC}		-0.4	0	+0.4	V
ALERTIN Low Comparator Threshold	V_{CL}		V_{AA}/2 - 0.4	V_{AA}/2	V_{AA}/2 + 0.4	V
ALERTIN Comparator Hysteresis	$V_{HYS_ALERTIN}$			75		mV
ALERTIN Common-mode Voltage bias	V_{CM}			V_{AA}/3		V
Leakage Current	$I_{LKG_ALERTIN}$	$V_{ALERTIN}$ = 1.5V		±1.0		µA
Input Capacitance	$C_{ALERTIN}$			2		pF
Bit Period (Note 14)	t_{BIT}			8		1/ f_{OSC_16M}
ALERTIN Fall Time (Note 8, 15)	$t_{ALERTIN_FALL}$				0.5	t_{BIT}
ALERTIN Rise Time (Note 8, 15)	$t_{ALERTIN_RISE}$				0.5	t_{BIT}
ALERTIN Qualification Time	$t_{ALERTIN_QUAL}$			25		µs
Propagation Delay (ALERTIN Port to ALERTOUT port)	t_{ALERT_PROP}			2.5	3	t_{BIT}
Start-Up Time from SHNDL high and VAA = 0V to ALERTIN valid	$t_{ALERTIN_STARTUP}$			1		ms

Electrical Characteristics (continued)

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25ºC. Operation is with the recommended application circuit. (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ALERTOUT						
Output Low Voltage	$V_{OL_ALERTOUT}$	I_{SINK} = 20mA			0.4	V
Output High Voltage	$V_{OH_ALERTOUT}$	I_{SOURCE} = 20mA	V_{DDL2} - 0.4			V
Leakage Current	$I_{LKG_ALERTOUT}$	$V_{ALERTOUT}$ = 1.5V	-1		+1	µA
REGULATOR						
Output Voltage	V_{AA}	0 ≤ I_{AA} < 20mA	3.2	3.3	3.4	V
Short-Circuit Current	I_{AASC}	V_{AA} shorted to AGND	30			mA
POR Threshold	$V_{PORFALL}$	V_{AA} falling	2.85	2.95	3.02	V
	$V_{PORRISE}$	V_{AA} rising		3	3.1	
	V_{PORHYS}			40		mV
Thermal Shutdown Temperature (Note 8)	T_{SHDN}	Temperature rising		145		°C
Thermal Shutdown Hysteresis (Note 8)	T_{HYS}			15		°C
HV CHARGE PUMP						
Output Voltage (VHV - VDCIN)	$V_{HV-DCIN}$	9V ≤ V_{DCIN} ≤ 12V, I_{LOAD} = 1.5mA	5.9	6.2	6.5	V
		12V ≤ V_{DCIN} ≤ 65V, I_{LOAD} = 3mA	5.9	6.2	6.5	
Output Voltage (VHV-VTOPCELL)	$V_{HV-DCIN_FLEX}$	14V ≤ V_{DCIN} ≤ 65V, I_{LOAD} = 3mA, FLXPCKEN1/2=1b	10.2		11	
Charge Pump Efficiency (Note 16)	Eff_{HVCP}	V_{DCIN} = 57.6V		38		V
OSCILLATORS						
32KHz Oscillator Frequency	f_{OSC_32K}		32.11	32.768	33.42	kHz
16MHz Oscillator Frequency	f_{OSC_16M}		15.68	16	16.32	MHz
DIAGNOSTIC TEST SOURCES						
Cell Test Source Current	I_{TSTCn}	CTSTDAC[3:0] = 9h, V_{C0} < V_{AA} - 1.4V, V_{AA} = 3.3V	50	62.5	75	µA
		CTSTDAC[3:0] = 6h, V_{C0} < V_{AA} – 1.4V, V_{AA} = 3.3V	36	45	54	
		CTSTDAC[3:0] = 6h, V_{C1-C14} > V_{AGND} + 1.4V	-54	-45	-36	
		CTSTDAC[3:0] =9Fh, V_{C1-C14} > V_{AGND} + 1.4V	-75	-62.5	-50	

Electrical Characteristics (continued)

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25ºC. Operation is with the recommended application circuit. (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HVMUX Test Source Current	$I_{TSTHVMUX}$	CTSTDAC[3:0] = 9h, V_{Cn} < V_{HV} - 1.4V, V_{HV} = 53.5V	25	31.25	37.5	µA
		CTSTDAC[3:0] = 6h, V_{Cn} < V_{HV} - 1.4V, V_{HV} = 53.5V	18	22.5	27	
AUXIN Test Source Current	$I_{TSTAUXIN}$	CTSTDAC[3:0] = 9h, V_{AUXINn} < V_{DDL2} - 1.4V, V_{DDL2} = 3.3V	50	62.5	75	µA
		CTSTDAC[3:0] = 6h, V_{AUXINn} < V_{DDL2} – 1.4V, V_{DDL2} = 3.3V	36	45	54	
		CTSTDAC[3:0] = 6h, V_{AUXINn} > V_{AGND} + 1.4V	-54	-45	-36	
		CTSTDAC[3:0] = 9h, V_{AUXINn} > V_{AGND} + 1.4V	-75	-62.5	-50	
CSAP & CSAN Test Source Current	I_{TSTCSA}	CTSTDAC[3:0] = 9h, V_{CSAn} < V_{AA} - 1.4V, V_{AA} = 3.3V	50	62.5	75	µA
		CTSTDAC[3:0] = 6h, V_{CSAn} < V_{AA} - 1.4V, V_{AA} = 3.3V	36	45	54	
DIAGNOSTIC REFERENCES						
ALTREF Voltage (Note 12)	V_{ALTREF}	DIAGSEL[2:0] = 001b	1.23	1.242	1.254	V
ALTREF Temperature Coefficient (ΔVALTREF/ΔT) (Note 8)	A_{ALTREF}			±25		ppm/°C
PTAT Output Voltage (Note 8)	V_{PTAT}	T_J = +120°C		1.2		V
PTAT Temperature Coefficient (ΔVPTAT/ΔT) (Note 8)	A_{V_PTAT}			3.02		mV/°C
PTAT Temperature Offset (Note 8)	T_{OS_PTAT}			-8.3		°C
ALERTS						
ALRTVDDLn Threshold	V_{VDDL_OC}	V_{AA} = 3.3V	3	3.15	3.25	V
ALRTGNDLn Threshold	V_{GNDL_OC}	AGND = 0V	0.05	0.15	0.3	V
ALRTHVUV Threshold	V_{HVUV}	V_{HV} - V_{DCIN} falling, FLXPCKEN1/2 = 0	4.5	4.75	5.0	V
		V_{HV} - V_{DCIN} falling, FLXPCKEN1/2 = 1	8.5	9.25	9.5	
ALRTHVOV Threshold	V_{HVOV}	V_{HV} - V_{DCIN} rising	14	16	20	V
ALRTHVHDRM Threshold	V_{HVHDRM}	ALRTHVHDRM = 0	4.7			V
ALRTTEMP Threshold (Note 8)	$T_{ALRTTEMP}$		115	120	125	°C
ALRTTEMP Hysteresis (Note 8)	$T_{ALRTTEMPHYS}$			2		°C

Electrical Characteristics (continued)

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25ºC. Operation is with the recommended application circuit. (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UART OUTPUTS (TXLP, TXLN, TXUP, TXUN)						
Output Low Voltage	V_{OL}	I_{SINK} = 20mA			0.4	V
Output High Voltage (TXLP, TXLN)	V_{OH}	I_{SOURCE} = 20mA	V_{DDL2} - 0.4			V
Output High Voltage (TXUP, TXUN)	V_{OH}	I_{SOURCE} = 20mA	V_{DDL3} - 0.4			V
Leakage Current	I_{LKG_TX}	V_{TX} = 1.5V	-1		+1	µA
UART INPUTS (RXLP, RXLN, RXUP, RXUN)						
Input Voltage Range	V_{RX}		-25		+25	V
Receiver High Comparator Threshold (Note 17)	V_{CH}		V_{AA}/2 - 0.4	V_{AA}/2	V_{AA}/2 + 0.4	V
Receiver Zero-Crossing Comparator Threshold (Note 17)	V_{ZC}		-0.4	0	+0.4	V
Receiver Low Comparator Threshold (Note 17)	V_{CL}		-V_{AA}/2-0.4	-V_{AA}/2	-V_{AA}/2+0.4	V
Receiver Comparator Hysteresis (Note 17)	V_{HYS_RX}			75		mV
Receiver Common-mode Voltage Bias (Note 17)	V_{CM}			V_{AA}/3		V
Leakage Current	I_{LKG_RX}	V_{RX} = 1.5V		±1.0		µA
Input Capacitance (RXLP, RXLN)	C_{RXL}			4		pF
Input Capacitance (RXUP, RXUN)	C_{RXU}			4		pF
UART TIMING						
Bit Period (Note 14)	t_{BIT}	Baud rate = 2Mb/s		8		1/ f_{OSC_16M}
		Baud rate = 1Mb/s		16		
		Baud rate = 0.5Mb/s		32		
RX Idle to START Setup Time (Note 8)	t_{RXSTSU}		0		1	t_{BIT}
STOP Hold Time to Idle (Note 8)	t_{SPHD}				0.5	t_{BIT}
RX Minimum Idle Time (STOP bit to START bit) (Note 8)	$t_{RXIDLESPST}$		1			t_{BIT}
RX Fall Time (Note 8, 15)	t_{FALL}				0.5	t_{BIT}
RX Rise Time (Note 8, 15)	t_{RISE}				0.5	t_{BIT}

Electrical Characteristics (continued)

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25ºC. Operation is with the recommended application circuit. (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay (RX Port to TX port)	t_{PROP}			2.5	3	t_{BIT}
Start-Up Time from SHNDL high and VAA = 0V to RXUP/RXUN valid	$t_{STARTUP}$			1		ms
SPI / SPI ELECTRICAL CHARACTERISTICS / POWER REQUIREMENTS						
I/O Supply Voltage	V_{DDIO}	V_{DDIO} = V_{DDL2} = V_{DDL3} for SPI applications.	V_{AA}	5	5.5	V
Static I/O Supply Current (Note SPI-1)	I_{DDIO}	Static inputs, all outputs unloaded			±25	µA
SPI / SPI ELECTRICAL CHARACTERISTICS / DIGITAL INPUT CHARACTERISTICS: SCLK, SDIN, CSB						
Input High Voltage	V_{IH}	3.0V < V_{DDIO} < 5.5V	0.7 x V_{DDIO}			V
Input Low Voltage	V_{IL}	3.0V < V_{DDIO} < 5.5V			0.3 x V_{DDIO}	V
Input Leakage Current (Note SPI-2)	I_{IN}	Vin = 0V or V_{DDIO}			±1	µA
Internal Safety Impedance (Note SPI-3, SPI-4)	R_{PD}	SDI, SCLK pull down to GND	40	100	160	kΩ
	R_{PU}	CSB pull up to V_{DDIO}	40	100	160	
Input Capacitance	C_{IN}			**20**		pF
Hysteresis Voltage	V_H			0.15		V
SPI / SPI ELECTRICAL CHARACTERISTICS / DIGITAL OUTPUT CHARACTERISTICS: SDO						
Output High Voltage	V_{OH}	V_{DDIO} > 3.0V, I_{SOURCE} = 5mA	V_{DDIO} -0.4			V
Output Low Voltage	V_{OL}	V_{DDIO} > 3.0V, I_{SINK} = 5mA			0.4	V
Output Short Circuit Current	I_{OSS_SOURCE}	I_{SOURCE}		600		mA
	I_{OSS_SINK}	I_{SINK}		220		
Output Tristate Leakage	I_{OZ}				±1	µA
Output Tristate Capacitance	C_{OZ}			**20**		pF
SPI / SPI TIMING CHARACTERISTICS						
SCLK Frequency (Note SPI-5)	f_{SCLK}		0.1		10	MHz
SCLK Period	t_{CP}		100		10000	ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
CSB Fall to SCLK Rise Setup Time	t_{CSS0}	To first SCLK rising edge	40			ns
CSB Fall to SCLK Rise Hold Time	t_{CSH0}	Applies to inactive rising edge preceding first rising edge	25			ns

Electrical Characteristics (continued)

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25ºC. Operation is with the recommended application circuit. (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Rise to CSB Rise Hold Time	t_{CSH1}	Applies to 32nd rising edge	25			ns
CSB Rise to SCLK Rise	t_{CSA}	Applies to 32nd rising edge, guarantees aborted (unqualified) sequence	15			ns
	t_{CSQ}	Applies to 33rd rising edge, guarantees qualified sequence	15			
CSB Pulse Width High	t_{CSPW}		400			ns
CSB Pulse Width High After SWPOR	t_{CSPWSP}	Applies after an accepted/executed SWPOR command.	100			µs
SDI to SCLK Rise Setup Time	t_{DS}		10			ns
SDI to SCLK Rise Hold Time	t_{DH}		10			ns
SCLK Fall to SDO Transition	t_{DOT}	C_{LOAD} = 20pf			30	ns
SCLK Fall to SDO Hold	t_{DOH}	C_{LOAD} = 0pf	2			ns
CSB Fall to SDO Transition	t_{DOE}	C_{LOAD} = 20pf			30	ns
CSB Rise to SDO Hi-Z	t_{DOZ}	Output disable time			25	ns
Time Out Period (Note SPI-6)	t_{TO}	Transactions exceeding this duration will be rejected			360	µs
I²C (Note I²C-1)						
Input Voltage Low	V_{IL}	$V_{AA} \le V_{DDL2} \le 5.5V$			$0.3V_{DDL2}$	V
Input Voltage High	V_{IH}	$V_{AA} \le V_{DDL2} \le 5.5V$	$0.7V_{DDL2}$			V
Input Voltage Hysteresis	V_{HYST}			0.15		V
Input Leakage Current (Note I²C-2)	I_{IN}		-1.0	0.1	1.0	µA
Input Capacitance	C_{IN}			10		pF
Output Voltage Low	V_{OL}	I_{SINK} = 3mA			0.4	V
SCL Clock Frequency	f_{SCL}	400kHz Mode (I2CFSCL = 1)	0		400	kHz
		100kHz Mode (I2CFSCL = 0)	0		100	
Hold Time for a (Repeated) START Condition	$T_{HD;STA}$	400kHz Mode (I2CFSCL = 1)	0.6			µs
		100kHz Mode (I2CFSCL = 0)	4.0			
SCL Pulse Width Low	t_{LOW}	400kHz Mode (I2CFSCL = 1)	1.3			µs
		100kHz Mode (I2CFSCL = 0)	4.7			
SCL Pulse Width High	t_{HIGH}	400kHz Mode (I2CFSCL = 1)	0.6			µs
		100kHz Mode (I2CFSCL = 0)	4.0			

Electrical Characteristics (continued)

(V_{DCIN} = +56V, T_A = T_{MIN} to T_{MAX} unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +125°C. Typical values are at T_A = +25ºC. Operation is with the recommended application circuit. (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for a Repeated START Condition	$t_{SU;STA}$	400kHz Mode (I2CFSCL = 1)	0.6			µs
		100kHz Mode (I2CFSCL = 0)	4.7			
Data Hold Time (Note I^2C-3)	$t_{HD;DAT}$		0			ns
Data Hold Time	$t_{HD;DAT}$	Master transmitting data.	300			ns
Data Setup Time	$t_{SU;DAT}$	Master receiving data, and 400kHz Mode (I2CFSCL = 1) bus monitor check.	100			ns
		Master receiving data, and 100kHz Mode (I2CFSCL = 0) bus monitor check.	250			
		Master transmitting data.	300			
Rise Time of SDA and SCL	t_r				300	ns
Fall Time of SDA and SCL	t_f				300	ns
Setup Time for STOP Condition	$t_{SU;STO}$	400kHz Mode (I2CFSCL = 1)	0.6			µs
		100kHz Mode (I2CFSCL = 0)	4.0			
Bus Free Time Between a STOP and START Condition	t_{BUF}	400kHz Mode (I2CFSCL = 1)	1.3			µs
		100kHz Mode (I2CFSCL = 0)	4.7			
Bus Capacitance Allowed	C_b				400	pF
Suppressed Spike Pulse Width	t_{sp}	Width of spikes that must be suppressed by the input filter of both SDA and SCL signals.		50		ns
Noise Margin at LOW Level	V_{nL}	For each connected device (including hysteresis).	$0.1V_{DDL}$ / 2			V
Noise Margin at HIGH Level	V_{nL}	For each connected device (including hysteresis).	$0.2V_{DDL}$ / 2			V

Note 5: Unless otherwise noted, limits are 100% production-tested at T_A = 25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 6: Acquisition mode (ADC conversions) is entered when the SCAN bit is set and ends when SCANDONE is set. With the typical acquisition duty-cycle very low, the average current I_{DCIN} is much less than I_{DCMEAS}. Total supply current during communication I_{DCIN} = I_{DCCOMM} + I_{DCSTBY}.

Note 7: Measurement accuracy range is guaranteed from V_{CELLn_min} +0.2V and V_{CELLn_max} - 0.2V.

Note 8: Guaranteed by design and not production tested.

Note 9: Not production tested. See Cell-Balancing Current section for details on the maximum allowed balancing current. Duty-cycle is calculated for a 10-year device lifetime.

Note 10: V_{CELLn} = V_{Cn} - V_{Cn-1}, V_{CELLn} = $V_{CELLn-1}$, and V_{DCIN} = 14 x $|V_{CELLn}|$ (V_{DCIN}=9V minimum). Accuracy measurements represent initial total measurement error with the input noise oversampled below 1LSB and over a temperature range of -20C to 125C. For specific measurement data criteria please contact Maxim.

Note 11: Accuracy measurements represent the initial total measurement error with the input noise oversampled below 1LSB.

Note 12: As measured during specified diagnostic mode.

Note 13: I_{SHDNL} measured with V_{SHDNL} = 0.3V, STOP characters, zero idle time, V_{RX_PEAK} = 3.3V.

Note 14: In daisy-chain applications, the bit time of the second stop bit may be less than specified to account for clock-rate variation and sampling error between devices.

Note 15: Fall time measured 90% to 10%; rise time measured 10% to 90%.

Note 16: Charge-pump efficiency = ΔI_{LOAD} / ΔI_{SUPPLY}, where I_{LOAD} is applied from HV to AGND, ΔI_{LOAD} = 5mA, and ΔI_{SUPPLY} = I_{DCIN} (for I_{LOAD} = 5mA) - I_{DCIN} (for I_{LOAD} = 0).

Note 17: Differential signal (V_{RXP} - V_{RXN}) where V_{RXP} and V_{RXN} do not exceed a common-mode voltage range of ±25V.

Note SPI-1: Static Logic inputs with V_{IL} = GNDL2/GNDL3 and V_{IH}=V_{DDIO} (Note 1). CSB = V_{IH} (if pull-up active).

Note SPI-2: No internal safety pullup/pulldown impedances active, input buffers only.

Note SPI-3: Internal safety pullup/pulldown impedances available, with enable function.

Note SPI-4: If pullup is supported, note CSB connection and diode to V_{DDL2}; this diode is present regardless of enable mode.

Note SPI-5: Applications must afford time for the device to drive data on the SDO bus and meet the µC setup time prior to the µC latching in the result on the following SCLK rising edge. In practice, this can be determined by loading and µC characteristics, and the relevant t_{DOT}/t_{DOE}.

Note SPI-6: Minimum specification is 32 x T_{CP_MAX} and must account for fastest possible frequency of the internal 16MHz oscillator (proposed numbers assume 5% variation over T_{PV}).

Note I²C-1: Timing parameters are subject to the variation of f_{OSC_16M}.

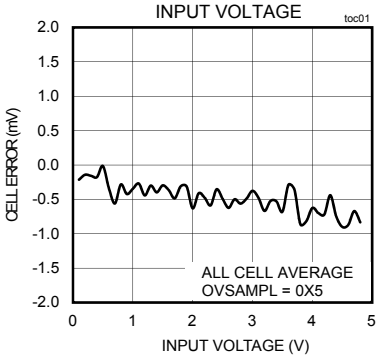
Note I²C-2: I²C pin leakage does not include the current associated with the R_{GPIO} pull down resistance.

Note I²C-3: A device must internally provide a hold time of at least 300nS for the SDA signal (referred to the V_{IH_min} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

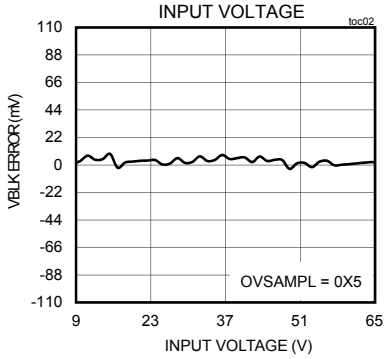
Typical Operating Characteristics

(DCIN = 56V, V_{AA} = 3.3V, T_A = +25°C unless otherwise noted)

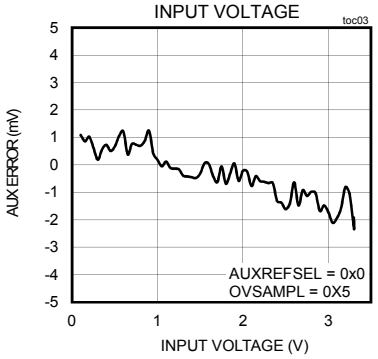
CELL ACCURACY vs. INPUT VOLTAGE



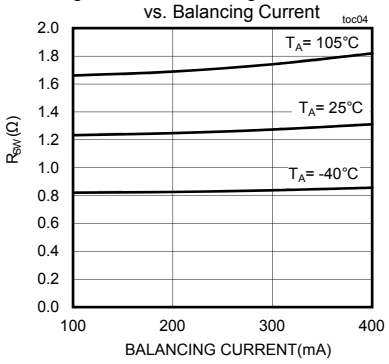
VBLK ACCURACY vs. INPUT VOLTAGE



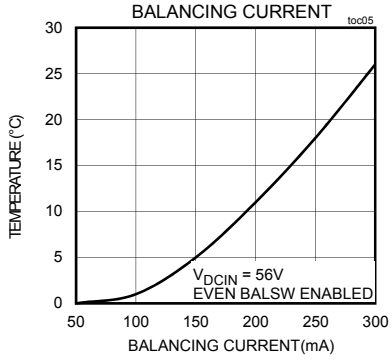
AUX ACCURACY vs. INPUT VOLTAGE

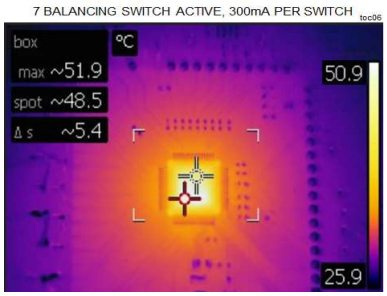


Single Channel Balancing Switch Resistance vs. Balancing Current

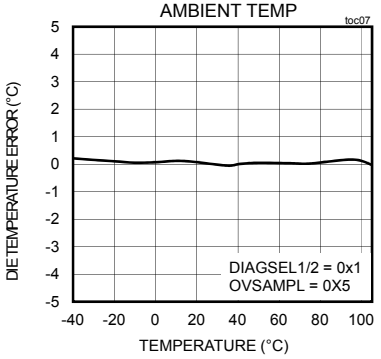


TEMPERATURE RISE vs. BALANCING CURRENT

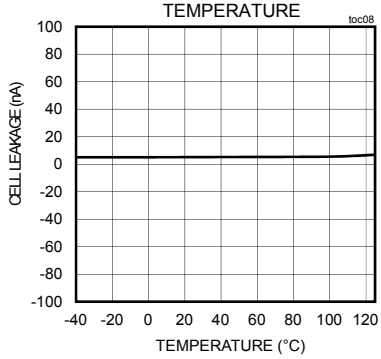




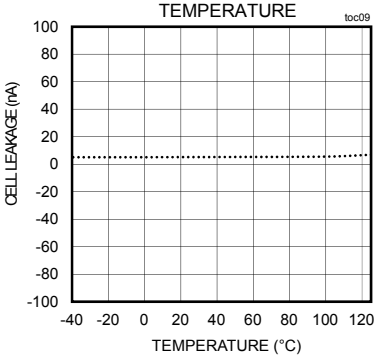
DIE TEMP ERROR vs. AMBIENT TEMP



CELL LEAKAGE vs. TEMPERATURE

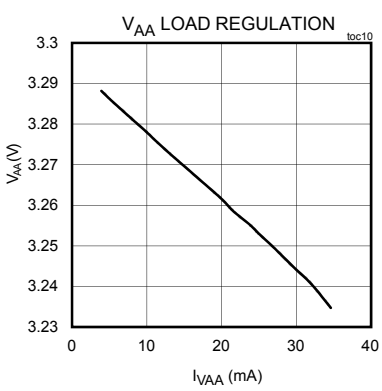


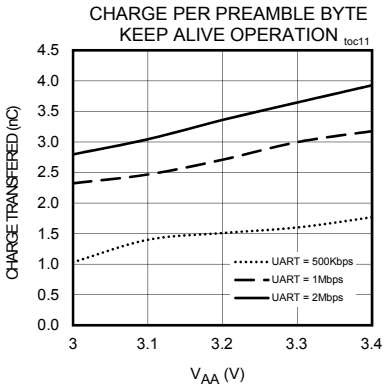
AUX LEAKAGE vs. TEMPERATURE



Typical Operating Characteristics (continued)

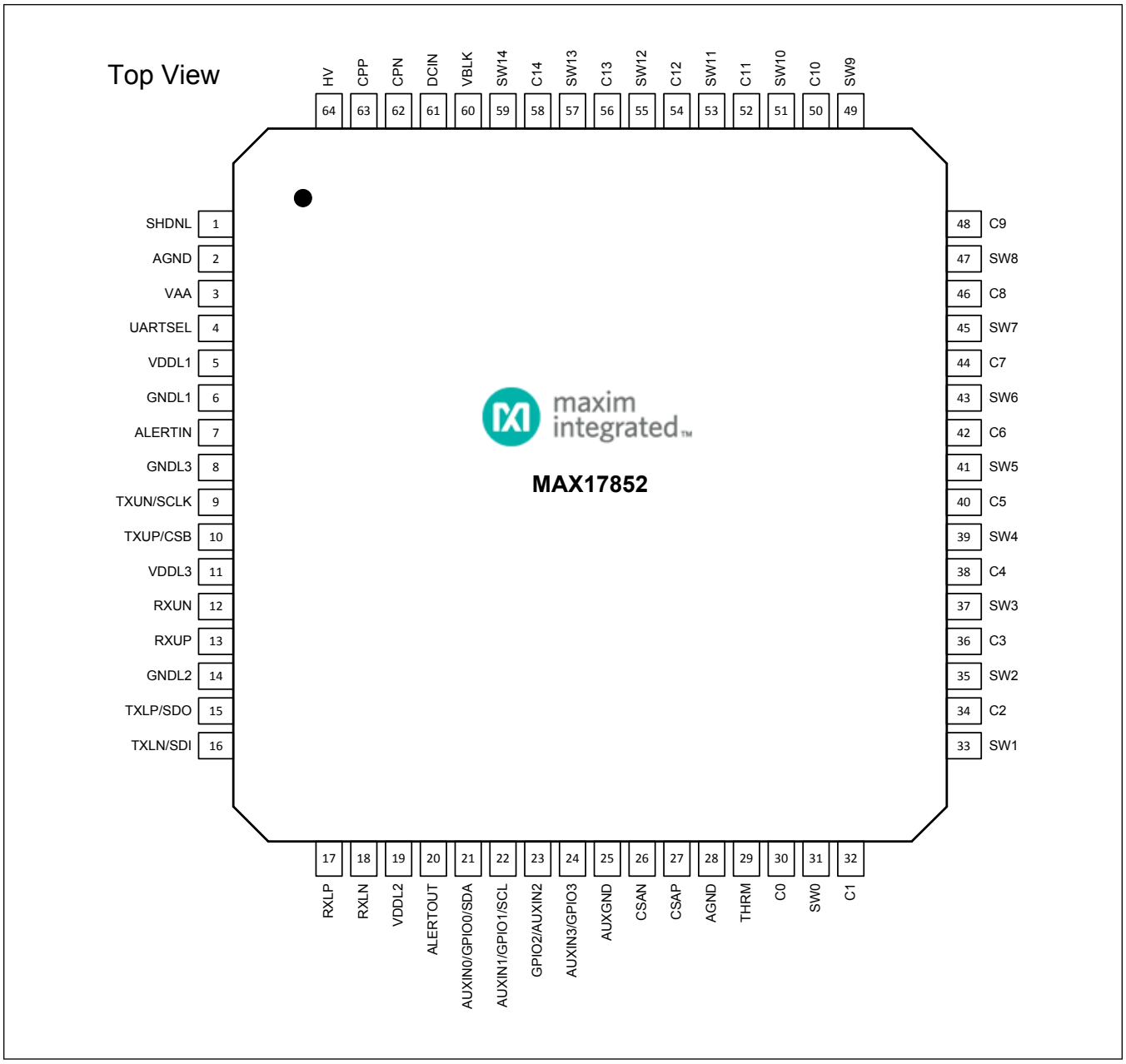
(DCIN = 56V, V_{AA} = 3.3V, T_A = +25°C unless otherwise noted)





Pin Configuration

MAX17852



Pin Description

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
1	SHDNL	Shutdown active-low input. Drive > 1.8V to enable operation and drive < 0.6V to reset the device and place it in shutdown mode. +72V tolerant. **UART Operation:** If not driven externally, this input can be controlled solely via UART communication and software control. Bypass with a 1nF capacitor to AGND. For single–ended UART, SHDNL must be driven externally. **SPI Operation:** SHDNL must be driven external.	AGND	Input
2	AGND	Analog ground. Connect to negative terminal of shunt resistor and ground plane.	DCIN	Ground
3	V_{AA}	V_{AA} output used to supply V_{DDL1}, and optionally V_{DDL2} and V_{DDL3}. Bypass with a 1µF capacitor to AGND.	AGND	Power
4	UARTSEL	UART/SPI Interface Selection. Connect to V_{AA} for UART interface, pull to AGND for SPI interface.	VDDL1	Input
5	V_{DDL1}	3.3V digital supply. Connect externally to V_{AA} and bypass with 0.47µF capacitor to GNDL1.	GNDL1	Power
6	GNDL1	Digital ground. Connect to ground plane.	V_{DDL1}	Ground
7	ALERTIN	Fault Alert input. Connect to upper daisy-chain device.	V_{AA}	Input
8	GNDL3	Ground for Upper-Port transmitter. Connect to ground plane.	V_{DDL3}	Ground
9	TXUN/SCLK	Negative output for Upper-UART transmitter or SCLK input for SPI interface depending on UARTSEL selection. Driven between V_{DDL3} and GNDL3.	V_{DDL3}	Output/Input
10	TXUP/CSB	Positive output for Upper-UART transmitter or CSB input for SPI interface depending on UARTSEL selection. Driven between V_{DDL3} and GNDL3.	V_{DDL3}	Output/Input
11	V_{DDL3}	Supply for Upper-UART transceiver, SPI Multifunctional Pins, and ALERT pins. Connect externally to V_{DDL2} and bypass with 0.47µF capacitor to GNDL3. V_{DDL3} must be ≥ V_{AA}.	GNDL3	Power
12	RXUN	Negative input for Upper-UART port receiver. If not used, pins can be left unconnected or connected to GNDL3. Tolerates ±30V.	V_{AA}	Input
13	RXUP	Positive input for Upper-UART port receiver. If not used, pins can be left unconnected or connected to GNDL3. Tolerates ±30V. If configured for single-ended UART, connect to GNDL3.	V_{AA}	Input
14	GNDL2	Ground for Lower-Port transmitter. Connect to ground plane.	V_{DDL2}	Ground
15	TXLP/SDO	Positive output for Lower-UART transmitter or SDO output (MISO) for SPI interface, depending on UARTSEL selection. Driven between V_{DDL2} and GNDL2.	V_{DDL2}	Output
16	TXLN/SDI	Negative output for Lower-UART transmitter or SDI (MOSI) input for SPI interface, depending on UARTSEL selection. Driven between V_{DDL2} and GNDL2.	V_{DDL2}	Output/Input
17	RXLP	Positive input for Lower-UART port receiver. If not used, pins can be left unconnected or connected to GNDL3. Tolerates ±30V. If configured for single-ended UART, connect to GNDL3.	V_{AA}	Input

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
18	RXLN	Negative input for Lower-UART port receiver. If not used, pins can be left unconnected or connected to GNDL2. Tolerates ±30V.	V_{AA}	Input
19	V_{DDL2}	Supply for Lower-UART transceiver, SPI Multifunctional Pins, and ALERT pins. Connect externally to V_{DDL3} and bypass with 0.47µF capacitor to GNDL2. V_{DDL2} must be ≥ V_{AA}.	GNDL2	Power
20	ALERTOUT	Alert output interface. Configured using SPIDRVINT as daisy-chained CMOS output (connected to ALERTIN), or open-drain output (connected to external 10kΩ pullup to V_{DDL2}, V_{DDL3}).	V_{DDL2}	Output
21	AUXIN0/ GPIO0/SDA	Configurable between Auxiliary Input, General-Purpose I/O or SDA. When configured as a ratiometric auxiliary input for temperature measurement, connect to a voltage-divider consisting of a 10KΩ pullup to THRM and a 10KΩ NTC thermistor to AGND. If not used, connect to the pullup only. When configured to GPIO, it is driven between V_{DDL2} and GNDL2. 2MΩ internal pulldown when the pin is configured as an input. When configure to I^2C SDA I/O, external pullup resistor is required. The pin is driven between V_{DDL2} and GNDL2.	V_{DDL2}	Input/Output
22	AUXIN1/ GPIO1/SCL	Configurable between Auxiliary Input, General-Purpose I/O or SCL. When configured as a ratiometric auxiliary input for temperature measurement, connect to a voltage divider consisting of a 10KΩ pullup to THRM and a 10KΩ NTC thermistor to AGND. If not used, connect to the pullup only. When configured to GPIO, it is driven between V_{DDL2} and GNDL2. 2MΩ internal pulldown when the pin is configured as an input. When configure to I^2C SCL, it becomes the clock output of I^2C.	V_{DDL2}	Input/Output
23	AUXIN2/ GPIO2	Configurable between Auxiliary Input, or General-Purpose I/O. When configured as a ratiometric auxiliary input for temperature measurement, connect to a voltage divider consisting of a 10KΩ pullup to THRM and a 10KΩ NTC thermistor to AGND. If not used, connect to the pullup only. When configured to GPIO, it is driven between V_{DDL2} and GNDL2. 2MΩ internal pulldown when the pin is configured as input.	V_{DDL2}	Input/Output

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
24	AUXIN3/ GPIO3	Configurable between Auxiliary Input, or General-Purpose I/O. When configured as a ratiometric auxiliary input for temperature measurement, connect to a voltage-divider consisting of a 10KΩ pullup to THRM and a 10KΩ NTC thermistor to AGND. If not used, connect to the pullup only. When configured to GPIO, it is driven between V_{DDL2} and GNDL2. 2MΩ internal pulldown when the pin is configured as input.	V_{DDL2}	Input/Output
25	AUXGND	Connect to AGND ground plane	V_{AA}	Power
26	CSAN	Current-sense negative input.	V_{AA}	Input
27	CSAP	Current-sense positive input.	V_{AA}	Input
28	AGND	Analog ground. Connect to negative terminal of shunt resistor and ground plane.	DCIN	Ground
29	THRM	Switched Output Connected Internally to V_{AA}. THRM is used to drive the external NTC voltage divider for the auxiliary inputs. The output is enabled only during measurements or as configured by THRMMODE[1:0]. This output can source up to 2mA.	AUXGND	Power
30	C0	Voltage input for Cell 1 negative. Connect to AGND.		Input
31	SW0	Balance input for Cell 1 negative.		Input
32	C1	Voltage input for Cell 1 positive (Cell 2 negative).		Input
33	SW1	Balance input for Cell 1 positive (Cell 2 negative).		Input
34	C2	Voltage input for Cell 2 positive (Cell 3 negative).		Input
35	SW2	Balance input for Cell 2 positive (Cell 3 negative).		Input
36	C3	Voltage input for Cell 3 positive (Cell 4 negative).		Input
37	SW3	Balance input for Cell 3 positive (Cell 4 negative).		Input
38	C4	Voltage input for Cell 4 positive (Cell 5 negative).		Input
39	SW4	Balance input for Cell 4 positive (Cell 5 negative).		Input
40	C5	Voltage input for Cell 5 positive (Cell 6 negative).		Input
41	SW5	Balance input for Cell 5 positive (Cell 6 negative).		Input
42	C6	Voltage input for Cell 6 positive (Cell 7 negative).		Input
43	SW6	Balance input for Cell 6 positive (Cell 7 negative).		Input
44	C7	Voltage input for Cell 7 positive (Cell 8 negative).		Input
45	SW7	Balance input for Cell 7 positive (Cell 8 negative).		Input
46	C8	Voltage input for Cell 8 positive (Cell 9 negative).		Input
47	SW8	Balance input for Cell 8 positive (Cell 9 negative).		Input
48	C9	Voltage input for Cell 9 positive (Cell 10 negative).		Input
49	SW9	Balance input for Cell 9 positive (Cell 10 negative).		Input
50	C10	Voltage input for Cell 10 positive (Cell 11 negative).		Input

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
51	SW10	Balance input for Cell 10 positive (Cell 11 negative).		Input
52	C11	Voltage input for Cell 11 positive (Cell 12 negative).		Input
53	SW11	Balance input for Cell 11 positive (Cell 12 negative).		Input
54	C12	Voltage input for Cell 12 positive. (Cell 13 negative).		Input
55	SW12	Balance input for Cell 12 positive. (Cell 13 negative).		Input
56	C13	Voltage input for Cell 13 positive. (Cell 14 negative).		Input
57	SW13	Balance input for Cell 13 positive. (Cell 14 negative).		Input
58	C14	Voltage input for Cell 14 positive.		Input
59	SW14	Balance input for Cell 14 positive.		Input
60	VBLK	Block voltage positive input. Internal pulldown resistor of R_{VBLK}.	DCIN	Input
61	DCIN	DC supply for the Low-Voltage Regulator, HV Charge Pump, and SHDNL Charge Pump. Connect to a voltage source between 9V and 65V via a 100Ω series resistor. Bypass with a 100V, 2.2µF capacitor to ground.		Power
62	CPN	Negative Capacitor Connection for the HV Charge Pump		Power
63	CPP	Positive Capacitor Connection for the HV Charge Pump. Connect a 100V, 0.1µF capacitor from CPP to CPN.		Power
64	HV	Decoupling Capacitor Connection for the HV Charge Pump. Bypass with a 50V, 4.7µF capacitor to DCIN.		Power

Detailed Description

The data acquisition system consists of the major blocks shown in Figure 1 and described in Table 1.

System Blocks

Table 1. SYSTEM BLOCKS

BLOCK	DESCRIPTION
ADC	Analog-to-Digital Converter. Uses a 12-bit successive-approximation register (SAR) with a reference voltage of 2.307V and supplied by V_{AA}.
HVMUX	14-channel high-voltage (65V) differential multiplexer for the C0-C14 inputs.
HV CHARGE PUMP	High-voltage charge-pump supply for the HVMUX, ALTMUX, BALSW, and LSAMP circuits, which must switch high-voltage signals. Supplied by DCIN.
LSAMP1	Level-shifting amplifier with a gain of 6/13. The result is that a 5V differential signal is attenuated to 2.307V, which is the reference voltage for the ADC.
LVMUX	Multiplexes various low-voltage signals including the level-shifted signals and temperature signals to the ADC for subsequent A-to-D conversion.
ALTMUX	12-channel, high-voltage differential multiplexer for the SW0-SW14 inputs.
BALSW	Cell-balancing switches.
LINREG	3.3V (V_{AA}) linear regulator used to power the ADC and digital logic. Supplied by DCIN.
REF	2.307V precision reference voltage for ADC and LINREG. Temperature-compensated.
ALTREF	1.242V precision reference voltage used for diagnostics.
16MHZ OSC	16MHz oscillator with 2% accuracy for clocking state-machines and UART timing.
32KHZ OSC	32,768Hz oscillator for driving charge pumps and timers.
LOWER PORT	Differential UART for communication with host or down-stack devices. Auto-detects baud rates of 0.5Mbps, 1Mbps, or 2Mbps.
UPPER PORT	Differential UART for communication with up-stack devices.
CONTROL AND STATUS	ALUs, control logic, and data registers
DIE TEMP	A proportional-to-absolute-temperature (PTAT) voltage source used to measure the die temperature.
COMPARATOR	A comparator path to detect OV/UV for Cell Voltage and AUXIN.
CURRENT SENSE AMPLIFIER	A programmable gain amplifier with gain of 4, 8, 16, 32, 64, 128, or 256 to measure a voltage across an external shunt resistance. Supplies from V_{AA} and provides differential signal +-2.307V, which is the reference voltage for the ADC.
SPI INTERFACE	SPI interface for communication with host.
LSAMP2	Level-shifting amplifier with a gain of 1. The result is a 5V differential signal that is compared against programmable OV and UV DAC thresholds.
I^2C MASTER	I^2C master interface for communication with I^2C slave.

MAX17852 Functional Block Diagram

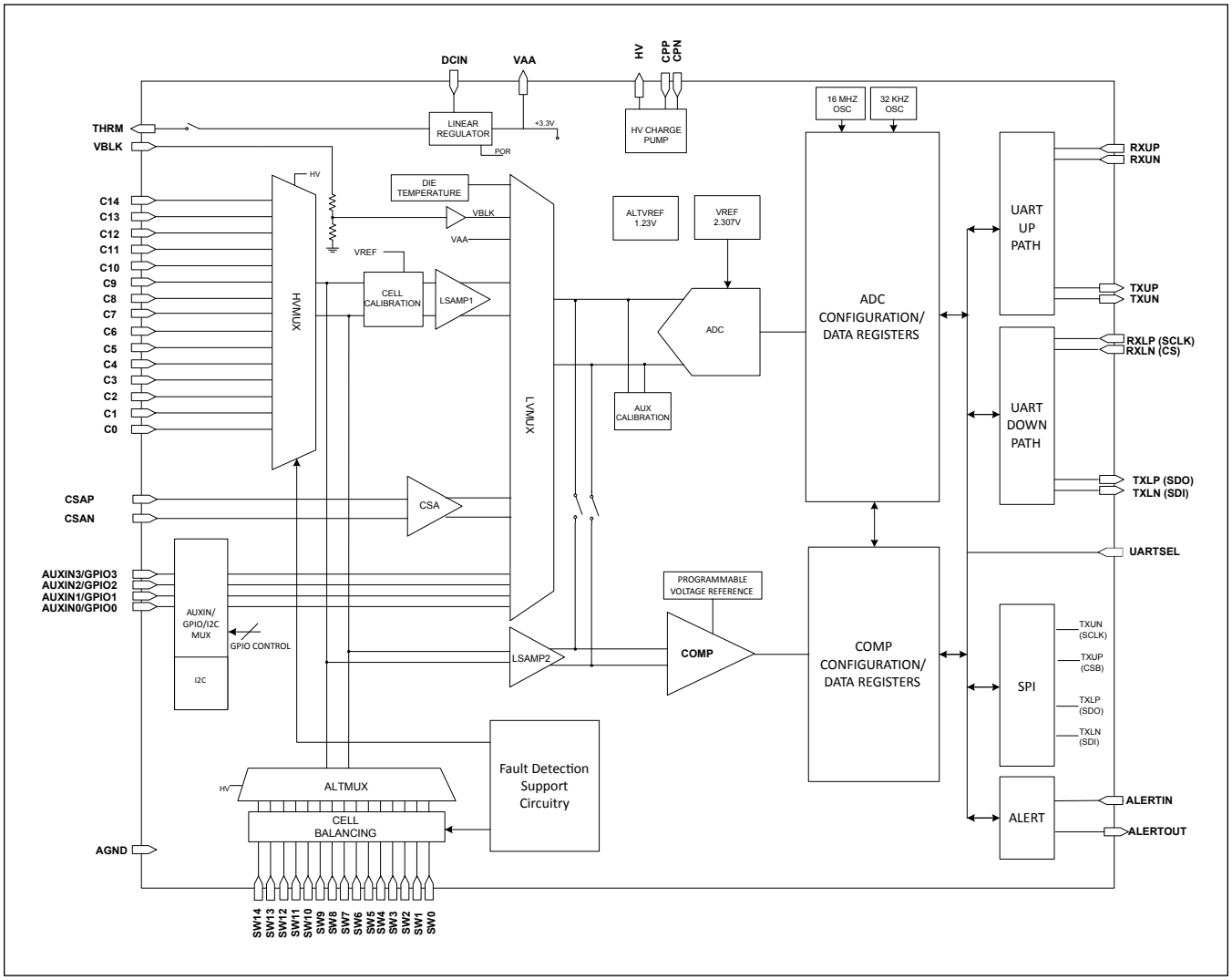


Figure 1. MAX17852 Functional Block Diagram

ESD Diodes Diagram

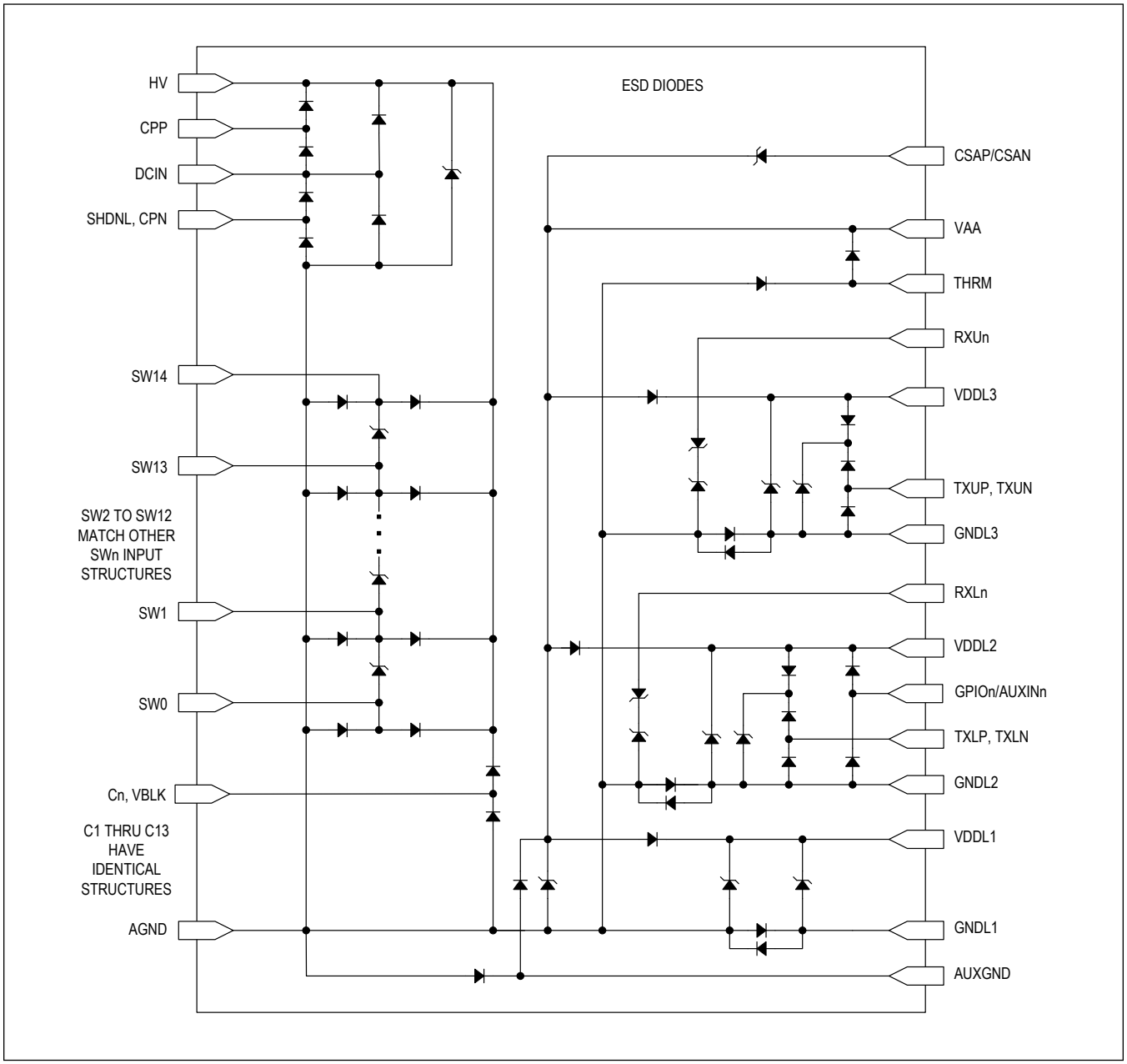


Figure 2. MAX17852 ESD Diagram

Notes:

1. All diodes are rated for ESD clamping conditions. They are not intended to accurately clamp DC voltage.
2. All diodes have a parasitic diode from AGND to their cathode that is omitted for clarity. These parasitic diodes have their anode at AGND.

MAX17852 Analog Front-End

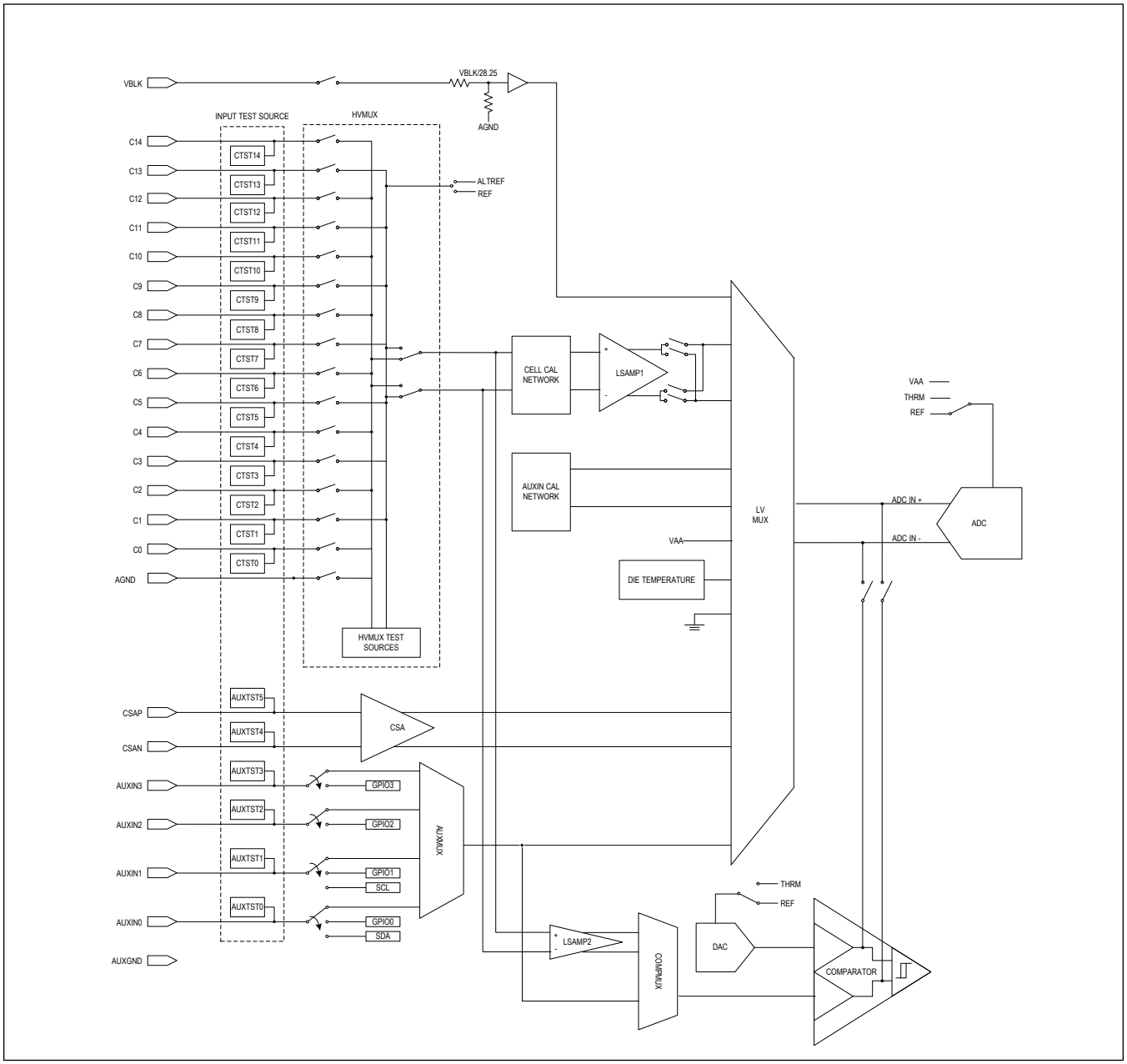


Figure 3. MAX17852 Analog Front-End

Terms, Definitions, and Data Conventions

Data Acquisition

A data acquisition is composed of the distinct processes defined in Table 2 and controlled by various configuration registers described in this section.

Configuration changes should be made prior to the acquisition in which the changes are to be effected.

Table 2. Data Acquisition Process

PROCESS	DESCRIPTION
Conversion	The ADC samples a single input channel, converts it into a 12-bit binary value, and stores it in an ALU register.
Scan	The ADC sequentially performs conversions on all enabled cell-input channels.
Measurement Cycle or Sample	The ADC performs two scans for the purpose of minimizing error in uncalibrated configurations. The conversions (two for each input channel) are averaged together to form a single 14-bit binary value called a measurement or sample.
Acquisition or Acquisition Mode	If oversampling is enabled, the ADC takes sequential measurements and averages them together to form one 14-bit binary value for each input channel sampled. If there is no oversampling, the acquisition is essentially a single measurement cycle.
Calibration	The measurement and correction factor applied to a Measurement Cycle or Sample based on current operating conditions. Calibration can be applied to a single scan in addition to the two-scan process to minimize error in the same fashion as a measurement cycle or sample **Note:** A single scan should not be implement without a valid calibration for the accuracy requirements defined in the Electrical Characteristics section.

Data Conventions

Representation of data follows the conventions shown in Table 3. All registers are 16-bit words.

Table 3. Numeric Conventions

DESCRIPTION	CONVENTION	EXAMPLE
Binary number	0b prefix	0b01100001 = 61h
Hexadecimal address	0x prefix	0x61
Hexadecimal data	h suffix	61h
Decimal data	d suffix	61d
Register bitfield	Register name [x]	STATUS[15] = 1
Register field	Field name [x:y]	DA[4:0] = 0b01100 = 0Ch = 12d
Register field and bitfield	Register name:bitfield	ADDRESS:DA
Concatenated numbers	{xxxx, yyyy}	{DA[4:0], 0b001} = 61h

Factory Trimming

The acquisition system is trimmed at the factory. The trim parameters are stored in a ROM consisting of 11 read-only registers (OTP2 – OTP12). ROMCRC is an 8-bit CRC value based on the calibration ROM and is stored in OTP12[15:8] at the factory. ROMCRC may be used to check the integrity of the trim as described in the *Diagnostics* section.

The factory trim can be further supplemented with a user on-demand calibration when used in a specific customer application.

Factory Programmed Device ID

The ID1 register together with ID2 provide a 32-bit manufacturing identification number, DEVID[31:0]. This ID will be unique among all devices with the same model type and version (VERSION:MOD,VER, respectively); taken together, VERSION, ID1, and ID2 provide a means to uniquely identify all devices shipped by the factory. Although not required, the manufacturing date information provided on the package provides a further means of device tracking. A device ID of zero is invalid.

Introduction

The MAX17852 is a software-configured ASIL-D data-acquisition system for both high-voltage and low-voltage (48V)-

rated applications, supporting a flexible configuration of cell-voltage measurements, pack-voltage measurements, temperature measurements, auxiliary-voltage measurements, and current measurements. All measurements are synchronously sampled within an acquisition and have minimal delay between acquired samples. Additional programmability is available for balancing currents, and system-interconnect measurements (bus bars) to provide a complete measurement solution independent of hardware configuration.

The following sections describe the device operation, feature set, and programming of the MAX17852.

Flexible Battery-Pack Configuration

The main supply voltage, DCIN, can be routed internally using the SW8-SW14 inputs of the highest stacked cell. This allows for a single hardware configuration to serve multiple battery modules without requiring external hardware or wiring-harness changes.

The flexible battery-pack configuration is enabled by default using FLXPCKEN1/2 bit, to allow for internal powering conditions. If this configuration is not required, the DCIN can still be driven externally, which will effectively disable the flexible battery-pack configuration. Prior to SDHNL being actively controlled, the DCIN voltage will be driven towards HV and clamped at the highest voltage applied at the SW8-SW14 inputs. When SHDNL is asserted, DCIN will be driven to within 1V below the highest stacked cell, if no external DCIN is provided. In this case, the host must define the TOPCELL1[3:0] and TOPCELL2[3:0] of the stack by writing to the PACKCFG register and by asserting the FLXPCKEN1 and FLXPCKEN2 bits. TOPCELL_[3:0] selection configures the top-cell position if less than 14 channels are used. TOPCELL_[3:0] selections 0x0 to 0x7 and 0xF are not supported and will be mapped to an OFF position (power-on default).

If FLXPCKEN1/2 is unintentionally de-asserted while the SHDNL is driven high with no external DCIN connection, it is expected that the voltage seen at the DCIN pin will fall at a rate proportional to the current consumption of the part and the external decoupling capacitance, until the POR threshold is reached. This resets the digital logic and returns the FLXPCKEN to the desired power-on reset state.

If FLEXPCKEN1 and FLEXPCKEN2 or TOPCELL1 and TOPCELL2 are not the same, the power-on default values will be applied.

Note: It is important that TOPCELL1 and TOPCELL2 selects the highest applied cell input, as an invalid configuration can create an internal path which would connect the highest battery voltage to the selected TOPCELL1/2 input.

A second mux internally connects VBLK to a selected cell input after host defines the TOPCELL_[3:0] of the stack and asserts the FLXPCKEN_ bit. TOPBLOCK[3:0] selects the Cn pin to be connected to the VBLOCK resistive divider. 0xF (default) selects the VBLK pin. TOPBLOCK_ selections 0x0 through 0x7 are not supported and will be mapped to 0xF (VBLK, default).

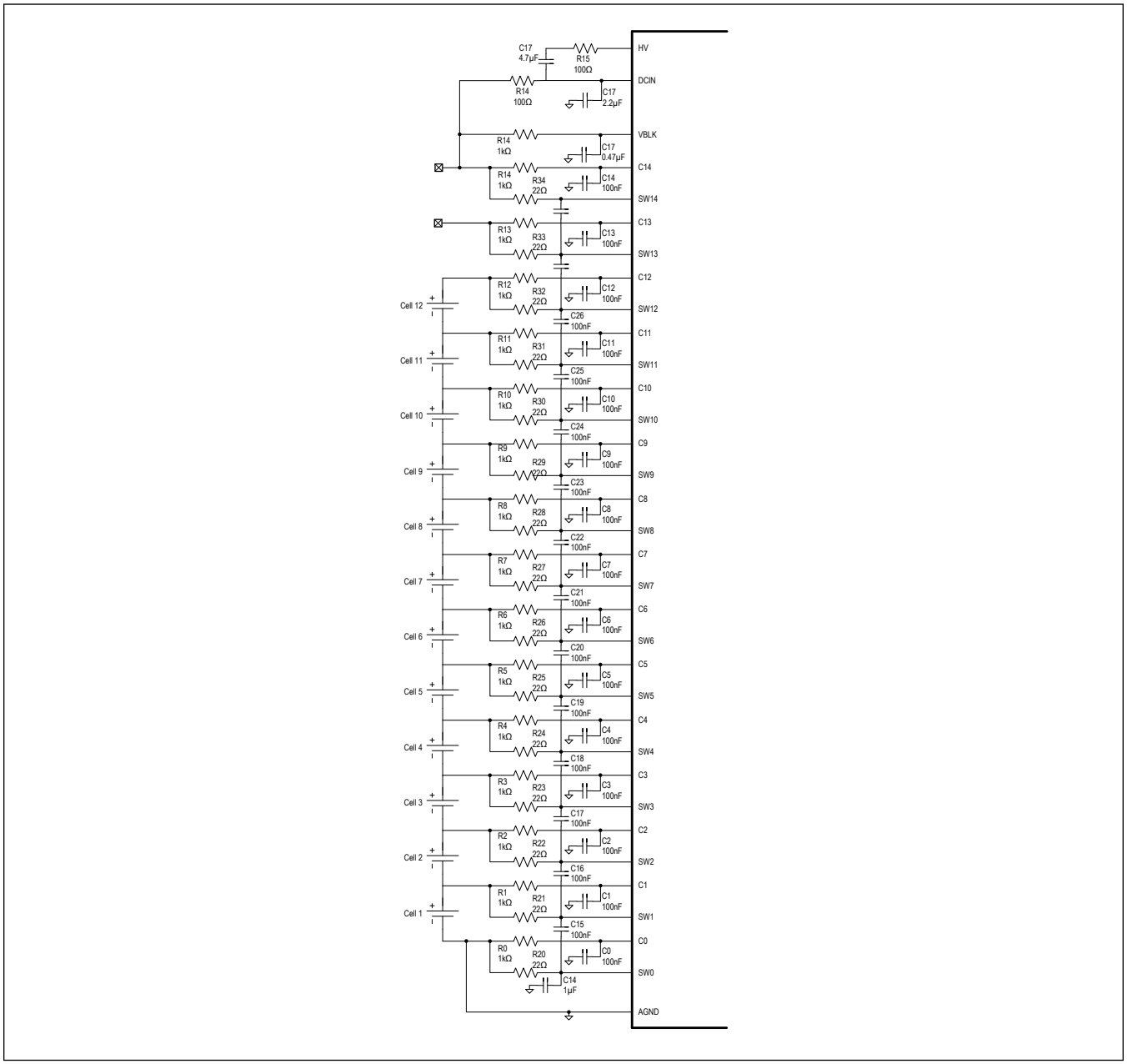


Figure 4. Flexible-Pack Configuration for 12-Cell Pack on 14-Channel CMC

Flexible Pack Interaction with Acquisitions

If FLXPCKEN1/2 and FLXPCKSCAN are asserted, the switch input denoted in the TOPCELL1 and TOPCELL2 bitfields is disconnected from DCIN and the internal power consumption will be supplied by the external decoupling/hold-up capacitance on the DCIN pin. A 30µs delay will be inserted prior to the TOPCELL conversion, allowing the external switch filter network to settle before converting the input voltage.

Note: FLXPCKSCAN only affects ALTMUX acquisitions. If the ALTMUX accuracy is not required for the application, no

changes are required to the application circuit regardless of the FLXPCKSCAN setting. It is however, recommended to set FLXPCKSCAN = 0 to ensure that the quickest sampling rate is achieved.

Power-Multiplexing Operation (Cell Balancing)

The top two balancing switches should not be configured simultaneously while in manual Cell-Balancing mode when the internal power multiplexing is configured. This configuration creates a voltage drop in the DCIN supply equivalent to a cell voltage, which can result in large measurement errors of the top-cell reading with both the HVMUX and ALTMUX configured.

TOPCELL_[3:0] and FLXPCKEN_ must refer to the top cell in the pack, and not a bus bar, if the top-used channel in the pack is a bus bar. TOPBLOCK_ can refer to cells above TOPCELL_.

Flexible Pack Alert

An ALRTDCINMUX is triggered to indicate a fault in the DCINMUX switch. A high condition indicates the enabled DCINMUX is not functioning properly in a Flex Pack application. Performance may be impacted, and/or other related faults may be issued. The ALRTDCINMUX is gated until clear of ALRTRST after power-up has occurred.

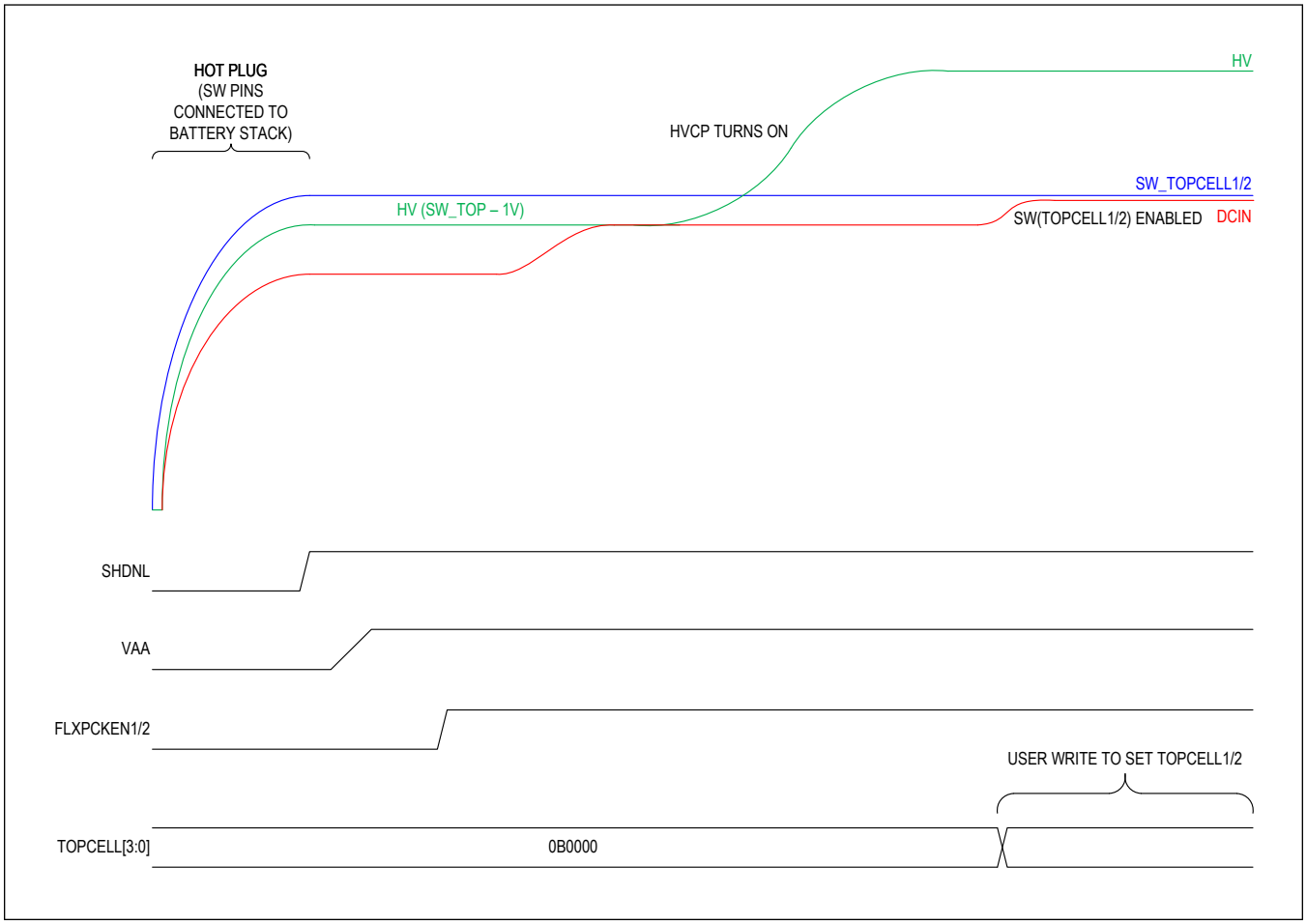


Figure 5. Flexible-Pack Power-On Timing

Cell Inputs

Up to 14 voltage measurements can be sampled differentially from the 15 cell inputs. The differential signal V_{CELLn} is defined as $V_{Cn} – V_{Cn-1}$ where n = 1 to 14.

The cell inputs are selected by the corresponding CELLEN bits in the MEASUREEN1 register. Additionally, the input path for the measurement acquisition is selected using SCANCTRL:ALTMUXSEL. The ALTMUXSEL bit allows for two different measurement configurations: HVMUX and ALTMUX acquisitions. The HVMUX path selection is used for the primary measurement acquisition due to the higher filtering achieved by the external input network. Alternatively, the ALTMUX path selection is primarily used for cell balancing and typically does not have a large RC filter. Due to the parallelism of the external filter network, as well as the internal block structures, the ALTMUX path selection also allows for independent measurement redundancy to improve safety, performance, and device robustness.

During the scan, the selected signal is multiplexed into the level-shifting amplifier (LSAMP1 or LSAMP2) as shown in Figure 6. Since the common-mode range of the input signals is 0V to 65V, the signal must be level-shifted to the common-mode range of the amplifier. Both ADC and comparator signal paths have a gain of 6/13 so that a 5V differential signal is attenuated to the ADC and Comparator full-scale reference voltage (V_{REF}).

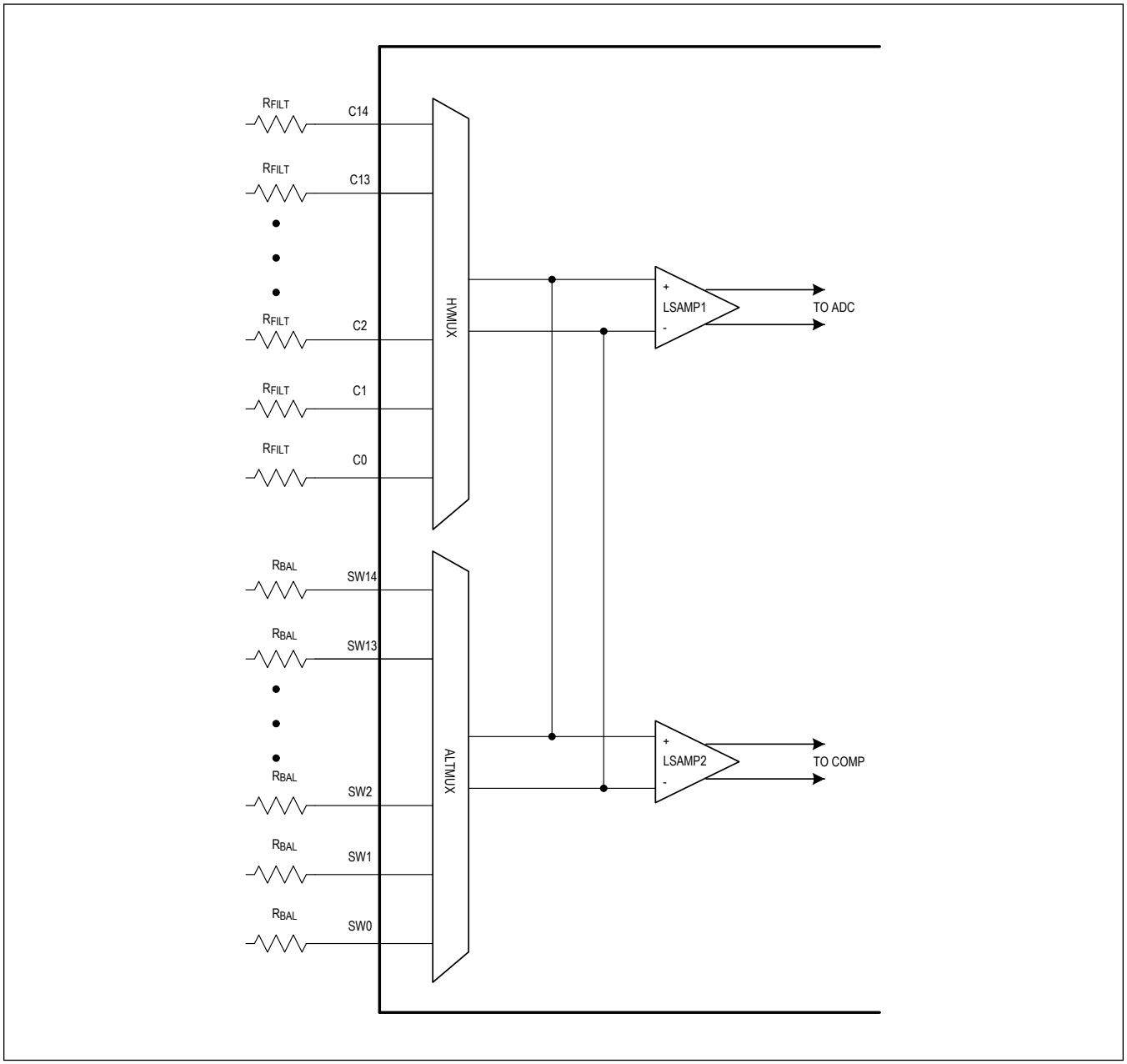


Figure 6. Cell Signal Path

Once the signal is properly conditioned, the ADC starts the conversion. The 12-bit conversion is stored in an ALU register where it can be averaged with subsequent conversions for increased resolution. The ALU output is a 14-bit value, relating to a 305µV voltage resolution, and is ultimately stored in a 16-bit register, CELLnREG, with the two least-significant bits 0. Disabled channels maintain their previous measurement result. Unless stated otherwise, measurement values are assumed to be 14-bit values. The 16-bit register values can be converted to 14-bit values by dividing by 4 (and vice-versa). To convert the measurement value in register CELLnREG to a voltage, convert the 14-bit hexadecimal value to a decimal value and then convert to voltage as follows:

V_{CELLn} = CELLnREG[15:2] x 5 V / 16384 = CELLnREG[15:2] x 305.176µV

Bus Bar Inputs

Bus-bar inputs can be applied to any of the 14 cell inputs. Due to the resistive nature of the bus bar, the current applied to the battery pack or discharged from the battery pack will affect the polarity of the voltage measurement. To support this requirement, the POLARITY bits corresponding to the bus-bar location must be configured for bipolar conversion (POLARITY[n] = 1b).

Due to the negative voltage that can be generated across the bus bars SW_n to SW_{n-1} inputs, it is recommended to place an external Schottky diode across the inputs to the reverse voltage seen by the body diode of the internal balancing switch, as shown below, to shunt current away from the internal conduction path.

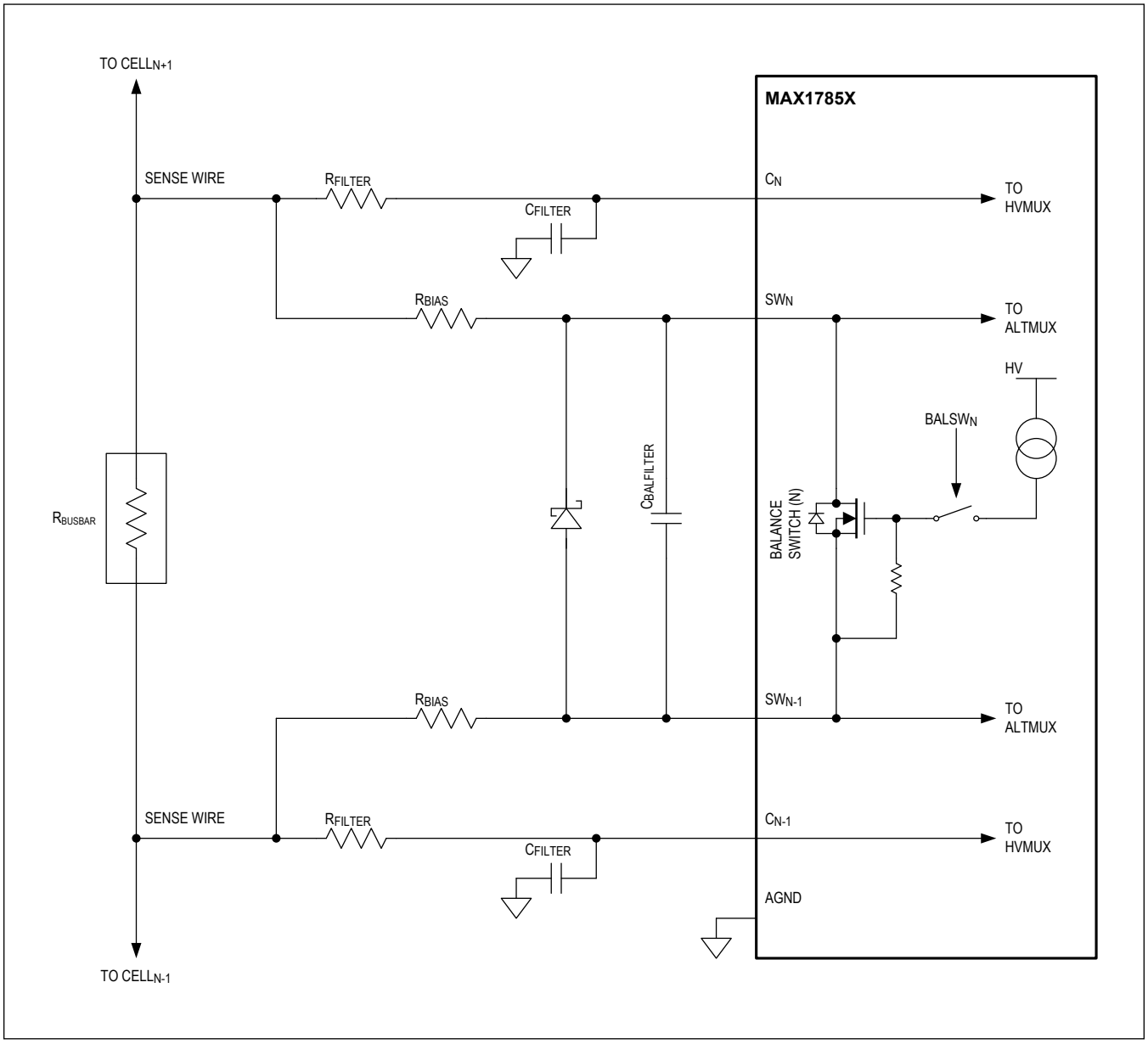


Figure 7. Bus-Bar Switch Configuration

Block-Voltage Input

The VBLK input pin to the MAX17852 allows for the pack voltage (total cell voltage) to be measured independently of summing the individual cell voltages from an acquisition. This comparison provides an extra layer of measurement redundancy within the system.

The VBLK voltage is attenuated by a voltage-divider of 28.17 for the acquisition process to translate the 65V full-scale block input voltage into the full-scale ADC input voltage (V_{REF})

Outside of the acquisition the VBLK input path is opened to avoid power consumption from the internal 10MΩ divider.

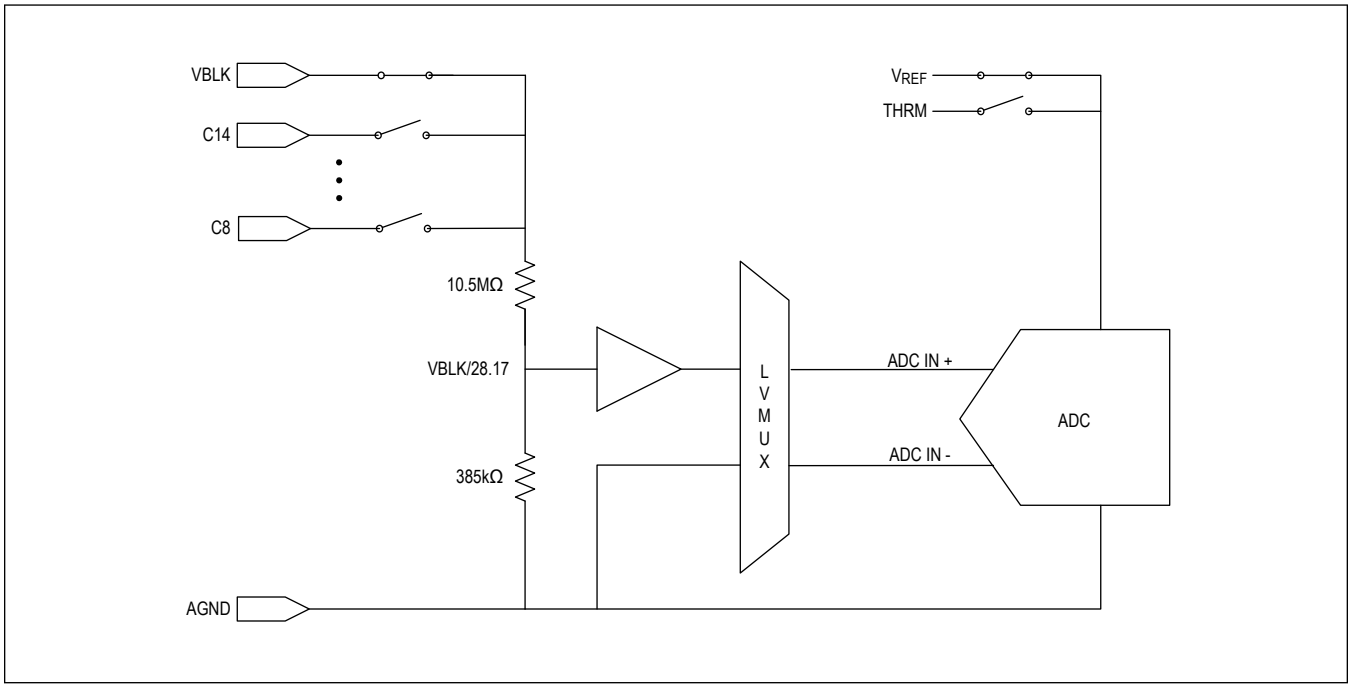


Figure 8. Block-Measurement Path

The measurement is enabled in an acquisition by asserting BLOCKEN in the MEASUREEN1 register. The measurement is stored in the VBLOCK[13:0] bits of the BLOCKREG register, where each bit has a resolution of 3.967mV.

Auxiliary Inputs

The MAX17852 has 4 auxiliary ports that can be used to measure external temperatures, measure external voltages, or be re-purposed for digital functions (GPIO or I^2C Master).

Auxiliary Inputs: Ratiometric Temperature Measurement

Individual auxiliary ports can be configured to measure external temperatures through enabling auxiliary measurements using the AUXEN bits in the MEASUREEN2 register, or through configuring the conversion voltage as ratiometric using the AUXREFSEL bits in the AUXREFCTRL register.

Note: If the individual auxiliary port is configured as a GPIO using GPIOEN bits in the AUXGPIOCFG register while the corresponding AUXEN bit is high, then the auxiliary setting will be ignored and the port will be configured as a GPIO.

The ratiometric configuration selects the conversion voltage of both the ADC and Comparator to $V_{AA,}$ while also outputting V_{AA} on the THRM pin. An external resistive divider can then be created with a pullup resistor to the THRM pin and a NTC connected to the AUXGND pin as shown in Figure 9.

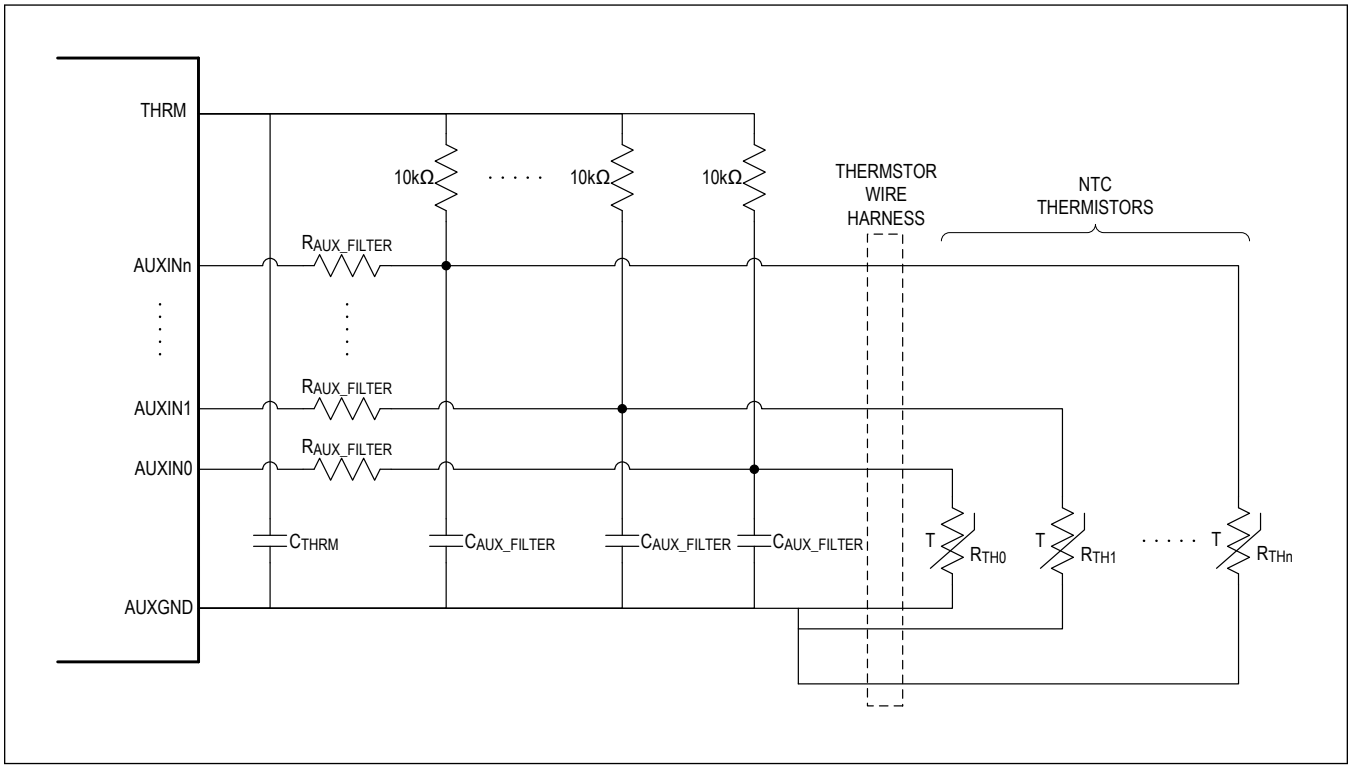


Figure 9. Auxiliary Application Circuit

Explicit control on the THRM pin output is provided using the THRMMODE bits in the ACQCFG register. Setting THRMMODE to 00b or 01b enables automatic mode, in which the THRM switch will be closed at the beginning of an acquisition. Setting THRMMODE to 11b enables manual mode, in which the THRM switch is always closed. The ability to configure THRMMODE allows for the application tradeoffs between the external NTC network's power consumption on V_{AA} and the need to settle the external NTC network to achieve the highest accuracy measurements.

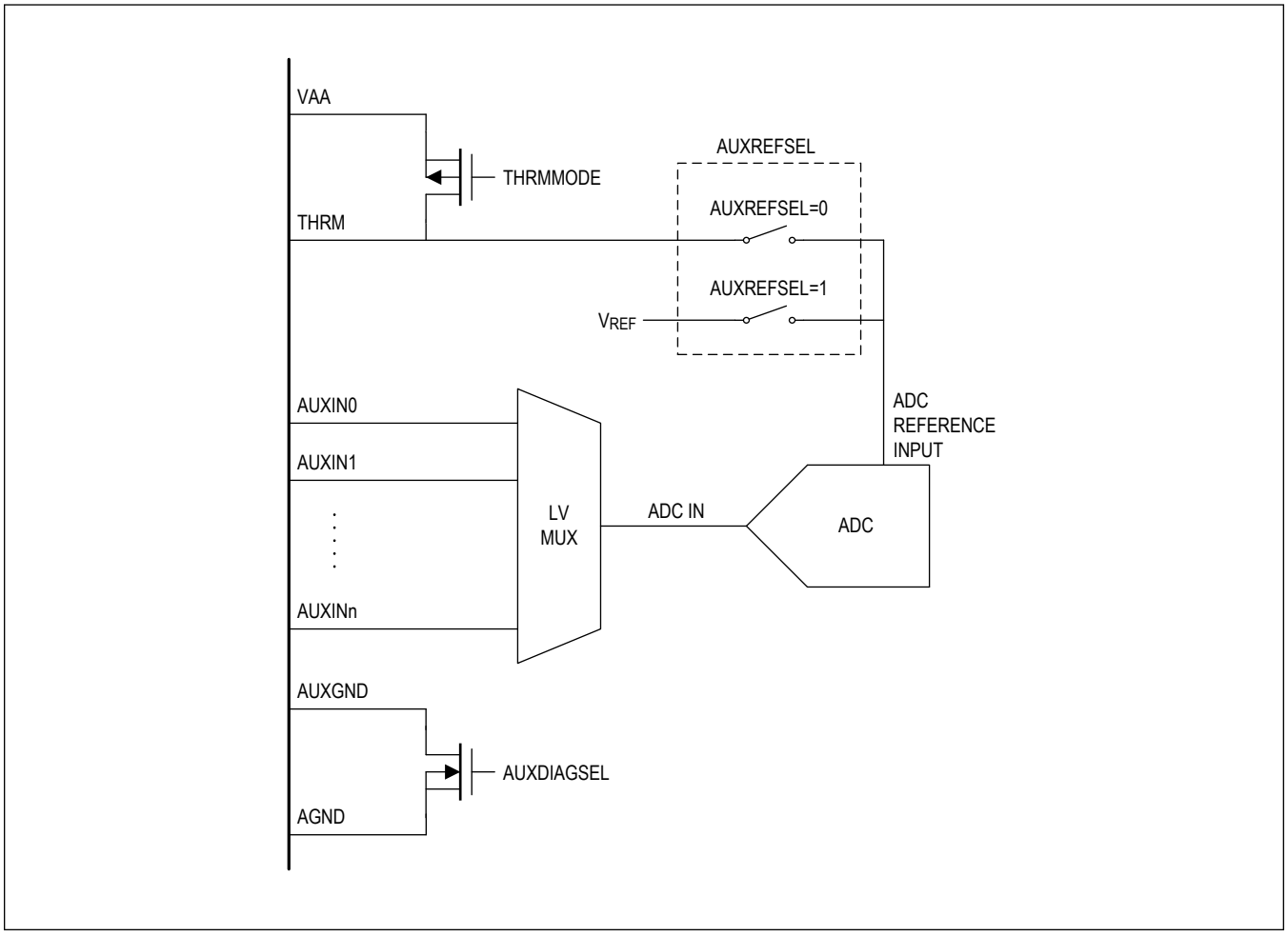


Figure 10. Auxiliary-Temperature Measurements

Table 4. THRM Output

MODE	THRMMODE	DESCRIPTION
Automatic	00b	THRM outputs V_{AA} (dynamically enabled at the beginning of the acquisition and disabled at the end of the acquisition)
	01b	
Manual	10b	THRM output disabled (static)
	11b	THRM outputs V_{AA} (static)

Depending on the external temperature network, there may be insufficient settling time to provide accurate measurements. To support the flexibility for different networks, the AUXTIME bits in the AUXTIMEREG register may be configured to impose a fixed delay of 0ms to 6.14ms prior to the first AUXINn measurement. For an acquisition with non-deterministic scan rates, the AUXTIME will be allowed to settle through the cell, block, and diagnostic measurement intervals of the first scan. However, for acquisitions requiring deterministic timing, such as 50Hz/100Hz rejection and 60Hz/120Hz rejection, the AUXTIME will be applied prior to the beginning of the acquisiton. Refer to the Oversampling section for further details on FOSR and deterministic acquisitions.

Table 5. AUXTIME

AUXTIME[9:0]	ADDITIONAL SETTLING TIME PER ENABLED AUXILIARY CHANNEL = (AUXTIME x 6µs)
0x000	0µs
0x001	6µs
0x002	12µs
…	…
0x3FF	6138 µs

The auxiliary measurements are oversampled to 14-bit values using the OVSAMPL bits in the SCANCTRL register and the output of each auxiliary measurement is stored in the corresponding AUX0 to AUX4 registers. Please refer to the Oversampling section and ADC, Comparator, and ADC+COMP Acquisitions sections for further details.

Ratiometric Auxiliary Input Range

Temperature measurement are converted ratio-metrically to eliminate error due to the biasing of the NTC network. Thus, the conversion range is proportional to the VTHRM (VAA) reference as shown below.

Both ADC and Comparator conversions use the same reference during the conversion and thus have the same input range. However the resolution for both will differ in accordance with the Table 6 and Table 7

Table 6. Auxiliary Temperature Input Range: ADC

AUXILIARY INPUT VOLTAGE	AUXn (14 BITS)		AUXnREG[15:0] (16 BITS)
Ratiometric mode	Hexadecimal	Decimal	
0V	0000h	0d	0000h
$V_{AA}/2$	2000h	8192d	8000h
V_{AA}	3FFFh	16383d	FFFCh

Table 7. Auxiliary Temperature Input Range: Comparator

AUXILIARY INPUT VOLTAGE	COMPOVTH, COMPUVTH, COMPAUXROVTH, COMPAUXRUVTH COMPAUXAOTH,COMPAUXAUVTH (10 BOTS)		COMPOVTHREG[15:0], COMPUVTHREG[15:0] COMPAUXROVTHREG[15:0], COMPAUXRUVTHREG[15:0] COMPAUXAOTHREG[15:0], OMPAUXAUVTHREG[15:0] (16 BITS)
Ratiometric mode	Hexadecimal	Decimal	
0V	000h	0d	0000h
$V_{AA}/2$	200h	512d	8000h
V_{AA}	3FFh	1024d	FFC0h

Computing Temperature

As shown in Figure 9, $V_{AUXINn} = V_{THRM} \times R_{TH} / (10k\Omega + R_{TH})$. This measurement is stored in the AUXn register. The thermistor resistance can then be solved for as follows:

$$R_{TH} = (V_{AUXINn} \times 10k\Omega) / (V_{THRM} - V_{AUXINn}) \text{ where } V_{THRM} = 3.3V \text{ nominally}$$

The resistance of an NTC thermistor increases as the temperature decreases and is typically specified by its resistance R_0 = 10kΩ at T_0 = 25°C = 298.15K and a material constant β (3400K typical). To the first order, the resistance R_{TH} at a temperature T in Kelvin may be computed as follows:

$$R_{TH} = R_0 e^{(\beta(\frac{1}{T} - \frac{1}{T_0}))}$$

The temperature T of the thermistor (in °C) can then be calculated as follows:

$$T\ (in\ °C) = (\beta\ /\ (\ ln(R_{TH}\ /\ 10k\Omega) + (\beta\ /\ 298.15K)) - 273.15K$$

Auxiliary Inputs: Absolute Voltage Measurements

Individual auxiliary ports can be configured to measure absolute voltages through enabling auxiliary measurements using the AUXEN bits in the MEASUREEN2 register as well as configuring the conversion voltage as absolute using the AUXREFSEL bits in the AUXREFCTRL register.

The absolute configuration selects the conversion voltage of both the ADC and Comparator to V_{REF}. An external voltage may be accurately measured as long as the voltage remains below V_{REF}. If higher voltages are required to be measured, a resistive divider must be used to ensure that the maximum auxiliary input does not exceed V_{REF} otherwise the voltage measurement will saturate to full scale. Additionally the user should take precautions that in the case of a single point failure on the external network the maximum auxiliary input doesn't exceed the absolute maximum rating on the port.

If all AUXREFSEL bits are set to 0b1 (Using V_{REF} for the ADC reference) it is recommended that THRMMODE be set to 0b10 (THRM switch always OFF).

Absolute Auxiliary Input Range

Absolute voltage measurement are converted using a fixed precision reference, V_{REF}. All voltages must meet the input range requirements. Otherwise the digital output will saturate resulting in a loss of resolution. Both ADC and Comparator conversions use the the same reference during the conversion but have different resolutions as shown in the Table 8 and Table 9 below

Table 8. Auxiliary Voltage Input Range: ADC

AUXILIARY-INPUT VOLTAGE	AUXn (14 BITS)		AUXnREG[15:0] (16 BITS)
Absolute mode	Hexadecimal	Decimal	
0V	0000h	0d	0000h
$V_{REF}/2$	2000h	8192d	8000h
V_{REF}	3FFFh	16383d	FFFCh

Table 9. Auxiliary Voltage Input Range: Comparator

AUXILIARY-INPUT VOLTAGE	COMPOVTH, COMPUVTH, COMPAUXROVTH, COMPAUXRUVTH COMPAUXAOTH,COMPAUXAUVTH (10 BITS)		COMPOVTHREG[15:0], COMPUVTHREG[15:0] COMPAUXROVTHREG[15:0], COMPAUXRUVTHREG[15:0] COMPAUXAOTHREG[15:0], COMPAUXAUVTHREG[15:0] (16 BITS)
Absolute mode	Hexadecimal	Decimal	
0V	000h	0d	0000h
$V_{REF}/2$	200h	512d	8000h
V_{REF}	3FFh	1024d	FFC0h

Auxiliary Inputs: Mixed Mode Measurements

Ratio-metric measurements and Absolute voltage measurements can both be performed during the same acquisition. Each measurement type will have individual OV and UV alerts threshold settings as described in the Measurement Alerts section.

Note: Auxiliary mixed mode measurement data for the ADC is output to the AUXn registers. The appropriate conversion as determined by the AUXREFSEL configuration must be applied to obtain correct voltage reading.

Ratio-metric Voltage Conversion

V_{AUXn} = AUXn[14:0] x V_{AA} / 16384d = AUXn[14:0] x 201.42µV, or alternatively AUXnREG[15:2] x 201.42µV

where V_{AA} is nominally 3.3V

Absolute Voltage Conversion

V_{AUXn} = AUXn[14:0] x V_{REF} / 16384d = AUXn[14:0] x 140.81µV, or alternatively AUXnREG[15:2] x 140.81µV

Auxiliary Input Protection

The Voltage on the AUXIN0 to AUXIN4 pins should never exceed V_{AA} when configured as an auxiliary input. If this condition does occur, the affected input will self-protect, becoming an open circuit. The associated ALRTAUXPRTCT bit will be set, indicating the overvoltage condition. To retry AUX operation and clear the fault condition, the user must re-write the desired configuration to the AUXGPIOCFG register.

All 4 ALRTAUXPRTCT bits will be logically OR'd together to form the ALRTAUXPRTCTSUM bit in the FMEA2 register.

GPIO Configuration

Any of the 4 auxiliary ports may be configured as a General Purpose Input/Output (GPIO) using the GPIOEN bits in the AUXGPIOCFG register. When a GPIOEN bit is high, the corresponding auxiliary port is configured as a GPIO regardless of the AUXEN configuration. When a GPIOEN bit is low, the corresponding GPIO portion is tri-stated.

Additionally, the AUXIN[1:0] pins can be configured as an I^2C master interface using the I2CEN bit in the AUXGPIOCFG register. When the I2CEN bit is high, AUXIN0 will operate as the SDA pin and AUXIN1 will operate as the SCL pin. By default, I2CEN is low and the I^2C master is disabled.

Table 10. GPIO/I2C/Auxiliary Enable Priority

I2CEN	GPIOEN	FUNCTION
0	0	Auxiliary Input
0	1	GPIO
1	x	AUXIN0 = SDA AUXIN1 = SCL

In the GPIO configuration, the I/O status is determined by the GPIODIR bits of the AUXGPIOCFG register. When a GPIODIR bit is programmed to 0b0, the corresponding port is configured as a digital input. The digital input has a 2MΩ pulldown resistance to ensure the input does not float and cause excessive power dissipation. When the GPIODIR bit is programmed to 0b1, the pin is configured as a digital output. Each GPIO port that is configured as a digital output can be configured to drive a logic-high level or logic-low level determined by the assignment in the GPIODRV bits of the GPIOCFG.

If I^2C functionality is enabled, the AUX0 and AUX1 registers will read 0x0000 and the GPIODIR[1:0], GPIOEN[1:0], and GPIODRV[1:0] bits will be ignored for functionality, but will still read back the user setting.

The GPIORD bits in the GPIOCFG register monitors the pin logic level regardless of whether the port is defined as an input or an output. If a pin is configured as an auxiliary input, the corresponding GPIORD bit will read back 0b0. If the I^2C functionality is enabled, GPIORD[1:0] will read back 0b00.

Table 11. GPIO Configuration

GPIOEN	GPIODIR	FUNCTION
0	x	Auxiliary Input
1	0	Digital Input
1	1	Digital Output

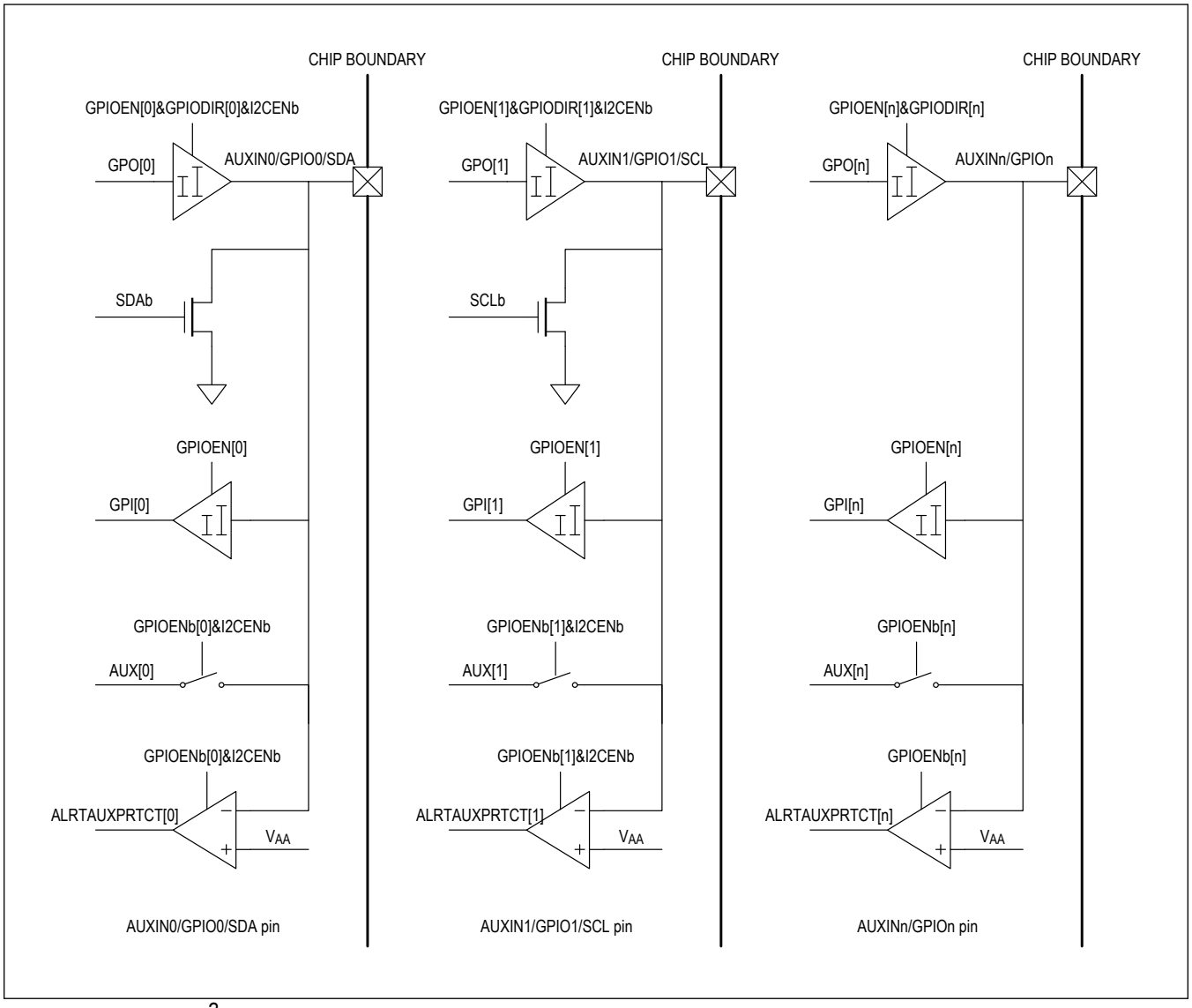


Figure 11. AUX/GPIO/I²C Pin Connections

Current Input

The CSAP and CSAN inputs measure the differential voltage across an external precision current shunt resistor to provide an accurate current measurement. Typical values used for the shunt resistor are 100µΩ and 50µΩ. However, the application may determine if other shunt resistor values are more appropriate to maximize the dynamic range of the ADC without saturating the digital output. If the peak shunt voltage exceeds the input voltage range for the ADC with the applied gain, then the ADC measurements will saturate.

Note that the AGND port should be connected to the CSAP port, allowing the CSAN port to go above or below AGND, depending on the direction of current flow (subject to the ±300mV specification limit). Also note that the current-sense resistor (R_{SHUNT}) lies outside of the Pack as defined and measured in VBLOCK acquisitions, and as such, the voltage drop across the resistor is excluded from the Pack voltage summation provided in the TOTAL register.

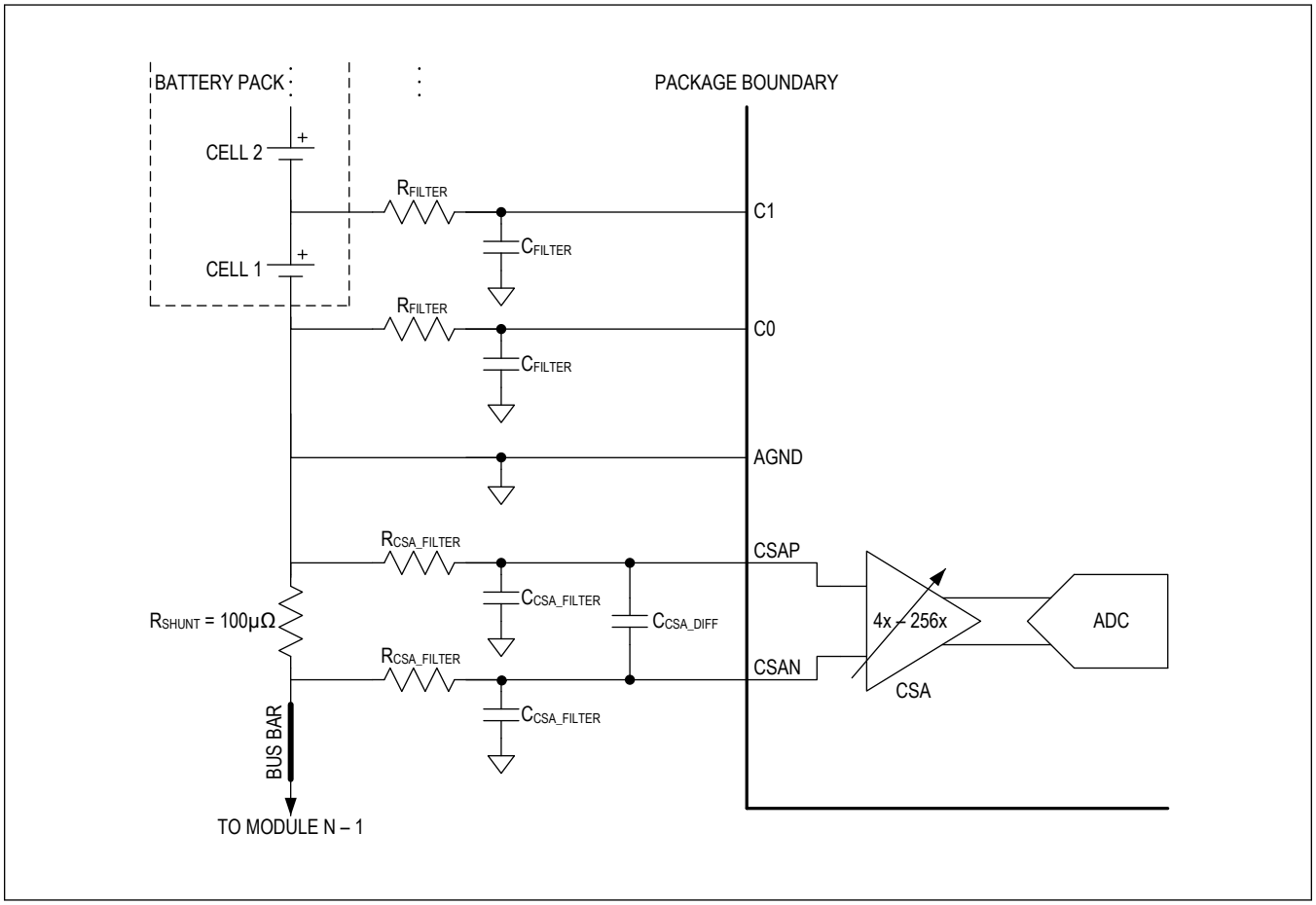


Figure 12. Current Measurement Configuration

To provide the ability to sense finer current resolutions, the current-shunt voltage is input to a current-sense amplifier (CSA), which scales this voltage to the full-scale voltage of the ADC. Seven programmable gain settings ranging from 4x to 256x are configured using the CSAGAIN bits in the ACQCFG register. Assuming a 100µΩ shunt resistor, this corresponds to a maximum current range of ±2880A (CSAGAIN = 0b000 for a gain of 4x) and a minimum current range of ±45A (CSAGAIN = 0b110 for a gain of 256x).

Table 12. Current Sense Amplifier Gain Setting

INPUT VOLTAGE RANGE	CURRENT RANGE (100µΩ SHUNT)	CSA GAIN	CSAGAIN[2]	CSAGAIN[1]	CSAGAIN[0]
±288mV	±2880A	4	0	0	0
±144mV	±1440A	8	0	0	1
±72mV	±720A	16	0	1	0
±36mV	±360A	32	0	1	1
±18mV	±180A	64	1	0	0
±9mV	±90A	128	1	0	1
±4.5mV	±45A	256	1	1	x

The following equation describes how the current shunt resistor can be optimized for the end application:

$R_{SHUNT} = V_{REF} / (2 \times I_{PEAK} \times A_{CSA})$

V_{REF} is the ADC reference voltage of 2.307V

I_{PEAK} is the maximum current achieved in the application

A_{CSA} is the minimum CSA gain setting (typically 4x)

Current-Sense Amplifier Settling

The current-sense amplifier acquisition time will be dependent upon the selected gain setting as shown in the Pyramid Mode ADC Acquisition Time and Ramp Mode ADC Acquisition Time sections.

To optimize the impact that the CSA has on the total acquisition time, the CSA current measurement and the cell voltage measurements will begin once the acquisition is started. If the cumulative cell voltage acquisition time is larger than the CSA acquisition time, then the CSA measurement will occur within 5.8µs. Otherwise, the effective CSA acquisition time will be reduced by the time of the requested voltage measurements. Only in the event that no cell voltage measurements are performed will the scan time be equivalent to the time listed for the CSA.

ADC Acquisition: Current Measurements

The current-sense amplifier (CSA) provides battery-pack current measurements while enabled (CSAEN = 1). These are stored in the CSA register as 14-bit values. The current measurement is initiated at the start of the scan in parallel with the voltage measurement to allow for optimization of the acquisition time during the required CSA settling time. However, the measurement conversion will start after the cell voltage measurements, as described in the ADC Acquisition section (Figure 23 through Figure 28).

Figure 13 shows an example of timing with only the VBLK portion of the cell measurements enabled. In this case, the CSA settling begins in parallel with the VBLK measurement, and the CSA measurement conversion takes place after the completion of the CSA settling time.

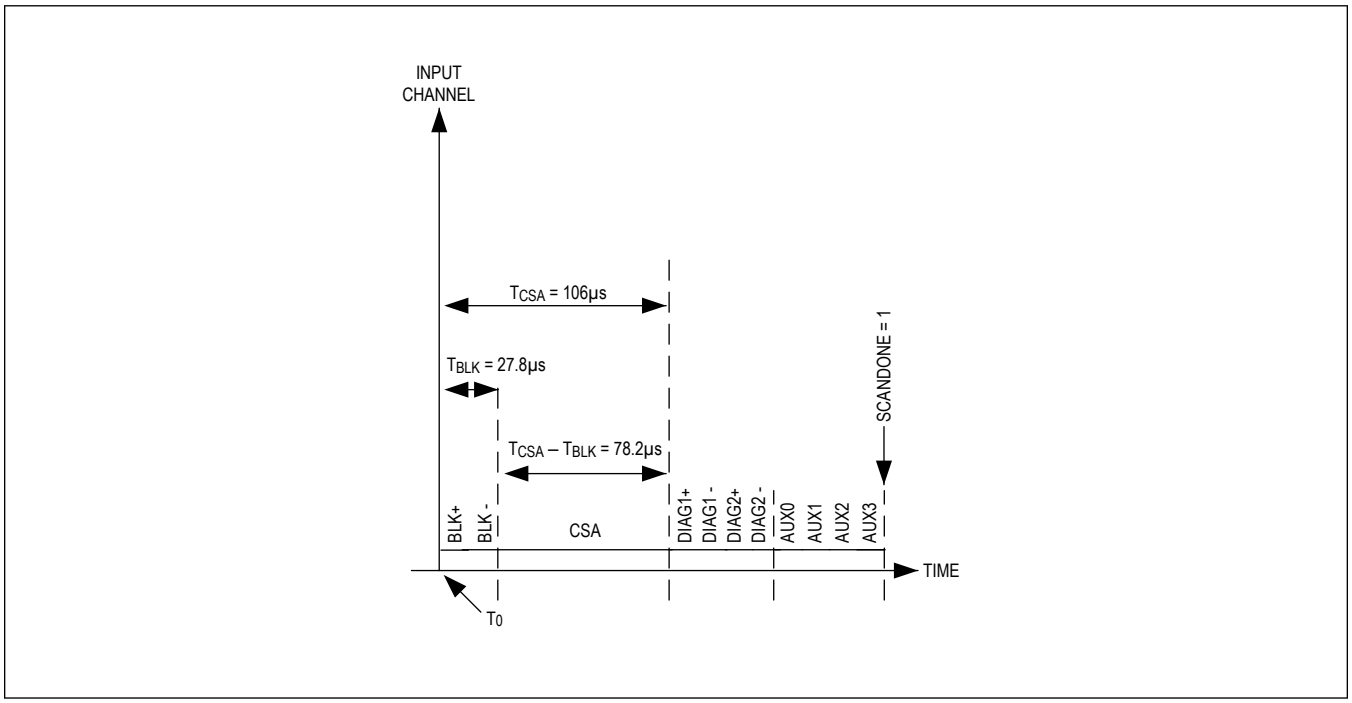


Figure 13. CSA Acquisition Timing Example, VBLK and CSA, CSAGAIN = 0b110 (256 V/V)

Note: Given the bidirectional nature of the battery current during charging and discharging operations, the ADC will only

be configured for bipolar conversions for CSA measurements.

Current and Voltage Measurement Alignment

Due to its concurrent settling, the CSA measurement is aligned in time with cell voltage measurements. For a typical acquisition of 14 cells in Pyramid Mode with CSAEN = 1, the time between the CSA measurement and the last voltage measurement is 5.8µs.

Operational Modes

There are three different operational modes supported: shutdown mode, standby mode, and acquisition mode. Shutdown mode is controlled by the applied voltage on the SHDNL pin. When the applied voltage is below V_{IL_SHDNL}, the device is in an ultra-low-power shutdown mode, and the various elements of the internal circuitry are disabled. If the voltage is above V_{IH_SHDNL}, the device is in standby mode and will act upon qualified interface commands. The device will remain in standby mode until the user commands an acquisition, at which point the device transitions into acquisition mode until completed as signaled by the SCANDONE. Alternatively, the transition from sleep mode to acquisition mode will be handled independent of user interaction only when long-term autonomous cell balancing with voltage measurements are enabled (refer to the *Cell Balancing* description for further information).

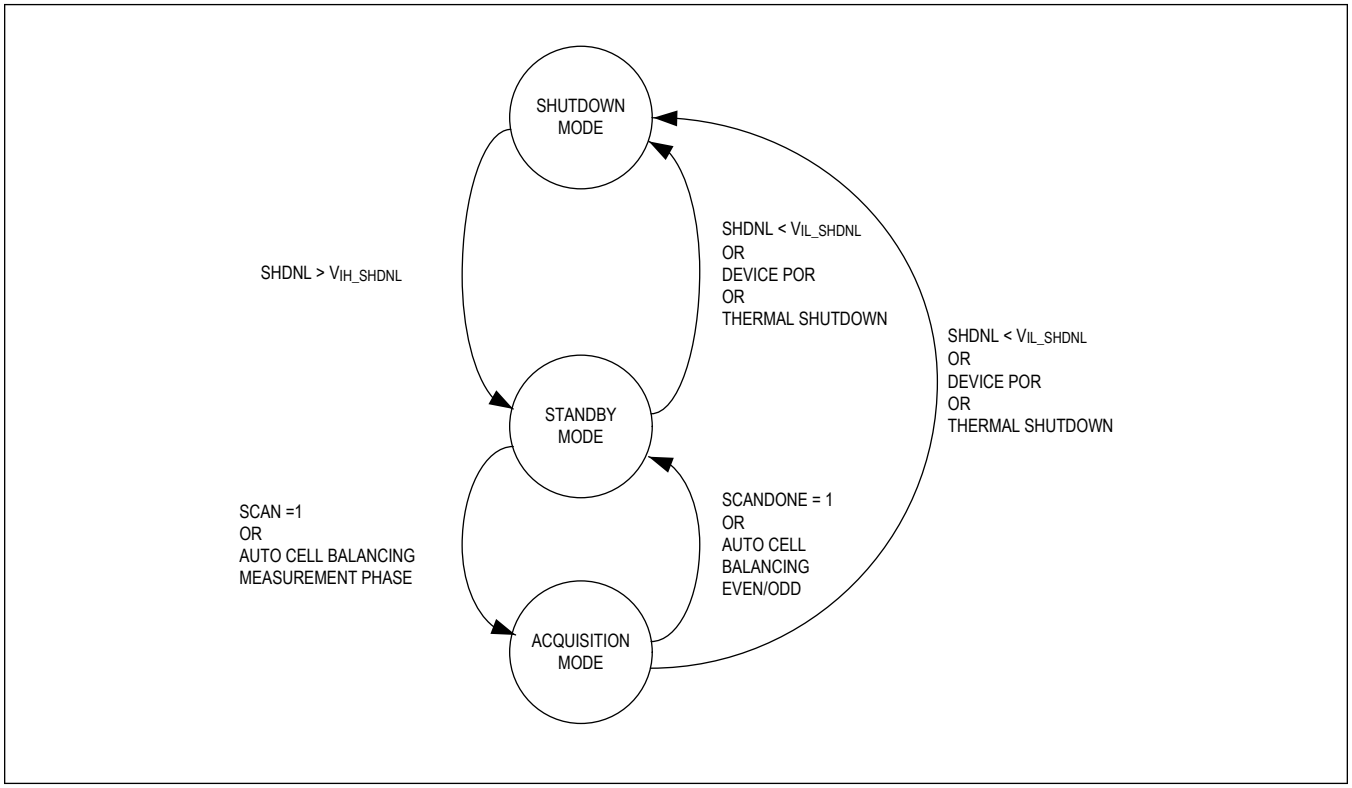


Figure 14. Operational Mode State Diagram

The following sections further detail the operational modes and device interactions.

Power-On (Standby Mode)

The configuration of the communication interface, as defined by the UARTSEL pin, determine the appropriate method to transition the device from shutdown mode into standby mode.

When configured as a differential UART interface (UARTSEL > V_{IH}), the SHNDL input may be driven externally above

V_{IH_SHDNL} threshold or it may be driven using internal charge pumps on the UART RXLP/RXLN and RXUP/RXUN inputs. If the SHDNL pin has no external connection to a host controller, the device must rely on the UART interface to drive the external network on the SHDNL pin. The recommended configuration with a 1nF capacitor will allow the device to drive the SHDNL pin above V_{IH_SHDNL} in 200µs. The charge pump self-regulates to $V_{SHDNLIMIT}$ and can maintain V_{SHDNL} at a logic one even with the UART idle 98% of the time. The internal charge pump operation requires a differential signal UART signal.

Note: When configured as a single-ended UART interface, the SHDNL pin must be driven by an external connection to a host controller. The power-on of the device will then be controlled by the host driving the SHDNL pin above V_{IH_SHDNL} threshold.

When configured as a SPI interface selection (UARTSEL < V_{IL}), the SHDNL input must be driven externally as done with the single-ended UART configuration. It is recommend that the unused RXLP/RXLN and RXUP/RXUN inputs should be pulled low to ensure that the charge pump remains inactive and does not inadvertently contend with the external driver.

Once the V_{IH_SHDNL} threshold is reached, the LDO output is enabled and V_{AA} output voltage will begin to rise. At 3V (typical), the POR signal is de-asserted, the oscillators are enabled, and the HV charge pump is enabled. Once the HV charge-pump is stable, the logic is enabled and the ALRTRST status bit is set. The device is fully operational (standby mode) within 1ms from the time communication is first received in the shutdown mode. Figure 15 details the power-on state transition.

Shutdown-to-Standby State Diagram

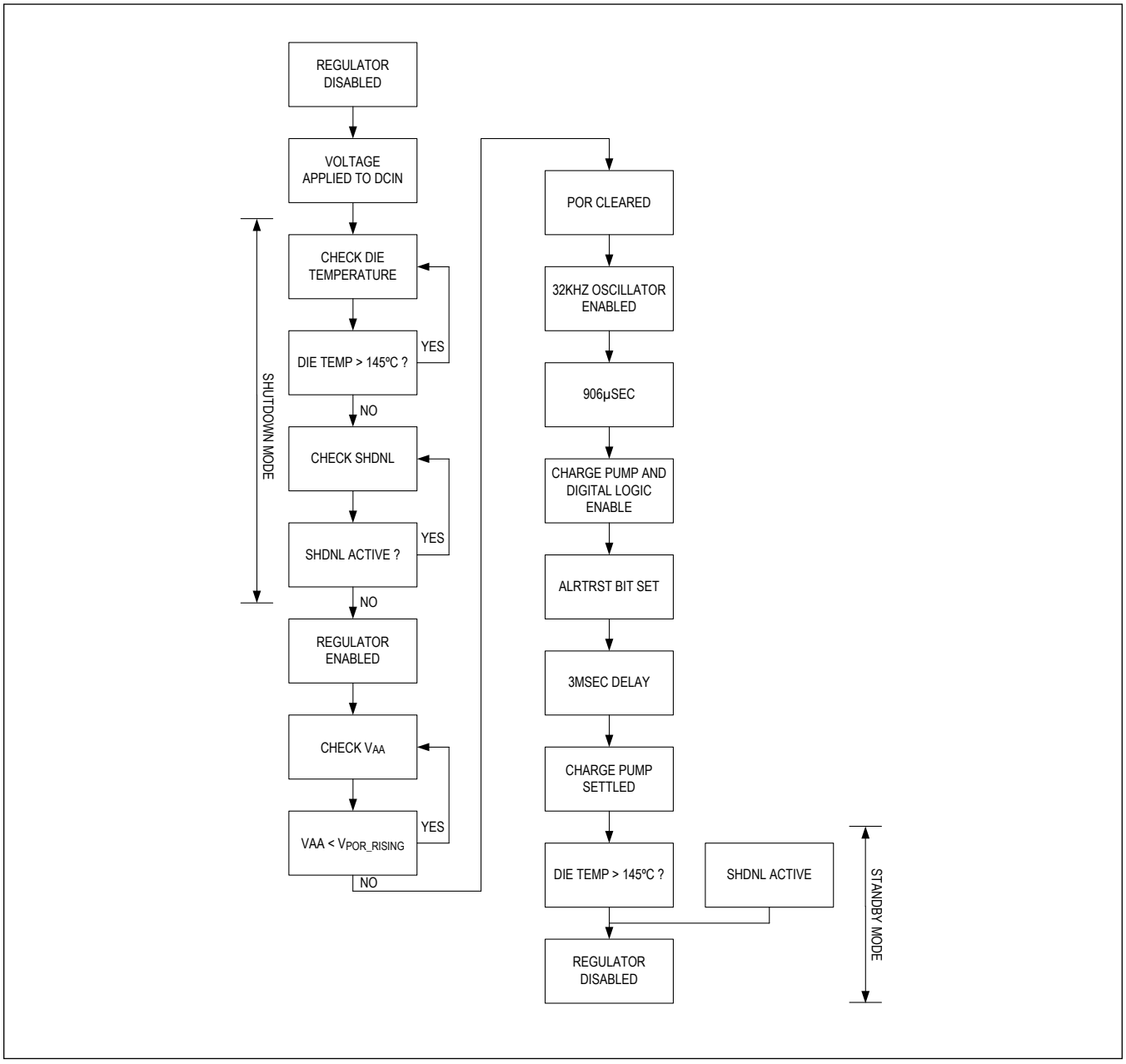


Figure 15. Power-On Sequence

Shutdown Mode

The device enters shutdown mode when SHDNL < V_{IL_SHNDL}. In shutdown, the low-voltage regulator and HV charge pump are disabled as soon as the SHDNL pin goes low. When the V_{AA} and V_{DDL} decoupling capacitors discharge below the POR threshold (2.95V typical), then the device registers are reset. The device is then in an ultra-low-power state until SHDNL is brought high. The control to enter this state is achieved using separate methods depending on the interface configuration, which has be optimized for the end application.

When the device is configured in UART communication (UARTSEL > $V_{IH_UARTSEL}$), shutdown is enabled by externally driving SHDNL low, stopping commanded and keep-alive communication through the differential UART, or commanding a register write to enable the FORCEPOR bit. In the later two conditions, the rate at which shutdown mode is entered is controlled by the time constant associated with the external C_{SHDNL} and the equivalent resistance. Through halting the communication to the device, there is no charge pumping and the capacitor discharges through an internal 10MΩ resistor with a 10ms time constant. If a faster shutdown rate is required, a 200kΩ resistor may be connected externally from SHDNL to AGND to create a 200µs time constant. Alternatively, the FORCEPOR bitfield may be utilized, which enables a 4.7kΩ pulldown to create a 4.7µs time constant.

Table 13. Shutdown Timing

SHUTDOWN METHOD	$R_{PULLDOWN}$		C_{SHDNL}	RC
1. External Controller	N/A	External	1nF	N/A
2. External SHDNL resistance to AGND	4.7kΩ	External		4.7µs
3. Register Configured FORCEPOR	4.7kΩ	Internal		4.7µs
4. Disconnect DCIN	200kΩ	External		200µs
5. Host places UART in idle mode	10MΩ	Internal		10,000 µs

Note: Attention should be paid when deciding on an external pulldown resistor to control the shutdown time, as this resistor will create a voltage-divider with the internal emergency discharge mode pullup resistance and could force the device into shutdown unintentionally when HOLDSHNDL is enabled. It is therefore recommended to use a minimum of 4.7kΩ to avoid any interaction.

If only a register reset is required, the host can issue a soft reset by enabling the SWPOR bitfield. This will reset all non-interface-related device bitfields (UARTCFG, TXUIDLEHIZ, TXLIDLEHIZ, ADAPTTXEN, UARTHOST, SFTYCSB, SFTYSCLK, SFTYSDI, SPIDRVINT,ALERTEN).

When the device is configured for SPI communication (UARTSEL < $V_{IL_UARTSEL}$), the recommended method to enter shutdown is enabled by externally driving SHDNL low. Although, not recommended, if the user plans to utilize the FORCEPOR bitfield, the external driver must have some series limiting resistance in order to ensure that a voltage-divider is created to allow SHDNL to fall below V_{IL_SHNDL}.

Shutdown State Diagram

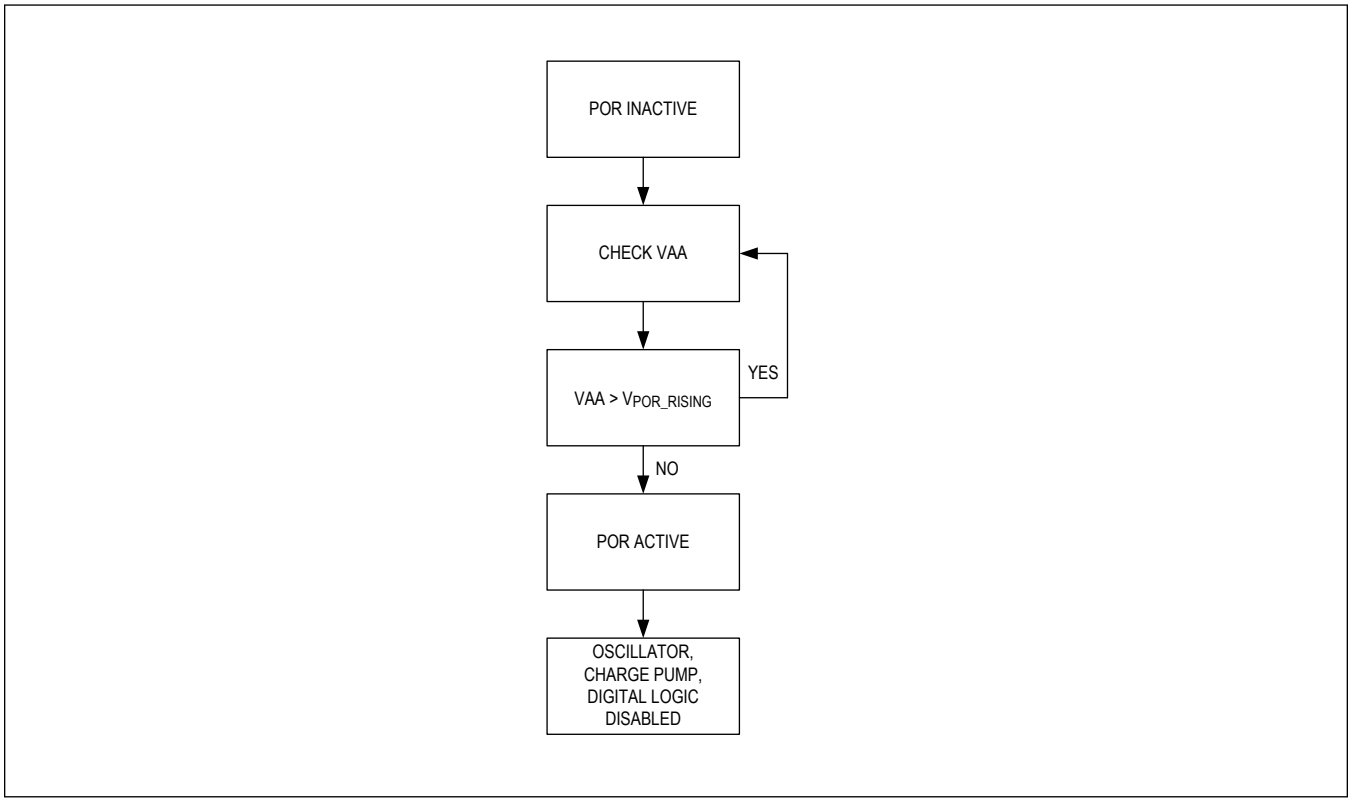


Figure 16. Shutdown Sequence

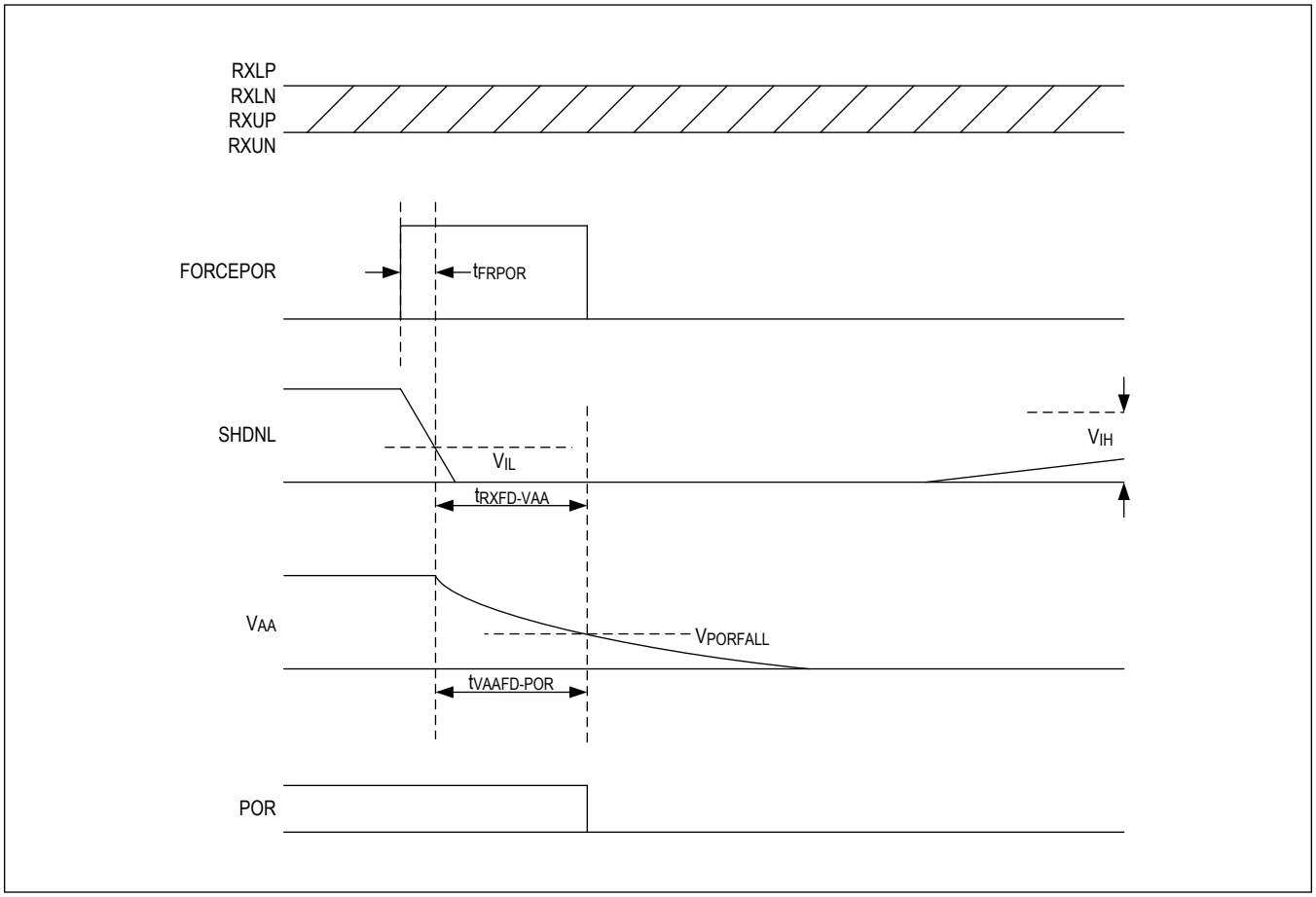


Figure 17. UART Operation (Shutdown Timing)

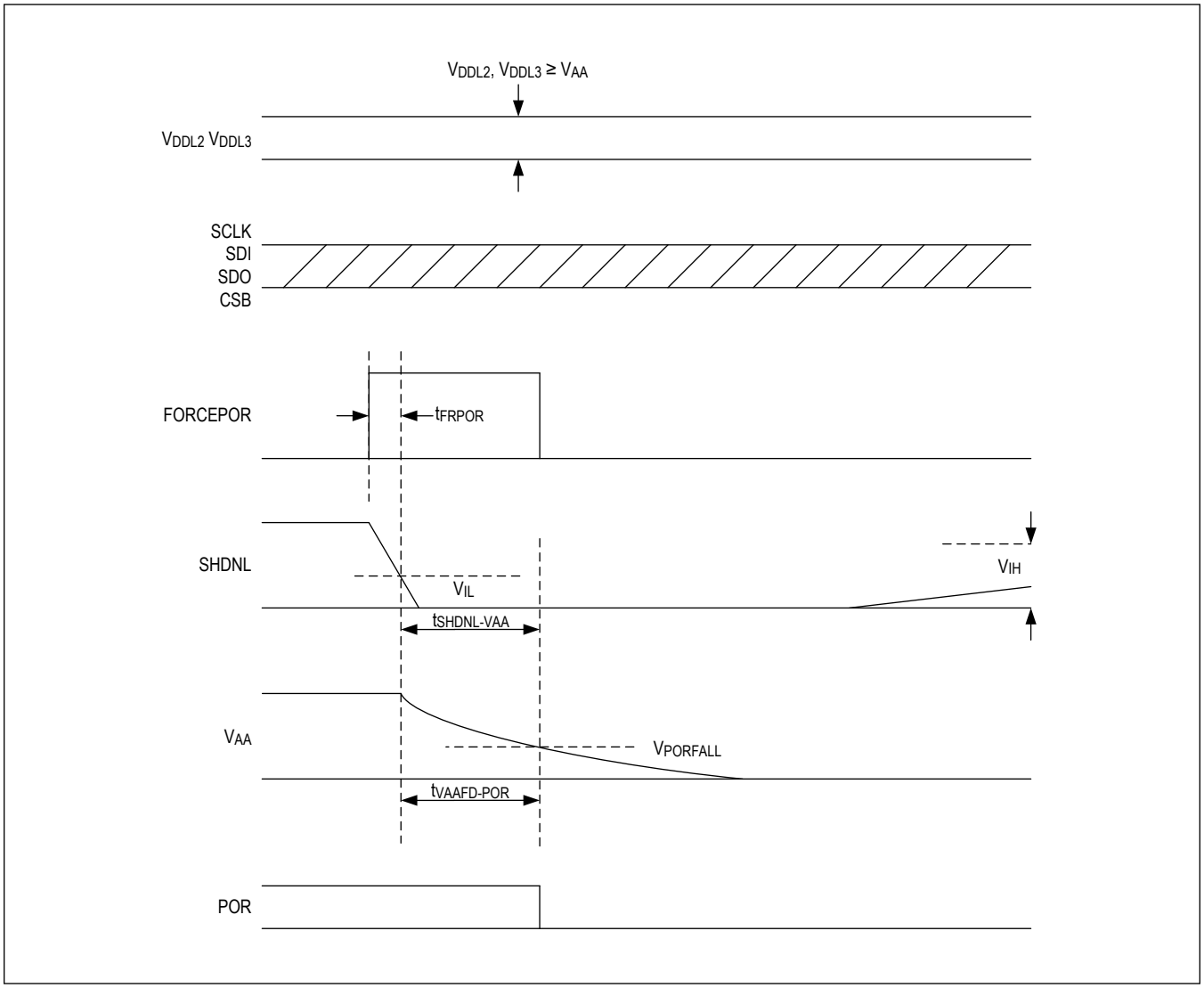


Figure 18. SPI Operation (Shutdown Timing)

Power-On and Shutdown Timing

The following diagrams provide details regarding the power-on control and shutdown timing as well as supply sequencing in a high-voltage daisy-chained system controlled by UART communication, as well as a low-voltage (48V) system with directed control over the SHDNL pin. It is important to note that the UART can also be used in low-voltage systems with single-ended communication as discussed in the Single-Ended RX Mode section. In this case, the directed control of the SHDNL pin will remain the same.

Note: As shown in Figure 21 AND Figure 22 the shutdown may also be controlled by writing the specific FORCEPOR bit. If the SHDNL is actively driven the application circuit should ensure that there is no contention and this is driven below V_{IL_SHDNL}.

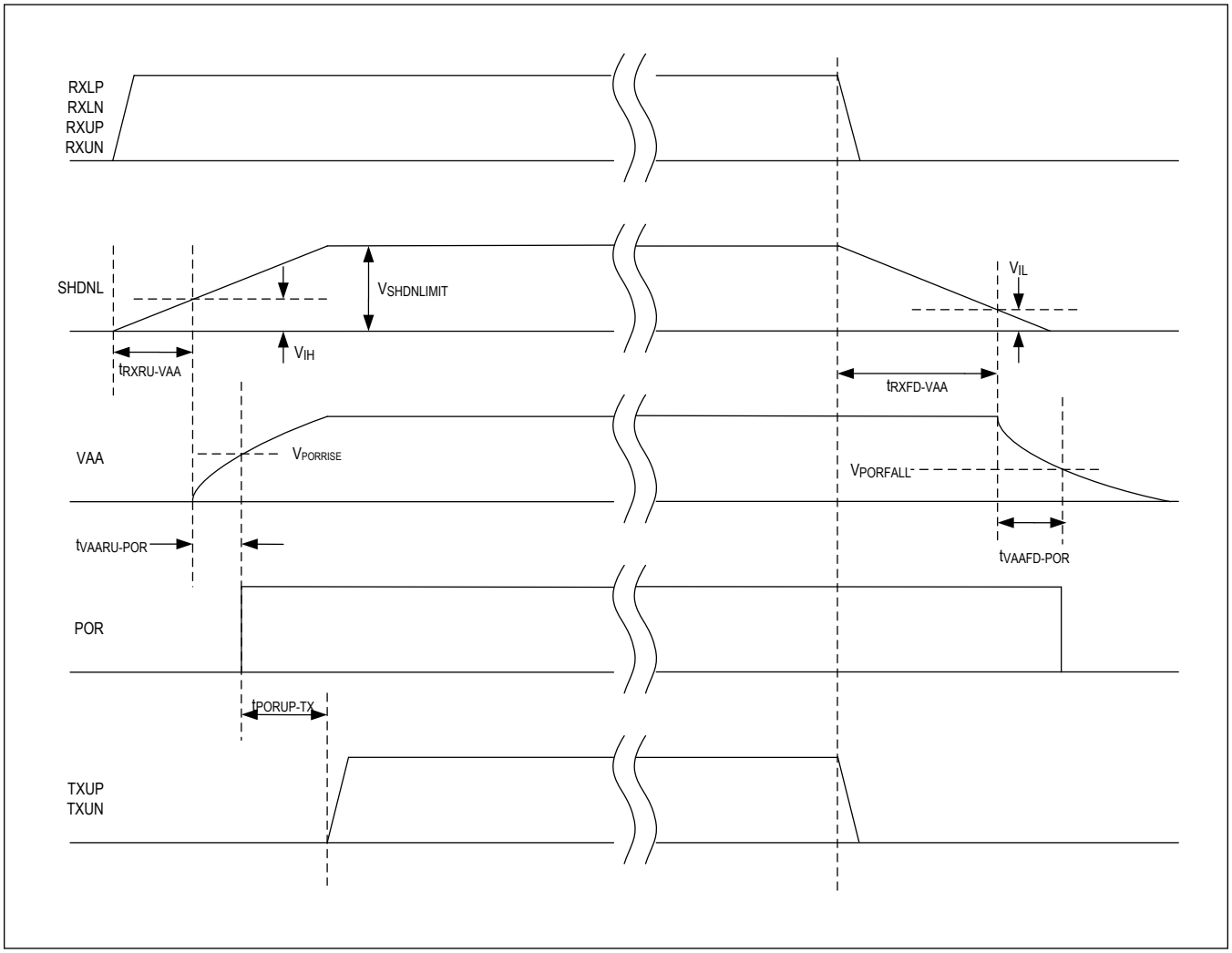


Figure 19. Power-On Timing (UART-Communication Control)

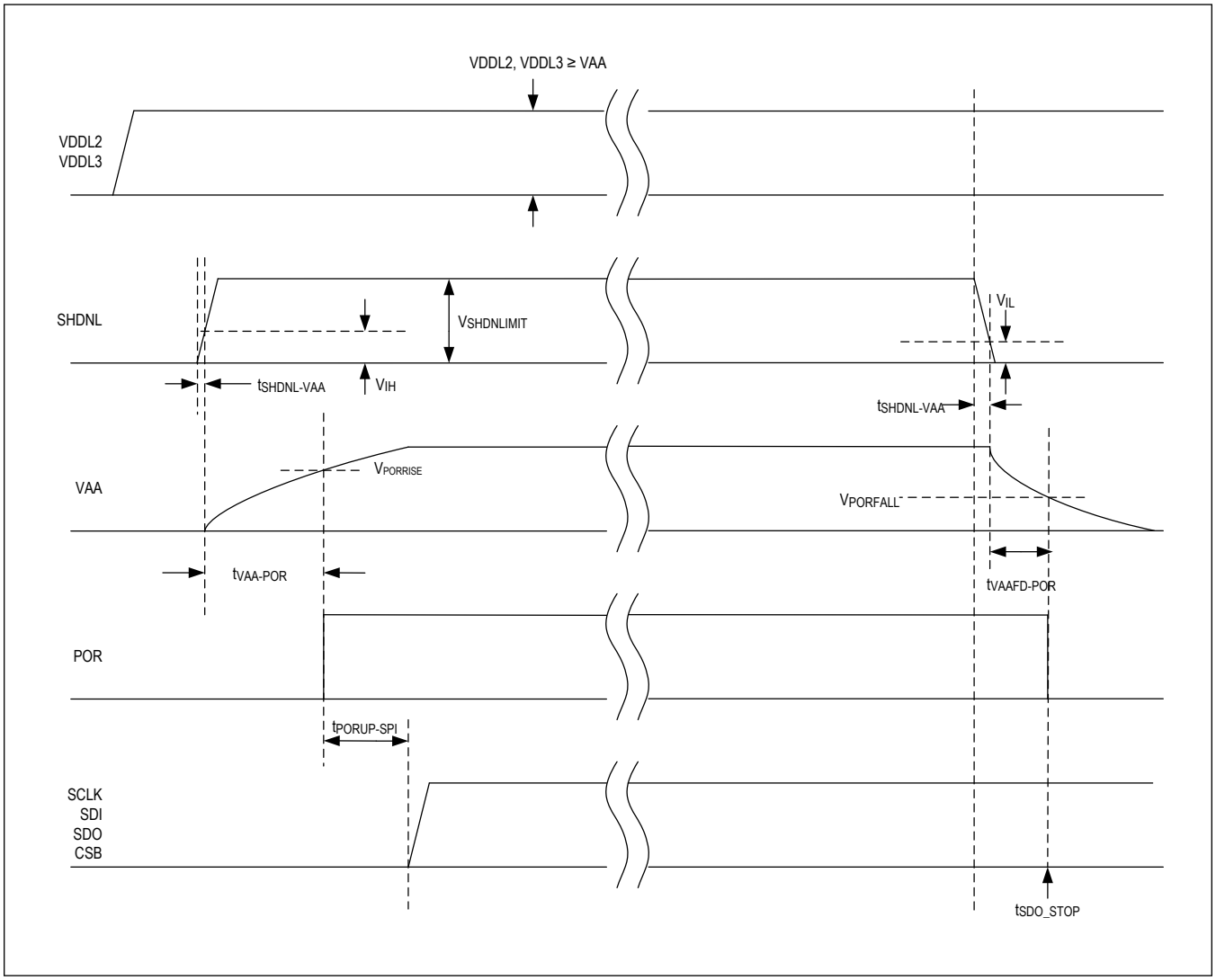


Figure 20. Power-On Timing (SPI Directed Control)

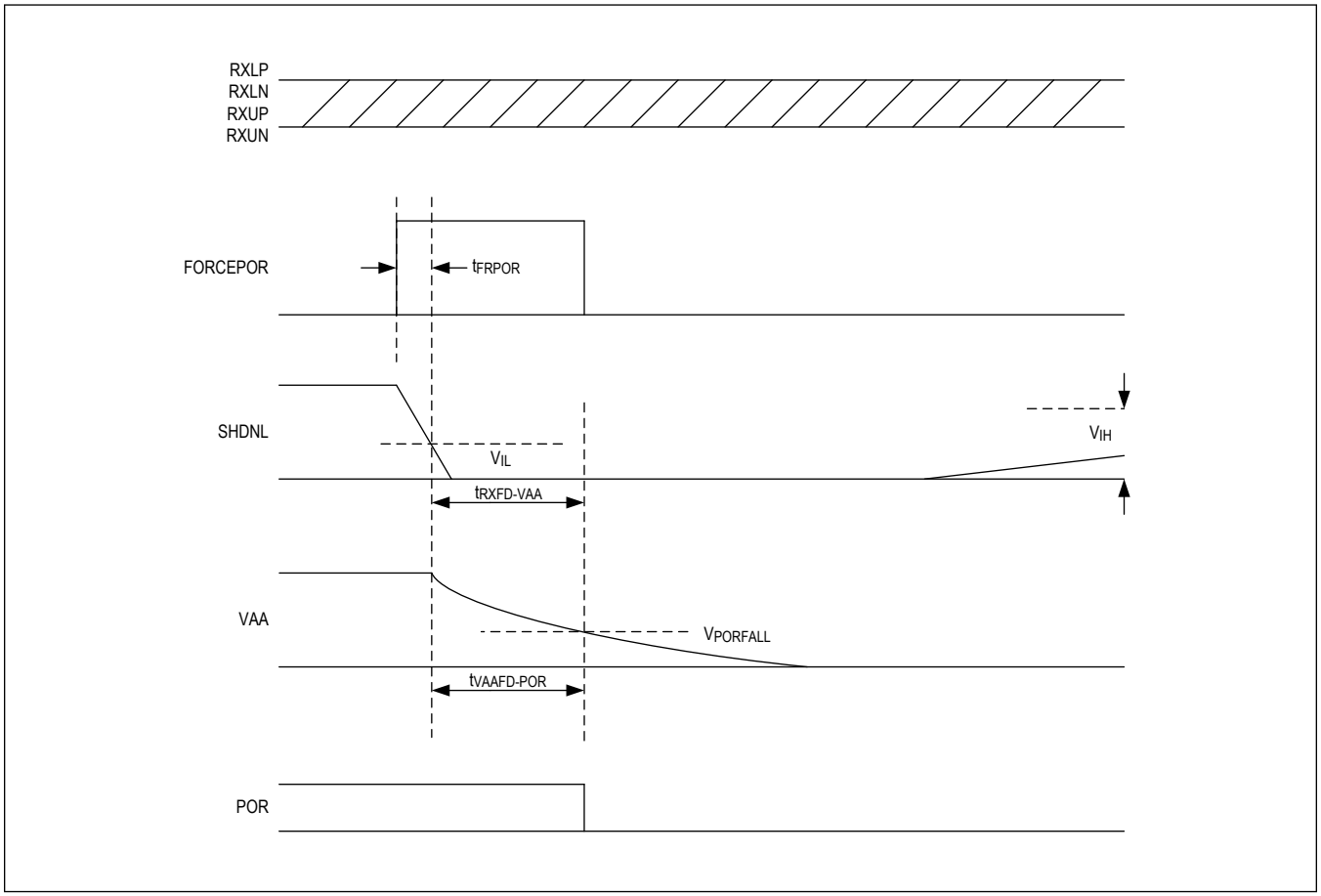


Figure 21. Power-On and Shutdown Timing (UART Control)

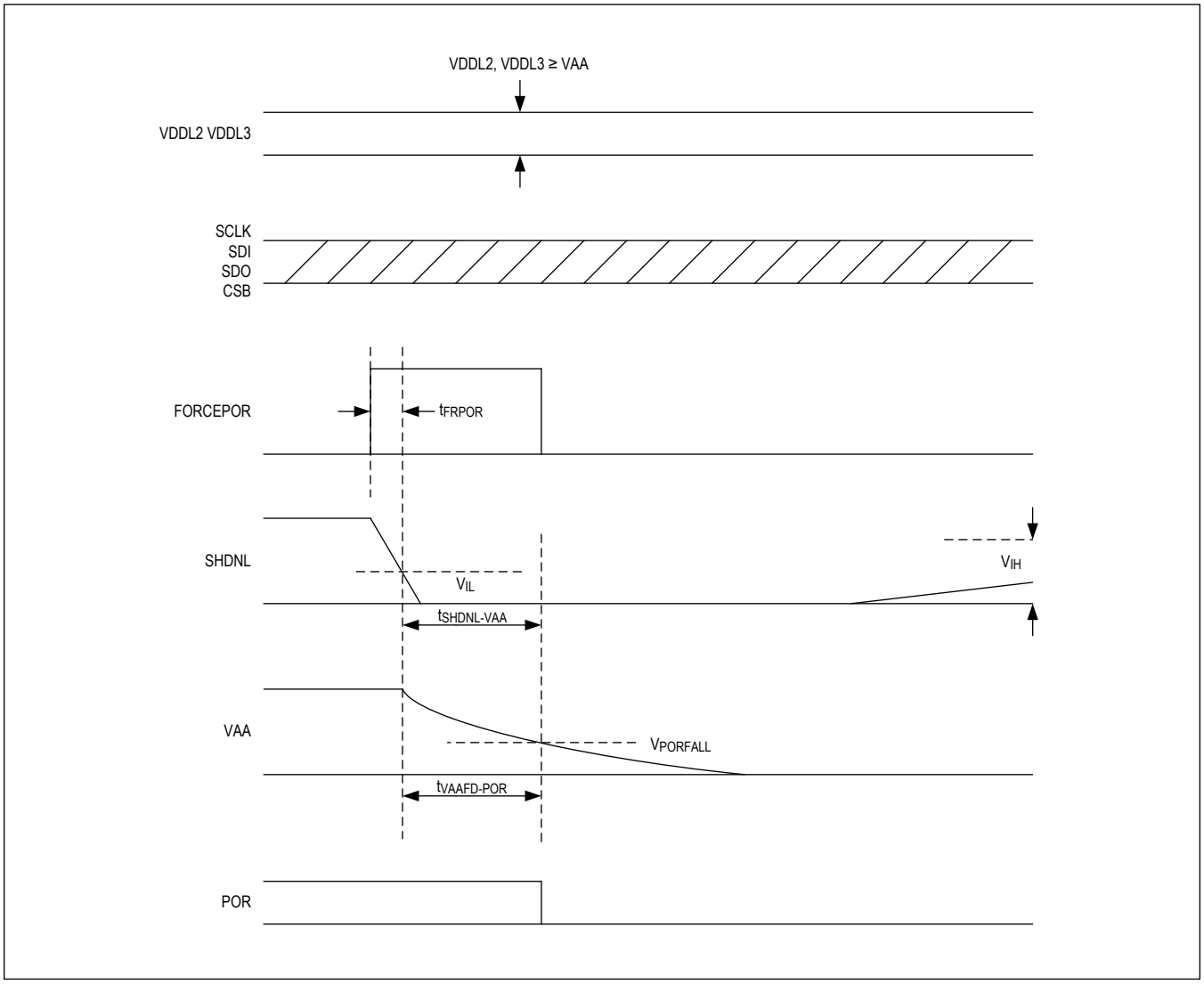


Figure 22. Power-On and Shutdown Timing (SPI Control)

Active Mode

The device will enter acquisition mode upon receiving a SCAN command or during cell-balancing operation with UV threshold detection. The overall time spent in acquisition mode is determined by the settings defined by the SCANCTRL and ACQCFG registers. Once the acquisition is completed (signified by SCANDONE and DATARDY), the device will enter the low-power standby mode operation. If at any point during acquisition mode SHDNL is pulled below V_{IL_SHDNL}, T_{SHDNL} is exceeded, or V_{AA} transitions below the POR threshold, the device will exit acquisition and enter shutdown mode.

Precision Internal Voltage References

The measurement system uses two precision, temperature-compensated voltage references. The references are completely internal to the device and do not require any external components. The primary voltage reference, or REF, is used to derive the linear regulator output voltage and to supply the ADC reference. An alternate, independent reference

(ALTREF) may be used to verify the primary reference voltage as described in the Diagnostics section.

Scan Methods

The MAX17852 has two parallel measurement engines (ADC and Comparator) that are capable of providing three different acquisitions (ADC Acquisition, Comparator Acquisition, and Simultaneous ADC + Comparator Acquisition). The combination of both measurement blocks provides hardware redundancy to accelerate fault detection and ensure added system reliability.

All modes are able to process the cell and auxiliary temperature/auxiliary voltage measurements and each have their own unique alert threshold settings to accelerate the communication of a system fault. Alert settings are described in further detail in the Measurement Alerts section.

ADC Input Range

The ADC supports unipolar and bipolar cell input acquisitions through the configuration settings of the POLARITY[13:0] bits in the POLARITYCTRL register. In the unipolar configuration, the input range is nominally 0V to 5V. In the bipolar configuration, the nominal input range is nominally -2.5V to 2.5V. Through combining the conversion data from the two scan configurations, the input range can effectively be extended from -2.5V to 5V where any bipolar measurements over 2.3V should be supplemented with the unipolar measurements.

The flexibility to support both unipolar and bipolar conversions ensures that both cell measurements, as well as bus-bar measurements, are able to be simultaneously captured within the same acquisition, which will help optimize acquisition time and interface throughput.

Note: Conversions for some diagnostic modes automatically pre-configure the device to use either bipolar or unipolar mode regardless of the POLARITY_n bit value in the POLARITYCTRL register.

The ADC also supports both ratiometric and absolute acquisitions for the auxiliary inputs through the configuration setting of the AUXREFSEL[5:0] bits in the AUXREFCTRL register. Ratiometric acquisitions are primarily used for NTC-based temperature measurements and support an input range of 0V to V_{AA}. Absolute acquisitions can be used for any on supplemental voltage measurement required by the application and supports an input range of 0V to V_{REF}. To ensure the highest accuracy for the application, the appropriate mode should be configured (it is not recommended to perform an ratiometric acquisition for an absolute measurement such as a supply voltage, as the variability in the reference (V_{AA}) can introduce unwanted measurement error).

The auxiliary configuration supports simultaneous acquisition of both absolute and ratiometric measurements to help optimize acquisition time and interface throughput.

Note: In all ADC configurations, reduced linearity may occur near the zero-scale and full-scale limits. Refer to the *Electrical Characteristics* table for device accuracy specification.

Table 14. ADC Input Range

CELL INPUT VOLTAGE		AUX RATIO INPUT VOLTAGE	AUX ABSOLUTE INPUT VOLTAGE	CELLn[15:2] AUXn[15:2] (14 BITS)		CELLn[15:0] AUXn[15:0] (16 BITS)
BIPOLAR MODE	UNIPOLAR MODE			HEXADECIMAL	DECIMAL	
-2.5V	0V	0V	0V	0000h	0d	0000h
0V	2.5V	$V_{AA}/2$	$V_{REF}/2$	2000h	8192d	8000h
2.5V	5V	V_{AA}	V_{REF}	3FFFh	16383d	FFFCh

Comparator Input Range

The comparator supports a unipolar cell input range from 0V to 5V input through the configuration of the POLARITY[13:0] bit in the POLARITYCTRL registers. If the individual POLARITY bit is configured for a bipolar acquisition, the comparator

cell measurement will be omitted from the scan.

The comparator also supports ratiometric and absolute acquisition for the auxiliary input that follows the same configuration as described in the ADC Input Range section. Ratiometric acquisitions support an input range of 0V to V_{AA} and absolute acquisitions supports an input range of 0V to V_{REF}.

Table 15. Comparator Input Range

CELL INPUT VOLTAGE	AUX RATIO INPUT VOLTAGE	AUX ABSOLUTE INPUT VOLTAGE	COMPOVTH, COMPUVTH, COMPAUXROVTH, COMPAUXRUVTH COMPAUXAOTH,COMPAUXAUVTH (10 BITS)		COMPOVTH[15:0], COMPUVTH[15:0], COMPAUXROVTH[15:0], OMPAUXRUVTH[15:0], COMPAUXAOTH[15:0], COMPAUXAUVTH[15:0] (16 BITS)
			HEXADECIMAL	DECIMAL	
0V	0V	0V	000h	0d	0000h
2.5V	$V_{AA}/2$	$V_{REF}/2$	200h	512d	8000h
5V	V_{AA}	V_{REF}	3FFh	1024d	FFC0h

Scan Configuration

The SCANCFG bits in the SCANCTRL register selects the acquisition that is to be performed. All available configurations are listed below.

- ADC Acquisition
- ADC and Comparator (ADC+COMP) Acquisition
- Comparator Acquisition
- Calibration
- Balancing Switch Short
- Balancing Switch Open
- Cell Sense Open Odds
- Cell Sense Open Evens

ADC, Comparator, and ADC+COMP acquisitions have programmable sample intervals through the configuration of the FOSR bit. This setting when coupled with the OVSAMPL allows for specific frequency rejection at either 50Hz/100Hz or 60Hz/120Hz. If not configured, the user may specifically control the sample interval through the timing of the interface to support any desired post processing on the host controller.

Note: The Balance Switch and Cell Sense acquisitions will immediately configure the internal balance switches once the SCANCFG bitfield is written. Please refer to the BALSW Diagnostic Section for details on the operation of this acquisition mode

ADC Configurations and Properties

ADC Polarity Configuration

Unipolar and bipolar measurements are supported within a single scan to capture all cell and bus-bar data without the need to reconfigure multiple scan configuration registers or perform multiple acquisitions. Cell polarity is configured using the POLARITYCTRL register where all cells are defaulted to unipolar measurements (POLARITY [13:0] = 0000h).

Bipolar cells are fault masked during BALSWDIAG ADC Measurement scans. MINMAXPOL determines whether Bipolar cells are included in MIN/MAXCELL and ALRTMSMTCH calculations.

Bipolar cell measurements are checked against BIPOVTH and BIPUVTH thresholds rather than OVTH and UVTH thresholds.

Bipolar cells are not included in Comparator Measurement scans, and ALRTCOMPOV/ALRTCOMPUV alerts are not evaluated.

ADC Scan Properties

ADC acquisitions can be applied to the Cell, Auxiliary, Block, Diagnostics, and CSA measurements.

The Cell measurements can be programmed through the SCANMODE bit in the SCANCTRL register to use two conversion phases (pyramid mode) or a single conversion phase (ramp mode).

For the Cell inputs, Pyramid Mode (SCANMODE = 0) will perform the first conversion phase in ascending cell order (bottom enabled cell to top enabled cell) and the second conversion phase is in descending order (top enabled cell to bottom enabled cell). The two-conversion scan will allow for chopping of the inputs to effectively remove any offsets or reference-induced errors as well as create a virtual sampling time that is the same for all cell measurements.

The Ramp mode (SCANMODE = 0b1) performs a single conversion phase (bottom enabled cell to top enabled cell) which will improve conversion speed, but is susceptible to offset errors in the measurement path. For this reason, to ensure the best possible cell accuracy and the accelerated scan times offered in Ramp mode, the following are recommended:

- Only run Ramp mode with calibration enabled (ADCCALEN = 1) such that the offset may be internally corrected
- Routinely perform On-Demand Calibration cycles (SCANCFG = 0b011) whenever DCIN voltage changes by more than 1V.

The auxiliary measurements do not require a pyramid (dual phase) sampling approach, and are sampled in a single conversion regardless of SCANMODE configuration.

ADC Acquisition

ADC acquisitions can be configured for the Cell, Auxiliary, Block, Diagnostics, and CSA. The acquisition is initiated by writing a logic one to the SCAN bit in the SCANCTRL register. This write acts as a strobe, and the SCAN bit content is automatically cleared, reading back a logic zero if polled. In daisy-chained devices, acquisitions in either UART path (depending on the Master configuration) will be delayed by the propagation delay, t_{PROP}, of the command packet through each device. The acquisition for device is signaled complete when SCANDONE bit is a logic one.

Note: If any additional write to the SCANCFG is issued prior to the SCANDONE bit being cleared, this command will be ignored.

Pyramid Mode Acqusition Sequence

The ADC acquisition process for Pyramid Mode (SCANMODE = 0) is outlined below:

1. Disable HV charge pump
2. VBLK conversion (first phase), if enabled
3. All enabled cell conversions (first phase), if enabled (ascending order 1 through 14)
4. All enabled cell conversions (second phase), if enabled (descending order 14 through 1)
5. VBLK conversion (second phase), if enabled
6. CSA conversion, if enabled
7. DIAG1 conversion (first phase), if enabled
8. DIAG1 conversion (second phase), if enabled
9. DIAG2 conversion (first phase), if enabled
10. DIAG2 conversion (second phase), if enabled
11. Auxiliary conversions, if enabled
12. Enable HV charge pump for recovery period unless OVSAMPL = 000b (no oversampling) or all oversample measurements are complete
13. Repeat steps 1 through 11 until all oversamples are done
14. Set SCANDONE bit

ADC Pyramid Mode Figures

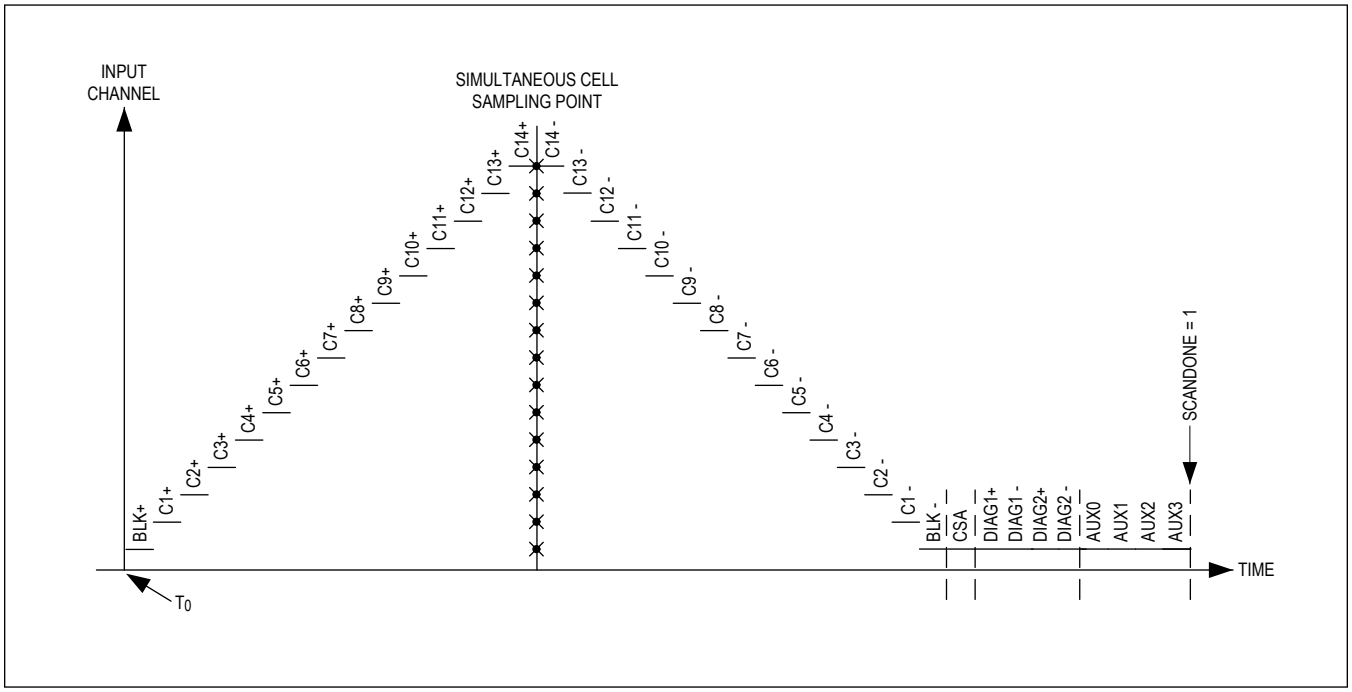


Figure 23. Acquisition - SCANCFG = 0h, SCANMODE = 0, OVSAMPL = 0h, ALTMUXSEL = 0, BLOCKEN = 1, CSAEN = 1, DIAGSEL1 > 0h, DIAGSEL2 > 0h, AUXEN = Fh

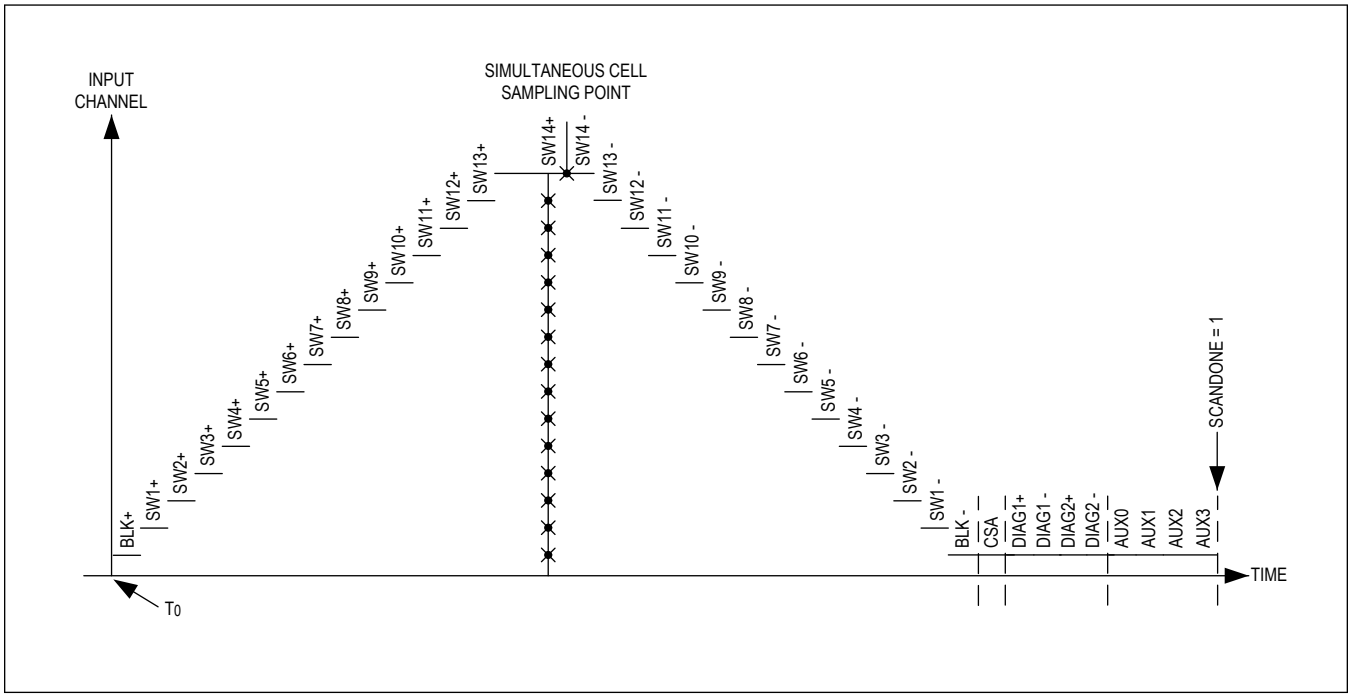


Figure 24. Acquisition - SCANCFG = 0h, SCANMODE = 0, OVSAMPL = 0h, TOPCELL1/2 = 14, ALTMUXSEL = 1, BLOCKEN = 1, CSAEN = 1, DIAGSEL1 > 0h, DIAGSEL2 > 0h, AUXEN = Fh

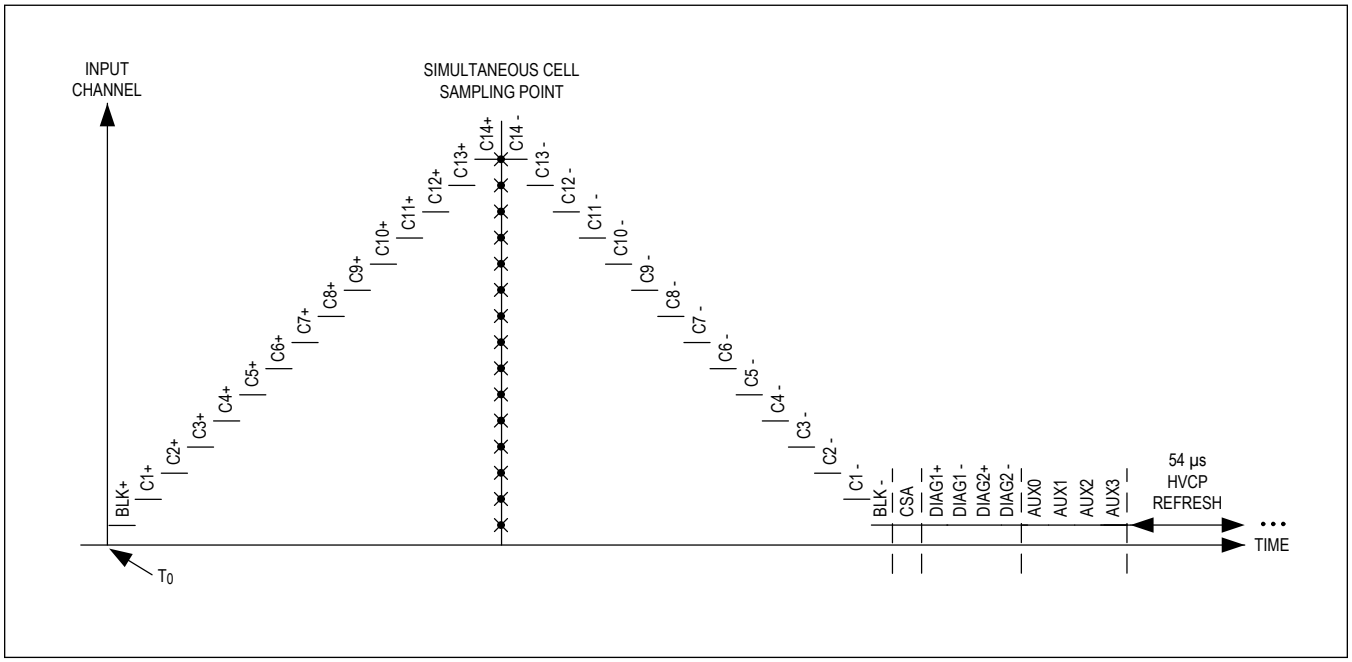


Figure 25. Acquisition - SCANCFG = 0h, SCANMODE = 0, OVSAMPL > 0h, ALTMUXSEL = 0, BLOCKEN = 1, CSAEN = 1, DIAGSEL1 > 0h, DIAGSEL2 > 0h, AUXEN = Fh

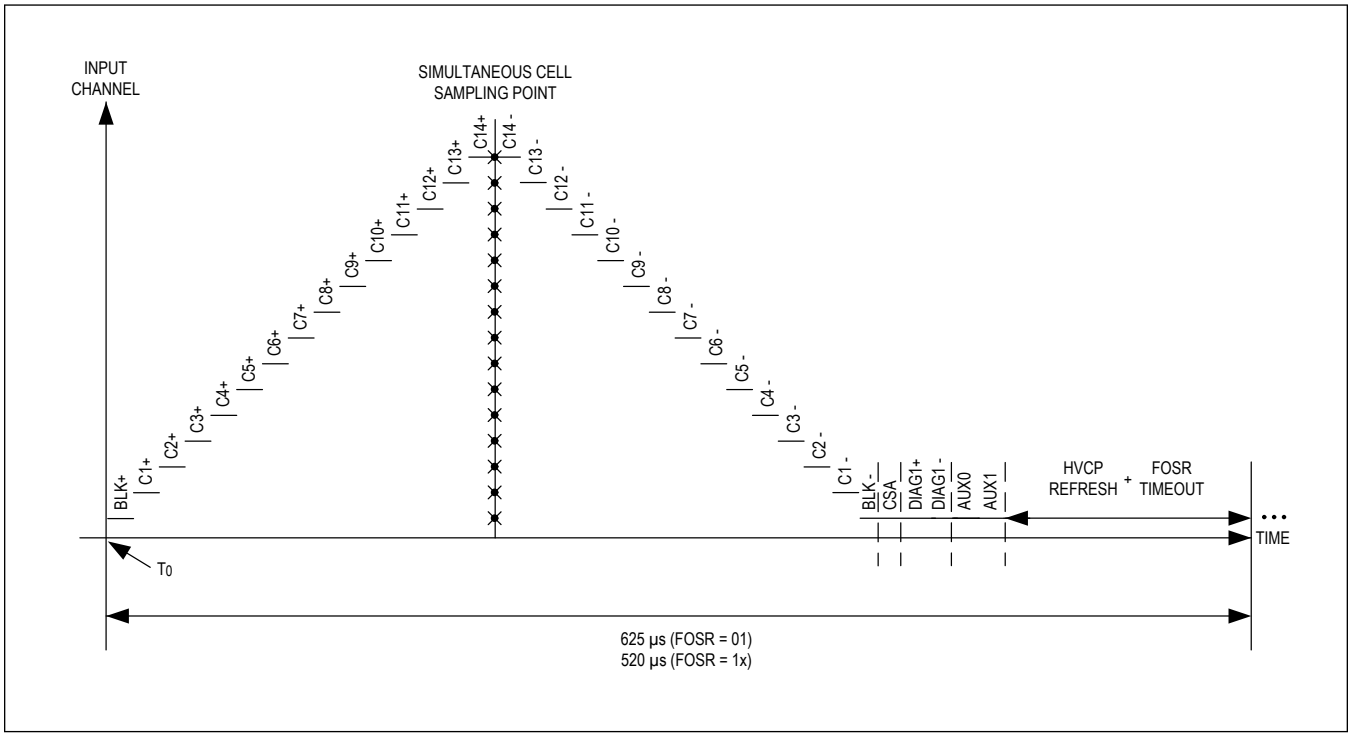


Figure 26. Acquisition - SCANCFG = 0h, SCANMODE = 0, OVSAMPL > 0h, ALTMUXSEL = 0, BLOCKEN = 1, CSAEN = 1, DIAGSEL1 > 0h, AUXEN = 03h, FOSR > 0h

Pyramid Mode Acquisition Time

The total time for ADC Pyramid Mode acquisitions can be calculated by summing all the conditional process times as shown in following tables. There is one measurement cycle per oversample acquisition.

ADC Acquisition Timing - Pyramid Mode

Table 16. ADC Pyramid Mode (SCANMODE = 0) Acquisition Time

PROCESS	TIME (µs)	CONDITION	FREQUENCY
Initialization	15	Always	Once Per Acquisition
AUXIN Settling (if enabled)	6 *x* AUXTIME[9:0]	THRMMODE = Automatic Mode and FOSR = 1.6kHz, 1.92kHz Mode	Once Per Acquisition
	6 *x* AUXTIME[9:0] - $t_{Initialization}$ - t_{VBLK} - $t_{Cell_Scan_Setup}$ - t_{Cell_Scan} - t_{Diag_Total}	THRMMODE = Automatic Mode and FOSR = Free Run Mode	
VBLK Measurement (if enabled)	27.75	BLOCKEN =1	Every Measurement Cycle
Cell Scan Setup	6.38	For any cell(s) enabled	
Cell Measurement	9 *x* y	For y = number of enabled cell inputs	
CSA Measurement (Note 1)	106.06	CSAGAIN = 256	

Table 16. ADC Pyramid Mode (SCANMODE = 0) Acquisition Time (continued)

PROCESS	TIME (µs)	CONDITION	FREQUENCY
	104.94	CSAGAIN = 128	
	45.88	CSAGAIN = 64	
	44.38	CSAGAIN = 32	
	37.25	CSAGAIN = 16	
	29.00	CSAGAIN = 8	
	26.38	CSAGAIN = 4	
DIAG1 Measurement AND / OR DIAG2 Measurement (if enabled)	32.44	Die Temperature Diagnostic	
	23.81	VAA Diagnostic	
	8.44	Comp Signal Path Diagnostic	
	24.44	Cell Gain Calibration Diagnostic	
	86.44	V_{ALTREF} Diagnostic	
	19.50	DAC 3/4, DAC 1/4	
	5.44	All Other Diagnostics	
AUXIN Measurement (if enabled)	5.44 x x	For x = number of enabled AUXIN Inputs	
HV Recovery (if oversampling enabled)	57 x (z - 1)	For z = number of oversamples	Every Measurement Cycle Except Last
ADCZSFS Diagnostic (if enabled)	11.2	ADCZSFSEN = 1	End of Acquisition

Note: The CSA conversion is concurrently performed with the voltage measurements. Therefore, the effective time is that listed in the table subtracted by t_{VBLK}, $t_{Cell_Scan_Setup}$, and t_{Cell_Scan} with a minimum achievable time of 5.8µs.

Ramp Mode Acquisition Sequence

The ADC acquisition process for Ramp Mode (SCANMODE = 0) is outlined below:

1. Disable HV charge pump
2. VBLK conversion (first phase), if enabled
3. All enabled cell conversions (1 through 14), if enabled
4. VBLK conversion (second phase), if enabled
5. CSA conversion, if enabled
6. DIAG1 conversion, if enabled
7. DIAG2 conversion, if enabled
8. Auxiliary conversions, if enabled
9. Enable HV charge pump for recovery period unless OVSAMPL = 000b (no oversampling) or all oversample measurements are complete
10. Repeat steps 1 through 7 until all oversamples are done
11. Set SCANDONE bit

ADC Ramp Mode Figures

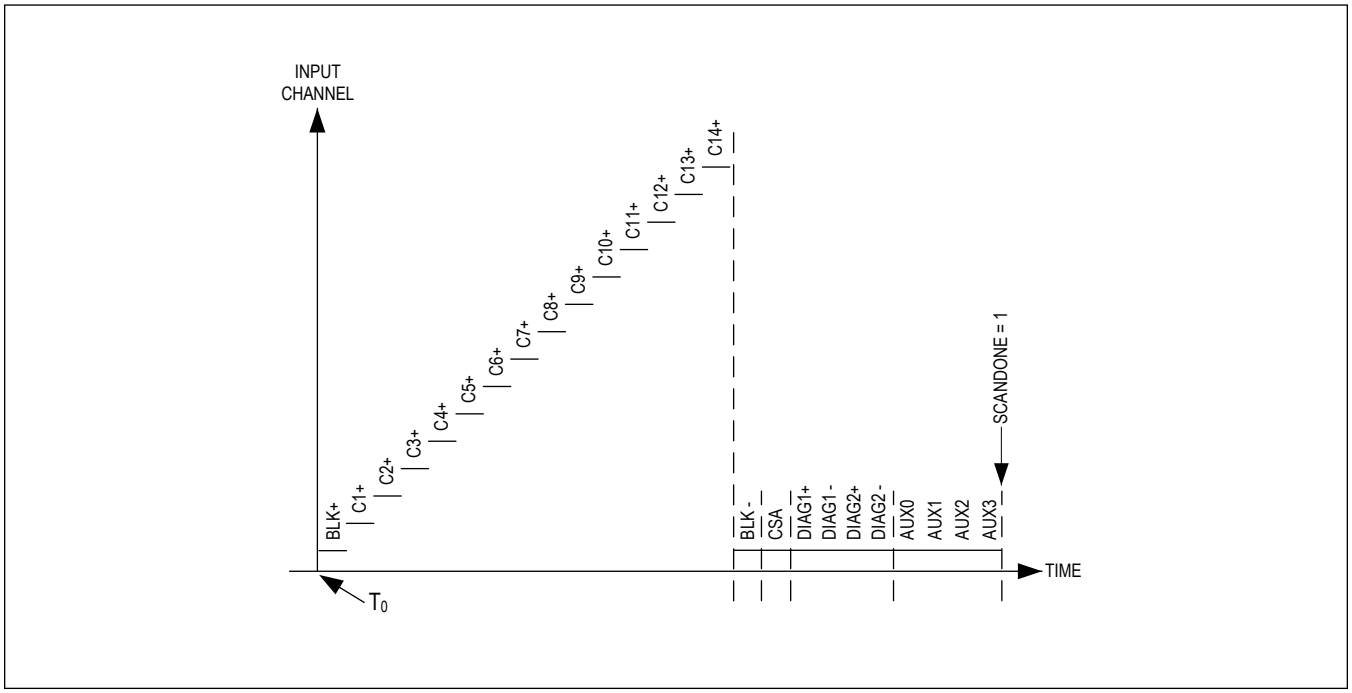


Figure 27. Acquisition - SCANCFG = 0h, SCANMODE = 1, OVSAMPL = 0h, ALTMUXSEL = 0, BLOCKEN = 1, CSAEN = 1 DIAGSEL1 > 0h, DIAGSEL2 > 0h, AUXEN = Fh

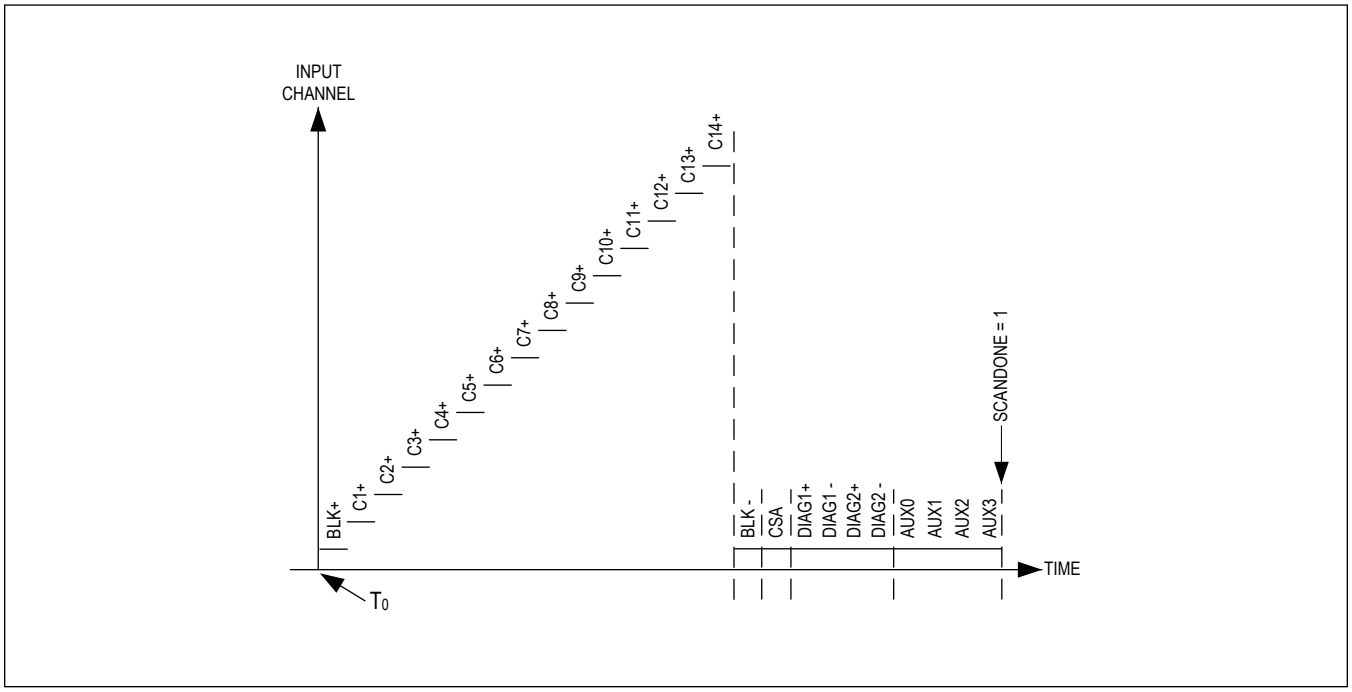


Figure 28. Acquisition - SCANCFG = 0h, SCANMODE = 1, OVSAMPL = 0h, TOPCELL1/2 = 14, ALTMUXSEL = 1, BLOCKEN = 1, CSAEN = 1, DIAGSEL1 > 0h, DIAGSEL2 > 0h, AUXEN = Fh

Ramp Mode Acquisition Time

The total time for ADC Ramp Mode acquisitions can be calculated by summing all the conditional process times as shown in Table 17. There is one measurement cycle per oversample acquisition.

ADC Acquisition Timing - Ramp Mode

Table 17. ADC Ramp Mode (SCANMODE = 1) Acquisition Time

PROCESS	TIME (µs)	CONDITION	FREQUENCY
Initialization	15	Always	Once Per Acquisition
AUXIN Settling (if enabled)	6 x AUXTIME[9:0]	THRMMODE = Automatic Mode & FOSR = 1.6kHz, 1.92kHz Mode	Once Per Acquisition
	6 x AUXTIME[9:0] - $t_{Initialization}$ - t_{VBLK} - $t_{Cell_Scan_Setup}$ - t_{Cell_Scan} - t_{Diag_Total}	THRMMODE = Automatic Mode & FOSR = Free Run Mode	
VBLK Measurement (if enabled)	27.75	BLOCKEN =1	Every Measurement Cycle
Cell Scan Setup	3.19	For any cell(s) enabled	
Cell Measurement	4.5 x y	For y = # of enabled cell inputs	
CSA Measurement (Note 1)	106.06	CSAGAIN = 256	
	104.94	CSAGAIN = 128	

Table 17. ADC Ramp Mode (SCANMODE = 1) Acquisition Time (continued)

PROCESS	TIME (µs)	CONDITION	FREQUENCY
	45.88	CSAGAIN = 64	
	44.38	CSAGAIN = 32	
	37.25	CSAGAIN = 16	
	29	CSAGAIN = 8	
	26.38	CSAGAIN = 4	
DIAG1 Measurement AND / OR DIAG2 Measurement (if enabled)	32.44	Die Temperature Diagnostic	
	23.81	VAA Diagnostic	
	8.44	Comp Signal Path Diagnostic	
	24.44	Cell Gain Calibration Diagnostic	
	86.44	V_{ALTREF} Diagnostic	
	19.5	DAC 3/4, DAC 1/4	
	5.44	All Other Diagnostics	
AUXIN Measurement (if enabled)	5.44 x x	For x = # of enabled AUXIN Inputs	
HV Recovery (if oversampling enabled)	57 x (z - 1)	For z = number of oversamples	Every Measurement Cycle Except Last
ADCZSFS Diagnostic (if enabled)	11.2	ADCZSFSEN = 1	End of Acquisition
COMPACC Diagnostic (if enabled)	13.5	COMPACCEN = 1	End of Acquisition

Note: The CSA conversion is concurrently performed with the voltage measurements. Therefore, the effective time is that listed in the table subtracted by t_{VBLK}, $t_{Cell_Scan_Setup}$, and t_{Cell_Scan} with a minimum achievable time of 5.8µs.

ADC Acquisition Time Example

Table 18 provides examples of common configuration and the associated acquisition time that can be achieved.

Table 18. ADC Acquisition Time Examples (with AUXTIME[9:0] = 000h)

ENABLED MEASUREMENTS	NO OVERSAMPLING (OVSAMPL[2:0] = 0h)		8x OVERSAMPLING (OVSAMPL[2:0]= 2h)		16x OVERSAMPLING (OVSAMPL[2:0]= 3h)	
	Pyramid Scan	Ramp Scan	Pyramid Scan	Ramp Scan	Pyramid Scan	Ramp Scan
14 Cells	148.3 µs	82.1 µs	1480.5 µs	951 µs	3003.1 µs	1944 µs
14 Cells, VBLK	175.7 µs	109.5 µs	1699.5 µs	1170 µs	3441.1 µs	2382 µs
14 Cells, 4 Aux	170.1 µs	103.9 µs	1654.6 µs	1125.1 µs	3351.2 µs	2292.2 µs
14 Cells, 4 Aux, CSA (CSAGAIN = 32)	175.7 µs	109.5 µs	1699.6 µs	1170.1 µs	3441.2 µs	2382.2 µs
14 Cells, VBLK, 4 AUX	197.5 µs	131.3 µs	1872.3 µs	1342.8 µs	3786.4 µs	2727.4 µs
14 Cells, VBLK, 4 Aux, CSA (CSAGAIN = 32)	203.1 µs	136.9 µs	1918.6 µs	1389.1 µs	3879.2 µs	2820.2 µs
14 Cells, VBLK, Die Temp DIAG, 4 Aux	229.7 µs	163.5 µs	2130.3 µs	1600.8 µs	4302.4 µs	3243.4 µs
14 Cells, VBLK, Die Temp DIAG, 4 Aux, CSA (CSAGAIN = 32)	235.3 µs	169.1 µs	2176.6 µs	1647.1 µs	4395.2 µs	3336.2 µs

Comparator Configuration and Properties

Comparator Scan Properities

The comparator acquisition can be configured for unipolar Cell measurements and Auxiliary measurements. If a cell input is configured for bipolar operation in the POLARITYCTRL register, the comparator measurement is idle for this acquisition period and the associated alert reporting in the ALRTCOMPOVREG and ALRTCOMPUVREG register will not be updated. If acquisition time is of critical importance for a comparator scan, it is recommended to disable bipolar inputs in the MEASUREEN1 register to prior to issuing a SCAN as this will omit these measurements from the acquisition.

The SCANMODE bit configuration also does not apply to the comparator acquisition and the comparator will operate only on the inputs indicated by the MEASUREEN1 and ALRTOVEN, ALRTUVEN registers. This is illustrated in the comparator acquisition process defined below.

Comparator Acquisition

The acquisition is initiated by writing a logic one to the SCAN bit in the SCANCTRL register. This write acts as a strobe, and the SCAN bit content is automatically cleared, reading back a logic zero if polled. In daisy-chained devices, acquisitions in either UART path (depending on the Master configuration) will be delayed by the propagation delay, tPROP, of the command packet through each device. The acquisition for device is signaled complete when SCANDONE bit is a logic one.

Note: If any additional write to the SCANCFG is issued prior to the SCANDONE bit being cleared this command will be ignored.

Comparator Acquisition Process

1. Disable HV charge pump
2. Perform overvoltage conversion on all enabled Cell Inputs (MEASUREEN1) against COMPOVTH threshold (ascending order 1 through 14)
3. Update ALRTCOMPOV Register (MEASUREEN1 & ALRTOVEN)
4. Perform undervoltage conversion on all enabled Cell Inputs (MEASUREEN1) against COMPUVTH threshold (descending order 14 through 1)
5. Update ALRTCOMPUV Register (MEASUREEN1 and ALRTUVEN)
6. Perform overvoltage conversion on all enabled Auxiliary Inputs (MEASUREEN2) against COMPAUXOVTH (ascending order 0 through 5)
7. Update ALRTCOMPAUXOV Register (MEASUREEN2 and ALRTAUXOVEN)
8. Perform undervoltage conversion on all enabled Auxiliary Inputs (MEASUREEN2) against COMPAUXUVTH (ascending order 0 through 5)
9. Update ALRTCOMPAUXUV Register (MEASUREEN2 and ALRTAUXUVEN)
10. HV Charge Pump refresh
11. Repeat steps 2-6 until all oversamples complete
12. Compare results against comparator thresholds and update alert status
13. Enable HV Charge Pump

Note: Comparator results are only available when the corresponding OV/UV Alerts are enabled.

Comparator Thresholds

The comparator cell measurements and auxiliary measurements can be programmed with OV and UV thresholds that are independent of the ADC OV and UV thresholds. However, all cell measurements will share the same threshold settings as defined by the COMPOVTH and COMPUVTH registers. Additionally, all ratiometric auxiliary measurement will share the same thresholds settings as defined by the COMPAUXROVTH and COMPAUXRUVTH registers and all absolute auxiliary measurements will share the same threshold settings as defined by the COMPAUXAOVTH and COMPAUXAUVTH registers.

As defined in the Comparator Input Range section, each threshold register is programmable up to 10 bits allowing for 4.9mV, 3.2mV, and 2.2mV of adjustable resolution on the cell, ratiometric auxiliary, and absolute auxiliary measurements respectively.

Note: for the auxiliary inputs since the full scale is dependent on V_{AA} this may have an impact on the resolution of the comparator over loading and temperature conditions.

If the pin configuration for the auxiliary inputs is set to GPIO or I^2C mode, both ALRTAUXOVEN and ALRTAUXUVEN are disabled (logic zero).

Comparator Acquisition Time

The total time for Comparator acquisitions can be calculated by summing all the conditional process times as shown in Table 19. There is one measurement cycle per oversample acquisition.

Table 19. Comparator Acquisition Time

PROCESS	TIME (µs)	CONDITION	FREQUENCY
Initialization	15	Always	Once Per Acquisition
AUXIN Settling (if enabled)	6 *x* AUXTIME[9:0]	THRMMODE = Automatic Mode and FOSR = 1.6kHz, 1.92kHz Mode	Once Per Acquisition
	6 *x* AUXTIME[9:0] - $t_{Initialization}$ - t_{VBLK} - $t_{Cell_Scan_Setup}$ - t_{Cell_Scan} - t_{Diag_Total}	THRMMODE = Automatic Mode and FOSR = Free Run Mode	
Cell Scan Setup	6.38	For any cell(s) enabled	Every Measurement Cycle
Cell Measurement	12 *x* y	For y = number of enabled cell inputs	
AUXIN Measurement (if enabled)	12.56 x	For x = number of enabled AUXIN Inputs	
HV Recovery (if oversampling enabled)	57 *x* (z - 1)	For z = number of oversamples	Every Measurement Cycle Except Last
COMPACC Diagnostic (if enabled)	13.5	COMPACCEN = 1	End of Acquisition

Comparator Acquisition Timing Example

Table 20 provides an example of common configuration and the associated acquisition time that can be achieved.

Table 20. Comparator Acquisition Time Examples (with AUXTIME[9:0] = 000h)

ENABLED MEASUREMENTS	NO OVERSAMPLING (OVSAMPL[2:0] = 0h)	8x OVERSAMPLING (OVSAMPL[2:0] = 2h)	16x OVERSAMPLING (OVSAMPL[2:0] = 3h)
14 Cells	190.3 µs	1816.5 µs	3675.1 µs
14 Cells, 4 Aux	265.7 µs	2419.4 µs	4880.8 µs

Comparator Scan Figures

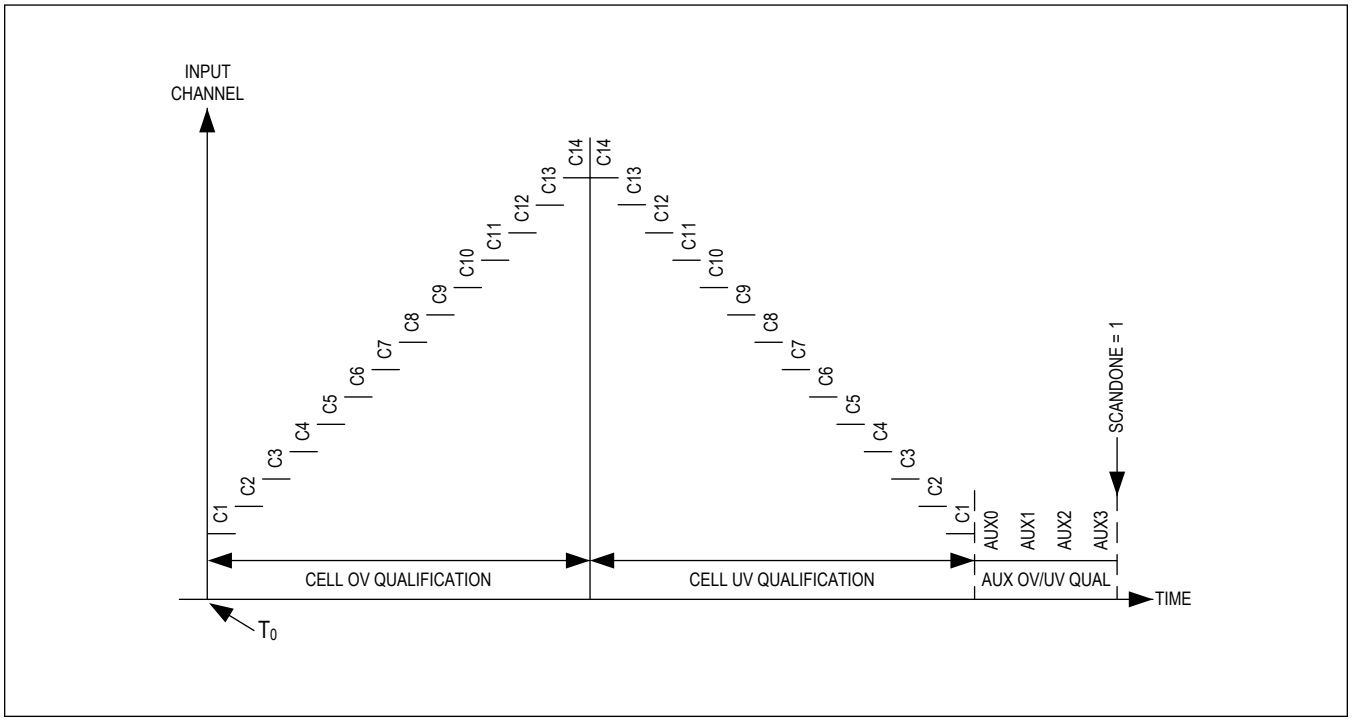


Figure 29. Comparator Single Scan Mode

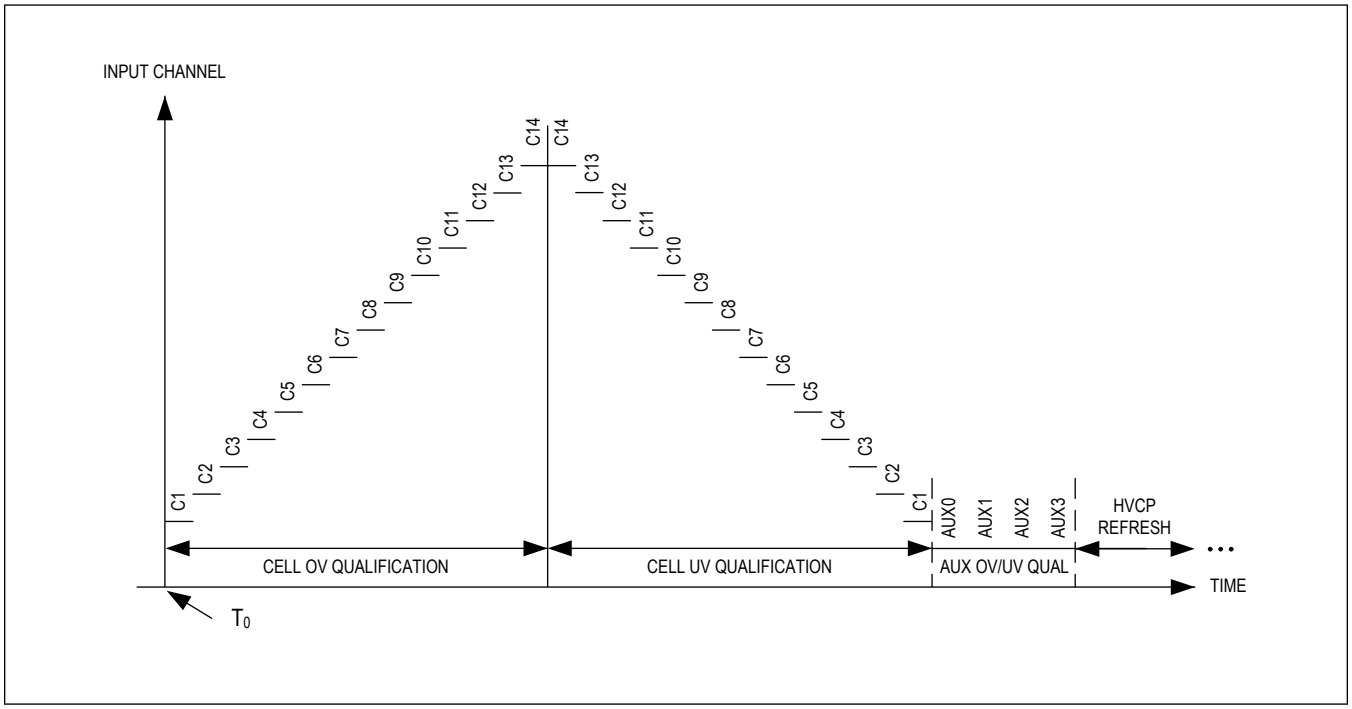


Figure 30. Comparator Single Scan With Oversampling

ADC+COMP Configuration and Properties

ADC+COMP Scan Mode

ADC+COMP acquisitions can be applied to the Cell, Auxiliary, Block, Diagnostics, and CSA measurements. Each measurement engine (ADC or Comparator) will retain the functionality discussed previously with additional clarification detailed below.

The comparator acquisition is applied to the unipolar Cell and Auxiliary inputs and will be idle during bipolar Cell, Block, Diagnostics, and CSA measurements. OV and UV alerts for the the cell path, (OVALRTEN and UVALERTEN) and Auxiliary path (AUXOVALRTEN and AUXUVALRTEN) are applied to both ADC and comparator with each capable of setting it unique threshold. If any OV or UV Alert is disabled the ADC measurement still occurs, however the comparator is idle during this portion of the acquisition.

In ADC+COMP scan mode, the ADC acquisition only operates in pyramid mode and the SCANMODE bit is ignored.

ADC+COMP Acquisition Time

The total time for ADC+COMP acquisitions can be calculated by summing all the conditional process times as shown in the following tables. There is one measurement cycle per oversample acquisition.

Table 21. ADC+COMP Acquisition Time

PROCESS	TIME (µs)	CONDITION	FREQUENCY
Initialization	15	Always	Once Per Acquisition
AUXIN Settling (if enabled)	6 *x* AUXTIME[9:0]	THRMMODE = Automatic Mode and FOSR = 1.6kHz, 1.92kHz Mode	Once Per Acquisition

Table 21. ADC+COMP Acquisition Time (continued)

PROCESS	TIME (µs)	CONDITION	FREQUENCY
	6 *x* AUXTIME[9:0] - $t_{Initialization}$ - t_{VBLK} - $t_{Cell_Scan_Setup}$ - t_{Cell_Scan} - t_{Diag_Total}	THRMMODE = Automatic Mode and FOSR = Free Run Mode	
VBLK Measurement (if enabled)	27.75	BLOCKEN =1	Every Measurement Cycle
Cell Scan Setup	6.38	For any cell(s) enabled	
Cell Measurement	12 *x* y	For y = # of enabled cell inputs	
CSA Measurement (Note 1)	106.06	CSAGAIN = 256	
	104.94	CSAGAIN = 128	
	45.88	CSAGAIN = 64	
	44.38	CSAGAIN = 32	
	37.25	CSAGAIN = 16	
	29.00	CSAGAIN = 8	
	26.38	CSAGAIN = 4	
DIAG1 Measurement AND/OR DIAG2 Measurement (if enabled)	32.44	Die Temperature Diagnostic	
	23.81	VAA Diagnostic	
	8.44	Comp Signal Path Diagnostic	
	24.44	Cell Gain Calibration Diagnostic	
	86.44	V_{ALTREF} Diagnostic	
	19.50	DAC 3/4, DAC 1/4	
	5.44	All Other Diagnostics	
AUXIN Measurement (if enabled)	12.56 *x* x	For x = number of enabled AUXIN Inputs	
HV Recovery (if oversampling enabled)	57 *x* (z - 1)	For z = number of oversamples	Every Measurement Cycle Except Last
ADCZSFS Diagnostic (if enabled)	11.2	ADCZSFSEN = 1	End of Acquisition
COMPACC Diagnostic (if enabled)	13.5	COMPACCEN = 1	End of Acquisition

Note: The CSA conversion is concurrently performed with the voltage measurements. Thus the effective time is that listed in the table subtracted by t_{VBLK}, $t_{Cell_Scan_Setup}$, and t_{Cell_Scan} with a minimum achievable time of 5.8µs.

ADC+COMP Acquisition Time Example

Table 22 provides examples of common configuration and the associated acquisition time that can be achieved:

Table 22. ADC+COMP Acquisition Time Examples (with AUXTIME[9:0] = 000h)

ENABLED MEASUREMENTS	NO OVERSAMPLING (OVSAMPL[2:0] = 0h)	8x OVERSAMPLING (OVSAMPL[2:0] = 2h)	16x OVERSAMPLING (OVSAMPL[2:0] = 3h)
14 Cells	187.1 µs	1791 µs	3624 µs
14 Cells, VBLK	241.5 µs	2010 µs	4062 µs
14 Cells, 4 Aux	237.4 µs	2192.9 µs	4427.9 µs

Table 22. ADC+COMP Acquisition Time Examples (with AUXTIME[9:0] = 000h) (continued)

ENABLED MEASUREMENTS	NO OVERSAMPLING (OVSAMPL[2:0] = 0h)	8x OVERSAMPLING (OVSAMPL[2:0] = 2h)	16x OVERSAMPLING (OVSAMPL[2:0] = 3h)
14 Cells, VBLK, CSA (CSAGAIN = 32), 4 Aux	270.4 µs	2456.9 µs	4955.9 µs
14 Cells, VBLK, CSA (CSAGAIN = 32), 4 Aux, Die Temp DIAG	302.6 µs	2714.9 µs	5471.9 µs

ADC+COMP Scan Figures

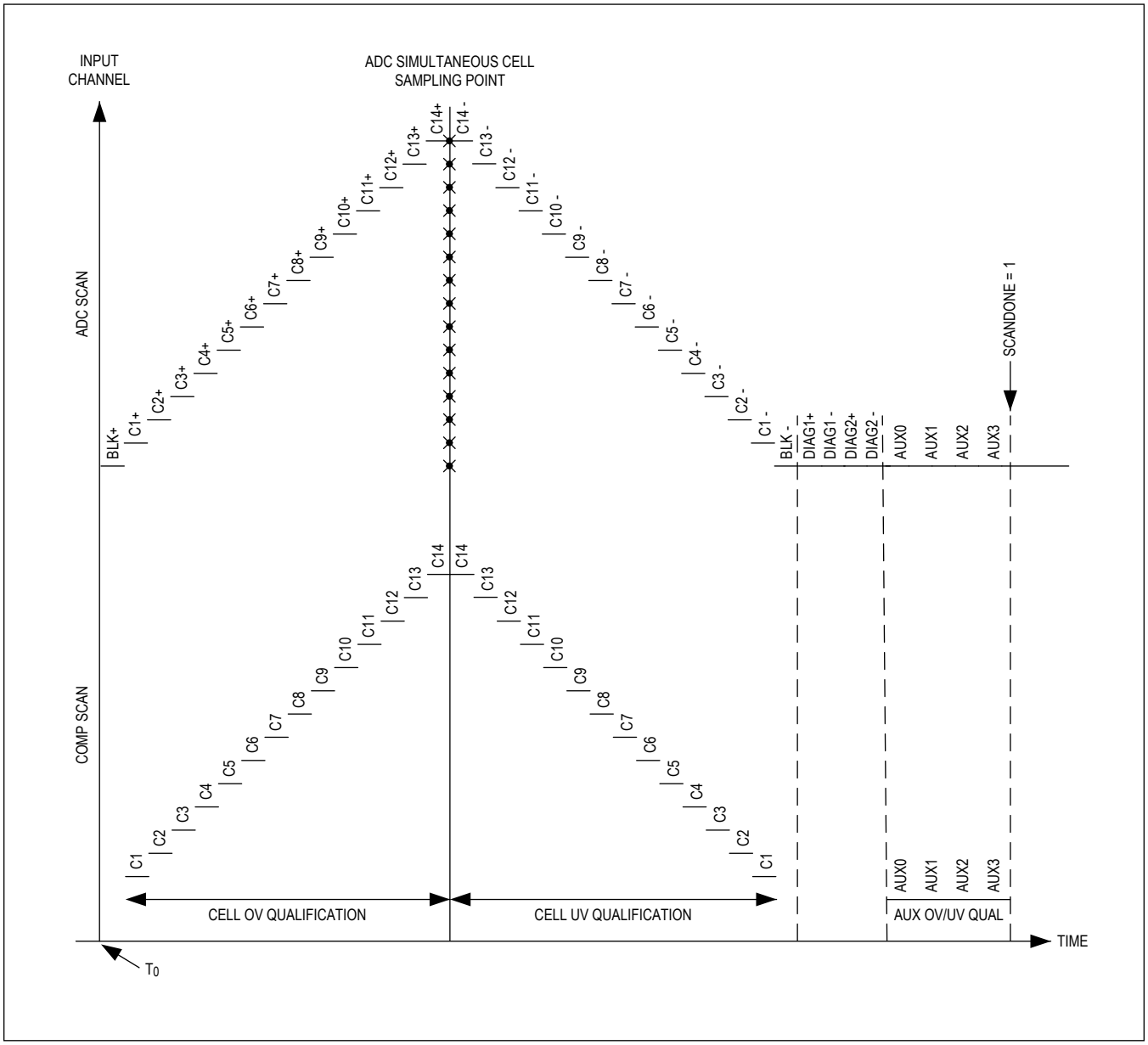


Figure 31. Simultaneous ADC+COMP Scan Mode

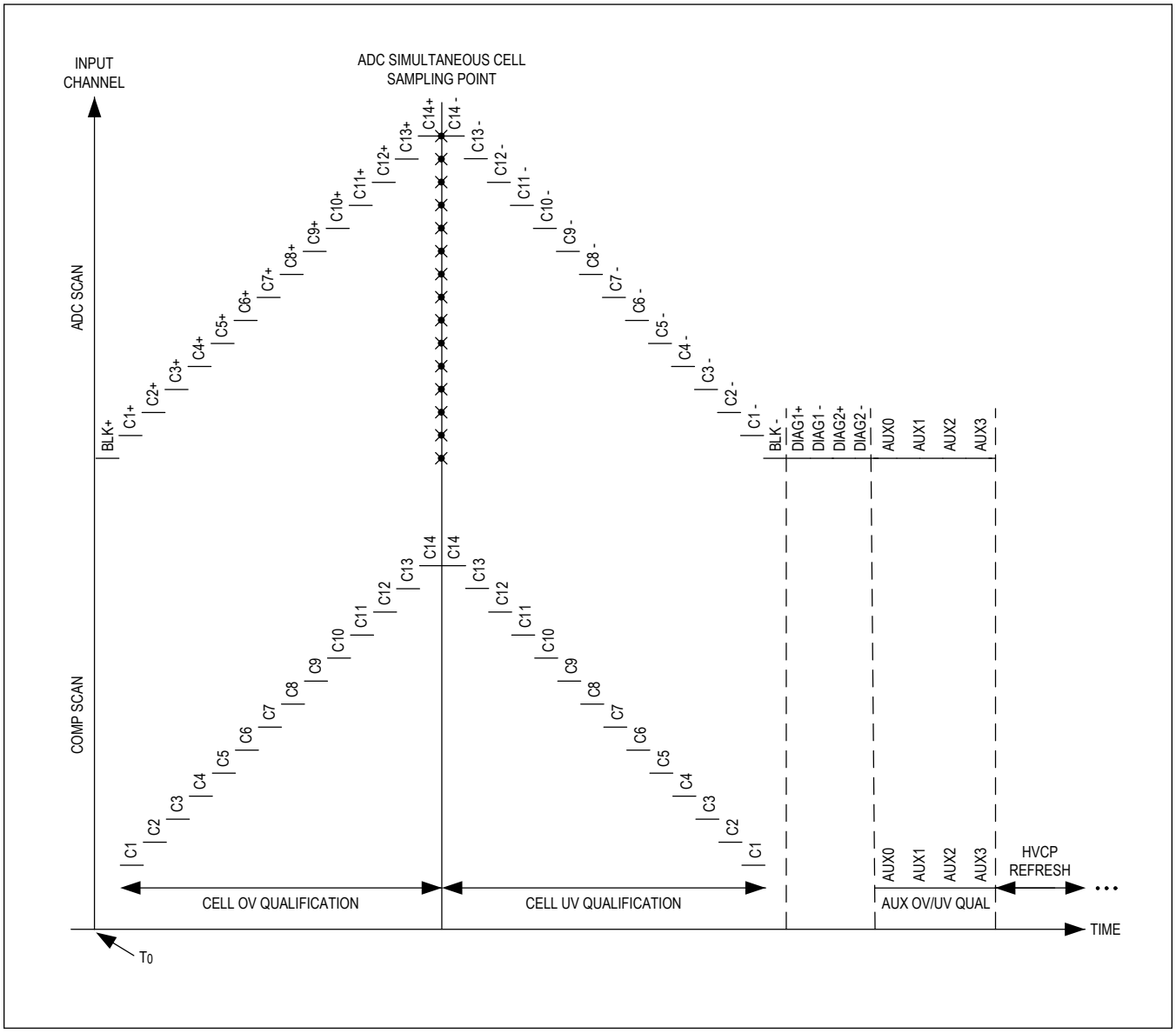


Figure 32. Simultaneous ADC+COMP Scan With Oversampling

On-Demand Calibration

The MAX17852 supports an integrated On-Demand calibration procedure, which can be commanded by the user to improve the internal measurement accuracy from inaccuracies of the internal signal chain. It should be noted, however, that the calibration process will not correct for inaccuracies within the external application components. The calibrated accuracy is described within the measurement accuracy section of *Electrical Characteristics*.

For a valid On-Demand calibration, a calibration acquisition must be commanded using the SCANCFG bits of the SCANCTRL register. The calibration acquisition automatically configures the internal calibration sources and performs ADC acquisitions to calculate and store calibration coefficients for the Cell Inputs, Auxiliary Inputs, Block Input, and CSA Input. The completion of the calibration acquisition will be signaled by the issuance of the SCANDONE bit like any

other acquisition. Any commands that are sent before the calibration acquisition is completed will be ignored but will still propagate through the daisy chain.

The calibration time is 3.75ms.

Note: The calibration acquisition is independent of the Scan Control Registers and Scan Setting Registers (POLARITYCTRL, SCANCTRL, ACQCFG).

The ADCCALEN bit must be set for the calibration coefficients to be applied to the measurement results. If ADCCALEN is disabled, even with the successful completion of a calibration acquisition, the measurement results will not have the calibration coefficients applied.

Note: The On-Demand calibration is independent of the factory calibration. In the event that the On-Demand calibration is applied, the device will retain its factory calibration setting. The factory calibration setting can never be overwritten and can be verified using the ROM CRC diagnostic in the Diagnostics section. See ADC Scan Properties for details on using calibration to maintain Ramp Mode accuracy over DCIN voltage range; factory calibration defaults are programmed using a 50V DCIN voltage.

Table 23 below indicates which calibration alerts are associated to the various measurement path

Table 23. Measurement Path Calibration Alerts

MEASUREMENT PATH	CALIBRATION ALERTS
Cell Input - Pyramid (SCANMODE = 0b)	ALRTCALGAINP, ALRTCALOSADC
Cell Input - Ramp (SCANMODE = 1b)	ALRTCALGAINR, ALRTCALOSR
Auxiliary Input - Absolute (REFSEL = 1b)	ALRTCALOSADC
Auxiliary Input - Ratiometric (REFSEL = 0b)	ALRTCALOSTHRM
Block Input	ALRTCALOSADC
CSA Input	ALRTCALOSADC

The On-Demand calibration adjustments can be verified by using the Cell Calibration and Offset Calibration commands in the DIAGSEL1 and DIAGSEL2 bits. Please see the Diagnostics section for further details.

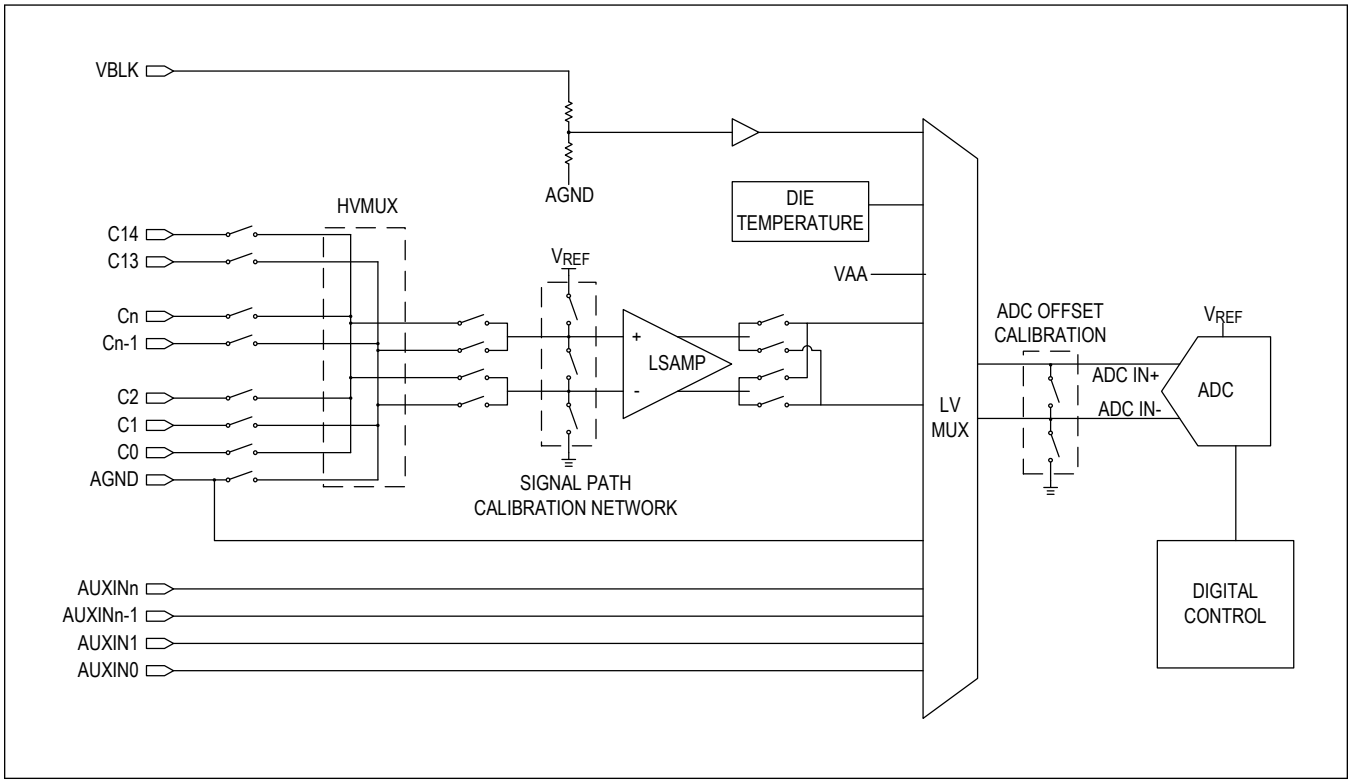


Figure 33. On Demand Calibration Block Diagram

Calibration Alerts

Internal safety mechanisms are implemented to ensure that the applied calibration coefficients are within predetermined bounds. If a calibration coefficient were to fall outside of these bounds, this would immediately raise a fault in the ALRTSUM register for the affected calibration process (ALRTCALOSADC, ALRTCALOSR, ALRTCALOSTHRM, ALRTCALGAINP, ALRTCALGAINR). This fault condition then propagates to the STATUS1 alert register, which is capable of flagging an issue within the Data Check Byte or within the hardware alert interface.

If the integrity of the calibration coefficients is questionable, it is recommended to issue a new calibration to verify and/or correct the fault, or to de-assert ADCCALEN and use the factory default calibration.

Oversampling

ADC Oversampling

Oversampling performs multiple measurement cycles in a single acquisition and averages the samples to reduce the measurement noise and effectively increase the resolution of each acquisition. The net increase of the measurement resolution depends on the number of oversamples. To add n bits of measurement resolution, at least 2^{2n} oversamples are required. Since the ADC resolution is 12 bits, 13-bit resolution requires at least 4 oversamples. In order to achieve the maximum 14-bit resolution, at least 16 oversamples are required. Therefore, with no oversampling, only the higher 12-bits of the measurement are statistically significant. With 4 or 8 oversamples, only the highest 13-bits are statistically significant. Taking more than 16 oversamples further reduces the measurement variation. With no oversampling, measurements can be averaged externally to achieve increased resolution but at a higher computational cost for the host.

Comparator Oversampling

To effectively mitigate high-frequency noise from affecting the comparator measurement, the output can be oversampled using the OVSAMPL bits in the SCANCTRL register. The accumulated oversamples are digitally averaged from the comparator output to gauge if a valid OV, UV condition is present. An OV, UV condition will require the comparator readings to meet or exceed the threshold listed in the table below for an alert to be generated as shown in Table 24. Thus, an OVSAMPL setting of 8 will afford 1 sample outside of the OV/UV condition before setting an alert. It is recommended for higher noise immunity that the OVSAMPL setting should be configured to 8 or higher for comparator acquisition with oversampling. When the ADC and comparator are simultaneously sampled, the oversampling will normally be set by the noise reduction required for ADC measurements.

Table 24. Comparator Faults for Alerts vs Oversampling

OVSAMPL	COMPARATOR FAULTS FOR ALERT
1	1
4	1
8	2
16	3
32	5
64	10
128	20

Note: The comparator acquisition can be performed using the cell input path (C_n) or the switch input path (SW_n) as configured by the ALTMUXSEL bit. In the event that the comparator acquisition is performed on the switch input path, it is recommended to increase the oversampling to account for the lessened noise attenuation from the inputs due to the higher lowpass cutoff frequency.

Oversampling Watchdog Timeout

Table 25. Watchdog-Timeout Duration

OVSAMPL	SAMPLES	THEORETICAL RESOLUTION	ACQUISITION WATCHDOG TIMEOUT
0b000	1	12 bits	750 µs
0b001	4	13 bits	3 ms
0b010	8	13 bits	6 ms
0b011	16	14 bits	12 ms
0b100	32	14 bits	24 ms
0b101	64	14 bits	48 ms
0b110	128	14 bits	96 ms

Note 1: *When AUTOBALSWDIS = 1, the watchdog timeout duration is extended by SWDLY or CELLDLY (depending on ALTMUXSEL).*

Note 2:*When AUXTIME is > 0, the timeout duration is extended by AUXTIME.*

100Hz & 120Hz Filtering

There are two types of scan configurations in which oversampling frequency can be utilized, each providing a different benefit to the system performance.

The first configuration is entered via FOSR = 0b00, which performs the acquisition with minimal time delay between measurement cycles to recharge the HV Charge Pump. The FOSR = 0b00 mode yields the highest number of measurements per sample period allowing for higher oversampling rates and further noise reduction. The total acquisition time is proportional to the number of oversamples configured by OVSAMPL and the type and number of enabled channels.

The FOSR settings of 0b01, 0b10 or 0b11 enables a notch filter at a frequency of 50Hz, 60Hz, 100Hz, or 120Hz. This mode may be particularly useful for accurate voltage detection during vehicle charging where noise from the power mains will effect the voltage seen by the battery pack. To enable proper filtering for 50Hz or 100Hz, the FOSR must be set to 0b01. For 60Hz or 120Hz filtering, the FOSR must be set to either 0b10 or 0b11.

Note: When configuring the FOSR the acquisition period will automatically be preconifgured to 625µs for 50Hz/100Hz and 520µs for 60Hz/120Hz.

Table 26. FOSR Notch-Filter Setting

REJECTION FREQUENCY (Hz)	FOSR	OVSAMPL
50	0x1	0x4
60	0x2 or 0x3	0x4
100	0x1	0x4 or 0x3
120	0x2 or 0x3	0x4 or 0x3
None	0x0	don't care

The typical notch-filter responses are shown below for both 100Hz (Figure 34) and 120Hz (Figure 35), respectively.

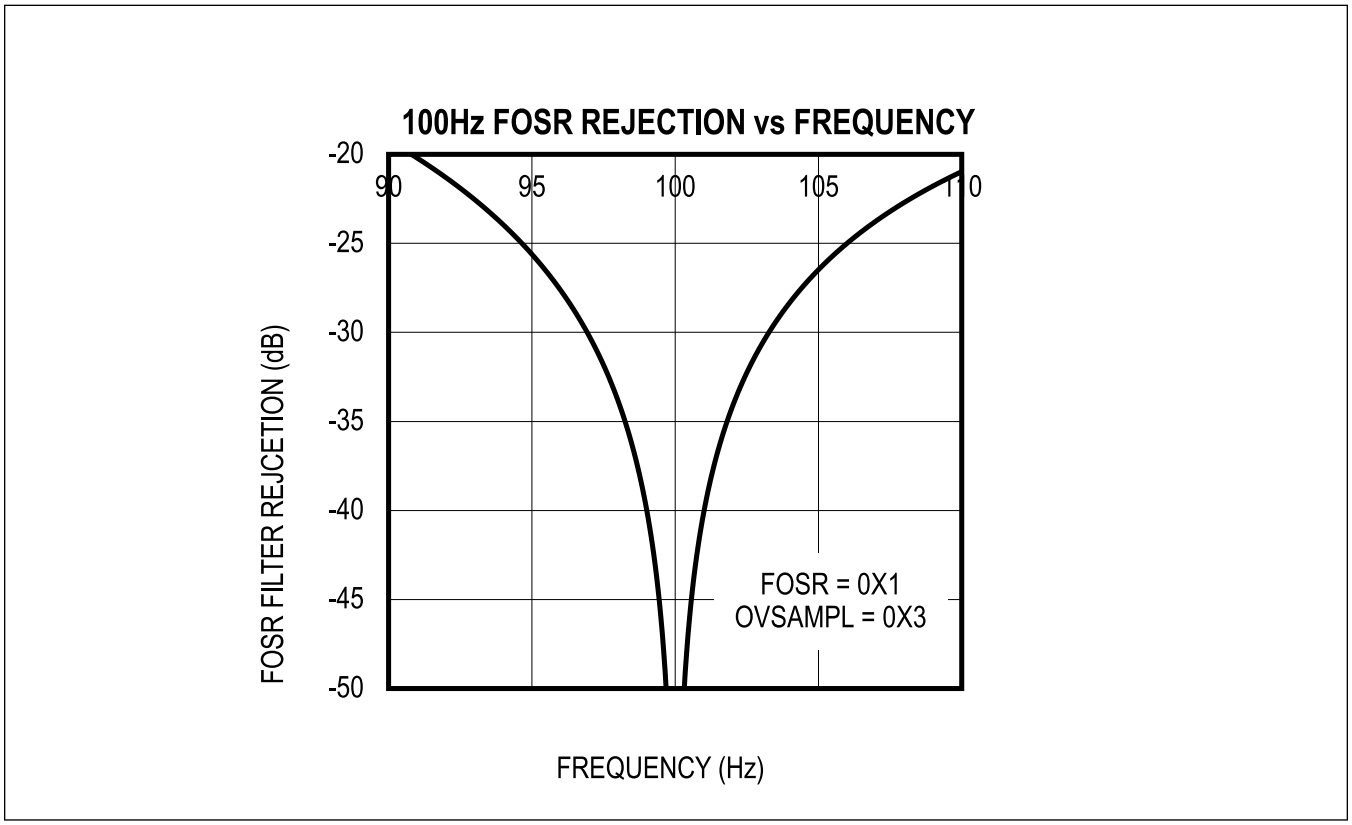


Figure 34. 100Hz Notch Filter

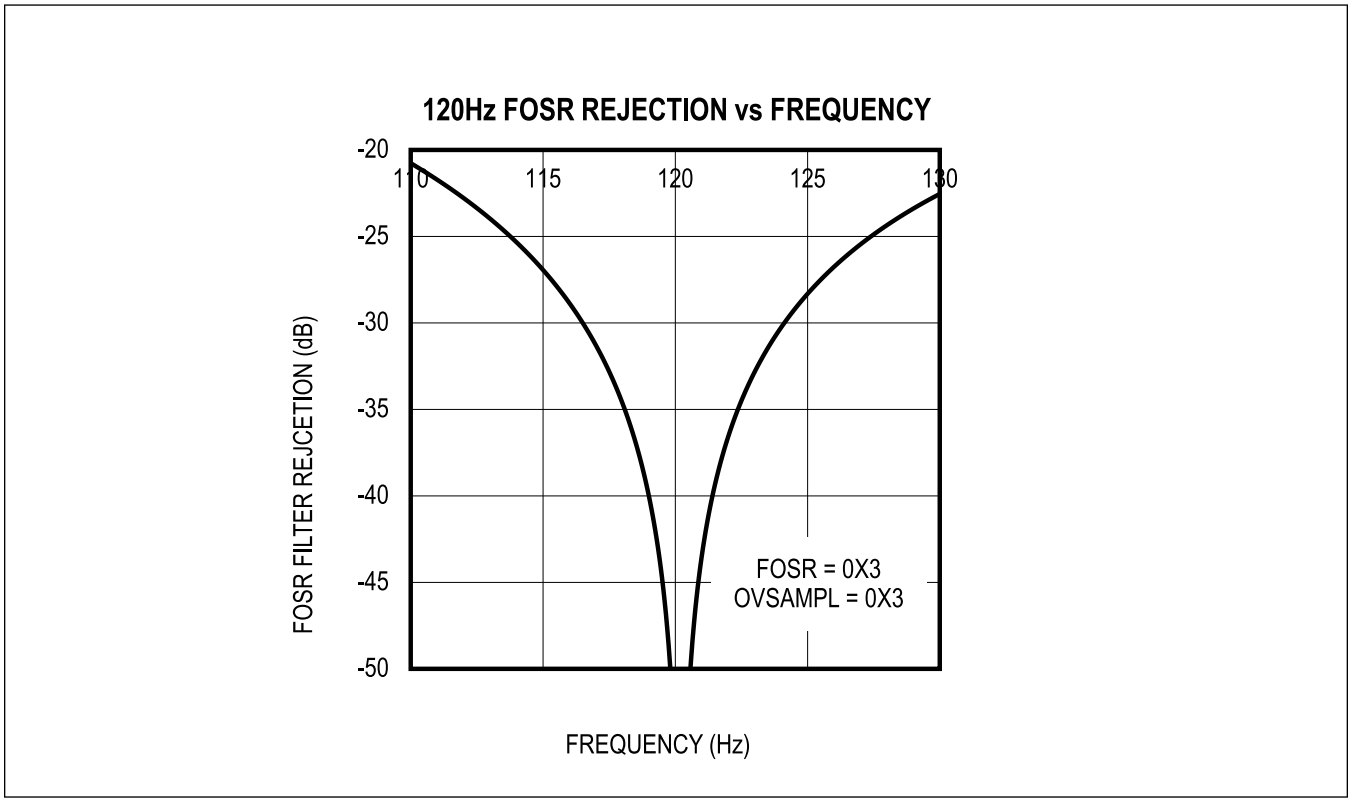


Figure 35. 120Hz Notch Filter

Acquisition Watchdog Timeout

If the acquisition does not finish within a predetermined time interval, the SCANTIMEOUT bit is set, the ADC logic is reset, the ALU registers are cleared, and the measurement data registers are also cleared. The acquisition watchdog timeout interval depends on the oversampling configuration as shown in Table 25.

If double-buffer mode is enabled (DBLBUFEN = 1), the ALU registers are cleared but the data registers remain unchanged as these are known good values previously stored. Once a move operation is evoked (SCAN = 1), the previously cleared ALU data is moved from the ALU registers to the data registers and the data registers now show as cleared. Please refer to the Double Buffer section for detailed information on the data control in mode.

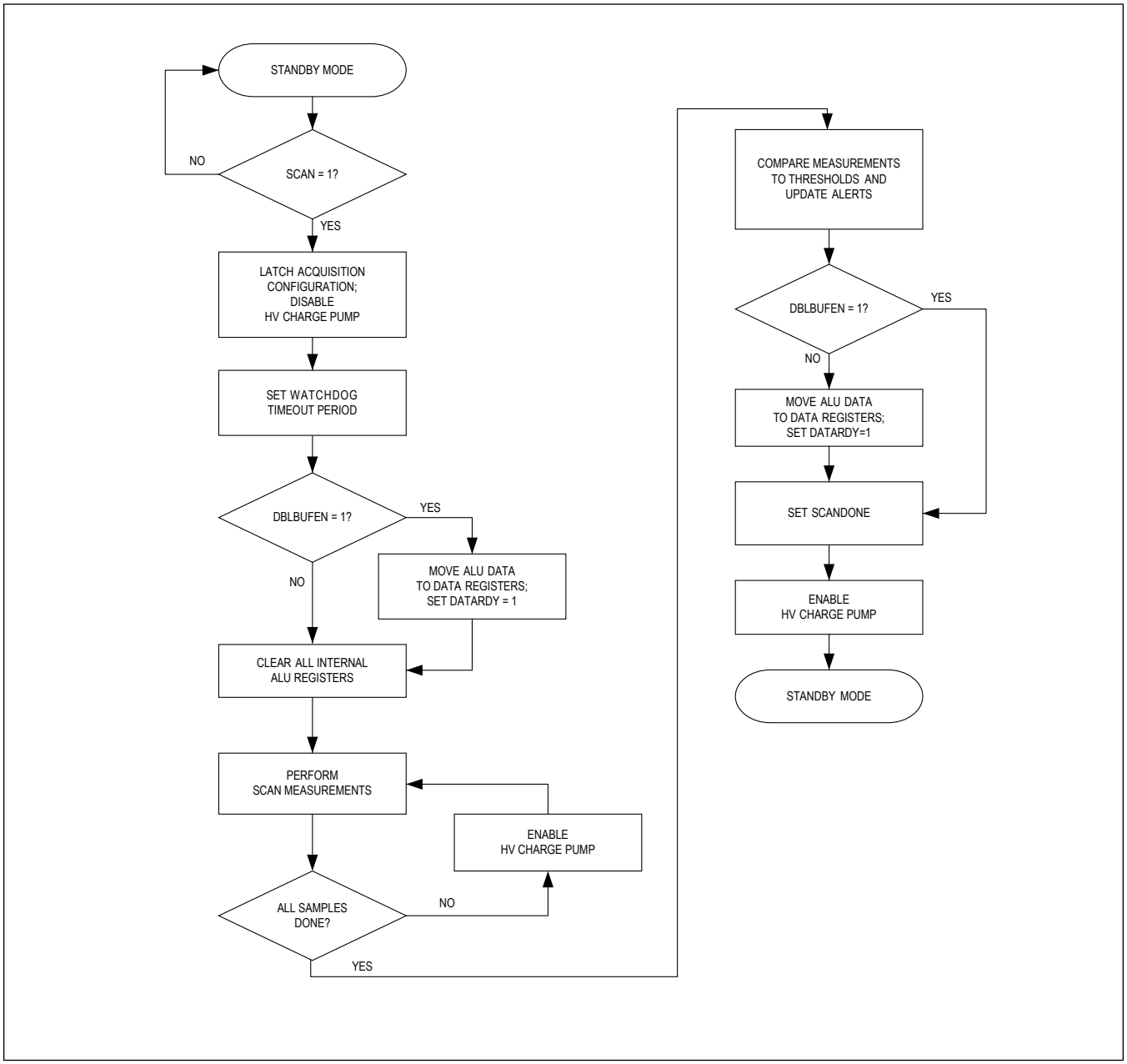


Figure 36. Acquisition-Mode Flowchart

Data Control

Acquisition Data Transfer and Control

The ADC data flow, Figure 37, can be directed through multiple data processing paths until it reaches the register space (CELLnREG, AUXnREG, BLOCKREG, CSAREG, DIAG1REG, DIAG2REG, TOTALREG, and MINMAXCELL) depending on the enabled configuration. The following sections detail the data flow through:

- Calibration
- IIR Filter
- Single Buffer Data Transfer
- Double Buffer Data Transfer
- Cell Balancing with Embedded Measurements

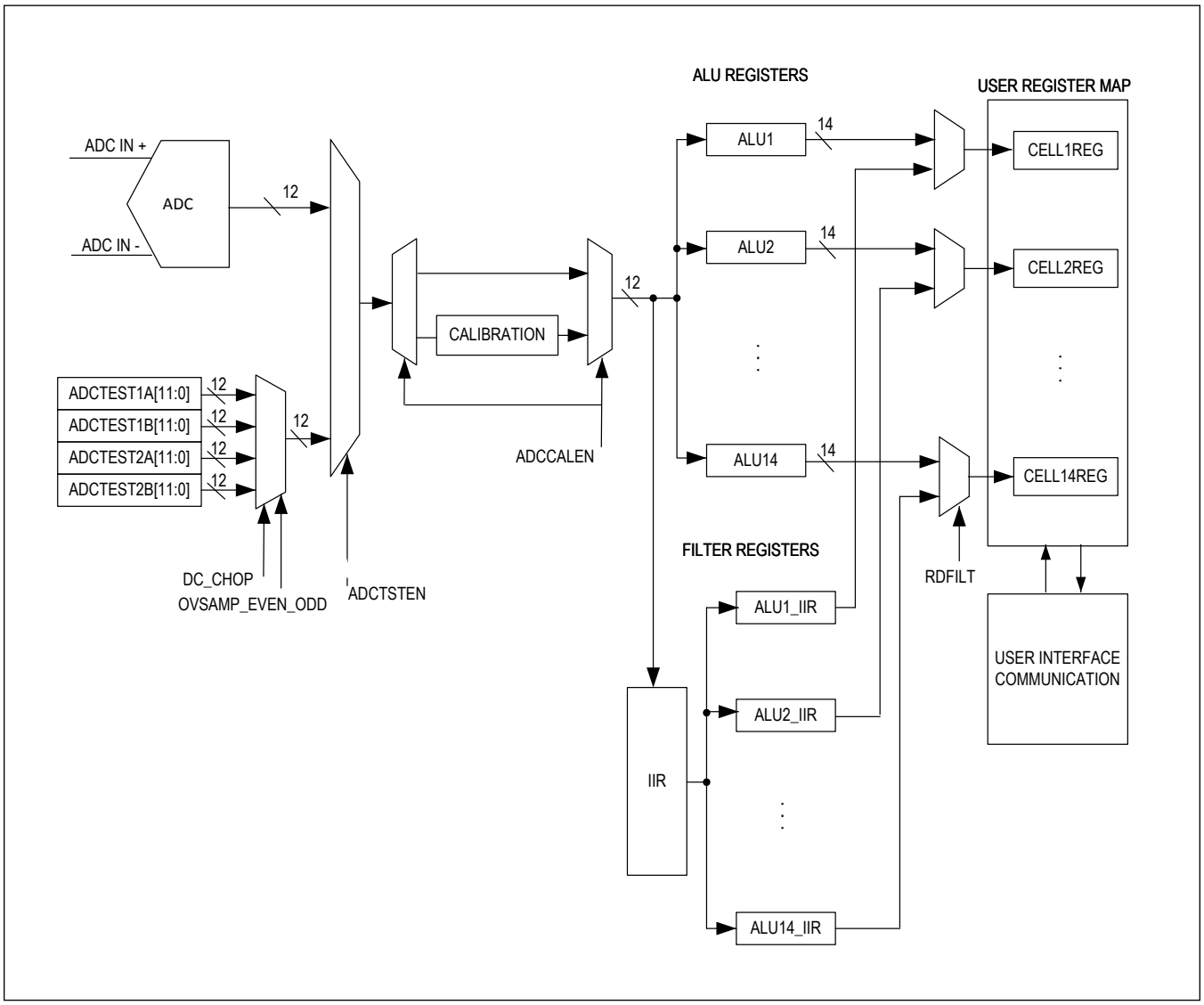


Figure 37. Data-Flow Diagram

Calibration Data Control

The ADC data is either directly output to the ALU or acted upon by the Calibration block depending on the state of the ADCCALEN bit. Please refer to the Calibration section for details on the configuration and application of calibration.

IIR Filter

To augment the accuracy performance over multiple measurement cycles, the user can enable the embedded IIR filter.

The filter acts upon all enabled Cn, CSA, and VBLK inputs according to the user defined settings in the MEASUREEN1 register. The TOTAL register does not have a unique IIR filter, but is instead directly computed from the sum of the IIR data registers as selected via RDFILT.

Additionally, when oversampling is enabled, the system response of the measurement data is the combination of the IIR filter and oversampling noise reduction.

Although the IIR filter can be updated dynamically on any individual acquisition via AMENDFILT, it is recommended to always allow non-diagnostic acquisitions into the IIR filter. Using the IIR filter leads to the greatest benefit in noise reduction with the external hardware filter combined with the digital filtering.

Diagnostics (including BALSWDIAG results) or higher noise data from ALTMUXSEL = 1 should not be processed within the IIR as this will corrupt the desired measurement result. This involves (but is not limited to) configuration with the diagnostic current sources (CTSTCFG, MUXDIAGEN), and CSA offset and gain diagnostics (CSATSTEL).

Note: IIR filtering is always applied to measurement cycle during automatic cell balancing. In the event the IIRFC = 111b (off) in automatic cell balancing modes, the IIR filter is internally forced to 000b (1/8). All other selection of IIRFC are valid.

Filter Description

The IIR filter is implemented per the following transfer function, Figure 38:

$$Y(n) = FC \times X(n) + (1-FC) \times Y(n - 1)$$

FC is a 3-bit user-programmable filter coefficient. The default value of 0b010 has a weight of 3/8.

The detailed filter coefficient settings are defined in the IIRFC register. The smaller that coefficient is, the more the history represented by Y(n-1) outputs in the equation. It is a trade-off between response times to change in input value versus the noise attenuation.

The filter can be turned off by setting the filter coefficient to 1 (IIRFC = 0b111). The filter can be temporarily bypassed by setting AMENDFILT = 0; this is useful when performing periodic safety and diagnostic checks, as the filtered main measurement results will be preserved within the filter memory registers. Both filtered and raw result data can be read back using the RDFILT option.

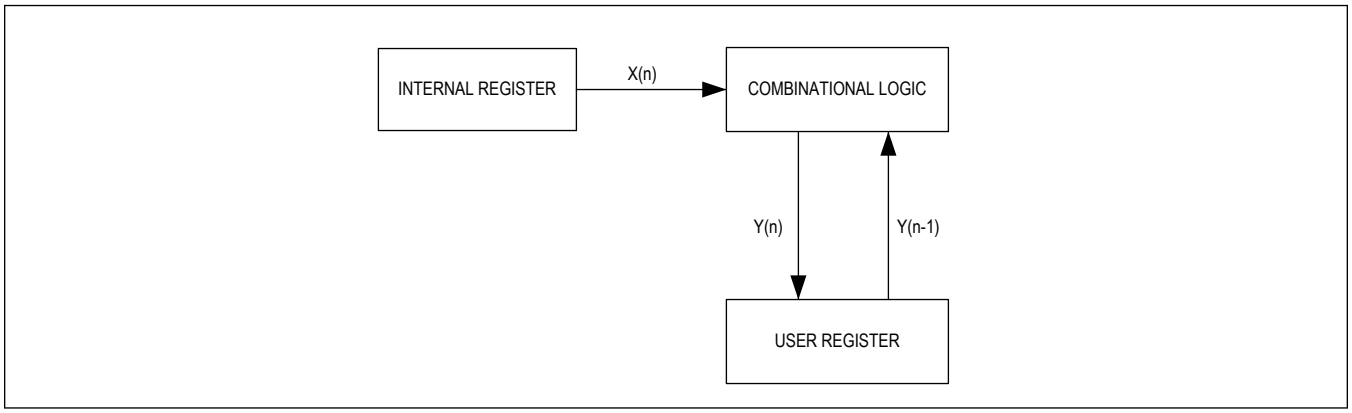


Figure 38. IIR Filter Algorithm

Filter Response

The IIR Filter provides a means to improve measurement noise rejection at a cost of increased settling time. This tradeoff can be managed by selecting the proper IIR Filter Coefficient for the application. Table 27 shows the number of samples taken by the IIR Filter to settle a full scale step (ex. 0V to 100mV Unipolar Cell transition) to 12-Bit and 14-Bit accuracy. Note this settling time can be significantly shortened after power-up, or when operating mode changes will require large step responses by using the MEASUREEN2:SCANIIRINIT or BALCTRL:CBIIRINIT initialization options,

which accelerate settling by loading the next acquired sample into the filter's accumulated result memory.

Table 27. IIR 100mV Step Response Settling

IIRFC SETTING:	0b000	0b001	0b010	0b011	0b100	0b101	0b110	0b111
IIR FILTER COEFFICIENT (FC):	**1/8**	**1/4**	**3/8**	**1/2**	**5/8**	**3/4**	**7/8**	**1**
12-Bit Settling (# Samples):	33	16	10	7	5	4	3	1
14-Bit Settling (# Samples):	44	21	13	9	6	5	3	1

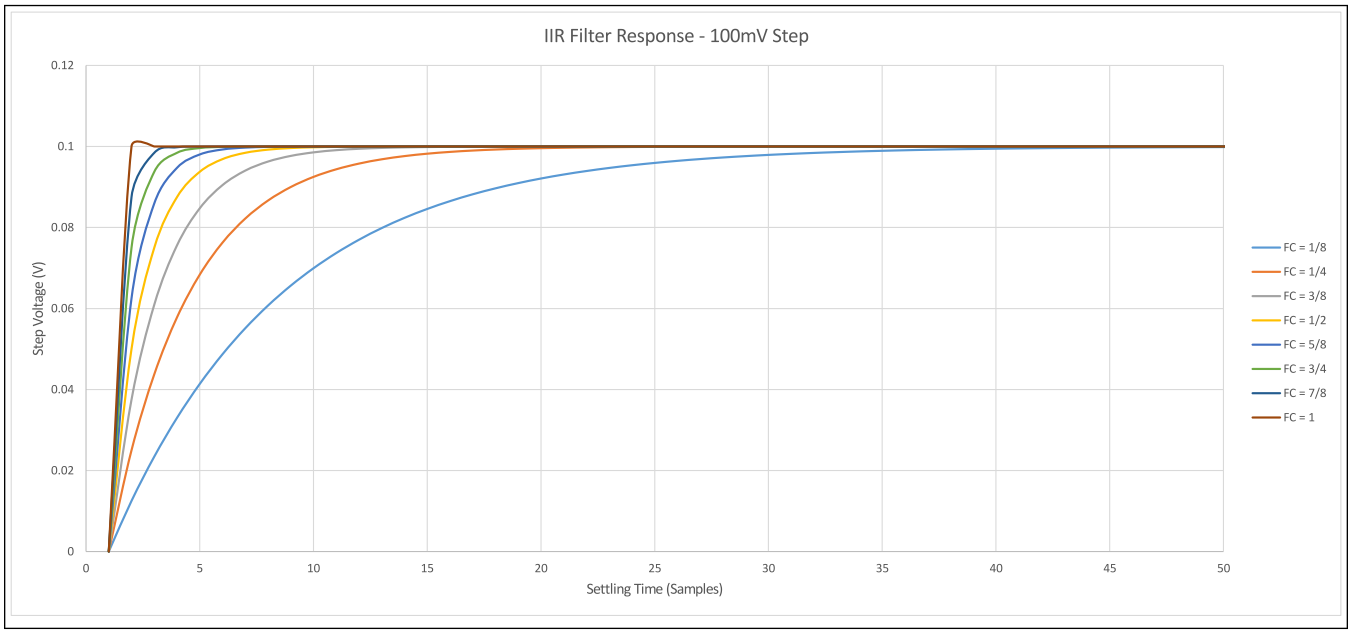


Figure 39. 100mV IIR Step Response

IIR Data Control

The control of ADC data into and around the IIR filter is performed using dedicated register bits (AMDENDFILT, RDFILT, ALRTFILT) in the SCANCTRL register. The following sections detail this operation.

AMENDFILT and RDFILT

The AMENDFILT bit directs the ALU data into the IIR for filtering operations or around the IIR filter to the output data registers (CELLn and BLOCKREG).

When the AMENDFILT bit is deasserted, the ADC acquisition in the ALU is not transferred into the IIR accumulator at the end of the scan sequence. This setting should be used for diagnostic operations which disrupt the input data or for operations which utilize a different measurement path, as both operations would corrupt the normal data. Examples of measurement modes which disrupt the input data are when the cell test current sources or HVMUX test current sources are enabled using the CTSTEN bit and MUXDIAGEN bits respectively. Alternatively, when AMENDFILT is asserted, the ADC acquisition in the ALU is automatically scaled and transferred into the IIR accumulator at the end of the scan sequence.

The RDFILT bit determines if IIR filtered data or normal acquisition data is read from the output data registers is issued (CELLn and BLOCKREG). Please refer to the *Single-Buffer Mode and Double-Buffer Mode* sections for details on how the RDFILT affects data transfer.

Notes:

If DBLBUFEN = 0 and SCAN = 1, the ALU results are loaded into the IIR automatically at the end of the requested measurement sequence.

If DBLBUFEN = 1 and SCAN = 1, the ALU results are loaded into the IIR automatically at the beginning of the following sequence.

If DBLBUFEN = x and SCAN = 0, the ALU results are loaded into the IIR during the requested data move sequence if DATARDY = 0.

Table 28 shows the interactions that can occur between the IIR Data Control Setting:

Table 28. IIR Data-Control Settings

AMENDFILT	RDFILT	USAGE
0	0	IIR Filter Disabled
0	1	Potential Stale Data Fetch IIR is not updated but IIR results read. **Note:** This operation is not recommended.
1	0	Reads Current Unfiltered Acquisition Data: IIR is updated but current acquisition read. Please refer to the *Out-of-Scan Data Transfer* Section for information on reading both filtered and unfiltered results
1	1	IIR Filter Updated and IIR Filter Read

ALRTFILTSEL

When IIR filter operation is enabled, there are two possible data sources for user access, the raw sequencer outputs (oversampling still applies), or the IIR filtered outputs. The Alert Filtering Selection bit, ALRTFILTSEL, is used to select one of these outputs to generate the relevant alerts.

When ALRTFILTSEL = 0, the raw sequencer outputs are used. This data source is used to assert all related alert bit assertions, calculate MINMAXCELL and TOTAL registers, and cell mismatch MSMTCH checks.

When ALRTFILTSEL = 1, the IIR filtered data is used. This IIR data is used to assert all related alert bit assertions, calculate MINMAXCELL and TOTAL registers, and cell mismatch MSMTCH checks.

Regardless of the ALRTFILTSEL settling, DIAG1 and DIAG2 register always come from the unfiltered sequencer outputs.

IIR Initialization

When IIR operation is engaged, the data to be operated upon initially is controlled by the Sequencer IIR Initialization Request bit, SCANIIRINIT.

By default, SCANIIRINIT = 0, IIR filter is in continuation mode. In Continuation mode, the current value in the IIR accumulators is kept (presumably from previous cell measurements) and sequencer measurements are amended normally.

When SCANIIRINIT = 1, IIR filter is in initialization mode. In Initialization mode, the IIR accumulators will be re-initialized to the first measurement taken, and further cell balancing measurements are amended normally.

Single Buffer Mode

The Single Buffer Mode, Figure 40, is activated when DBLBUFEN = 0. In this mode data is moved to the CELLnREG, AUXnREG, BLOCKREG, CSAREG, DIAG1REG, DIAG2REG, TOTALREG, and MINMAXCELL registers at the end of the scan indicated by SCANDONE = 1 and DATARDY = 1.

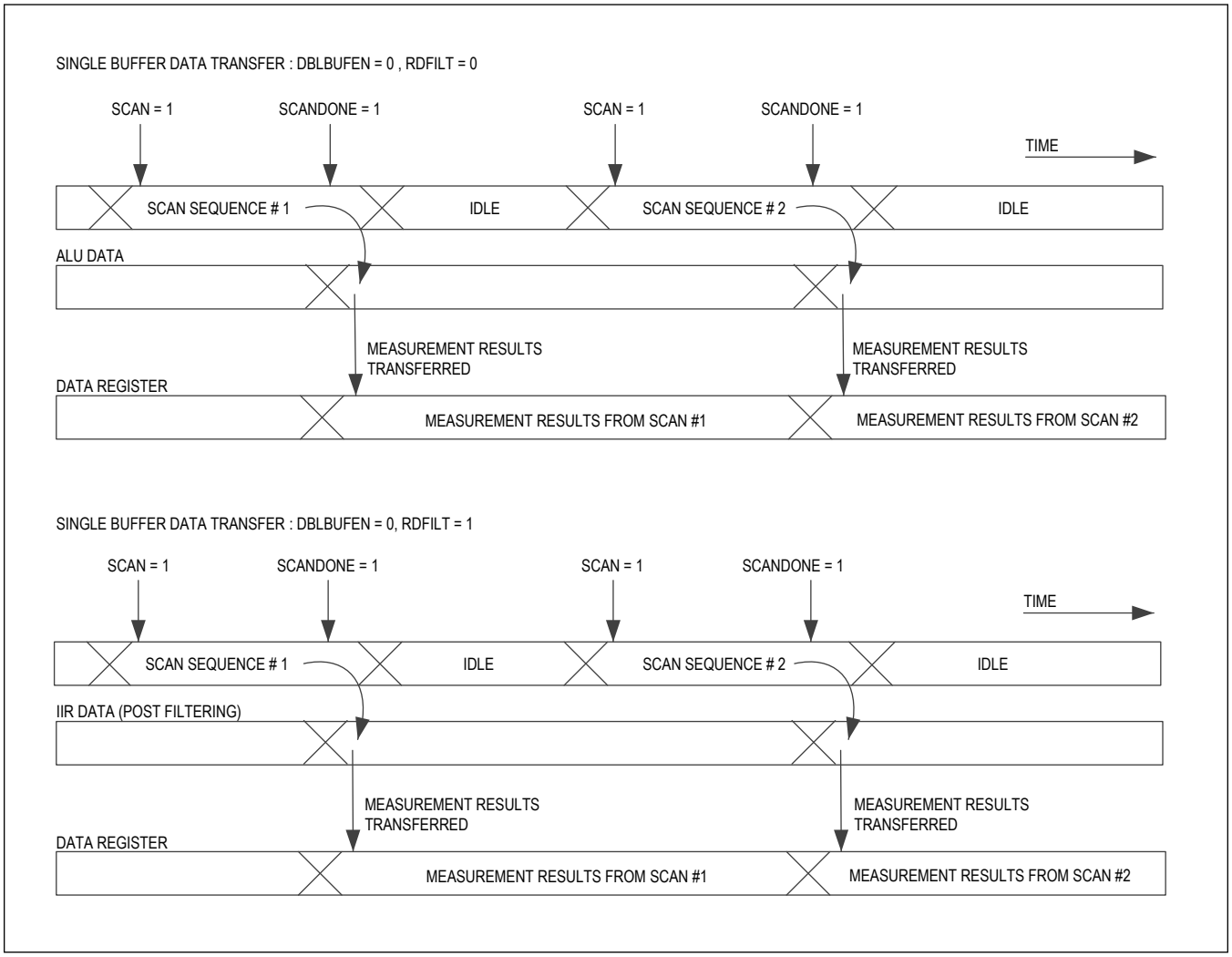


Figure 40. Single-Buffer Data Transfer

Double Buffer Mode

With DBLBUFEN = 1, the Double Buffer Mode, Figure 41, is activated. In this mode, data is moved to the CELLnREG, AUXnREG, BLOCKREG, CSAREG, DIAG1REG, DIAG2REG, TOTALREG, and MINMAXCELL registers at the start of the next scan when SCAN = 1 and is indicated by DATARDY = 1. This allows the host to read data from the last scan while the current scan is in progress. In the event that a final measurement is requested prior to a sleep or shutdown event, the host would need to issue another SCAN request to force the data transfer from the last acquisition or move the data via the Out-of-Scan data transfer method.

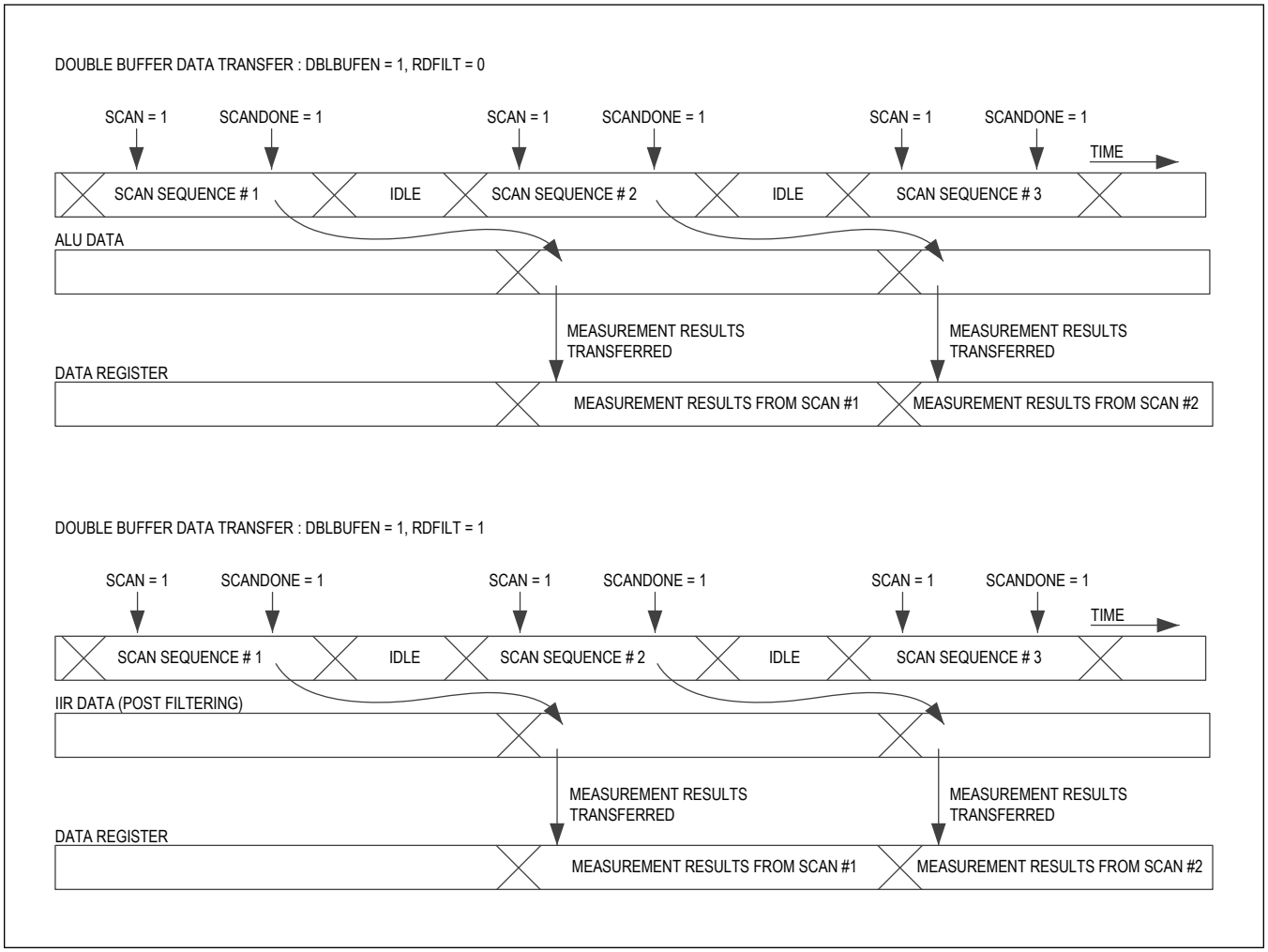


Figure 41. Double-Buffer Data Transfer

Out-of-Scan Data Transfer

Out-of-Scan data transfer occurs in the period after a scan is complete, indicated by SCANDONE = 1, and before a new scan request, SCAN = 1, is issued by the host. Since data exists in both the ALU and IIR accumulator but only one set is transferred to the data registers depending on the RDFILT setting, this procedure allows access to the other set of data that was not transferred to the data registers. By setting DATARDY = 0, RDFILT = 0 and SCAN = 0, data from the ALU is transferred to the data registers. By setting DATARDY = 0, RDFILT = 1 and SCAN = 0, data from the IIR accumulator is transferred to the data registers.

If an Out-of-Scan data transfer is issued, the MINMAXCELL, TOTAL, and MSMTCH registers are not updated when changing RDFILT and SCAN = 0. Additionally, Out-of-Scan alert processing will not be updated when changing ALRTFILTSEL and SCAN = 0. If updated data processing is required a new acquisition (SCAN = 1) must be requested.

Cell Balancing with Embedded Measurement Data Control

The data control for cell balancing with embedded measurements is controlled by the CBSCAN bit in the BALDATA register. This bit acts as a strobe, and the CBSCAN bit content is automatically cleared, reading back a logic zero when polled.

Upon writing CBSCAN (and after any automatic cell-balancing measurement operation in complete), all enabled conversion parameters are updated in the CELLnREG, AUXnREG, BLOCKREG, CSAREG, DIAG1REG, DIAG2REG, TOTALREG, and MINMAXCELL output registers. Refer to the Cell Balancing section for further detail.

Measurement Alerts

After the acquisition, the ALU compares the enabled measurement data to the enabled OV/UV thresholds for both measurement paths (ADC and Comparator) as shown in Table 29. If outside of the configured threshold, the associated alert bit is set during data transfer into the ALU or IIR ALU blocks. In the event that calibration is enabled using the ADCCALEN bit, the digital correction is performed prior to the alert generation. This ensures that the alert is generated from the correct accuracy results.

Note: The ALRTFILTSEL bit for the IIR data control will determine if the alerts will be generated upon filtered or unfiltered data.

The data control settings will impact the management of alert signaling. The aforementioned alert handling details the Single Buffer Mode data control. Since Double Buffered mode allows for simultaneous data offload and acquisition, it is recommended to read alert status after the SCANDONE for the current acquisition and prior to initiating the next acquisition.

Table 29. Measurement Alerts

DESCRIPTION	SIGNAL PATH	CONDITION OR RESULT	ALERT BIT	LOCATION
Cell overvoltage (OV)	ADC	$V_{Cn} - V_{Cn-1} > V_{OVTHSET}$ for POLARITYn=0	ALRTCELLOVST, ALRTADCOVST, ALRTOVn	STATUS1, ALRTSUM, ALRTOVCELL
Cell overvoltage (OV)	COMP	$V_{Cn} - V_{Cn-1} > V_{COMPOVTH}$	ALRTCELLOVST, ALRTADCOVST, ALRTCOMPOVn	STATUS1, ALRTSUM, ALRTCOMPOVREG
Cell undervoltage (UV)	ADC	$V_{Cn} - V_{Cn-1} < V_{UVTHSET}$ for POLARITYn=0	ALRTCELLUVST, ALRTADCUVST, ALRTUVn	STATUS1, ALRTSUM, ALRTUVCELL
Cell undervoltage (UV)	COMP	$V_{Cn} - V_{Cn-1} < V_{COMPUVTH}$	ALRTCELLUVST, ALRTADCUVST, ALRTCOMPUVn	STATUS1, ALRTSUM, ALRTCOMPUVREG
Bipolar cell/bus-bar overvoltage (OV)	ADC only	$V_{Cn} - V_{Cn-1} > V_{BIPOVTHSET}$ for POLARITYn=1	ALRTCELLOVST, ALRTADCOVST, ALRTOVn	STATUS1, ALRTSUM, ALRTOVCELL
Bipolar cell/Bus-bar undervoltage (UV)	ADC only	$V_{Cn} - V_{Cn-1} < V_{BIPUVTHSET}$ for POLARITYn=1	ALRTCELLUVST, ALRTADCUVST, ALRTUVn	STATUS1, ALRTSUM, ALRTUVCELL
Block overvoltage (OV)	ADC only	$V_{BLK} > V_{BLKOVTHSET}$	ALRTBLKOV	STATUS1
Block undervoltage (UV)	ADC only	$V_{BLK} < V_{BLKUVTHSET}$	ALRTBLKUV	STATUS1
Cell Mismatch	ADC only	$V_{MAX} - V_{MIN} > V_{MSMTCH}$	ALRTMSMTCH	STATUS1
Cell with minimum voltage	ADC only	n where $V_{CELLn} = V_{MIN}$ Unipolar if MINMAXPOL=0 else Bipolar	None	MINMAXCELL
Cell with maximum voltage	ADC only	n where $V_{CELLn} = V_{MAX}$ Unipolar if MINMAXPOL=0 else Bipolar	None	MINMAXCELL
Total of all Cell and CSA voltage	ADC only	$\Sigma V_{CELLn} + V_{CSA}$ for n = 1 to TOPCELL1/2	None	TOTAL

Table 29. Measurement Alerts (continued)

DESCRIPTION	SIGNAL PATH	CONDITION OR RESULT	ALERT BIT	LOCATION
AUXINn overvoltage (undertemperature)	ADC	V_{AUXINn} > ($V_{AUXROVTHSET}$ or $V_{AUXAOVTHSET}$)	ALRTAUXOVST, ALRTADCAUXOVST, ALRTAUXOVn	STATUS1, ALRTSUM, ALRTAUXOV
AUXINn overvoltage (undertemperature)	COMP	V_{AUXINn} > ($V_{COMPAUXROVTH}$ or $V_{COMPAUXAOVTH}$)	ALRTAUXOVST, ALRTCOMPAUXOVST, ALRTCOMPAUCOVn	STATUS1, ALRTSUM, ALRTCOMPAUXOV
AUXINn undervoltage (overtemperature)	ADC	V_{AUXINn} < ($V_{AUXRUVTHSET}$ or $V_{AUXAUVTHSET}$)	ALRTAUXUVST, ALRTADCAUXUVST, ALRTAUXUVn	STATUS1, ALRTSUM, ALRTAUXUV
AUXINn undervoltage (overtemperature)	COMP	V_{AUXINn} < ($V_{COMPAUXRUVTH}$ or $V_{COMPAUXAUVTH}$)	ALRTAUXUVST, ALRTCOMPAUXUVST, ALRTCOMPAUCUVn	STATUS1, ALRTSUM, ALRTCOMPAUXUV

Voltage Alerts

The ALRTOVEN and ALRTUVEN registers are configured to enable voltage alerts for the Cell, Block, and CSA inputs. These alerts have programmable OV and UV set thresholds as well as programmable OV and UV clear thresholds allowing for programmable hysteresis in both OV or UV measurements as mentioned in below Table 30. This is beneficial for the programming of alert detection in lithium-ion cells where the characteristics are different at fully charged and discharged states.

Overvoltage alerts in the ALRTOVCELL or ALRTCOMPOVREG registers are set when the CELLn voltage exceeds the programmed threshold voltages $V_{OVTHSET}$ and $V_{COMPOVTH}$, respectively. Alternatively, undervoltage alerts in the ALRTUVCELL and ALRTCOMPUVREG registers are set when the CELLn voltage exceeds the programmed threshold voltage $V_{UVTHSET}$ and $V_{COMPUVTH}$, respectively. It is important to note that due to the different resolutions of the ADC and Comparator (described in the ADC Input Range section and Comparator Input Range section) the user may experience a condition where the alert for the ADC may be set while the alert for the comparator my be cleared and vice-versa.

Note: ADC alerts will provide the most accurate indications of the acquisition.

Alerts are cleared when the cell voltage moves in the opposite direction and crosses the OVTHCLR, COMPOVTH and UVTHCLR, COMPUVTH thresholds. The voltage must cross the threshold; if it is equal to a threshold, the alert flag does not change. Therefore, setting the overvoltage set threshold to full-scale, or setting the undervoltage set threshold to zero-scale, effectively disables voltage alerts independent of the ALRTOVEN and ALRTUVEN.

Table 30. Set- and Clear-Threshold Selection

DESCRIPTION	SIGNAL PATH	OVERVOLTAGE THRESHOLD	UNDERVOLTAGE THRESHOLD	OV HYSTERESIS	UV HYSTERESIS
Cell	ADC	OVTHSET	UVTHSET	OVTHCLR	UVTHCLR
Cell	COMP	COMPOVTH	COMPUVTH	Not Applicable	Not Applicable
Bus bar	ADC	BIPOVTHSET	BIPUVTHSET	BIPOVTHCLR	BIPUVTHCLR
Block	ADC	BLKOVTHSET	BLKUVTHSET	BLKOVTHCLR	BLKUVTHCLR

Alert conditions for the individual ADC Cell inputs are summarized using the ALRTADCOVST and ALRTADCUVST bits in the ALRTSUM register and occur when any alert bit is set in the ALRTOVCELL or ALRTUVCELL registers, respectively. Similarly, alert conditions for the individual Comparator Cell inputs are set using the ALRTCOMPOVST and ALRTCOMPUVST bits in the ALRTSUM register when any alert bit is set in the ALRTCOMPOVREG or ALRTCOMPUVREG registers, respectively. To ease identification of any OV or UV alerts, both ADC summary alerts and Comparator summary alerts are further logically OR'ed and summarized in the ALRTCELLOVST and ALRTCELLUVST bits in the STATUS1. This enables the alert information to get propagated using the hardware alert interface or the data

check byte.

Alert conditions for the Block input are directly summarized using the ALRTBLKOVST and ALRTBLKUVST bits in the STATUS1 register when the acquired BLOCK voltage is over $V_{BLKOVTHSET}$ or under $V_{BLKUVTHSET}$ respectively.

If an alert does not need to be propagated using the alert interface or data check byte, these can be individually masked. Please refer to the Alert interface for further details on the masking.

The cell and block voltage hysteresis diagram is as shown in below Figure 42.

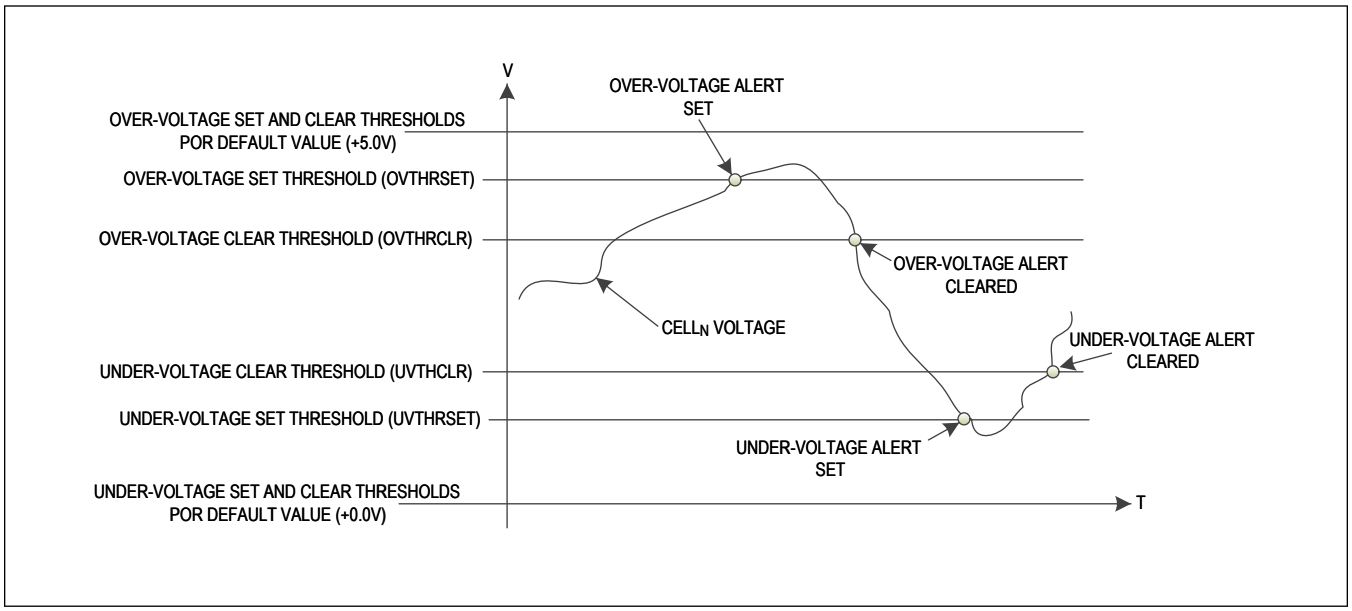


Figure 42. Cell Voltage-Alert Thresholds

Cell Mismatch

Enable the mismatch alert to signal when the minimum and maximum cell voltages differ by more than a specified voltage. The MSMTCHREG register sets the 14-bit threshold ($V_{MSMTCHREG}$) for the mismatch alert, ALRTMSMTCH. Whenever V_{MAX} - V_{MIN} > $V_{MSMTCHREG}$, then ALRTMSMTCH = 1. The alert bit will be cleared when a new acquisition does not exceed the threshold condition. To disable the alert, write 3FFFh to the MSMTCHREG register bitfield (default value).

Cell Statistics

The cell numbers corresponding to the lowest and highest enabled voltage measurements are stored in the MINCELL, MAXCELL bitfields. When multiple cells have the same minimum or same maximum voltage, only the lowest cell position having that voltage is reported. For acquisitions with no enabled cell inputs, the MINCELL MAXCELL and TOTAL bitfields are not updated.

The RDFILT bit determines the source data (filtered/unfiltered) used for MINCELL, MAXCELL bitfields and TOTALREG (x56) register.

The MINMAXPOL bit ensures that only like measurements are used for the statistical processing of MINCELL, MAXCELL and ALRTMSMTCH. This ensures that bus bars do not affect the cell statistics in mixed mode acquisitions. When MINMAXPOL = 0 only unipolar measurements are used. When MINMAXPOL = 0b1, only bipolar measurements are used. upon unipolar or bipolar measurement.

Note: For lithium-ion applications MINMAXPOL should be configured for unipolar statistics, while fuel cell application should be configured for bipolar statistics.

The sum of all enabled cell voltages, regardless of the POLARITY configuration, will be stored in the TOTAL register as a 16-bit value.

Example:

Assume four cell inputs are enabled CELL1, CELL2, CELL3, CELL4 where CELL1, CELL2 are configured as unipolar, CELL3 is bipolar and CELL4 as unipolar. The measured values after the acquisition reads 2V, 2V, -1V, and 2.5V, respectively.

The TOTALREG register reads:

TOTAL = 2 + 2 - 1 + 2.5 = 5.5 V

The MINCELL bitfield will read CELL1 and the MAXCELL bitfield will read CELL4.

Temperature Alerts

The ALRTAUXOVEN and ALRTAUXUVEN registers are configured to enable the temperature alerts for the enabled AUXn inputs. Like the cell-voltage alerts, the temperature alerts have programmable OV and UV set thresholds as well as programmable OV and UV clear thresholds to provide user programmable hysteresis to avoid unwanted alerts in the presence of measurement noise as shown in Table 31.

Table 31. Temperature Alert Threshold

DESCRIPTION	SIGNAL PATH	TYPE	OVERVOLTAGE THRESHOLD/UNDER TEMPERATURE	UNDERVOLTAGE THRESHOLD/OVER TEMPERATURE	HYSTERESIS OV	HYSTERESIS UV
AUXINn	ADC	Ratio metric	AUXROVTHSET	AUXRUVTHSET	AUXROVTHCLR	AUXRUVTHCLR
AUXINn	ADC	Absolute	AUXAOVTHSET	AUXAUVTHSET	AUXAOVTHCLR	AUXAUVTHCLR
AUXINn	COMP	Ratiometric	COMPAUXROVTH	COMPAUXRUVTH	Not Applicable	Not Applicable
AUXINn	COMP	Absolute	COMPAUXAOVTH	COMPAUXAUVTH	Not Applicable	Not Applicable

Overvoltage alerts in the ALRTAUXOV or ALRTCOMPAUXOV registers are set when the AUXn voltage exceeds the programmed threshold voltages of $V_{AUXAOVTHSET}$ OR $V_{AUXROVTHSET}$ and $V_{COMPAUXAOVTH}$ OR $V_{COMPAUXROVTH}$, respectively. The appropriate threshold used will be determined by the AUXREFSEL bits which can be different per channel. Alternatively, undervoltage alerts in the ALRTAUXUVREG and ALRTCOMPAUXUVREG registers are set when the AUXn voltage exceeds the programmed threshold voltage $V_{AUXUVTHSET}$ OR $V_{AUXRUVTHSET}$ and $V_{COMPAUXRUVTH}$ OR $V_{COMPAUXAUVTH}$, respectively. It is important to note that due to the different resolutions of the ADC and Comparator (described in the ADC Input Range section and Comparator Input Range section) the user may experience a condition where the alert for the ADC may be set while the alert for the comparator may be cleared, and vice-versa.

Note: An OV alert for the ratiometric acquisition will signal an undertemperature (UT) event for the NTC measurement and a UV alert will signal an overtemperature (OT) event for the NTC measurement.

Alerts are cleared when the cell voltage moves in the opposite direction and crosses the AUXROVTHCLR, AUXAOVTHCLR and AUXRUVTHCLR, AUXAUVTHCLR thresholds. The voltage must cross the threshold; if it is equal to a threshold, the alert flag does not change. Therefore, setting the overvoltage set threshold to full-scale, or setting the undervoltage set threshold to zero-scale, effectively disables voltage alerts independent of the ALRTAUXOVEN and ALRTAUXUVEN.

Alert conditions for the individual ADC auxiliary inputs are summarized using the ALRTADCAUXOVST and ALRTADCAUXUVST bits in the ALRTSUM register and occur when any alert bit is set in the ALRTAUXOV or ALRTAUXUV bitfields, respectively.

Note: The ALRTSUM alert status does not specify the auxiliary input measurement mode in AUXREFSEL; however, this can be determined from polling the alert channel within ALRTAUXOV or ALRTAUXUV.

Similarly, alert conditions for the individual Comparator auxiliary inputs are set using the ALRTCOMPAUXOV and ALRTCOMPAUXUV bits in the ALRTSUM register when any alert bit is set in the ALRTCOMPAUXOVSTREG or

ALRTCOMPAUXUVREG registers, respectively.

To ease identification of any OV or UV alerts, both ADC summary alerts and Comparator summary alerts are further logically OR'ed and summarized in the ALRTAUXOVST and ALRTAUXUVST bits in the STATUS1. This enables the alert information to get propagated using the hardware alert interface or the data check byte.

Cell Balancing

Cell balancing may be performed using any combination of the 14 internal cell balancing switches according to the programming of the enabled BALSWCTRL:BALSWEN configuration and POLARITYCTRL configuration. Each configured channel will perform cell balancing according to the configured operational mode which includes manual or automatic balancing, discharge control using a timer and/or undervoltage threshold, as well as duty-cycle configuration.

Cell Balancing Mode Configurations

Cell balancing is initiated using the CBMODE bits in the BALCTRL register. This selection defines automatic versus manual balancing control, channel timer configuration, and timer resolution. Once a CBMODE mode is selected and started, the device remains in this mode until a new value is written to CBMODE, or until a successful exit criteria is achieved from all enabled conditions (UV threshold, timer, and thermal).

To determine the current state of cell balancing, the CBACTIVE bits can be polled using the BALCTRL, BALSTAT or BALUVSTAT registers. The current timer value can be read via CBTIMER, and a 1Hz alive counter can be read via CBCNTR. The timer units (i.e. second, minute, hour) can be read via CBUINT. These status registers are only cleared when CBMODE is written to a new mode or disabled. The combination of these bitfields allows for user verification that the cell balancing machine is responsive; meanwhile, an internal health check is performed prior to verify hardware integrity prior to balancing. ALRTCBTIMEOUT notifies the user of a health check failure (if one is found).

Once a CBMODE mode is selected and started, the device remains in this mode until a new value is written to CBMODE. Note that all CBMODE active operations automatically end due to either timer expiration(s), thermal faults, and/or Cell UV thresholds being met. In these cases, the CBMODE is still engaged although the balancing operation is ended - the status of the operation can be checked by reading the BALSTAT and BALUVSTAT registers.

After cell balancing is initiated, write access to specific cell balancing registers will be blocked; if a write to a blocked register is attemped, it will be ignored and the ALRTRJCT flag will be set in the STATUS2 register. See the Table 32 for specific register behavior. Note that blockage operations are implemented at the register level.

Table 32. Cell-Balancing Register Write Behavior when Cell Balancing is Selected

REGISTER	BITFEILD	AUTO (INDIVIDUAL OR GROUP) MODE (1xx)			MANUAL MODE (01x)			EMERGENCY DISCHARGE MODE (001)		
		Data applicable in this mode?	Write accepted in this mode?	ALRT-RJCT Status	Data applicable in this mode?	Write accepted in this mode?	ALRT-RJCT Status	Data applicable in this mode?	Write accepted in this mode?	ALRT-RJCT Status
BALSWCTRL	CBRESTART	No	No	1	Yes	Yes	-	No	Yes	-
	BALSWEN	Yes	No		Yes	Yes		No	Yes	
BALEXP1	BALEXP1	Yes	No	1	Yes	No	1	Yes	No	1
BALEXP2-14	BALEXP2-14	Yes	No	1	No	Yes	-	No	Yes	-
BALAUTOUVTHR	CBUVTHR	Yes	No	1	No	Yes	-	No	Yes	-
	CBUVMINCELL	Yes	No		No	Yes		No	Yes	
BALDLYCTRL	CBNTFYCFG	Yes	No	1	No	Yes	-	Yes	No	1
	CBCALDLY	Yes	No		No	Yes		Yes	No	

Notes: The CBRESTART is a strobe bit to manually restart/refresh the watchdog timer during Manual Mode Cell Balancing operation. Although this can be written in other balancing modes, no internal action is taken.

Writes to the BALSWEN bitfields during Manual Cell Balancing Mode are expected and supported.

Writes to BALAUTOUVTHR with CBUVMINCELL = 1 will be rejected if a measurement scan is in progress (since data from the last completed scan is used to populate CBUVTHR).

Any value (re)writen to CBMODE other than 000 (Disable) will restart the CBTIMER at zero and (re)launch the requested mode of operation.

Manual Mode

In Manual mode, Balance Switches (BALSWn) are controlled directly by BALSWEN[14:1] with a watchdog timeout set by CBEXP1 as follows:

BALSWn = BALSWEN[n] & (CBTIMER ≤ CBEXP1) & ~(AUTOBALSWDIS & measurement in progress)

CBTIMER is incremented on a real time basis, regardless of BALSWEN settings or suspensions for ADC or CAL events. This means the watchdog will time out as set in CBEXP1 once manual cell balancing is initiated.

Manual cell balancing operations can be temporarily suspended during measurements using the AUTOBALSWDIS feature.

In certain instances as defined by the AUTOBALSWDIS operation or other manual diagnostic operation, the user may wish to have explicit control of the BALSWEN without the desire to refresh the CBTIMER watchdog. In this case, the user can configure CBEXP1 = 3FFh to disable the timer. Thus, balancing will be controlled only using the BALSWEN; this is also equivalent to the cell balancing behavior supported in Maxim legacy battery management devices.

CBRESTART is provided as a means to refresh the active balancing switches or the watchdog timer during normal BALSWn cycling operations. CBUVTHR exit settings are ignored, measurements and calibrations operations are requested via normal scan control registers allowing for simultaneous measurements and balancing.

Notes:

Writing 1 to CBRESTART after cell balancing timer expiration has no effect. To perform another manual mode cell balancing event, user must issue a separate write to BALCTRL register.

Manual balancing allows for adjacent balancing switches to turn on simultaneously according to the application requirement. Enabling adjacent balancing switches simultaneously under manual cell balancing modes will increase the balancing current significantly so care must be taken to not exceed the device's maximum operating conditions.

AUTOBALSWDIS Feature

Configuring AUTOBALSWDIS = 1 will automatically disable the balancing switches (in manual cell balancing modes only) during measurements to eliminate the additional voltage drop caused due to cell balancing application circuit and will provide enhanced balancing performance during vehicle operation . This ultimately allows the system to achieve higher accuracy cell measurements to help calculate higher accuracy of State of Charge (SoC).

Measurement settling time control for cell measurement (CELLDLY) and BALSW diagnostic/ALTMUX (SWDLY) is configured in the BALSWDLY register. These delay registers provides programmable settling (wait) times from 0 µs up to 24.57 ms, in steps of 96 µs, between the time when the acquisition is enabled and the start of actual measurement to allow for the external application circuit to settle to accurate voltages. In the BALSWDLY register, CELLDLY is the upper 8-bit delay setting for cell recovery time while SWDLY is the lower delay setting for certain diagnostics such as sense wire open. When AUTOBALSWDIS = 1 and ALTMUXSEL = 0, CELLDLY is selected. When AUTOBALSWDIS = 1 and ALTMUXSEL sets to 1, SWDLY is selected. Hence, this feature can be used during normal cell measurements as well as during diagnostic measurements with two separate delay timers which can be independently set. Any write to the BALSWDLY register will be ignored, signaled by ALRTRJCT, while a Measurement Sequence or an Auto Cell Balancing mode is active.

Note: The appropriate delay time is dependent on the application circuit and the level of accuracy required. For the typical application circuit on the Cell input, utilizing a input filter network of 1 kΩ and 0.1 µF, it is recommended to choose a settling time of 960 µs to achieve calibrated accuracy specified in the *Electrical Characteristics* table.

Note: AUTOBALSWDIS effects Cell Balancing Switch behavior in manual cell balancing modes only.

Note: Cell Balancing Timer incrementing/expiration behavior is not effected by AUTOBALSWDIS setting.

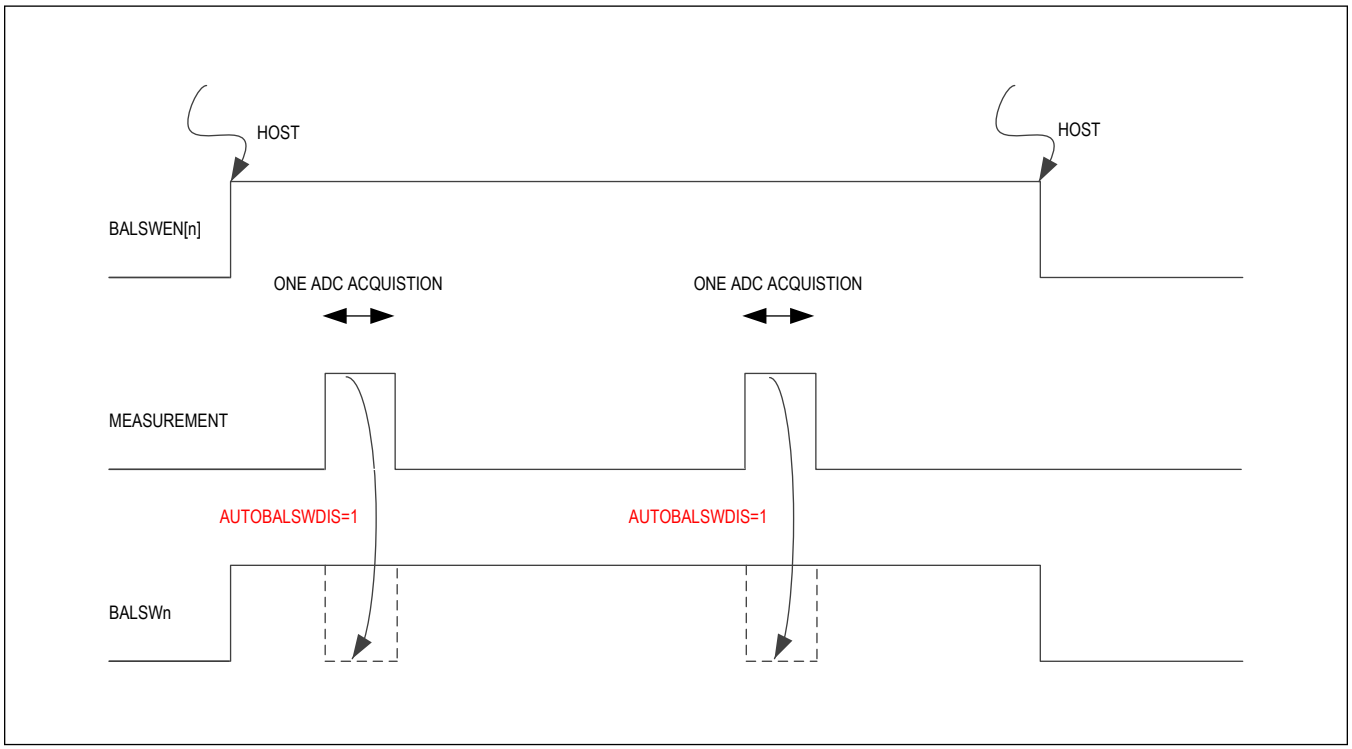


Figure 43. Logic Diagram when Balancing Switches Will be Disabled

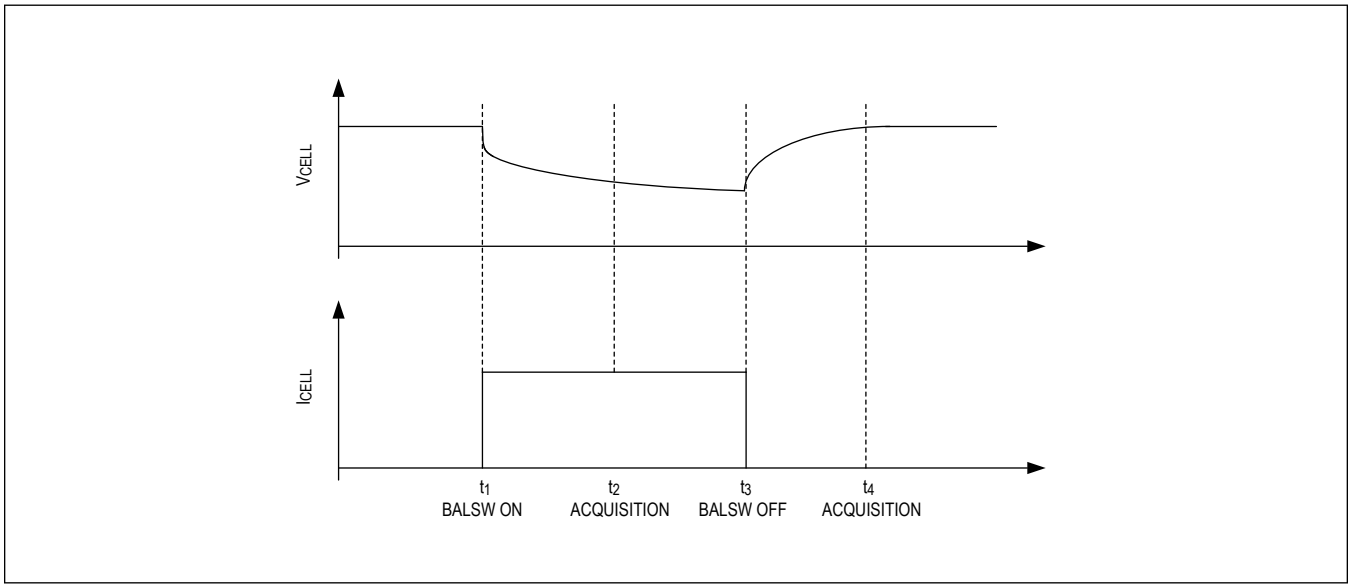


Figure 44. AUTOBALSWDIS Measurement Settling

Manual Cell Balancing Mode with FlexPack

During manual cell balancing, the top two consecutive cells should not be enabled for manual cell balancing. This creates a situation where $SW_{TOPCELL1/2}$,$SW_{TOPCELL1/2-1}$, $SW_{TOPCELL1/2-2}$ could potentially all be 5V below the TOPCELL1/2 cell input voltage. Although the MAX17852 digital logic will not prevent user from using such a configuration, the ALRTHVUV is expected to trip and the TOPCELL1/2 cell input measurements will not be valid.

Auto Individual Mode

The Auto Individual Mode performs cell balancing in a controlled manner so that the cells can be individually discharged for a duration and/or to a specific voltage level, as required in the end application. The host initiates Auto Individual Mode by setting CBMODE to 0b100 (duration is seconds) or 0b101 (duration in minutes), configuring CBEXPn to the desired value (where the LSB = 1 second or minute, respectively), and setting individual BALSWENn bits, a group voltage target can also be set using CBUVTHR.

In Auto Individual Mode, the balancing switches defined by BALSWEN[n] are automaticly controlled via non-overlapping Even/Odd cycling in accordance with the programmable timer duration (CBEXPn) and/or the undervoltage threshold (CBUVTHR). The balancing switch duty cycle can further be controlled using CBDUTY to programmatically set the average balancing current. This is indicated as below:

Even Cells (2, 4, ... 14):

BALSWn = BALSWEN[n] & (CBTIMER ≤ CBEXPn) & CBEVEN & (((CBMEASEN == 0b11) & (CELLn ≥ CBUVTHR)) | (CBMEASEN != 0b11))

Odd Cells (1, 3, ... 13):

BALSWn = BALSWEN[n] & (CBTIMER ≤ CBEXPn) & CBODD & (((CBMEASEN == 0b11) & (CELLn ≥ CBUVTHR)) | (CBMEASEN != 0b11))

CBUVTHR exit settings apply, and ADC measurement and calibration operations can be performed, if enabled, to support host controller read back.

CBTIMER is incremented on a duty-cycled basis indicating the time each channel is subject to discharge (i.e. one T_{CBEO} cycle out of each E/O/M discharge cycle). This means that in real time, the discharge operation will always run at least 2x the maximum value set in CBEXPn. As an example, if both an even and odd cell must be balanced for 1 hour and the CBDUTY = 100%, the associated timers would be set accordingly and the operation would last for ~2 hours (accounting for non-overlap timing). If the CBDUTY is now set to 50% with the same timer settings, the total operation time would extend to ~4 hours.

The read-only counter CBCNTR increments at a 1 Hz rate with periodic roll-over at 0b11. The host can read this counter periodically to confirm the auto individual mode is active.

SHDNL operation can be controlled by HOLDSHDNL, preventing device shutdown during auto individual mode in case of an extended lapse in host communication.

Once initiated, Auto Individual Mode will normally continue to run until CBTIMER reaches max(CBEXPn) or all Cells reach the voltage CBUVTHR (whichever comes first, depending on configuration settings), at this point, balancing switch operations will cease and CBACTIVE will be set to 0b10, indicating a normal exit condition. Cell balancing checks for thermal, calibration, and watchdog faults apply if enabled; if any of these conditions occur, switching activity will be halted immediately and CBACTIVE will be set to 0b11, notifying the µC of the result. The cell-balancing timer (CBTIMER) continues to run until expiration (CBEXPn), and HOLDSHDNL extensions are supported (if enabled). This allows the µC to confirm the exit condition.

Auto Group Mode

The Auto Group Mode performs cell balancing in a controlled manner so that the cells can be discharged as a group for a duration and/or to a specific voltage level, as required in the end application. The host initiates an Auto Group Mode by setting CBMODE to 0b110 (duration is seconds) or 0b111 (duration in minutes), configuring CBEXP1 to the desired value (where the LSB = 1 second or minute, respectively), and setting individual BALSWENn bits, a group voltage target can also be set using CBUVTHR.

In Auto Group Mode, the balancing switches defined by BALSWEN[n] are automatic controlled via non-overlapping Even/Odd cycling in accordance with the programmable timer duration (CBEXP1) and/or the under voltage threshold (CBUVTHR). The balancing switch duty cycle can further be controlled using CBDUTY to programmatically set the average balancing current. This is indicated as below:

Even Cells (2, 4, ... 14):

BALSWn = BALSWEN[n] & (CBTIMER ≤ CBEXP1) & CBEVEN & (((CBMEASEN ==0b11) & (CELLn ≥ CBUVTHR)) | (CBMEASEN != 0b11))

Odd Cells (1, 3, ... 13):

BALSWn = BALSWEN[n] & (CBTIMER ≤ CBEXP1) & CBODD & (((CBMEASEN ==0b11) & (CELLn ≥ CBUVTHR)) | (CBMEASEN != 0b11))

Auto Group Modes are identical to Auto Individual Modes except all timer durations are checked against CBEXP1 (a single expiration event).

Emergency Discharge Mode

The Emergency Discharge Mode performs cell balancing in a controlled manner so that the cells can be discharged in the event of an emergency or battery end-of-life.

The host initiates the emergency discharge mode by setting CBMODE to 0b001 and configures CBEXP1 to the desired value (where the LSB = 1 hour). After emergency discharge mode is activated, battery cells are discharged until CBTIMER expires or CBMODE is set to 0b000 (disabled).

In Emergency Discharge Mode, all Balance Switches (BALSWn) are enabled regardless of BALSWEN[n] settings, with a CBTIMER duration set by CBEXP1, and are governed by non-overlapping Even/Odd cycling, as follows:

Even Cells (2, 4, ... 14):

BALSWn = (CBTIMER ≤ CBEXP1) & CBEVEN

Odd Cells (1, 3, ... 13):

BALSWn = (CBTIMER ≤ CBEXP1) & CBODD

CBUVTHR exit settings do not apply, but ADC measurement and calibration operations can still performed if enabled to support host controller read back.

CBTIMER is incremented on a duty-cycled basis indicating the time each channel is subject to discharge (i.e. one T_{CBEO} cycle out of each E/O/M discharge cycle). This means in real time, the discharge operation will always run at least 2x the maximum value set in CBEXP1. As an example, if both an even and odd cell must be balanced for 1 hour and the CBDUTY = 100%, the associated timers would be set to 0x3C and the operation would last for ~2 hours (accounting for non-overlap timing). If the CBDUTY is set to 50% with the same timer setting, the total operation time would extend to ~4hours.

The read-only counter CBCNTR increments at a 1 Hz rate with periodic roll-over at 0b11. The host can read this counter periodically to confirm the emergency discharge mode is active.

SHDNL operation can be controlled by HOLDSHDNL, preventing device shutdown during emergency discharge mode due to the extended lapse in host communication.

Once initiated, Emergency Discharge mode will normally continue to run until CBTIMER reaches CBEXP1, at this point, balancing switch operations will cease and CBACTIVE will be set to 0b10, indicating a normal exit condition. Cell balancing checks for thermal, calibration, and watchdog faults apply if enabled; if any of these conditions occur, switching activity will be halted immediately and CBACTIVE will be set to 0b11, notifying the µC of the result. The cell-balancing timer (CBTIMER) continues to run until expiration (CBEXPn), and HOLDSHDNL extensions are supported (if enabled). This allows the µC to confirm the abnormal exit condition.

Cell-Balancing Modes Summary

Table 33 summarizes the Cell-Balancing Modes supported by the MAX17852.

Table 33. Cell-Balancing Mode

CBMODE[2:0]	DESCRIPTION	CBEXPn[9:0]	TIMER RESOLUTION	TCBEO	RRANGE OF CBEXPn[9:0]	
					MINIMUM	MAXIMUM
000b	Cell Balancing Disabled	000h	-	-	-	
001b	Emergency/EOL Discharge by Hour	001h - 3FFh	1 hr	0.5 min	1 hr	1022 hr
010b	Manual Cell Balancing by Second	001h - 3FFh	1 s		1 s	1022 s
011b	Manual Cell Balancing by Minute	001h - 3FFh	1 min		1 min	1022 min
100b	Auto Individual Cell Balancing by Second	001h - 3FFh	1 s	0.5 s	1 s	1022 s
101b	Auto Individual Cell Balancing by Minute	001h - 3FFh	1 min	0.5 min	1 min	1022 min
110b	Auto Group Cell Balancing by Second	001h - 3FFh	1 s	0.5 s	1 s	1022 s
111b	Auto Group Cell Balancing by Minute	001h - 3FFh	1 min	0.5 min	1 min	1022 min

Note: T_{CBEO} is the effective time that the even or odd switches are balanced within the timer resolutions

Auto Even-Odd Cell Balancing

Auto even-odd cell balancing will control the enabling of adjacent balancing switches automatically with timing resolution from 1 second to 1 hour depending on the CBMODE configuration. This ensures that only even or odd switches are not enabled simultaneously, while balancing equally within the balancing period. This allows the host to program the BALSWEN bit once without having adjust the balance switches or timer period which can be beneficial during system low power operational modes where the host controller is asleep.

In order to prevent simultaneous channel conduction, a non-overlap period ($T_{NONOVERLAP}$ = 1 µs) is inserted between disabling one switch and enabling the adjacent switch. When the UV threshold is disabled, the total cell-balancing period is (t_{CBEO} + $t_{NONOVERLAP}$) x 2. When the UV threshold is enabled, the cell-balancing period is increased by the ADC measurement time ($t_{MEASUREMENT}$). In this case, the total cell-balancing period is (t_{CBEO} + $t_{NONOVERLAP}$) x 2 + $t_{MEASUREMENT}$.

Note: t_{CBEO} = 1/2 x Timer Resolution

The measurement time ($t_{MEASUREMENT}$) includes the cell-balancing path recovery delay selection (CELLDLY), a user-programmable delay determined by the external application circuit that is imposed after each pair of even and odd discharge cycles. The other component of the measurement time includes the physical time for ADC acquisition as defined in the SCANCTRL register (OVSAMPL in cell-balancing mode is non-programmable and fixed at 16 to ensure the highest accuracy measurements).

Note: CELLDLY is used in Manual Cell-Balancing mode when using AUTOBALSWDIS = 0b1 and ALTMUXSEL = 0b0. It is also used in Automatic Cell Balancing and Discharge modes after each pair of Even and Odd discharge cycles.

CBMODE = 0x4, CBUVTHR = 0x3FF

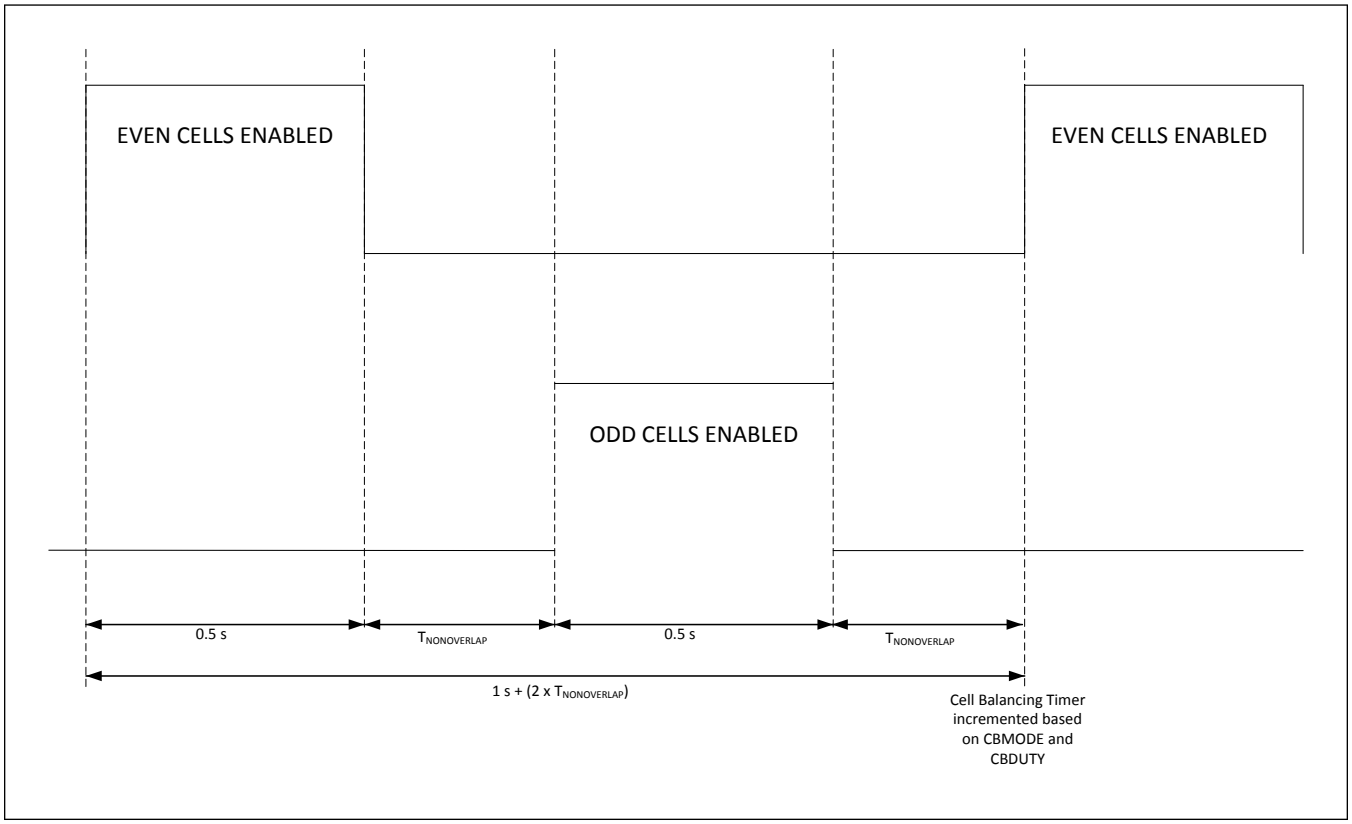


Figure 45. Auto Even and Odd Cell Balancing without UV Detection

CMODE = 5h, FLXPCKEN1/2 = 1, TOPCELL1/2 = ODD

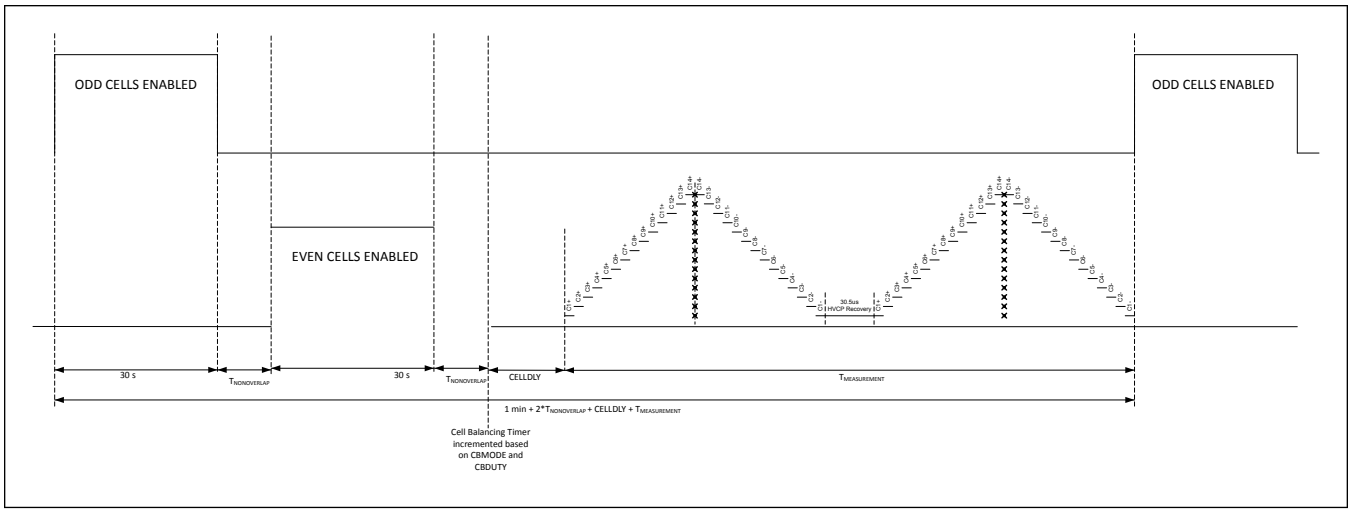


Figure 46. Auto Even Odd Cell Balancing with UV Detection, ADC with OVSAMPL

Note: Figure 45 and Figure 46 are not drawn to exact timescale. Some sections have been exaggerated for visibility.

See the *Cell-Balancing UV Detection* section for further details and recommendation for embedded measurements during cell balancing.

Cell-Balancing Timer CBTIMER

Manual, Emergency Discharge, and Auto Group Mode Timing: In Manual, Emergency Discharge, and Auto Group modes, the CBEXP1 bitfield within the BALEXP1 register is used as the cell-balancing timer duration setting. The duration can be configured from 1-1023 seconds, from 1-1023 minutes, or from 1-1023 hours depending on the CBMODE setting (LSB = hour, minute, or second). A value of 0x3FF will allow the switches to be enabled indefinitely for CELLn if BALSWENn is also enabled (CBTIMER will be active, and will roll over at 3FFh, but is not checked against CBEXP1). In Manual, Emergency Discharge, and Auto Group modes, the 10-bit timer (CBTIMER) counts up until it reaches the duration set by BALEXP1. When the cell balancing timer expires, all cell balancing switches are disabled.

When CBEXP1 is non-zero, the cell balancing timer (CBTIMER) will run and any requested measurement and calibration operations will be performed until expiration, even if BALSWEN[14:1] = 000h (i.e. no balancing switches are actually activated), this ensures the µC can still access the device to confirm balancing operation progress and exit status.

A value of CBEXP1 = 000h ensure no cell balancing occur.

For safety concerns, all BALEXPn are defaulted to 0x000, ensures no cell balancing without prior configuration.

Auto Individual Mode Timing: In Auto Individual mode, the CBEXPn bits within the BALEXPn registers are used as individual cell-balancing duration times for each corresponding CELLn. Individual durations can be configured from 1-1023 seconds, or from 1-1023 minutes depending on the CBMODE setting (LSB = minute, or second). A value of 0x3FF will allow the switches to be enabled indefinitely for CELLn if BALSWENn is also enabled (CBTIMER will be active, and rollover at 3FFh, but is not checked against CBEXPn). The 10-bit expiration timer (CBTIMER) counts up until it reaches the maximum CBEXPn timeout value in the register block (regardless of the BALSWENn settings), governing the balancing operations of all balancing switches. When an individual cell expiration time is reached (determined by CBEXPn), the CELLn switch is disabled going forward.

When any CBEXPn is non-zero, the cell-balancing timer will run and any requested measurement and calibration operations will be performed until expiration, even if BALSWEN[14:1] = 000h (i.e. no balancing switches are actually activated). This ensures the µC can still access the device to confirm balancing operation progress and exit status.

If all 14 CBEXPn settings are 000h, no cell balancing will occur for the switches.

General Timing and Safety Features (All Modes): For safety concerns, all BALEXPn are defaulted to 0x000, which ensures no cell balancing will occur without prior configuration.

The CBTIMER will run to expiration, even if active cell balancing is halted due to UV or Thermal exit conditions, which ensures the µC can still access the part to confirm balancing operation progress and exit status. If an extended SHDNL hold time is requested (HOLDSHDNL = 1x), CBTIMER will read back the governing CBEXP time for the duration of the extended hold interval, allowing the µC to confirm the requested balancing operation has run to completion.

CBRESTART Usage in Manual Mode

The CBRESTART bit within the BALSWCTRL register must periodically be written to a 1 to restart the watchdog timer and prevent the cell balancing switches from being automatically disabled due to exiting Manual Mode when CBTIMER reaches CBEXP1. In the event that a host fails to write the CBRESTART bit or forgets to disable the cell balancing switches, the cell balancing watchdog can automatically disable all cell balancing switches regardless of the BALSWEN configuration. The cell balancing watchdog does not modify the contents of the BALSWEN bits within the BALSWCTRL register.

The CBRESTART bit is used in Manual Cell Balancing Mode only. It provides a means to select new BALSW settings and refresh the Watchdog timer with a single command.

This bit is ignored and has no effect outside of an active Manual Cell Balancing operation. If a Manual operation was selected and the timer is allowed to expire, the operation must be re-launched with a write to BALCTRL (i.e. CBRESTART will not re-initiate a Manual operation which has allowed the CBTIMER to expire).

Emergency-Discharge Mode and CBDUTY Behavior

In Emergency-Discharge Mode, CBTIMER is incremented on a duty-cycled basis indicating the effective time each channel is subject to discharge. Since the active duty-cycle within each 30s t_{CBEO} period is specified by CBDUTY register, the CBTIMER is incremented at specified fractions of 30s (see Table 34).

For example, when CBDUTY is set to 1hr, CBTIMER is incremented in steps of 3.750s at the end of the E/O/M cycle.

Table 34. Emergency-Discharge Mode

FUNCTION	REGISTER FIELD	CONFIGURATION	BEHAVIOR
Emergency Discharge Duty-cycle	CBDUTY[3:0]	0x0	Switches on for 6.25% for 30s (1.875 s per 30s)
		0x1	Switches on for 12.5% for 30s (3.750 s per 30s)
		…	…
		0xF	Switches on for 100% for 30s (less $t_{NONOVERLAP}$)

Note: It is recommended to design the external balancing current at 100% duty-cycle operation to avoid potential thermal issues

Notification Alerts Using CBNTFYCFG

In Automatic and Discharge modes, the Cell-Balancing Notification Alert (ALRTCBNTFY) can be issued to confirm normal progression of automated operations. The frequency of issuance is 1 hour, 2 hours, or 4 hours, in real time (i.e. not CBDUTY-adjusted). Notification alerts will continue to be issued during HOLDSHDNL extension periods.

Cell-Balancing Expiration Timer Summary

In summary, the implementation of the CBTIMER is shown in Figure 47.

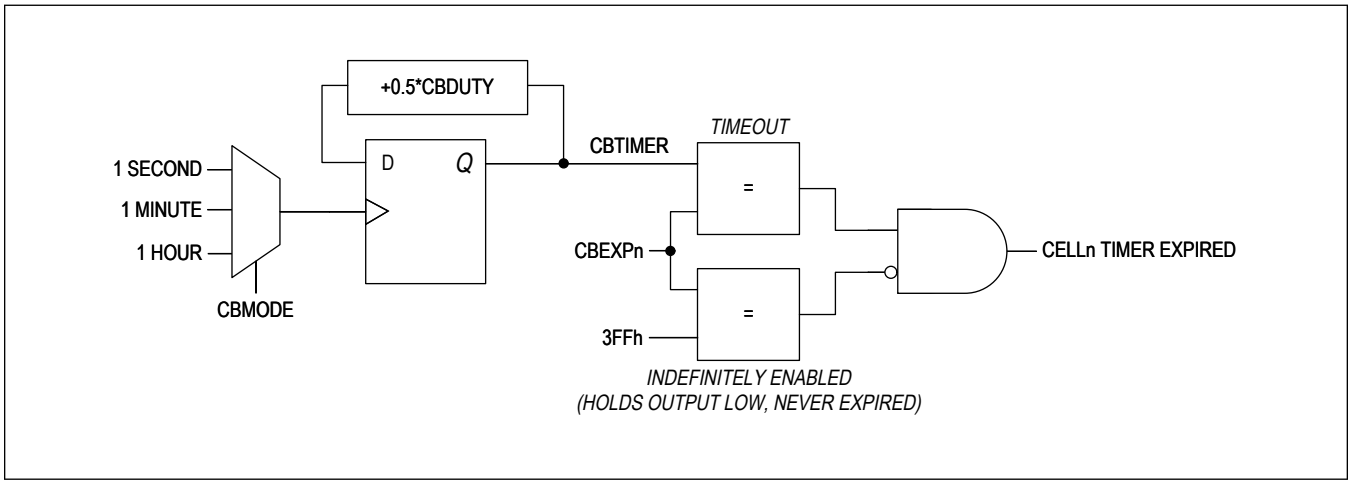


Figure 47. Cell-Balancing Expiration Timer

Note: The CELLn time-expired output feeds into the cell-balancing stop control logic.

Cell-Balancing UV Detection

Cell balancing to a UV threshold allows for all enabled cells configured by BALSWEN to be individually balanced to a specified and uniform voltage level as shown in Figure 48. When a cell reaches the UV threshold, the corresponding balance switch is disabled and remains in an idle state until re-initialized by the host.

Automated Cell Balancing with CBUVTHR checking is only supported for unipolar cell measurements in locations with BALSWEN[n] = 0b1. The user must also ensure CELLEN[n] = 0b1 and POLARITY[n] = 0b0 to allow the required

measurement updates; if the measurement is not supported, balancing of the cell automatically ends with a CBUVSTAT[n] = 0b1 exit condition.

CBUVSTAT[n] in the BALUVSTAT register indicates the corresponding CELLn+1 result falls below the threshold specified by CBUVTHR and that cell-balancing operations on that cell have ended. CBUVSTAT[n] is only cleared when CBMODE is written to 0b000 (Disabled) or when a new CBMODE operation is initiated via BALCTRL.

Automatic cell-balancing to a UV threshold is configured by setting the CBMEASEN bits within the BALCTRL register to 0b11. The UV threshold can be used independently or alongside the cell-balancing timer(s) (CBEXP1 or CBEXPn). In the case that a timer is programmed, it will serve as a redundant mechanism to ensure that a cell is not over-discharged. When all cells have reached the UV threshold, all cell-balancing switches will be disabled but the cell-balancing timer will run until completion, this ensures the µC can still access the device to confirm balancing operation progress and exit status. To use a defined UV threshold, the threshold level must be written to the CBUVTHR in the BALAUTOUVTHR register. This register allows for 14 bit values relating to a 305 µV LSB.

Optionally, the MINCELL value from the prior ADC acquisition can be used as the the desired threshold value. When CBUVMINCELL is disabled, the value written to CBUVTHR during a valid write to BALAUTOUVTHR will be loaded to CBUVTHR. When CBUVMINCELL is enabled the current value in the CELL[n] register corresponding to the MINCELL address will be automatically loaded to CBUVTHR during a valid write to BALAUTOUVTHR (and the content in CBUVTHR during the write will be ignored). When the BALAUTOUVTHR register is read back, the current value of CBUVTHR will be provided, with CBUVMINCELL indicating the means by which it was selected.

The HVMUX and ADC signal chain is used for the balancing measurement and threshold comparison. The acquisition will be determined by the channels enabled in the BALSWEN bitfield as well as the parameters set in the SCANCTRL register. The achievable accuracy of the UV measurement will be determined by ADC accuracy specifications in the electrical characteristics. For the highest accuracy, calibration should be asserted prior to initiating balancing.

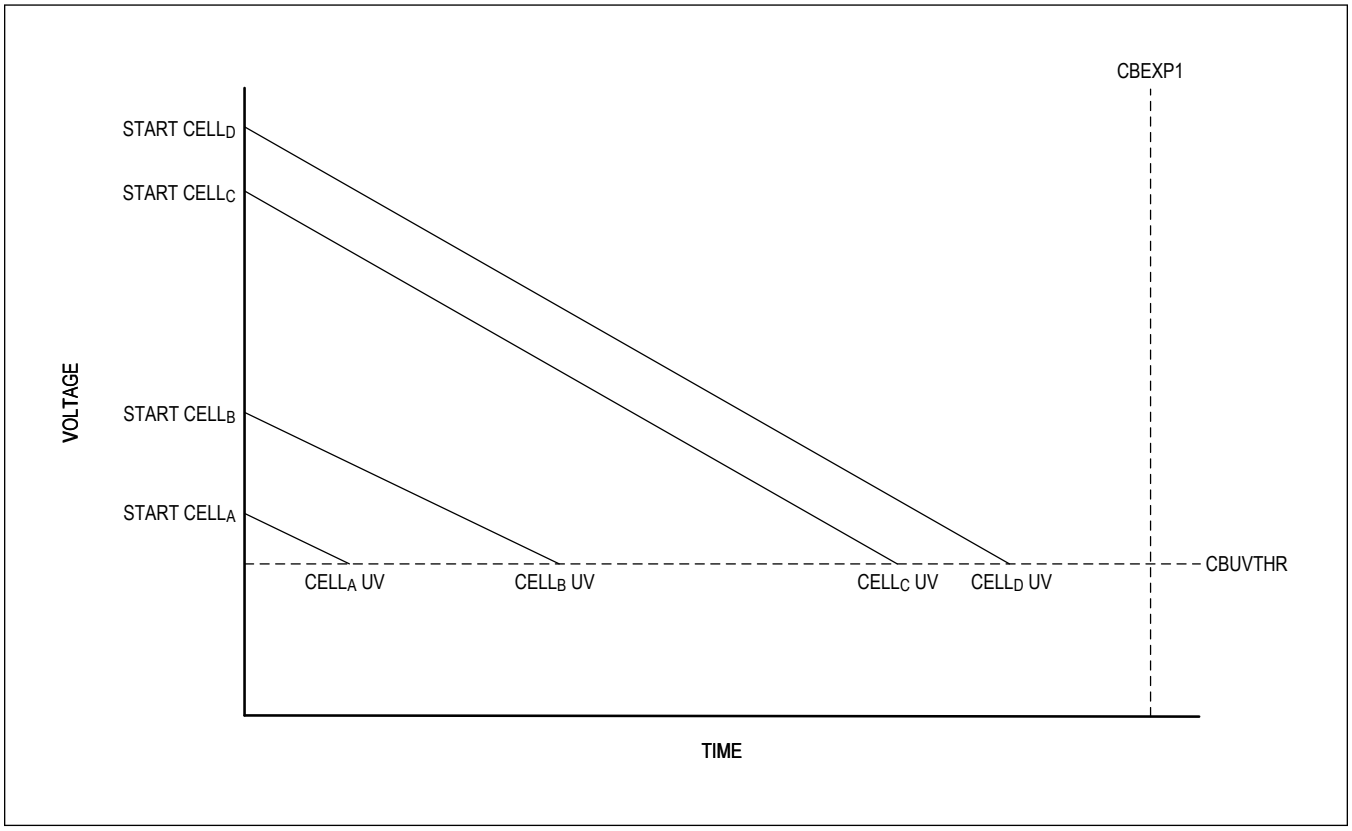


Figure 48. Cell-Balancing UV Threshold Crossing

Note: $CELL_A$, $CELL_B$, $CELL_C$ and $CELL_D$ are non-specific cells. $CELL_A$ represents the cell with the lowest starting voltage. $CELL_D$ represents the cell with the highest starting voltage. In this example, CBUVTHR is the UV threshold for all cells and CBEXP1 is the Cell Balancing Expiration Timer for Auto Group Cell Balancing mode (CBMODE = 0b11x). The $CELL_N$ UV-threshold crossings are inputs to the cell-balancing stop control logic.

Cell-Balancing Measurement

Embedded cell-balancing measurements will only occur when requested by CBMEASEN, as indicated in Table 35:

Table 35. Cell-Balancing measurement enable

CBMEASEN[1:0]	DESCRIPTION
0b0x	Provides the highest duty cycling by skipping all measurement operations. Only cell-balancing timer(s) will be used to terminate cell balancing normally.
0b1x	Enables embedded measurements for manual UV monitoring or supervision by the host processor.
0b11	Enables embedded measurements and internal CBUVTHR checks in Automated modes (checking is not supported in Emergency Discharge mode).

CBMEASEN selections are only functional in discharge and automated Cell-Balancing modes; this setting is ignored in all other modes..

Measurements are taken using the ADC with a fixed OVSAMPL = 16x, SCANMODE = 'pyramid' to provide the highest accuracy measurements. All other scan parameters will be set according the current SCANCTRL, ACQCFG, DIAGCFG, POLARITYCTRL registers. Any attempt to overwrite the scan parameters during balancing be ignored and an ALRTRJCT

condition be issued.

Cell-Balancing IIR Filtering

In Auto-Discharge and Automated Cell-Balancing modes, the automated ADC measurements are processed through each of the individual cells' IIR filter. This filter allows for more accurate measurements and provides noise immunity to maintain robust balancing performance.

In these modes, the IIR filter maintains the setting configured by the user if enabled (IIRFC != 0b111). In the event that the IIR is not used in the normal application (IIRFC = 0b111 = 8/8), the IIR filter will be enabled with an equivalent IIRFC = 0b000 = 1/8 for use in debouncing measurements.

In addition, if the IIR filter is not used in normal applications or has not been routinely updated using AMENDFILT, the CBIIRINIT bit should be used to initialize the IIR with the first acquisition's measurements to avoid falsely exiting the UV threshold due to the long settling response. How the filter behaves upon entry into an Automatic or Emergency Discharge Cell Balancing mode thus depends on CBIIRINIT setting:

In Continuation mode (CBIIRINIT = 0) , the current value in the IIR accumulators is kept (presumably from previous cell measurements) and cell balancing measurements are amended normally.

In Initialization mode (CBIIRINIT = 1), the IIR accumulators will be re-initialized to the first measurement taken, and further cell balancing measurements are amended normally. CBUVTHR checking will not be enabled after the 16th measurement is taken (checking begins on the 17th measurement), giving the IIR time to settle.

Cell-Balancing Calibration

In automated and discharge modes, after each pair of even/odd cell-balancing periods, a supervisory ADC Measurement can be taken (and checked against CBUVTHR, if enabled/applicable - see CBMEASEN). Due to the expected temperature rise during cell balancing, it is recommend to allow automated calibration sequences to be interleaved with the measurement acquisitions. This is done by programming the CBCALDLY to a non-zero value, which signifies how many measurement cycles are taken prior to a calibration being taken. See Table 36.

Table 36. Cell-Balancing Calibration Selection

ADCCALEN (APPLY CALIBRATION)	CBCALDLY (PERFORM CALIBRATION	RESULTING OPERATION
1 (ON)	Non-Zero (ON)	ADC results are post-processed based on calibration coefficients obtained periodically during the cell balancing operation
1 (ON)	000 (OFF)	ADC results are post-processed based on calibration coefficients obtained prior to the cell balancing operation
0 (OFF)	Non-Zero (ON)	Calibration is performed during the cell-balancing operation, but ADC results are based on factory defaults (not recommended)
0 (OFF)	000 (OFF)	ADC results are based on factory defaults.

CBCALDLY settings are only functional if CBMEASEN=0b1x (cell balancing measurements are requested), otherwise they are ignored.

A value of 0x00 (default) in the CBCALDLY bits within the BALDLYCTRL register disables CAL operations (only ADC measurement operations are performed).

If a non-zero value is selected, the first ADC measurement (ADC) operation will be replaced with an on-demand Calibration (CAL) operation. From that point on, this selection determines how often the ADC operation is automatically replaced with an CAL operation (to address thermal drift due to power dissipation during Cell Balancing). 0b001 means ADC and CAL alternate every other cycle. 0b010 means a CAL occurs once every 4 cycles. 0b111 (maximum setting) means a CAL occurs once every 32 cycles. See Table 37 for a list of all possible settings.

Table 37. Calibration Frequency

CBCALDLY	CALIBRATION FREQUENCY
0b000	Periodic Calibration Disabled
0b001	2 cycles
0b010	4 cycles
0b011	8 cycles
0b100	12 cycles
0b101	16 cycles
0b110	24 cycles
0b111	32 cycles

Calibration Out-of-Range During Cell Balancing

After a measurement or calibration is completed, the cell balancer checks the status of the ALRTCAL register bit if calibration is enabled (ADCCALEN = 1). If ALRTCAL is set, it indicates that calibration is out of range, and that calibrated ADC results could be corrupted as a result.

If ALRTCAL is set and calibration is enabled (ADCCALEN = 1), the ALRTCBCAL bit will be set and active cell balancing operations will be immediately halted to prevent balancing errors due to inaccurate measurements. All subsequent measurement, calibration, and switching cycles will be skipped until the cell balancing duration expires, or is otherwise aborted/restarted. The cell balancing timer (CBTIMER) continues to run until the governing CBEXP time is reached, and HOLDSHDNL extensions still apply (if enabled), allowing the µC to confirm exit status. Note that once ALRTCBCAL is issued, data in the CBUVSTAT bitfield and data fetched by CBSCAN requests should be treated as compromised.

If an ALRTCAL/ALRTCBCAL condition is issued, the user can exit the cell-balancing operation, and attempt to resolve the condition. If the condition cannot be resolved, cell-balancing operations can be requested using factory calibration defaults by setting ADCCALEN = 0.

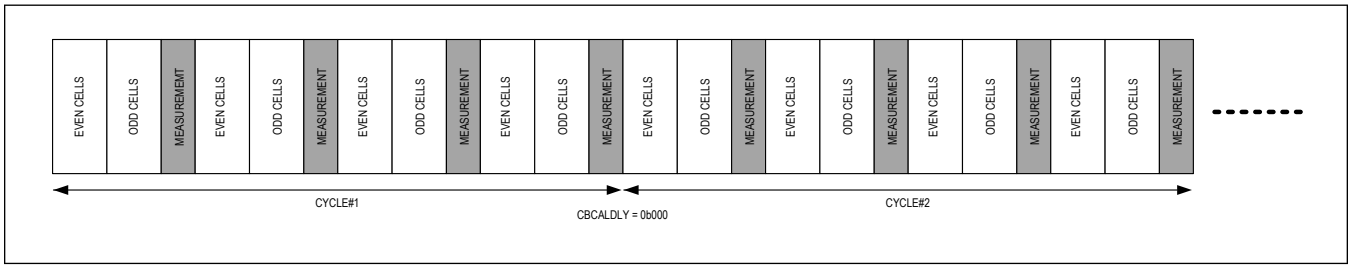


Figure 49. Cell Balancing with No Calibration

Cell Balancing with Calibration

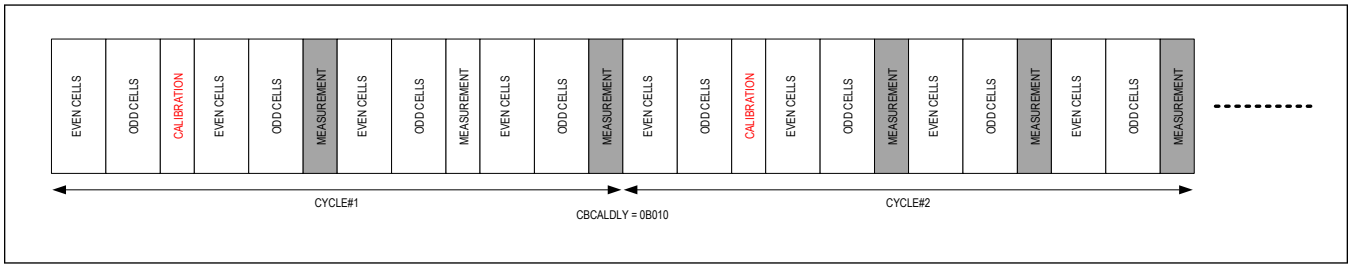


Figure 50. Cell Balancing with Calibration

Transfer-Measurement Results using CBSCAN

The CBSCAN bit in the BALDATA register can initiate a manual transfer of results from the IIR to the CELL data registers (RDFILT is ignored, and IIR data is always transferred, since the IIR governs cell balancing operations). CBSCAN is provided to support readback of measurement results taken during Automated and Emergency Discharge Cell Balancing modes. If CBSCAN is issued during these cell balance measurements, the move will be executed once the sequence is complete.

CBSCAN acts as a strobe bit and therefore does not need to be cleared (self-clearing). It always reads logic zero.

CBSCAN is not valid outside of automated cell-balancing operation. If automated cell balancing is stopped or when manual balancing is operational, the measurement scan bitfields in the SCANCTRL register must be used for data control into the cell registers.

Cell-Balancing Completion

In summary, after the host initializes the cell-balancing operation, the operation will be stopped by any of the following:

- Watchdog timer expiration (CBTIMER = CBEXPn)
- Reaching the UV threshold (per-cell in Automatic modes only, if CBMEASEN=0b11)
- Thermal fault condition (Automatic and Discharge modes only, if CBTEMPEN = 0b1)
- Calibration fault condition (Automatic and Discharge modes only, if ADCCALEN = 0b1)
- Aborting the operation by changing CBMODE to 0b000 (Disabled)
- Re-initiating an operation by changing CBMODE to a value other than 0b000

Manual cell-balancing-mode switch activity can be temporarily suspended for calibration or ADC measurements if AUTOBALSWDIS = 0b1.

In discharge, manual, and auto-group modes, the CBTIMER is stopped when it reaches CBEXP1, regardless of BALSWEN settings.

In auto-individual modes, the CBTIMER is stopped when it reaches MAX(CBEXPn), regardless of BALSWENn settings.

Automatic and discharge modes are halted if temperature exit is enabled (CBTEMPEN = 0b1) and an overtemperature fault occurs.

Automatic and discharge modes are halted if (CBMEASEN = 0b1x) and a calibration fault occurs.

All timed modes run CBTIMER for the full duration specified, even if actual cell-balancing operations are stopped due to UV or thermal-exit conditions, allowing the µC to confirm the exit status. Additional time for the µC to check exit status can be afforded using HOLDSHDNL options.

CBACTIVE allows confirmation of cell-balancing operation status. A cell-balancing operation is considered completed normally if the CBTIMER expires (all CB modes), or when all enabled cells reach the programmed CBUVTHR limit (automatic modes only, if CBMEASEN = 1b1). A cell-balancing operation is considered completed abnormally in the event of an ALRTCBCAL or ALRTCBTEMP condition.

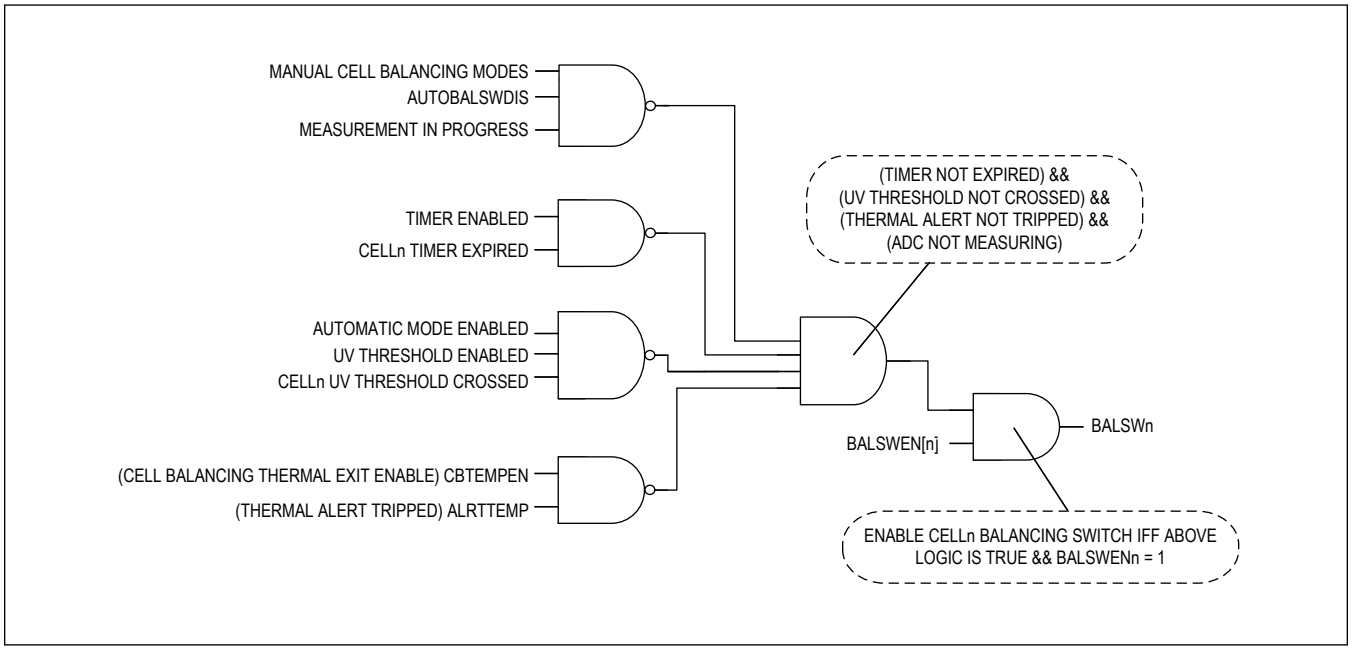


Figure 51. Cell-Balancing Stop Control

Note: The thermal fault will limit the temperature rise to a safe level below the maximum junction temperature of the device as defined by the ALRTTEMP specification in the electrical characteristics section. For applications requiring maximum cell-balancing current, this can be disabled, but the system should take caution to ensure that the device is not damaged by exceeding the absolute maximum rated junction temperature.

Automatic SHDNL Control using HOLDSHDNL

In order to allow for timed balancing with no host interaction the SHDNL pin can be pulled up to V_{AA} to keep SHDNL high while the timers or UV detection is running by appropriately configuring the HOLDSHDNL bitfield within the BALCTRL register. When enabled and engaged, this mode activates an internal diode pull-up from the V_{AA} pin to SHDNL. This will keep the device operational, even if UART operation is suspended for long periods of time.

The HOLDSHDNL options have no effect in Disabled or Manual modes.

In mode 0b01, the pullup will be engaged for the selected CBEXP1 interval for group operations, or the longest CBEXPn time selected for individual operations, even if switch activity is halted due to thermal protection (ALRTCBTEMP), calibration issues (ALRTCBCAL), or reaching the specified voltage target (CBUVTHR).

In mode 0b10, the pullup will be engaged for the selected CBEXP1 interval for group operations, or the longest CBEXPn time selected for individual operations even if switch activity is halted due to thermal protection (ALRTCBTEMP), calibration issues (ALRTCBCAL), or reaching the specified voltage target (CBUVTHR). After CBTIMER expires, HOLDSHDNL will continue to be held for the greater of 5 minutes or 6.25% of the relevant CBEXPn interval. If CBEXPn timing is disabled/infinite (3FFh), SHDNL will be held until removed by a write to BALCTRL.

In mode 0b11, the pullup will be engaged until removed by a write to BALCTRL.

If HOLDSHDNL= 0b1x, CBTIMER will read back the governing CBEXP time for the duration of the extended hold interval, allowing the µC to confirm the requested balancing operation has run to completion. In modes HOLSDSHDNL = 0b1x, the hold behavior can be removed after operations are completed and the exit status has been confirmed by writing CBMODE to Disabled, allowing the device to power down.

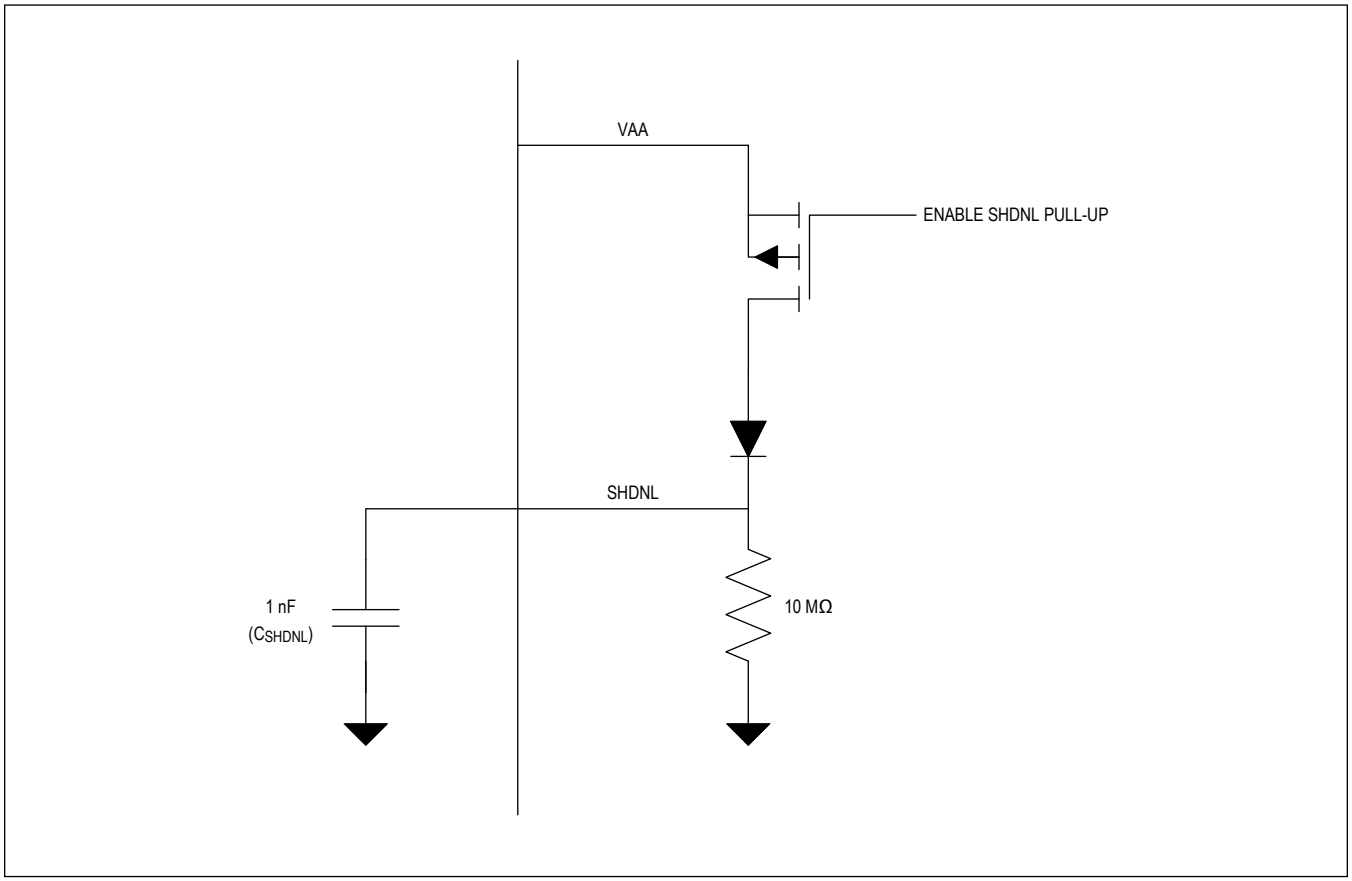


Figure 52. SHDNL Pullup Control

Cell-Balancing Switches

The cell-balancing current is limited by the external balancing resistance, $R_{BALANCE}$, and the internal balancing switch resistance (R_{SW}), Figure 53. Cell-balancing switches are internally controlled with even and odd switching sequence in auto/manual modes or independently in Emergency-Discharge mode. Fault detection is described in the *Diagnostics* section.

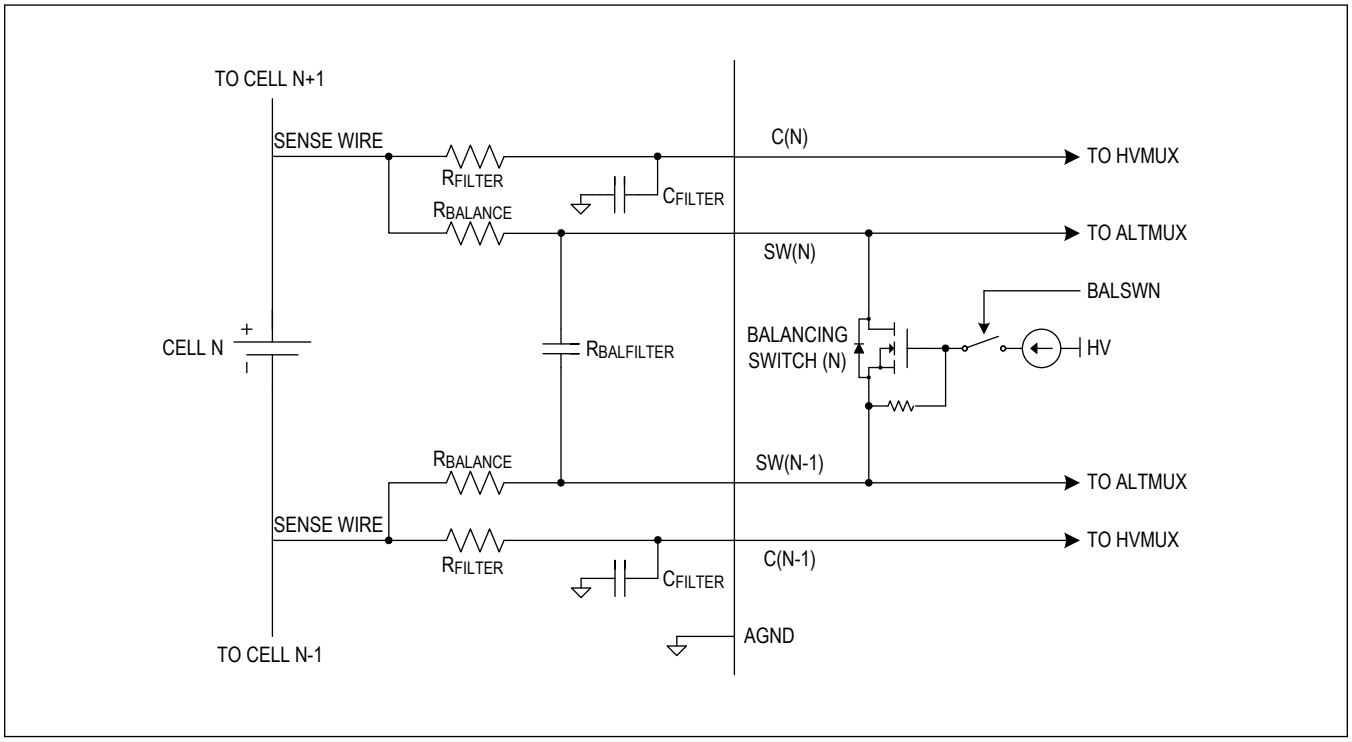


Figure 53. Internal Cell-Balancing Switches

Cell-Balancing Current

The cell-balancing current is limited by package power dissipation, average die temperature, average duty cycle, and the number of switches conducting current at any one time. The system designer must carefully control the device power dissipation by selecting a balancing current resistance ($R_{BALANCE}$) to ensure the die and package temperature are below the absolute maximum package rating and neither the device thermal shutdown threshold nor the ADC measurement accuracy is impacted. The maximum per-switch balancing current for 7 switches concurrently enabled is shown in Figure 54 for an assumed 10 year device lifetime.

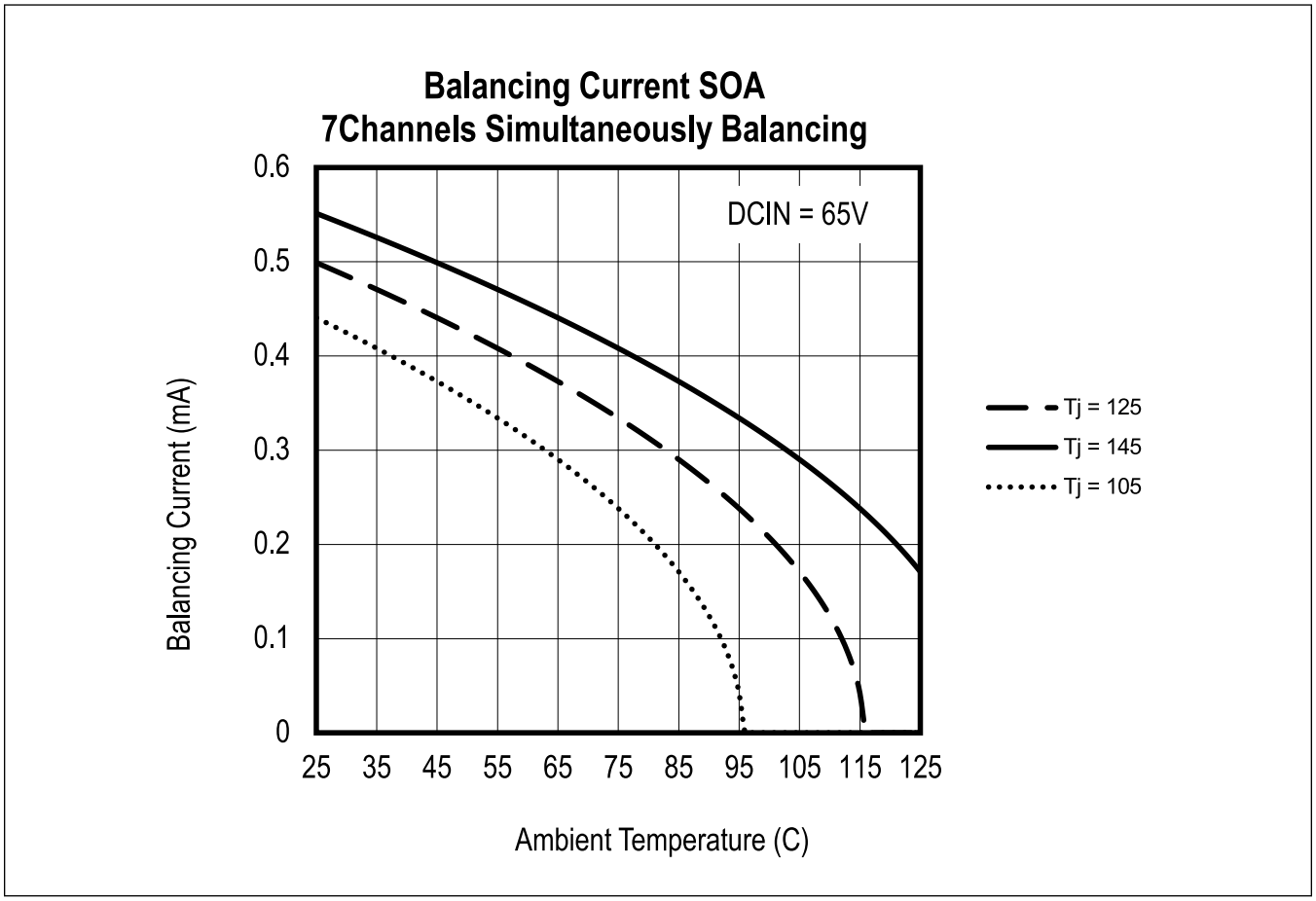


Figure 54. Typical Balancing-Current Performance

Example: Autonomous-Cell Balancing by Time

Autonomous-cell balancing can be commanded within the MAX17852 which enables balancing while the host microcontroller enters a sleep state. The following procedure illustrates how autonomous cell balancing is invoked with the primary stop mechanism as a timer:

1. Host calculates SOC for each of the individual cells
2. Host determines which cells to balance and associated balancing time
3. Host programs balancing channels using BALSWEN[13:0]
4. Host programs effective balancing current

   Effective balancing current = V_{CELLn}/(2 x RBALANCE) x CBDUTY[7:4]
5. Host programs CBEXP1-CBEXP14 based on effective balancing current and SOC
6. Host programs HOLDSHDNL to determine shutdown behavior at completion of cell balancing
7. Host initiates balancing using CBMODE "auto-individual cell balancing by second" or "auto-Individual cell balancing by minute"

Example: Autonomous-Cell Balaning with Programmable UV Threshold

Autonomous-cell balancing controlled via a programmable UV threshold can be commanded within the MAX17852 to enable balancing while the host microcontroller enters a sleep state. The following procedure illustrates how balancing

is invoked with the primary stop mechanism configured to be a voltage measurement and a secondary stop mechanism being a programmable timer.

1. Host calculates SOC for each of the individual cells
2. Host determines which cells to balance and associated balancing time

   Timer is a secondary stop mechanism and should have additional margin applied as not to interact with primary UV measurement stop threshold
3. Host programs balancing channels using BALSWEN[13:0]
4. Host programs effective balancing current

   Effective balancing current = $V_{CELLn}/(2 \times R_{BALANCE}) \times$ CBDUTY[7:4]
5. Host programs CBEXP1-CBEXP14 based on effective balancing current and balancing time calculation
6. Host programs CBUVTHR or CBUVMINCELL to program UV measurement stop threshold
7. Host programs CBMEASEN as "Embedded ADC/CAL Measurements enabled, CBUVTHR checking enabled"
8. Host programs CBCALDLY to force measurement calibration to account for temperature rise from balancing

   Calibration choice should be chosen based on the thermal time constant of the board
9. Host programs HOLDSHDNL shutdown behavior at completion of cell balancing
10. Host initiates balancing using CBMODE as "auto-individual cell balancing by second" or "auto-individual cell balancing by minute"

Interface

Interface Options

The MAX17852 supports two different interfaces to control the data-acquisition system. The applied interface is configured using the UARTSEL pin. Drive this pin externally by applying a pullup resistor to V_{AA} to enable UART, or a pulldown resistor to AGND to enable SPI. This interface flexibility allows one device to serve multiple battery applications for high-voltage and low-voltage systems, but it cannot dynamically change between them both.

UART Interface

UART Interface

The Battery-Management UART Protocol allows up to 32 devices to be independently addressed in a daisy-chain fashion as shown in Figure 55. The host initiates all communication with the daisy-chain devices via a UART interface such as the MAX17841B. The UART can be configured to support a variety of flexible implementations depending on the application requirement. The configurations as defined using UARTCFG, are shown in Table 38.

Table 38. UART Configurations

UARTCFG	UART CONFIGURATION	UART UP PATH	UART DOWN PATH
0b00	Single UART Interface with External Loopback	Active	Inactive (Buffered/Pass Through)
0b01	Single UART Interface with Internal Loopback	Active	Inactive (Buffered/Pass Through)
0b10	Single UART Interface with Differential Alert Interface	Active	Differential Alert
0b11	Dual UART Interface	Active	Active

Single-UART Interface with External Loopback

When UARTCFG is configured for single-UART with external loopback, the data flow is always unidirectional from the host, up the daisy chain (Up path), and then loops back down the daisy chain (Down path) to the host, as shown in Figure 55.

In the Up path, each device first receives data at its lower RX port and immediately re-transmits data from its upper TX port to the lower RX port of the next device. The last device uses an external loopback differential cable to transfer data from its upper TX port directly into its upper RX port and then immediately re-transmits the data from its lower TX

port to the upper RX port of the next down-stack device. The Down Path then acts as a pass-through, buffering and re-transmitting the data. It will not act on any commands in this configuration.

The external loopback has two advantages:

- It is quicker to determine device count for applications where the host does not assume what the device count is.
- It helps to match the supply current of the last device to that of the other daisy-chain devices (because the hardware configuration is identical).

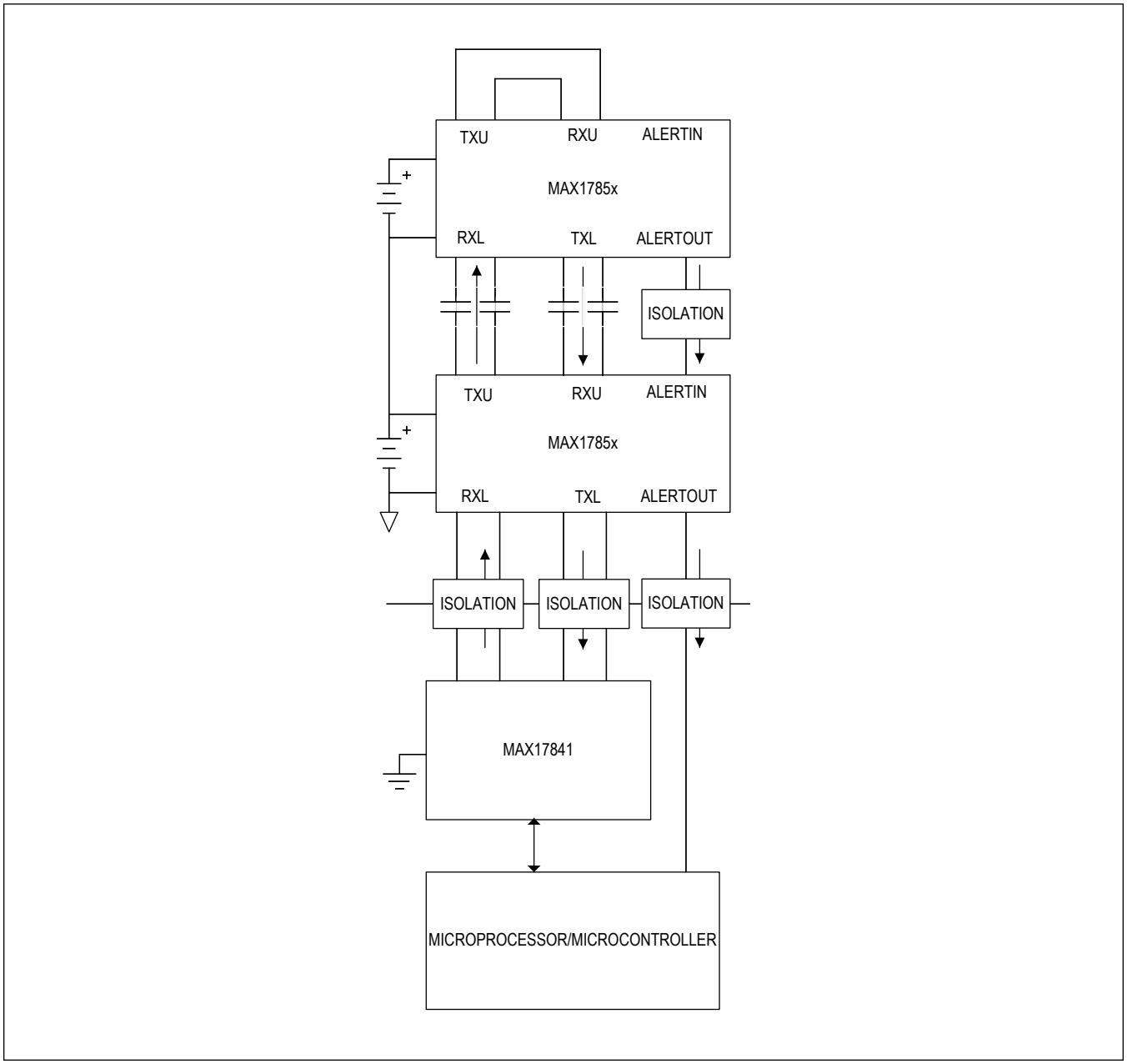


Figure 55. Single UART with External Loopback

Single UART with Internal Loopback

Single UART with internal loopback (UARTCFG = 0b01) routes the upper-port transmit data internally to the upper-port receiver. This can be used to configure the top device in the daisy chain to prevent the need for external components and wire connections. Additionally, this mode is useful to diagnose the location of any daisy-chain signal breaks. This is done by enabling the internal-loopback mode on the first device, checking communication, then moving the loopback mode to the next device and continuing up the stack until communication is lost.

Changing the UART configuration to single UART with internal loopback immediately changes that device's upper-port configuration so the signal is routed internally from the upper transmitter to the upper receiver, while external signals present on the upper-port receivers' input pins are ignored; therefore, when UARTCFG is written to 0b01, the WRITE command forwarded in the Up path is interrupted in the down-stack direction, interrupting its return to the host. To verify if the operation was successful, issue this command twice. If the MAX17841B interface is used, its receive buffer should be cleared before changing UARTCFG, and cleared again after changing the loopback configuration because the communication was interrupted.

Single UART with Differential Alert Interface

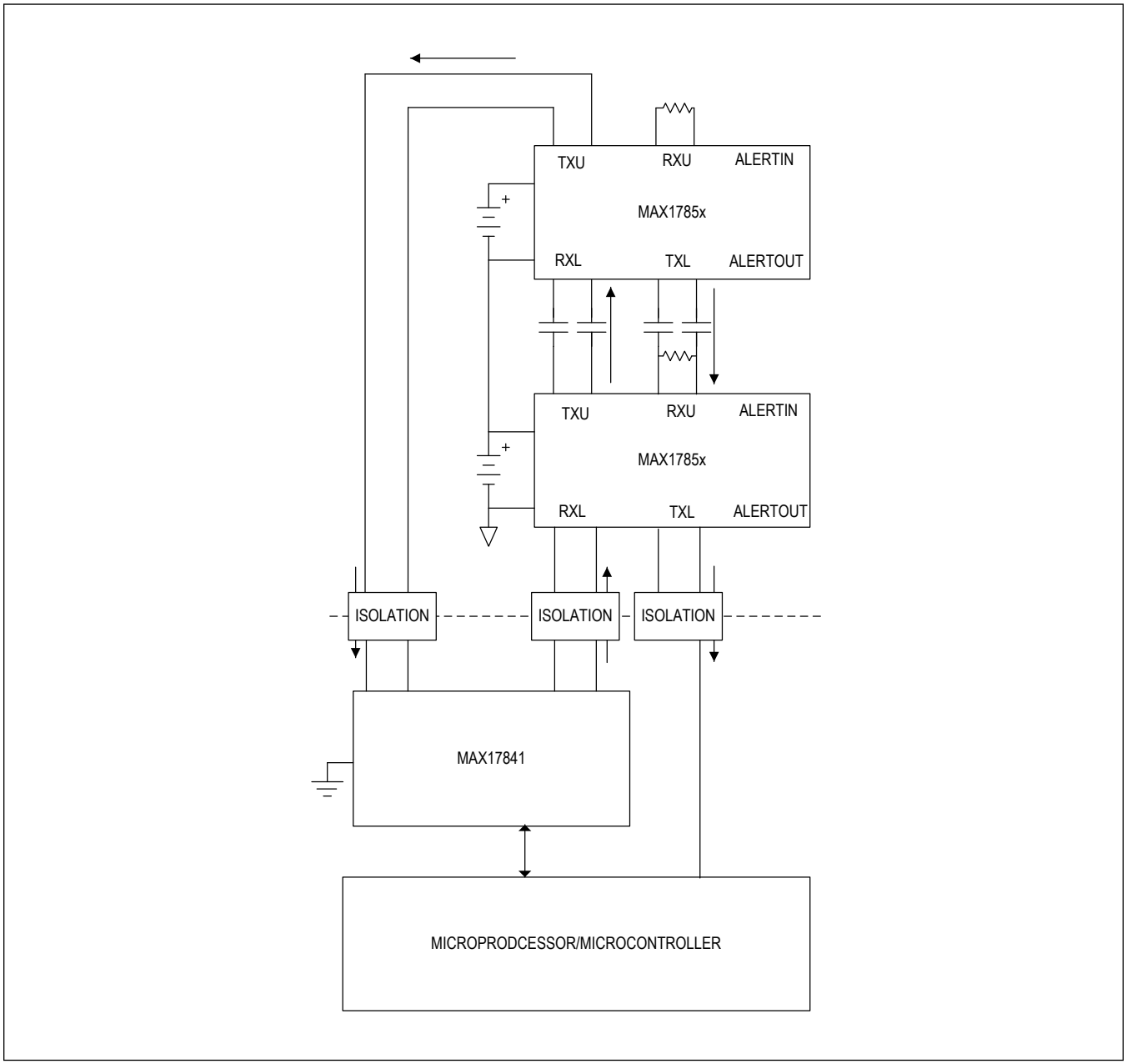


Figure 56. Single UART with Differential Alert Interface

Dual-UART Interface

If the end application requires higher data throughput or a redundant communication path for safety, a dual-UART-interface configuration can be utilized by writing UARTCFG = 0b11. When configured, the Down path acts as an independent UART path that enables simultaneous read processing from both UART paths. This essentially doubles the effective interface rate to ~4Mbps. In the event of a broken interface wire, the independent UART paths allow

uninterrupted access to all devices in the daisy-chain by dynamically changing the master interface with no loss of functionality.

Note: For this configuration to be utilized, both hardware and software configurations should match.

By default, the Down-path UART operates as a slave device and as such, has no response to a WRITE or WRITEALL command. The slave interface only responds to the READ, READALL, and READBLOCK commands. If a WRITE command is issued on the slave UART, the write is ignored and passed through to the next device in the daisy-chain, eventually returning to the MAX17841. Each device in the daisy chain asserts its ALRTDUALUART bit in the STATUS2 register to indicate that a valid WRITE command was received but not acted upon. This bit remains set until cleared by the master interface.

Configuration of the master is performed using the UPHOST, or DOWNHOST commands and identification of the master is performed by reading the UARTHOST bit. Please refer to the the *Battery-Management UART Protocol* Commands section.

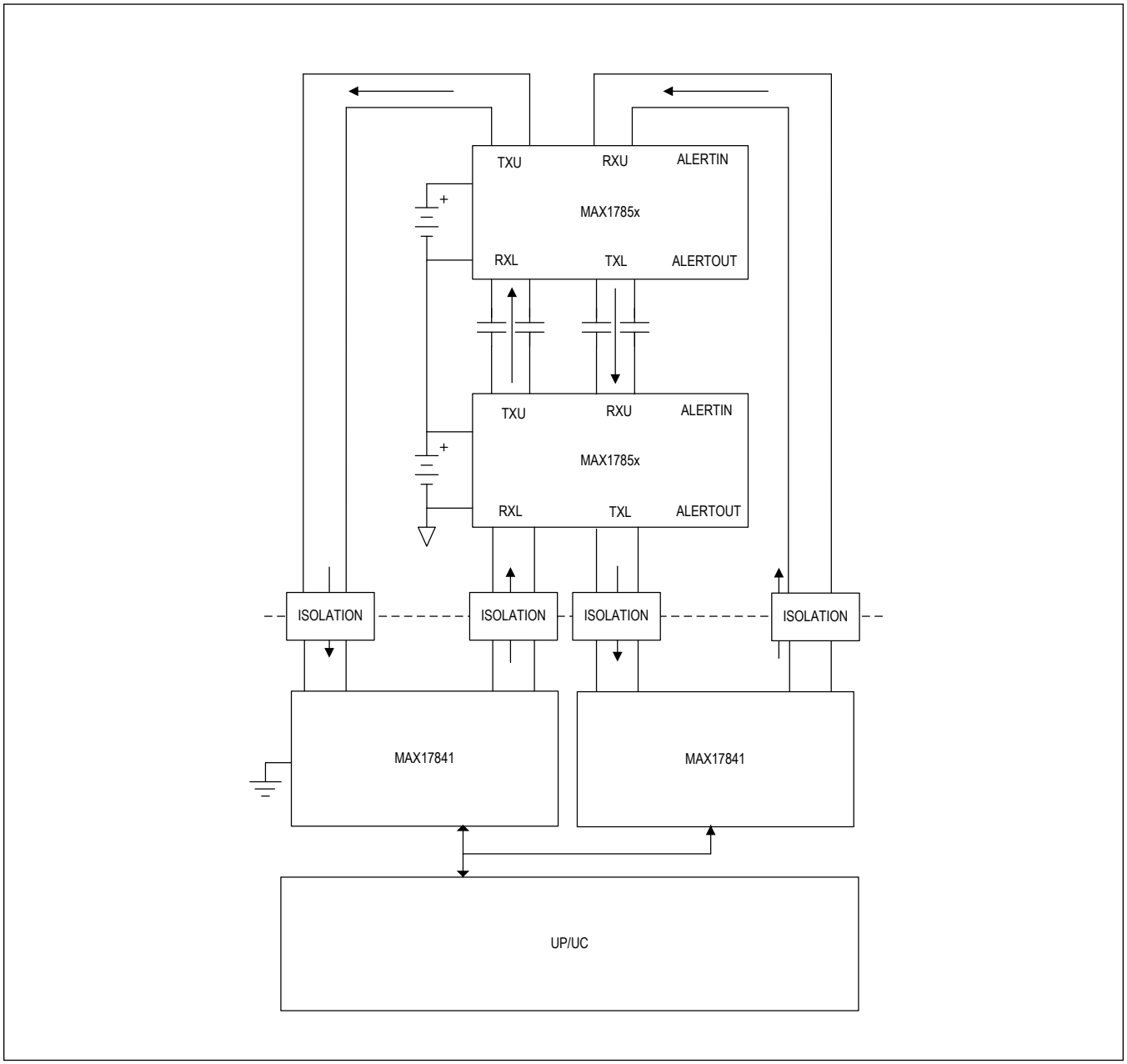


Figure 57. Dual-UART Interface

Dual-UART Master Configuration

If the upstream UART path cannot communicate due to a failure condition, the downstream UART path can reinitialize itself as the master through a DOWNHOST UART command packet issued by the host. This allows the downstream path to have full read and write capability. The upstream path then hands over master functionality and configures itself as a slave. If the upstream path regains functionality, it is able to only issue READ commands, unless it reinitializes itself as the master using the UPHOST command.

If an interface is reinitialized, the host should poll the UARTHOST bit to ensure that all devices within the daisy-chain are configured to the same master interface.

Note: The UPHOST command is only valid on the upstream UART and the DOWNHOST command is only valid on the downstream UART. If an UPHOST command is issued on the downstream UART, no action is taken and the ALRTDUALUART bit will be set.

Dual-UART Master/Slave Interaction

The upstream and downstream UART timing should be synchronized by the host controller to avoid potentially reading data from the prior acquisition. This may occur when the master issues a WRITE command and the slave attempts to read the data before the entire data packet propagates through the last device on the daisy chain. See Figure 58 and Figure 59 as an example of the timing considerations. The master UART path will not prevent this interaction and should be handled by the host.

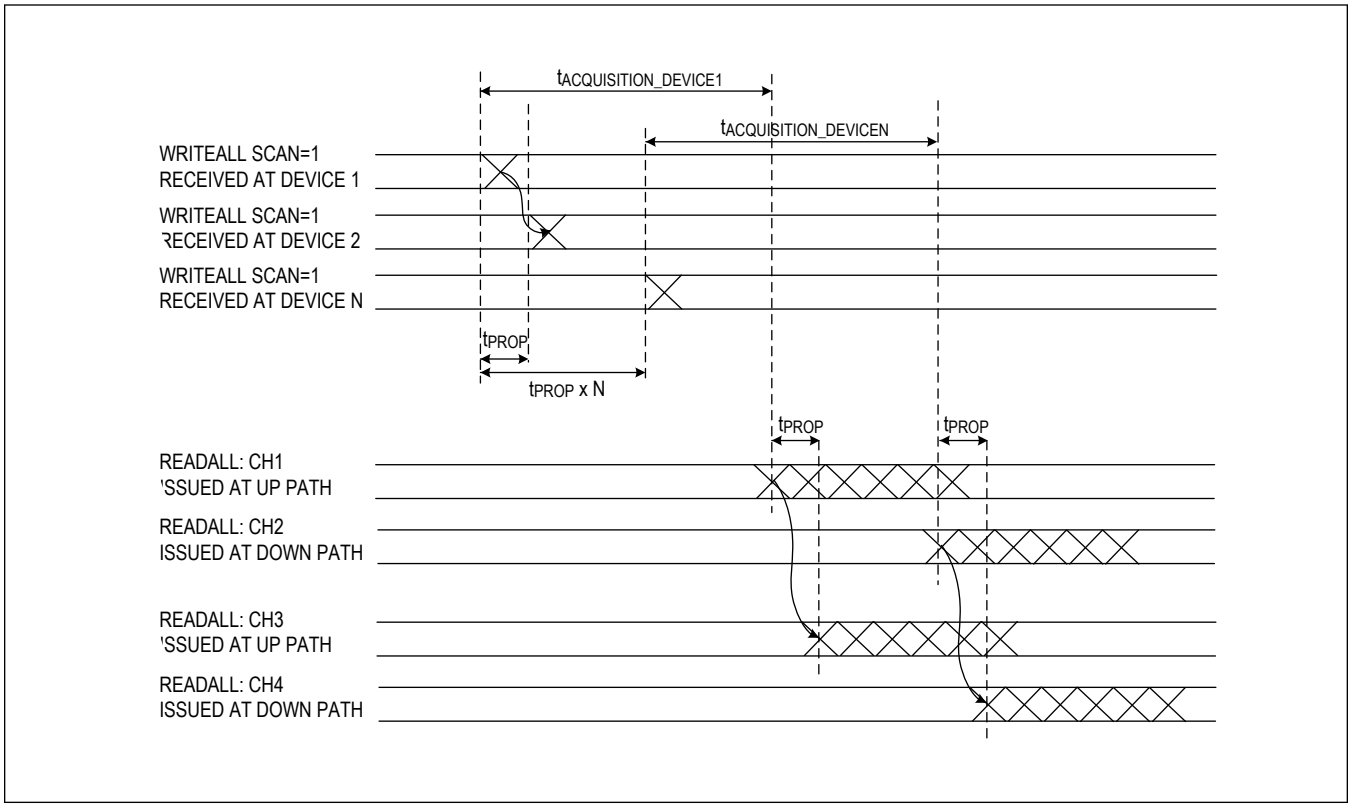


Figure 58. Dual-UART Master/Slave Interaction (Timing Considerations)

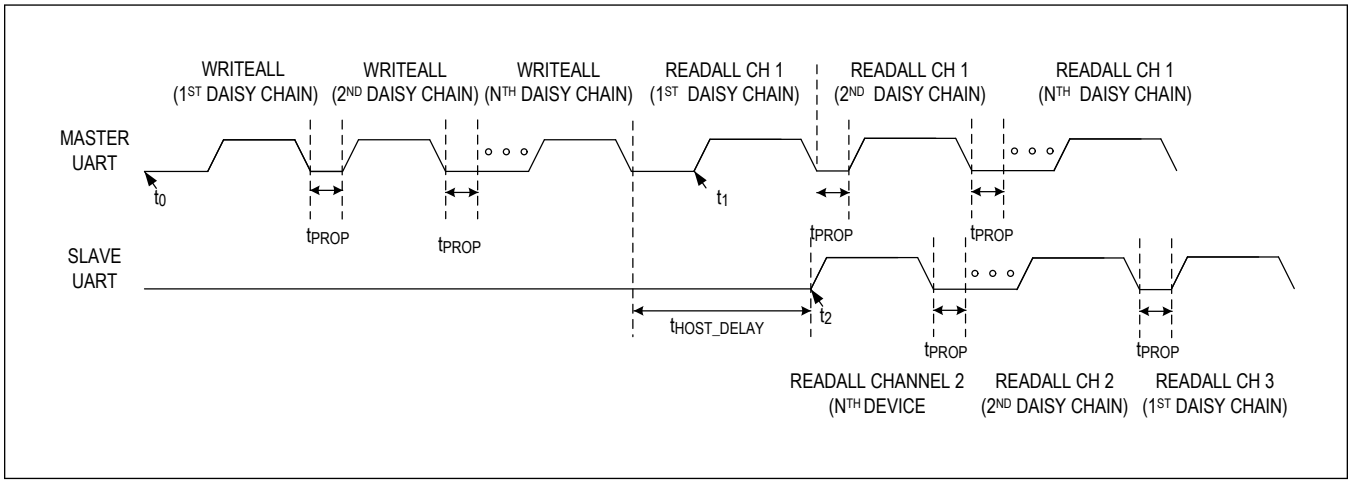


Figure 59. Dual-UART Command Timing

Similarly, the UPHOST and DOWNHOST commands should not be sent simultaneously to avoid an unknown state to the host controller. The host controller will be able to diagnose the incorrect state by reading the UARTHOST bit or by invalid commands signified by the ALRTDUALUART.

UART Ports

Two UART ports are utilized, a lower port (RXL/TXL) and an upper port (RXU/TXU). Each port consists of a differential line driver and differential line receiver. DC-blocking capacitors or transformers may be used to isolate daisy-chain devices that are operating at different common-mode voltages. During communication, the character encoding provides a balanced signal (50% duty-cycle) that ensures charge neutrality on the isolation capacitors.

UART Transmitter

When no data is being transmitted by the UART, the differential outputs must be driven to a common level to maintain a neutral charge difference between the AC-coupling capacitors or to avoid saturation of the isolation transformers. In the default idle mode (low-Z), the transmitter drives both outputs to a logic-low level to balance the charge on the capacitors; this also works well with transformer coupling. The high-Z idle mode (TXLIDLEHIZ, TXUIDLEHIZ = 0b1) places the TXn pins in a high-Z state during time periods where the UART is inactive, which can be desirable to minimize the effects of charging and discharging the isolation capacitors. The idle mode for the upper and lower ports can be controlled independently through the TXUIDLEHIZ and TXLIDLEHIZ configuration bits.

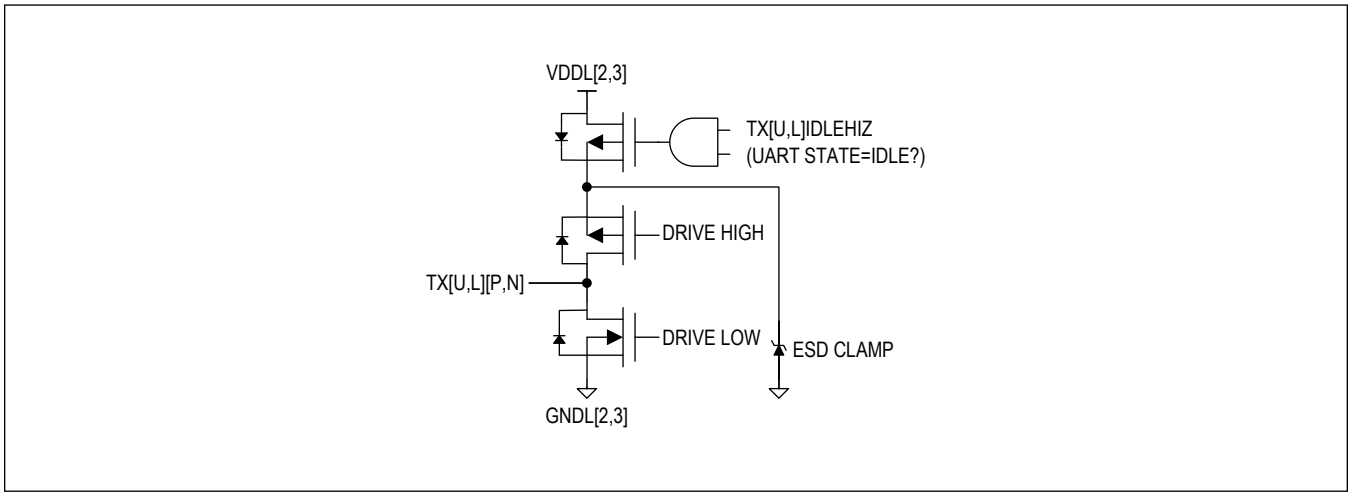


Figure 60. UART Transmitter

UART Receiver

The UART receiver has a wide common-mode input range to tolerate harsh EMC conditions. It can be operated in differential mode or single-ended mode (see Table 38). By default, the UART receivers are configured for differential mode. In single-ended mode, the RXP input is grounded and the RXN input receives inverse data as described in the *Application Information* Section see (Figure 123). In single-ended mode, the receiver input threshold is negative so that a zero differential voltage (V_{RXP}, V_{RXN} = 0V) is considered to be a logic one and a negative differential voltage (V_{RXN} high) is a logic zero.

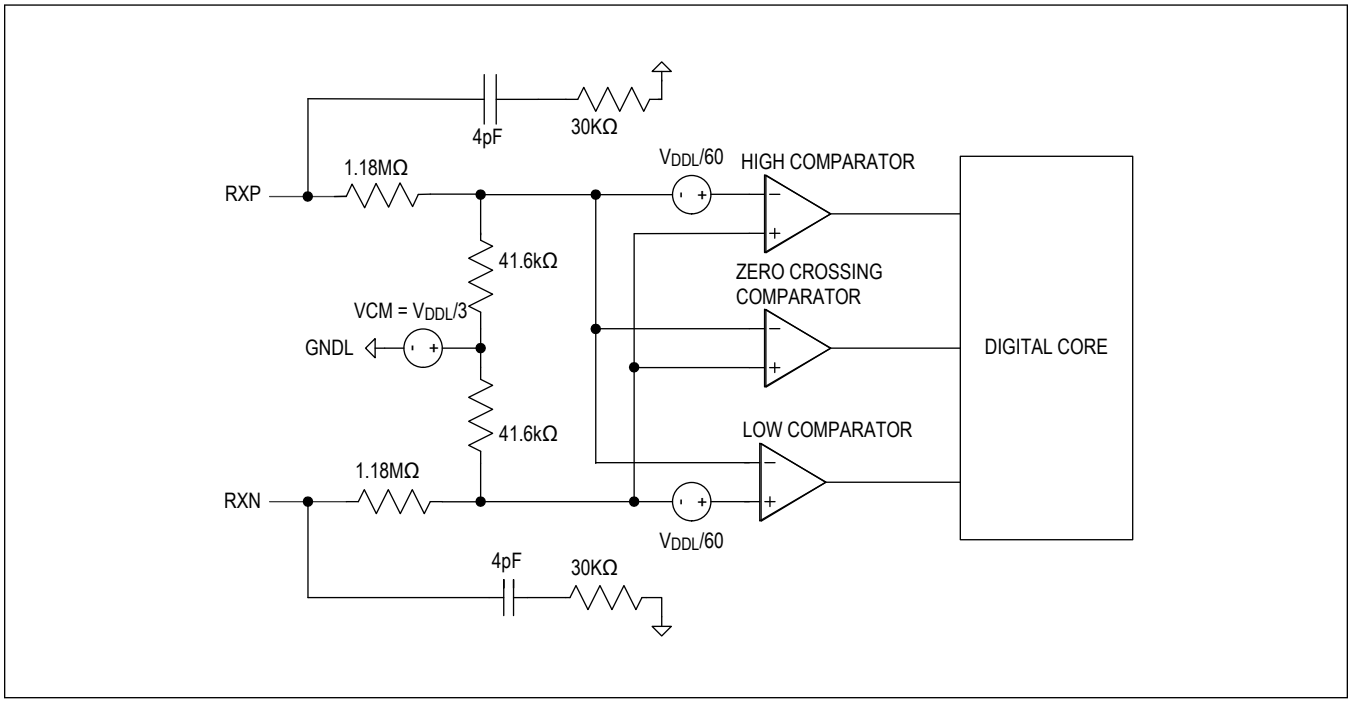


Figure 61. UART Receiver

SHDNL Charge Pump

The SHNDL input can be driven externally or can be controlled using UART communication only. Using a differential UART configuration, the signaling on the lower-port receiver drives an internal charge pump that charges up the external 1nF capacitor connected to the SHDNL input, as shown in Figure 62. V_{SHDNL} reaches 1.8V in 200µs (typ). The charge pump then self-regulates to the $V_{SHDNLIMIT}$ and can maintain V_{SHDNL} even with the UART idle for long durations. In the event communication is halted, the SHDNL pin voltage falls, with a 10ms time constant (assuming only a 1nF capacitor).

Note: Both upper and lower UART RX ports are enabled with charge pumps, allowing for either communication on either Up path or Down path to initialize the device.

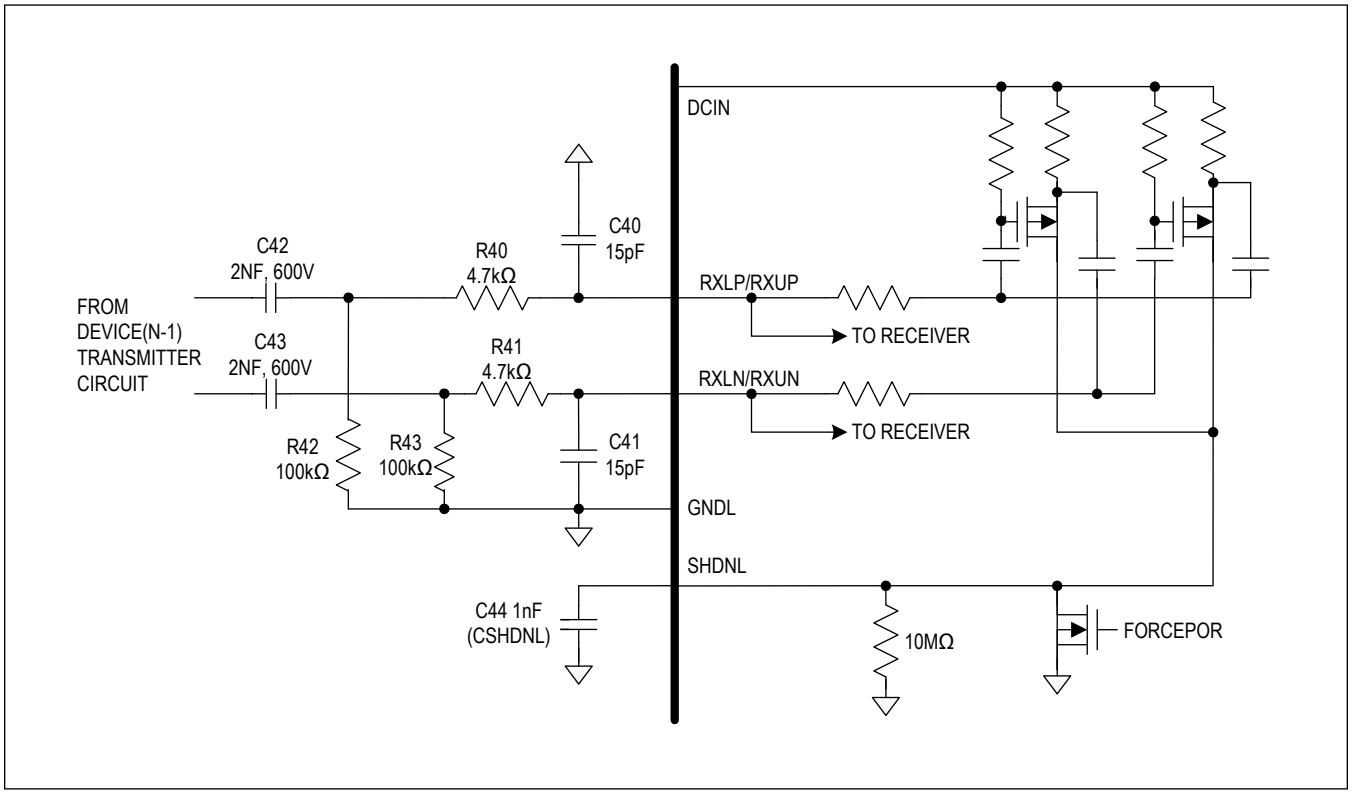


Figure 62. SHDNL Charge Pump

UART RX Modes

During the first preamble received after a reset, the receiver automatically detects if the received signal is single-ended, and if valid, the receiver is appropriately configured in single-ended mode. The device must be reset for any change in the receiver hardware configuration to be detected. Device reset is signaled to the host via the ALRTRST status bit. In normal operation, this bit is cleared after the first HELLOALL command.

The receiver mode is indicated using the following bits:

- ALRTCOMMSEU1 (for the upper port), and ALRTCOMMSEL1 (for the lower port) of the FMEA1 register are set after STATUS1:ALRTRST has been cleared
- ALRTCOMMSEU2 (for the upper port), and ALRTCOMMSEL2 (for the lower port) of the FMEA1 register are set before STATUS1:ALRTRST has been cleared

See Table 39 for a list of the conditions under which ALRTCOMMSEU1 and ALRTCOMMSEL1 are set. If the RXP input is open circuit, the RX-mode detection will place the UART in single-ended mode so that the port can still operate, albeit with reduced noise immunity. The host can diagnose this condition by checking ALRTCOMMSELn and ALRTCOMMSEUn bits. Any other faults result in communication errors. Table 40 lists the conditions under which ALRTCOMMSEU2 and ALRTCOMMSEL2 are set.

Table 39. UART RX Modes (Post ALRTRST Being Cleared)

STATUS1:ALRTRST	RXP	RXN	ALRTCOMMSEx1	RX MODE
x	Connected to data	Connected to inverse data	0	Differential mode (normal)

Table 39. UART RX Modes (Post ALRTRST Being Cleared) (continued)

STATUS1:ALRTRST	RXP	RXN	ALRTCOMMSEx1	RX MODE
0	Grounded	Connected to inverse data	1	Single-ended mode (normal)
0	Open-circuit (fault)	Connected to inverse data	1	Single-ended mode (low noise immunity)
x	Connected to data	Open-circuit (fault)	0	Differential mode (communication errors)
1	Don't care	Don't care	0	--

Table 40. UART RX Modes (Prior to ALRTRST Being Cleared)

STATUS1:ALRTRST	RXP	RXN	ALRTCOMMSEx2	RX MODE
x	Connected to data	Connected to inverse data	0	Differential mode (normal)
1	Grounded	Connected to inverse data	1	Single-ended mode (normal)
1	Open-circuit (fault)	Connected to inverse data	1	Single-ended mode (low noise immunity)
x	Connected to data	Open-circuit (fault)	0	Differential mode (communication errors)
0	Don't care	Don't care	0	--

Note: ALRTCOMMSEU1 and ALRTCOMMSEL1 both read 0b0 if STATUS1:ALRTRST = 0b1.

ALRTCOMMSEU2, and ALRTCOMMSEL2 both read 0b0 if STATUS1:ALRTRST = 0b0.

Baud-Rate Detection

The UART can operate at a baud rate of 2Mbps, 1Mbps, or 0.5Mbps. The baud rate is controlled by the host and is automatically detected by the device when the first preamble character is received after reset. If the host changes the baud rate, it must issue a reset and resend a minimum of 2 x n preambles at the new baud rate (where n = number of devices). The 2 x n preambles are necessary because the transmitter for the upper port does not transmit data until the lower-port receiver has detected the baud rate; likewise, the transmitter on the lower port does not transmit data until the upper-port receiver has detected the baud rate. A simple way to do this is for the host to start transmitting preambles and stop when a preamble has been received back at the host Rx port.

Sending 2 x n preambles completes baud detection on all n devices in the chain. To receive a preamble back at the host Rx port, (2 x n) + 1 preambles must be sent.

Note: Baud rate for dual-UART configuration is determined during the initialization sequence of either the Up path or Down path. Both paths operate at the same communication rate.

TX Adaptive Mode for Single-Ended Mode

To overcome the error tolerance limitation when connecting a MAX17852 to a conventional UART port, an adaptive transmit timing feature has been added. The feature works by monitoring the location of the incoming Manchester transitions at the RXL port with respect to the local clock to calculate a correction factor. This correction factor is then applied to the TXL port so that the outgoing Down path signal has similar timing characteristics to the incoming Up path signal. With this adaptive transmit timing, the interface between a conventional UART node and a Maxim proprietary battery-monitoring system node has a tolerance for baud rate mismatch that is much higher than that of the conventional receiver port alone, giving a high level of timing margin for direct connection applications.

Battery-Management UART Protocol

The Battery-Management UART Protocol uses the following features to maximize the integrity of the communications:

- All transmitted data bytes are Manchester-encoded, where each data bit is transmitted twice, with the second bit inverted (G.E. Thomas convention).
- Every transmitted character contains 12 bits, which include a start bit, a parity bit, and two stop bits.
- Read/write packets contain a CRC-8 Packet-Error Checking (PEC) byte
- Each packet is framed by a preamble character and stop character.
- Read packets contains a data-check byte for verifying the integrity of the transmission.

The protocol is also designed to minimize power consumption by allowing slave devices to shut down if the UART is idle for a specified period of time. The host must periodically transmit data to prevent shutdown, unless the SHDNL input is driven externally.

Command Packet

A command packet is defined as a sequence of UART characters originating at the host. Each packet starts with a preamble character, followed by data characters, and ending with a stop character, as shown in Figure 63. After sending a packet, the host either goes into idle mode or sends another packet.

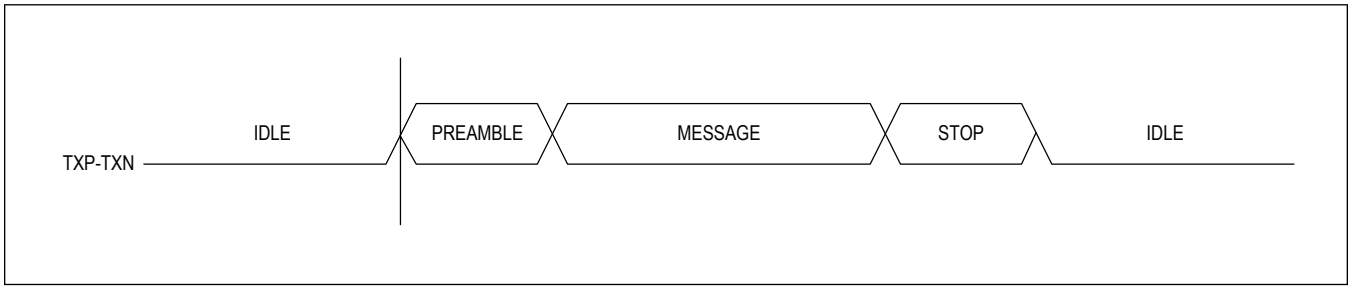


Figure 63. Command Packet

Preamble Character

The preamble is a framing character that signals the beginning of a command packet. It is transmitted as an unencoded 15h with a logic-one parity bit and a balanced duty cycle. If any bit(s) other than the stop bits deviate from the unique preamble sequence, then the character is not interpreted as a valid preamble, but rather as a data character. See Figure 64 for an example.

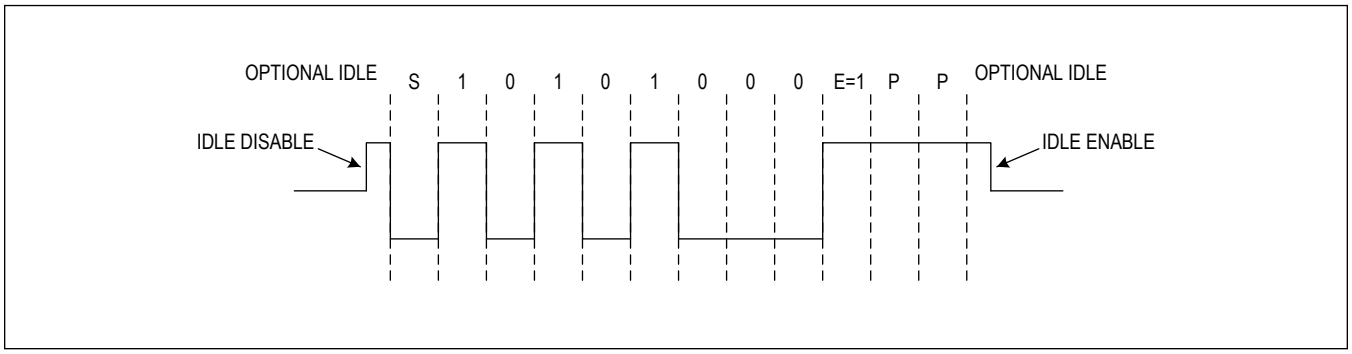


Figure 64. Preamble Character

Data Characters

Each data character contains a single-nibble (4-bit) payload, so two characters must be transmitted for each byte of data. All data is transmitted least-significant bit, least-significant nibble, and least-significant byte first. See Table 41, and Figure

65 for an example. The data itself is Manchester encoded, which means that each data bit is followed by its complement. If the UART detects a Manchester-encoding error in any received data character, it sets the ALRTMANUP bit. In a dual-UART configuration, a Manchester error in the Up path sets the ALRTMANUP, and a Manchester error in the Down path sets the ALRTMANDN.

The parity is even, meaning the parity bit's value should always result in an even number of logic-one bits in the character. Given the data is Manchester encoded and there are two stop bits, the parity bit for data characters is always transmitted as a logic zero. If the UART detects a parity error in any received data character, it sets the ALRTPARUP or ALRTPARDN bit in the STATUS2 register. All single-UART configurations set the ALRTPARUP bit. In a dual-UART configuration, a parity error in the Up path sets ALRTPARUP and a parity error in the Down path sets ALRTPARDN.

Table 41. Data Character Description

BIT	NAME	SYMBOL	DESCRIPTION
1	Start	S	First bit in character, always logic zero
2	Data0		Least significant bit of data nibble (true)
3	Data0/		Least significant bit of data nibble (inverted)
4	Data1		Data bit 1 (true)
5	Data1/		Data bit 1 (inverted)
6	Data2		Data bit 2 (true)
7	Data2/		Data bit 2 (inverted)
8	Data3		Most significant bit of data nibble (true)
9	Data3/		Most significant bit of data nibble (inverted)
10	Parity	E	Always logic zero (even parity)
11	Stop	P	Always logic one
12	Stop	P	Last bit in character, always logic one

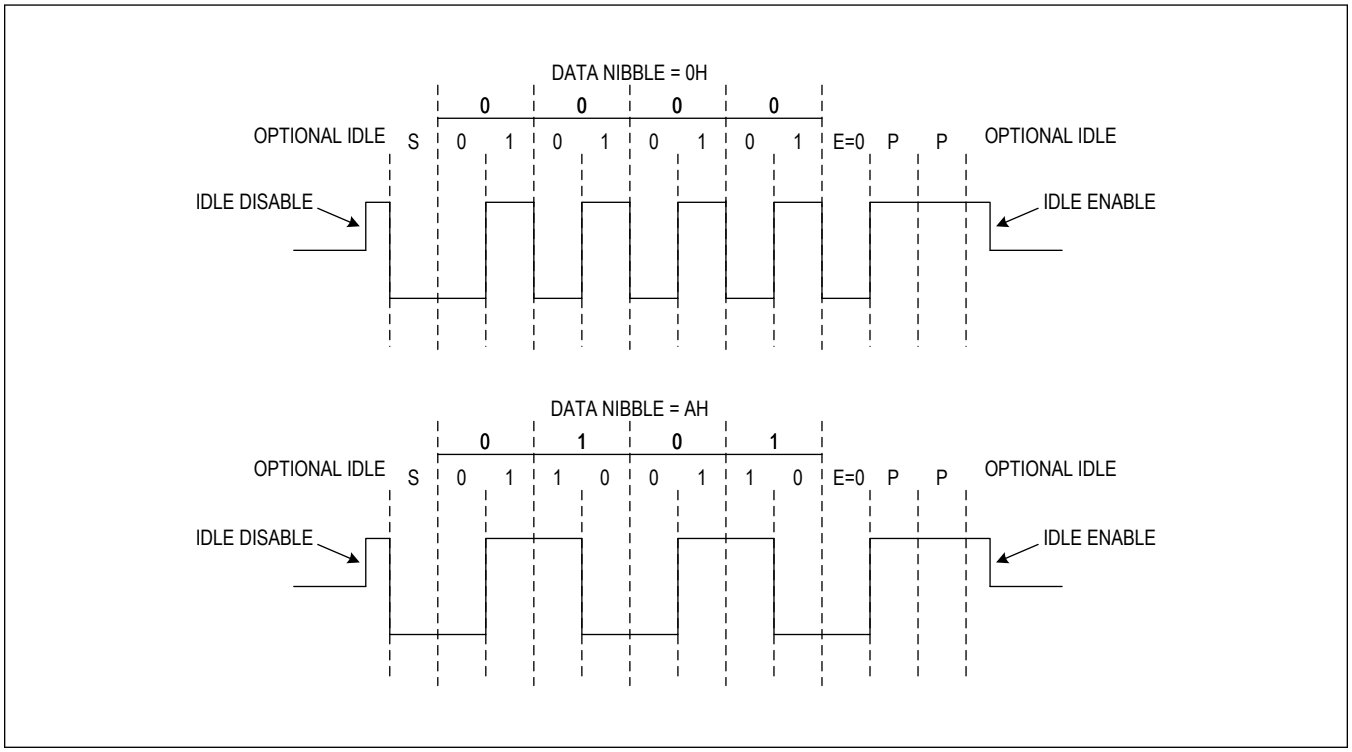


Figure 65. Data Characters

Stop Character

The stop character is a framing character that signals the end of a command packet. It is transmitted as an unencoded 54h with a logic-one parity bit and a balanced duty cycle.

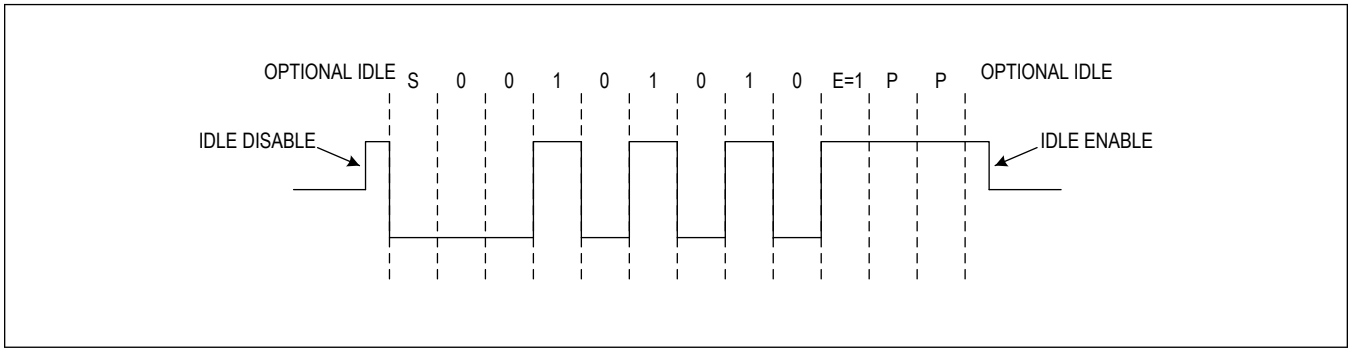


Figure 66. Stop Character

UART Idle Mode

In the low-Z (default) idle mode, the transmitter outputs are both driven to 0V as shown in Figure 67. In the high-Z idle mode, the transmitter outputs are not driven by the UART. The MAX17841B interface automatically places its transmitter in idle mode immediately after each command packet and remains in idle mode until either the next command packet is sent or it goes into keep-alive mode sending periodic stop characters to prevent the daisy-chain device(s) from going into

shutdown.

UART Communication Mode

When transitioning from idle mode to communication mode, the TXP pin must be pulled high (logic one) prior to signaling the start bit (logic zero) as shown in Figure 67. The duration of the logic one is minimized to maintain a balanced duty-cycle while still meeting the timing specification. When transitioning from the stop bit back to idle mode, the delay, if any, is also minimized.

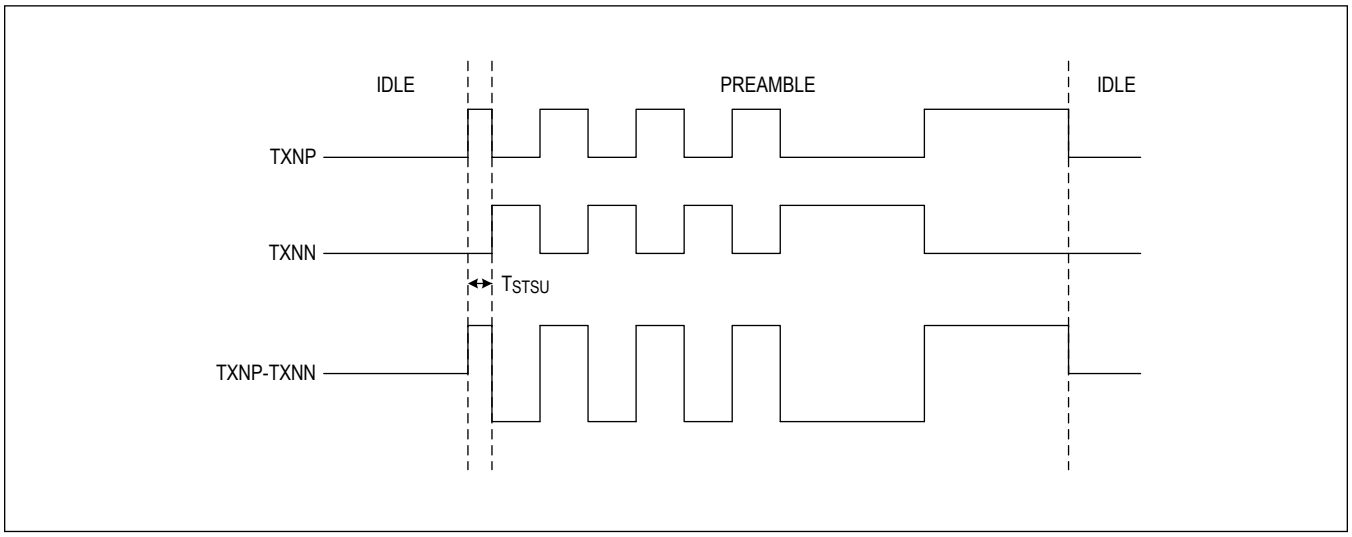


Figure 67. Communication Mode

Data Types

The Battery-Management UART Protocol employs several different data types as described in Table 42.

Table 42. Data Types

DATA TYPE	DESCRIPTION
Command byte	A byte defining the command packet type, generally either a READ or a WRITE
Register address	A byte defining the register address to be read from or written to
Register data	Register data bytes being read from or written to
Data-check byte	An error and alert-status byte sent and returned with all reads
Packet-error checking byte	A packet-rrror checking (PEC) byte sent and returned with every packet except HELLOALL
Alive-counter	A byte functioning as a device counter on all reads and writes, if ALIVECNTEN=1
Fill byte	Bytes transmitted in READALL and READBLOCK command packets (for clocking purposes only)

Command Bytes

The Battery-Management UART Protocol supports eight command types summarized in Table 43.

Table 43. Command Packet Types

COMMAND	DESCRIPTION	DATA-CHECK	PEC	ALIVE-COUNTER	PACKET SIZE (CHARACTERS)
HELLOALL	Writes a unique device address to each device in the daisy chain. Required for system initialization.	No	No	No	8

Table 43. Command Packet Types (continued)

COMMAND	DESCRIPTION	DATA-CHECK	PEC	ALIVE-COUNTER	PACKET SIZE (CHARACTERS)
WRITEALL	Writes a specific register in all devices.	No	Yes	Yes	14
WRITEDEVICE	Writes a specific register in a single device.	No	Yes	Yes	14
READALL	Reads a specific register from all devices.	Yes	Yes	Yes	12 + (4z)
READDEVICE	Reads a specific register from a single device.	Yes	Yes	Yes	16
READBLOCK	Reads a set of registers from a single device	Yes	Yes	Yes	14 + (4* BS)
UPHOST	Makes the UP path the master in a DUAL UART configuration. Sets bit field UARTHOST to 0b1	No	Yes	No	10
DOWNHOST	Makes the DOWN path the master in a DUAL UART configuration. Sets bit field UARTHOST to 0b0	No	Yes	No	10
ALERTPACKET	Reads and logically ORs the STATUS1 register and from all devices. Writes a unique bit location for each daisy chain position which contains a fault as described in the STATUS1 register.	No	Yes	No	18

Note: z = total number of devices, ALIVECNTEN = 1, packet size includes framing characters

* Block size[4:0] = 1-32, which is the number of registers read.

Command Byte Encoding

Command bytes encoding is described in Table 44. For READDEVICE and WRITEDEVICE commands, the device address is encoded in the command byte. The device ignores those commands containing a device address other than its own.

Table 44. Battery Management Protocol Command Byte Encoding

COMMAND	BYTE*	7	6	5	4	3	2	1	0
HELLOALL	57h	0	1	0	1	0	1	1	1
ALERTPACKET	21h	0	0	1	0	0	0	0	1
WRITEDEVICE	04h	DA4	DA3	DA2	DA1	DA0	1	0	0
WRITEALL	02h	0	0	0	0	0	0	1	0
READDEVICE	05h	DA4	DA3	DA2	DA1	DA0	1	0	1
READALL	03h	0	0	0	0	0	0	1	1
READBLOCK	06h	BS4	BS3	BS2	BS1	BS0	1	1	0
DOWNHOST	09h	0	0	0	0	1	0	0	1
UPHOST	08h	0	0	0	0	1	0	0	0

*Assumes DA[4:0] = 0x00 where DA[4:0] is the device address in the ADDRESS register.

BS[4:0] = Block size (1-32).

Register Addresses

All register addresses are single-byte quantities and are defined in the Register Map. In general, if the register or device address in a received command is not a valid address for the device, the device will ignore the read or write and simply pass-through the packet to the next device.

Register Data

All registers are 16-bit words (2 data bytes) and are defined in the Register Map.

Data-Check Byte

The host uses the returned data-check byte to promptly determine if any communication errors occurred during the packet transmission and to check if alert flags are set in any devices, as shown in Table 45. Individual alert conditions can be masked out of the Data-Check Byte using settings in ALRTIRQEN; however, the underlying alert information will always be available for read back in the STATUS1 register. The data-check byte is returned by the READALL, READDEVICE, and READBLOCK commands. For READDEVICE, the data-check byte is updated only by the addressed device.

The Data-Check Byte sent by the host is a seed value normally set to 00h, although non-zero values may be used as a diagnostic. Each device logically ORs the received Data-Check Byte with its own status and transmits it to the next device. A PEC error detected by any device will set the appropriate ALRTPECUP or ALRTPECDN bit in the STATUS2 register, and thus ALRTPEC roll-up bit in the STATUS1 register. The device will also set the PEC Error bit in the Data-Check Byte within the associated path's command packet, as described below.

Table 45. Data-Check Byte

BIT	NAME	DESCRIPTION
7	PEC ERROR	PEC Error detected during the current transaction on the Up/Down path issuing this bit.
6	ALRTFMEA	(ALRTFMEA1 & FMEA1ALRTEN) or (ALRTFMEA2 & FMEA2ALRTEN)
5	ALRTSTATUS	ALRTRST or (ALRTMSMTCH & MSMTCHALRTEN) or (ALRTBLKOVST & BLKOVALRTEN) or (ALRTBLKUVST & BLKUVALRTEN) or (ALRTINTRFC & INTRFCALRTEN) or (ALRTCAL & CALALRTEN) or (ALRTCBAL & CBALALRTEN)
4	AUXOV (UT)	(ALRTAUXOVST & AUXOVSTALRTEN)
3	AUXUV (OT)	(ALRTAUXUVST & AUXUVSTALRTEN)
2	CELLOV	(ALRTCELLOVST & CELLOVSTALRTEN)
1	CELLUV	(ALRTCELLUVST & CELLUVSTALRTEN)
0	OVERCURRENT	(ALRTCSAST & CSASTALRTEN)

Note: STATUS1[15]:ALRTSCAN is a procedural notification bit and is intentionally not included in the DCByte; it is available for inclusion in the ALERT Interface, to support interrupt-driven applications. STATUS1[14]:ALRTRST indicates a POR condition, and thus cannot be masked. STATUS1[5]:ALRTPEC is intentionally not included in the DCByte.

PEC Byte

The PEC byte is a CRC-8 Packet-Error Check sent by the host with all read and write commands. If any device receives an invalid PEC byte, it sets the ALRTPECUP, or ALRTPECDN bit in the STATUS2 register, and also ALRTPEC bit in the STATUS1 register. All single UART configurations will set ALRTPECUP bit. In a Dual-UART configuration, a PEC error in the Up path will set ALRTPECUP, and a PEC error in the Down path will set the ALRTPECDN. During any write transaction, a device does not execute the write command internally unless the received PEC matches the expected calculated value. For read commands, the device must return its own calculated PEC byte based on the returned data. The host should verify that the received PEC byte matches the calculated value and if an error is indicated, the data should be discarded. See *Application Information* section for details on the PEC calculation.

Alive-Counter Byte

The alive-counter byte is the last data byte of the command packets (except HELLOALL, UPHOST, and DOWNHOST) if the ALIVECNTEN bit is set in the DEVCFG1 register. The host typically transmits the alive-counter seed value as 00h, but any value is permitted. For WRITEALL or READALL commands, each device will re-transmit the alive-counter incremented by one. For WRITEDEVICE or READDEVICE commands, only the addressed device will increment it. The alive-counter is not used in the HELLOALL, UPHOST, and DOWNHOST commands. If the alive-counter reaches FFh, the next device increments it to 00h.

Since the alive-counter comes after the PEC byte, an incorrect PEC value will not affect the incrementing of the alive-counter byte. Also, the PEC calculation does not include the alive-counter byte. The host should verify that the alive-counter equals the original seed value plus the number of devices and considering that if the alive-counter reaches FFh,

the next device increments it to 00h.

Fill Bytes

In the READALL command, the host sends two fill bytes for each device in the daisy chain. The fill bytes are the locations within the packet and are used by the device to place the read data. The fill byte values transmitted by the MAX17841B interface alternate between C2h and D3h. As the command packet propagates through the device, the device overwrites the appropriate fill bytes with the register data. The device uses the ADDRESS register to determine which specific fill bytes in the packet are to be overwritten.

For a READBLOCK command, the number of fill bytes sent is equal to the read data block size.

For a READDEVICE command, only two fill bytes are required since only one device responds (returning two data bytes). Also, fill bytes are not required for write commands because the data received is exactly the same as the data re-transmitted.

Battery-Management UART Protocol Commands

HELLOALL Command

The HELLOALL command initializes the daisy chain device addresses after a POR. The device addresses are stored in the DA[4:0] bits of the ADDRESS register with the highest address being 0x1F. Thus, a maximum of 32 devices may be addressed.

The device address bits (DA[4:0]) in the HELLOALL Command Packet are seeded by host microcontroller. The command will proceed to the first device of the daisy chain and will be stored in that device's DA bits of the ADDRESS register. The first device will then increment or decrement the HELLOALL command packet DA[4:0] bitfield according the UARTHOST configuration settling (refer to *HELLOALL Operation in Dual UART Configuration* Section). Thus, the initial seeded value will correspond the first devices address of the daisy chain. The command will continue to propagate to the next device until it returns to the host at which point the host will be able to determine the total number of devices in the daisy chain for subsequent READALL, READ DEVICE, READ BLOCK commands.

Table 46. HELLOALL Command Packet

HELLOALL
Preamble
57h
00h
{0b000,DA[4:0]}
Stop

HELLOALL Operation in Dual-UART Configuration

By default, dual-UART operation is configured with the primary communication path being the Up path (refer to the UARTCFG and UARTHOST bits in the DEVCFG1 register for details about defaults and possible configurations), where the Up path is defined as transmission from the TXU port to the RXL port. The DA[4:0] bits in the HELLOALL command packet are incremented as they progress up the daisy-chain. Thus, when the HELLOALL is received by the host microcontroller, the DA[4:0] value returned is one greater than the address assigned to the top device.

It is recommended that the host seeds the initial address of the Up path at a value of 0x00. This configuration applies to the first address of the daisy chain at the same value of the default condition of the bottom address (BA bits in the ADDRESS register). Therefore, it is not necessary to write the bottom address BA[4:0] to all the devices. The host microcontroller should never set the bottom address at a value that would result in the device address exceeding 0x1F

Note: The device address is only stored and incremented in the Up path, and then passes through the Down path, leaving the device address unaffected. As such, if the hardware is configured as a single daisy-chain and the UART is looped back using the Down path, the UARTHOST configuration prevents the Down path from changing the device address already determined.

Table 47. HELLOALL Up Path Sequencing

HELLOALL UP PATH SEQUENCING (z = TOTAL NUMBER OF DEVICES)			
HOST TX	**DEVICE (n) RXL**	**DEVICE (n) TXU**	**HOST RX**
Preamble	Preamble	Preamble	Preamble
57h	57h	57h	57h
00h	00h	00h	00h
{0b000,DA[4:0]}	{0b000,DA[4:0]+n-1}	{0b000,DA[4:0]+n}	{0b000,DA[4:0]+z}
Stop	Stop	Stop	Stop

The HELLOALL command packet can also be applied through the Down path, where the Down path is defined as transmission from the TXL port to the RXU port. For proper operation, the host microcontroller must first send the DOWNHOST command through the Down path prior to sending the HELLOALL.

The device address in the HELLOALL command packet is decremented as it progresses down the daisy chain. Therefore, the address of the top daisy chain (first device in the Down path) will be the value that is seeded in the DA[4:0] bits of the HELLOALL command packet. This top daisy-chain device proceeds to decrement the DA[4:0] and propagates the value down the daisy chain. When the HELLOALL is received by the host microcontroller, the DA[4:0] value returned is one less than the address assigned to the bottom device. The host microcontroller should never set the top address at a value which would result in a DA[4:0] decremented below 0x0.

After the HELLOALL is processed, the TA bits (Top Address bits) in the ADDRESS register must be set to the initial DA[4:0] seeded value.

It is recommended that the host seeds the initial address of the Down path at a value equal to the number of devices in the daisy chain, such that the bottom address is 0x00. This configuration ensures that whether the HELLOALL is sent through the Up path or Down path, the device address remains the same, which is ideal for consistency with the addressing of the READDEVICE, and READALL commands.

Table 48. HELLOALL Down Path Sequencing

HELLOALL SEQUENCING (z = TOTAL NUMBER OF DEVICES)			
HOST TX	**DEVICE (n) RXU**	**DEVICE (n) TXL**	**HOST RX**
Preamble	Preamble	Preamble	Preamble
57h	57h	57h	57h
00h	00h	00h	00h
{0b000,ADDR[4:0]}	{0b000,ADDR[4:0]-(n-1)}	{0b000,ADDR[4:0]-n}	{0b000,ADDR[4:0]-z}
Stop	Stop	Stop	Stop

HELLOALL Operation In Single-UART Configuraton

In single-UART configuration, the HELLOALL will be processed the same as in the dual-UART Up path.

Special considerations exist if the host desires to use internal loopback instead of external loopback. The first HELLOALL command is not returned to the host because the internal loopback (UARTCFG) for the top device has not yet been written. If the number of devices is known to the host, the host can use a WRITEDEVICE to set the internal loopback bit on the last device and then verify with a READALL. If the number of devices is unknown, the internal loopback bit must be set on the first device, verified and then cleared. It can then be set on the second device and verified, and so on incrementally until there is no response (end of stack). With the number of devices known, the loopback bit can be reset on the top device and all ADDRESS registers verified.

HELLOALL Address Lock

When a device receives a valid HELLOALL command, it clears the ADDRUNLOCK bit of the ADDRESS register. When this bit is 0, HELLOALL commands are ignored to prevent inadvertently changing any device address. To reconfigure the device address, the ADDRUNLOCK bit must first be set to 1, or a POR event must occur. After configuring the device

addresses, they should be verified using the READALL command.

WRITEALL Command

The WRITEALL command writes a 16-bit value to a specified register in all daisy-chain devices. Since most configuration information is common to all the devices, this command allows faster setup than writing to each device individually. If the register address is not valid for the device, the command is ignored. The command sequence is shown in Table 49.

The register value is written immediately after the valid PEC byte is received or, if NOPEC is set, after the last byte is received. If the received PEC byte does not match the internal calculation, the command is not executed, but is still forwarded to the next device. The PEC is calculated from the first four bytes of the command starting after the preamble. If any device receives an invalid PEC byte, it sets the ALRTPECUP, or ALRTPECDN bit in the STATUS2 register, and also ALRTPEC bit in the STATUS1 register. All single UART configurations will set ALRTPECUP bit. In a DUAL UART configuration, a PEC error in the UP path will set ALRTPECUP, and a PEC error in the DOWN path will set the ALRTPECDN.

Table 49. WRITEALL Sequencing (Unchanged by Daisy Chain)

HOST TX	DEVICE(n) RXL (UP PATH) OR RXU (DOWN PATH)	DEVICE(n) TXU (UP PATH) OR TXL (DOWN PATH)	HOST RX
Preamble	Preamble	Preamble	Preamble
02h	02h	02h	02h
[REG ADDR]	[REG ADDR]	[REG ADDR]	[REG ADDR]
[DATA LSB]	[DATA LSB]	[DATA LSB]	[DATA LSB]
[DATA MSB]	[DATA MSB]	[DATA MSB]	[DATA MSB]
[PEC]	[PEC]	[PEC]	[PEC]
[ALIVE]*	[ALIVE]*	[ALIVE]*	[ALIVE]*
Stop	Stop	Stop	Stop

* If alive-counter mode is enabled

WRITEDEVICE Command

The WRITEDEVICE command writes a 16-bit value to the specified register in the addressed device only. If the register address is not valid for the device, the command is ignored. The command sequence is shown in Table 50.

The register value is written immediately after the valid PEC byte is received or, if NOPEC is set, after the last byte is received. If the received PEC byte does not match the internal calculation, the command is not executed, but is still forwarded to the next device. The PEC is calculated from the first four bytes of the command starting after the preamble. If the addressed device receives an invalid PEC byte, it sets the ALRTPECUP, or ALRTPECDN bit in the STATUS2 register, and also ALRTPEC bit in the STATUS1 register. All single-UART configurations will set ALRTPECUP bit. In a dual-UART configuration, a PEC error in the UP path will set ALRTPECUP, and a PEC error in the DOWN path will set the ALRTPECDN. A PEC error can only occur in the addressed device.

Table 50. WRITEDEVICE Sequencing (Unchanged by Daisy Chain)

HOST TX	DEVICE RXL (UP PATH) OR RXU (DOWN PATH)	DEVICE TXU(UP PATH) OR TXL (DOWN PATH)	HOST RX
Preamble	Preamble	Preamble	Preamble
{(DA[4:0]),0b100}	{(DA[4:0]),0b100}	{(DA[4:0]),0b100}	{(DA[4:0]),0b100}
[REG ADDR]	[REG ADDR]	[REG ADDR]	[REG ADDR]
[DATA LSB]	[DATA LSB]	[DATA LSB]	[DATA LSB]
[DATA MSB]	[DATA MSB]	[DATA MSB]	[DATA MSB]

Table 50. WRITEDEVICE Sequencing (Unchanged by Daisy Chain) (continued)

HOST TX	DEVICE RXL (UP PATH) OR RXU (DOWN PATH)	DEVICE TXU(UP PATH) OR TXL (DOWN PATH)	HOST RX
[PEC]	[PEC]	[PEC]	[PEC]
[ALIVE]*	[ALIVE]*	[ALIVE]*	[ALIVE]*
Stop	Stop	Stop	Stop

* If alive-counter mode is enabled

READALL Command

The READALL command returns register data from the specified register for all daisy-chain devices. The data for the first device (connected to host) is returned last. The command sequence is shown in Table 51 and Table 52. If the received PEC byte does not match the calculated value, the UART sets the ALRTPECUP, or ALRTPECDN bit in the STATUS2 register, and also ALRTPEC bit in the STATUS1 register. All single UART configurations will set ALRTPECUP bit. In a DUAL UART configuration, a PEC error in the UP path will set ALRTPECUP, and a PEC error in the DOWN path will set the ALRTPECDN. However, the command proceeds to the next device in the daisy chain. A Manchester error immediately switches the data propagation from read mode to write (pass-through) mode insuring that the Manchester error is propagated through the daisy chain and back to the host.

Table 51. READALL Command Sequencing In Single-UART or Dual-UART Up Path (z = Number of Devices)

HOST TX	DEVICE(n) RXL	DEVICE(n) TXU	HOST RX
Preamble	Preamble	Preamble	Preamble
03h	03h	03h	03h
[REG ADDR]	[REG ADDR]	[DATA ADDR]	[REG ADDR]
[DC] = 0x00	[DATA LSB(n-1)]	[DATA LSB(n)]	[DATA LSB(z)] = [DATA LSB(TA)]
[PEC]	[DATA MSB(n-1)]	[DATA MSB(n)]	[DATA MSB(z)] = [DATA MSB(TA)]
[ALIVE]*	...	...	[DATA LSB(z-1)] = [DATA LSB(TA-1)]
[FD(1) C2h]	...	...	[DATA MSB(z-1)] =[DATA MSB(TA-1)]
[FD(1) D3h]	[DATA LSB(1)] = [DATA LSB(BA)]	[DATA LSB(1)] = [DATA LSB(BA)]	...
[FD(2) C2h]	[DATA MSB(1)] = [DATA MSB(BA)]	[DATA MSB(1)] = [DATA MSB(BA)]	...
[FD(2) D3h]	[DC]	[DC]	...
...	[PEC]	[PEC]	...
...	[ALIVE]*	[ALIVE]*	...
...	[FD(1) C2h]	[FD(1) C2h]	...
...	[FD(1) D3h]	[FD(1) D3h]	[DATA LSB(1)] = [DATA LSB(BA)]
...	...	...	[DATA MSB(1)] = [DATA MSB(BA)]
...	...	...	[DC]
[FD(z) C2h]	[FD(z-n) C2h]	[FD(z-n-1) C2h]	[PEC]
[FD(z) D3h]	[FD(z-n) D3h]	[FD(z-n-1) D3h]	[ALIVE]*
Stop	Stop	Stop	Stop

Table 51. READALL Command Sequencing In Single-UART or Dual-UART Up Path (z = Number of Devices) (continued)

HOST TX	DEVICE(n) RXL	DEVICE(n) TXU	HOST RX
12+(4 x z) characters	12+(4 x z) characters	12+(4 x z) characters	12+(4 x z) characters

* If alive-counter mode is enabled.

Table 52. READALL Command Sequencing In Dual-UART Down Path (z = Number of Devices)

HOST TX	DEVICE(n) RXU	DEVICE(n) TXL	HOST RX
Preamble	Preamble	Preamble	Preamble
03h	03h	03h	03h
[REG ADDR]	[REG ADDR]	[DATA ADDR]	[REG ADDR]
[DC] = 0x00	[DATA LSB(n-1)]	[DATA LSB(n)]	[DATA LSB(z)] = [DATA LSB(BA)]
[PEC]	[DATA MSB(n-1)]	[DATA MSB(n)]	[DATA MSB(z)] = [DATA MSB(BA)]
[ALIVE]*	...	...	[DATA LSB(z-1)] = [DATA LSB(BA +1)]
[FD(1) C2h]	...	...	[DATA MSB(z-1)] = [DATA MSB(BA +1)]
[FD(1) D3h]	[DATA LSB(1)]= [DATA LSB(TA)]	[DATA LSB(1)]= [DATA LSB(TA)]	...
[FD(2) C2h]	[DATA MSB(1)] =[DATA MSB(TA)]	[DATA MSB(1)] =[DATA MSB(TA)]	...
[FD(2) D3h]	[DC]	[DC]	...
...	[PEC]	[PEC]	...
...	[ALIVE]*	[ALIVE]*	...
...	[FD(1) C2h]	[FD(1) C2h]	...
...	[FD(1) D3h]	[FD(1) D3h]	[DATA LSB(1)] = [DATA LSB(TA)]
...	...	...	[DATA MSB(1)] =[DATA MSB(TA)]
...	...	...	[DC]
[FD(z) C2h]	[FD(z-n) C2h]	[FD(z-n-1) C2h]	[PEC]
[FD(z) D3h]	[FD(z-n) D3h]	[FD(z-n-1) D3h]	[ALIVE]*
Stop	Stop	Stop	Stop
12+(4 x z) characters	12+(4 x z) characters	12+(4 x z) characters	12+(4 x z) characters

*If alive-counter mode is enabled.

The fill-byte values transmitted by the MAX17841B interface alternate between C2h and D3h as shown. As the packet propagates through the device, the device re-transmits it in the order shown in the sequencing table (device TXU column). The device knows which bytes to overwrite since its ADDRESS register contains the top and bottom device addresses, as well as its own device address, and therefore it knows where in the data stream it belongs.

READDEVICE Command

The READDEVICE command returns a 16-bit word read from the specified register in the addressed device only. If the register address is not valid for the device, the command is ignored. The command sequence is shown in Table 53 and Table 54.

The command packet is forwarded up the daisy chain until it reaches the addressed device. The addressed device overwrites the received fill bytes with the two bytes of register data and forwards the packet to the next device. The alive-counter byte (if enabled) is only incremented by the addressed device. A Manchester error immediately switches the data propagation from read mode to write (pass-through) mode insuring that the Manchester error is propagated through the daisy-chain and back to the host.

Table 53. READDEVICE Sequencing In Single-UART or Dual-UART Up Path

HOST TX	DEVICE RXL	DEVICE TXU	HOST RX
Preamble	Preamble	Preamble	Preamble
{DA[4:0], 0b101}	{DA[4:0], 0b101}	{DA[4:0], 0b101}	{DA[4:0], 0b101}
[REG ADDR]	[REG ADDR]	[REG ADDR]	[REG ADDR]
[DC]	[DC]	[DATA LSB]	[DATA LSB]
[PEC]	[PEC]	[DATA MSB]	[DATA MSB]
[ALIVE]*	[ALIVE]*	[DC]	[DC]
[FD(1) C2h]	[FD(1) C2h]	[PEC]	[PEC]
[FD(1) D3h]	[FD(1) D3h]	[ALIVE]*	[ALIVE]*
Stop	Stop	Stop	Stop
16 characters	16 characters	16 characters	16 characters

*If alive-counter mode is enabled

Table 54. READDEVICE Sequencing In Dual-UART Down Path

HOST TX	DEVICE RXU	DEVICE TXL	HOST RX
Preamble	Preamble	Preamble	Preamble
{DA[4:0], 0b101}	{DA[4:0], 0b101}	{DA[4:0], 0b101}	{DA[4:0], 0b101}
[REG ADDR]	[REG ADDR]	[REG ADDR]	[REG ADDR]
[DC]	[DC]	[DATA LSB]	[DATA LSB]
[PEC]	[PEC]	[DATA MSB]	[DATA MSB]
[ALIVE]*	[ALIVE]*	[DC]	[DC]
[FD(1) C2h]	[FD(1) C2h]	[PEC]	[PEC]
[FD(1) D3h]	[FD(1) D3h]	[ALIVE]*	[ALIVE]*
Stop	Stop	Stop	Stop
16 characters	16 characters	16 characters	16 characters

*If alive-counter mode is enabled

READBLOCK Command

The READBLOCK command returns an 18-byte read from the specified register for a block size of 1 in the addressed device only. If the register address is not valid for the device, it returns 0 for any invalid addresses. If the Device Address is not valid, the command will be ignored. The command sequences for a block size of 1 are shown in Table 55 and Table 56. The command sequences for a block size of 2 are shown in Table 57 and Table 58. The command packet is forwarded up the daisy chain until it reaches the addressed device. The addressed device overwrites the received fill bytes with the two bytes of register data (from a single device) and forwards the packet to the next device. The alive-counter byte (if enabled) is only incremented by the addressed device. A Manchester error immediately switches the data propagation from read mode to write (pass-through) mode, ensuring that the Manchester error is propagated through the daisy chain and back to the host.

Table 55. READBLOCK Sequencing In Single-UART or Dual-UART Up Path Block Size = 1

HOST TX	DEVICE RXL	DEVICE TXU	HOST RX
Preamble	Preamble	Preamble	Preamble
{BS[4:0], 3b110}	{BS[4:0], 3b110}	{BS[4:0], 3b110}	{BS[4:0], 3b110}
[DEVICE ADDR]	[DEVICE ADDR]	[DEVICE ADDR]	[DEVICE ADDR]
[REG ADDR]	[REG ADDR]	[REG ADDR]	[REG ADDR]
[DC]	[DC]	[DATA LSB]	[DATA LSB]
[PEC]	[PEC]	[DATA MSB]	[DATA MSB]
[ALIVE]*	[ALIVE]*	[DC]	[DC]
[FD(1) C2h]	[FD(1) C2h]	[PEC]	[PEC]
[FD(1) D3h]	[FD(1) D3h]	[ALIVE]*	[ALIVE]*
Stop	Stop	Stop	Stop
18 characters	18 characters	18 characters	18 characters

* If alive-counter mode is enabled

Table 56. READBLOCK Sequencing In Dual-UART Down Path Block Size = 1

HOST TX	DEVICE RXU	DEVICE TXL	HOST RX
Preamble	Preamble	Preamble	Preamble
{BS[4:0], 3b110}	{BS[4:0], 3b110}	{BS[4:0], 3b110}	{BS[4:0], 3b110}
[DEVICE ADDR]	[DEVICE ADDR]	[DEVICE ADDR]	[DEVICE ADDR]
[REG ADDR]	[REG ADDR]	[REG ADDR]	[REG ADDR]
[DC]	[DC]	[DATA LSB]	[DATA LSB]
[PEC]	[PEC]	[DATA MSB]	[DATA MSB]
[ALIVE]*	[ALIVE]*	[DC]	[DC]
[FD(1) C2h]	[FD(1) C2h]	[PEC]	[PEC]
[FD(1) D3h]	[FD(1) D3h]	[ALIVE]*	[ALIVE]*
Stop	Stop	Stop	Stop
18 characters	18 characters	18 characters	18 characters

* If alive-counter mode is enabled.

Table 57. READBLOCK Sequencing In Single-UART or Dual-UART Up Path Block Size = 2

HOST TX	DEVICE RXL	DEVICE TXU	HOST RX
Preamble	Preamble	Preamble	Preamble
{BS[4:0], 3b110}	{BS[4:0], 3b110}	{BS[4:0], 3b110}	{BS[4:0], 3b110}
[DEVICE ADDR]	[DEVICE ADDR]	[DEVICE ADDR]	[DEVICE ADDR]
[REG ADDR]	[REG ADDR]	[REG ADDR]	[REG ADDR]
[DC]	[DC]	[DATA0 LSB]	[DATA0 LSB]
[PEC]	[PEC]	[DAT0 MSB]	[DATA0 MSB]
[ALIVE]*	[ALIVE]*	[DATA1 LSB]	[DATA1 LSB]
[FD(1) C2h]	[FD(1) C2h]	[DATA1 MSB]	[DATA1 MSB]
[FD(1) D3h]	[FD(1) D3h]	[DC]	[DC]

Table 57. READBLOCK Sequencing In Single-UART or Dual-UART Up Path Block Size = 2 (continued)

HOST TX	DEVICE RXL	DEVICE TXU	HOST RX
[FD(1) C2h]	[FD(1) C2h]	[PEC]	[PEC]
[FD(1) D3h]	[FD(1) D3h]	[ALIVE]*	[ALIVE]*
Stop	Stop	Stop	Stop
22 characters	22 characters	22 characters	22 characters

* If alive-counter mode is enabled

Table 58. READBLOCK Sequencing In Single-UART or Dual-UART Down Path Block Size = 2

HOST TX	DEVICE RXU	DEVICE TXL	HOST RX
Preamble	Preamble	Preamble	Preamble
{BS[4:0], 3b110}	{BS[4:0], 3b110}	{BS[4:0], 3b110}	{BS[4:0], 3b110}
[DEVICE ADDR]	[DEVICE ADDR]	[DEVICE ADDR]	[DEVICE ADDR]
[REG ADDR]	[REG ADDR]	[REG ADDR]	[REG ADDR]
[DC]	[DC]	[DATA0 LSB]	[DATA0 LSB]
[PEC]	[PEC]	[DAT0 MSB]	[DATA0 MSB]
[ALIVE]*	[ALIVE]*	[DATA1 LSB]	[DATA1 LSB]
[FD(1) C2h]	[FD(1) C2h]	[DATA1 MSB]	[DATA1 MSB]
[FD(1) D3h]	[FD(1) D3h]	[DC]	[DC]
[FD(1) C2h]	[FD(1) C2h]	[PEC]	[PEC]
[FD(1) D3h]	[FD(1) D3h]	[ALIVE]*	[ALIVE]*
Stop	Stop	Stop	Stop
22 characters	22 characters	22 characters	22 characters

* If alive-counter mode is enabled.

DOWNHOST Command

Only one of the dual-UART paths (Up path or Down path) can be granted WRITE access through using the UPHOST or DOWNHOST commands, however, both paths have read access. The path that holds the WRITE access is specified using the UARTHOST register bit. By default only the Up Path has the WRITE access (UARTHOST = 1b1).

The DOWNHOST command is used when WRITE access is required to be passed from the Up path (UARTHOST = 1b1) to the Dpwn Path (UARTHOST = 1b1). Alternatively, the UPHOST command is used when WRITE access is required to be passed from the Down path to the Up path. The UPHOST command is detailed in a different section.

When the DOWNHOST command is sent, each device will modify the UARTHOST bit in the DEVCFG1 register to change master control as well as increments the DEVCOUNT variable as it sends the command to the next device, downstream, in the chain. The final value of DEVCOUNT received by the host will be equal to the initial DEVCOUNT plus total number of devices in the chain. If the DOWNHOST command is sent on the Up path, the command will pass through the device unmodified while leaving the UARTHOST unchanged; the ALRTDUALUART bit will also be set in the STATUS2 register, signifying that an invalid command was received. Additionally, If the DOWNHOST command is sent on the Down path while the Down path is designated as the master, then the command will pass through the device unmodified while leaving the UARTHOST unchanged with the down Path indication.

Note: The DOWNHOST command is relevant only when the device is configured in Dual-UART mode. Sending the DOWNHOST command outside of a dual-UART configuration will not have any effect on the device and the command is

passed through without changing the DEVCOUNT.

Table 59. DOWNHOST Sequencing (z = Total Number of Devices)

HOST Tx	DEVICE (n) RXU	DEVICE (n) TXL	HOST RX
Preamble	Preamble	Preamble	Preamble
09h	09h	09h	09h
00h	00h	00h	00h
{0b000,DEVCOUNT[4:0]}	{0b000,DEVCOUNT[4:0]+n-1}	{0b000,DEVCOUNT[4:0]+n}	{0b000,DEVCOUNT[4:0]+z}
Stop	Stop	Stop	Stop

UPHOST Command

Only one of the dual-UART paths (Up path or Down path) can be granted WRITE access using the UPHOST or DOWNHOST commands; however, both paths have read access. The path that holds the write access is specified using the UARTHOST register bit. By default, only the Up path has write access (UARTHOST = 1b1). See Table 60.

The UPHOST command is used when write access needs to be passed from the Down path (UARTHOST = 1b1) to the Up path (UARTHOST = 1b1). Alternatively, the DOWNHOST command is used when write access needs to be passed from the Up path to the Down path. See the DOWNHOST Command section for further detail.

When the UPHOST command is sent, each device modifies the UARTHOST bit in the DEVCFG1 register to change master control, and also increments the DEVCOUNT variable as it sends the command to the next device upstream in the chain. The final value of DEVCOUNT received by the host should be equal to the initial DEVCOUNT plus the total number of devices in the chain. If the UPHOST command is sent on the Down path, the command passes through the device unmodified, leaving the UARTHOST unchanged; the ALRTDUALUART bit will also be set in the STATUS2 register, signifying that an invalid command was received. Additionally, If the UPHOST command is sent on the Up path while the Up path is designated as the master, the command passes through the device unmodified, leaving the UARTHOST unchanged with the Up path indication.

Note: The DOWNHOST command is relevant only when the device is configured in dual-UART mode. Sending the DOWNHOST command outside of a dual-UART configuration will not have any effect on the device; the command is passed through unchanging the DEVCOUNT.

Table 60. UPHOST Sequencing (z = Total Number of Devices)

HOST Tx	DEVICE (n) RXL	DEVICE (n) TXU	HOST Rx
Preamble	Preamble	Preamble	Preamble
08h	08h	08h	08h
00h	00h	00h	00h
{0b000,DEVCOUNT[4:0]}	{0b000,DEVCOUNT[4:0]+n-1}	{0b000,DEVCOUNT[4:0]+n}	{0b000,DEVCOUNT[4:0]+z}
Stop	Stop	Stop	Stop

ALERTPACKET Command

The MAX17852 supports the transmission of an ALERT packet from either the host microcontroller or SPI-to-UART Bridge. This packet contains the alert Command Byte, daisy-chain module alert data address location (DA[4:0]), Alert Status byte, and the PEC byte of the protected data. See Table 61.

The module alert location is a 32-bit value that is split into four transmission data packets where each bit represents the device address (DA[4:0]) defined by the HELLOALL command. The Alert Status is the 16-bit output of the STATUS1 register, subject to masking via ALRTIRQEN, as described below. As the data passes through the daisy chain, the Module Alert Location will contain a unique identifier while the STATUS output will be logically OR'ed to communicate the alert type. This creates a method to quickly assess the module status and health with little host interaction.

Table 61. ALERTPACKET Sequencing

ALERT PACKET
Preamble
Command Byte (0x21)
Module Alert Location 1 {(DA[4:7]), (DA[0:3])}
Module Alert Location 2 {(DA[12:15]),(DA[8:11])}
Module Alert Location 3 {(DA[20:23]),(DA[16:19])}
Module Alert Location 4 {(DA[28:31]),(DA[24:27])}
[STATUS LSB]
[STATUS MSB]
[PEC]
Stop

SPI Interface

When a single device is used in a single battery pack application with no daisy chain, the host could use the SPI interface to communicate with the device. The host should set UARTSEL low. When UARTSEL is set high, the device uses the UART interface to communicate with the microprocessor.

Overview

The MAX17852 SPI interface is SPI/QSPI/Micro-wire/DSP compatible, ensuring compatible operation with standard microcontrollers (µCs) from a variety of manufacturers.

The µC always operate as the master, and is able to initiate read and write transactions to individual slave devices selected by a specific CSB connection. The operation and timing criteria of the SPI interface is shown in Figure 68. The MAX17852 will be programmed by a qualified 32-cycle SPI instruction framed by a CSB low interval.

The SCLK line should be driven by the master and distributed to all slave devices. Only the slave device with its CSB line held low will accept SCLK. SPI transactions to the slave devices are defined by SCLK rising edges. The start of the transaction is defined by the SCLK rising edge, following the CSB falling edge (subject to t_{CSH0} and t_{CSS0} timing criteria). Transactions including a number of SCLK rising edges not equal to 32 will not be qualified for execution (also based on t_{CSA}, t_{CSH1}, and t_{CSQ} timing criteria). Qualified transactions will be executed on the rising edge of CSB. In order to abort a transaction sequence, the rise of CSB must precede a qualified (32^{nd}) rising edge of SCLK (meeting the t_{CSA} timing requirement);

Note: An aborted command will result in the issuance of a SPI CLK Error.

The SDI line should be hooked up to a Master-Out-Slave-In (MOSI) port and distributed to all slave devices. SDI data is latched into the selected slave device on SCLK rising edges, subject to setup and hold criteria (t_{DS}, t_{DH}). The SDI content of the SPI transaction consists of four bytes for qualified transactions.

The SDO line should be hooked up to a Master-In-Slave-Out (MISO) port and distributed to all slave devices. SDO is actively driven by the selected slave device when CSB falls (t_{DOE} timing applies), initially presenting the MSB of the output data (the SPI_CRC_ERR bit for all transactions). Following the initial SCLK rising edge, SDO is updated in response to SCLK falling edges, conforming to hold and transition time criteria (t_{DOH}, t_{DOT}), allowing the µC to latch the data on SCLK rising edges. When CSB is high, the SDO line is high-impedance, allowing other slave devices to access the SDO bus.

Transactions lasting longer than the time-out interval (t_{TO}), measured from CSB falling edge to CSB rising edge, will not be qualified or executed.

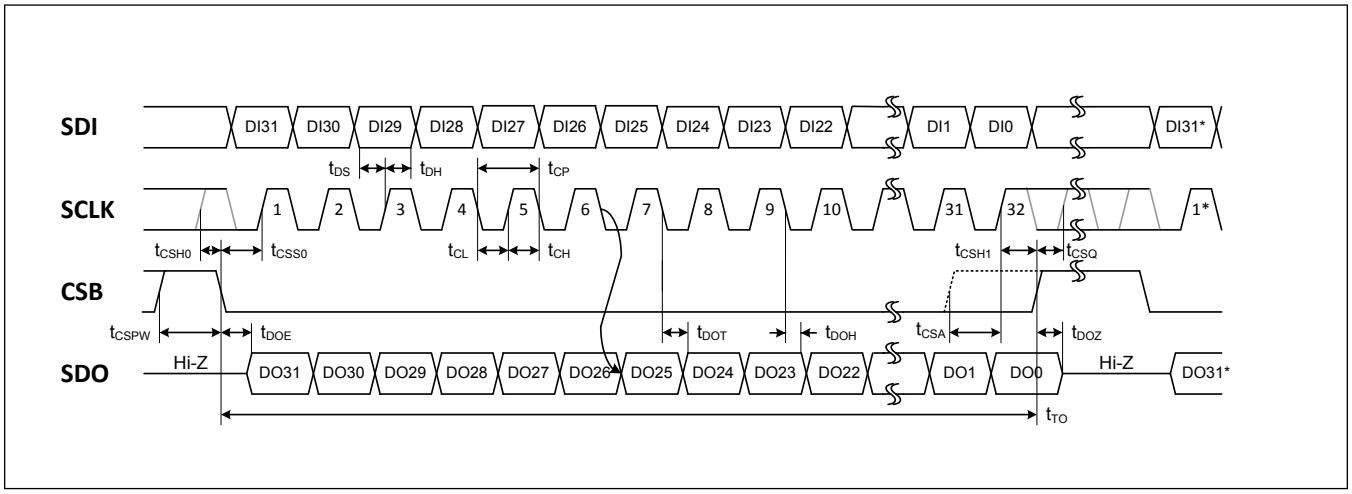


Figure 68. SPI Timing Diagram

System-Level Connection

Following the above guidelines, the SPI interface allows multiple devices to share the SPI interface, with the active device for the transaction being selected by pulling its unique CSB port low. Note that each slave device in on the interface requires a dedicated CSB line from the Master. The SCLK, SDI, and SDO lines are common to all devices. A total of (3 + N) lines is required for an interface supporting N slave devices. Transaction qualification criteria remain in effect, and in write mode, the device will only execute instructions exactly 32 bits in length. In read mode, it will return the requested data through SDO during the read-mode transaction. A standard connection example is show in Figure 69.

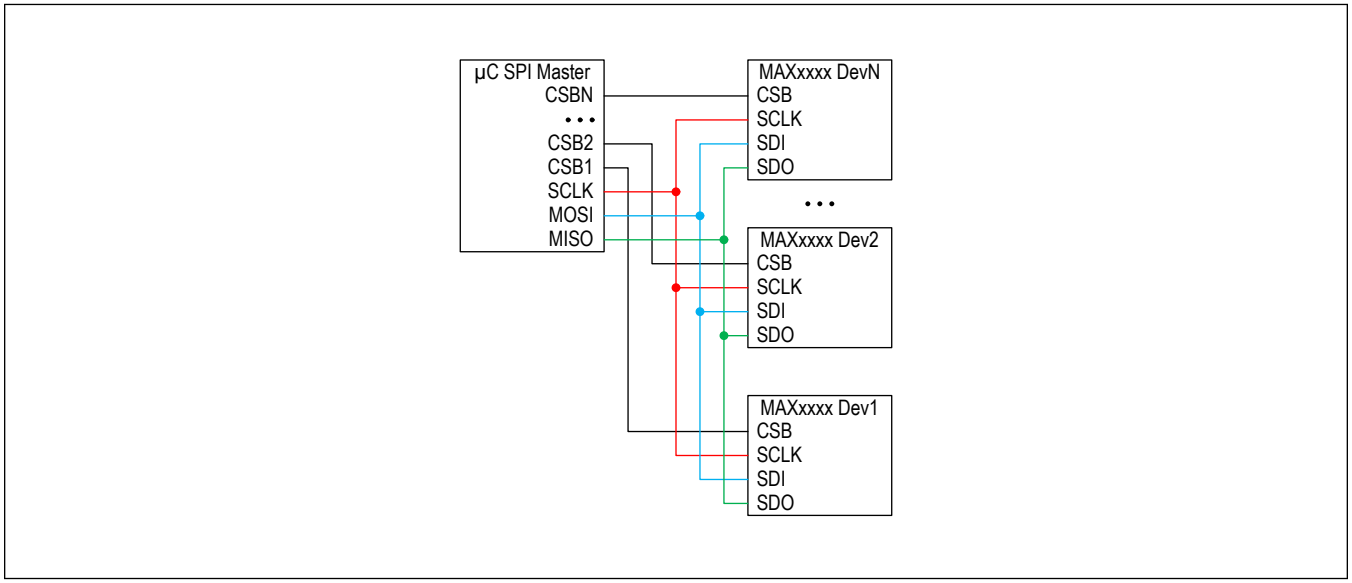


Figure 69. SPI Device Connection

Supported Transaction Alignments

The MAX17852 is capable of supporting SPI transactions with masters using either (CPOL = 0 and CPHA = 0) or (CPOL

= 1 and CPHA = 1). Examples of these transactions are shown in Figure 70.

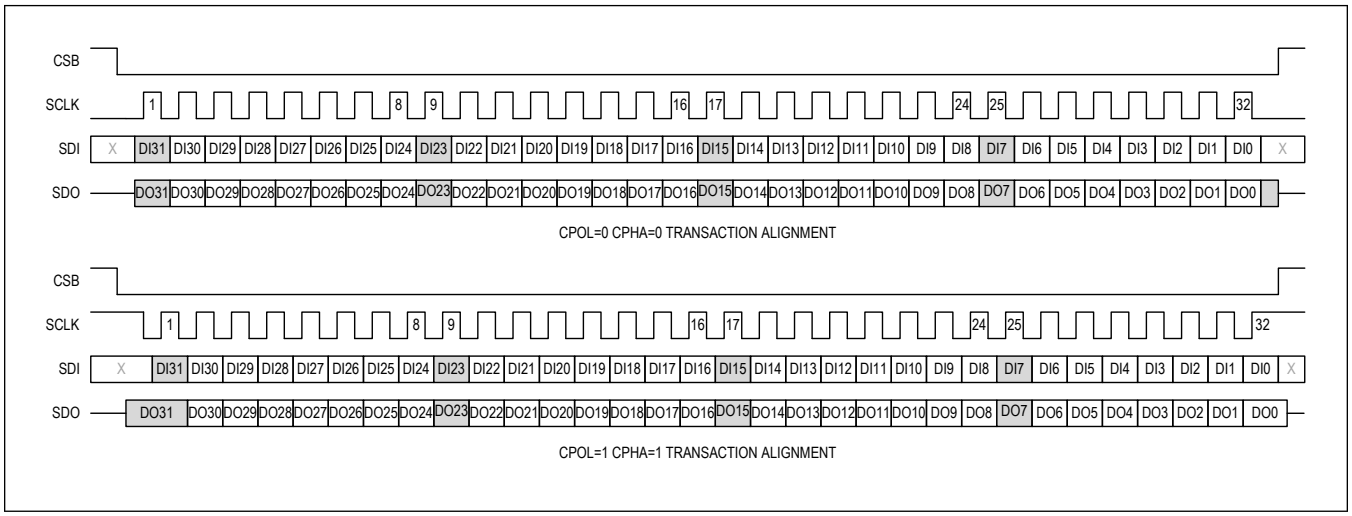


Figure 70. SPI Supported Transaction Alignments

Safety Pullup/Pulldown Resistors

In order to guard against broken SPI interface connections, the MAX17852 includes internal safety terminations on all SPI interface input ports. SCLK and SDI have internal pulldowns to GND. CSB has an internal pullup to V_{DDL3}. All safety resistors are 100kΩ (nom).

The internal safety resistors can be individually enabled or disabled using DEVCFG1 register bits (SFTYSCLK, SFTYSDI, SFTYCSB) with a high state (default) indicating the safety termination is enabled/engaged and a low state indicating it is disengaged. This allows the user to eliminate loading currents when the safety resistors are not needed. Note that pullup resistors will still have a resistor and diode connection to V_{DDL3} even if disengaged (limiting CSB voltage to V_{DDL3} + 0.3V to avoid conduction).

SPI Transactions

SPI Write Mode Transcations

A properly constructed write mode transaction is made up of a 32-bit data frame. Each SDI data frame from the master contains a R/WB = 0 bit, an 8-bit command/address, a 3-bit CRC covering the command/address, 2 bytes of input data, a confirmation of the R/WB = 0 bit, and a 3-bit CRC covering the input data.

During a write-mode transaction, the MAX17852 will output data on the SDO line confirming device status, as well as the command/address and input data received. Each SDO data frame from the slave will contain 5 bits of status information protected by a 3-bit CRC, followed by a 24-bit direct read back of the command/address and input data received during the transaction. Note while the 24-bit read back is not CRC protected, the transaction can be verified with 100% confidence since the master will know exactly what data was set to the device during the transaction.

The MAX17852 will only accept and execute qualified SPI transactions, based on the 32 bits of SDI data received, and several interface integrity checks. Details of write mode transactions are explained below and summarized in Figure 71.

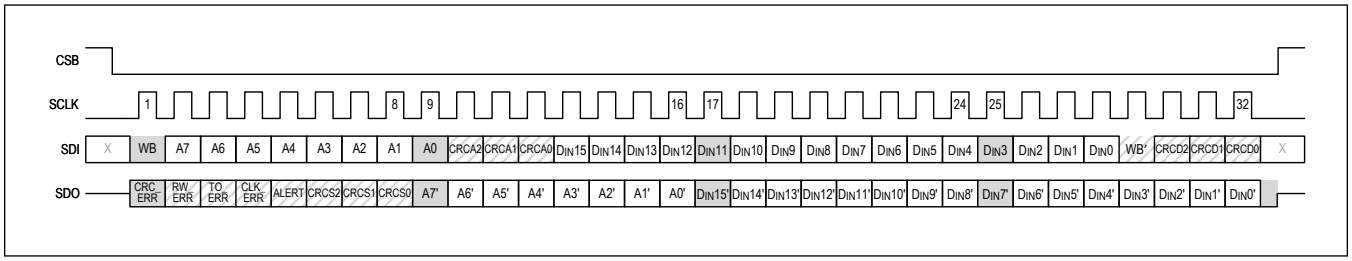


Figure 71. SPI Write-Mode Transaction Format

SPI Write Mode Input Data Format

During write mode transactions, the MAX17852 will accept qualified instructions via the SDI input as described below. If more than 32 SCLK cycles are provided in the transaction, the device will ignore the excess data provided during the remaining clock cycles, the transaction will be ignored, and a SPI Clock Error will be issued.

A SPI Error due to frame length will set ALRTINTRFC and ALRTSPI bits in the STATUS1 and STATUS2 registers, respectively, as well as the CLK_ERR diagnostic bit (DO[28]) present in every SPI frame.

Write Bit - R/WB = 0 (DI[31])

Write mode transactions are identified by R/WB = 0 in MSB position of the 32 bit data frame.

Address - A[7:0] (DI[30:23])

Write mode transactions allow new information to be written to internal configuration/command registers within the device. The register address to be written is indicated by A[7:0] within the data frame.

Address Cyclic Redundancy Check - CRCA[2:0] (DI[22:20])

Write mode command/address data transactions are protected by a 3-bit CRC with polynomial 0x5 (x^3+x+1). A total of 9 bits are protected, yielding a Hamming Distance of 2 (HD=2). The CRCA check is calculated over the following bits: R/WB + A[7:0] (i.e. positions DI[31:23]), confirming the integrity of the incoming command. The master must embed the correct CRCA value within each data frame in positions DI[22:20] for the transaction to qualify for execution. The receiving slaves will only accept/execute the transaction if the CRCA check is passed, otherwise the transaction will be ignored and a SPI CRC Error will be issued.

SPI errors caused by CRCA failures will set the ALRTPEC bit in the STATUS1 register, as well as the CRC_ERR diagnostic bit (DO[31]) present in every SPI frame.

Input Data – DIN[15:0] (DI[19:4])

These two bytes of input data in the 32-bit data frame represent data that will be written to the requested register or describe internal operations to be executed.

Repeated-Write Bit — R/WB‘ = 0 (DI3)

Write mode transactions are confirmed by a repeated R/WB = 0 in position DI[3] of the bit data frame. If the data in positions DI[31] and DI[3] do not match, the transaction will be ignored and a SPI RW Error will be issued.

SPI errors caused by R/WB and R/WB' mismatches will set the ALERTINTRFC and ALRTSPI bits in the STATUS1 and STATUS2 registers, respectively, as well as the RW_ERR diagnostic bit (DO[30]) present in every SPI frame.

Input Data Cyclic-Redundancy Check — CRCD[2:0] (DI[2:0])

Write mode input data transactions are protected by a 3-bit CRC with polynomial 0x5 (x^3+x+1). A total of 16 bits are protected, yielding a Hamming Distance of 2 (HD=2). The CRCD check is calculated over the following bits: D_{IN}[15:0] (i.e. positions DI[19:4]). The master must embed the correct CRCD value within each data frame in positions DI[2:0]

for the transaction to qualify for execution. The slave will only accept/execute the transaction if the CRCD is passed, otherwise the transaction will be ignored and a SPI CRC Error will be issued.

SPI errors caused by CRCD failures will set the ALRTPEC bit in the STATUS1 register, as well as the CRC_ERR diagnostic bit (DO[31]) present in every SPI frame.

SPI Write-Mode Output Data Format

During write mode transactions, the MAX17852 outputs data via the SDO line confirming both device status and the received instructions as described below. If more than 32 SCLK cycles are provided in the transaction, the device will output zeros for the remaining cycles, the transaction will be ignored, and a SPI Clock error will be issued.

Status Information – STAT[4:0] (DO[31:27])

During write-mode transactions, the MAX17852 will output status data via the SDO line confirming current device status. Since the STAT[4:0] information is identical for both read- and write-mode transactions, the definition of these bits is described in a common section below.

Status Cyclic Redundancy Check – CRCS[2:0] (DO[26:24])

During write mode transactions, the MAX17852 will output Status CRC data protecting the Status Information provided via SDO. Since the CRCS[2:0] information is identical for both read and write mode transactions, the definition of these bits is described in a common section below.

Address Confirmation – A‘[7:0] (DO[23:16])

During write mode transactions, the MAX17852 will relay the incoming Address (A[7:0]) data received via SDI in positions DO[23:16] via SDO. This behavior allows the master a complete confirmation that what was sent via the SPI interface was accurately received by the device; given this, the write mode confirmation data is not covered by a CRC. If any error is detected, the master should react accordingly, knowing that the flawed transaction will have been rejected if a SPI Error condition was detected and/or the CRCA check on the incoming transaction did not pass.

Input Data Confirmation — DIN‘[7:0] (DO[15:0])

During write mode transactions, the MAX17852 will relay the incoming Input Data (D_{IN}[15:0]) received via SDI in positions DO[15:0] via SDO. This behavior allows the master a complete confirmation that what was sent via the SPI interface was accurately received by the device; given this, the write mode confirmation data is not covered by a CRC. If any error is detected, the master should react accordingly, knowing that the flawed transaction will have been rejected if a SPI Error condition was detected and/or CRCD check on the incoming transaction did not pass.

SPI Write-Mode Qualification Checks

In order to qualify for write-mode execution, the following conditions must be met:

- The SPI transaction must be exactly 32 bits in length (with no CLK_ERR recorded)
- The CRCA Address CRC check must pass (with no CRC_ERR recorded)
- The CRCD Input Data CRC check must pass (with no CRC_ERR recorded)
- R/WB must match R/WB’ (i.e. DI[31] = DI[3], no RW_ERR recorded)
- The SPI transaction must be completed within the time out interval (t_{TO}, no TO_ERR recorded)

If the SPI transaction is qualified, the instruction will be executed, and the requested internal register contents will be updated or the requested action will be performed.

If the SPI write transaction is not qualified, the instruction will not be executed, and the appropriate SPI Error diagnostic bits will be set. The SPI Error diagnostic bits will be returned in response to later read and write-mode transactions, notifying the µC that the SPI interface may be compromised.

SPI Read Mode Transactions

A properly constructed read mode transaction will be made up of a 32-bit data frame. Each SDI data frame from the master will contain a R/WB = 1 bit, an 8-bit requested address, a 3-bit CRC covering the address, two bytes of input data

= 0000\h, a confirmation of the R/WB = 1 bit, and a 3-bit CRC covering the input data.

During a read mode transaction, the MAX17852 will output data on the SDO line confirming device status, and providing the data requested with full CRC protection. Each SDO data frame from the slave device will contain 5 bits of status information protected by a 3-bit CRC, four ones (indicating a read operation is pending), followed by 16 bits of output data, and finally, a read mode confirmation bit and a 3-bit CRC protecting the output data.

The MAX17852 will only accept and execute qualified SPI transactions, based on the 32 bits of SDI data received, and several interface integrity checks. Details of read mode transactions are explained below and summarized in Figure 72.

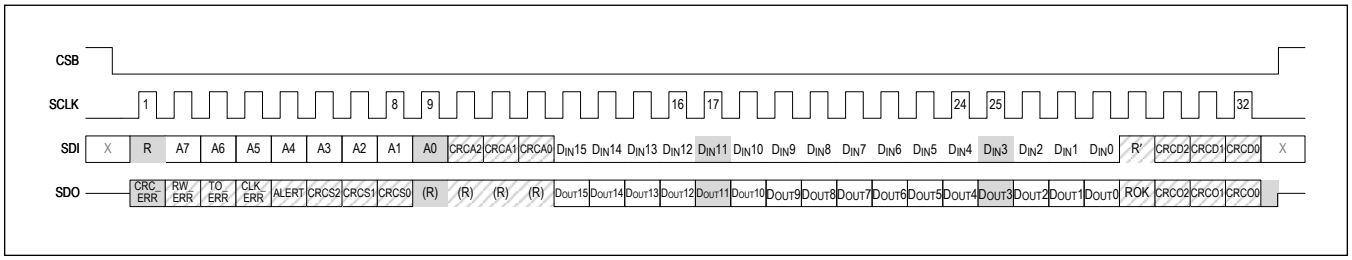


Figure 72. SPI Read Mode Transaction Format

SPI Read-Mode Input Data Format

During read-mode transactions, the MAX17852 will accept qualified instructions via the SDI input as described below. If more than 32 SCLK cycles are provided in the transaction, the device will ignore the excess data provided during the remaining clock cycles, the transaction will be ignored, and a SPI Clock Error will be issued.

A SPI Error due to frame length will set ALRTINTRFC and ALRTSPI bits in the STATUS1 and STATUS2 registers, respectively, as well as the CLK_ERR diagnostic bit (DO[28]) present in every SPI frame.

Read Bit - R/WB = 1 (DI[31]):

Read mode transactions are identified by R/WB = 1 in the MSB position of the 32-bit data frame.

Address - A[7:0] (DI[30:23])

Read mode transactions fetch the information from the register requested by the Address byte (A[7:0]). If the CRCA check fails, indicating a problem with the transaction or interface, the MAX17852 will still read back the data requested by A[7:0]. This may not be what the master intended, and the master will be notified of this via the read mode confirmation bit (ROK, see description below). Note that reading from a reserved address will result in a read back value of D_{OUT}[15:0] = 0000\h.

Address Cyclic Redundancy Check - CRCA[2:0] (DI[22:20])

Read mode command/address data transactions are protected by a 3-bit CRC with polynomial 0x5 (x^3+x+1). A total of 9 bits are protected, yielding a Hamming Distance of 2 (HD=2). The CRCA check is calculated over the following bits: R/WB + A[7:0] (i.e. positions DI[31:23]), confirming the integrity of the incoming command. The master must embed the correct CRCA value within each data frame in positions DI[22:20] for the transaction to qualify for execution. The receiving slave device will only accept/execute the transaction if the CRCA is passed, otherwise the transaction will be ignored and a SPI CRC Error will be issued.

SPI errors caused by CRCA failures will set the ALRTPEC bit in the STATUS1 register, as well as the CRC_ERR diagnostic bit (DO[31]) present in every SPI frame.

Input Data – DIN[15:0] (DI[19:4])

These 2 bytes of input data in the 32-bit data frame must be set to zero (0000h), otherwise the transaction will be ignored and a SPI Error will be issued.

SPI Errors generated by read transactions with non-zero input data will set the ALERTINTRFC and ALRTSPI bits in the

STATUS1 and STATUS2 registers, respectively, as well as the RW_ERR diagnostic bit (DO[30]) present in every SPI frame.

Repeated Read Bit - R/WB‘ = 1 (DI[3])

Read mode transactions are confirmed by a repeated R/WB = 1 in position DI[3] of the bit data frame. If the data in positions DI[31] and DI[3] do not match, the transaction is ignored and an SPI RW Error will be issued.

SPI errors caused by R/WB and R/WB' mismatches will set the ALERTINTRFC and ALRTSPI bits in the STATUS1 and STATUS2 registers, respectively, as well as the RW_ERR diagnostic bit (DO[30]) present in every SPI frame.

Input Data Cyclic Redundancy Check – CRCD[2:0] (DI[2:0])

Read-mode input-data transactions are protected by a 3-bit CRC with polynomial 0x5 (x3 + x + 1). A total of 16 bits are protected, yielding a Hamming distance of 2 (HD = 2). The CRCD check is calculated over the following bits: D_{IN}[15:0] (i.e., positions DI[19:4]). The master must embed the correct CRCD value within each data frame in positions DI[2:0] for the transaction to qualify for execution. The slave will only accept/execute the transaction if the CRCD is passed; otherwise, the transaction is ignored and an SPI CRC error issued.

SPI errors caused by CRCD failures will set the ALRTPEC bit in the STATUS1 register, as well as the CRC_ERR diagnostic bit (DO[31]) present in every SPI frame.

SPI Read-Mode Output Data Format

During read mode transactions, the MAX17852 will output data via the SDO line confirming device status and the requested output data as described below. If more than 32 SCLK cycles are provided in the transaction, the device will output zeros for the remaining cycles, the transaction will be ignored, and a SPI Clock Error will be issued.

Status Information – STAT[4:0] (DO[31:27])

During read mode transactions, the MAX17852 will output status data via the SDO line confirming current device status. Since the STAT[4:0] information is identical for both read and write mode transactions, the definition of these bits is described in a common section below.

Status Cyclic Redundancy Check – CRCS[2:0] (DO[26:24])

During read mode transactions, the MAX17852 will output Status CRC data protecting the Status Information provided via SDO. Since the CRCS[2:0] information is identical for both read and write mode transactions, the definition of these bits is described in a common section below.

Read Confirmation Bits – F\h (DO[23:20])

During read mode transactions, the MAX17852 will relay four ones in the DO[23:20] position, indicating the R/WB bit received was a one and a read mode transaction has been requested. Since all addresses above 0x98 are reserved, seeing all ones in this position during a *write mode command* will indicate an interface or protocol fault. Likewise seeing anything but all ones in this position during a *read mode command* will indicate the R/WB was not received or the interface is compromised. If either error is detected, the master should react accordingly, knowing that the flawed transaction will have been rejected if SPI Error and/or CRC checks on the incoming transaction did not pass.

Output Data – DOUT[15:0] (DO[19:4])

During read mode transactions, the MAX17852 will relay the requested Output Data (D_{OUT}[15:0]) in positions DO[19:4] via SDO.

Read OK Bit - ROK (DO[3])

During read mode transactions, the MAX17852 will relay a one in the DO[3] position, indicating a read mode transaction is in progress and that the CRCA check passed. This, combined with the Read Confirmation Bits in positions DO[23:20] will allow the master to confirm the data received matches the address requested.

Output Data Cyclic Redundancy Check – CRCO[2:0] (DO[2:0])

Read-mode output data transmissions are protected by a 3-bit CRC with polynomial 0x5 ($x^3 + x + 1$). A total of 16 bits are protected, yielding a Hamming distance of 2 (HD = 2). The CRC check is calculated over the following bits: DOUT[15:0] (i.e., positions DO[19:4]). The MAX17852 will embed the correct CRC value within each data frame in positions DO[2:0] for the transaction to be qualified by the master. The master should only accept the output data as valid if the CRCO check passed; otherwise, the data should be considered compromised.

SPI Read-Mode Qualification Checks

In order to qualify for read-mode execution, the following conditions must be met:

- The SPI transaction must be exactly 32 bits in length (with no CLK_ERR recorded)
- The CRCA Address CRC check must pass (with no CRC_ERR recorded)
- The CRCD Input Data CRC check must pass (with no CRC_ERR recorded)
- R/WB must match R/WB' (i.e. DI[31] = DI[3], with no RW_ERR recorded)
- D_{IN}[15:0] must match the required value (0000\h, with no RW_ERR recorded)
- The SPI transaction must be completed within the time out interval (t_{TO}, no TO_ERR recorded)

Since the full SPI transaction cannot be fully qualified until it is completed, the MAX17852 will respond to all read mode transactions as received, providing the requested output data within the frame, based on the received value of A[7:0]. However, if the command in its entirety is found to fail any qualification check, the command will be rejected, meaning any clear-on-read behaviors expected will not be executed internally.

In addition, if the SPI write transaction is not qualified, the appropriate SPI Error diagnostic bits will be set. The SPI Error diagnostic bits will be returned in response to later read and write mode transactions, notifying the µC that the SPI interface may be compromised.

SPI General Transaction Information

The following sections describe behaviors common to both read and write mode transactions.

Status and Status CRC Output Data

The MAX17852 provides Status (STAT[4:0]) and Status CRC (CRCS[2:0]) data via SDO during the MSByte of each SPI transaction. The content is identical for both read and write mode transactions, and is defined below.

Status Information – STAT[4:0] (DO[31:27])

The MAX17852 will provide the following SPI Error diagnostic bits and alerts during both read and write mode transactions.

- **SPI CRC_ERR (STAT[4])** indicates a previous transaction was rejected due a CRC failure for checks CRCA or CRCD.
- **SPI RW_ERR (STAT[3])** indicates a previous transaction was rejected due one or more of the following errors:
  - A repeated R/WB mismatch, R/WB ≠ R/WB' (i.e. DI[31] ≠ DI[3], protocol error)
  - D_{IN}[15:0] ≠ 0000\h for any read mode transaction (protocol error)
- **SPI TO_ERR (STAT[2])** indicates a previous transaction was rejected due to a time out violation.
- **SPI CLK_ERR (STAT[1])** indicates a previous transaction was rejected due to one or more of the following conditions:
  - The number of SCLK cycles not being exactly 32 (ALRTSCLKERR)
  - The 16MHz HF OSC is halted or drifting severely (ALRTOSC3)
  - The expected transfer to the internal memory bus has failed (ALRTINTBUS)
- **ALERT (STAT[0])** indicates one or more alert conditions exist in the STATUS or FMEA registers

If multiple SPI Protocol Errors occur during a single transaction, only the first error will be reported in the following order of precedence: CLK_ERR (ALRTSCLKERR), CRC_ERR, RW_ERR. SPI Time Out Errors, TO_ERR, and Internal Clock Errors, CLK_ERR (ALRTOSC3 and ALRTINTBUS) may be reported with other errors occurring in the same transaction. This is done to aide identification of root cause. For example, a malformed transaction 33 SCLK cycles in length would fail the clock check, but may also fail CRC and address checks since the data is also likely misaligned as a result. In such

a case, only the CLK_ERR SPI diagnostic bit would be set, due to precedence.

All SPI diagnostic bits are "Write 0 to Clear", meaning once asserted, they will continue to read back as high until the content is cleared by writing 1'b0 to the particular status register bit: ALRTSPI (will clear CRC_ERR, RW_ERR, and TO_ERR), component bits in STATUS2 will clear individual components of CLK_ERR. The MAX17852 will thus keep a cumulative list of all SPI failure types observed during failed transactions until the read back is performed. Note that the SPI CRC_ERR condition is reported using the dedicated STATUS1:ALRTPEC bit (read only), but is cleared using this STATUS2:ALRTSPI (i.e. the CRC_ERR condition is not reported in ALRTSPI). To clear ALRTPEC, it will be necessary to write ALRTSPI to zero even if it is already zero (if no other SPI Errors are reported).

All device STATUS alert bits will remain asserted (and thus the ALERT interface will remain asserted), until the content is cleared by the proper operations. See STATUS register definitions for specific details.

Note that transactions processed after any SPI diagnostic or device alert bit is set and remains high will be qualified and executed/accepted as defined under normal operation—a previous/uncleared error condition will not prevent further transactions from being executed.

SPI ALERT Bit Masking Operations

Assertion of the SPI ALERT status bit (STAT[0], DO[27]) is based on the contents of the STATUS1 register. Individual alert conditions can be masked out of the SPI ALERT bit using settings in ALRTIRQEN; however, the underlying alert information will always be available for read back in the STATUS1 register.

SPI ALERT =

ALRTRST or (ALRTMSMTCH & MSMTCHALRTEN) or

(ALRTCELLOVST & CELLOVSTALRTEN) or (ALRTCELLUVST & CELLUVSTALRTEN) or

(ALRTBLKOVST & BLKOVALRTEN) or (ALRTBLKUVST & BLKUVALRTEN) or

(ALRTAUXOVST & AUXOVSTALRTEN) or (ALRTAUXUVST & AUXUVSTALRTEN) or

(ALRTCSAST & CSASTALRTEN) or

(ALERTPEC & PECALRTEN) or (ALRTINTRFC & INTRFCALRTEN) or

(ALRTCAL & CALALRTEN) or (ALRTCBAL & CBALALRTEN) or

(ALRTFMEA1 & FMEA1ALRTEN) or (ALRTFMEA2 & FMEA2ALRTEN)

Note: STATUS1:ALRTRST indicates a POR condition, and thus cannot be masked. STATUS1:ALRTSCAN is a procedural notification bit and is intentionally not included in the SPI ALERT bit; it is available for inclusion in the ALERT Interface, to support interrupt-driven applications.

Status Cyclic Redundancy Check – CRCS[2:0] (DO[26:24])

Status output data content is protected by a 3-bit CRC with polynomial 0x5 ($x^3 + x + 1$). A total of 5 bits are protected, yielding a Hamming distance of 2 (HD=2, meaning the CRC will reliably catch transactions with 2-bit errors or less). The CRCS check is calculated over the following bits: STAT[4:0] (i.e., positions DO[31:27]). The MAX17852 embeds the correct CRCS value within each data frame in positions DO[26:24] for the transaction to be qualified by the master. The master should only accept the status data as valid if the CRCS check is passed; otherwise, the data should be considered compromised.

SPI CRC Calculations

All SPI CRC calculations use the same polynomial and CRC calculation method. CRC operations on incoming SDI data streams (CRCA and CRCD) are performed by the MAX17852 and require the host to compute the required CRC Remainders for inclusion in the SDI input data stream. CRC operations on outgoing SDO data streams (CRCS and CRCO) are performed by the host, based on CRC Remainders supplied by the MAX17852. To support SPI CRC computations and checking, the host must implement a CRC-3 encoding and decoding algorithm based on the following polynomial (0x5):

$$P(x) = x^3 + x^1 + 1$$

This polynomial is capable of protecting the covered SPI content with a Hamming Distance of two, meaning any combination of two bits of error or less is guaranteed to be identified. If more than two bits of error are encountered, the SPI CRC operation will very likely identify the problem, though this cannot be mathematically guaranteed.

The list of CRCn operations and the effective bit transaction masking operations are shown in Table 62. A hardware implementation of the CRC calculation is shown in Figure 73. The CRC Engine shown would be implemented within both MAX17852 and the host. Be sure to note the ordering of the bits within the Remainder, as shown in the figure (i.e. BIT[2:0] = CRCn[2:0]). All SPI CRC calculations are performed by supplying the MSB first, in the order presented in the SPI transaction.

Table 62. SPI CRC Operation Summary

CRCn OPERATION	R/W TRANSACTION	COVERED DATA	DATA POSITION	TRANSACTION BIT MASK	CRCn REMINDER	CRCn POSITION
Address (CRCA)	Read and Write	R/WB + A[7:0]	DI[31:23]	0xFF80_0000	CRCA[2:0]	DI[22:20]
Input Data (CRCD)	Read and Write	D_{IN}[15:0]	DI[19:4]	0x000F_FFF0	CRCD[2:0]	DI[2:0]
Status (CRCS)	Read and Write	STAT[5:0]	DO[31:27]	0xF800_0000	CRCS[2:0]	DO[26:24]
Output Data (CRCO)	Read only	D_{OUT}[15:0]	DO[19:4]	0x000F_FFF0	CRCO[2:0]	DO[2:0]

For incoming SDI data streams, the MAX17852 will first clear the CRC engine and then provide the covered bits within the incoming data stream into the the CRC Engine, MSB-first. The host should perform the same operation in parallel. After the final bit of data is processed (in this case, the LSB of the incoming data stream is applied to the Engine), the Engine is stopped and the CRCn Remainder is known. The CRCn Remainder, as calculated by the host using its copy of the CRC Engine then follows within the SPI transaction (also MSB first), and is internally compared against the CRC Remainder as calculated by the MAX17852. If the CRCn Remainder received from the host matches the CRC Remainder calculated by the device for the incoming data stream, the CRC operation is successful, and the transaction is accepted and executed by the MAX17852. If there is a mismatch, the MAX17852 will reject the transaction and issue the SPI CRC_ERR status bit and STATUS1:ALRTPEC flag, notifying the host of the issue, so the transaction can be resent.

For outgoing SDO data streams, the MAX17852 first clears the CRC Engine and then provides the covered bits within the outgoing data stream into the the CRC Engine, MSB first. The host should perform the same operation in parallel. After the final bit of data is processed (in this case, the LSB of the outgoing data stream is applied to the Engine), the Engine is stopped and the CRCn Remainder is known. The CRCn Remainder, as calculated by the MAX17852 using its copy of the CRC Engine, then follows within the SPI transaction (also MSB first), for comparison against the CRC Remainder as calculated by the host. At this point, there are two equivalent ways the host can complete the CRCn operation to establish the validity of the received data:

- Direct Comparison Method: The host stops the CRC Engine once the data LSB is applied and compares the resulting CRCn Remainder to the Remainder supplied by the MAX17852 (again, MSB first). If the two Remainders match, the data is accepted as valid, otherwise, it should be rejected. This is the method employed by the MAX17852 internally, as described above.
- Zero Remainder Method: The host continues CRC Engine computations after the data LSB is applied by appending the received Remainder to the end of the data stream, MSB first (i.e. in the order received during the SPI transaction). Once the LSB of the Remainder arrives at the input of the CRC Engine, if the resulting CRC Remainder = 0h, the data is accepted as valid, otherwise, it should be rejected.

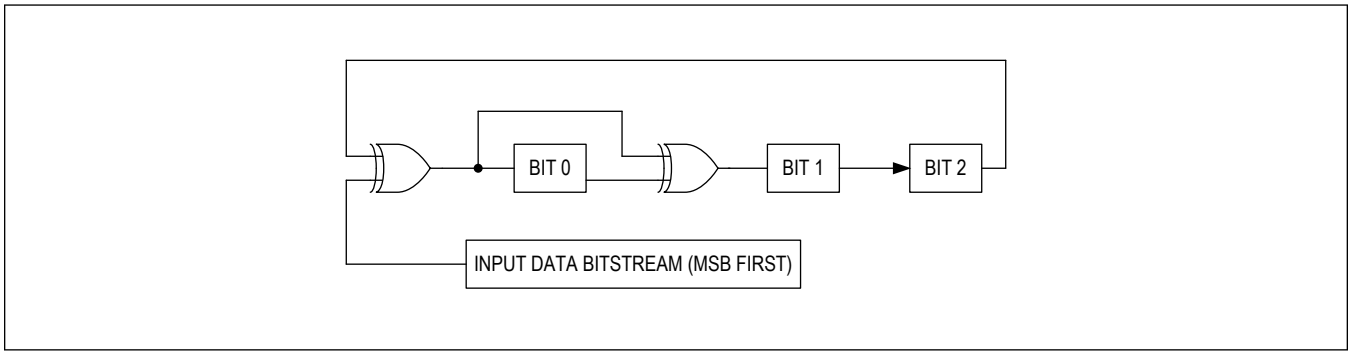


Figure 73. SPI CRC Calculation

SPI CRC Pseudocode Example

```
Function SPI_CRC_Calculation(Data, CRC)
{
        //Data - the incoming data [MSB:LSB] for which CRC needs to be calculated
        //CRC  - the calculated CRC that will be returned by the function
         //Calculate length of incoming data
         //Data length is 5 for Status (CRCS), 9 for Address (CRCA), and 16 for Data (CRCD and CRCO)
         DataLength = Length(Data)
         //CRC polynomial = x^3 + x + 1
         POLY = 4'hB //Polynomial = 4'b1011
         //Append Data with 3 zeros for 3 bit CRC
         DataCalc = {Data, 3'b000}
         //Append zeros to POLY such that it is of the same length as DataCalc
          PolyZeros = {{(DataLength + 3 - 4) 1'b0}}  //Data Calc length = DataLength + 3       //Since POLY = 4bits, subtract 4
         PolyCalc = {POLY, PolyZeros}                  //Append Zeros to POLY
         For Counter = (DataLength+3) to 4           //Counter decremented from MSB to LSB of Data
         (
         //Check MSB of DataCalc
         //If DataCalc[Counter] = 1'b1, bitwise XOR PolyCalc with DataCalc, and store result in DataCalc
         //If DataCalc[Counter] = 1'b0, skip the XOR operation
         //Circular Shift PolyCalc right by 1 bit every iteration.
         if(DataCalc[Counter] == 1'b1) Then
         DataCalc = DataCalc XOR PolyCalc
         End If
         PolyCalc = {PolyCalc[0], PolyCalc[Length[PolyCalc-1 : 1]} //Circular Shift Right PolyCalc by 1 bit
         )
         Return DataCalc[3:1] //3 LSBs of DataCalc give the 3 bit CRC
```

}

SPI Time-Out Behavior

All SPI transactions are timed by an internal 16MHz oscillator and are measured from the falling edge of CSB initiating a transaction to the rising edge of CSB terminating a transaction. If the time-out interval (t_{TO}) is exceeded by a transaction, the transaction will be timed out and will not be qualified or executed.

If a transaction is paused/interrupted for any reason (defined by a cessation of SCLK activity), and later resumed under the same CSB low interval, the SPI interface will continue to accept input data via SDI and relay the expected output data via SDO, as would normally be expected for the remainder of the transaction. However, even if all other qualification criteria are eventually met, the transaction will not be qualified or executed, and the TO_ERR diagnostic bit will be set.

In order to resolve a timed-out transaction and move forward with subsequent transactions, the timed-out transaction needs to be terminated by bringing CSB high. It is not necessary to complete the transaction by supplying 32 clocks; though if this is not done, the SPI CLK_ERR condition will be reported in addition to the TO_ERR condition. New transactions can then begin, initiated by pulling CSB low.

I^2C Interface

The MAX17852 features an I^2C-/SMBus™-compatible, 2-wire master serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). The interface is enabled/active if I2CEN is set high; in which case AUX/GPIO[0] is configured as an open-drain SDA I/O and AUX/GPIO[1] is configured as an-open drain SCL output. In this configuration, the device is capable of functioning as an I^2C-compatible master, and is able to read and write to any number of associated I^2C-compatible slave devices connected to the 2-wire bus at clock rates of 100kHz or 400kHz.

Note that the I^2C Master functionality is limited: the device must be the only master on the bus and is assumed to be the only device controlling the SCL line, as no provisions for arbitration are supported. In addition, the I^2C Master does not support slave devices which hold the clock low to force the master into a wait state (clock stretching). Clock stretching is optional and in fact, most slave devices do not include an SCL driver so they are unable to stretch the clock.

I^2C Timing Diagram and Data Format

The I²C timing diagram is shown in Figure 74. See *Electrical Characteristics* for complete timing specifications.

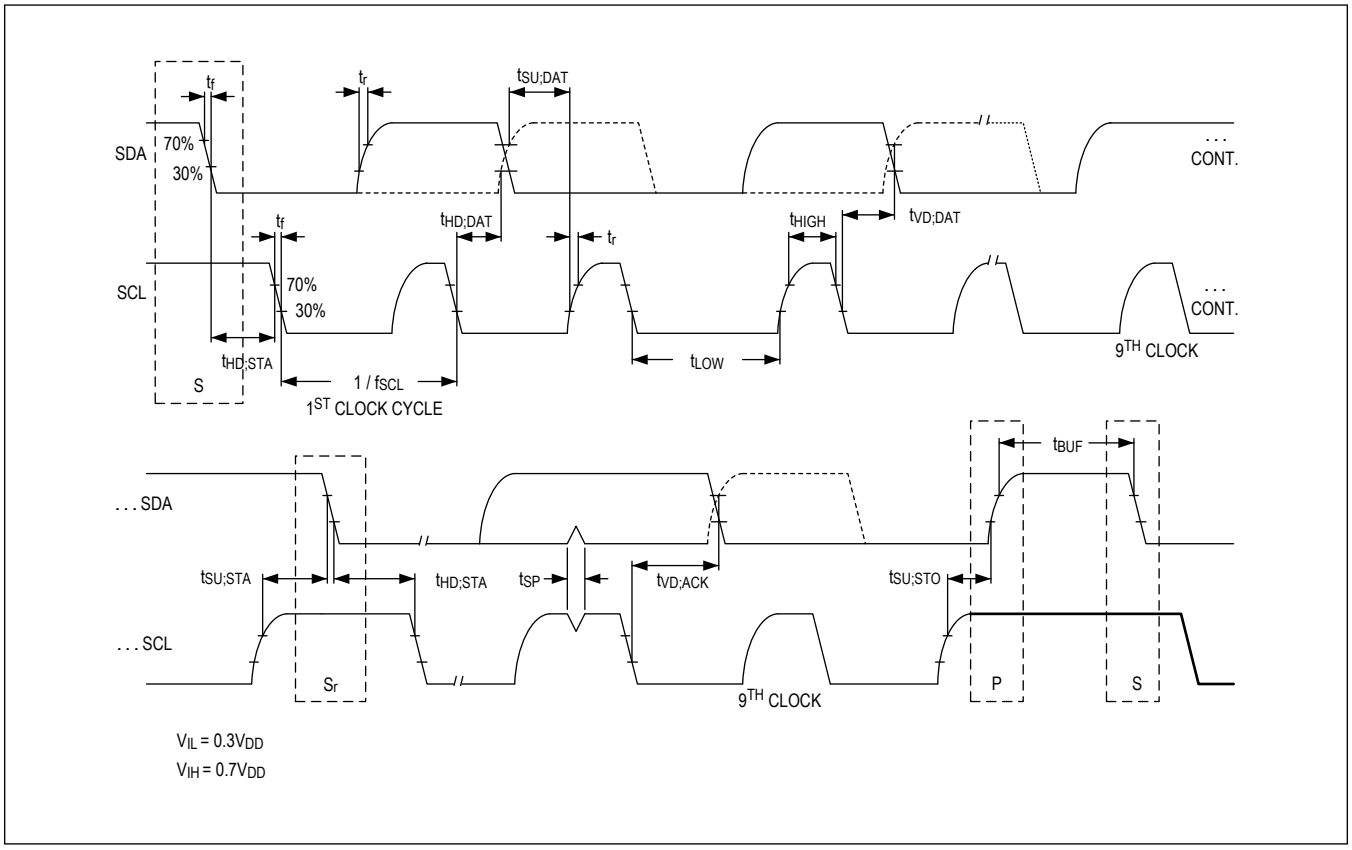


Figure 74. Standard I²C BUS Timing Diagram

I²C Start and Stop Conditions

SDA and SCL idle high when the bus is not in use. One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changing SDA while SCL is high will result control conditions being issued.

A high-to-low transition on the SDA line while SCL is high defines a START (S) condition. A low-to-high transition on the SDA line while SCL is high defines a STOP (P) condition. START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition. The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In this respect, the START (S) and repeated START (Sr) conditions are functionally identical.

I²C Acknowledge and Not Acknowledge Conditions

An acknowledge takes place after every byte sent/received. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. The master generates all clock pulses, including the acknowledge ninth clock pulse.

The Acknowledge (A or ACK) signal is defined as follows: the transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line low and it remains stable low during the high period of this clock pulse. Set-up and hold times must also be taken into account.

When SDA remains high during this ninth clock pulse, this is defined as the Not Acknowledge signal (~A or NACK). The master will recognize a transaction failure if a slave device fails to acknowledge its address or a sent data byte. Note for

all read mode transactions, the master will issue a NACK after the last byte of the transaction.

I2C Bus Construction

Pullup resistors, typically 4.7kΩ, are required on SDA and SCL. The I2C master includes slew control on the SCL and SDA output drivers, but custom slew profiles can be obtained by proper selection of pullup resistors and bus capacitance and/or the addition of in-line resistors placed in series with the SCL and SDA outputs (see Figure 75). Series resistors can also protect the digital inputs from high voltage spikes on the bus lines and minimize crosstalk and undershoot of the bus signals.

The I2C Master can accommodate bus voltages higher than V_{IO} up to a limit of 5.5V; bus voltages lower than V_{IO} (VIO is V_{DDL2} for this part) are not recommended and may result in significantly increased interface currents. Typically, the bus is terminated to the highest interface supply, if multiple supplies are required in the application.

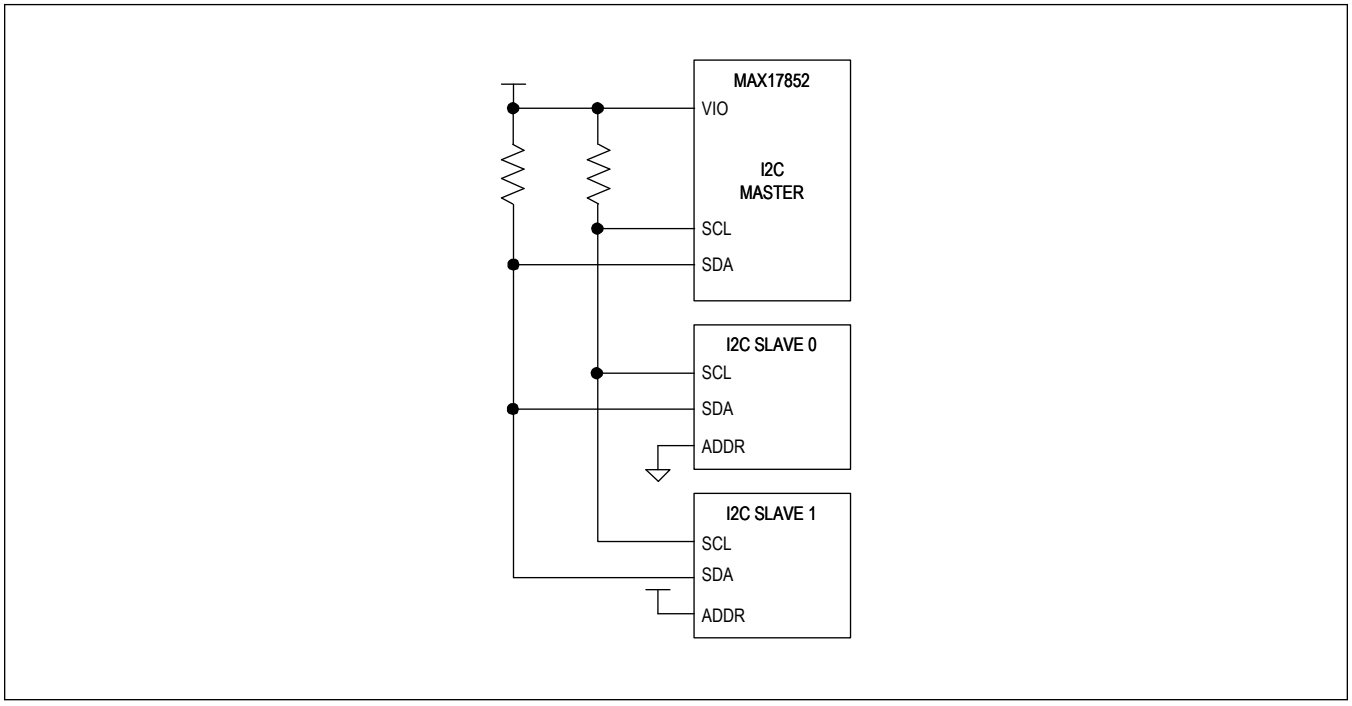


Figure 75. I²C Device Connection

I2C Master Configuration and Input Data

Prior to use, the I2C Master must be configured by writing data to the registers described below. See the Register Map for detailed descriptions.

I2CCFG Register

I2CCFG includes all settings which govern the configuration and formatting of I2C read and write transactions to be performed by the master. This register can also be read back to verify contents. When communicating with slave devices of a single type, it will generally only be necessary to write to the configuration register once.

I2CFSCL selects the I2C SCL Frequency (0b0 = 100kHz, 0b1 = 400kHz).

I2CWALT sets the write mode data length options available. I2CWALT mode should only be used when it is necessary to send Write Mode transactions consisting only of Slave Addresses and a Pointer (no Data). Transactions of this type are sometimes required to set up pointers for use in Normal Format Read Mode transactions. When I2CWALT mode is engaged, the 3 Byte Data length write option is replaced by a 0 Byte Data write option. Read length options are not

impacted.

I2CRFMT selects the format used for read mode transactions (0b0 = Normal, 0b1 = Combined). Write mode transactions are not impacted.

I2C10BIT selects the slave address format used for all transactions (0b0 = 7 bit, 0b1 = 10 bit).

I2CPNTRLNGTH selects the number of bytes sent as the command portion of write and combined format read mode transactions (0b0=1 Byte, 0b1 = 2 Bytes). If one byte pointer mode is used (default, standard), both pointer bytes are available for use in I2C Master transactions using I2CPNTRSEL (minimizing configuration time).

I2CALRTEN allows errors encountered during I2C transactions to be reported via ALRTI2C in the STATUS registers (0b0=disabled, 0b1=enabled). The alert will be cleared when I2CSTAT is read back and no new faults have been reported.

I2CANACONTEN enables analog bus contention monitoring and its associated alert component (0b0 = disabled, 0b1 = enabled).

I2CCONTEN enables digital bus contention monitoring and its associated alert component (0b0 = disabled, 0b1 = enabled).

I2CGLITCHEN enables bus glitch monitoring and its associated alert component (0b0 = disabled, 0b1 = enabled).

I2CNOISEEN enables bus noise monitoring and its associated alert component (0b0 = disabled, 0b1 = enabled).

I2CRDTREN enables redundant read mode checking and its associated alert component (0b0 = disabled, 0b1 = enabled).

I2CTOEN enables watchdog checking of I2C transactions using the 32kHz oscillator (0b0 = disabled, 0b1 = enabled).

I2CPNTR Register

This register contains I2CPBYTE1 and I2CPBYTE0 of pointer (command) data sent as the command portion of write and combined format read mode transactions. If I2CPNTRLNGTH = 0b0, either byte can be sent (selected by I2CPNTRSEL), so two I2C command transactions can be supported by writing to this register only once. If I2CPNTRLNGTH = 0b1, both bytes are sent. This register can also be read back to verify contents.

I2CWDATA Registers

The I2CWDATA1 and I2CWDATA2 registers contain 4 bytes of data that can be sent to slave devices during the data portion of write mode transactions. Selection of which bytes are sent and how many bytes are sent is determined by I2CDATALNGTH and I2CDATASEL, thus for transactions of one or two bytes of data, it is possible for several write mode transactions to be supported by writing to this register only once. This register can also be read back to verify contents.

I2C Transaction Requests and Results

Once the I2C Master is properly configured and supplied with any required input data, transactions can be sent. See the Register Map for detailed descriptions.

I2CSEND Register

The I2C master initiates clock and data transactions on the bus in response to an accepted/qualified write to the I2CSEND command register. Each accepted/qualified write to this register will initiate a transaction, unless a transaction is already in progress (in which case the new transaction request will be ignored and the I2CRJCT alert component will be set). Transaction progress and status can be monitored using the I2CSTATUS register. This register can also be read back to verify the specifics of the last accepted transaction.

I2CPNTRSEL selects the byte sent as the command portion of write and combined format read mode transactions (applicable only if I2CPNTRLNGTH = 0b0). If I2CPNTRLNGTH = 0b1 (two byte pointer mode), this bit is ignored and both bytes are sent.

I2CDATALNGTH selects the number of data bytes to be sent in a write mode transaction or received in a read mode transaction.

I2CDATASEL selects the data register locations to be sent in write mode transactions or filled during read mode

transactions. Selects the location of the data bytes(s) to be transferred during Write transactions and the target location for data byte(s) used for storage during Read transactions. The selection indicates the location of the MSByte of the data space used during the transaction, the number of bytes used is set by I2CDATALNGTH.

Some limitations do apply:

If I2CDATALNGTH = 0b11 (4 Bytes), this selection is ignored and Bytes[3:0] are used.

If I2CDATALNGTH = 0b10 (3 Bytes), this selection is ignored and Bytes[2:0] are used.

If I2CDATALNGTH = 0b01 (2 Bytes), the LSB is ignored; for 0x, Bytes[1:0] are used, and for 1x, Bytes[3:2] are used.

If I2CDATALNGTH = 0b00 (1 Byte), any of the four available bytes can be used.

If I2CDATALNGTH = 0b10 and I2CWALT = 0b1 (0 Byte Write), this selection is ignored and no bytes are used.

I2CDEVIDEXT and I2CDEVID are used to set the slave address sent during I2C transactions (I2CDEVIDEXT is only used if I2C10BIT = 0b1, otherwise it is ignored).

I2CRWB determines if the I2C transaction sent write (0) or read (1).

I2CRDATA Registers

The I2CRDATA1 and I2CRDATA2 registers contains 4 bytes (I2CRBYTE3, I2CRBYTE2, I2CRBYTE1, I2CRBYTE0) of memory that can be filled with data received from slave devices during the data portion of read mode transactions. Selection of which bytes are used in support of a read mode transaction is determined by I2CDATALNGTH and I2CDATASEL, thus for transactions of 1 or 2 bytes of data, it is possible for several read mode transactions to be supported by filling this register using multiple transactions, while reading this register only once when filled. This register is read only.

Note: during read commands, data is updated as each byte is received/acknowledged, reading back target registers during read transactions may yield corrupted results.

I2CSTAT Register

The I2CSTAT register provides information on active and completed I2C transactions.

I2CSTATUS reports the status of the last requested transaction and its resolution if completed. No Transaction (0b00) indicates no transaction has been requested since I2CSTAT was last read. Transaction in Progress (0b01) indicates the last requested transaction is in progress, this status will not be changed until the transaction terminates. Once a transaction is completed, the Transaction Complete (0b11, if successful) or Transaction Error (0b10, if unsuccessful) status will be reported. A transaction error if the following alert conditions are detected and enabled (note: I2CRJCT, I2CDEVNACK, and I2CDATANACK are always enabled). These status bits will be cleared/updated when I2CSTAT is read back or when a new transaction is begun.

The remaining bits relate alert conditions if a problem was encountered. They are updated as they occur, as opposed to waiting until the end of transaction.

I2CRJCT indicates one or more I2C transactions were rejected because a write to I2CSEND was attempted during an ongoing transaction (note the ongoing transaction will not be impacted).

I2CDEVNACK indicates the I2C transaction Device ID Byte(s) were not acknowledged by a slave. This may indicate the slave is malfunctioning or not present on the bus. For Combined Format Read transactions, both slave address acknowledge pulses are required to avoid an error. The current I2C transaction will continue until completion. That is, the master will not issue a STOP bit immediately.

I2CDATANACK indicates one or more I2C transaction Data Byte(s) written were not acknowledged by a slave. This may indicate the slave is malfunctioning, not present on the bus, is busy, or has rejected an unsupported transaction. The current I2C transaction will continue until completion. That is, the master will not issue a STOP bit immediately.

I2CANACONT and I2CCONT indicates a bus contention condition was observed. Contention is reported when the port result does not match the value driven by the I2C Master. This monitor observes the SCL port and the SDA port when driven by the I2C Master. See I2C Bus Contention Monitor for more details.

I2CGLITCH indicates a bus glitch condition was observed. A glitch is reported when a port monitor reports two or more

consecutive samples (125ns) that disagree with the evaluated value. This condition may also be reported if slow transition times, setup time, or hold time violations occur (outside I2C specifications). This monitor observes the SCL port and the SDA port outside specified transition intervals. See I2C Glitch Monitor for more details.

I2CNOISE indicates a noisy bus condition was observed. A noise condition is reported when a port monitor reports a large number of samples that disagree with the evaluated value. This condition may also be reported if slow transition times, setup time, or hold time violations occur (outside I2C specifications). This monitor observes the SCL port and the SDA port outside specified transition intervals. See I2C Noise Monitor for more details.

I2CRDTRERR indicates the results of an I2C Redundant Read Transaction Check failed (enabled if I2CRDTREN = 0b1).

I2CTIMEOUT indicates the I2C transaction did not complete in the expected period of time (enabled if I2CTOEN = 0b1).This register is read only.

I2C Master Register Access During Active I2C Transactions

Since the I2C Master register contents are in use during active I2C transactions, User interface access to the registers during ongoing I2C transactions is strictly controlled. Attempts to write or read content to/from these registers that may result in data corruption or synchronization issues will be rejected and will result in I2CSTAT:I2CRJCT and STATUS2:ALRTI2C being issued, notifying the user that the request has been ignored. Table 63 provides a summary of register accessibility by active I2C transaction and User transaction type. See the Register Map for complete details on all I2C Master registers.

Table 63. Summary of I2C Register Access During Active I2C Transactions

I2C REGISTER	TYPE	DURING ACTIVE I2C WRITE TRANSACTIONS		DURING ACTIVE I2C READ TRANSACTIONS		COMMENT
		USER READ	USER WRITE	USER READ	USER WRITE	
I2CPNTR	R/W	Allowed	Rejected	Allowed	Rejected	Pointer data is protected during all I2C Transactions
I2CWDATA1&2	R/W	Allowed	Rejected	Allowed	Rejected	Write data is protected during all I2C Transactions
I2CRDATA1&2	R	Allowed	N/A	Rejected	N/A	Read data is updated during I2C Read Transactions
I2CCFG	R/W	Allowed	Rejected	Allowed	Rejected	Configuration data is protected during all I2C Transactions
I2CSTAT	R/W	Allowed	Rejected	Allowed	Rejected	Status data is protected during all I2C Transactions
I2CSEND	R/W	Allowed	Rejected	Allowed	Rejected	Only a single I2C Transaction at a time is supported

I2C Write Transactions

The I2C master initiates clock operation and data transfer on the bus in response to an accepted/qualified write to the I2CSEND command register with I2CRWB = 0b0. The master controls SCL for the entirety of the transaction. The master will also control the SDA line during all byte transfers, except those cycles reserved for acknowledge bits. The master writes data to associated slave devices by transmitting the selected slave address byte(s), followed by the command byte(s), and then the requested number of data bytes (0 to 4 byte data fields are supported in write mode). The write data comes from I2CWBYTE3, I2CWBYTE2, I2CWBYTE1, and I2CWBYTE0.

Each write mode transaction is framed by a START (S) condition and a STOP (P) condition generated by the master. After each byte sent, the addressed slave is expected to Acknowledge (A) receipt of the byte by pulling the SDA line low. The master will recognize and report a transaction failure if a slave device fails to acknowledge its address or a sent data byte, but the transaction will run to completion. In the event of a failure (I2CSTATUS = 0b10), the user may instruct the master to retry the transaction by issuing another I2CSEND command with the same content.

The figures below show I2C Write Mode Transaction examples Figure 76 using 7-bit and Figure 77 using 10-bit

addressing, 1-byte pointer, and 2-byte data length (I2C10BIT = 0b0/1, I2CPNTRLENGTH = 0b0, I2CDATALNGTH = 0b01. Command/pointer widths of 1 or 2 bytes, and written data widths of 0 (command/pointer only) to 4 bytes can be achieved with alternate configuration settings. In general, it is assumed 0-byte writes would only be used to set pointer locations for following normal format read transactions. When using 10-bit addressing, note multiple slave devices may acknowledge Byte 1, but only the addressed slave device will acknowledge Byte 2.

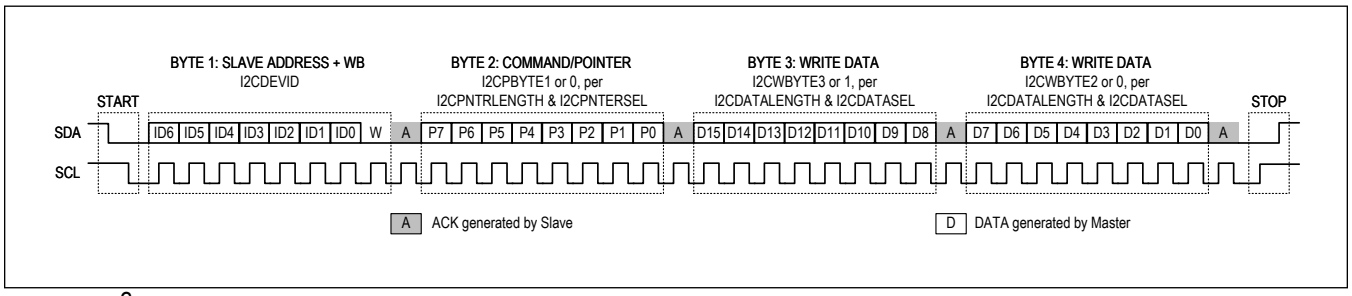


Figure 76. I²C Write Mode Transaction Example -- 7-Bit Address, I2C10BIT = 0

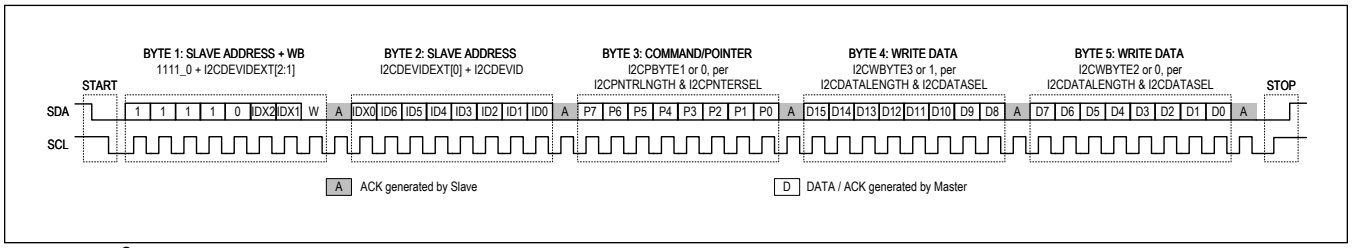


Figure 77. I²C Write Mode Transaction Example -- 10-Bit Address, I2C10BIT = 1

I²C Combined Format Read Transactions

In general, it is assumed most slave devices are capable of supporting combined format read transactions, as this provides the most efficient use of the I²C master in terms of configuration and commands. Combined format read transactions are enabled when I2CRFMT = 0b1 (default).

The I²C master initiates clock operation and data transfer on the bus in response to an accepted/qualified write to the I2CSEND command register with I2CRWB = 0b1. The master controls SCL for the entirety of the transaction.

The transaction begins with a START (S) condition. The master will control the SDA line during all byte transfers of the write portion of the command (bytes preceding the REPEATED START (Sr)), except those clock cycles reserved for slave acknowledge bits. During this portion of the command, the master will write the selected pointer byte(s) to the slave, typically indicating which register contents are to be read back during the read portion of the command.

The master will continue to control the SDA line during the initial byte of the read portion of the command (the byte immediately following the Sr). After the slave acknowledge bit for the initial address byte, the master will shift to receive mode and relinquish control of SDA to the slave for all incoming byte transfers. The master will acknowledge each byte received from the slave by pulling SDA low during the ACK cycle following each byte transfer. A not acknowledge (NACK) is sent when the master reads the final byte of data from the slave, (determined by I2CDATALNGTH) before terminating the transaction with a STOP (P).

The figures below show I²C Combined Format Read Mode Transaction examples Figure 78 using 7-bit and Figure 79 using 10-bit addressing, 1-byte pointer, and 2-byte data length (I2C10BIT = 0b0/1, I2CPNTRLENGTH = 0b0, I2CDATALNGTH = 0b01. Command/pointer widths of 1 or 2 bytes, and received data widths of 1 to 4 bytes can be achieved with alternate configuration settings. When using 10-bit addressing, note multiple slave devices may acknowledge Byte 1, but only the addressed slave device will acknowledge Byte 2, 3, and 4.

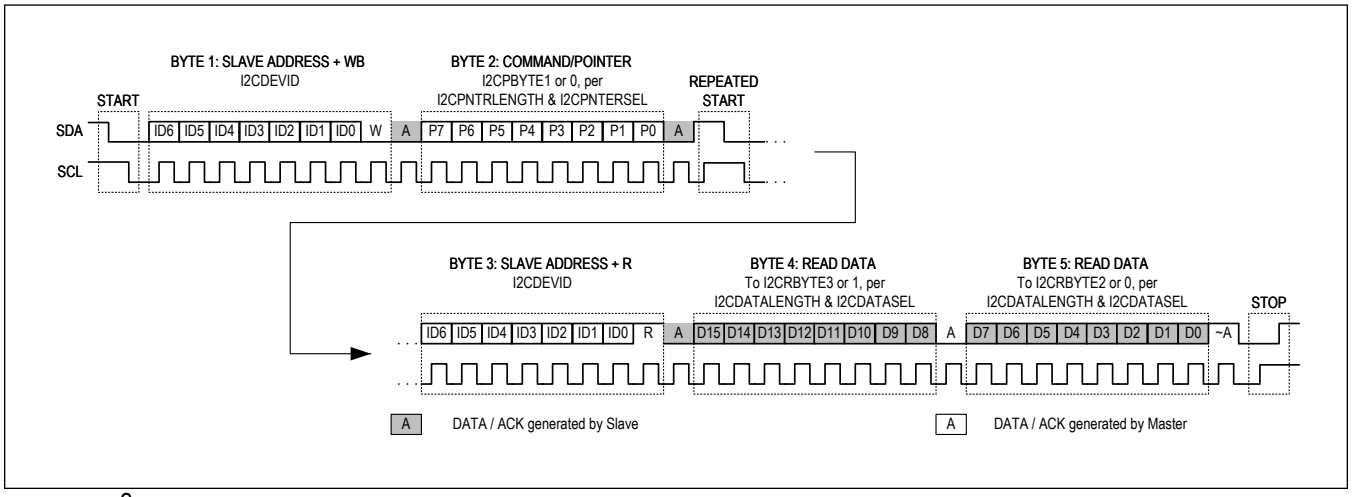


Figure 78. I²C Combined Format Read Mode Transaction Example -- 7-Bit Address, I2C10BIT = 0, I2CRFMT = 1

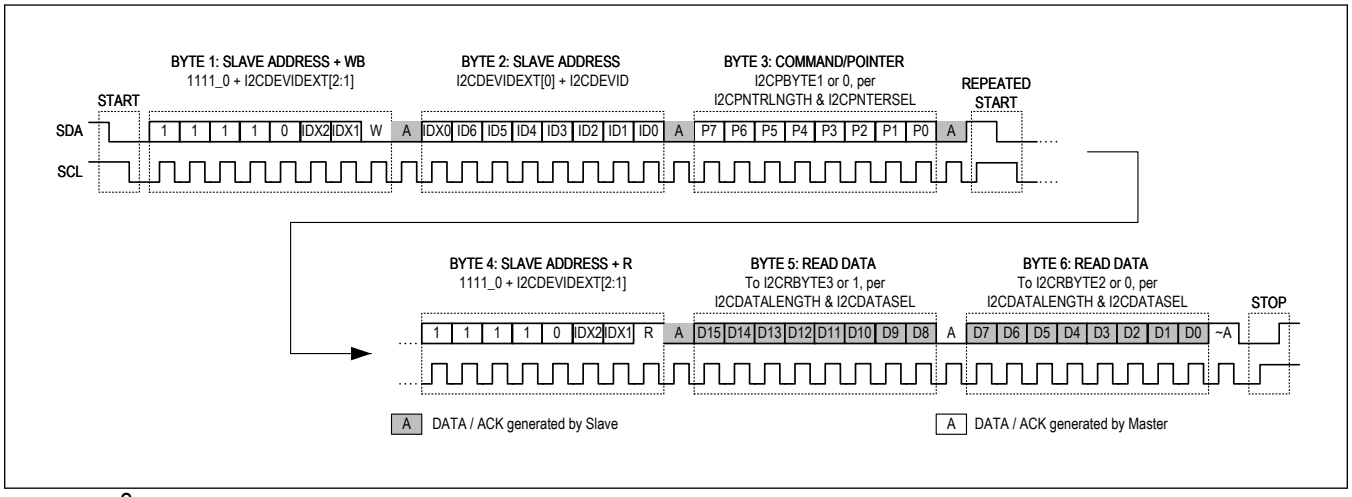


Figure 79. I²C Combined Format Read Mode Transaction Example -- 10-Bit Address, I2C10BIT = 1, I2CRFMT = 1

I²C Normal Format Read Transactions

In general, it is assumed most slave devices are capable of supporting combined format read transactions, as this provides the most efficient use of the I²C master in terms of configuration and commands. Combined format read transactions are enabled when I2CRFMT = 0b1 (default).

The I²C master initiates clock operation and data transfer on the bus in response to an accepted/qualified write to the I2CSEND command register with I2CRWB = 0b1. The master controls SCL for the entirety of the transaction.

The transaction begins with a START (S) condition. The master will control the SDA line during all byte transfers of the write portion of the command (bytes preceding the REPEATED START (Sr)), except those clock cycles reserved for slave acknowledge bits. During this portion of the command, the master will write the selected pointer byte(s) to the slave, typically indicating which register contents are to be read back during the read portion of the command.

The master will continue to control the SDA line during the initial byte of the read portion of the command (the byte immediately following the Sr). After the slave acknowledge bit for the initial address byte, the master will shift to receive

mode and relinquish control of SDA to the slave for all incoming byte transfers. The master will acknowledge each byte received from the slave by pulling SDA low during the ACK cycle following each byte transfer. A not acknowledge (NACK) is sent when the master reads the final byte of data from the slave, (determined by I2CDATALNGTH) before terminating the transaction with a STOP (P).

The figures below show I2C Combined Format Read Mode Transaction examples Figure 78 using 7-bit and Figure 79 using 10-bit addressing, 1-byte pointer, and 2-byte data length (I2C10BIT = 0b0/1, I2CPNTRLENGTH = 0b0, I2CDATALNGTH = 0b01. Command/pointer widths of 1 or 2 bytes, and received data widths of 1 to 4 bytes can be achieved with alternate configuration settings. When using 10-bit addressing, note multiple slave devices may acknowledge Byte 1, but only the addressed slave device will acknowledge Byte 2, 3, and 4.

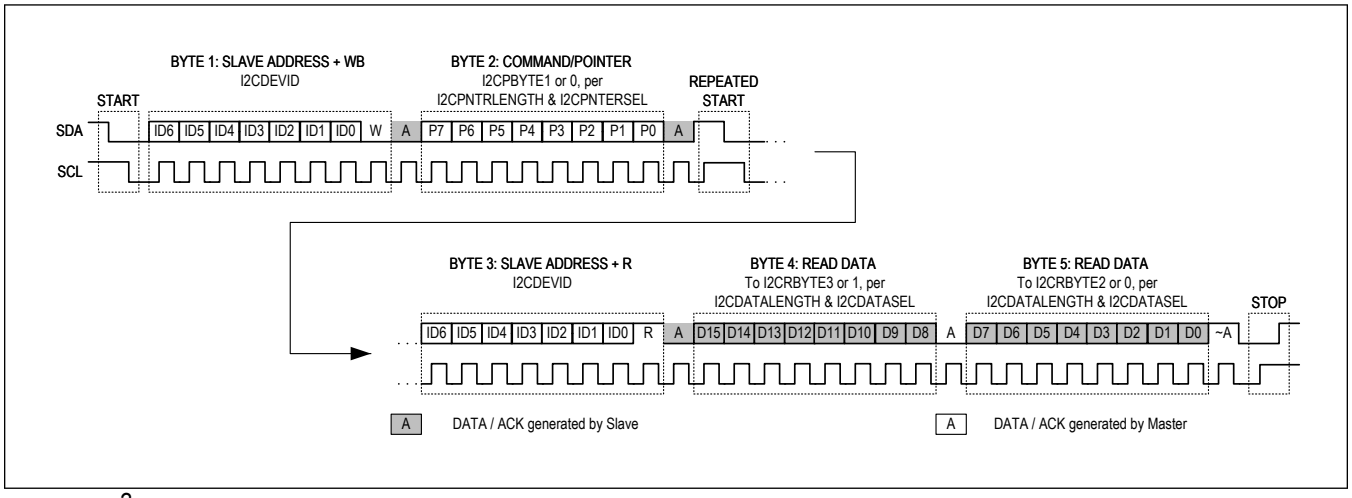


Figure 80. I2C Combined Format Read Mode Transaction Example -- 7-Bit Address, I2C10BIT = 0, I2CRFMT = 1

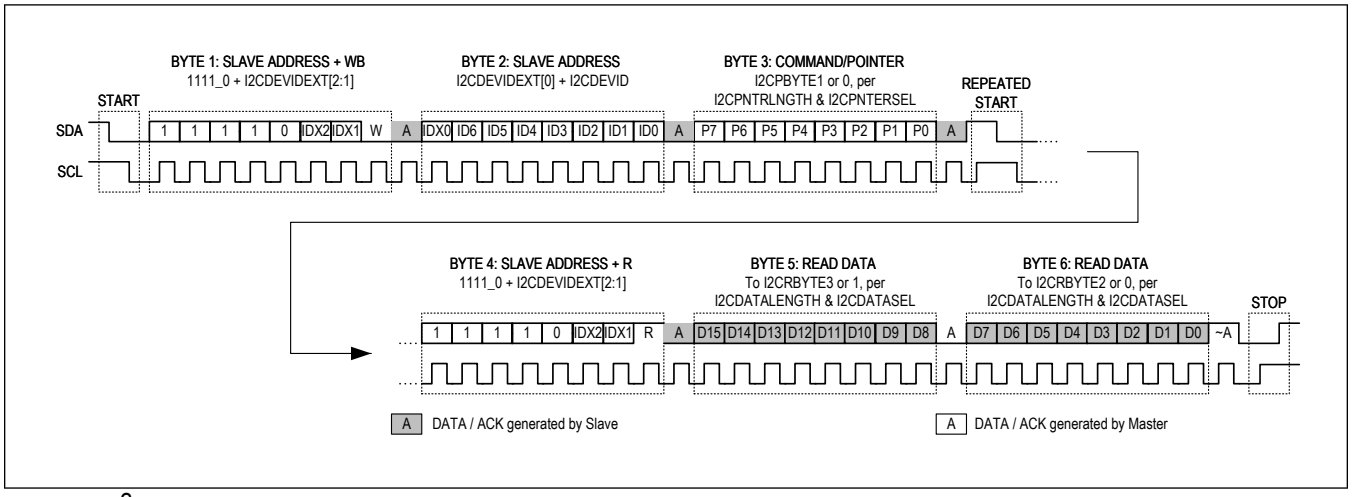


Figure 81. I2C Combined Format Read Mode Transaction Example -- 10-Bit Address, I2C10BIT = 1, I2CRFMT = 1

7-Bit Address Transactions

The I2C master initiates clock operation and data transfer on the bus in response to an accepted/qualified write to the I2CSEND command register with I2CRWB = 0b1. The master controls SCL for the entirety of the transaction.

The transaction begins with a START (S) condition. The master will control the SDA line during the initial byte transfers associated with address portion of the transaction, except the clock cycle reserved for the slave acknowledge bit.

After the slave acknowledge bit for the initial byte, the master will shift to receive mode and relinquish control of SDA to the slave for all incoming byte transfers. The master will acknowledge each byte received from the slave by pulling SDA low during the ACK cycle following each byte transfer. A not acknowledge (NACK) is sent when the master reads the final byte of data from the slave, (determined by I2CDATALNGTH) before terminating the transaction with a STOP (P).

The Figure 82 shows a Normal Format Read Mode Transaction example using 7-bit addressing, 1-byte pointer, and 2-byte data length (I2C10BIT = 0b0, I2CPNTRLENGTH = 0b0, I2CDATALNGTH=0b01. Received data widths of 1 to 4 bytes can be achieved with alternate configuration settings.

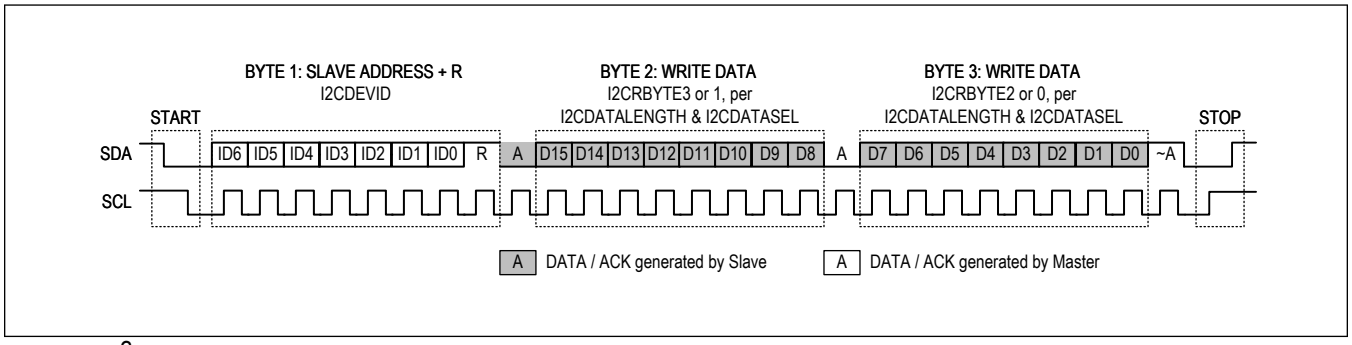


Figure 82. I2C Normal Format Read Mode Transaction Example -- 7-Bit Address, I2C10BIT = 0, I2CRFMT = 0

10-Bit Address Transactions

When using 10-Bit addressing with I2CRFMT = 0b0, the structure of the Normal Format Read Mode Transaction is quite similar to the Combined Format transaction, except no pointer is sent during the write portion of the command. The I2C master initiates clock operation and data transfer on the bus in response to an accepted/qualified write to the I2CSEND command register with I2CRWB = 0b1. The master controls SCL for the entirety of the transaction.

The transaction begins with a START (S) condition. The master will control the SDA line during all byte transfers of the write portion of the command (bytes preceding the REPEATED START (Sr)), except those clock cycles reserved for slave acknowledge bits.

The master will continue to control the SDA line during the initial byte of the read portion of the command (the byte immediately following the Sr). After the slave acknowledge bit for the initial address byte, the master will shift to receive mode and relinquish control of SDA to the slave for all incoming byte transfers. The master will acknowledge each byte received from the slave by pulling SDA low during the ACK cycle following each byte transfer. A not acknowledge (NACK) is sent when the master reads the final byte of data from the slave, (determined by I2CDATALNGTH) before terminating the transaction with a STOP (P).

The Figure 83 shows an I2C Combined Format Read Mode Transaction example using 10-bit addressing, 1-byte pointer, and 2-byte data length (I2C10BIT = 0b1, I2CPNTRLENGTH = 0b0, I2CDATALNGTH = 0b01. Received data widths of 1 to 4 bytes can be achieved with alternate configuration settings. When using 10-bit addressing, note multiple slave devices may acknowledge Byte 1, but only the addressed slave device will acknowledge Byte 2 and 3.

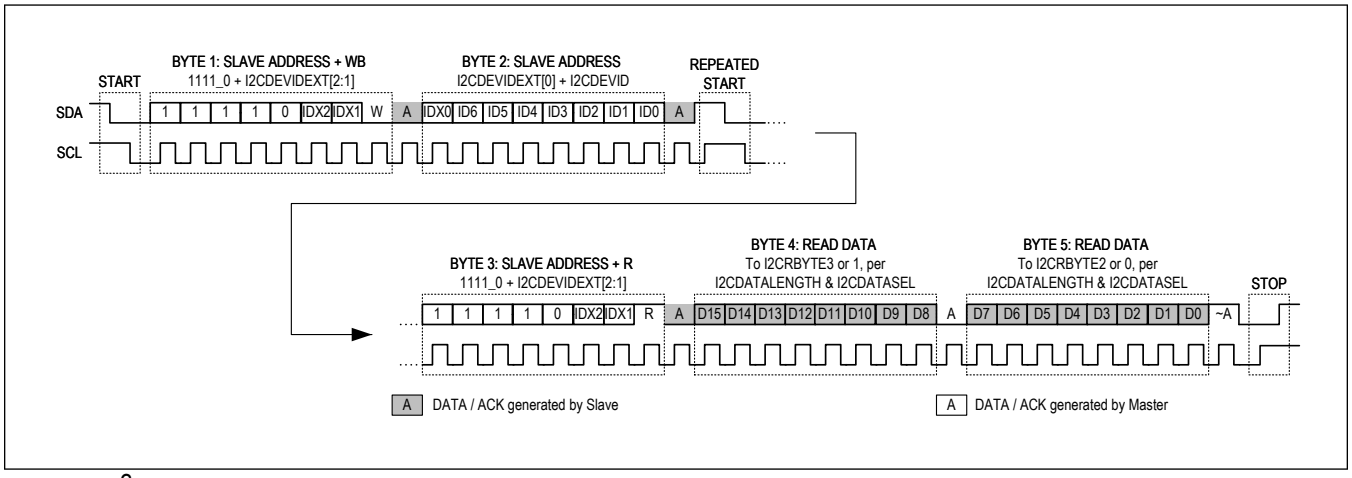


Figure 83. I²C Normal Format Read Mode Transaction Example -- 10-Bit Address, I2C10BIT = 1, I2CRFMT = 0

I²C Master Safety Features

The I²C Master supports a variety of safety features to provide feedback on the quality of the interface transactions and the operation of the bus.

I²C Bus Contention Monitor

I2CCONT is reported when the evaluated port result does not match the value driven by the I²C Master. This monitor observes the SCL port and the SDA port when driven by the I²C Master. The contention monitor is always enabled. When I2CCONTEN = 0b1, STATUS2 register bit ALRTI2C bit is set of I2CCONT is set. When I2CCONTEN = 0b0, STATUS2 register bit ALRTI2C does not depend on I2CCONT value.

I²C Bus Analog Contention Monitor

I2CANACONT is reported when the evaluated port result does not match the value seen on the analog filtered port. This monitor observes the SCL port and the SDA port when driven by the I²C Master. The contention monitor is always enabled. When I2CANACONTEN = 0b1, STATUS2 register bit ALRTI2C bit is set of I2CANACONT is set. When I2CANACONTEN = 0b0, STATUS2 register bit ALRTI2C does not depend on I2CANACONT value.

I2CANACONT vs. I2CCONT

I2CCONT monitors the raw value of the SDA/SCL ports. I2CANACONT monitors the internal analog filtered value of the SDA/SCL ports. The difference between I2CANACONT and I2CCONT is illustrated in the Figure 84 timing diagram.

The first diagram shows the fault of a weak pullup resistor on GPIO[0]. At time evaluation (green dotted line), the raw value (observed response) is slightly above Vih. However, the analog filtered value is still below Vih. Thus, only I2CANACONT is set.

The second diagram shows the fault when the I²C slave prematurely pulls GPIO[0] low while I²C master is still driving it high. Since the slave pulls GPIO[0] less than 1 analog filter time constant before the master pulls it low, the analog filtered value is still high but the raw value is low. Thus, only I2CCONT is set.

The third diagram shows the fault when GPIO[0] is stuck low. Both I2CANACONT and I2CCONT are set.

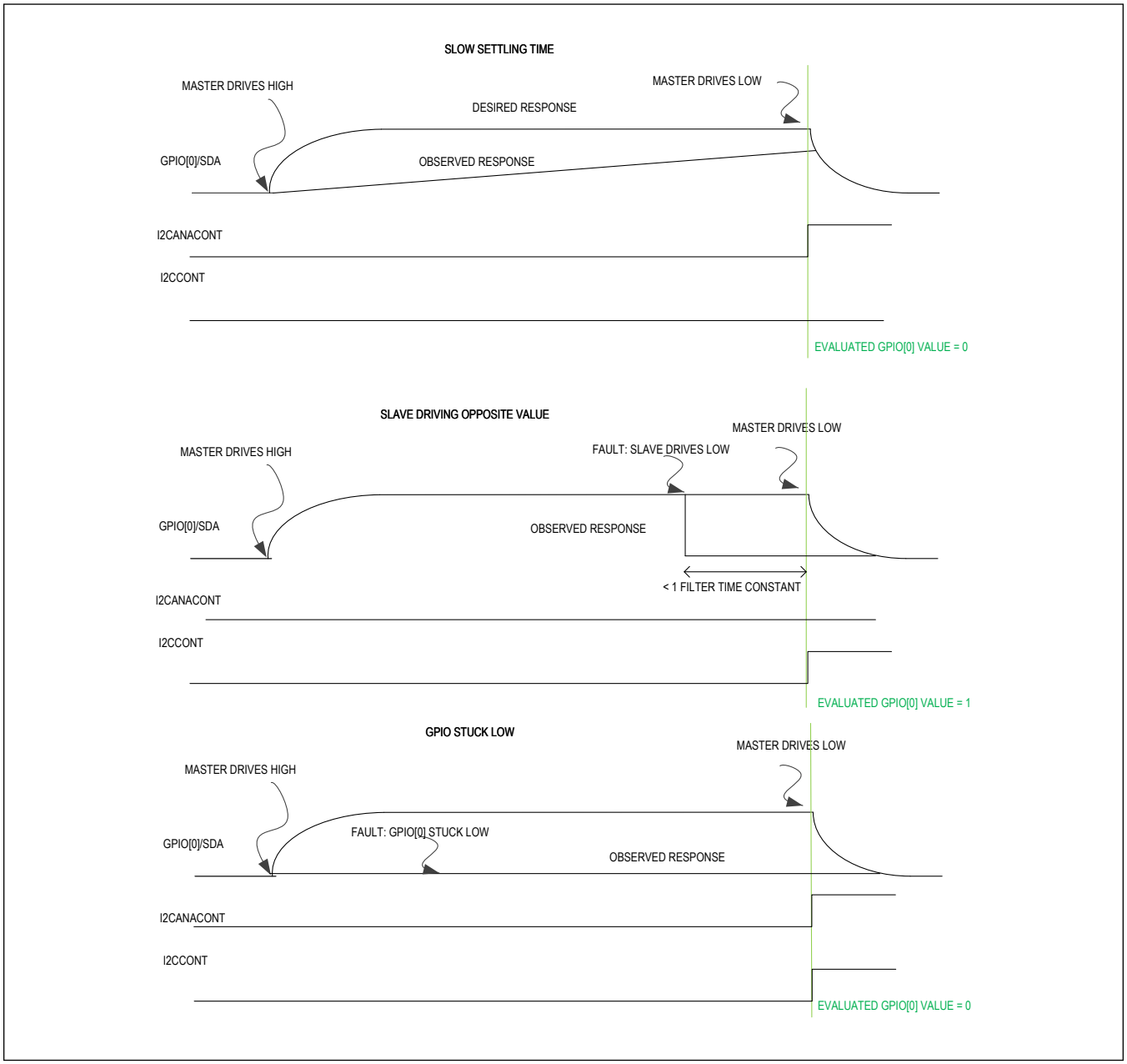


Figure 84. GPIO, I2CANACONT and I2CCONT timing diagram

I²C Glitch Monitor

I2CGLITCH is reported when a port monitor reports two or more consecutive 16MHz samples that disagree with the evaluated filter value. This condition may also be reported if slow transition times, setup time, or hold time violations occur (outside I²C specifications). This monitor observes the SCL port and the SDA port outside specified transition intervals. The glitch monitor is always enabled. When I2CGLITCHEN = 0b1, STATUS2 register bit ALRTI2C bit is set of I2CGLTICHEN is set. When I2CGLITCHEN = 0b0, STATUS2 register bit ALRTI2C does not depend on I2CGLITCH

value.

I²C Noise Monitor

I2CNOISE condition is reported when a port monitor see more than 25% of samples that disagree with the evaluated filter value. This condition may also be reported if slow transition times, setup time, or hold time violations occur (outside I²C specifications). This monitor observes the SCL port and the SDA port outside specified transition intervals. The noise monitor is always enabled. When I2CNOISEEN = 0b1, STATUS2 register bit ALRTI2C bit is set of I2CNOISE is set. When I2CNOISEEN = 0b0, STATUS2 register bit ALRTI2C does not depend on I2CNOISE value.

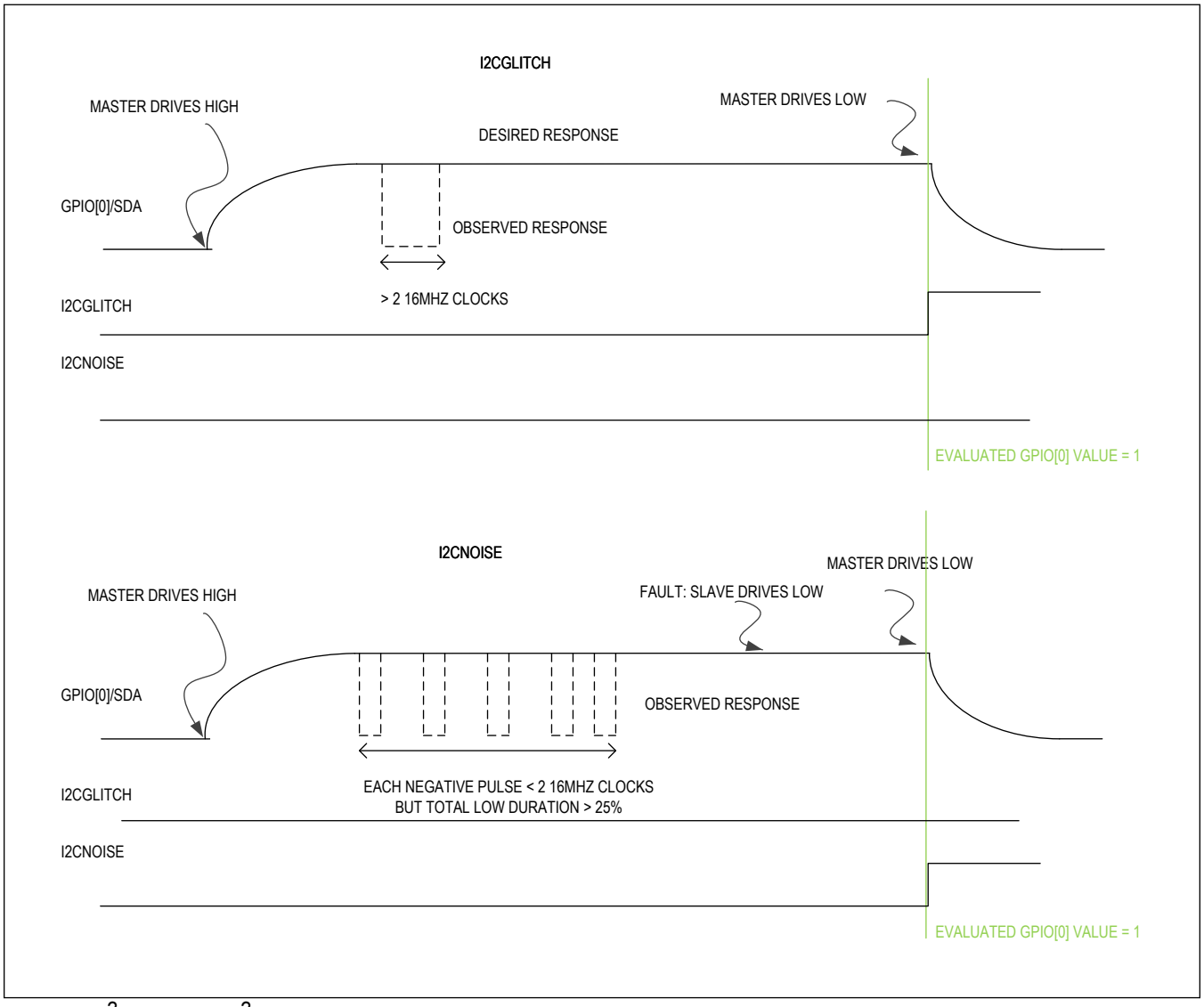


Figure 85. I²C Glitch and I²C Noise Monitor

I²C Repeated Read Checks

If Redundant Read Checking is enabled (I2CRDTREN = 0b1), all I²C Read Transactions will be automatically repeated twice in their entirety. The data received in the initial transaction will be loaded into the register space specified by

I2CDATALNGTH and I2CDATASEL as the transaction progresses. During the repeated transaction, the redundant data will be checked against the data received in the initial transaction before the data in register space specified by I2CDATASEL is overwritten with the redundant data.

If any mismatch is found, the I2CSTATUS will read back a Transaction Error (0b10) and the I2CRDTRERR alert component bit will be set high for the transaction. While the redundant data from the repeated transaction will be made available for read back in the register space specified, this data should be treated as compromised if I2CRDTRERR is set.

Note: Redundant Read Checking may not be advisable in some applications. In particular, if the slave device updates register content autonomously (and could change the data during/between the redundant transactions), or if the data requested is subject to noise (as might be the case if the read transaction triggers a measurement/observation which is read back). If used to read a FIFO with a pointer subject to increment upon read back, this method will not work. Special consideration should be given when using Normal Format Read Transactions—in particular, if slave pointers are auto-incremented in response to read transactions, results may be incompatible with transactions of this type (without a preceding Write Transaction to reset the pointer to the original location. Review the operation of all slave devices carefully before using this feature.

There is no write mode equivalent of a redundant check. Write mode transactions are best checked for success via a read back of written slave register content, assuming the slave register supports R/W access.

I²C Watchdog Timer

The I²C Watchdog Timer will monitor all transactions for completion in the expected time required for the command. If the I²C Watchdog Timer is enabled (I2CTOEN = 0b1), the I²C Master Transaction is monitored for completion against a time out limit based on the transaction requested and mode settings. If the transaction fails to complete, the transaction will be aborted (stopped), any missing read data bytes will not be updated, I2CSTATUS will show a Transaction Error (0b10), and the I2CTIMEOUT fault indicator bit will be set high. The I²C Watchdog Timer counts in 32 kHz clock increments; 488 us for 400 kHz operation, 1953 µs for 100 kHz operation, while I2CSEND is enabled. If terminal time is reached before completion of the current transaction, I2CSEND is cleared, and I2CTIMEOUT fault indicator bit is set, and the master returns to idle state (SDA = SCL = pulled high).

Freeing a Stuck I²C Bus

In the unlikely event of an aborted I²C Transaction (due to either an I²C time out fault, or an unexpected reset of the {max_num}), it is possible for a slave device to occupy the SDA bus and hold it in a low position. This would prevent the MAX17852 from issuing new transactions until the slave device vacates the SDA bus, allowing the I²C master to send Start and Stop information. If this were to occur, contention errors would be reported.

I²C Method (I2CEN = 1): In order to recover, I²C write transactions should be sent to a non-existent slave Device ID. The recommended transaction is a seven-bit address, single-byte data I²C Write transaction with all DEVID, PBYTE, and WBYTE content set to ones. Eventually, the slave device occupying the bus will recognize the SCL activity, vacate the SDA bus, and observe the STOP condition. Contention errors will continue to be reported until the bus is freed. Normal I²C communication should then be restored, and new transactions to valid slave Device IDs can proceed.

GPIO Method (I2CENB = 0): Alternatively, the bus can be freed by sending a stream of SCL pulses until the stuck slave device finishes its transaction and frees the bus. This can be accomplished by setting I2CEN = 0, and configuring AUX0/SDA as a GPIO input (GPIOEN[0] = 1, GPIODIR[0]=0, GPIODRV=x) and configuring AUX1/SCL as a GPIO output (GPIOEN[1] = 1, GPIODIR[1] = 1, GPIODRV = toggle). Send SCL pulses using GPIODRV[1] until the slave frees SDA (GPIORD[0] = 1 for a sustained number of SCL cycles. Once the slave vacates the bus, it will be able to observe the START/STOP conditions present in normal I²C transactions, and communication will be restored.

Alert Interface

The alert interface communicates the presence of a fault condition generated from the logical OR of the STATUS1 register, which flags any error within safety critical functionality: voltage measurements, temperature measurements, interface communication robustness, calibration, and other internal hardware diagnostics. As the safety consideration per platform may differ, each of the associated alerts can be masked to provide individualized control. Additionally,

the interface may be actively driven without the need of an actual alert condition to validate the functionality when commanded. This is done using the ALRTUSER bit in the FMEA2 register.

The alert interface, by default, is a single-ended, unidirectional interface using the ALERTIN and ALERTOUT pins. The ALERTIN pin is configured as a single-ended UART receiver with RXP grounded (see UART Receiver section for details). The ALERTOUT uses a single UART Transmitter as its output driver. If UARTSEL = 0 (SPI Interface), ALERTOUT becomes a DC active-low output which can be configured for Open-Drain (Wired-OR) or CMOS operation. For UARTSEL = 1 (UART Interface), ALERTOUT is an AC CMOS output.

Alternatively, a differential alert interface can be configured as using the UARTCFG bits as discussed in the UART Interface section as shown in the Single Ended RX Mode section. The Differential Alert Interface allows for robust low cost configurations using capacitive isolation to communicate the presence of a fault, where the single ended configuration allows for full UART flexibility at the need for an different isolation component (opto-isolators).

Table 64. Alert-Interface Configuration in UART Mode

UARTCFG	UART CONFIGURATION	UART UP PATH	UART DOWN PATH	SINGLE ENDED ALERT
0b00	Single UART Interface with External Loopback	Active	Inactive (Buffered/Pass Through)	ALERTEN Configured
0b01	Single UART Interface with Internal Loopback	Active	Inactive (Buffered/Pass Through)	ALERTEN Configured
0b10	Single UART Interface with Differential Alert Interface	Active	Differential Alert	Disabled (except in ALRTDCTSTEN mode)
0b11	Dual UART Interface	Active	Active	ALERTEN Configured

If the hardware alert interface is disabled then no alerts can be communicated via the hardware interface options. The ALERTIN pin will remain a high impedance input and will not respond to any input. Table 65 describes the configuration of the alert output drivers for both single-ended or differential alerts.

Note: Although the alert hardware interface can be disabled, the user will still have the option to validate alerts by reading the STATUS registers as well as the communication of the UART Data-Check byte or SPI ALERT Status bit.

Table 65. Alert Output Driver Configuration

UARTSEL	UARTCFG	SPIDRVINT	ALERTOUT ACTIVE/ASSERTED	ALERTOUT INACTIVE/ DEASSERTED OR ALERTEN=0
SPI (Pulldown)	Don't Care	0 (Open Drain)	0	Hi-Z
SPI (Pulldown)	Don't Care	1 (CMOS)	0	1
UART (Pullup)	0b00, 0b01, 0b11	Don't Care	AC Active	GND (TXLIDLEHIZ = 0) Hi-Z (TXLIDLEHIZ = 1)
UART (Pullup)	0b10 (Differential)	Don't Care	GND (TXLIDLEHIZ = 0) Hi-Z (TXLIDLEHIZ = 1)	GND (TXLIDLEHIZ = 0) Hi-Z (TXLIDLEHIZ = 1)
UART (Pullup) ALERTDCTSTEN = 1	Don't Care	Don't Care	0	1

SPI Mode Alert Operation (UARTSEL = 1'b0)

When configured to communicate via the SPI interface (UARTSEL= 0), the ALERTOUT driver is re-configured as an open-drain output or CMOS output depending on the SPIDRVINT selection. If an alert is present, the ALERTOUT output is driven active-low. This is done to minimize power consumption of the application when configured as an open-drain output. If no ALERT condition is present, the ALERTOUT will be driven high (CMOS mode) or pulled high through an external connection to a pullup resistor for the open-drain configuration.

The open-drain configuration allows for the ALERTOUT signal to be logically OR'ed with any other signals at the application level to drive a host controller interrupt.

Note: If an open-drain configuration, the voltage should not exceed V_{DDL2}.

In the SPI mode, there are no daisy-chain devices, so any signal on the ALERTIN input is ignored.

UART Mode Alert Detection (UARTSEL = 1'b1)

This alert interface will outputs a 2MHz continuous square wave with 50% duty cycle in the presence of a fault condition. The fault output will persist for the duration of the fault and will be updated at the rate determined by the scan mode. For a valid alert command to be recognized at the ALERTIN pin, the signal must be valid for 25µs and at the desired frequency. If the duration is shorter than the allocated time or at a different frequency then this will not be recognized as fault and signal will not be propagated to the host. SeeFigure 86.

In the absence of an alert, the output status depends on TXLIDLEHIZ - TXLIDLEHIZ = 1'b1, ALERTOUT is driven HIZ, and TXLIDLEHIZ = 1'b0, ALERTOUT is driven low.

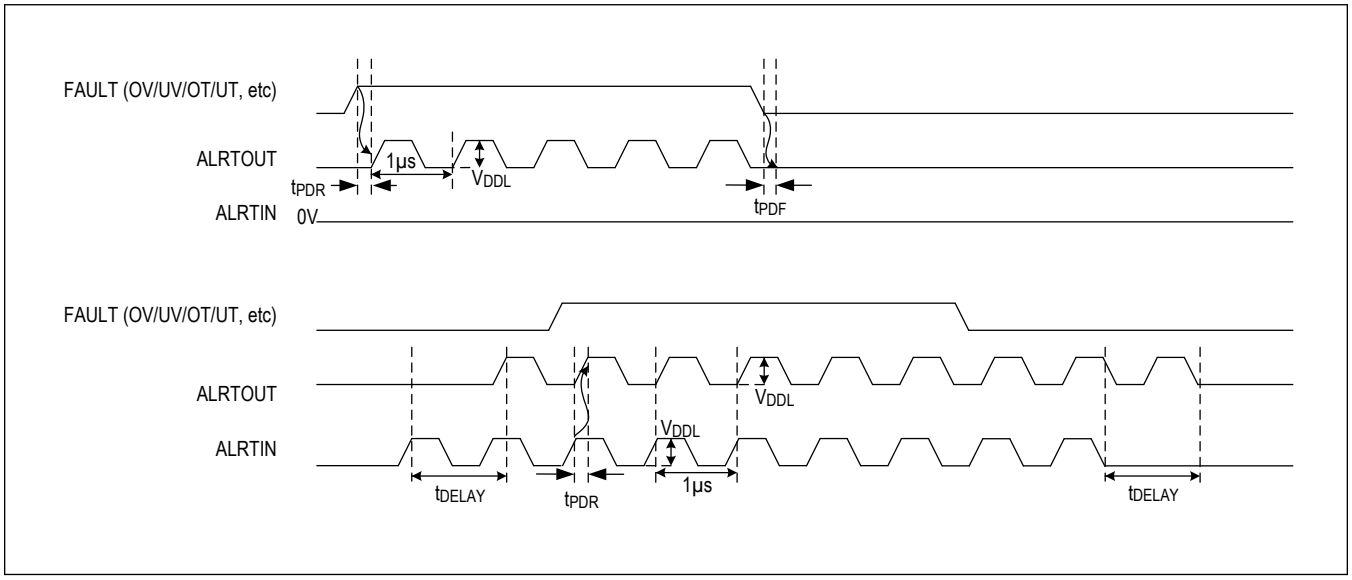


Figure 86. UART Mode Alert Detection Timing Diagram

ALERT Interface Masking Operations

The Alert interface activity is based on the contents of the STATUS1 register. Individual alert conditions can be masked out of the Alert Interface using settings in ALRTIRQEN; however, the underlying alert information will always be available for readback in the STATUS1 register.

Active =

(ALRTSCAN & SCANALRTEN) or ALRTRST or (ALRTMSMTCH & MSMTCHALRTEN) or

(ALRTCELLOVST & CELLOVSTALRTEN) or (ALRTCELLUVST & CELLUVSTALRTEN) or

(ALRTBLKOVST & BLKOVALRTEN) or (ALRTBLKUVST & BLKUVALRTEN) or

(ALRTAUXOVST & AUXOVSTALRTEN) or (ALRTAUXUVST & AUXUVSTALRTEN) or

(ALRTCSAST & CSASTALRTEN) or

(ALERTPEC & PECALRTEN) or (ALRTINTRFC & INTRFCALRTEN) or

(ALRTCAL & CALALRTEN) or (ALRTCBAL & CBALALRTEN) or

(ALRTFMEA1 & FMEA1ALRTEN) or (ALRTFMEA2 & FMEA2ALRTEN)

Note: ALRTRST indicates a POR condition, and thus cannot be masked.

ALERTPACKET STATUS Masking

The UART Alert Packet content is based on the contents of the STATUS1 register. Individual alert conditions can be masked out of the Alert Packet using settings in ALRTIRQEN register; however, the underlying alert information will always be available for read back in the STATUS1 register. The masking operations for each STATUS1 bits is detailed below.

ALRT_PKT_STAT[15] = 0

ALRT_PKT_STAT[14] = ALRTRST

ALRT_PKT_STAT[13] = (ALRTMSMTCH & MSMTCHALRTEN)

ALRT_PKT_STAT[12] = (ALRTCELLOVST & CELLOVSTALRTEN)

ALRT_PKT_STAT[11] = (ALRTCELLUVST & CELLUVSTALRTEN)

ALRT_PKT_STAT[10] = (ALRTBLKOVST & BLKOVALRTEN)

ALRT_PKT_STAT[9] = (ALRTBLKUVST & BLKUVALRTEN)

ALRT_PKT_STAT[8] = (ALRTAUXOVST & AUXOVSTALRTEN)

ALRT_PKT_STAT[7] = (ALRTAUXUVST & AUXUVSTALRTEN)

ALRT_PKT_STAT[6] = (ALRTCSAST & CSASTALRTEN)

ALRT_PKT_STAT[5] = (ALRTPEC & PECALRTEN)

ALRT_PKT_STAT[4] = (ALRTINTRFC & INTRFCALRTEN)

ALRT_PKT_STAT[3] = (ALRTCAL & CALALRTEN)

ALRT_PKT_STAT[2] = (ALRTCBAL & CBALALRTEN)

ALRT_PKT_STAT[1] = (ALRTFMEA1 & FMEA1ALRTEN)

ALRT_PKT_STAT[0] = (ALRTFMEA2 & FMEA2ALRTEN)

Note: STATUS1[15]:ALRTSCAN is a procedural notification bit and is intentionally not included in the UART Alert Packet; it is available for inclusion in the ALERT Interface, to support interrupt-driven applications. STATUS1[14]:ALRTRST indicates a POR condition, and thus cannot be masked.

Alert Masking TOPCELL1/2

If the battery stack contains less than 14 cells and the Flexible Pack Configuration is not enabled, then lowest-order inputs (e.g. C1 and C0) should be utilized first and connected to the lowest common-mode signals. Any unused cell inputs should be shorted together and unused switch inputs should be shorted together. The TOPCELL1 and TOPCELL2 registers will mask all ALRTBALSW diagnostics from being reported.

All selections are supported for this function, and if TOPCELL2 is not equal to TOPCELL1, no alerts are masked.

Low-Voltage Regulator

An internal linear regulator supplies low-voltage power (V_{AA}) for the ADC and digital logic. The regulator is disabled when SHDNL is active-low or when the die temperature (T_{DIE}) exceeds 145°C. Once V_{AA} decays below 2.95V typical, an internal power-on reset (POR) will be generated as summarized in Table 66 and shown in Figure 87. This POR event can be detected with the ALRTRST bit as shown in Table 67. After a thermal shutdown, the regulator will not be enabled until T_{DIE} < 130°C due to hysteresis.

Table 66. Low-Voltage Regulator Operating Characteristics

INPUT:	**DCIN**
Input Voltage:	9V to 65V
Output:	V_{AA}
Output Voltage:	3.3V
Disable:	V_{SHNDL} < 0.6V or T_{DIE} > 145°C

Table 67. Low-Voltage Regulator Diagnostic

FAULT	CONDITION	ALERT	LOCATION
V_{AA} under-voltage	V_{AA} < 2.95V	ALRTRST	STATUS1

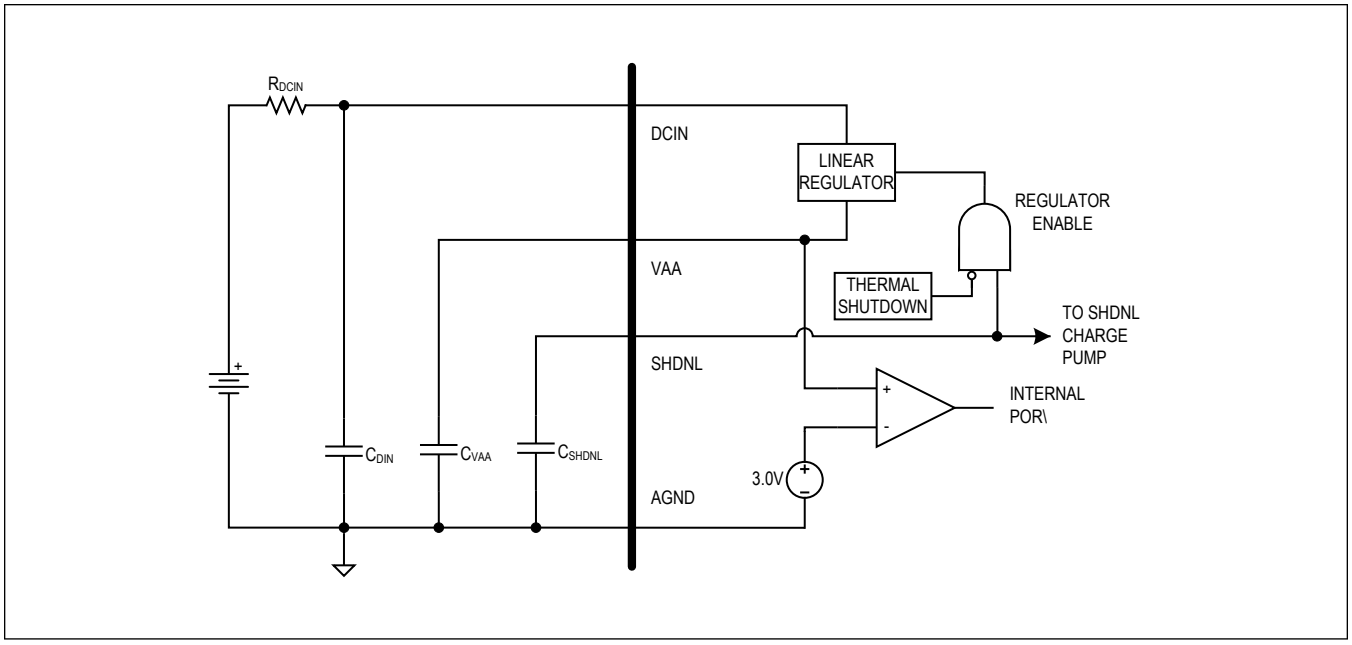


Figure 87. Low-Voltage Regulator and Thermal-Shutdown Circuit

HV Charge Pump

The high-voltage multiplexers must be powered by a supply higher than any monitored voltage. To this end, an internal charge pump draws power from the DCIN pin to provide a high-voltage supply V_{HV} which is regulated to V_{DCIN} + $V_{HV-DCIN}$. When the charge pump achieves regulation, $V_{HV-DCIN}$, charge pumping stops until the voltage drops by 20mV. The charge pump is automatically disabled during shutdown.

During the measurement cycle for ADC, Comparator, ADC+COMP, and Calibration, the charge pumping is paused to eliminate any potential impact of the charge pump noise within the measurements. The charge pump will then become active, operating on an 83KHz clock, during an inter-charge time (defined as the time between consecutive scan sequences) which lasts for 57µs on the ADC, Comparator, and ADC+COMP. During calibration, the inter-charge time is reduced to 21us. The inter-charge time ensures that the charge on C_{HV} capacitor is replenished prior to the next measurement cycle.

Note: The charge pump is operational during AUXTIME, CELLDLY, and SWDLY settling periods greater than 30µs, which is considered a worst settling delay for the SW input.

Outside of an acquisition, the charge pump is clocked at 32kHz.

An undervoltage comparator detects if $V_{HV-DCIN}$ drops below V_{HVUV}. If an undervoltage is detected the ALRTHVUV bitfield is set. Assertion of the ALRTHVUV bit is gated until ALRTRST is cleared for the first time following power-up.

An overvoltage comparator disables the charge pump when VHV - VDCIN exceeds VHVOV. This condition is indicated by the ALRTHVOV bit in the FMEA1 register; the ALRTHVOV alert does not necessarily indicate a condition that affects measurement accuracy. HV charge-pump diagnostics are summarized in Table 68.

If V_{HV} drops too low relative to the top cell inputs, there is insufficient headroom to guarantee that the HVMUX switch resistance is sufficiently low or enough headroom exists for the LSAMP1 and LSAMP2 input for an accurate acquisition

of the channel. Headroom alerts are indicated with the ALRTHVDRM bit in the FMEA1 register.

The HV undervoltage and HV headroom alert functions can be verified by disabling the HV charge pump HVCPDIS = 1 and allowing V_{HV} to decay while in acquisition mode.

Table 68. HV Charge Pump Diagnostics

FAULT	CONDITION	ALERT BIT	LOCATION
V_{HV} undervoltage	$V_{HV} - V_{DCIN} < V_{HVUV}$	ALRTHVUV	FMEA1:ALRTHVUV
V_{HV} overvoltage	$V_{HV} - V_{DCIN} > V_{HVOV}$	ALRTHVOV	FMEA1:ALRTHVOV
V_{HV} low headroom	$V_{HV} - V_{TOPCELL1/2} < V_{HVHDRM}$ (max)	ALRTHVHDRM	FMEA1:ALRTHVHDRM

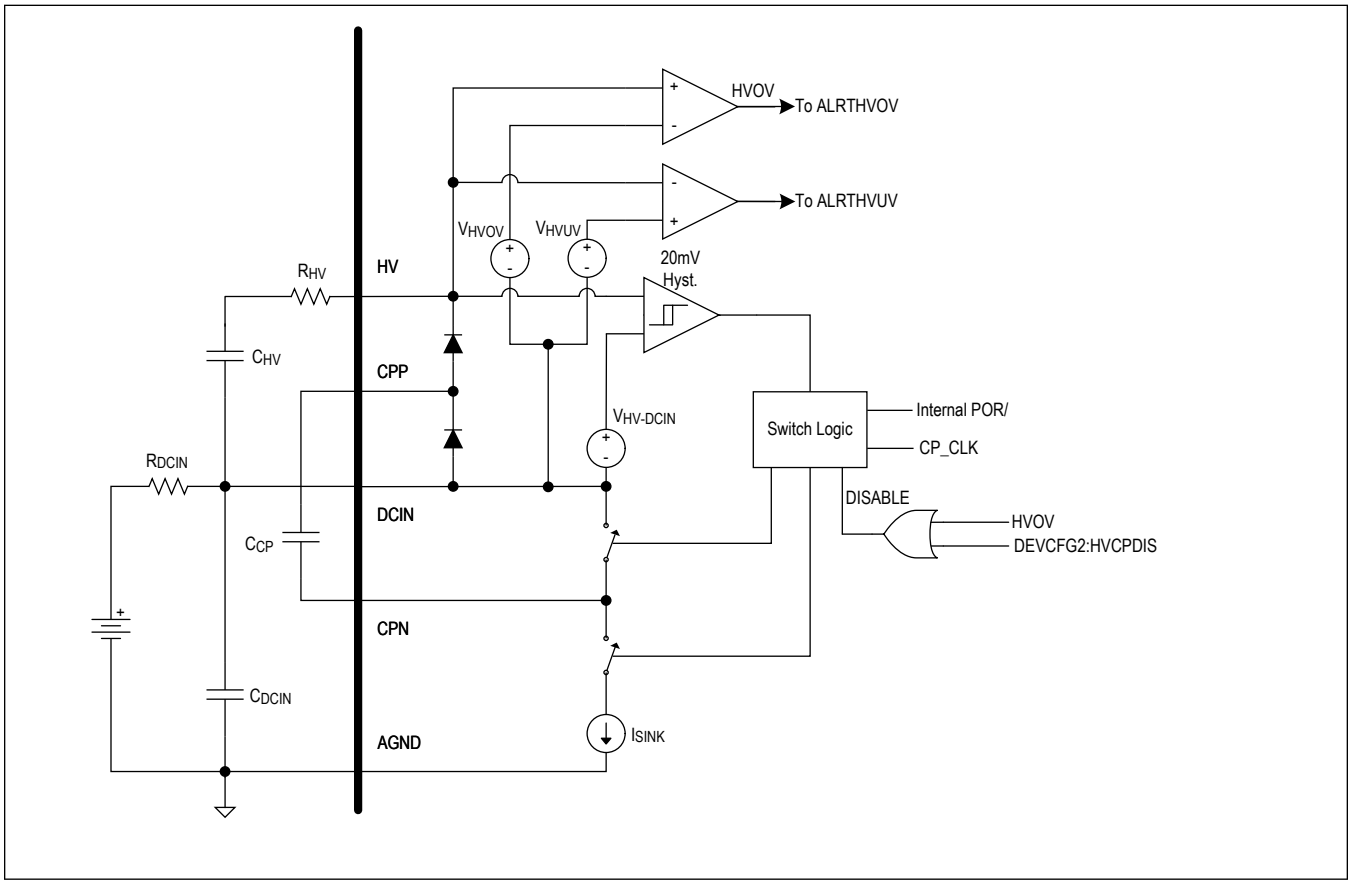


Figure 88. HV Charge Pump

Oscillators

Two factory-trimmed oscillators provide all timing requirements: a 16MHz oscillator for the UART and control logic, a 32.768kHz oscillator for the HV charge pump and timers. A special diagnostic counter, clocked by the 16MHz signal, is employed to check the 32kHz oscillator. Every two periods of the 32kHz clock, the counter is sampled. If the count varies more than 5% from the expected value, the *ALRTOSC1* bit is set as shown in Table 69. A redundant alert bit, ALRTOSC2 bit, increases the integrity level. If the 16MHz oscillator varies by more than 5%, for UART part, communication errors may be indicated. For SPI configuration, the ALRTOSC3 bit is set as shown in Table 69.

Table 69. Oscillator Diagnostics

FAULT	CONDITION	ALERT BIT	LOCATION
32.768kHz oscillator	31.129kHz > f_{osc_32k} > 34.406kHz	ALRTOSC1	FMEA1[15]
32.768kHz oscillator	31.129kHz > f_{osc_32k} > 34.406kHz	ALRTOSC2	FMEA1[14]
16MHz oscillator	15MHz > f_{osc_16M} > 17MHz	ALRTOSC3	STATUS2[5]

DIAGNOSTICS

Built-in diagnostics support ISO 26262 (ASIL) requirements by detecting specific fault conditions as shown in Table 70. The device automatically performs some of the diagnostics while the host can perform others during initialization (e.g., at key-on) or periodically during operation as required by the application. Diagnostics performed automatically by the device are previously described in the relevant functional sections. A description of the diagnostics requiring specific configurations are provided in this section.

Note: Pin faults such as an open pin or adjacent pins shorted to each other must be detectable. Pin faults do not result in device damage but have a specific device response such as a communication error, or will be detectable through a built-in diagnostic. Analyzing the effect of pin faults is referred to as a pin FMEA. Contact Maxim Applications to obtain pin FMEA results.

Table 70. Summary of Built-In Diagnostics

DIAGNOSTICS PERFORMED AUTOMATICALLY BY DEVICE WITH NO HOST INTERVENTION		
FAULT	DIAGNOSTIC PROCEDURE	OUTPUT
VAA undervoltage	Continuous voltage comparison	ALRTRST
VHV undervoltage	Continuous voltage comparison	ALRTHVUV
VHV overvoltage	Continuous voltage comparison	ALRTHVOV
VHV low headroom	Voltage comparison – updated during measurement	ALRTHVHDRM
32kHz oscillator fault	Continuous frequency comparison	ALRTOSC1, ALRTOSC2
16MHz oscillator fault	Communication error checking	ALRTMAN, ALRTPAR, ALRTOSC3
Communication fault	Communication error checking	ALRTPEC, ALRTMAN, ALRTPAR
RX pin open/short	Verify RX mode after POR	ALRTCOMMSEUn/ALRTCOMMSELn
VDDLx pin open/short	Continuous voltage comparison	ALRTVDDLx
GNDLx pin open/short	Continuous voltage comparison	ALRTGNDLx
Die overtemperature	Temperature comparison	ALRTTEMP
Measurement accuracy	Accuracy comparison -updated after oversampled acquisition	ALRTCOMPACCOV/ALRTCOMPACCUV
Flex Pack fault	Continuous fault checking of Flex Pack operation	ALRTDCINMUX

DIAGNOSTICS PERFORMED DURING ACQUISITION MODE AS SELECTED BY DIAGSEL OR SCACFG (BALSW DIAGNOSTICS)			
FAULT	DIAGNOSTIC PROCEDURE	DIAGSEL[3:0] OR SCANCFG	OUTPUT
Die Temp (PTAT) fault	Die Temperature (PTAT) diagnostic	DIAGSEL1/2 = 1h	DIAGSEL1/2[15:0] = PTAT Voltage
V_{AA} voltage fault	V_{AA} Verification	DIAGSEL1/2 = 2h	DIAGSEL1/2[15:0] = V_{AA} Voltage
Reference voltage fault	ALTREF verification	DIAGSEL1/2 = 3h	DIAGSEL1/2[15:0] = ALTREF Voltage
Comp cell signal path fault	Comp signal path verification	DIAGSEL1/2 = 4h	DIAGSEL1/2[15:0] = COMP Error Voltage

Table 70. Summary of Built-In Diagnostics (continued)

Cell gain calibration fault	Cell gain calibration verification	DIAGSEL1/2 = 5h	DIAGSEL1/2[15:0] = Calibration Voltage (6/13)
Offset calibration fault	Offset calibration verification	DIAGSEL1/2 = 6h	DIAGSEL1/2[15:0] = Calibration Offset Voltage (0V)
DAC bit stuck high	DAC 3/4 Scale	DIAGSEL1/2 = 7h	DIAGSEL1/2[15:0] = DAC Code 1772d
DAC bit stuck low	DAC 1/4 Scale	DIAGSEL1/2 = 8h	DIAGSEL1/2[15:0] = DAC Code 591d
NTC(THRM)offset calibration fault	NTC(THRM) offset calibration verification	DIAGSEL1/2 = 9h	DIAGSEL1/2[15:0] = Calibration Offset Error with THRM
ADC bit stuck high	Zero-Scale ADC diagnostic	DIAGSEL1/2= Ah	DIAGSEL1/2[15:0] = ADC Zero Scale
ADC bit stuck low	Full-Scale ADC diagnostic	DIAGSEL1/2 = Bh	DIAGSEL1/2[15:0] = ADC Full Scale
LSAMP offset too high	LSAMP offset diagnostic	DIAGSEL1/2 = Ch	DIAGSEL1/2[15:0] (LSAMP offset voltage)
Balancing switch short	BALSW diagnostic mode	SCANCFG = 4h	ALRTBALSW, FMEA1:ALRTBALSWSUM
Balancing switch open	BALSW diagnostic mode	SCANCFG = 5h	ALRTBALSW, FMEA1:ALRTBALSWSUM
Odd Cell sense-wire open	BALSW diagnostic mode	SCANCFG = 6h	ALRTBALSW, FMEA1:ALRTBALSWSUM
Even Cell sense-wire open	BALSW diagnostic mode	SCANCFG = 7h	ALRTBALSW, FMEA1:ALRTBALSWSUM
Procedural diagnostics: Contact Maxim Applications for the complete listing of procedural diagnostics found in the safety manual.			

ALERTOUT Pin to Pin Short Diagnostic

The UART Alert DC Diagnostic Test is used to test the ALERTOUT pin for shorts to AUXIN0/GPIO0 pins. When UARTSEL = 0b1 (UART mode), this test is enabled by setting ALERTDCTSTEN bit to 0b1.

When the DC Diagnostic Test is enabled, the ALERTOUT pin will be driven low if an Alert condition is present, and driven high otherwise. ALRTUSER bit field can be written to exercise ALRTOUT in either direction. Neighboring pins such as AUXIN0/GPIO0 can be monitored directly or in diagnostic modes to detect a fault.

This function works in all UARTCFG modes, including the differential alert, which does not normally use the ALERTOUT pin. This setting has no impact in SPI mode (UARTSEL = 0), the same functionality can be realized using SPIDRVINIT and ALRTUSER.

CELL Pin Open Diagnostics

If an input of the MAX17852 is disconnected from the cell input through any mechanical failure, the position of the failure can be detected by performing cell-open diagnostics. It is recommended that comparator measurements are used for quick identification against the default threshold setting COMPOPNTH. If measurement is below the set threshold, the corresponding cell alerts are flagged in ALRTCOMPOV.

This diagnostic is enabled by setting CELLOPNDIAGSEL = 1 and performing comparator scan (SCANCFG = 0b010). Only unipolar measurements are allowed for this diagnostic and if a cell position is set as bipolar, the corresponding cell is skipped and the alert flag is not set for that bipolar cell. Normally in Open Diagnostic modes, pulldown current sources are enabled on all measured channels using CTSTEN for required cells. Various current-configuration settings are available for the user and can be configured using the DIAGCFG:CTSTDAC bitfield.

Die Temperature Measurement

The die temperature measurement allows the host to compute the device temperature (T_{DIE}) as it relates to the acquisition accuracy and allows the device to automatically shut itself down when T_{DIE} > 145°C. The measurement employs a source whose voltage, V_{PTAT}, is proportional to absolute temperature (PTAT) as shown in Figure 89 below. The V_{PTAT} measurement is enabled by setting DIAGSEL1[3:0] or DIAGSEL2[3:0] to 0b0001 and the 14-bit measurement is stored in DIAG1 = DIAG1REG[15:2] or DIAG2 = DIAG2REG[15:2], respectively. The die temperature measurement requires a settling time of 39µs from the start of the measurement cycle until the diagnostic conversion. As long as two

or more cell measurements are enabled, there will be sufficient settling time for this measurement. Refer to the can we say acquisition timing sections for more details.

The PTAT voltage is computed as follows:

Equation 2:

$$V_{PTAT} = (DIAG1 / 16384d) \times V_{REF}$$

or

$$V_{PTAT} = (DIAG2/ 16384d) \times V_{REF}$$

Where V_{REF} = 2.3077V. The measured voltage can be converted into °C as follows:

Equation 3:

$$T_{DIE} (in °C) = (V_{PTAT} / A_{V_PTAT}) + T_{OS_PTAT} - 273°C$$

Refer to *Electrical Characteristics* for A_{V_PTAT} and T_{OS_PTAT} values.

Die Temperature Alert

The die temperature is continuously monitored in an interval of 1ms to detect if the $T_{DIE} > T_{ALRTTEMP}$. In the event that die temperature is greater, ALRTTEMP bit in FMEA2 register is asserted. The only exception is that ALRTTEMP monitoring is temporarily disabled when the die temperature measurement is requested by configuring DIAGSEL1[3:0] or DIAGSEL2[3:0] = 1h. The signal path for Die Temperature alert and measurement is shown in Figure 89 below.

If ALRTTEMP is set, the host should consider the possibility that the acquisition does not meet the expected accuracy specification, or that the die temperature measurement itself may be inaccurate due to insufficient settling time (< 2 cell measurements enabled).

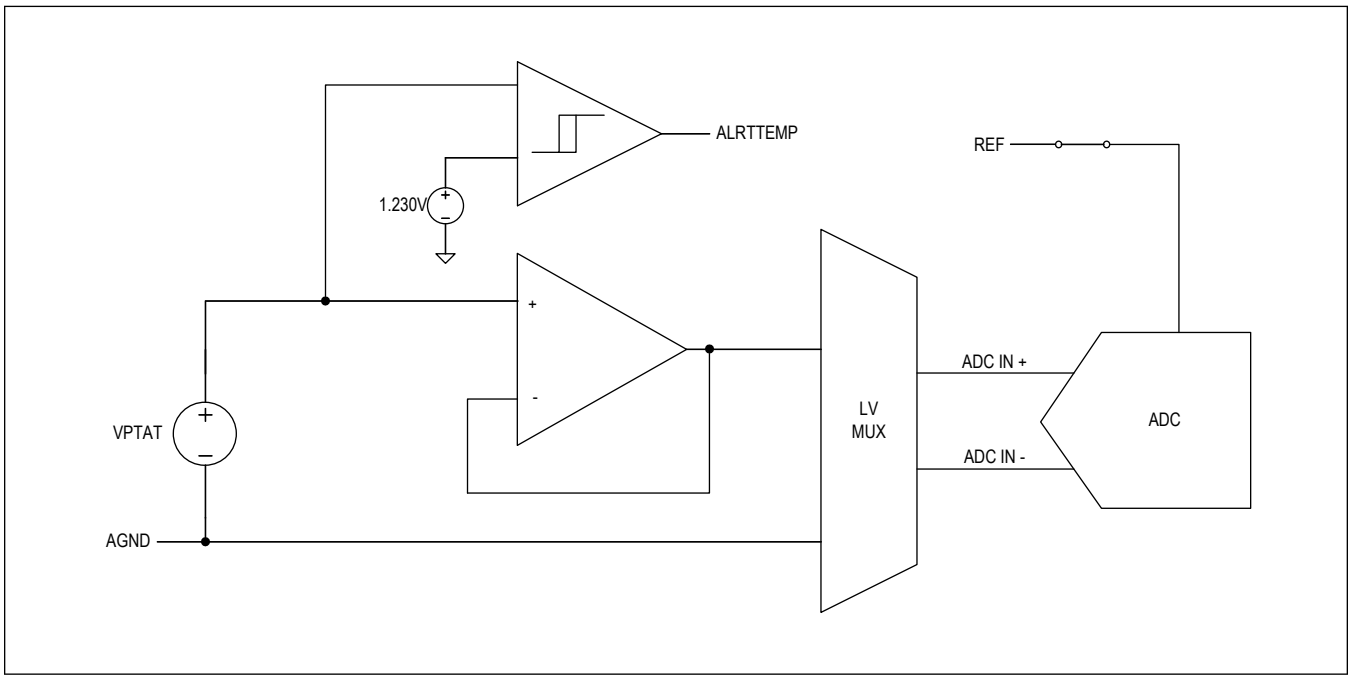


Figure 89. Die Temperature Measurement

V_{AA} Diagnostic Measurement

The V_{AA} diagnostic measurement (DIAGSEL1 or DIAGSEL2 = 0b0010) verifies that V_{AA} is within specification. This

diagnostic measures V_{REF} while using V_{AA} as the ADC reference. Signal path for the V_{AA} diagnostics is as shown below in Figure 90

The voltage into the ADC is computed from the result in the DIAG1REG (or DIAG2REG) register as follows:

Equation 2:

$$(6/13) \times V_{REF} = (DIAG1REG[15:2] / 16384) \times V_{AA}$$

V_{AA} can be calculated as follows:

Equation 3:

$$V_{AA} = (6/13) \times V_{REF} \times 16384 / DIAG[15:2]$$

where V_{REF} = 2.3077V

The result for V_{AA} should fall within the range provided in the *Electrical Characteristics* table for V_{AA}.

For ADCCALEN = 1, the 14-bit ADC measurement which passes the diagnostic ranges from 0x1576 to 0x13E4 based on *Electrical Characteristics* table specs.

For ADCCALEN = 0, the 14-bit ADC measurement which passes the diagnostic ranges from 0x1592 to 0x13CA based on *Electrical Characteristics* table specs.

Note: With any sampled measurement, the signal chain noise performance must be considered within the measurement result. For consistent measurement performance, V_{AA} is recommended to be averaged within multiple system measurement cycles to mitigate the variation seen by noise.

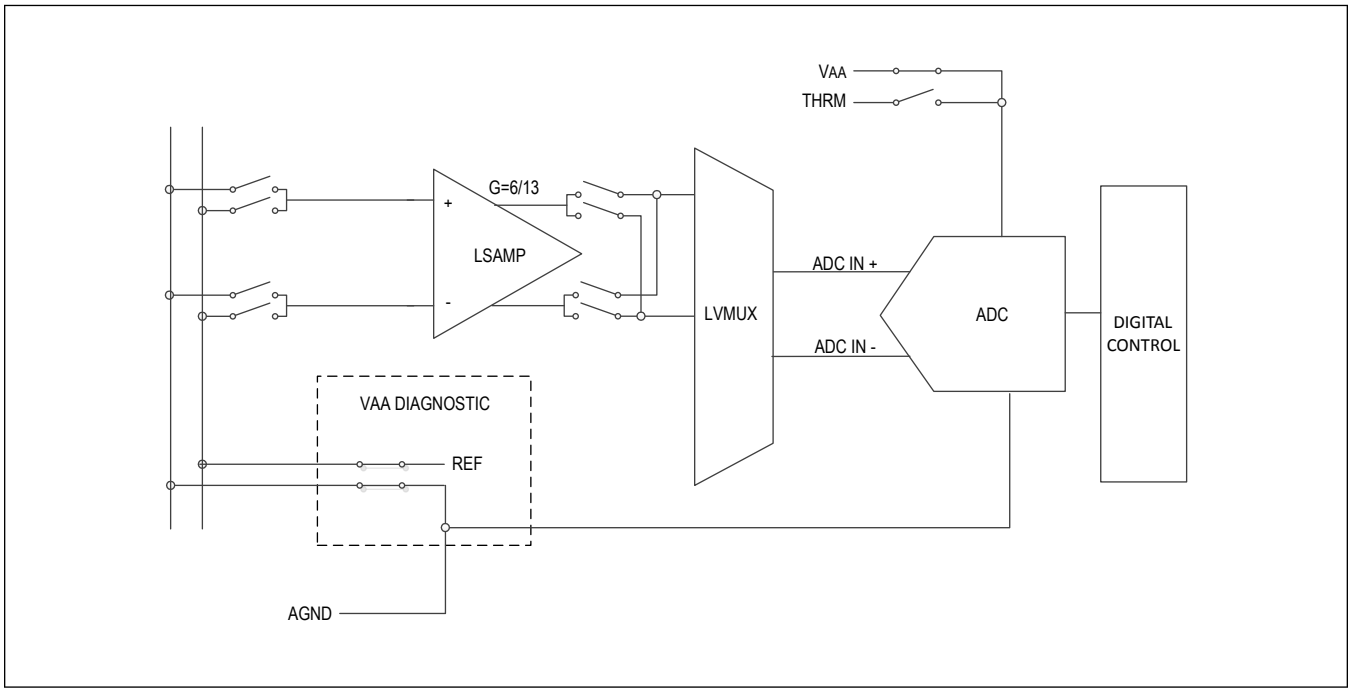


Figure 90. V_{AA} Diagnostic

ALTREF Diagnostic Measurement

The ALTREF diagnostic measurement (DIAGSEL1 or DIAGSEL2 = 0b0011) checks the primary voltage reference of the ADC by measuring the alternate reference voltage, (V_{ALTREF}), while using V_{REF} as the ADC reference. The result is available in the DIAG1REG (or DIAG2REG) registers. The ALTREF voltage is computed from the result in the DIAG register as follows:

Equation 1:

$$V_{ALTREF} \times (6/13) = (DIAG[15:2] / 16384) \times V_{REF}$$

Because $V_{REF}/(6/13)$ should nominally equal 5V, V_{ALTREF} can be determined as follows:

Equation 2:

$$V_{ALTREF} = (DIAG[15:2] / 16384) \times 5V$$

During ALTREF Diagnostic measurements ADC is automatically set to unipolar mode. Signal path for ALTREF Diagnostic is as shown in Figure 91 below.

Since $1.23V < V_{ALTREF} < 1.254V$ and $V_{ALTREF} = 1.242V$ nominally, the expected range for DIAG[15:2] are shown below.

For ADCCALEN = 1, the 14-bit ADC measurement which passes the diagnostic ranges from 0x0FFA to 0xFD5.

For ADCCALEN = 0, the 14-bit ADC measurement which passes the diagnostic ranges from 0x1024 to 0xFAE.

Note: With any sampled measurement, the signal chain noise performance must be considered within the measurement result. For consistent measurement performance, (V_{ALTREF}) is recommended to be averaged within multiple system measurement cycles to mitigate the variation seen by noise.

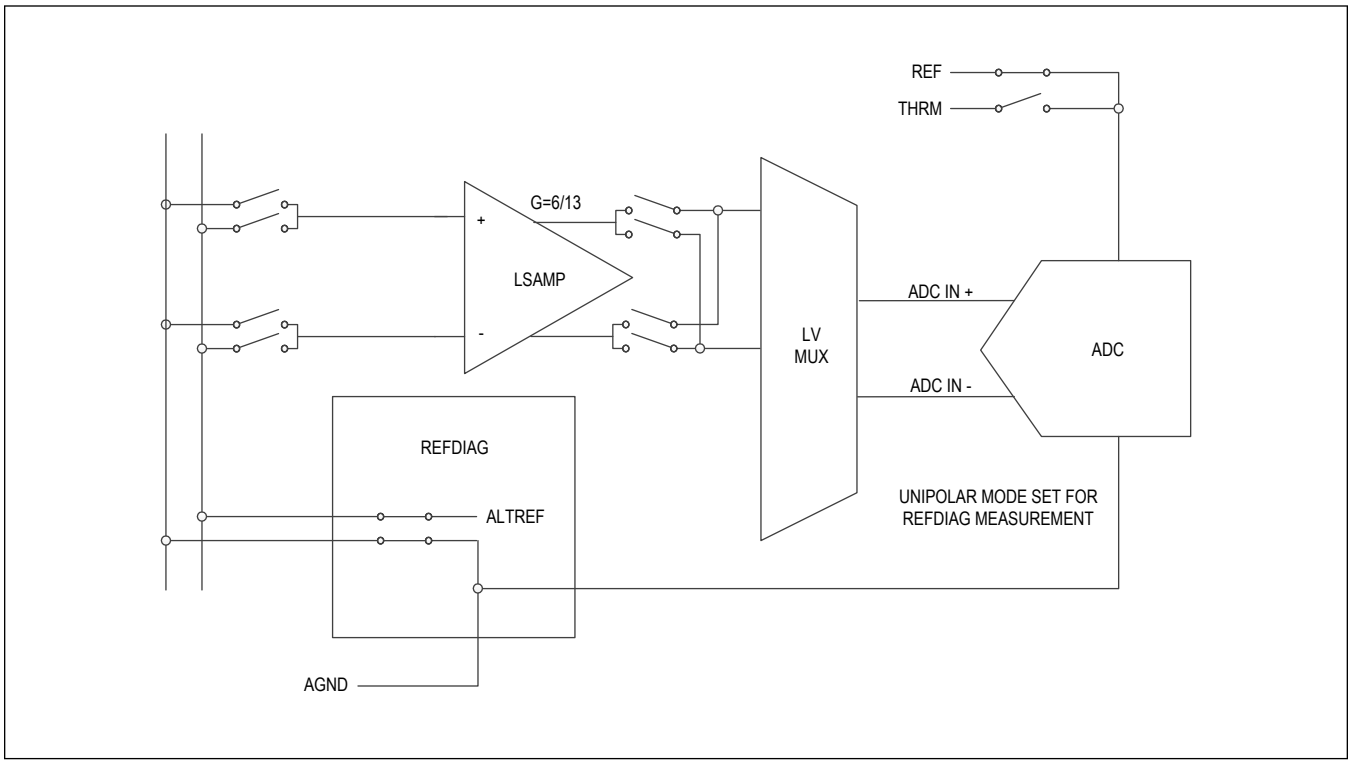


Figure 91. ALTREF Diagnostic

Diagnostic Measurement

The comparator signal-conditioning path can be measured by the ADC, which allows for the following capabilities:

- Comparator functionality verification against specification
- Comparator thresholds calibration
- Increased comparator performance for improved specification beyond that described in the electrical specifications

The functionality of the comparator signal conditioning path (shown in Figure 92) can be measured using DIAGSEL1 = 0b0100 or DIAGSEL2 = 0b0100 in the DIAGCFG register. This configuration applies an input of V_{REF} = 2.3077V to the LSAMP2 while the DAC is programmed to 0x1D8 (DAC reference of 2.3077V). The LSAMP2 path is gained up by 6 and compared against the DAC output gained by a factor of 13. The output of the comparator pre-amp is routed to the ADC input where it is effectively measured. The result of the adc measurement will be presented in corresponding DIAG1REG[15:2] or DIAG2REG[15:2] registers.

Note: It is recommended to calibrate the ADC prior to running this diagnostic to improve the accuracy of the comparator signal path measurement.

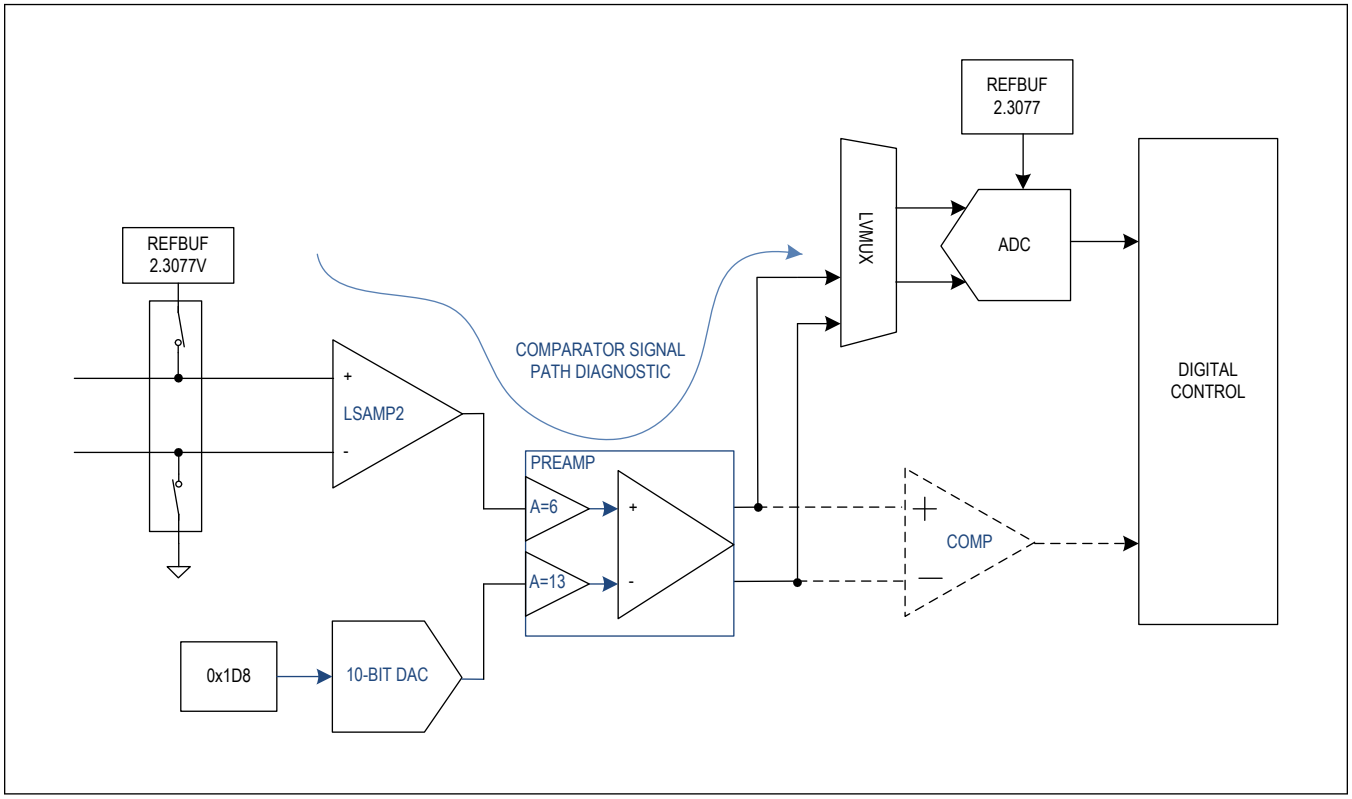


Figure 92. Comparator Signal Path to ADC

Comparator functionality is verified by comparing the DIAG register outputs against the ranges shown in table shown below:

Table 71. Comp Signal Path Diagnostic Verification Ranges

	UPPER DIAGNOSTIC RANGE	LOWER DIAGNOSTIC RANGE
ADCALEN = 1	0x2480	0x1BC0
ADCALEN = 0	0x24A0	0x1BA0

In addition to verifying functionality against the specification, the DIAG register output can be used to calculate the error of the comparator cell signal path as shown in the following equation.

$$\varepsilon_{COMP_CELLPATH} = \frac{1}{13} \cdot \left(\frac{DIAG1REG[15:2] - 0d8224}{0d16384} \right) \cdot 5V$$

The error can then be used by the user to manually adjust the comparator OV and UV thresholds (COMPOVTH, COMPUVTH, COMPACCOVTHREG, COMPACCUVTHREG) to ensure that the thresholds are applied to the true

comparator performance.

$$COMPOVTH_{Adjusted} = COMPOVTH_{Desired} + Round(\varepsilon_{COMP_CELLPATH} x 1023 / 5)$$

$$COMPUVTH_{Adjusted} = COMPUVTH_{Desired} + Round(\varepsilon_{COMP_CELLPATH} x 1023 / 5)$$

Note: the above threshold corrections cannot be applied to the AUX measurements since the correction includes LSAMP2 errors.

The computed error value also allows the user to specify improvement in the comparator accuracy beyond what that described in the electrical specifications.

$$V_{OS_COMP_Effective} = \sqrt{\varepsilon_{COMP_CELLPATH}^2 + 0.004^2}$$

For example, if the DIAG1 register output reads 0x1FEC (0d7996) then the following adjustments can be applied

$$\varepsilon_{COMP_CELLPATH} = \frac{1}{13} \cdot \left(\frac{0d7996 - 0d8224}{0d16384}\right) \cdot 5V = -5.35mV$$

$$COMPOVTH_{Adjusted} = COMPOVTH_{Desired} + Round(-5.35mV x 1023 / 5)$$

$$COMPOVTH_{Adjusted} = COMPOVTH_{Desired} - 1$$

$$COMPUVTH_{Adjusted} = COMPUVTH_{Desired} + Round(-5.35mV x 1023 / 5)$$

$$COMPUVTH_{Adjusted} = COMPUVTH_{Desired} - 1$$

Comparator Accuracy Diagnostic

The COMPACCEN bit in ACQCFG register is used to test the accuracy of the comparator and is evaluated at the end of a measurement-sequence for configurations that use the comparator (SCANCFG = 001b or 010b in the SCANCTRL register) during scans. When COMPACCEN = 1, V_{REF} = 2.3077 V is configured as input to the LSAMP2 and the 10-bit DAC uses values from the COMPACCOVTH and COMPACCUVTH registers.

An overvoltage alert is issued by setting the ALRTCOMPACCOV bit in the FMEA2 register if the threshold value in COMPACCOVTH is violated.

If COMPACCOVTH is set to 1D8h, the comparator may set the ALRTCOMPACCOV bit (expected to be set for the ideal case).

An undervoltage alert is issued by setting the ALRTCOMPACCUV bit in the FMEA2 register if the threshold value in COMPACCUVTH is violated.

If COMPACCUVTH is set to 1D8h, the comparator may not set ALRTCOMPACCUV bit (not expected to be set for the ideal case).

Comparator Accuracy Diagnostic signal path is shown below in Figure 93.

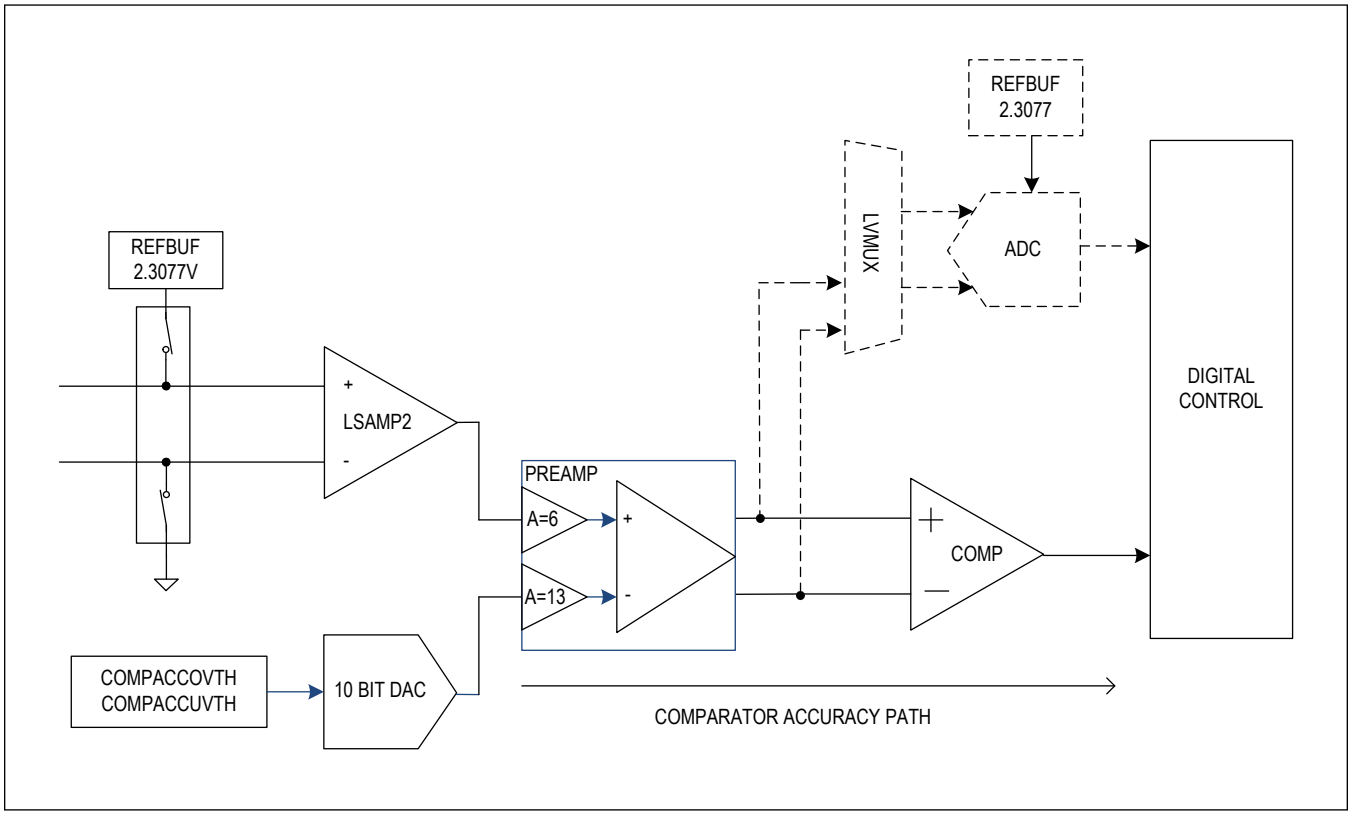


Figure 93. Comparator Accuracy Diagnostic Path

In order to eliminate false alerts, user should adjust COMPACCOVTH and COMPACCUVTH by ± 5 DAC codes.

Refer to the Comparator Signal Path Diagnostic section for details on setting these thresholds.

Comparator Accuracy Diagnostics procedure when requested by setting COMPACCEN = 1 will be run only once at the end of last over sample of SCAN measurement request as indicated in Figure 94 below.

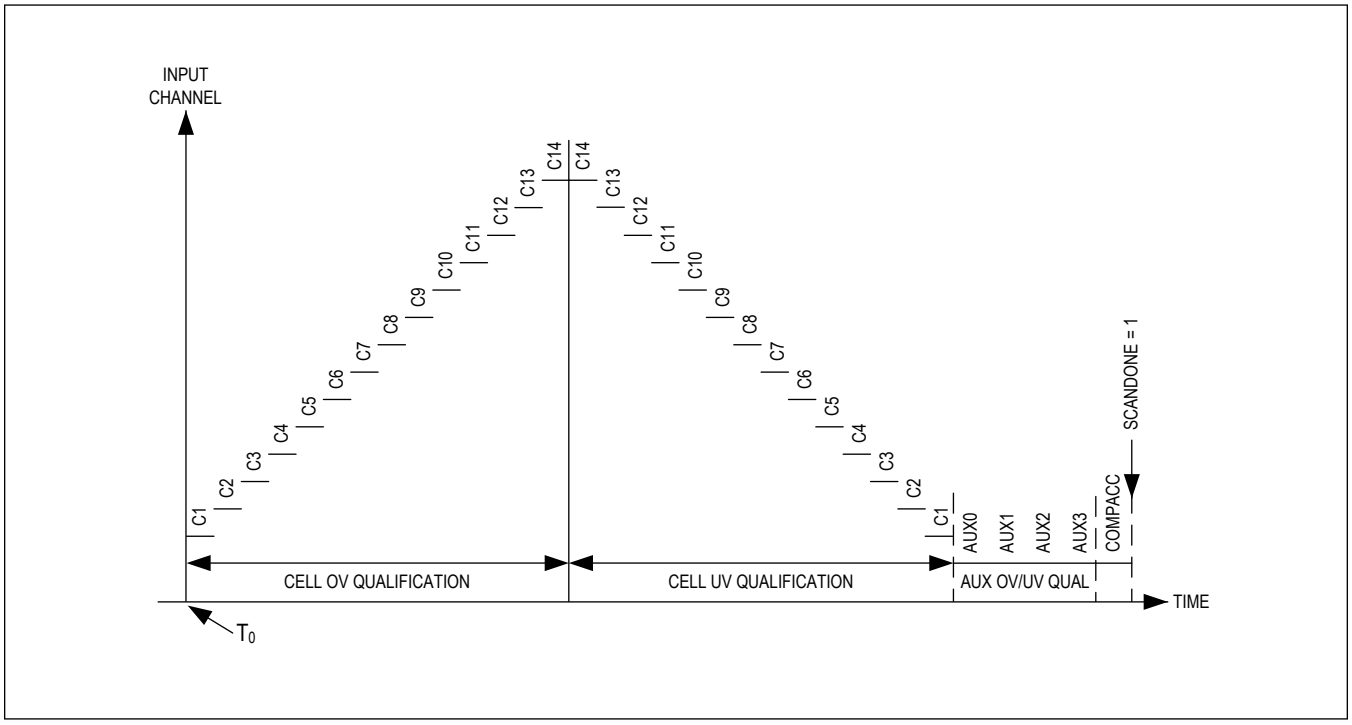


Figure 94. Comparator Accuracy End of Scan Measurement

Cell Gain Calibration Diagnostic Measurement

The cell gain-calibration diagnostic verifies that on-demand calibration is functioning correctly and the ADC and LSAMP1 are operating within the specification described by the electrical characteristics section. This diagnostic is run by setting the DIAGSEL1 = 0b0101 or DIAGSEL2 = 0b0101 in the DIAGCFG register in accordance with the SCANMODE setting. Thus, if SCANMODE is configured for Pyramid mode operation when this diagnostic is run, then the sampling will occur as two conversion phases and effectively chop the offset. Similarly, if SCANMODE is configured for Ramp mode operation when this diagnostic is run, then only a single conversion phase canmplemented. This diagnostic must be run for each of the SCANMODE configurations utilized by the application to validate calibration.

The diagnostic is performed by multiplexing V_{REF} into the LSAMP1 inputs as shown below in Figure 95. The OVSAMPL bitfield used during this diagnostic acquisition must be minimally configured to an oversample of 16 which ensures proper accuracy performance.

The expected result is 6/13 of full scale (0x1D8A) voltage and can be read from DIAG1REG [15:2] or DIAG2REG[15:2] registers. To allow for 14-bit ADC measurements should extend from 0x1D7D to 0x1D97.

Note: This diagnostic should not be run without enabling calibration.

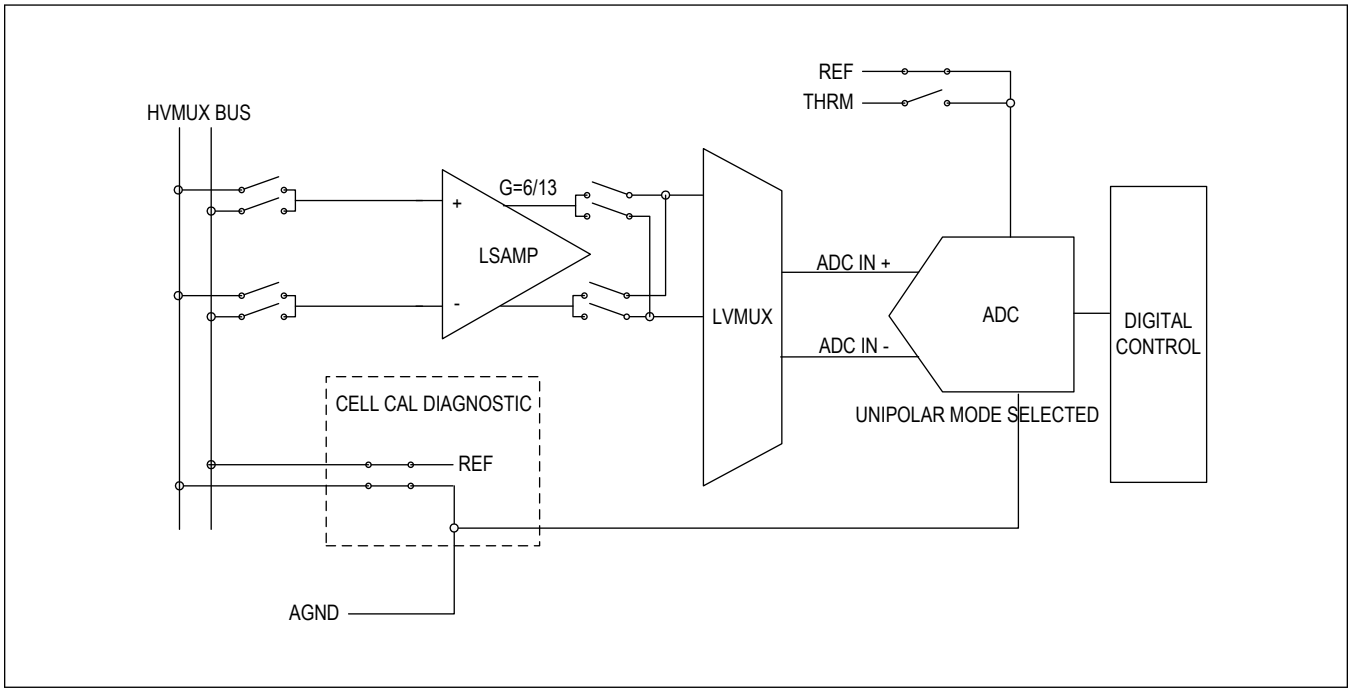


Figure 95. Cell Gain Calibration-Diagnostic Measurement

Offset Calibration Diagnostic

The offset calibration diagnostic is run by setting the DIAGSEL1 = 0b0110 or DIAGSEL2 = 0b0110 in the DIAGCFG register. This diagnostic verifies that on-demand calibration is functioning correctly and operating within the electric table specifications.

This diagnostic is configured differently depending on the SCANMODE setting in the SCANCTRL register. When configured in pyramid mode (SCANMODE = 0), the diagnostic is performed by shorting the ADC inputs and performing an acquisition with the ADC polarity overridden in bipolar mode. When configured in ramp mode (SCANMODE = 1), the diagnostic is performed by shorting the LSAMP1 inputs to ground and performing an un-chopped acquisition with the ADC polarity overridden in bipolar mode. For both SCANMODE configurations, the OVSAMPL bitfield used during this diagnostic acquisition must be minimally configured to an oversample of 16 which ensures proper accuracy performance. The expected result is 0V (0x2000) and can be read from DIAG1REG [15:2] or DIAG2REG[15:2] registers.

For pyramid mode, the 14-bit ADC measurement bound which passes this diagnostic ranges from 1FF3h to 200dh.

For ramp mode, the 14-bit ADC measurement bound which passes this diagnostic ranges from 1FEAh to 2011h.

The signal path is shown below in Figure 96.

Note: This diagnostic is should not be run without enabling calibration.

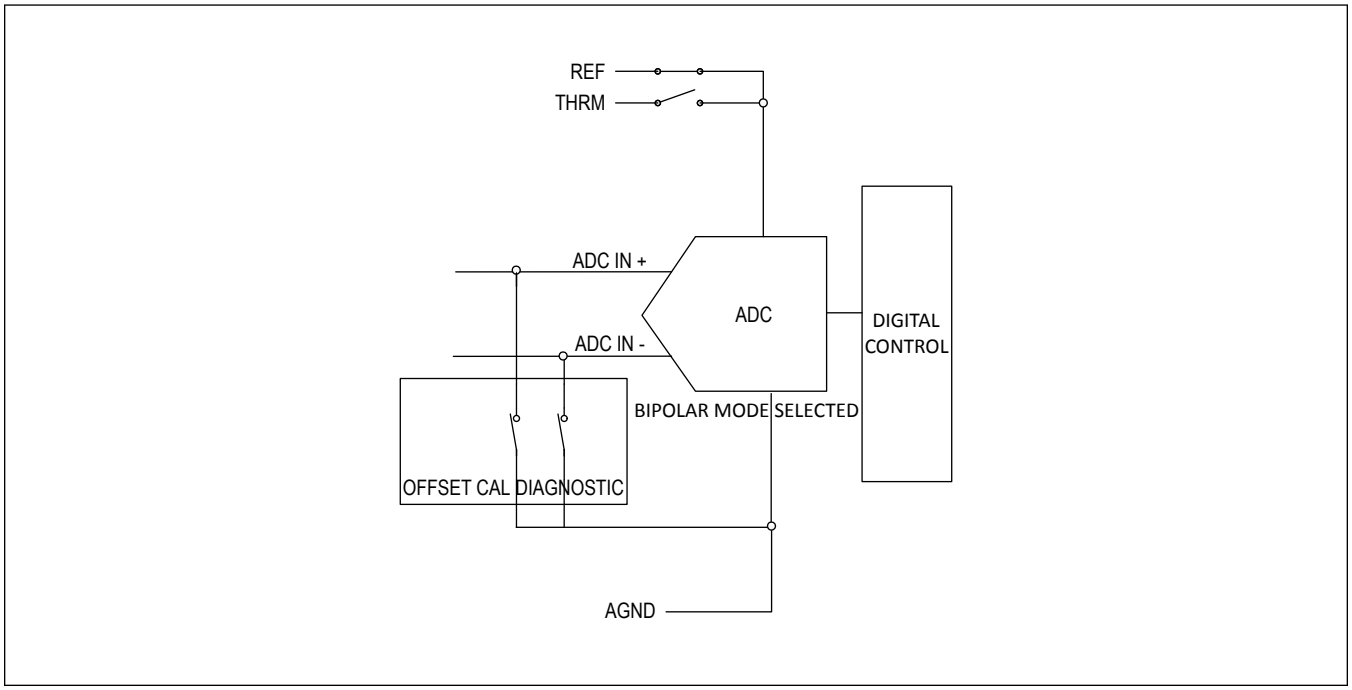


Figure 96. Offset-Calibration Diagnostic

THRM Offset Calibration Diagnostic

The THRM offset calibration diagnostic is run by setting the DIAGSEL1 = 0b1001 or DIAGSEL2 = 0b1001 in the DIAGCFG register. The diagnostic verifies that on-demand calibration for the THRM case is functioning correctly and the ADC is operating within the specification described by the electrical characteristics section. This is performed by shorting the ADC inputs to ground with ADC reference connected to THRM and performing an acquisition with recommendation of minimum 16x oversample (OVSAMPL = 0b011) in bipolar mode.If ADCCALEN = 1, appropriate calibration coefficients are applied to the diagnostic result. Signal path can be seen below in Figure 97.

The expected result is 0 V or DIAG1/2 [15:2] = 2000h, nominally.

For ADCCALEN = 1, the 14-bit ADC measurement bound which passes this diagnostic ranges from 1FF8h to 2003h.

For ADCCALEN = 0, the 14-bit ADC measurement bound which passes this diagnostic ranges from 1FB0h to 204Fh.

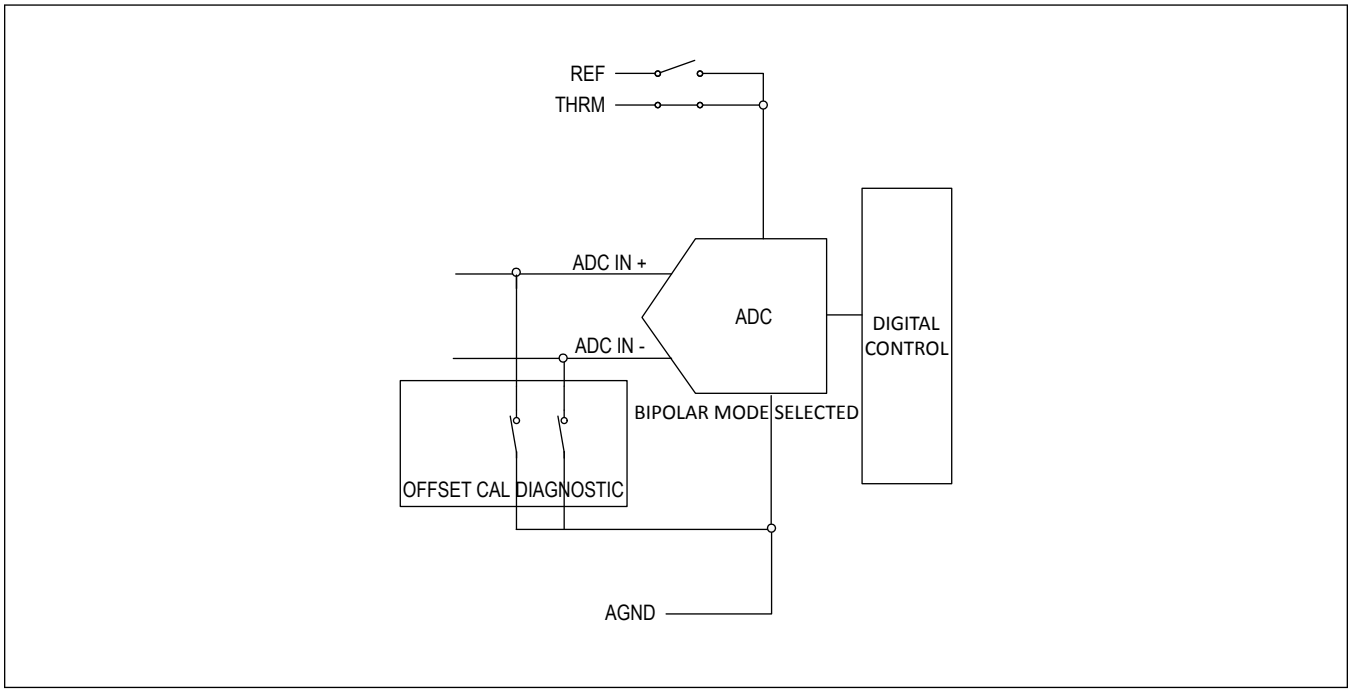


Figure 97. THRM Offset -Calibration Diagnostic

LSAMP Offset Diagnostic Measurement

The LSAMP diagnostic measurement (DIAGSEL1 or DIAGSEL2 = 0b1100) measures the level-shift amplifier offset by shorting the LSAMP inputs during the diagnostic portion of the acquisition. The result is available in the DIAG1REG or DIAG2REG registers after an acquisition. For this measurement, the ADC polarity is automatically set to bipolar mode to allow accurate measurement of voltages near zero. This measurement eliminates the chopping phase to preserve the offset error. If the diagnostic measurement exceeds the valid range for V_{OS_LSAMP} as specified in *Electrical Characteristics*, the chopping function may not be able to cancel out all of the offset error and acquisition accuracy could be degraded accordingly. Signal path for this diagnostic is shown below in Figure 98.

The LSAMP offset is computed from the result in the DIAG1 or DIAG2 as follows:

LSAMP Offset = (|DIAGn[15:2] - 2000h| / 16384d) x 5V

For ADCCALEN = 0, the 14-bit ADC measurement bound which passes this diagnostic ranges from 1D59 to 22A9h.

For ADCCALEN = 1, the 14-bit ADC measurement bound which passes this diagnostic ranges from 1D70h to 228Fh.

The validity of measurements through LSAMP is further confirmed by the ALTREF and V_{AA} diagnostics, and comparison of the VBLK measurement to the sum of the cell measurements.

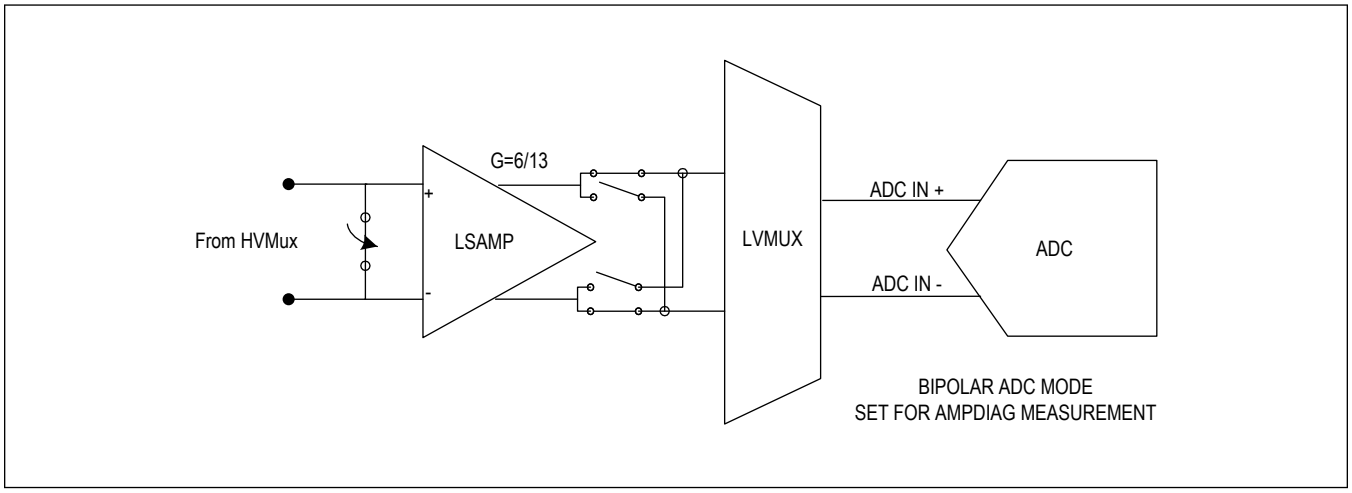


Figure 98. LSAMP Offset-Diagnostic

Zero-Scale ADC Diagnostic Measurement

Stuck ADC output bits can verified with a combination of the zero-scale and full-scale diagnostics. The zero-scale ADC diagnostic measurement (DIAGSEL1 or DIAGSEL2 = 0b1010) verifies that the ADC conversion results in 000h (12-bit) when its input is at $-V_{AA}$ in bipolar mode (since for an input ≤ -2.5V, DIAG1/2[13:0] = 0000h). For this measurement, the ADC is automatically set to bipolar mode. Signal path for this diagnostic is shown below in Figure 99

If the user desires a quick combination of ADC Zero Scale and Full Scale to detect if ADC is stuck at some value, this can be performed as part of End of Scan by configuring ADCZSFZEN = 1 and then requesting a SCAN. Refer to the acquisition timing sections for details on insertion into the scan and timing.

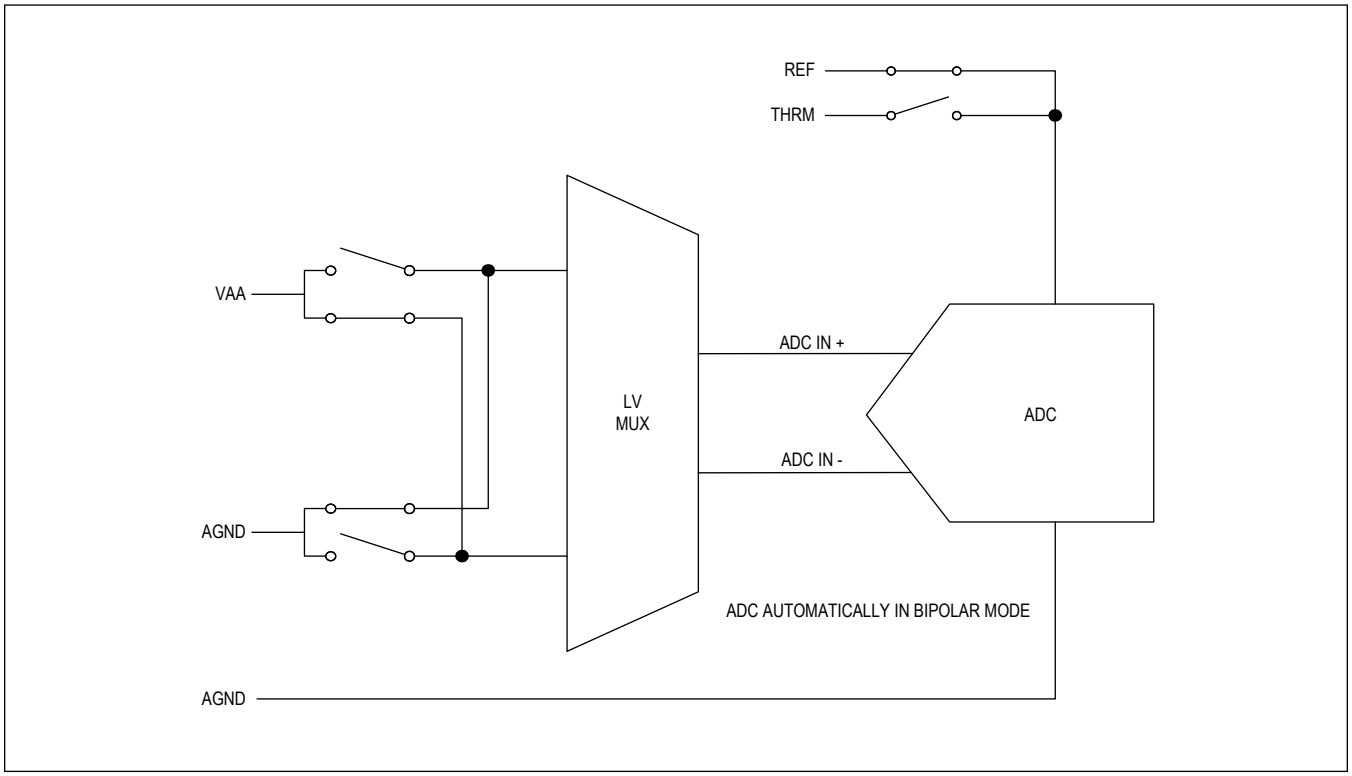


Figure 99. ADC Zero-Scale Diagnostic

Full-Scale ADC Diagnostic Measurement

Stuck ADC output bits can be verified with a combination of the zero-scale and full-scale diagnostics. The full-scale ADC diagnostic measurement (DIAGSEL1 or DIAGSEL2 = 0b1011) verifies that the ADC conversion results in FFFh (12-bit) when its input is at V_{AA} in bipolar mode (since for an input ≥ 2.5V, DIAG1/2[13:0] = 3FFCh). For this measurement, the ADC is automatically set to bipolar mode. Signal path for this diagnostic is shown below in Figure 100.

If the user desires a quick combination of ADC Zero Scale and Full Scale to detect if ADC is stuck at some value, this can be performed as part of End of Scan by configuring ADCZSFZEN = 1 and then requesting a SCAN. Refer to the acquisition timing sections for details on insertion into the scan and timing.

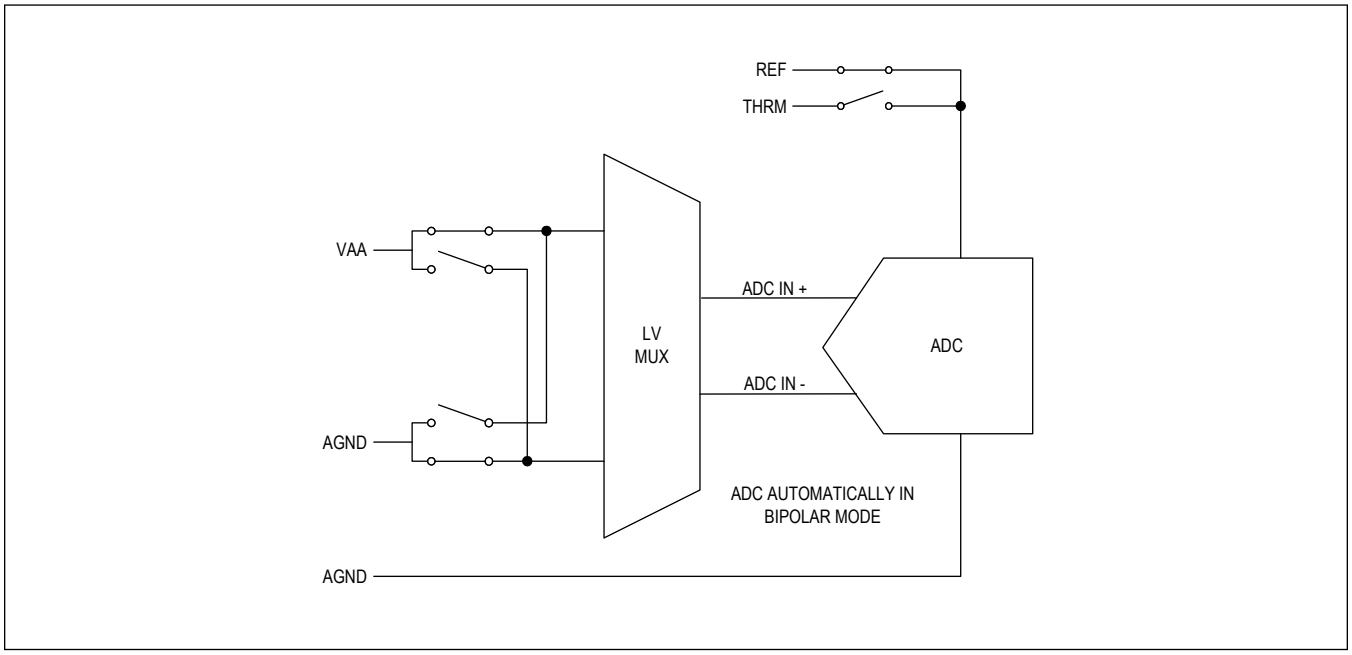


Figure 100. Full-Scale ADC Diagnostic Measurement

DAC 1/4 Scale Diagnostic

The DAC 1/4 scale diagnostic can be requested by setting DIAGSEL1 or DIAGSEL2 = 0x1000 this will configure the internal DAC used to set the comparator thresholds to 1/4 of Full Scale (V_{REF}) or 0x100. The DAC voltage is muxltiplexed to the ADC and then compared against the bounds shown below in Figure 101.

The nominal DAC and ADC voltages are

V_{DAC} = 256/1023 x 2.3077 = 0.5775V

V_{ADC} = 0.5775/2.3077 x 16384 = 4100 = 0 x 1004

For ADCCALEN = 1, the 14-bit ADC measurement bounds for passing this diagnostic ranges from 0x0FD0 to 0x1040.

For ADCCALEN = 0, the 14-bit ADC measurement bounds for passing this diagnostic ranges from 0x0FA0 to 0x1060.

This can used in coordination with the DAC 3/4 scale diagnostic to ensure that there are no stuck bits which may cause errors with the comparator threshold settings.

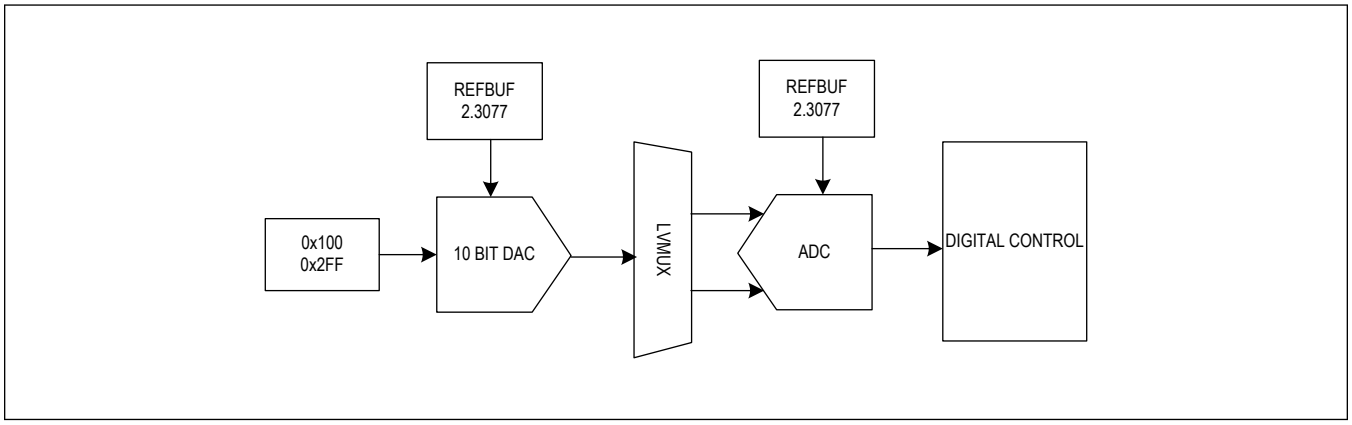


Figure 101. DAC 1/4 and 3/4 Diagnostic

DAC 3/4 Scale Diagnostic

The DAC 3/4 scale diagnostic can be requested by setting DIAGSEL1 or DIAGSEL2 = 0x0111 this will configure the internal DAC used to set the comparator thresholds to 3/4 of Full Scale (V_{REF}) or 2FFh. The DAC voltage is multiplexed to the ADC and then compared against the bounds shown below.

The nominal DAC and ADC voltages are:

V_{DAC} = 767/1023 x 2.3077 = 1.73 V

V_{ADC} = 1.73/2.3077 x 16384 = 2FFAh

For ADCCALEN = 1, the 14-bit ADC measurement bounds for passing this diagnostic range from 2F80h to 3070h.

For ADCCALEN = 0, the 14-bit ADC measurement bounds for passing this diagnostic range from 2F70h to 3080h.

This will be used in coordination with the DAC 1/4 scale diagnostic to ensure that there are no stuck bits which may cause errors with the comparator threshold settings.

BALSW Diagnostics

Four balancing switch diagnostic modes are available to facilitate the following diagnostics:

- Balancing switch shorted (SCANCFG[2:0]=0b100)
- Balancing switch open (SCANCFG[2:0] = 0b101)
- Odd sense wire open (SCANCFG[2:0] = 0b110)
- Even sense wire open (SCANCFG[2:0] = 0b111)

Enabling any of these modes automatically configures several acquisition settings (e.g. enables the ALTMUX measurement path). The host must initiate the acquisition, but the diagnostic mode automatically compares the measurements to the specific thresholds as configured through BALSHRTTHR, BALLOWTHR, or BALHIGHTHR threshold registers and sets any corresponding alerts in ALRTBALSW register field. The host presets the thresholds as determined by the minimum and maximum resistance of the switch (R_{SW}) specified in *Electrical Characteristics* and the intended cell-balancing current.

The Balance Switch Fault Alert Register (ALRTBALSW[13:0]) is cleared at the start of a new scan request if balancing switch diagnostic mode is requested (SCANCFG = 0b100, 0b101, 0b110, or 0b111). The result from the current balancing switch diagnostic is written to ALRTBALSW[13:0] at the end of scan (SCANDONE = 1). The previous result will persist in ALRTBALSW until a new scan is requested, with balancing-switch diagnostic mode enabled.

Table 72 describes which Balance Switch Diagnostic Alert Thresholds contribute to ALRTBALSW in each of the four modes.

Table 72. BALSW Diagnostic

MODE	SCANCFG[2:0]	THRESHOLD	FAULT CONDITION
Balancing Switch Short	0b100	BALSHRTTHR	Data < BALSHRTTHR
Balancing Switch Open	0b101	BALLOWTHR, BALHIGHTHR	Data < BALLOWTHR, or Data > BALHIGHTHR
Cell Sense Open Odds	0b110	BALLOWTHR, BALHIGHTHR	Data < BALLOWTHR, or Data > BALHIGHTHR
Cell Sense Open Evens	0b111	BALLOWTHR, BALHIGHTHR	Data < BALLOWTHR, or Data > BALHIGHTHR

The summary status bitfield ALRTBALSWSUM is updated at the end of scan when a balancing switch diagnostic mode is enabled. ALRTBALSWSUM is a bit-wise logical OR of ALRTBALSW[13:0].

ALRTBALSW is a bitwise alert status for all 14 channels/switches; the alert masking will depend on the TOPCELL1 and TOPCELL2 settings. The user should ensure that if TOPCELL1 != TOPCELL2 then none of the alerts are masked. If TOPCELL1 = TOPCELL2 all the alerts above TOPCELL1/2 position are masked. These conditions will apply for all the four BALSW diagnostic SCAN requests.

The balancing switch diagnostic summary status ALRTBALSWSUM can be cleared if all enabled ALRTBALSW[13:0] alerts are resolved (by subsequent scan) or by writing to logic zero.

Note: In balancing switch diagnostic mode, the ALRTOV, ALRTUV, and ALRTMSMTCH alerts are not updated because these are only applicable during normal cell measurements.

BALSW Short Diagnostic

A short-circuit fault in the balancing path could be a short between SWn and SWn-1 as shown in Figure 102 or that a balancing FET is stuck in the conducting state. In the short-circuit state, the voltage between SWn and SWn-1 (switch voltage) is less than the voltage between Cn and Cn-1 (cell voltage).

When enabled, the balancing switch short diagnostic mode (SCANCFG[2:0] = 0b100) functions as follows:

- Disables the balancing switches automatically
- Configures the acquisition using ALTMUX path automatically
- Host initiates the acquisition on selected Unipolar Cells only (~POLARITYn & CELLENn)
- Compares the measurement to the threshold value BALSHRTTHR automatically (for Unipolar Cells only, i.e. POLARITYn = 0, see Table 73)
- If outside the threshold, sets the corresponding flag in ALRTBALSW automatically

For the best sensitivity to leakage current, set the threshold value based on the minimum cell voltage minus a small noise margin (100mV), then update the threshold value periodically or every time a measurement is taken, depending on how fast the cell voltages are expected to change.

BALSW Short decision is as shown below in Table 73.

Table 73. BALSW Short Diagnostics Operation

BALSW	VSWn	FAULT INDICATED?	POSSIBLE FAULT CONDITION
Off	> $V_{BALSHRTTHR}$	No	None
	< $V_{BALSHRTTHR}$	Yes	Short Circuit or Leakage Current

An example of a BALSW short is shown below in Figure 102.

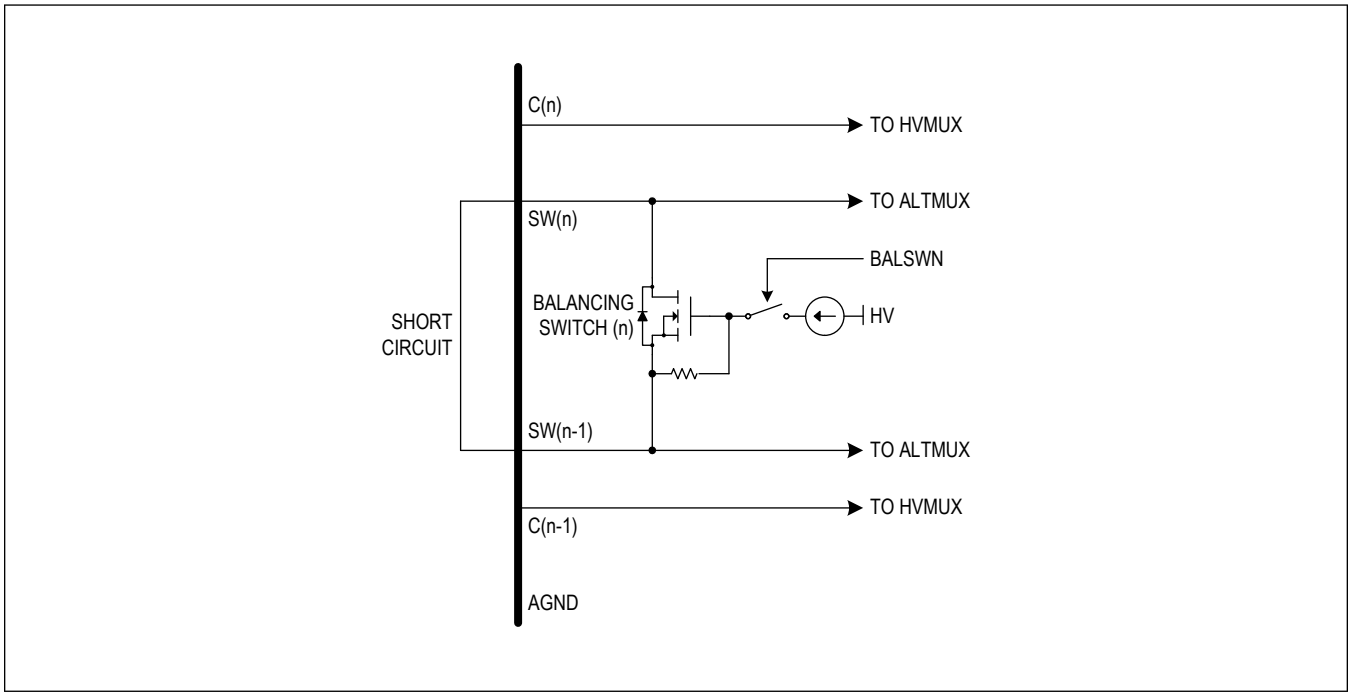


Figure 102. Balancing Switch Short

The BALSW Short Diagnostic procedural flow chart is shown in Figure 103.

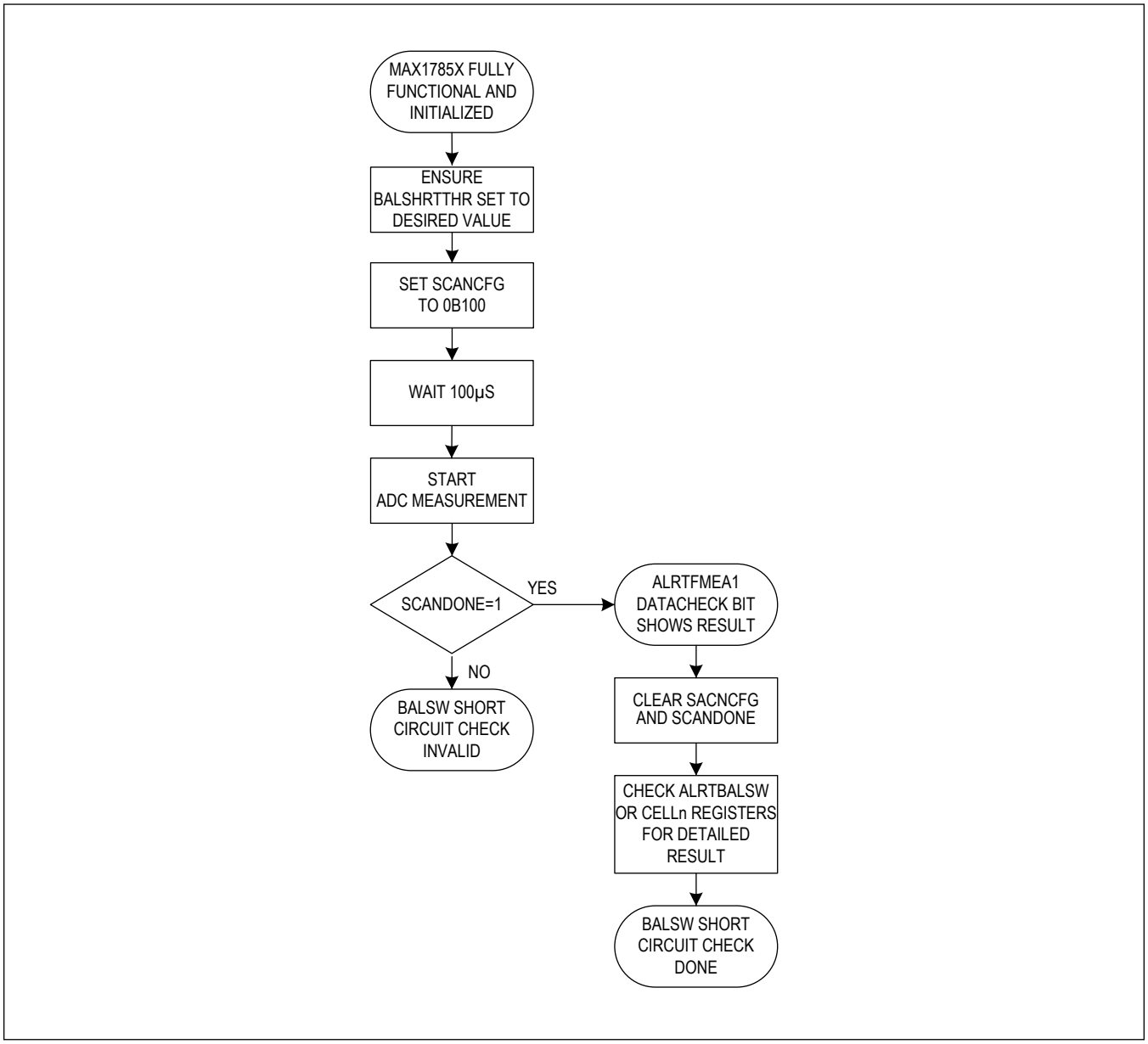


Figure 103. BALSW Short Diagnostic Chart

The BALSW Short Diagnostic automatically overrides the configuration settings during the measurements scan as shown in Table 74 below.

Table 74. BALSW Short Diagnostic Auto-Configuration

CONFIGURATION BITS	AUTOMATIC SETTING	PURPOSE
MEASUREEN1[15:14]	0b00	Disable CSA and VBLK measurements
MEASUREEN1[13:0]	(~POLARITYn & CELLENn)	Enable only selected Unipolar Cell measurements
MEASUREEN2[3:0]	0b0000	Disable AUXn measurements

Table 74. BALSW Short Diagnostic Auto-Configuration (continued)

CONFIGURATION BITS	AUTOMATIC SETTING	PURPOSE
BALSWEN[13:0]	0x0000	Disable all balancing switches
DIAGSEL1/2	0x0	Disable all diagnositics
SCANCTRL:ALTMUXSEL	1	Enable ALTMUX measurement path
SCANCTRL:OVSAMPL	0x0	Oversample rates configured to 1

BALSW Open Diagnostic

The BALSW open diagnostic (SCANCFG[2:0] = 0b101) verifies that each enabled balancing switch is conducting (not open) as follows:

- Configures acquisition for bipolar mode (for measuring voltages near zero) automatically
- Configures acquisition for ALTMUX path automatically
- Configures acquisition to measure switch voltages for those switches enabled by BALSWENn automatically on all unipolar cell positions(~POLARITYn & BALSWENn).
  - Note it is NOT necessary for the device to be in an active Manual Cell Balancing operation, only that BALSWEN be configured as desired.
- Host initiates acquisition
- Compares each measurement to the threshold value BALLOWTHR and BALHIGHTHR automatically, see Table 75
- If outside the threshold, set the corresponding flag in ALRTBALSW automatically

Set the thresholds by taking into account the minimum and maximum R_{SW} of the switch itself as specified in *Electrical Characteristics* and the balancing current for the application.

BALSW Open Diagnostics Operation decision is as shown in below Table 75.

Table 75. BALSW Open-Diagnostic Operation

BALSW	VSWn	FAULT INDICATED?	POSSIBLE FAULT CONDITION
On	> $V_{BALHIGHTHR}$	Yes	Switch Open Circuit, or Overcurrent
	> $V_{BALLOWTHR}$	No	None
	< $V_{BALHIGHTHR}$		
	< $V_{BALLOWTHR}$	Yes	Path Open Circuit or Short Circuit

The BALSW Open Diagnostic procedural flow chart is shown in Figure 104.

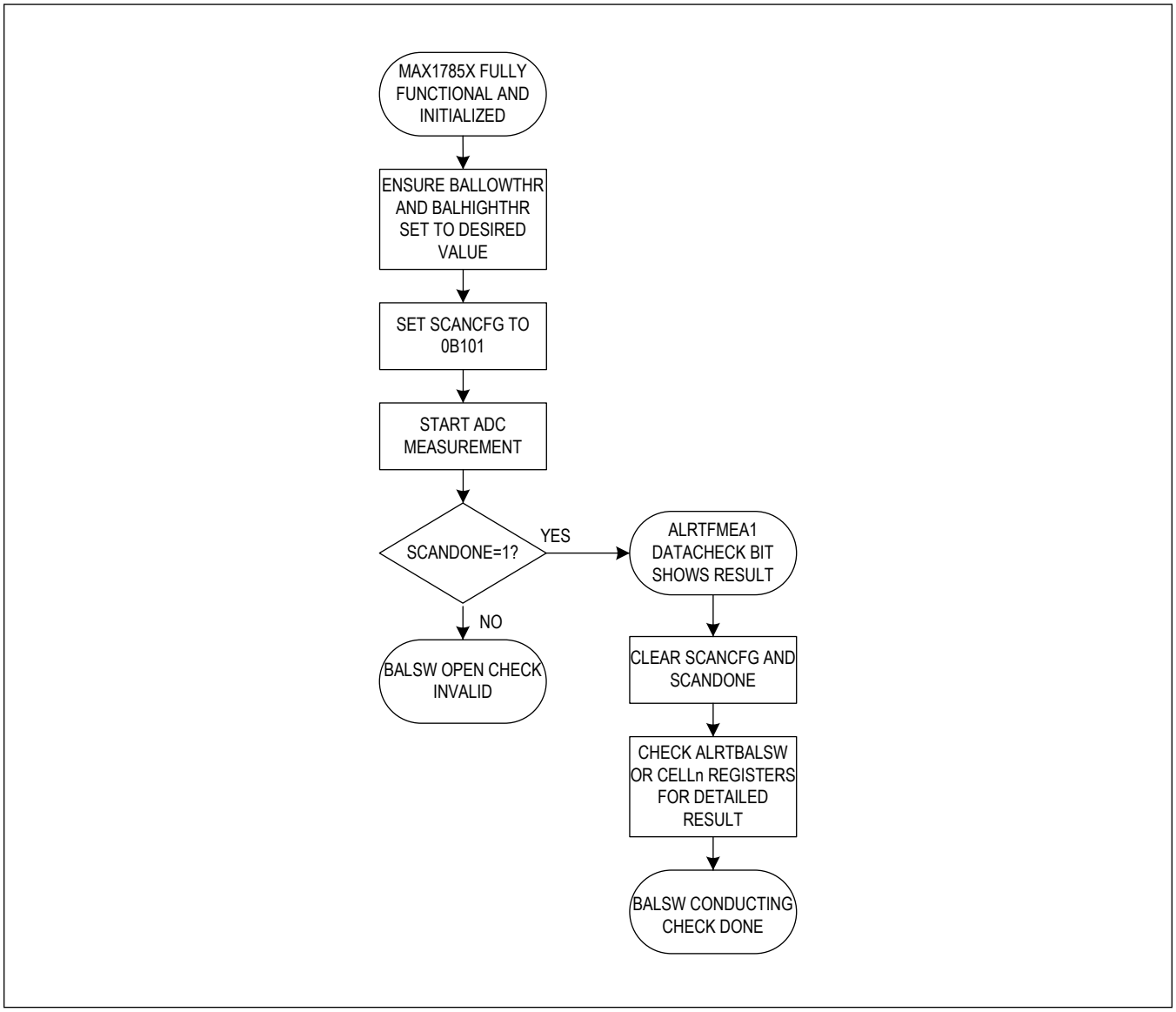


Figure 104. BALSW Open-Diagnostic

The BALSW Short Diagnostic automatically overrides the configuration settings during the measurements scan as shown in Table 76 below.

Table 76. BALSW Open-Diagnostic Auto-Configuration

CONFIGURATION BITS	AUTOMATIC SETTING	PURPOSE
MEASUREEN1[15:14]	0b00	Disable CSA and VBLK measurements
MEASUREEN1[13:0]	BALSWENn & ~POLARITYn	Measure only active unipolar switch positions
MEASUREEN2[3:0]	0b0000	Disable AUXn measurements
DIAGSEL1/2	0x0	Disable all diagnostics
SCANCTRL:ALTMUXSEL	1	Enable ALTMUX measurement path

Table 76. BALSW Open-Diagnostic Auto-Configuration (continued)

CONFIGURATION BITS	AUTOMATIC SETTING	PURPOSE
SCANCTRL:OVSAMPL	0x0	Oversample rate configured to 1

Even/Odd Sense-Wire Open Diagnostics

If enabled, the sense-wire open diagnostic modes detect if a cell-sense wire is disconnected as follows:

- Configures acquisition for bipolar mode (for measuring voltages near zero) automatically
- Closes nonadjacent switches (even or odd automatically)
- Configures acquisition to use ALTMUX path automatically
- Host waits 100µs for settling and then initiates the acquisition
- Compares the result to the BALHIGHTHR and BALLOWTHR registers automatically
- If outside thresholds, sets flags in ALRTBALSW automatically

Examples of normal and faulty operation are shown in Figure 106 through Figure 110 for examples with and without bus bars (identified by POLARITYn = 1). By examining the combined reported results from Even and Odd runs, the location and type of fault can be determined. Figure 105 shows the procedure performed by the MAX17852 during an Open Sense-Wire Diagnostic.

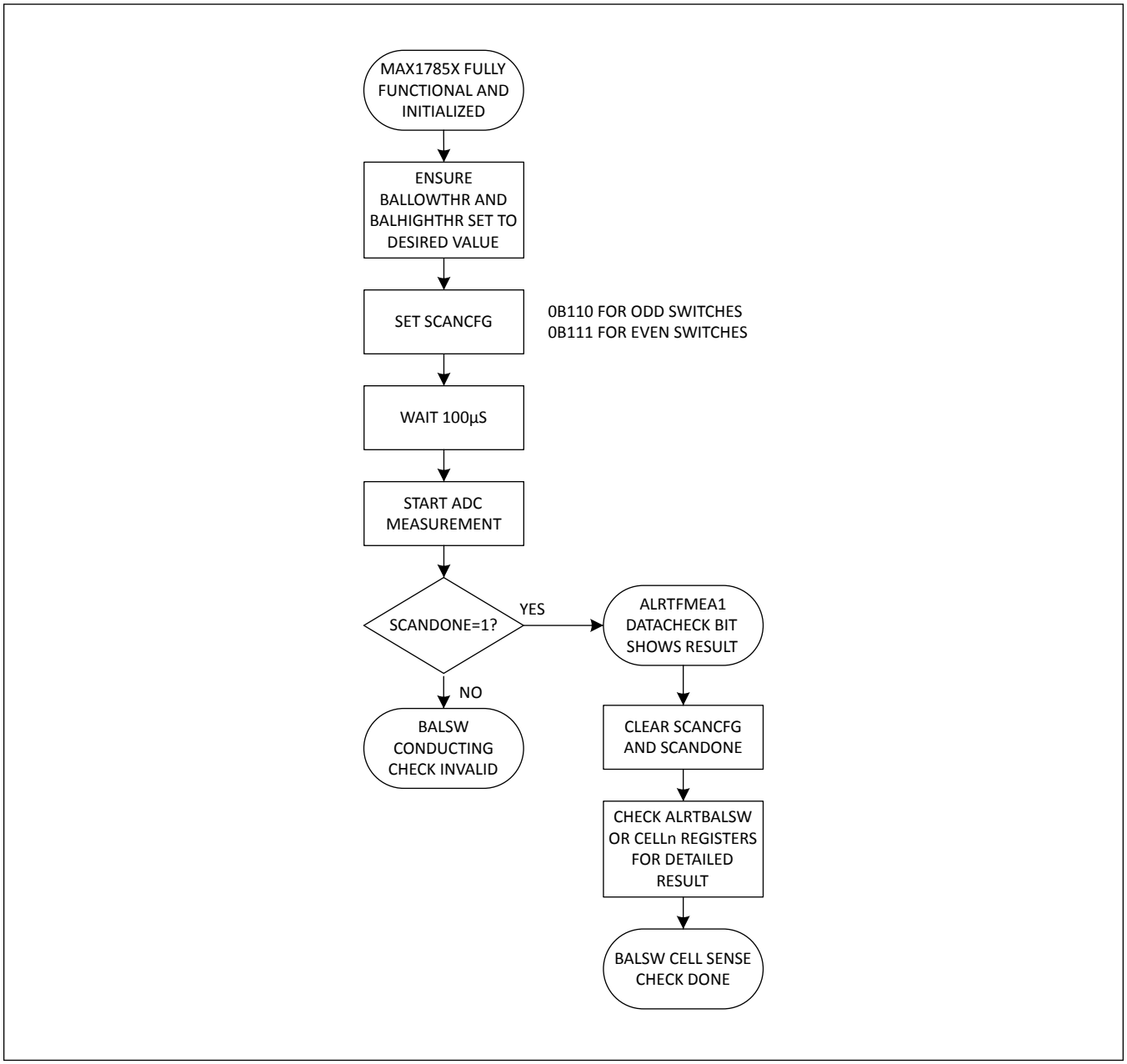


Figure 105. Sense-Wire Open-Diagnostic Flow

Table 77 shows the configuration setting overrides the MAX17852 will temporarily enforce during an Open Sense-Wire Diagnostic measurement scan.

Table 77. Sense-Wire Open-Diagnostic Automatic Configuration Overrides

CONFIGURATION BIT(S)	CONFIGURATION STATE	TASK
BALSWEN[13:0]	1555h (SCANCFG[2:0] = 0b110) or 2AAAh (SCANCFG[2:0] = 0b111)	Enable odd switches Enable even switches Switch positions with POLARITYn = 1 (bipolar/bus bar) and those above TOPCELL are masked/disabled.
MEASUREEN1[15:14]	0b00	Disable CSA and VBLK measurements
MEASUREEN1[13:0]	BALSWENn & ~POLARITYn)	BALSWEN[13:0] is set as per automatic overrides shown above. Measure only active switch positions per automatic BALSWEN overrides and unipolar positions.
MEASUREEN2[3:0]	0b0000	Disable AUXn measurements
DIAGSEL1/2	0x0	Disable all diagnostics
SCANCTRL:ALTMUXSEL	1	Enable ALTMUX measurement path
SCANCTRL:OVSAMPL	0x0	Oversample configured to 1

These overrides are only active during the scan, normal configured operation is restored at the end of the scan.

Examples of Normal Sense-Wire Operation

Figure 106 shows the electrical behavior during both Odd and Even Sense-Wire Open-Diagnostics when no sense wires are open or compromised.

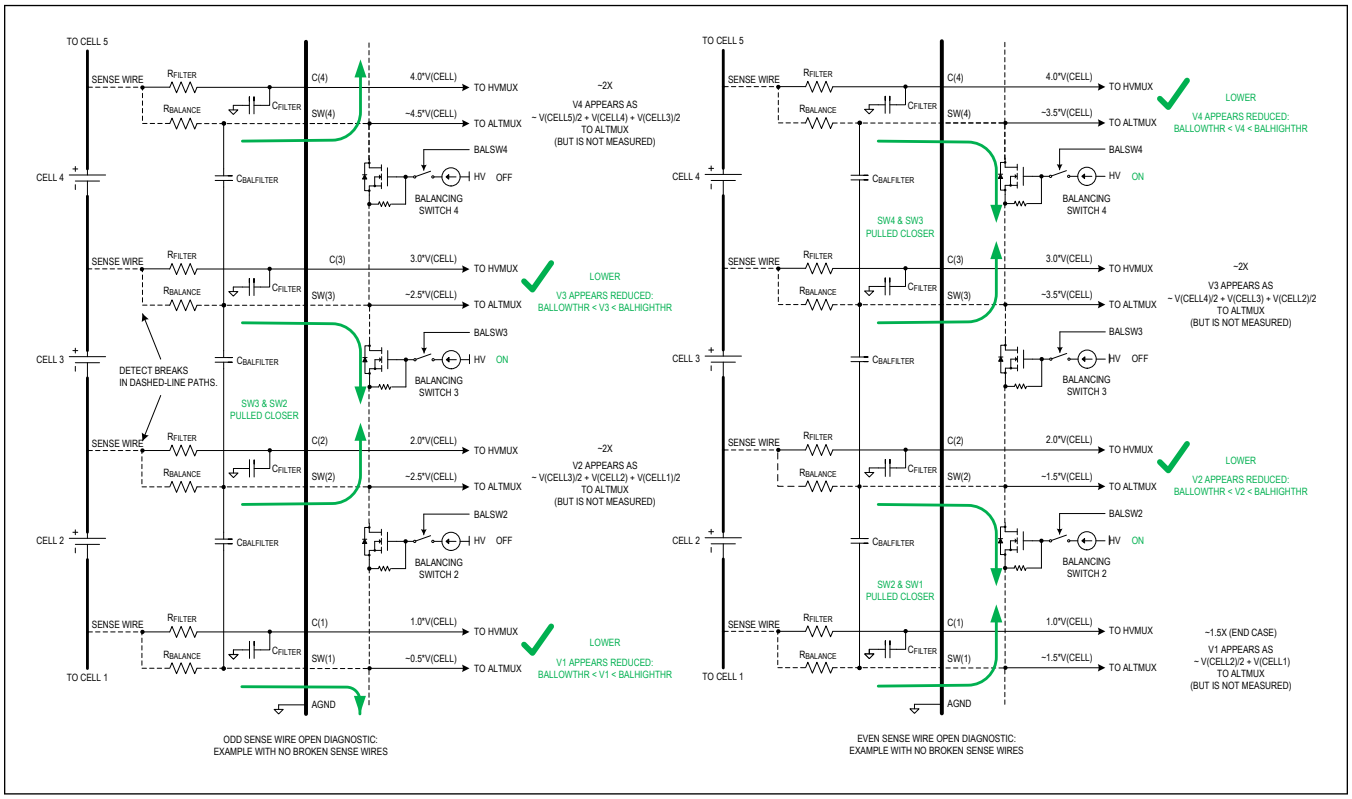


Figure 106. Cell Sense-Wire Open-Diagnostic Operations - (Normal Operation)

Figure 107 shows the electrical behavior during both Odd and Even Sense-Wire Open-Diagnostics when no sense wires are open or compromised, with bus bars included.

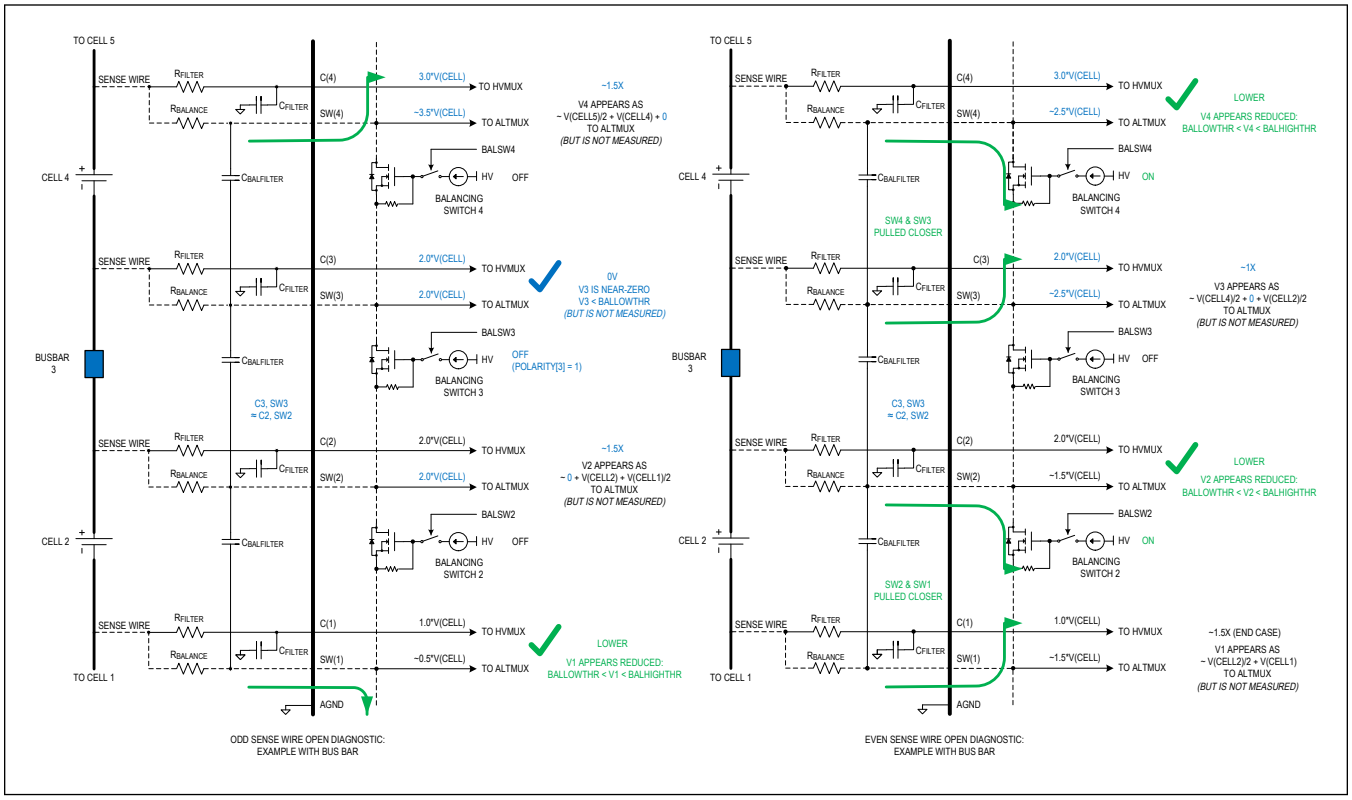


Figure 107. Cell Sense-Wire Open-Diagnostic Operations - (Normal Operation, Including Bus Bars)

Examples of Broken-Sense-Wire Fault Detection

Figure 108, Figure 109, Table 78, and Table 80 show examples of how broken sense wires are detected and diagnosed using combinations of Odd and Even Sense-Wire Open Diagnostics.

Figure 108 shows the electrical behavior during both Odd and Even Sense-Wire Open-Diagnostic sequences when a sense wire in an odd position is broken. The alerts that will be issued as a result of the fault are also shown.

Figure 109 shows the electrical behavior during both Odd and Even Sense-Wire Open-Diagnostic sequences when a sense wire in an even position is broken. The alerts that will be issued as a result of the fault are also shown.

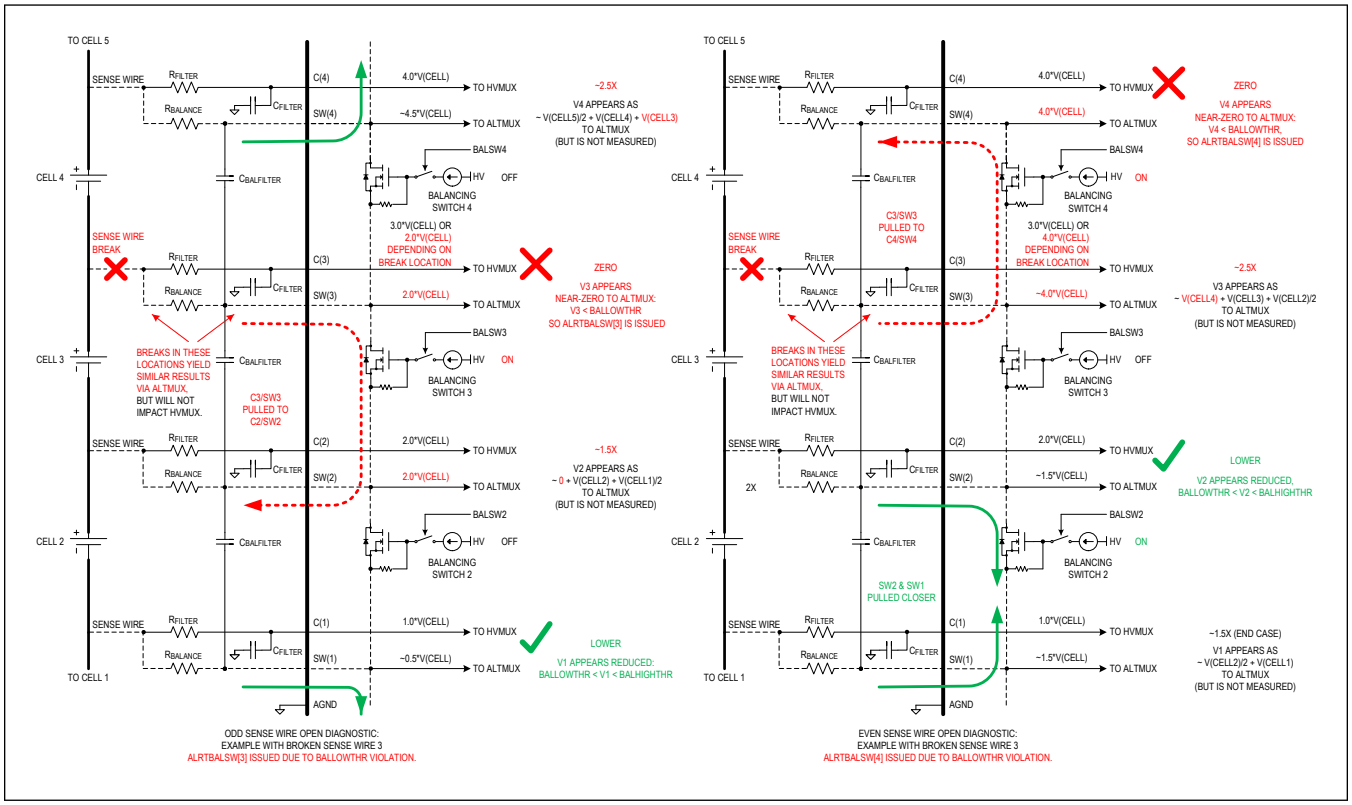


Figure 108. Cell Sense-Wire Open-Diagnostic Operations - Example with Odd Sense-Wire Fault

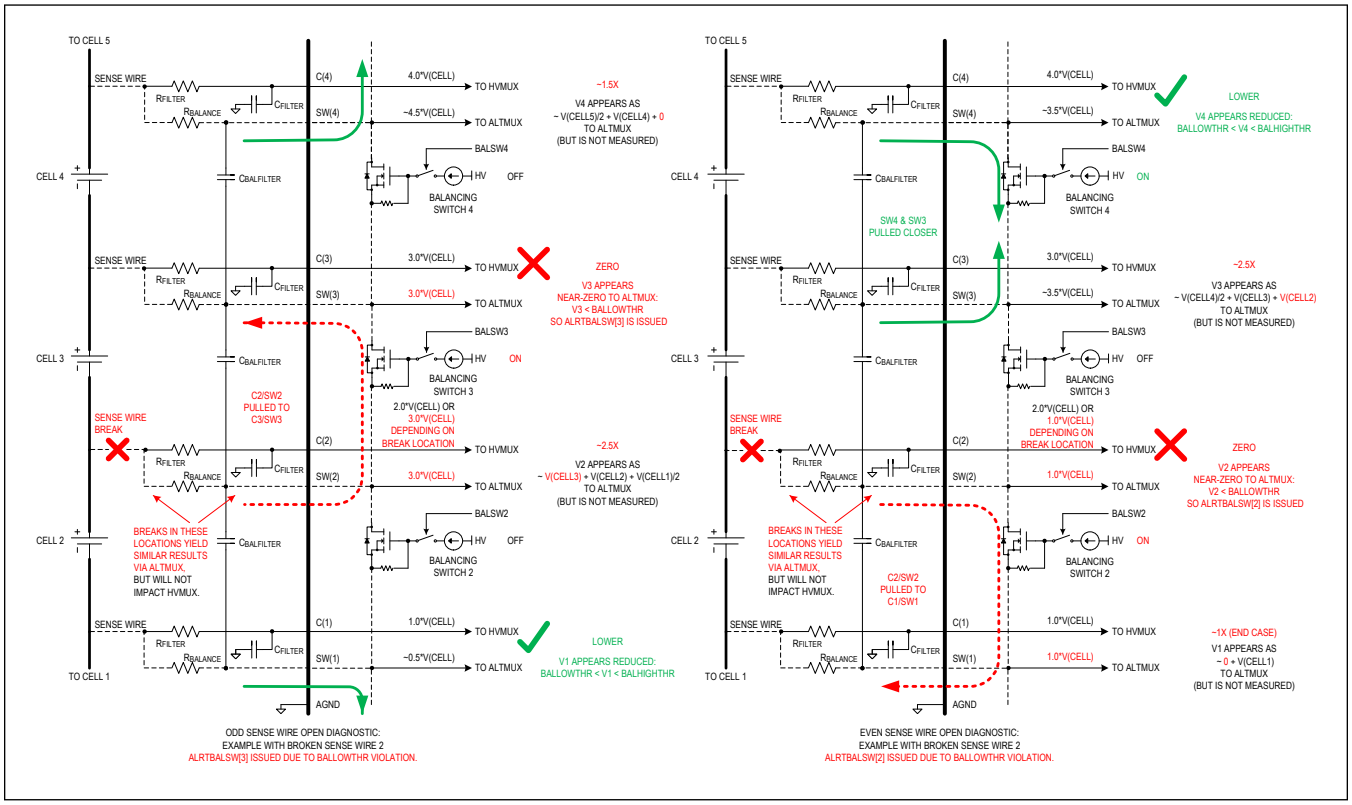


Figure 109. Cell Sense-Wire Open-Diagnostic Operations - Example with Even Sense-Wire Fault

Sense Wire Open Fault Detection Results

Table 78 shows the measurement alerts that correspond to a break in each sense-wire position during an Odd Sense-Wire Open Diagnostic. When combined with the results from an Even Sense-Wire Open Diagnostic, the exact location of the Sense-Wire fault can be determined.

Table 78. Odd Sense-Wire Open-Measurement Results for Broken Sense Wires

		SENSE-WIRE OPEN-FAULT LOCATION														
		SW0	**SW1**	**SW2**	**SW3**	**SW4**	**SW5**	**SW6**	**SW7**	**SW8**	**SW9**	**SW10**	**SW11**	**SW12**	**SW13**	**SW14**
Cell Measurement	**Cell1**	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell2	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell3	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell4	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell5	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell6	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell7	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK
	Cell8	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell9	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK
	Cell10	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell11	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK

Table 78. Odd Sense-Wire Open-Measurement Results for Broken Sense Wires (continued)

	Cell12	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell13	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK
	Cell14	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM

Note: OK = No error detected; LO = BALLOWTHR violation; NM = Not measured; Maximum result is 2.5V

Table 79 shows the measurement alerts that correspond to a break in each sense wire position during an Even Sense-Wire Open Diagnostic. When combined with the results from an Odd Sense-Wire Open Diagnostic, the exact location of the Sense-Wire fault can be determined.

Table 79. Even Sense-Wire Open-Measurement Results for Broken Sense Wires

		SENSE-WIRE OPEN-FAULT LOCATION														
		SW0	**SW1**	**SW2**	**SW3**	**SW4**	**SW5**	**SW6**	**SW7**	**SW8**	**SW9**	**SW10**	**SW11**	**SW12**	**SW13**	**SW14**
Cell Measurement	**Cell1**	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell2	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell3	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell4	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell5	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell6	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK
	Cell7	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell8	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK
	Cell9	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell10	OK	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK
	Cell11	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell12	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK
	Cell13	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM
	Cell14	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**

Note: OK = No error detected; LO = BALLOWTHR Violation; NM = Not Measured; Maximum result is 2.5V

When combined together, the two diagnostics can identify the exact location of a broken sense-wire. The combined diagnostic results are shown in Table 80.

Table 80. Odd and Even Sense-Wire Open-Measurement Results Overlay for Broken Sense Wires

		SENSE-WIRE OPEN-FAULT LOCATION														
		SW0	**SW1**	**SW2**	**SW3**	**SW4**	**SW5**	**SW6**	**SW7**	**SW8**	**SW9**	**SW10**	**SW11**	**SW12**	**SW13**	**SW14**
Cell Measurement	**Cell1**	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell2	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell3	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell4	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell5	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell6	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK	OK
	Cell7	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK	OK
	Cell8	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK	OK

Table 80. Odd and Even Sense-Wire Open-Measurement Results Overlay for Broken Sense Wires (continued)

	Cell9	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK	OK
	Cell10	OK	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK	OK
	Cell11	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK	OK
	Cell12	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK	OK
	Cell13	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**	OK
	Cell14	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	**LO**	**LO**

Note: OK = No error detected; LO = BALLOWTHR violation; maximum result is 2.5V

Examples of Broken Internal Switch/Trace Fault Detection

Figure 110 and Table 80 show examples of how broken sense wires are detected and diagnosed using combinations of Odd and Even Sense-Wire Open Diagnostics.

Figure 110 shows the electrical behavior during both Odd and Even Sense-Wire Open-Diagnostic sequences when there is a fault in an internal switch or connection. The alerts that will be issued as a result of the fault are also shown.

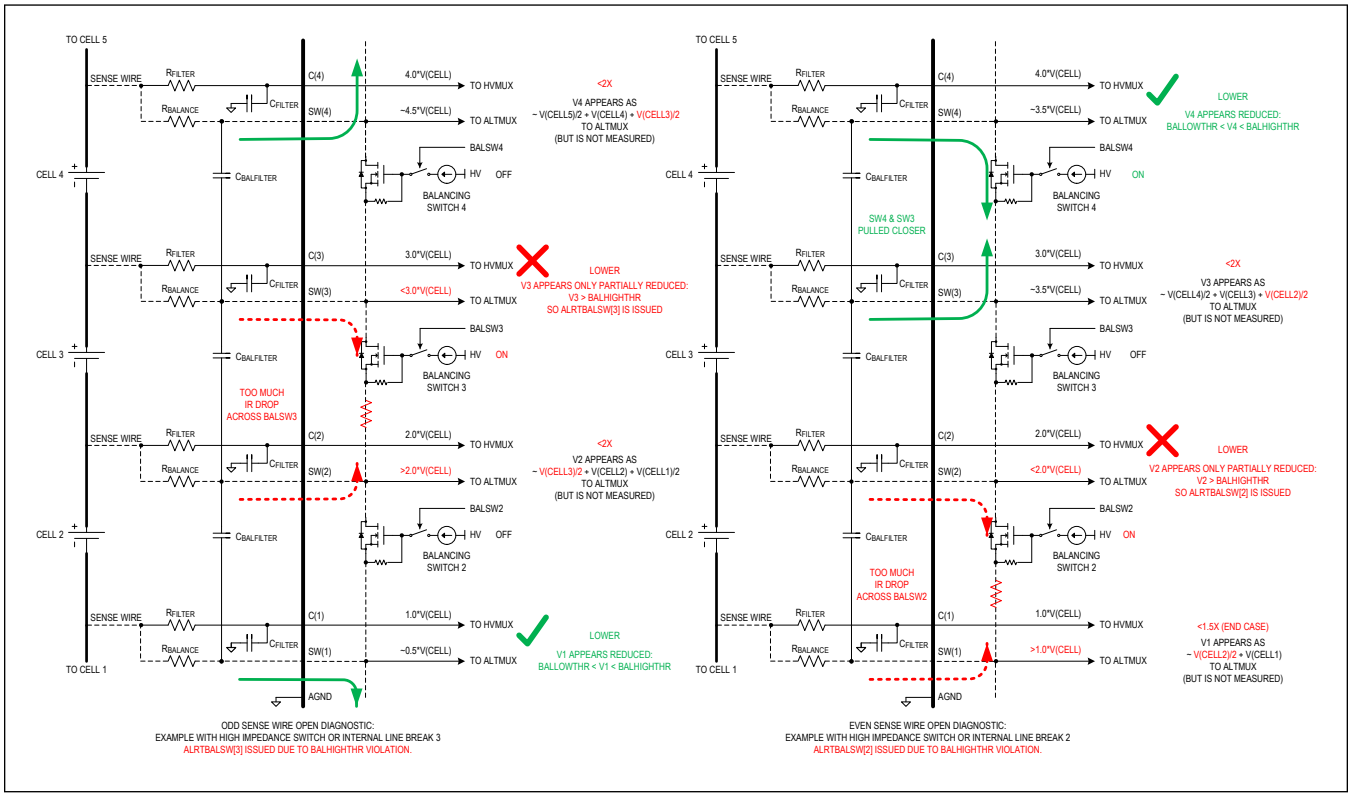


Figure 110. Cell Sense-Wire Open-Diagnostic Operations - Example with Broken BALSW or Internal Trace

Broken Switch Fault-Detection Results

When combined together, the two diagnostics can cover and identify the exact location of a faulty switch or internal trace. The combined diagnostic results are shown in Table 80. Notice that unlike a broken sense wire, only a single ALRTBALSW alert is issued for faults of this type.

Table 81. Odd and Even Sense-Wire Open-Measurement Results Overlay for Broken Sense Wires

		SWITCH OR TRACE FAULT LOCATION (BALSW)													
		1	2	3	4	5	6	7	8	9	10	11	12	13	14
Cell Measurement	Cell1	HI	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell2	OK	HI	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell3	OK	OK	HI	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell4	OK	OK	OK	HI	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell5	OK	OK	OK	OK	HI	OK	OK	OK	OK	OK	OK	OK	OK	OK
	Cell6	OK	OK	OK	OK	OK	HI	OK	OK	OK	OK	OK	OK	OK	OK
	Cell7	OK	OK	OK	OK	OK	OK	HI	OK	OK	OK	OK	OK	OK	OK
	Cell8	OK	OK	OK	OK	OK	OK	OK	HI	OK	OK	OK	OK	OK	OK
	Cell9	OK	OK	OK	OK	OK	OK	OK	OK	HI	OK	OK	OK	OK	OK
	Cell10	OK	OK	OK	OK	OK	OK	OK	OK	OK	HI	OK	OK	OK	OK
	Cell11	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	HI	OK	OK	OK
	Cell12	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	HI	OK	OK
	Cell13	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	HI	OK
	Cell14	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	HI

Note: OK = No error detected; HI = BALHIGHTHR violation; maximum result is 2.5V

ADC End Of Scan Diagnostics

This diagnostic is performed at the end of a measurement sequence that is configured to use the ADC (SCANCFG = 0b000 or 0b001) when ADCZSFSEN = 1. The ADC measurements are taken in bipolar mode.

For full-scale diagnostic: $ADC_{REF} = V_{REF}$ and $ADC_{IN} = V_{AA}$.

If the result from the ADC is less than FFFh (12-bit result), an alert is issued by setting the ALRTADCFS bit in the FMEA2 register.

For zero-scale diagnostic: $ADC_{REF} = V_{REF}$ and $ADC_{IN} = -V_{AA}$

If the result from the ADC is greater than 000h, an alert is issued by setting the ALRTADCZS bit in the FMEA2 register.

The DIAGSEL1 and DIAGSEL2 registers can be configured to obtain further diagnostic information regarding the ADC.

Register Map

MAX17852 User Register Map

Register Map Usage Guidelines

The Register Map (RMap) for the MAX17852 is detailed in the section below. General usage guidelines pertaining to the entire RMap are outlined here, detailing the expected usage of the RMap, including how various protocol and access issues are handled.

Interface Protocol Errors

In order for read and write transactions to be accepted, all interface protocol expectations must be met. If a Protocol Error occurs, these will be reported via alerts in the STATUS1 and STATUS2 registers, notifying the user of the issue observed. If a Protocol Error occurs, none of the behaviors listed below will apply, because the transaction will be rejected, even if the transaction addresses a Reserved Register address. See the UART and SPI Interface descriptions for complete details on expected interface protocols.

Reserved Registers

All User Accessible Registers are contained in the address space 0x00 to 0x98. Any address/register in this space not specifically listed in the RMap should be treated as Reserved; for the MAX17852, the following addresses within the user address space are reserved: 0x5D and 0x5E. The address space 0x99 to 0xFF is also Reserved for Maxim Use Only.

If an otherwise valid attempt to read or write to a Reserved Register address occurs (with no Protocol or CRC/PEC Errors), no errors will be issued for the SPI/UART transaction. No data written to a Reserved Register address will be internally stored, and Reserved Registers will always read back all zeros. If a UART Block Read Back request includes any Reserved Register addresses, these addresses will be included in the read back data, with all zeros returned; no addresses will be skipped during UART Block Read Back transactions. Users should normally avoid writing to Reserved Registers, as the MAX17852 will not respond to such transactions.

Unused Bitfields

Within the User Accessible Registers, there are many Unused Bitfields, denoted by a dash (-) in the RMap. During read and write transactions, PEC and CRC checks will apply to all 16 bits of data, including any Unused Bitfields. No data written to an Unused Bitfield will be internally stored, and Unused Bitfields will always read back all zeros.

Reserved Bitfields

Within the RMap, there are two Reserved Bitfields: DEVCFG1RSRV (1 bit) and DEVCFG2RSRV (4 bits); these are reserved for future use. During read and write transactions, PEC and CRC checks will apply to all 16 bits of data, including any Reserved Bitfields. Data written to a Reserved Bitfield will be internally stored (though the settings of these bitfields will have no effect on internal operations), and the Reserved Bitfields will always read back their current settings.

Register Blocks and Transaction Reject Behavior

The RMap is organized into several Register Blocks. Each Register Block is subject to specific transaction rejection behaviors as detailed in the Register Block descriptions which follow. These behaviors ensure that register content currently in use by any requested internal process is not subject to alteration while in use. In general, the Register Blocks are organized and defined to provide maximum transaction efficiency while also ensuring the ultimate level of safety.

If a valid write transaction to a blocked (busy) register occurs, the transaction will be rejected, and the ALRTRJCT bit will be set, indicating the write was ignored since that register was currently being used by an ongoing internal operation. In general, user software should be written to avoid modifying register content that is currently in use, instead confirming that the internal process has completed before any modifications are written to the MAX17852.

ADDRESS	NAME	MSB							LSB
STATUS Registers									
0x00	VERSION[15:8]	MOD[11:4]							
	VERSION[7:0]	MOD[3:0]				VER[3:0]			
0x01	ADDRESS[15:8]	ADDRUNLOCK	BA[4:0]					TA[4:3]	
	ADDRESS[7:0]	TA[2:0]			DA[4:0]				
0x02	STATUS1[15:8]	ALRTSCAN	ALRTRST	ALRTMSMTCH	ALRTCELLOVST	ALRTCELLUVST	ALRTBLKOVST	ALRTBLKUVST	ALRTAUXOVST
	STATUS1[7:0]	ALRTAUXUVST	ALRTCSAST	ALRTPEC	ALRTINTRFC	ALRTCAL	ALRTCBAL	ALRTFMEA2	ALRTFMEA1
0x03	STATUS2[15:8]	ALRTPECUP	ALRTPECDN	ALRTMANUP	ALRTMANDN	ALRTPARUP	ALRTPARDN	ALRTDUALUART	–
	STATUS2[7:0]	ALRTSPI	ALRTSCLKERR	ALRTOSC3	ALRTINTBUS	–	ALRTI2C	–	ALRTRJCT
0x04	STATUS3[15:8]	ALRTCBTIMEOUT	ALRTCBTEMP	ALRTCBCAL	ALRTCBNTFY	ALRTCBDONE	–	–	–
	STATUS3[7:0]	–	–	–	–	–	–	–	–
0x05	FMEA1[15:8]	ALRTOSC1	ALRTOSC2	ALRTCOMMSEU1	ALRTCOMMSEL1	ALRTCOMMSEU2	ALRTCOMMSEL2	ALRTVDDL3	ALRTVDDL2
	FMEA1[7:0]	ALRTVDDL1	ALRTGNDL3	ALRTGNDL2	ALRTGNDL1	ALRTHVUV	ALRTHVHDRM	ALRTHVOV	ALRTBALSWSUM
0x06	FMEA2[15:8]	ALRTUSER	ALRTDCINMUX	ALRTAUXPRTCTSUM	ALRTTEMP	ALRTSCANTIMEOUT	–	–	–
	FMEA2[7:0]	–	–	–	–	ALRTADCZS	ALRTADCFS	ALRTCOMPACCOV	ALRTCOMPACCUV
0x07	ALRTSUM[15:8]	ALRTADCOVST	ALRTCOMPOVST	ALRTADCUVST	ALRTCOMPUVST	ALRTADCAUXOVST	ALRTCOMPAUXOVST	ALRTADCAUXUVST	ALRTCOMPAUXUVST
	ALRTSUM[7:0]	ALRTCSAOV	ALRTCSAUV	–	ALRTCALOSADC	ALRTCALOSR	ALRTCALOSTHRM	ALRTCALGAINP	ALRTCALGAINR
0x08	ALRTOVCELL[15:8]	–	–	ALRTOV[14:9]					
	ALRTOVCELL[7:0]	ALRTOV[8:1]							
0x09	ALRTUVCELL[15:8]	–	–	ALRTUV[14:9]					
	ALRTUVCELL[7:0]	ALRTUV[8:1]							
0x0A	MINMAXCELL[15:8]	–	–	–	–	MAXCELL[3:0]			
	MINMAXCELL[7:0]	–	–	–	–	MINCELL[3:0]			
0x0B	ALRTAUXPRTCTREG[15:8]	–	–	–	–	–	–	–	–
	ALRTAUXPRTCTREG[7:0]	–	–	–	–	ALRTAUXPRTCT[3:0]			
0x0C	ALRTAUXOVREG[15:8]	–	–	–	–	–	–	–	–

ADDRESS	NAME	MSB							LSB
	ALRTAUXOVREG[7:0]	–	–	–	–	ALRTAUXOV[3:0]			
0x0D	ALRTAUXUVREG[15:8]	–	–	–	–	–	–	–	–
	ALRTAUXUVREG[7:0]	–	–	–	–	ALRTAUXUV[3:0]			
0x0E	ALRTCOMPOVREG[15:8]	–	–	ALRTCOMPOV[14:9]					
	ALRTCOMPOVREG[7:0]	ALRTCOMPOV[8:1]							
0x0F	ALRTCOMPUVREG[15:8]	–	–	ALRTCOMPUV[14:9]					
	ALRTCOMPUVREG[7:0]	ALRTCOMPUV[8:1]							
0x10	ALRTCOMPAUXOVREG[15:8]	–	–	–	–	–	–	–	–
	ALRTCOMPAUXOVREG[7:0]	–	–	–	–	ALRTCOMPAUXOV[3:0]			
0x11	ALRTCOMPAUXUVREG[15:8]	–	–	–	–	–	–	–	–
	ALRTCOMPAUXUVREG[7:0]	–	–	–	–	ALRTCOMPAUXUV[3:0]			
0x12	ALRTBALSWREG[15:8]	–	–	ALRTBALSW[13:8]					
	ALRTBALSWREG[7:0]	ALRTBALSW[7:0]							
0x13	SWACTION[15:8]	–	–	–	–	–	–	–	–
	SWACTION[7:0]	–	–	–	–	–	–	–	SWPOR
GENERAL CONFIGURATION Registers									
0x14	DEVCFG1[15:8]	UARTCFG[1:0]		TXUIDLEHIZ	TXLIDLEHIZ	ADAPTTXEN[1:0]		ALIVECNTEN	UARTHOST
	DEVCFG1[7:0]	SFTYCSB	SFTYSCLK	SFTYSDI	SPIDRVINT	DEVCFG1RSRV	NOPEC	ALERTEN	DBLBUFEN
0x15	DEVCFG2[15:8]	IIRFC[2:0]			–	DEVCFG2RSRV[3:0]			
	DEVCFG2[7:0]	–	HVCPDIS	FORCEPOR	ALERTDCTSTEN	–	SPITODIS	SCANTODIS	CBTODIS
0x16	AUXGPIOCFG[15:8]	I2CEN	–	–	–	GPIOEN[3:0]			
	AUXGPIOCFG[7:0]	–	–	–	–	GPIODIR[3:0]			
0x17	GPIOCFG[15:8]	–	–	–	–	GPIODRV[3:0]			
	GPIOCFG[7:0]	–	–	–	–	GPIORD[3:0]			
0x18	PACKCFG[15:8]	FLXPCKEN2	FLXPCKEN1	FLXPCKSCAN	–	TOPBLOCK[3:0]			
	PACKCFG[7:0]	TOPCELL2[3:0]				TOPCELL1[3:0]			
ALERT CONFIGURATION Registers									
0x19	ALRTIRQEN[15:8]	SCANALRTEN	–	MSMTCHALRTEN	CELLOVSTALRTEN	CELLUVSTALRTEN	BLKOVSTALRTEN	BLKUVSTALRTEN	AUXOVSTALRTEN
	ALRTIRQEN[7:0]	AUXUVSTALRTEN	CSASTALRTEN	PECALRTEN	INTRFCALRTEN	CALALRTEN	CBALALRTEN	FMEA2ALRTEN	FMEA1ALRTEN

ADDRESS	NAME	MSB							LSB
0x1A	ALRTOVEN[15:8]	CSAOVALRTEN	BLKOVALRTEN	OVALRTEN[14:9]					
	ALRTOVEN[7:0]	OVALRTEN[8:1]							
0x1B	ALRTUVEN[15:8]	CSAUVALRTEN	BLKUVALRTEN	UVALRTEN[14:9]					
	ALRTUVEN[7:0]	UVALRTEN[8:1]							
0x1C	ALRTAUXOVEN[15:8]	–	–	–	–	–	–	–	–
	ALRTAUXOVEN[7:0]	–	–	–	–	AUXOVALRTEN[3:0]			
0x1D	ALRTAUXUVEN[15:8]	–	–	–	–	–	–	–	–
	ALRTAUXUVEN[7:0]	–	–	–	–	AUXUVALRTEN[3:0]			
0x1E	ALRTCALTST[15:8]	–	–	–	–	–	–	–	–
	ALRTCALTST[7:0]	–	–	–	CALOSADCALRTFRC	CALOSRALRTFRC	CALOSTHRMALRTFRC	CALGAINPALRTFRC	CALGAINRALRTFRC
THRESHOLD Registers									
0x1F	OVTHCLRREG[15:8]	OVTHCLR[13:6]							
	OVTHCLRREG[7:0]	OVTHCLR[5:0]						–	–
0x20	OVTHSETREG[15:8]	OVTHSET[13:6]							
	OVTHSETREG[7:0]	OVTHSET[5:0]						–	–
0x21	UVTHCLRREG[15:8]	UVTHCLR[13:6]							
	UVTHCLRREG[7:0]	UVTHCLR[5:0]						–	–
0x22	UVTHSETREG[15:8]	UVTHSET[13:6]							
	UVTHSETREG[7:0]	UVTHSET[5:0]						–	–
0x23	MSMTCHREG[15:8]	MSMTCH[13:6]							
	MSMTCHREG[7:0]	MSMTCH[5:0]						–	–
0x24	BIPOVTHCLRREG[15:8]	BIPOVTHCLR[13:6]							
	BIPOVTHCLRREG[7:0]	BIPOVTHCLR[5:0]						–	–
0x25	BIPOVTHSETREG[15:8]	BIPOVTHSET[13:6]							
	BIPOVTHSETREG[7:0]	BIPOVTHSET[5:0]						–	–
0x26	BIPUVTHCLRREG[15:8]	BIPUVTHCLR[13:6]							
	BIPUVTHCLRREG[7:0]	BIPUVTHCLR[5:0]						–	–
0x27	BIPUVTHSETREG[15:8]	BIPUVTHSET[13:6]							
	BIPUVTHSETREG[7:0]	BIPUVTHSET[5:0]						–	–
0x28	BLKOVTHCLRREG[15:8]	BLKOVTHCLR[13:6]							
	BLKOVTHCLRREG[7:0]	BLKOVTHCLR[5:0]						–	–
0x29	BLKOVTHSETREG[15:8]	BLKOVTHSET[13:6]							
	BLKOVTHSETREG[7:0]	BLKOVTHSET[5:0]						–	–

ADDRESS	NAME	MSB							LSB
0x2A	BLKUVTHCLRREG[15:8]	BLKUVTHCLR[13:6]							
	BLKUVTHCLRREG[7:0]	BLKUVTHCLR[5:0]						–	–
0x2B	BLKUVTHSETREG[15:8]	BLKUVTHSET[13:6]							
	BLKUVTHSETREG[7:0]	BLKUVTHSET[5:0]						–	–
0x2C	CSAOVTHCLRREG[15:8]	CSAOVTHCLR[13:6]							
	CSAOVTHCLRREG[7:0]	CSAOVTHCLR[5:0]						–	–
0x2D	CSAOVTHSETREG[15:8]	CSAOVTHSET[13:6]							
	CSAOVTHSETREG[7:0]	CSAOVTHSET[5:0]						–	–
0x2E	CSAUVTHCLRREG[15:8]	CSAUVTHCLR[13:6]							
	CSAUVTHCLRREG[7:0]	CSAUVTHCLR[5:0]						–	–
0x2F	CSAUVTHSETREG[15:8]	CSAUVTHSET[13:6]							
	CSAUVTHSETREG[7:0]	CSAUVTHSET[5:0]						–	–
0x30	AUXROVTHCLRREG[15:8]	AUXROVTHCLR[13:6]							
	AUXROVTHCLRREG[7:0]	AUXROVTHCLR[5:0]						–	–
0x31	AUXROVTHSETREG[15:8]	AUXROVTHSET[13:6]							
	AUXROVTHSETREG[7:0]	AUXROVTHSET[5:0]						–	–
0x32	AUXRUVTHCLRREG[15:8]	AUXRUVTHCLR[13:6]							
	AUXRUVTHCLRREG[7:0]	AUXRUVTHCLR[5:0]						–	–
0x33	AUXRUVTHSETREG[15:8]	AUXRUVTHSET[13:6]							
	AUXRUVTHSETREG[7:0]	AUXRUVTHSET[5:0]						–	–
0x34	AUXAOVTHCLRREG[15:8]	AUXAOVTHCLR[13:6]							
	AUXAOVTHCLRREG[7:0]	AUXAOVTHCLR[5:0]						–	–
0x35	AUXAOVTHSETREG[15:8]	AUXAOVTHSET[13:6]							
	AUXAOVTHSETREG[7:0]	AUXAOVTHSET[5:0]						–	–
0x36	AUXAUVTHCLRREG[15:8]	AUXAUVTHCLR[13:6]							

ADDRESS	NAME	MSB							LSB
	AUXAUVTHCLRREG[7:0]	AUXAUVTHCLR[5:0]						–	–
0x37	AUXAUVTHSETREG[15:8]	AUXAUVTHSET[13:6]							
	AUXAUVTHSETREG[7:0]	AUXAUVTHSET[5:0]						–	–
0x38	COMPOVTHREG[15:8]	COMPOVTH[9:2]							
	COMPOVTHREG[7:0]	COMPOVTH[1:0]	–	–	–	–	–	–	
0x39	COMPUVTHREG[15:8]	COMPUVTH[9:2]							
	COMPUVTHREG[7:0]	COMPUVTH[1:0]	–	–	–	–	–	–	
0x3A	COMPAUXROVTHREG[15:8]	COMPAUXROVTH[9:2]							
	COMPAUXROVTHREG[7:0]	COMPAUXROVTH[1:0]	–	–	–	–	–	–	
0x3B	COMPAUXRUVTHREG[15:8]	COMPAUXRUVTH[9:2]							
	COMPAUXRUVTHREG[7:0]	COMPAUXRUVTH[1:0]	–	–	–	–	–	–	
0x3C	COMPAUXAOVTHREG[15:8]	COMPAUXAOVTH[9:2]							
	COMPAUXAOVTHREG[7:0]	COMPAUXAOVTH[1:0]	–	–	–	–	–	–	
0x3D	COMPAUXAUVTHREG[15:8]	COMPAUXAUVTH[9:2]							
	COMPAUXAUVTHREG[7:0]	COMPAUXAUVTH[1:0]	–	–	–	–	–	–	
DIAGNOSTIC THRESHOLD Registers									
0x3E	COMPOPNTHREG[15:8]	COMPOPNTH[9:2]							
	COMPOPNTHREG[7:0]	COMPOPNTH[1:0]	–	–	–	–	–	–	
0x3F	COMPAUXROPNTHREG[15:8]	COMPAUXROPNTH[9:2]							
	COMPAUXROPNTHREG[7:0]	COMPAUXROPNTH[1:0]	–	–	–	–	–	–	
0x40	COMPAUXAOPNTHREG[15:8]	COMPAUXAOPNTH[9:2]							
	COMPAUXAOPNTHREG[7:0]	COMPAUXAOPNTH[1:0]	–	–	–	–	–	–	
0x41	COMPACCOVTHREG[15:8]	COMPACCOVTH[9:2]							
	COMPACCOVTHREG[7:0]	COMPACCOVTH[1:0]	–	–	–	–	–	–	
0x42	COMPACCUVTHREG[15:8]	COMPACCUVTH[9:2]							
	COMPACCUVTHREG[7:0]	COMPACCUVTH[1:0]	–	–	–	–	–	–	

ADDRESS	NAME	MSB							LSB
0x43	BALSHRTTHRREG[15:8]	BALSHRTTHR[13:6]							
	BALSHRTTHRREG[7:0]	BALSHRTTHR[5:0]						–	–
0x44	BALLOWTHRREG[15:8]	BALLOWTHR[13:6]							
	BALLOWTHRREG[7:0]	BALLOWTHR[5:0]						–	–
0x45	BALHIGHTHRREG[15:8]	BALHIGHTHR[13:6]							
	BALHIGHTHRREG[7:0]	BALHIGHTHR[5:0]						–	–
CELL DATA Registers									
0x46	CSAREG[15:8]	CSA[13:6]							
	CSAREG[7:0]	CSA[5:0]						–	–
0x47	CELL1REG[15:8]	CELL1[13:6]							
	CELL1REG[7:0]	CELL1[5:0]						–	–
0x48	CELL2REG[15:8]	CELL2[13:6]							
	CELL2REG[7:0]	CELL2[5:0]						–	–
0x49	CELL3REG[15:8]	CELL3[13:6]							
	CELL3REG[7:0]	CELL3[5:0]						–	–
0x4A	CELL4REG[15:8]	CELL4[13:6]							
	CELL4REG[7:0]	CELL4[5:0]						–	–
0x4B	CELL5REG[15:8]	CELL5[13:6]							
	CELL5REG[7:0]	CELL5[5:0]						–	–
0x4C	CELL6REG[15:8]	CELL6[13:6]							
	CELL6REG[7:0]	CELL6[5:0]						–	–
0x4D	CELL7REG[15:8]	CELL7[13:6]							
	CELL7REG[7:0]	CELL7[5:0]						–	–
0x4E	CELL8REG[15:8]	CELL8[13:6]							
	CELL8REG[7:0]	CELL8[5:0]						–	–
0x4F	CELL9REG[15:8]	CELL9[13:6]							
	CELL9REG[7:0]	CELL9[5:0]						–	–
0x50	CELL10REG[15:8]	CELL10[13:6]							
	CELL10REG[7:0]	CELL10[5:0]						–	–
0x51	CELL11REG[15:8]	CELL11[13:6]							
	CELL11REG[7:0]	CELL11[5:0]						–	–
0x52	CELL12REG[15:8]	CELL12[13:6]							
	CELL12REG[7:0]	CELL12[5:0]						–	–
0x53	CELL13REG[15:8]	CELL13[13:6]							
	CELL13REG[7:0]	CELL13[5:0]						–	–
0x54	CELL14REG[15:8]	CELL14[13:6]							
	CELL14REG[7:0]	CELL14[5:0]						–	–
0x55	BLOCKREG[15:8]	VBLOCK[13:6]							
	BLOCKREG[7:0]	VBLOCK[5:0]						–	–

ADDRESS	NAME	MSB							LSB
TOTAL DIAG AUX DATA Registers									
0x56	TOTALREG[15:8]	TOTAL[15:8]							
	TOTALREG[7:0]	TOTAL[7:0]							
0x57	DIAG1REG[15:8]	DIAG1[13:6]							
	DIAG1REG[7:0]	DIAG1[5:0]						–	–
0x58	DIAG2REG[15:8]	DIAG2[13:6]							
	DIAG2REG[7:0]	DIAG2[5:0]						–	–
0x59	AUX0REG[15:8]	AUX0[13:6]							
	AUX0REG[7:0]	AUX0[5:0]						–	–
0x5A	AUX1REG[15:8]	AUX1[13:6]							
	AUX1REG[7:0]	AUX1[5:0]						–	–
0x5B	AUX2REG[15:8]	AUX2[13:6]							
	AUX2REG[7:0]	AUX2[5:0]						–	–
0x5C	AUX3REG[15:8]	AUX3[13:6]							
	AUX3REG[7:0]	AUX3[5:0]						–	–
SCAN SETTINGS Registers									
0x5F	POLARITYCTRL[15:8]	MINMAX POL	–	POLARITY[14:9]					
	POLARITYCTRL[7:0]	POLARITY[8:1]							
0x60	AUXREFCTRL[15:8]	–	–	–	–	–	–	–	–
	AUXREFCTRL[7:0]	–	–	–	–	AUXREFSEL[3:0]			
0x61	AUXTIMEREG[15:8]	–	–	–	–	–	–	AUXTIME[9:8]	
	AUXTIMEREG[7:0]	AUXTIME[7:0]							
0x62	ACQCFG[15:8]	ADCZSFSEN	ADCCALEN	COMPACCEN	FOSR[1:0]		THRMMODE[1:0]		CSAGAIN[2]
	ACQCFG[7:0]	CSAGAIN[1:0]		–	–	–	–	–	–
0x63	BALSWDLY[15:8]	CELLDLY[7:0]							
	BALSWDLY[7:0]	SWDLY[7:0]							
SCAN CONTROL Registers									
0x64	MEASUREEN1[15:8]	CSAEN	BLOCKEN	CELLEN[14:9]					
	MEASUREEN1[7:0]	CELLEN[8:1]							
0x65	MEASUREEN2[15:8]	SCANIIRINIT	–	–	–	–	–	–	–
	MEASUREEN2[7:0]	–	–	–	–	AUXEN[3:0]			
0x66	SCANCTRL[15:8]	SCANDONE	SCANTIMEOUT	DATARDY	AUTOBALSWDIS	ALRTFILTSEL	AMENDFILT	RDFILT	SCANCFG[2]
	SCANCTRL[7:0]	SCANCFG[1:0]		OVSAMPL[2:0]			ALTMUXSEL	SCANMODE	SCAN
DIAGNOSTIC SETTINGS Registers									
0x67	ADCTEST1AREG[15:8]	ADCTSTEN	–	–	–	ADCTEST1A[11:8]			
	ADCTEST1AREG[7:0]	ADCTEST1A[7:0]							

ADDRESS	NAME	MSB							LSB
0x68	ADCTEST1BREG[15:8]	–	–	–	–	ADCTEST1B[11:8]			
	ADCTEST1BREG[7:0]	ADCTEST1B[7:0]							
0x69	ADCTEST2AREG[15:8]	–	–	–	–	ADCTEST2A[11:8]			
	ADCTEST2AREG[7:0]	ADCTEST2A[7:0]							
0x6A	ADCTEST2BREG[15:8]	–	–	–	–	ADCTEST2B[11:8]			
	ADCTEST2BREG[7:0]	ADCTEST2B[7:0]							
DIAGNOSTIC CONTROL Registers									
0x6B	DIAGCFG[15:8]	CTSTDAC[3:0]				CTSTSRC	MUXDIAGBUS	MUXDIAGPAIR	MUXDIAGEN
	DIAGCFG[7:0]	DIAGSEL2[3:0]				DIAGSEL1[3:0]			
0x6C	CTSTCFG[15:8]	CELLOPNDIAGSEL	CTSTEN[14:8]						
	CTSTCFG[7:0]	CTSTEN[7:0]							
0x6D	AUXTSTCFG[15:8]	–	–	–	–	–	–	–	–
	AUXTSTCFG[7:0]	–	–	AUXTSTEN[5:4]		AUXTSTEN[3:0]			
0x6E	DIAGGENCFG[15:8]	AUXDIAGSEL[2:0]			CSATSTSEL[1:0]		–	–	–
	DIAGGENCFG[7:0]	–	–	–	–	–	–	–	–
CELL BALANCING Registers									
0x6F	BALSWCTRL[15:8]	CBRESTART	–	BALSWEN[14:9]					
	BALSWCTRL[7:0]	BALSWEN[8:1]							
0x70	BALEXP1[15:8]	–	–	–	–	–	–	CBEXP1[9:8]	
	BALEXP1[7:0]	CBEXP1[7:0]							
0x71	BALEXP2[15:8]	–	–	–	–	–	–	CBEXP2[9:8]	
	BALEXP2[7:0]	CBEXP2[7:0]							
0x72	BALEXP3[15:8]	–	–	–	–	–	–	CBEXP3[9:8]	
	BALEXP3[7:0]	CBEXP3[7:0]							
0x73	BALEXP4[15:8]	–	–	–	–	–	–	CBEXP4[9:8]	
	BALEXP4[7:0]	CBEXP4[7:0]							
0x74	BALEXP5[15:8]	–	–	–	–	–	–	CBEXP5[9:8]	
	BALEXP5[7:0]	CBEXP5[7:0]							
0x75	BALEXP6[15:8]	–	–	–	–	–	–	CBEXP6[9:8]	
	BALEXP6[7:0]	CBEXP6[7:0]							
0x76	BALEXP7[15:8]	–	–	–	–	–	–	CBEXP7[9:8]	
	BALEXP7[7:0]	CBEXP7[7:0]							
0x77	BALEXP8[15:8]	–	–	–	–	–	–	CBEXP8[9:8]	
	BALEXP8[7:0]	CBEXP8[7:0]							
0x78	BALEXP9[15:8]	–	–	–	–	–	–	CBEXP9[9:8]	
	BALEXP9[7:0]	CBEXP9[7:0]							
0x79	BALEXP10[15:8]	–	–	–	–	–	–	CBEXP10[9:8]	
	BALEXP10[7:0]	CBEXP10[7:0]							

ADDRESS	NAME	MSB							LSB
0x7A	BALEXP11[15:8]	–	–	–	–	–	–	CBEXP11[9:8]	
	BALEXP11[7:0]	CBEXP11[7:0]							
0x7B	BALEXP12[15:8]	–	–	–	–	–	–	CBEXP12[9:8]	
	BALEXP12[7:0]	CBEXP12[7:0]							
0x7C	BALEXP13[15:8]	–	–	–	–	–	–	CBEXP13[9:8]	
	BALEXP13[7:0]	CBEXP13[7:0]							
0x7D	BALEXP14[15:8]	–	–	–	–	–	–	CBEXP14[9:8]	
	BALEXP14[7:0]	CBEXP14[7:0]							
0x7E	BALAUTOUVTHR[15:8]	CBUVTHR[13:6]							
	BALAUTOUVTHR[7:0]	CBUVTHR[5:0]						–	CBUVMINCELL
0x7F	BALDLYCTRL[15:8]	–	–	–	–	–	–	CBNTFYCFG[1:0]	
	BALDLYCTRL[7:0]	–	–	–	–	–	CBCALDLY[2:0]		
0x80	BALCTRL[15:8]	CBACTIVE[1:0]		CBMODE[2:0]			CBIIRINIT	HOLDSHDNL[1:0]	
	BALCTRL[7:0]	CBDUTY[3:0]				CBDONEALRTEN	CBTEMPEN	CBMEASEN[1:0]	
0x81	BALSTAT[15:8]	CBACTIVE_M1[1:0]		CBUNIT[1:0]		CBCNTR[1:0]		CBTIMER[9:8]	
	BALSTAT[7:0]	CBTIMER[7:0]							
0x82	BALUVSTAT[15:8]	CBACTIVE_M2[1:0]		CBUVSTAT[14:9]					
	BALUVSTAT[7:0]	CBUVSTAT[8:1]							
0x83	BALDATA[15:8]	CBACTIVE_M3[1:0]		DATARDY_M	–	–	–	–	–
	BALDATA[7:0]	–	–	–	–	–	–	–	CBSCAN
I2C MASTER Registers									
0x84	I2CPNTR[15:8]	I2CPBYTE1[7:0]							
	I2CPNTR[7:0]	I2CPBYTE0[7:0]							
0x85	I2CWDATA1[15:8]	I2CWBYTE3[7:0]							
	I2CWDATA1[7:0]	I2CWBYTE2[7:0]							
0x86	I2CWDATA2[15:8]	I2CWBYTE1[7:0]							
	I2CWDATA2[7:0]	I2CWBYTE0[7:0]							
0x87	I2CRDATA1[15:8]	I2CRBYTE3[7:0]							
	I2CRDATA1[7:0]	I2CRBYTE2[7:0]							
0x88	I2CRDATA2[15:8]	I2CRBYTE1[7:0]							
	I2CRDATA2[7:0]	I2CRBYTE0[7:0]							
0x89	I2CCFG[15:8]	I2CFSCL	I2CWALT	I2CRFMT	I2C10BIT	I2CPNTRLNGTH	I2CALRTEN	–	–
	I2CCFG[7:0]	–	–	I2CANACONTEN	I2CCONTEN	I2CGLITCHEN	I2CNOISEEN	I2CRDTREN	I2CTOEN
0x8A	I2CSTAT[15:8]	I2CSTATUS[1:0]		–	–	–	–	–	I2CRJCT
	I2CSTAT[7:0]	I2CDEVNACK	I2CDATANACK	I2CANACONT	I2CCONT	I2CGLITCH	I2CNOISE	I2CRDTRERR	I2CTIMEOUT

ADDRESS	NAME	MSB							LSB
0x8B	I2CSEND[15:8]	I2CPNTRSEL	I2CDATALNGTH[1:0]		I2CDATASEL[1:0]		I2CDEVIDEXT[2:0]		
	I2CSEND[7:0]	I2CDEVID[6:0]							I2CRWB
ROM SUPPORT Registers									
0x8C	ID1[15:8]	DEVID[15:8]							
	ID1[7:0]	DEVID[7:0]							
0x8D	ID2[15:8]	DEVID[31:24]							
	ID2[7:0]	DEVID[23:16]							
0x8E	OTP2[15:8]	OTP2[15:8]							
	OTP2[7:0]	OTP2[7:0]							
0x8F	OTP3[15:8]	OTP3[15:8]							
	OTP3[7:0]	OTP3[7:0]							
0x90	OTP4[15:8]	OTP4[15:8]							
	OTP4[7:0]	OTP4[7:0]							
0x91	OTP5[15:8]	OTP5[15:8]							
	OTP5[7:0]	OTP5[7:0]							
0x92	OTP6[15:8]	OTP6[15:8]							
	OTP6[7:0]	OTP6[7:0]							
0x93	OTP7[15:8]	OTP7[15:8]							
	OTP7[7:0]	OTP7[7:0]							
0x94	OTP8[15:8]	OTP8[15:8]							
	OTP8[7:0]	OTP8[7:0]							
0x95	OTP9[15:8]	OTP9[15:8]							
	OTP9[7:0]	OTP9[7:0]							
0x96	OTP10[15:8]	OTP10[15:8]							
	OTP10[7:0]	OTP10[7:0]							
0x97	OTP11[15:8]	OTP11[15:8]							
	OTP11[7:0]	OTP11[7:0]							
0x98	OTP12[15:8]	ROMCRC[7:0]							
	OTP12[7:0]	OTP12[7:0]							

Register Details

VERSION (0x0)

VERSION is a read only accessible register which returns information on the device.

BIT	15	14	13	12	11	10	9	8
Field	MOD[11:4]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	MOD[3:0]				VER[3:0]			
Reset					0x7			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
MOD	15:4	Device Model Number 0x852 = MAX17852 Read-only.
VER	3:0	Si Version Current Version = 0x7 Read-only.

ADDRESS (0x1)

ADDRESS is a read and write accessible register which sets the first, last, and device address used by a device in a UART chain (UARTSEL=1).

This register has no effect on a device operating in SPI mode (UARTSEL=0).

BIT	15	14	13	12	11	10	9	8
Field	ADDRUNLOCK	BA[4:0]					TA[4:3]	
Reset	0b1	0b0_0000					0b0_0000	
Access Type	Write, Read, Ext	Write, Read, Ext					Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	TA[2:0]			DA[4:0]				
Reset	0b0_0000			0b0_0000				
Access Type	Write, Read, Ext			Write, Read, Ext				

BITFIELD	BITS	DESCRIPTION
ADDRUNLOCK	15	UART Device Address Unlock 0 = Normal Operation (following HELLOALL) 1 = Disable write-protection of device address DA[4:0], allowing re-sends of HELLOALL to reassign device addresses without POR (also POR default). Cleared only by HELLOALL command (writes to zero are ignored). This bitfield is unaffected in the event of a SWPOR (Software POR) request by the Host. *Note: This bit should normally be written to zero when populating BA and TA content, it should only be necessary to set this bit if the user believes the original DA content populated by the HELLOALL command is corrupted.*

BITFIELD	BITS	DESCRIPTION
BA	14:10	Bottom Device Address in a UART Chain Address of the device at the bottom of the daisy chain. If the host sends an initial address other than 0x00 in the HELLOALL command via the UART UP path (assign/increment), then the host must write that bottom address (as well as the expected top address) to all devices in the daisy-chain with a WRITEALL command to this bitfield. READALL commands and Alert Packets require that BA[4:0], TA[4:0], and DA[4:0] be correct in order for the data-check and PEC features to function as intended. This bitfield is unaffected in the event of a SWPOR (Software POR) request by the Host.
TA	9:5	Top Device Address in a UART Chain Address of the device connected to the top of the daisy chain. If the host sends an initial address in the HELLOALL command via the UART DOWN path (assign/decrement), then the host must write that top address (as well as the expected bottom address) to all devices in the daisy-chain with a WRITEALL command to this bitfield. READALL commands and Alert Packets require that BA[4:0], TA[4:0], and DA[4:0] be correct in order for the data-check and PEC features to function as intended. This bitfield is unaffected in the event of a SWPOR (Software POR) request by the Host.
DA	4:0	Device Address Device address written only by the HELLOALL command as it propagates through the daisy-chain. If HELLOALL is issued via the UART UP path, this bitfield is accepted and then automatically incremented by each device. If HELLOALL is issued via the UART DOWN path, this bitfield is accepted and then automatically decremented by each device. The host must choose an initial (bottom) address 0x00 or greater and ensure the resulting top address will not exceed the maximum address of 0x1F during the propagation of the HELLOALL command via the UP path. Likewise, the host must choose an initial (top) address 0x1F or lower and ensure that the resulting bottom address will be 0x00 or greater after propagation of the HELLOALL command via the DOWN path. Writing has no effect, only a HELLOALL command executed while ADDRUNLOCK = 1 will update this content. This bitfield is unaffected in the event of a SWPOR (Software POR) request by the Host.

STATUS1 (0x2)

STATUS1 is a read and write accessible register which relates the current status of the device. STATUS1 also contains summary information on STATUS2, STATUS3, and FMEA registers, and other selected registers indicating if additional read back checks are required.

BIT	15	14	13	12	11	10	9	8
Field	ALRTSCAN	ALRTRST	ALRTMSMTCH	ALRTCELLOVST	ALRTCELLUVST	ALRTBLKOVST	ALRTBLKUVST	ALRTAUXOVST
Reset	0b0	0b1	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Write 0 to Clear, Read	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BIT	7	6	5	4	3	2	1	0
Field	ALRTAUXUVST	ALRTCSAST	ALRTPEC	ALRTINTRFC	ALRTCAL	ALRTCBAL	ALRTFMEA2	ALRTFMEA1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
ALRTSCAN	15	Scan Done Alert 0 = No Measurement requested or Measurement in progress (default) 1 = Measurement Complete Cleared if SCANCRTL:SCANDONE is removed. Read only.
ALRTRST	14	Reset Alert Indicates a power-on-reset event occurred. UART users should clear this alert after power-on and after a successful HELLOALL transaction in order to detect future resets. SPI users should clear this alert immediately after power-on in order to detect future resets. Cleared only by writing to logic zero. Writing to a logic one has no effect.
ALRTMSMTCH	13	Cell Voltage Mismatch Alert Indicates V_{MAX} - V_{MIN} > V_{MSMTCH} threshold. Read MINMAXCELL for detailed information on which channels are involved to aide diagnosis. Cleared at next acquisition if the condition is false. Read-only.
ALRTCELLOVST	12	Cell Overvoltage Status Summary Alert Bit-wise logical OR of ALRTOV[14:1] and ALRTCOMPOV[14:1]. Read ALRTSUM for information on whether the ADC, Comparator, or both circuits detected the fault to aide diagnosis. Cleared on next acquisition, if all enabled overvoltage conditions are resolved. Read-only.

BITFIELD	BITS	DESCRIPTION
ALRTCELLUVST	11	Cell Undervoltage Status Summary Alert Bit-wise logical OR of ALRTUV[14:1] and ALRTCOMPUV[14:1]. Read ALRTSUM for information on whether the ADC, Comparator, or both circuits detected the fault to aide diagnosis. Cleared on next acquisition, if all enabled undervoltage conditions are resolved. Read-only.
ALRTBLKOVST	10	Block Overvoltage Status Alert Inidcates the latest Block voltage measurement exceeded the threshold set by BLKOVTHSET. Cleared on next Block voltage acquisition, if condition is resolved. Read-only.
ALRTBLKUVST	9	Block Undervoltage Status Alert Inidcates the latest Block voltage measurement was below the threshold set by BLKUVTHSET. Cleared on next Block voltage acquisition, if condition is resolved. Read-only.
ALRTAUXOVST	8	Auxiliary Overvoltage (Cold) Status Summary Alert Logical OR of ALRTAUXOV[5:0] and ALRTCOMPAUXOV[5:0] auxiliary alerts. Read ALRTSUM for information on whether the ADC, Comparator, or both circuits detected the fault to aide diagnosis. Cleared on next acquisition, if all enabled overvoltage conditions are resolved. Read-only.
ALRTAUXUVST	7	Auxiliary Undervoltage (Hot) Status Summary Alert Logical OR of ALRTAUXUV[5:0] and ALRTCOMPAUXUV[5:0] auxiliary alerts. Read ALRTSUM for information on whether the ADC, Comparator, or both circuits detected the fault to aide diagnosis. Cleared on next acquisition, if all enabled undervoltage conditions are resolved. Read-only.
ALRTCSAST	6	Current-Sense Amplifier Alert Status Summary Logical OR of ALRTCSAOV and ALRTCSAUV. Read ALRTSUM to determine which fault(s) occured and complete the diagnosis. Cleared on next acquisition, if all CSA undervoltage/overvoltage conditions are resolved. Read-only.

BITFIELD	BITS	DESCRIPTION
ALRTPEC	5	PEC (CRC) Alert Indicates a received UART/SPI character/transaction contained a PEC/CRC error and was ignored as a result. Logical OR of (ALRTPECUP, ALRTPECDN, SPICRCERR). Cleared if component alerts are resolved in STATUS2:ALRTPECUP/DN (UART), or STATUS2:ALRTSPI (SPI), see component bitfield descriptions for details. *Note: in UARTSEL=0 (SPI Mode), the SPICRCERR bit only appears in the SPI transaction as STAT[4] (DO[31]), it does not activate STATUS2:ALRTSPI, though it is cleared by writing STATUS2:ALRTSPI to zero.* Read only.
ALRTINTRFC	4	Interface Specific Error Alert Indicates that an error specific to the selected interface (UART or SPI User interface and/or I2C Master interface (if enabled) has occurred. For UART operation, this is the bitwise OR of (ALRTMANUP/DN, ALRTPARUP/DN, ALRTDUALART, ALRTRJCT, ALRTI2C). For SPI operation, this is the bitwise OR of (ALRTSPI, ALRTSCLKERR, ALRTOSC3, ALRTINTBUS, ALRTRJCT, ALRTI2C). ALRTPEC is common to both UART and SPI interfaces and holds a dedicated position in the STATUS register (assertion of ALRTPEC will not assert ALRTINTRFC). If this alert bit is set, the specific error(s) can be read and cleared using the STATUS2 register.
ALRTCAL	3	Calibration Fault Alert Logical OR of all calibration alerts (ALRTCALOSADC, ALRTCALOSR, ALERTCALOSTHRM, ALRTCALGAINP, ALRTCALGAINR). Cleared if component alerts are resolved in ALRTSUM, see ALRTSUM and ALRTIRQEN for details. Read only. If a calibration error occurs during an Automated Cell Balancing or Discharge operation, the operation will end and issue CBACTIVE=11 and ALRTCBCAL, notifying the user of the termination.

BITFIELD	BITS	DESCRIPTION
ALRTCBAL	2	Cell Balancing Status Alert 0 = Cell Balancing Inactive/Normal 1 = Cell Balancing Complete/Fault Logical OR of all enabled/unmasked cell balancing alerts (ALRTCBTIMEOUT, ALRTCBTEMP, ALRTCBCAL, ALRTCBNTFY, ALRTCBDONE). Cleared if component alerts are resolved in STATUS3, see STATUS3 and ALRTIRQEN for details. Read only.
ALRTFMEA2	1	FMEA2 Condition Summary Alert Bit-wise logical OR of FMEA2[15:0]. Read-only.
ALRTFMEA1	0	FMEA1 Condition Summary Alert Bit-wise logical OR of FMEA1[15:0]. Read-only.

STATUS2 (0x3)

STATUS2 is a read and write accessible register which contains summary information on alerts related to interface and communication faults.

BIT	15	14	13	12	11	10	9	8
Field	ALRTPECUP	ALRTPECDN	ALRTMANUP	ALRTMANDN	ALRTPARUP	ALRTPARDN	ALRTDUALUART	–
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	–
Access Type	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	–

BIT	7	6	5	4	3	2	1	0
Field	ALRTSPI	ALRTSCLKERR	ALRTOSC3	ALRTINTBUS	–	ALRTI2C	–	ALRTRJCT
Reset	0b0	0b0	0b0	0b0	–	0b0	–	0b0
Access Type	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	–	Read Only	–	Write 0 to Clear, Read

BITFIELD	BITS	DESCRIPTION
ALRTPECUP	15	UART Up Interface Packet Error Check Alert Indicates a character/transaction recieved by the UART Up Interface contained a PEC error and was ignored as a result. Cleared only by writing to logic zero. Writing to a logic one has no effect. Applies only to parts operating using the UART interface (UARTSEL=1), PEC is not used in SPI mode (SPI CRC checking is reported and managed directly via ALRTPEC and ALRTSPI,respectively).

BITFIELD	BITS	DESCRIPTION
ALRTPECDN	14	UART Down Interface Packet Error Check Alert Indicates a character/transaction recieved by the UART Down Interface contained a PEC error and was ignored as a result. Cleared only by writing to logic zero. Writing to a logic one has no effect. Applies only to parts operating using the Dual UART interface (UARTSEL=1, UARTCFG=11), not used in SPI mode.
ALRTMANUP	13	UART Up Interface Manchester Encoding Error Indicates that a character received by the UART Up Interface (via RXL) contained a Manchester error. Cleared only by writing to logic zero. Writing to a logic one has no effect. Applies only to parts operating using the UART interface (UARTSEL=1). Manchester encoding is not used in SPI mode.
ALRTMANDN	12	UART Down Interface Manchester Encoding Error Indicates that a character received by the UART Down Interface (via RXU) contained a Manchester error. Cleared only by writing to logic zero. Writing to a logic one has no effect. Applies only to parts operating using the Dual UART interface (UARTSEL=1, UARTCFG=11). Manchester encoding is not used in SPI mode.
ALRTPARUP	11	UART Up Interface Parity Error Indicates that a character received by the UART Up Interface (via RXL) contained a parity error. Cleared only by writing to logic zero. Writing to a logic one has no effect. Applies only to parts operating using the UART interface (UARTSEL=1). Parity checking is not used in SPI mode.
ALRTPARDN	10	UART Down Interface Parity Error Indicates that a character received by the UART Down Interface (via RXU) contained a parity error. Cleared only by writing to logic zero. Writing to a logic one has no effect. Applies only to parts operating using the Dual UART interface (UARTSEL=1, UARTCFG=11). Parity checking is not used in SPI mode.

BITFIELD	BITS	DESCRIPTION
ALRTDUALUART	9	Dual UART Fault Alert 0 = No Dual UART Fault Detected 1 = Invalid Dual UART Command Received ALRTDUALUART indicates one or more of the following conditions occured: A WRITEDEVICE or WRITEALL command sent through a path not configured as Host was ignored (only the Host path accepts writes). An UPHOST command was issued and ignored on the downstream UART path. An DOWNHOST command was issued and ignored on the upstream UART path. These conditions are checked only when UARTCFG=DUAL (11). Cleared only by writing to logic zero. Writing to a logic one has no effect.
ALRTSPI	7	SPI Error Summary Alert Indicates one or more of the following SPI transaction errors have occured: ● R/WB != R/WB' (i.e. DI[31] != DI[3], RW_ERR) ● D_{IN}[15:0] != 0x0000 in Read Mode (RW_ERR) ● Transaction Time Out (TO_ERR) Specific error condition breakouts are reported as STAT[4:0] (DO[31:27]) as part of all SPI transactions. All existing SPI CRC_ERR, RW_ERR, and TO_ERR, alerts will be cleared by writing this bit to logic zero. Writing to a logic one has no effect. Applies only to parts operating using the SPI interface (UARTSEL=0). *Note: The SPI CRC_ERR condition is reported using the dedicated STATUS1:ALRTPEC bit (read only), but is cleared using this bitfield (i.e. the CRC_ERR condition is not reported in ALRTSPI). To clear ALRTPEC, it will be necessary to write ALRTSPI to zero even if it is already zero (if no other SPI Errors are reported). SPI clock issues covered by SPI CLK_ERR are broken out, reported, and cleared individually (see ALRTSCLKERR, ALRTOSC3, and ALRTINTBUS for details).*
ALRTSCLKERR	6	SPI SCLK Error Alert Indicates a SPI transaction was received that was not exactly 32 SCLK cycles in length. This error condition is one of three reported as STAT[1] (DO[28]) as part of all SPI transactions. Cleared by writing this bit to logic zero. Writing to a logic one has no effect. Applies only to parts operating using the SPI interface (UARTSEL=0).

BITFIELD	BITS	DESCRIPTION
ALRTOSC3	5	16MHz Oscilator Fault Alert Indicates that the 16MHz oscillator frequency is not within +/-5% of its expected value when measured against the 32kHz oscillator. The status is updated every two cycles (32kHz). Required/supported only in SPI mode (UARTSEL=0). While it is possible for the SPI interface to continue to function under drift alert conditions, it will not function if the 16MHz oscillator is dead or extremely fast/slow. This error condition is one of three reported as STAT[1] (DO[28]) as part of all SPI transactions. Cleared only by writing to logic zero if the condition has been resolved. Writing to a logic one has no effect.
ALRTINTBUS	4	SPI Internal Bus Transaction Failure Indicates a SPI read or write transaction was not correctly passed across the internal memory bus. This can happen if the 16MHz oscillator (or branch) clocking the internal bus is dead, intermittent, or severely out of its specified frequency range. May be accompanied by ALRTOSC1, 2, or 3 alerts. This error condition is one of three reported as STAT[1] (DO[28]) as part of all SPI transactions. Cleared by writing this bit to logic zero. Writing to a logic one has no effect. Applies only to parts operating using the SPI interface (UARTSEL=0).
ALRTI2C	2	I^2C Master Fault Alert Logical OR of I2CSTAT[8:0] error indicator bits, subject to masking by I2CCFG:I2CALRTEN. Cleared only when unmasked component alerts are resolved in the I2CSTAT register. Read-only.
ALRTRJCT	0	Protected Command Rejection Alert 0 = Normal Operation 1 = Invalid Command Rejected during an active Scan or Cell Balancing operation ALRTRJCT is issued when an invalid write to a protected register is received during an active/gating Scan or Cell Balancing operation. The invalid command will be ignored. Cleared only by writing to logic zero. Writing to a logic one has no effect.

STATUS3 (0x4)

STATUS3 is a read and write accessible register which contains summary information on alerts related to automated cell balancing operations.

BIT	15	14	13	12	11	10	9	8
Field	ALRTCBTIMEOUT	ALRTCBTEMP	ALRTCBCAL	ALRTCBNTFY	ALRTCBDONE	–	–	–
Reset	0b0	0b0	0b0		0b0	–	–	–
Access Type	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
ALRTCBTIMEOUT	15	Cell Balancing Time Out Alert 0 = Cell Balancing Disabled or in Progress 1 = Cell Balancing Operation Halted due to Timeout Fault ALRTCBTIMEOUT is issued when a Discharge, or Automated Cell Balancing operation is halted due to an internal logic fault condition triggering the watchdog timer. This alert is automatically enabled if CBTODIS=0. Cleared only by writing to logic zero. Writing to a logic one has no effect.
ALRTCBTEMP	14	Cell Balancing Thermal Alert 0 = Cell Balancing Disabled or in Progress 1 = Cell Balancing Operation Halted due to Thermal Fault ALRTCBTEMP is issued when a Maunual, Discharge, or Automated Cell Balancing operation is halted due to a thermal fault condition. This alert is automatically enabled if CBTEMPEN=1. Cleared only by writing to logic zero after the automated cell balancing operation which generated the alert has been completed or otherwise ended. Writing to a logic one has no effect.
ALRTCBCAL	13	Cell Balancing Calibration Alert 0 = Cell Balancing Disabled or in Progress 1 = Cell Balancing Operation Halted due to Calibration Fault ALRTCBCAL is issued when a Discharge, or Automated Cell Balancing operation is halted due to an embedded calibration fault condition. Cleared only by writing to logic zero after the automated cell balancing operation which generated the alert has been completed or otherwise ended. Writing to a logic one has no effect.

BITFIELD	BITS	DESCRIPTION
ALRTCBNTFY	12	Cell Balancing Notification Alert 0 = No Cell Balancing Progression Notification Present 1 = Cell Balancing Progression Notification ALRTCBNTFY is periodically issued during Discharge and Automated Cell Balancing operations to confirm normal progression of the operation. This alert is enabled and configured by CBNTFYCFG. Cleared only by writing to logic zero. Writing to a logic one has no effect.
ALRTCBDONE	11	Cell Balancing Complete Alert 0 = Cell Balancing Disabled or in Progress 1 = Cell Balancing Operation Complete ALRTCBDONE is issued when a Maunual, Discharge, or Automated Cell Balancing operation completes due to a normal timed or under voltage exit condition. Cleared only by writing to logic zero. Writing to a logic one has no effect.

FMEA1 (0x5)

FMEA1 is a read and write accessible register which relates current information on possible fault conditions.

BIT	15	14	13	12	11	10	9	8
Field	ALRTOSC1	ALRTOSC2	ALRTCOMMSEU1	ALRTCOMMSEL1	ALRTCOMMSEU2	ALRTCOMMSEL2	ALRTVDDL3	ALRTVDDL2
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write 0 to Clear, Read	Write 0 to Clear, Read	Read Only	Read Only	Read Only	Read Only	Write 0 to Clear, Read	Write 0 to Clear, Read

BIT	7	6	5	4	3	2	1	0
Field	ALRTVDDL1	ALRTGNDL3	ALRTGNDL2	ALRTGNDL1	ALRTHVUV	ALRTHVHDRM	ALRTHVOV	ALRTBALSWSUM
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write, Read, Ext

BITFIELD	BITS	DESCRIPTION
ALRTOSC1	15	32kHz Oscilator Fault Alert Indicates that the 32kHz frequency is not within +/-5% of its expected value when measured against the 16MHz oscillator. The status is updated every two cycles (32kHz). Cleared only by writing to logic zero if the condition has been resolved. Writing to a logic one has no effect.
ALRTOSC2	14	32kHz Oscilator Fault Alert (Redundant) Identical to ALRTOSC1 - redundant alert with independent latch. Cleared only by writing to logic zero if the condition has been resolved. Writing to a logic one has no effect.

BITFIELD	BITS	DESCRIPTION
ALRTCOMMSEU1	13	UART Upper Port Single-Ended Alert Indicates that the UART has placed the upper port receiver in single-ended mode based on the first preamble received after POR. This bit is not set until the ALRTRST bit is cleared. Read-only.
ALRTCOMMSEL1	12	UART Lower Port Single-Ended Alert Indicates that the UART has placed the lower port receiver in single-ended mode based on the first preamble received after POR. This bit is not set until the ALRTRST bit is cleared. Read-only.
ALRTCOMMSEU2	11	UART Upper Port Single-Ended Redundant Alert Same as ALRTCOMMSEU1 (redundant alert) except that it sets before ALRTRST is cleared. Read-only.
ALRTCOMMSEL2	10	UART Lower Port Single Ended Redundant Alert Same as ALRTCOMMSEL1 (redundant alert) except that it sets before ALRTRST is cleared. Read-only.
ALRTVDDL3	9	V_{DDL3} Fault Alert Indicates $V_{DDL3} < V_{VDDL_OC}$. This bit is not set until the ALRTRST bit is cleared. Cleared only by writing to logic zero if condition is resolved. Writing to a logic one has no effect.
ALRTVDDL2	8	V_{DDL2} Fault Alert Indicates $V_{DDL2} < V_{VDDL_OC}$. This bit is not set until the ALRTRST bit is cleared. Cleared only by writing to logic zero if condition is resolved. Writing to a logic one has no effect.
ALRTVDDL1	7	V_{DDL1} Fault Alert Indicates $V_{DDL1} < V_{VDDL_OC}$. This bit is not set until the ALRTRST bit is cleared. Cleared only by writing to logic zero if condition is resolved. Writing to a logic one has no effect.
ALRTGNDL3	6	GNDL3 Fault Alert Indicates an open-circuit on the GNDL3 pin. This bit is not set until the ALRTRST bit is cleared. Cleared only by writing to logic zero. Writing to a logic one has no effect.
ALRTGNDL2	5	GNDL2 Fault Alert Indicates an open-circuit on the GNDL2 pin. This bit is not set until the ALRTRST bit is cleared. Cleared only by writing to logic zero. Writing to a logic one has no effect.
ALRTGNDL1	4	GNDL1 Fault Alert Indicates an open-circuit on the GNDL1 pin. This bit is not set until the ALRTRST bit is cleared. Cleared only by writing to logic zero. Writing to a logic one has no effect.
ALRTHVUV	3	HV Undervoltage Fault Alert Indicates $V_{HV} < V_{HVUV}$. This bit is not set until the ALRTRST bit is cleared. Cleared only by writing to logic zero. Writing to a logic one has no effect.

BITFIELD	BITS	DESCRIPTION
ALRTHVHDRM	2	HV Headroom Fault Alert Indicates that $V_{HV} - V_{TOPCELL1/2}$ was too low during the acquisition for an accurate measurement. Checked only during measurement activity. Cleared only by writing to logic zero. Writing to a logic one has no effect.
ALRTHVOV	1	HV Overvoltage Fault Alert Indicates that $V_{HV} - V_{DCIN} > V_{HVOV}$. This bit is not set until the ALRTRST bit is cleared. Cleared only by writing to logic zero. Writing to a logic one has no effect.
ALRTBALSWSUM	0	Balance Switch Fault Alert Summary Bit-wise logical OR of ALRTBALSW[13:0]. Updated at the end of a BALSWDIAG scan. Cleared if all enabled ALRTBALSW alerts are resolved or by writing to logic zero. Writing to a logic one has no effect.

FMEA2 (0x6)

FMEA1 is a read and write accessible register which relates current information on possible fault conditions.

BIT	15	14	13	12	11	10	9	8
Field	ALRTUSER	ALRTDCINMUX	ALRTAUXPRTCTSUM	ALRTTEMP	ALRTSCANTIMEOUT	–	–	–
Reset	0b0	0b0	0b0	0b0	0b0	–	–	–
Access Type	Write, Read	Write 0 to Clear, Read	Read Only	Write 0 to Clear, Read	Read Only	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	ALRTADCZS	ALRTADCFS	ALRTCOMPACCOV	ALRTCOMPACCUV
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read

BITFIELD	BITS	DESCRIPTION
ALRTUSER	15	User-Defined Alert (Diagnostic) Used to test the Alert Interface. Asserted by writing to logic one. The resulting alert will be relayed via the Alert Interface/UART DCByte/SPI ALERT bit and can be read back using the FMEA2 command. Cleared by writing to logic zero (default).

BITFIELD	BITS	DESCRIPTION
ALRTDCINMUX	14	DCIN MUX Fault Alert 0 = No DCINMUX Fault Detected (default) 1 = DCINMUX Fault Detected A high condition indicates the enabled DCINMUX is not functioning properly in a Flex Pack application. Connections will be made by diodes, and performance may be impacted, and/or other related faults may be issued. This alert is enabled if the DCINMUX is enabled (FLXPACKEN=1), after STATUS1:ALRTRST has been cleared. The PACKCFG register makes selections on which SW[n] input is used for DCIN supply and which C[n] is used for VBLK measurements in Flex Pack applications. Cleared only by writing to logic zero if condition has been resolved. Writing to a logic one has no effect.
ALRTAUXPRTCTSUM	13	Auxiliary Protection Fault Alert Summary Logical OR of all enabled ALRTAUXPRTCT bits, indicating one or more AUXINn inputs is in a fault mode with input protection engaged. These alerts are enabled for all AUX/GPIO pins currently configured as AUXINn inputs. This bit will only be cleared when the ALRTAUXPRTCT register is cleared, see ALRTAUXPRTCT register for specific details. Read only.
ALRTTEMP	12	Die Overtemperature Fault Alert Indicates that T_{DIE} > 115°C (120°C typical). Cleared only by writing to logic zero. Writing to a logic one has no effect. If a thermal alert occurs during an Automated Cell Balancing or Discharge operation, the operation will end and issue CBACTIVE=11 and ALRTCBTEMP, notifying the user of the termination.
ALRTSCANTIMEOUT	11	Scan Time Out Alert 0 = Scan not requested or progressing normally (default) 1 = Scan operation halted due to Timeout fault ALRTSCANTIMEOUT is a copy of SCANTIMEOUT. This alert is automatically enabled if SCANTODIS=0. Cleared only by writing SCANCTRL:SCANTIMEOUT to zero. Read only.
ALRTADCZS	3	ADC Zero-Scale BIST Alert 0 = ADC Zero-Scale BIST Passed 1 = ADC Zero-Scale BIST Failed Reports the result of the ADC Zero-Scale BIST measurement performed during the last acquisition. Tests the SAR ADC DAC, Comparator, and logic components. Enabled using ADCZSFSEN. Cleared only by writing to logic zero. Writing to a logic one has no effect. *Note: If detailed results are desired, use the Zero-Scale ADC Detailed Diagnostic.*

BITFIELD	BITS	DESCRIPTION
ALRTADCFS	2	ADC Full-Scale BIST Alert 0 = ADC Full-Scale BIST Passed 1 = ADC Full-Scale BIST Failed Reports the result of the ADC Full-Scale BIST measurement performed during the last acquisition. Tests the SAR ADC DAC, Comparator, and logic components. Enabled using ADCZSFSEN. Cleared only by writing to logic zero. Writing to a logic one has no effect. *Note: If detailed results are desired, use the Full-Scale ADC Diagnostic.*
ALRTCOMPACCOV	1	End-of-Sequence Comparator Accuracy Diagnostic Over Voltage Alert 0 = COMP Accuracy OV Test Passed 1 = COMP Accuracy OV Test Failed Result of the end-of-sequence comparator accuracy over voltage diagnostic if enabled (SCANCFG=001 or 010, and COMPACCEN=1). Cleared only by writing to logic zero. Writing to a logic one has no effect.
ALRTCOMPACCUV	0	End-of-Sequence Comparator Accuracy Diagnostic Under Voltage Alert 0 = COMP Accuracy UV Test Passed 1 = COMP Accuracy UV Test Failed Result of the end-of-sequence comparator accuracy under voltage diagnostic if enabled (SCANCFG=001 or 010, and COMPACCEN=1). Cleared only by writing to logic zero. Writing to a logic one has no effect.

ALRTSUM (0x7)

ALRTSUM is a read accessible register which relates added, detailed information on the current status of the device, breaking out several summary bits in STATUS1.

BIT	15	14	13	12	11	10	9	8
Field	ALRTADCOVST	ALRTCOMPOVST	ALRTADCUVST	ALRTCOMPUVST	ALRTADCAUXOVST	ALRTCOMPAUXOVST	ALRTADCAUXUVST	ALRTCOMPAUXUVST
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BIT	7	6	5	4	3	2	1	0
Field	ALRTCSAOV	ALRTCSAUV	–	ALRTCALOSADC	ALRTCALOSR	ALRTCALOSTHRM	ALRTCALGAINP	ALRTCALGAINR
Reset	0b0	0b0	–	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
ALRTADCOVST	15	Cell ADC Overvoltage Alert Status Summary Bit-wise logical OR of ALRTOV[14:1], based on ADC measurements. Cleared on next acquisition, if all enabled overvoltage conditions are resolved. Read-only.

BITFIELD	BITS	DESCRIPTION
ALRTCOMPOVST	14	Comparator Cell Overvoltage Alert Status Summary Bit-wise logical OR of ALRTCOMPOV[14:1], based on redundant comparator monitoring. Cleared on next acquisition, if all enabled overvoltage conditions are resolved. Read-only.
ALRTADCUVST	13	Cell ADC Undervoltage Alert Status Summary Bit-wise logical OR of ALRTUV[14:1], based on ADC measurements. Cleared on next acquisition, if all enabled undervoltage conditions are resolved. Read-only.
ALRTCOMPUVST	12	Comparator Cell Undervoltage Alert Status Summary Bit-wise logical OR of ALRTCOMPUV[14:1], based on redundant comparator monitoring. Cleared on next acquisition, if all enabled undervoltage conditions are resolved. Read-only.
ALRTADCAUXOVST	11	Auxiliary ADC Overvoltage (Cold) Alert Status Summary Logical OR of ALRTAUXOV[5:0], based on ADC measurements. Cleared on next acquisition, if all enabled overvoltage conditions are resolved. Read-only.
ALRTCOMPAUXOVST	10	Comparator Auxiliary Overvoltage (Cold) Alert Status Summary Logical OR of ALRTCOMPAUXOV[5:0], based on redundant comparator monitoring. Cleared on next acquisition, if all enabled overvoltage conditions are resolved. Read-only.
ALRTADCAUXUVST	9	Auxiliary ADC Undervoltage (Hot) Alert Logical OR of ALRTAUXUV[5:0], based on ADC measurements. Cleared on next acquisition, if all enabled undervoltage conditions are resolved. Read-only.
ALRTCOMPAUXUVST	8	Comparator Auxiliary Undervoltage (Hot) Alert Status Summary Logical OR of ALRTCOMPAUXUV[5:0], based on redundant comparator monitoring. Cleared on next acquisition, if all enabled undervoltage conditions are resolved. Read-only.
ALRTCSAOV	7	Current Sense Amplifier Overvoltage (High Charge Current) Alert Inidcates the latest CSA measurement was above the threshold set by CSAOVTHSET. Cleared on next CSA voltage acquisition, if condition is resolved. Read-only.
ALRTCSAUV	6	Current Sense Amplifier Undervoltage (High Discharge Current) Alert Inidcates the latest CSA measurement was below the threshold set by CSAUVTHSET. Cleared on next CSA voltage acquisition, if condition is resolved. Read-only.

BITFIELD	BITS	DESCRIPTION
ALRTCALOSADC	4	ADC Offset Calibration Alert 0 = ADC Offset Calibration Valid 1 = ADC Offset Calibration Fault ALRTCALOSADC indicates the ADC offset calibration operation returned a result outside expected boundaries. Cleared when a later calibration operation or write to CALOSADC returns an expected result. Read only.
ALRTCALOSR	3	Ramp LSA + ADC Offset Calibration Alert 0 = LSA + ADC Offset Calibration Valid 1 = LSA + ADC Offset Calibration Fault ALRTCALOSR indicates the LSA + ADC offset calibration operation returned a result outside expected boundaries. Cleared when a later calibration operation or write to CALOSR returns an expected result. Read only.
ALRTCALOSTHRM	2	ADC Ratiometric Offset Calibration Alert 0 = Ratiometric ADC Offset Calibration Valid 1 = Ratiometric ADC Offset Calibration Fault ALRTCALOSTHRM indicates the ratiometric ADC offset calibration operation returned a result outside expected boundaries. Cleared when a later calibration operation or write to CALOSTHRM returns an expected result. Read only.
ALRTCALGAINP	1	Pyramid Gain Calibration Alert 0 = Pyramid Gain Calibration Valid 1 = Pyramid Calibration Fault ALRTCALGAINP indicates the gain calibration operation returned a result outside expected boundaries. Cleared when a later calibration operation or write to CALGAINP returns an expected result. Read only.
ALRTCALGAINR	0	Ramp Gain Calibration Alert 0 = Ramp Gain Calibration Valid 1 = Ramp Calibration Fault ALRTCALGAINR indicates the gain calibration operation returned a result outside expected boundaries. Cleared when a later calibration operation or write to CALGAINR returns an expected result. Read only.

ALRTOVCELL (0x8)

ALRTOVCELL is a read accessible register which relates current information on cell over voltage fault alerts based on ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	–	–	ALRTOV[14:9]					
Reset	–	–	0x0000					
Access Type	–	–	Read Only					

BIT	7	6	5	4	3	2	1	0
Field	ALRTOV[8:1]							
Reset	0x0000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ALRTOV	13:0	Cell Overvoltage Fault Alert ALRTOV[n] indicates V_{CELLN} > V_{OV} (OVTHSET threshold for POLARITY = 0, BIPOVTHSET for POLARITY =1); evaluated/enabled if OVALRTEN[n]=1. Cleared on next acquisition, if the overvoltage condition is resolved. Read only.

ALRTUVCELL (0x9)

ALRTOVCELL is a read accessible register which relates current information on cell under voltage fault alerts based on ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	–	–	ALRTUV[14:9]					
Reset	–	–	0x0000					
Access Type	–	–	Read Only					

BIT	7	6	5	4	3	2	1	0
Field	ALRTUV[8:1]							
Reset	0x0000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ALRTUV	13:0	Cell Undervoltage Fault Alert ALRTOV[n] indicates V_{CELLN} < V_{UV} (UVTHSET threshold for POLARITY = 0, BIPUVTHSET for POLARITY =1); evaluated/enabled if UVALRTEN[n]=1. Cleared on next acquisition, if the undervoltage condition is resolved. Read only.

MINMAXCELL (0xA)

MINMAX is a read accessible register which relates the cell locations with the highest and lowest values measured.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	MAXCELL[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Read Only			

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	MINCELL[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
MAXCELL	11:8	Maximum Voltage Cell Cell number [14:1] of the maximum cell voltage enabled/observed (for all CELLENn=1) in the last scan (SCAN=1) based on ALU/IIR data as selected by RDFILT. This bitfield is not updated for data requests made with SCAN=0. If multiple cells have the same maximum value, this field contains the lowest cell number reporting that result. *Note: This operation works on Unipolar or Bipolar measurement sets, as selected by MINMAXPOL. If MINMAXPOL is set such that no measurements in the scan meet the criteria (ex. MINMAXPOL = 1 (Bipolar), but POLARITY[14:1] = 0000h), a result of Fh will be returned (indicating no valid result was found).* Read only.
MINCELL	3:0	Minimum Voltage Cell Cell number [14:1] of the minimum cell voltage enabled/observed (for all CELLENn=1) in the last scan (SCAN=1) based on ALU/IIR data as selected by RDFILT. This bitfield is not updated for data requests made with SCAN=0. If multiple cells have the same minimum value, this field contains the lowest cell number reporting that result. *Note: This operation works on Unipolar or Bipolar measurement sets, as selected by MINMAXPOL. If MINMAXPOL is set such that no measurements in the scan meet the criteria (ex. MINMAXPOL = 1 (Bipolar), but POLARITY[14:1] = 0000h), a result of Fh will be returned (indicating no valid result was found).* Read only.

ALRTAUXPRTCTREG (0xB)

ALRTAUXPRTCT is a read accessible register which relates current information on auxiliary input protection fault alerts.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	ALRTAUXPRTCT[3:0]			
Reset	–	–	–	–	0x00			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
ALRTAUXPRTCT	3:0	Auxiliary Protection Fault Alert ALRTAUXPRTCT[n] indicates $V_{AUX[n]} > V_{AA}$; the alert is evaluated/enabled on each AUX/GPIO pin configured as an AUXINn input (see AUXGPIOCFG). Once the fault condition is detected on a pin, the AUX[n] input switch is disabled to protect internal circuitry. AUX[n] measurements and alerts for that pin will be invalid until proper operating conditions are restored. Cleared only if the condition is resolved upon a retry, or if the affected pin is no longer configured as an AUXINn input (disabling the protection circuit). In order to retry AUX operation and clear the fault condition, re-write the desired configuration to the AUXGPIOCFG register (it is not necessary to toggle the configuration). Read only.

ALRTAUXOVREG (0xC)

ALRTAUXOV is a read accessible register which relates current information on auxiliary over voltage (cold) fault alerts.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	ALRTAUXOV[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
ALRTAUXOV	3:0	Auxiliary Overvoltage (Cold) Fault Alert ALRTAUXOV[n] indicates $V_{AUXINn} > V_{AUXOVTHSET}$; evaluated/enabled if AUXOVALRTEN[n]=1. Cleared on next acquisition, if the over-voltage condition is resolved. Read only.

ALRTAUXUVREG (0xD)

ALRTAUXUV is a read accessible register which relates current information on auxiliary under voltage fault (hot) alerts.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	ALRTAUXUV[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
ALRTAUXUV	3:0	Auxiliary Undervoltage (Hot) Fault Alert ALRTAUXUV[n] indicates $V_{AUXINn} < V_{AUXUVTHSET}$; evaluated/enabled if AUXUVALRTEN[n]=1. Cleared on next acquisition, if the under-voltage condition is resolved. Read only..

ALRTCOMPOVREG (0xE)

ALRTCOMPOV is a read accessible register which relates current information on cell over voltage fault alerts based on the redundant comparator.

BIT	15	14	13	12	11	10	9	8
Field	–	–	ALRTCOMPOV[14:9]					
Reset	–	–	0x0000					
Access Type	–	–	Read Only					

BIT	7	6	5	4	3	2	1	0
Field	ALRTCOMPOV[8:1]							
Reset	0x0000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ALRTCOMPOV	13:0	Cell Overvoltage Fault Comparator Alert ALRTCOMPOV[n] indicates $V_{CELL[n]} > V_{COMPOVTH}$ (Comparator Over Voltage Threshold); evaluated/enabled if OVALRTEN[n]=1. Cleared on next comparator acquisition, if the overvoltage condition is resolved. Read only.

ALRTCOMPUVREG (0xF)

ALRTCOMPUV is a read accessible register which relates current information on cell under voltage fault alerts based on the redundant comparator.

BIT	15	14	13	12	11	10	9	8
Field	–	–	ALRTCOMPUV[14:9]					
Reset	–	–	0x0000					
Access Type	–	–	Read Only					

BIT	7	6	5	4	3	2	1	0
Field	ALRTCOMPUV[8:1]							
Reset	0x0000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ALRTCOMPUV	13:0	Cell Undervoltage Fault Comparator Alert ALRTCOMPUV[n] indicates $V_{CELL[n]} < V_{COMPUVTH}$ (Comparator Under Voltage Threshold); evaluated/enabled if UVALRTEN[n]=1. Cleared on next comparator acquisition, if the undervoltage condition is resolved. Read only.

ALRTCOMPAUXOVREG (0x10)

ALRTCOMPAUXOV is a read accessible register which relates current information on auxiliary over voltage fault (cold) alerts based on the redundant comparator.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	ALRTCOMPAUXOV[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
ALRTCOMPAUXOV	3:0	Auxiliary Overvoltage (Cold) Fault Comparator Alert ALRTCOMPAUXOV[n] indicates $V_{AUXINn} > V_{COMPOVTH}$ (Comparator Overvoltage Threshold, Cold); evaluated/enabled if AUXOVALRTEN[n]=1. Cleared on next comparator acquisition, if the over-voltage condition is resolved. Read only.

ALRTCOMPAUXUVREG (0x11)

ALRTCOMPAUXUV is a read accessible register which relates current information on auxiliary under voltage fault (hot) alerts based on the redundant comparator.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	ALRTCOMPAUXUV[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
ALRTCOMPAUXUV	3:0	Auxiliary Under Voltage (Hot) Fault Comparator Alert ALRTCOMPAUXUV[n] indicates $V_{AUXINn} < V_{COMPUVTH}$ (Comparator Under Voltage Threshold, Hot); evaluated/enabled if AUXUVALRTEN[n]=1. Cleared on next acquisition, if the under-voltage condition is resolved. Read only.

ALRTBALSWREG (0x12)

ALRTBALSW is a read accessible register which relates current summary information on balancing switch fault alerts.

BIT	15	14	13	12	11	10	9	8
Field	–	–	ALRTBALSW[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Read Only					

BIT	7	6	5	4	3	2	1	0
Field	ALRTBALSW[7:0]							
Reset	0x0000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ALRTBALSW	13:0	Balance Switch Fault Alert ALRTBALSW[n] indicates the corresponding measurement result fails the threshold specified by the Balance Switch Diagnostic modes (SCANCFG = 100 through 111). Testing and faults above the TOPCELL1/2 position are automatically masked out of this register (see PACKCFG:TOPCELL1&2 for complete details). Cleared on next acquisition if the condition is resolved. Read only.

SWACTION (0x13)

SWACTION is a read and write accessible register which contains bits allowing software exit and reset requests. These requests are not recommended for general use, but may be of use in case of error.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	SWPOR
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read, Pulse

BITFIELD	BITS	DESCRIPTION
SWPOR	0	Software POR Request 0 = Normal Operation (default, no effect) 1 = Initiates Software POR event Always reads logic zero.

DEVCFG1 (0x14)

DEVCNFG1 is a read and write accessible register which governs the configuration of the device interface operation.

BIT	15	14	13	12	11	10	9	8
Field	UARTCFG[1:0]		TXUIDLEHIZ	TXLIDLEHIZ	ADAPTTXEN[1:0]		ALIVECNTEN	UARTHOST
Reset	0b11		0b0	0b0	0b00		0b0	0b1
Access Type	Write, Read, Ext		Write, Read, Ext	Write, Read, Ext	Write, Read, Ext		Write, Read, Ext	Read Only

BIT	7	6	5	4	3	2	1	0
Field	SFTYCSB	SFTYSCLK	SFTYSDI	SPIDRVINT	DEVCFG1RSRV	NOPEC	ALERTEN	DBLBUFEN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read	Write, Read, Ext	Write, Read, Ext	Write, Read

BITFIELD	BITS	DESCRIPTION
UARTCFG	15:14	UART Interface Configuration 00 - Single UART Interface with External Loopback 01 - Single UART Interface with Internal Loopback 10 - Single UART Interface with Differential Alert Interface 11 - Dual UART Interface (default) Single UART options with Loopback (modes 0x): the UART Up path is used for read and write commands and the Down path is used as a return (pass-through) path. If an internal loopback path is desired, the internal shunt should only be engaged on the last device in the chain using mode 01. Alert Interface is Single-Ended (using the ALERTIN and ALERTOUT pins) since the Down path is engaged for UART communications. Single UART with Differential Alert Interface (mode 10): the UART Up path is used for read and write commands with a direct wire return path from the last device in the chain to the uC. The Down path is used as a differential Alert path. The single ended ALERT interface path is disabled - the ALERTOUT port will idle HIZ, and the ALERTIN port will be disabled. Dual UART Interface: both the Up and Down Interfaces are used for UART communication. Only the Host path (selected using UPHOST or DOWNHOST commands, and indicated by HOSTUART) accepts write commands, while both paths can accept read commands. Alert Interface is Single-Ended (using the ALERTIN and ALERTOUT pins) since the Down path is engaged for UART communications. For all the above options, the UART Up path uses the RXL->TXU ports, and the Down UART path ususes the TXL->RXU ports. These bits have no effect if UARTSEL is set low (SPI interface enabled). This bitfield is unaffected in the event of a SWPOR (Software POR) request by the Host. *Note: The device hardware must be pre-configured to support the correct operational mode. The device powers up in the Dual UART mode to ensure any hardware configuration can configure the device. If the incorrect operating mode is configured, the UART Master should cease communications (and possibly issue a FORCEPOR) to reset the device to default status via SHDNL assertion.*
TXUIDLEHIZ	13	UART Upper TX Idle Mode Selection 0 = TXU Drivers idle in logic zero (default) 1 = TXU Drivers idle in High-Z Leave in default state for normal operation. This bit has no effect if UARTSEL is set low. This bitfield is unaffected in the event of a SWPOR (Software POR) request by the Host.

BITFIELD	BITS	DESCRIPTION
TXLIDLEHIZ	12	UART Lower TX Idle Mode Selection 0 = TXL Drivers idle in logic zero (default) 1 = TXL Drivers idle in High-Z Leave in default state for normal operation. This bit has no effect if UARTSEL is set low. This bitfield is unaffected in the event of a SWPOR (Software POR) request by the Host.
ADAPTTXEN	11:10	UART Adaptive Transmission Enable 00 = Adaptive Transmission Off (default) 01 = Enable UP Path Adaptive Transmission on TXU 10 = Enable DN Path Adaptive Transmission on TXL 11 = Unsupported - Adaptive Transmission Off Selections should only be made on device(s) at the end of UP/DN path(s) which transmit directly to the uC/uP. This bit has no effect if UARTSEL is set low. This bitfield is unaffected in the event of a SWPOR (Software POR) request by the Host.
ALIVECNTEN	9	Enable UART Interface Alive-Counter 0 = Do not send alive counter byte (defualt) 1 = Enables inclusion of alive-counter byte at end of all write and read packets.
UARTHOST	8	UART Host Mode Indicator Bit 0 = UART Down Path is Host 1 = UART Up Path is Host (default) Signfies which UART Path is currently configured as the host. Down host mode is only accessible if UARTCFG=DUAL (11). The host mode is selected using UPHOST and DOWNHOST commands. This bit has no meaning if UARTSEL is set low, and will always read back one. Read only. This bitfield is unaffected in the event of a SWPOR (Software POR) request by the Host.
SFTYCSB	7	SPI CSB Safety Pullup Enable 0 = CSB Pullup Disabled (default) 1 = CSB Pullup Enabled Determines if 100kΩ safety pullup to V_{DDL2} is enabled on the CSB interface input pin. This bit has no effect if UARTSEL is set high. This bitfield is unaffected in the event of a SWPOR (Software POR) request by the Host.

BITFIELD	BITS	DESCRIPTION
SFTYSCLK	6	SPI SCLK Safety Pulldown Enable 0 = SCLK Pulldown Disabled (default) 1 = SCLK Pulldown Enabled Determines if 100kΩ safety pulldown to GND is enabled on the SCLK interface input pin. This bit has no effect if UARTSEL is set high. This bitfield is unaffected in the event of a SWPOR (Software POR) request by the Host.
SFTYSDI	5	SPI SDI Safety Pulldown Enable 0 = SDI Pulldown Down Enabled Determines if 100kΩ safety pulldown to GNDL2/3 is enabled on the SDI interface input pin. This bit has no effect if UARTSEL is set high. This bitfield is unaffected in the event of a SWPOR (Software POR) request by the Host.
SPIDRVINT	4	SPI IRQB Output Drive Mode 0 = Open Drain nMOS (default) 1 = CMOS Drive Determines drive mode for SPI IRQB function on ALERTOUT pin. This bit has no effect if UARTSEL is set high. This bitfield is unaffected in the event of a SWPOR (Software POR) request by the Host.
DEVCFG1RSRV	3	Reserved. Reads back the value written.
NOPEC	2	UART/SPI PEC/CRC Disable 0 = PEC/CRC Enabled (default) 1 = PEC/CRC Disabled Determines if Packet Error Checking is enforced using the UART interface and if Cyclic Redundancy Checking is enforced using the SPI interface. If this bit is set, the PEC characters should be omitted from the UART packet/command (UARTSEL=1), and the incoming CRC bits will be ignored during SPI transactions (UARTSEL=0).

BITFIELD	BITS	DESCRIPTION
ALERTEN	1	Alert Interface Enable 0 = Alert Interface is Disabled (Default) 1 = Alert Interface Enabled If Disabled, the following conventions apply: If UARTSEL=1 and UARTCFG=0x or 11 (Single Ended Alert), the ALERTOUT port will idle HiZ and the ALERTIN port will be disabled/ignored. If UARTSEL=1 and UARTCFG=10 (Differential Alert), the UART Down Path will idle as set by TXLIDLEHIZ. If UARTSEL=0 (SPI), the ALRTOUT pin will idle high with drive determined by SPIDRVINT. The ALERTIN pin will be disabled/ignored in SPI mode (no shoot through current will result if the pin is floated). This bit is unaffected in the event of SWPOR (Soft POR) request by Host. If Enabled, the following conventions apply: If UARTSEL=1, the device will initiate alerts based on STATUS1 content, as well as pass through any alerts received from/to the daisy chain. If UARTSEL=0 (SPI), the part will generate active low alerts based on STATUS1 content with drive determined by SPIDRVINT. The ALERTIN pin will be disabled and ignored in SPI mode (no shoot through current will result if the pin is floated).
DBLBUFEN	0	Double Buffer Mode Enable 0 = Normal Operation (default) 1 = Double Buffered Operation Enables the double-buffer mode. This mode automatically transfers data from the ALU/IIR to the data registers at the start of the next acquisition instead of at the end of an acquisition. *This mode may be used so the host can start a second acquisition and then begin reading the data from the first acquisition (during the second acquisition). This works even if the first data read transactions take longer than the second acquisition to complete; simply hold off on a third acquisition until the first acquistion data is retrieved. Launching a third acquisition will move the data from the second acquistion to the data registers for readback during the third acquisition, and so forth...*

DEVCFG2 (0x15)

DEVCNFG2 is a read and write accessible register which governs the configuration of the device filtering, several top level diagnostic modes, and timeout monitors.

BIT	15	14	13	12	11	10	9	8
Field	IIRFC[2:0]			–	DEVCFG2RSRV[3:0]			
Reset	0b010			–	0b0000			
Access Type	Write, Read			–	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	–	HVCPDIS	FORCEPOR	ALERTDCTSTEN	–	SPITODIS	SCANTODIS	CBTODIS
Reset	–	0b0	0b0	0b0	–	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
IIRFC	15:13	IIR Filter Coefficient Selection 000 = 0.125 001 = 0.250 010 = 0.375 (default) 011 = 0.500 100 = 0.625 101 = 0.750 110 = 0.875 111 = 1.000 (filter off) This setting determines the wieght of the current measurement result vs. the previously accumulated results in the IIR filter. A setting of 1.0 effectively disables the filter.
DEVCFG2RSRV	11:8	Reserved. Reads back the value written.
HVCPDIS	6	HV Charge Pump Disable 0 = Normal Operation (default) 1 = Disable HV Charge Pump Used for ALRTHVUV diagnostic. If the HV charge pump is disabled in normal operation, measurement errors will result due to V_{HV} under-voltage condition.
FORCEPOR	5	Force POR Event 0 = Normal Operation (default) 1 = Enables hard POR by pulling down SHDNL internally. If cleared before the POR occurs, the active pull-down on SHDNL will be removed. *Note: This bit is used to accelerate a complete POR event issued by SHDNL falling. In UART applications, it is possible continued UART activity will fight or overcome the SHDNL pull down. For best results, cease UART communications when using this mode.*
ALERTDCTSTEN	4	UART Alert DC Diagnostic Test Enable 0 = UART Alert DC Testing Disabled (Default) 1 = UART Alert DC Testing Enabled Used to place the ALRTOUT pin in a DC diagnostic mode for use in testing for shorts to GPIO/AUX0. If Enabled while UARTSEL=1, the ALRTOUT pin will be driven low if an Alert condition is present, and driven high otherwise. ALRTUSER can be written to exercise ALRTOUT in either direction. Neighboring pins such as AUX/GPIO[0] can be monitored directly or in diagnostic modes to detect a fault. This function works in all UARTCFG modes, including 10 (Differential Alert), which does not normally use the ALRTOUT pin. This setting has no impact in SPI mode (UARTSEL=0), the same functionality can be realized using SPIDRVINIT and ALRTUSER.

BITFIELD	BITS	DESCRIPTION
SPITODIS	2	SPI Time Out Disable 0 = SPI Time Out Enabled (default) 1 = SPI Time Out Disabled Determines if SPI time out monitor function is enabled.This bit has no effect if UARTSEL is set high.
SCANTODIS	1	Scan Time Out Disable 0 = Normal Operation (default) 1 = Disables the acquisition watchdog but does not clear the SCANTIMEOUT flag in the SCANCTRL register if it is set.
CBTODIS	0	Cell Balancing Time Out Disable 0 = Normal Operation (default) 1 = Disables the cell balancing watchdog but does not clear the ALRTCBTIMEOUT flag in the STATUS3 register if it was previously set.

AUXGPIOCFG (0x16)

AUXGPIOCFG is a read and write accessible register which governs the configuration of the AUX/GPIO multifunction pins.

BIT	15	14	13	12	11	10	9	8
Field	I2CEN	–	–	–	GPIOEN[3:0]			
Reset	0b0	–	–	–	0xF			
Access Type	Write, Read, Ext	–	–	–	Write, Read, Ext			

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	GPIODIR[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read, Ext			

BITFIELD	BITS	DESCRIPTION
I2CEN	15	Digital I^2C Mode Enable 0 = Normal Configured Operation (default) 1 = I^2C Master Operation If I2CEN is set high, AUX/GPIO[0] is configured as the SDA open-drain I/O and AUX/GPIO[1] is configured as the SCL open-drain output driver for use as an I^2C Master. If this bit is set, all remaining selections in AUXGPIOCFG, GPIO, and MEASUREEN2 will be ignored for AUX/GPIO[1:0].
GPIOEN	11:8	Digital GPIO Mode Enable 0 = Analog Input (AUX) Mode (High-Z) 1 = Digital GPIO Mode (default) GPIOEN[n] configures the corresponding AUX/GPIO[n] pin for operation in the selected mode. *Note: if I2CEN=1, GPIOEN[1:0] are ignored, but will still readback the user setting.*

BITFIELD	BITS	DESCRIPTION
GPIODIR	3:0	Digital GPIO Direction Selection 0 = Digital Input Mode (High-Z, default) 1 = Digital Output Mode GPIODIR[n] configures the direction of the corresponding AUX/GPIO[n] pin. This setting is only applicable if GPIOEN[n] = 1 (Digital GPIO Mode enabled). In digital input mode (GPIOEN=1 and GPIODIR=0), a 2MΩ pulldown (R_{GPIO}) will be enabled to prevent the GPIO input from floating. In digital output mode (GPIOEN=1 and GPIODIR=1), the GPIO input circuitry will continue to operate, allowing direct observation of the port staus. *Note: if I2CEN=1, GPIODIR[1:0] is ignored, but will still readback the user setting.*

GPIOCFG (0x17)

GPIO is a read and write accessible register which governs the output state of GPIO outputs and reads back the input state of GPIO inputs.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	GPIODRV[3:0]			
Reset	–	–	–	–	0b0			
Access Type	–	–	–	–	Write, Read, Ext			

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	GPIORD[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
GPIODRV	11:8	Digital GPIO Output State 0 = Output Logic Zero (default) 1 = Output Logic One GPIODRV[n] sets the output logic state direction of the corresponding AUX/GPIO[n] pin. This setting is only applicable if GPIOEN[n] = 1 and GPIODIR[n] = 1 (Digital GPIO Output Mode enabled). *Note: if I2CEN=1, GPIODRV[1:0] is ignored, but will still readback the user setting.*

BITFIELD	BITS	DESCRIPTION
GPIORD	3:0	Digital GPIO Input State Indicator 0 = Logic Zero (default) 1 = Logic One GPIORD[n] indicates the current logic state of each active GPIO[n] input buffer. Data is only relevant if GPIOEN[n] = 1 (all Digital GPIO pins are monitored in Input or Output mode), otherwise zero will be read back. For UART, the logic state is sampled at the end of the parity bit of the register address byte during a read transaction. For SPI, the logic state is sampled in response to the 9th SCLK rising edge during a read transaction. Read only. *Note: if I2CEN=1, GPIORD[1:0] is no longer valid, and will readback 00.*

PACKCFG (0x18)

PCKCFG is a read and write accessible register which configures the part such that the top most cell and block used in the application is known. Details of Flex Pack applications are also configured within this register.

BIT	15	14	13	12	11	10	9	8
Field	FLXPCKEN2	FLXPCKEN1	FLXPCKSCAN	–	TOPBLOCK[3:0]			
Reset	0b1	0b1	0b1	–	0xF			
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	TOPCELL2[3:0]				TOPCELL1[3:0]			
Reset	0xF				0xF			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
FLXPCKEN2	15	Flex Pack Enable 2 0 = Flex Pack functions disabled 1 = Flex Pack selection of Top Cell and Top Block Enabled (default) Indicates the Flexible Pack Support is engaged (DCINMUX and VBLKMUX), selecting the internal power and block routing path when the DCIN pin is not supplied externally. This selection is protected by a redundant bitfield. FLXPCKEN1 & FLXPCKEN2 must agree, resulting in a valid internal FLXPCKEN1/2 selection. If the two bitfields do not agree, the internal FLXPCKEN1/2 selection will be mapped to 1 (enabled, default) and DCINMUX selection will be mapped to the OFF position. SWn selection is determined by TOPCELL1/2 (based on TOPCELL1&2). Valid selections range from Cell 8 (0x8) to Cell 14 (0xE). If an unsupported selection (0x0 to 0x7, 0xF) is made in TOPCELL1/2, the DCINMUX selection switches are disabled, but the DCINMUX common switch is enabled (this is the default condition). In this condition, DCIN is initially pulled to a diode below the highest SWn input and there is no interference if DCIN is externally supplied. Block selection is determined by TOPBLOCK. Valid cell selections range from Cell 8 (0x8) to Cell 14 (0xE). If an unsupported selection (0x0~0x7, 0xF) is made in TOPBLOCK, the VBLKP port is selected.
FLXPCKEN1	14	Flex Pack Enable 1 (Redundant Bitfield) 0 = Flex Pack functions disabled 1 = Flex Pack selection of Top Cell and Top Block Enabled (default) See FLXPCKEN2 for complete details on operation and redundant bitfield checking.
FLXPCKSCAN	13	Flex Pack Scan Configuration 0 = Flex Pack ALTMUX scan unmodified 1 = Flex Pack ALTMUX scan modifed with additional 30µs delay before acquistion of TOPCELL1/2 (default) FLEXPCKSCAN will configure the measurement sequence such that for any scan with ALTMUXSEL=1, there will be 30µs delay prior to sampling the TOPCELL1/2 voltage regardles of SCANMODE. This delay affords the SW[TOPCELL1/2] input time to settle for an accurate diagnostic measurement when DCIN loading is temporarily suspended in Flex Pack configrations. Impacts scan sequences where FLXPCKEN1/2=1 and TOPCELL1/2 is set to a supported value (0x8 to 0xE), and ALTMUXSEL=1 (effective value). Ignored otherwise.

BITFIELD	BITS	DESCRIPTION
TOPBLOCK	11:8	Top Block Selection Configures the top block position if a selection other than the VBLK pin is chosen. Used to properly determine the connection point for the VBLOCK resistive divider. TOPBLOCK[3:0] selects the Cn pin to be connected to the VBLOCK resistive divider. 0xF (default) selects the VBLK pin. Selections 0x0 through 0x7 are not supported and will be mapped to 0xF (VBLK, default). TOPBLOCK may differ from TOPCELL1/2 if there are Bus Bars installed in channels above the Top Cell. TOPBLOCK is ignored if FLXPCKEN1/2=0.
TOPCELL2	7:4	Top Cell Selection 2 Configures the top cell position if less than 14 channels are used. Used to properly mask the ALRTBALSW diagnostic alerts (always) and to make DCINMUX selections when FLXPCKEN1/2=1. This selection is protected by a redundant bitfield. TOPCELL1 & TOPCELL2 must agree, resulting in a valid internal TOPCELL1/2 selection. If the two bitfields do not agree, no ALRTBALSW alerts are masked, and the internal DCINMUX selection will be mapped to the OFF position. 0xF (default) removes all ALRTBALSW masking, and places DCINMUX in the OFF position. Flex Pack Behavior TOPCELL1/2 selects the SW pin to be connected to the DCIN pin. Selections 0x8 to 0xE map to SW[8] to SW[14]. Selections 0x0 to 0x7 and 0xF are not supported and will be mapped to an OFF position. In the OFF position, DCIN is initially pulled to a diode below the highest SWn input. Masking Behavior TOPCELL1/2 also sets masking behavior in ALRTBALSW diagnostics. All selections are supported for this function.
TOPCELL1	3:0	Top Cell Selection 1 (Redundant Bitfield) Configures the top cell position if less than 14 channels are used. Used to properly mask the ALRTBALSW diagnostic alerts (always) and to make DCINMUX selections when FLXPCKEN1/2=1. See TOPCELL2 for complete details on operation and redundant bitfield checking.

ALRTIRQEN (0x19)

ALRTIRQEN is a read and write accessible register which selects which STATUS1 alerts trigger interrupts via the ALERT interface port(s), and are included in the DCByte and Alert Packet (UART) or ALERT bit (SPI) notifications. Note the information in the STATUS1 register itself (or any component terms rolled up into STATUS1) is not masked/disabled by these settings, allowing the underlying data to always be available via STATUS1 readback.

BIT	15	14	13	12	11	10	9	8
Field	SCANALRTEN	–	MSMTCHALRTEN	CELLOVSTALRTEN	CELLUVSTALRTEN	BLKOVSTALRTEN	BLKUVSTALRTEN	AUXOVSTALRTEN
Reset	0b0	–	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	AUXUVSTALRTEN	CSASTALRTEN	PECALRTEN	INTRFCALRTEN	CALALRTEN	CBALALRTEN	FMEA2ALRTEN	FMEA1ALRTEN
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read, Ext	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
SCANALRTEN	15	Scan Complete Alert Enable 0 = ALRTSCAN masked (default) 1 = ALRTSCAN enabled Disabled by default since this is not a safety feature, but a notification option. Applies to the Alert Interface only in order to support interrupt-driven applications; ALRTSCAN is never included in the UART DCByte & Alert Packet, or the SPI ALERT bit.
MSMTCHALRTEN	13	Cell Voltage Mismatch Alert Enable 0 = ALRTMSMTCH masked 1 = ALRTMSMTCH enabled (default) Applies to the Alert Interface, UART DCByte & Alert Packet, and SPI ALERT bit.
CELLOVSTALRTEN	12	Cell Overvoltage Status Summary Alert Enable 0 = ALRTCELLOVST masked 1 = ALRTCELLOVST enabled (default) Applies to the Alert Interface, UART DCByte & Alert Packet, and SPI ALERT bit.
CELLUVSTALRTEN	11	Cell Undervoltage Status Summary Alert Enable 0 = ALRTCELLUVST masked 1 = ALRTCELLUVST enabled (default) Applies to the Alert Interface, UART DCByte & Alert Packet, and SPI ALERT bit.
BLKOVSTALRTEN	10	Block Overvoltage Status Alert Enable 0 = ALRTBLKOVST masked 1 = ALRTBLKOVST enabled (default) Applies to the Alert Interface, UART DCByte & Alert Packet, and SPI ALERT bit.
BLKUVSTALRTEN	9	Block Undervoltage Status Alert Enable 0 = ALRTBLKUVST masked 1 = ALRTBLKUVST enabled (default) Applies to the Alert Interface, UART DCByte & Alert Packet, and SPI ALERT bit.
AUXOVSTALRTEN	8	Auxiliary Overvoltage Status Summary Alert Enable 0 = ALRTAUXOVST masked 1 = ALRTAUXOVST enabled (default) Applies to the Alert Interface, UART DCByte & Alert Packet, and SPI ALERT bit.

BITFIELD	BITS	DESCRIPTION
AUXUVSTALRTEN	7	Auxiliary Undervoltage Status Summary Alert Enable 0 = ALRTAUXUVST masked 1 = ALRTAUXUVST enabled (default) Applies to the Alert Interface, UART DCByte & Alert Packet, and SPI ALERT bit.
CSASTALRTEN	6	CSA Status Summary Alert Enable 0 = ALRTCSAST masked 1 = ALRTCSAST enabled (default) Applies to the Alert Interface, UART DCByte & Alert Packet, and SPI ALERT bit.
PECALRTEN	5	Packet Error Check (CRC) Alert Enable 0 = ALRTPEC masked 1 = ALRTPEC enabled (default) Applies to the Alert Interface, UART Alert Packet, and SPI ALERT bit; ALRTPEC is not included in the UART DCByte.
INTRFCALRTEN	4	Interface Specific Error Alert Enable 0 = ALRTINTRFC masked 1 = ALRTINTRFC enabled (default) Applies to the Alert Interface, UART DCByte & Alert Packet, and SPI ALERT bit.
CALALRTEN	3	Calibration Fault Alert Enable 0 = ALRTCAL masked 1 = ALRTCAL enabled (default) Applies to the Alert Interface, UART DCByte & Alert Packet, and SPI ALERT bit.
CBALALRTEN	2	Cell Balancing Status Alert Enable 0 = ALRTCBAL masked 1 = ALRTCBAL enabled (default) Applies to the Alert Interface, UART DCByte & Alert Packet, and SPI ALERT bit.
FMEA2ALRTEN	1	FMEA2 Condition Summay Alert Enable 0 = ALRTFMEA2 masked 1 = ALRTFMEA2 enabled (default) Applies to the Alert Interface, UART DCByte & Alert Packet, and SPI ALERT bit.
FMEA1ALRTEN	0	FMEA1 Condition Summary Alert Enable 0 = ALRTFMEA1 masked 1 = ALRTFMEA1 enabled (default) Applies to the Alert Interface, UART DCByte & Alert Packet, and SPI ALERT bit.

ALRTOVEN (0x1A)

ALRTOVEN is a read and write accessible register which enables over voltage fault checks on selected input channels during scans using either the ADC or Comparator.

BIT	15	14	13	12	11	10	9	8
Field	CSAOVALRTEN	BLKOVALRTEN	OVALRTEN[14:9]					
Reset	0b0	0b0	0x0000					
Access Type	Write, Read, Ext	Write, Read	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	OVALRTEN[8:1]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CSAOVALRTEN	15	CSA Overvoltage Fault Check Enable CSAOVALRTEN enables over voltage fault checking on CSA ADC measurements against threshold CSAOVTHSET. Comparator measurements are not supported for the CSA. Clearing also clears the associated CSA alert.
BLKOVALRTEN	14	Block Overvoltage Fault Check Enable BLKOVALRTEN enables over voltage fault checking on ADC Block measurements against threshold BLKOVTHSET. Clearing also clears the associated Block alert.
OVALRTEN	13:0	Overvoltage Fault Check Enable OVALRTEN[n] enables over voltage fault checking on CELL[n] against threshold OVTHSET (ADC) and COMPOVTH (Comparator). Clearing also clears the associated cell alert in ALRTOVCELL and ALRTCOMPOVREG.

ALRTUVEN (0x1B)

ALRTUVEN is a read and write accessible register which enables under voltage fault checks on selected input channels during scans using either the ADC or Comparator.

BIT	15	14	13	12	11	10	9	8
Field	CSAUVALRTEN	BLKUVALRTEN	UVALRTEN[14:9]					
Reset	0b0	0b0	0x0000					
Access Type	Write, Read, Ext	Write, Read	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	UVALRTEN[8:1]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CSAUVALRTEN	15	CSA Undervoltage Fault Check Enable CSA UVALRTEN enables under voltage fault checking on CSA ADC measurements against threshold CSAUVTHSET. Comparator measurements are not supported for the CSA. Clearing also clears the associated CSA alert.

BITFIELD	BITS	DESCRIPTION
BLKUVALRTEN	14	Block Undervoltage Fault Check Enable BLKUVALRTEN enables under voltage fault checking on ADC Block measurements against threshold BLKUVTHSET. Clearing also clears the associated Block alert.
UVALRTEN	13:0	Undervoltage Fault Check Enable UVALRTEN[n] enables under voltage fault checking on CELL[n] against threshold UVTHSET (ADC) and COMPUVTH (Comparator). Clearing also clears the associated cell alert in ALRTOVCELL and ALRTCOMPOVREG.

ALRTAUXOVEN (0x1C)

ALRTAUXOVEN is a read and write accessible register which enables auxiliary over voltage (cold) fault checks on selected Auxiliary channels during scans using either the ADC or Comparator.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AUXOVALRTEN[3:0]			
Reset	–	–	–	–	0x00			
Access Type	–	–	–	–	Write, Read, Ext			

BITFIELD	BITS	DESCRIPTION
AUXOVALRTEN	3:0	Auxiliary Overvoltage (Cold) Fault Check Enable AUXOVALRTEN[n] enables over voltage (cold) fault checking on AUX[n] against the ratiometric/absolute threshold AUXROVTHSET/AUXAOVTHSET (ADC) and COMPAUXROVTH/COMPAUXAOVTH (Comparator), as selected by AUXREFSEL[n]. Clearing also clears the associated alert. *Note: If the I2CEN bit (Digital I2C mode, applies to [1:0] only), or the respective GPIOEN bit is set (GPIO mode), this bit is ignored, but will still read back the user setting.*

ALRTAUXUVEN (0x1D)

ALRTAUXUVEN is a read and write accessible register which enables auxiliary under voltage (hot) fault checks on selected Auxiliary channels using either the ADC or Comparator.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AUXUVALRTEN[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read, Ext			

BITFIELD	BITS	DESCRIPTION
AUXUVALRTEN	3:0	Auxiliary Undervoltage (Hot) Fault Check Enable AUXUVALRTEN[n] enables undervoltage (hot) fault checking on AUX[n] against the ratiometric/absolute threshold AUXRUVTHSET/AUXAUVTHSET (ADC) and COMPAUXRUVTH/COMPAUXAUVTH (Comparator), as selected by AUXREFSEL[n]. Clearing also clears the associated alert. *Note: If the I2CEN bit (Digital I2C mode, applies to [1:0] only), or the respective GPIOEN bit is set (GPIO mode), this bit is ignored, but will still read back the user setting.*

ALRTCALTST (0x1E)

ALRTCALTST is a read and write accessible register which allow the user to force Calibration alerts to test readback and interrupt logic. The forced alert(s) will remain forced until this register is written back to zeros (assuming the existing calibration data is with range).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	CALOSADCALRTFRC	CALOSRALRTFRC	CALOSTHRMALRTFRC	CALGAINPALRTFRC	CALGAINRALRTFRC
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
CALOSADCALRTFRC	4	ADC Offset Calibration Alert Force 0 = ALRTCALOSADC normal operation (default) 1 = ALRTCALOSADC forced if unmasked Used to test alert functionality.
CALOSRALRTFRC	3	Ramp LSA + ADC Offset Calibration Alert Force 0 = ALRTCALOSR normal operation (default) 1 = ALRTCALOSR forced if unmasked Used to test alert functionality.
CALOSTHRMALRTFRC	2	Ratiometric ADC Offset Calibration Alert Force 0 = ALRTCALOSTHRM normal operation (default) 1 = ALRTCALOSTHRM forced if unmasked Used to test alert functionality.

BITFIELD	BITS	DESCRIPTION
CALGAINPALRTFRC	1	Pyramid Gain Calibration Alert Force 0 = ALRTCALGAINP normal operation (default) 1 = ALRTCALGAINP forced if unmasked Used to test alert functionality.
CALGAINRALRTFRC	0	Ramp Gain Calibration Alert Force 0 = ALRTCALGAINR normal operation (default) 1 = ALRTCALGAINR forced if unmasked Used to test alert functionality.

OVTHCLRREG (0x1F)

OVTHCLR is a read and write accessible register which selects the cell over voltage alert clear threshold used with unipolar ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	OVTHCLR[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	OVTHCLR[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
OVTHCLR	15:2	Unipolar Cell Overvoltage Alert Clear Threshold 14-bit threshold value at/below which ALRTOV alerts will be cleared/ deasserted for unipolar cell measurements. *Note: for proper operation, this value should always be less than or equal to OVTHSET.*

OVTHSETREG (0x20)

OVTHSET is a read and write accessible register which selects the cell over voltage alert set threshold used with unipolar ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	OVTHSET[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	OVTHSET[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
OVTHSET	15:2	Unipolar Cell Overvoltage Alert Set Threshold 14-bit threshold value above which ALRTOV alerts will be set/asserted for unipolar cell measurements. A value of 0x3FFF effectively disables over voltage checking.

UVTHCLRREG (0x21)

UVTHCLR is a read and write accessible register which selects the cell under voltage alert clear threshold used with unipolar ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	UVTHCLR[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	UVTHCLR[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
UVTHCLR	15:2	Unipolar Cell Undervoltage Alert Clear Threshold 14-bit threshold value at/above which ALRTUV alerts will be cleared/ deasserted for unipolar cell measurements. *Note: For proper operation, this value should always be greater than or equal to UVTHSET.*

UVTHSETREG (0x22)

UVTHSET is a read and write accessible register which selects the cell under voltage alert set threshold used with unipolar ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	UVTHSET[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	UVTHSET[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
UVTHSET	15:2	Unipolar Cell Undervoltage Alert Set Threshold 14-bit threshold value below which ALRTUV alerts will be set/asserted for unipolar cell measurements. A value of 0x0000 effectively disables under voltage checking.

MSMTCHREG (0x23)

MSMTCH is a read and write accessible register which selects the cell voltage mismatch alert threshold used with ADC cell scan measurements.

BIT	15	14	13	12	11	10	9	8
Field	MSMTCH[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	MSMTCH[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
MSMTCH	15:2	Cell Voltage Misimatch Alert Threshold 14-bit threshold value; if the difference between maximum and minimum cell voltages exceeds this value, ALRTMSMTCH will be set/asserted. Whether only unipolar ADC measurements (POLARITYn=0) are included in mismatch calculations or all measurements are included is determined by POLARITYCTRL:MINMAXPOL.

BIPOVTHCLRREG (0x24)

BIPOVTHCLR is a read and write accessible register which selects the cell over voltage alert clear threshold used with bipolar ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	BIPOVTHCLR[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BIPOVTHCLR[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BIPOVTHCLR	15:2	Bipolar Cell Overvoltage Alert Clear Threshold 14-bit threshold value at/below which ALRTOV alerts will be cleared/ deasserted for bipolar cell measurements. Bipolar format. *Note: For proper operation, this value should always be less than or equal to BIPOVTHSET.*

BIPOVTHSETREG (0x25)

BIPOVTHSET is a read and write accessible register which selects the cell over voltage alert set threshold used with bipolar ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	BIPOVTHSET[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BIPOVTHSET[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BIPOVTHSET	15:2	Bipolar Cell Over Voltage Alert Set Threshold 14-bit threshold value above which ALRTOV alerts will be set/asserted for bipolar cell measurements. Bipolar format. A value of 0x3FFF effectively disables over voltage checking.

BIPUVTHCLRREG (0x26)

BIPUVTHCLR is a read and write accessible register which selects the cell under voltage alert clear threshold used with bipolar ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	BIPUVTHCLR[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BIPUVTHCLR[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BIPUVTHCLR	15:2	Bipolar Cell Undervoltage Alert Clear Threshold 14-bit threshold value at/above which ALRTUV alerts will be cleared/ deasserted for bipolar cell measurements. Bipolar format. *Note: for proper operation, this value should always be greater than or equal to BIPUVTHSET.*

BIPUVTHSETREG (0x27)

BIPUVTHSET is a read and write accessible register which selects the cell under voltage alert set threshold used with bipolar ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	BIPUVTHSET[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BIPUVTHSET[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BIPUVTHSET	15:2	Bipolar Cell Undervoltage Alert Set Threshold 14-bit threshold value below which ALRTUV alerts will be set/asserted for bipolar cell measurements. Bipolar format. A value of 0x0000 effectively disables under voltage checking.

BLKOVTHCLRREG (0x28)

BLKOVTHCLR is a read and write accessible register which selects the block over voltage alert clear threshold used with ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	BLKOVTHCLR[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BLKOVTHCLR[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BLKOVTHCLR	15:2	Block Overvoltage Alert Clear Threshold 14-bit threshold value at/below which the ALRTBLKOV alert will be cleared/ deasserted. *Note: for proper operation, this value should always be less than or equal to BLKOVTHSET.*

BLKOVTHSETREG (0x29)

BLKOVTHSET is a read and write accessible register which selects the block over voltage alert set threshold used with ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	BLKOVTHSET[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BLKOVTHSET[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BLKOVTHSET	15:2	Block Overvoltage Alert Set Threshold 14-bit threshold value above which the ALRTBLKOV alert will be set/asserted. A value of 0x3FFF effectively disables over voltage checking.

BLKUVTHCLRREG (0x2A)

BLKUVTHCLR is a read and write accessible register which selects the block under voltage alert clear threshold used with ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	BLKUVTHCLR[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BLKUVTHCLR[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BLKUVTHCLR	15:2	Block Undervoltage Alert Clear Threshold 14-bit threshold value at/below which the ALRTBLKUV alert will be cleared/ deasserted. *Note: for proper operation, this value should always be greater than or equal to BLKUVTHSET.*

BLKUVTHSETREG (0x2B)

BLKUVTHSET is a read and write accessible register which selects the block under voltage alert set threshold used with ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	BLKUVTHSET[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BLKUVTHSET[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BLKUVTHSET	15:2	Block Undervoltage Alert Set Threshold 14-bit threshold value below which the ALRTBLKUV alert will be set/asserted. A value of 0x0000 effectively disables under voltage checking.

CSAOVTHCLRREG (0x2C)

CSAOVTHCLR is a read and write accessible register which selects the CSA over voltage alert clear threshold used with ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	CSAOVTHCLR[13:6]							
Reset	0x3FFF							
Access Type	Write, Read, Ext							

BIT	7	6	5	4	3	2	1	0
Field	CSAOVTHCLR[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read, Ext						–	–

BITFIELD	BITS	DESCRIPTION
CSAOVTHCLR	15:2	CSA Overvoltage Alert Clear Threshold 14-bit threshold value at/below which ALRTCSAOV alerts will be cleared/ deasserted. Bipolar format. CSA ADC Measurements are made in bipolar mode with CSA Gain applied. Code 0x2000 indicates zero current, lesser codes indicate the pack is discharging, greater codes indicate the pack is charging. *Note: for proper operation, this value should always be less than or equal to CSAOVTHSET.*

CSAOVTHSETREG (0x2D)

CSAOVTHSET is a read and write accessible register which selects the CSA over voltage alert set threshold used with ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	CSAOVTHSET[13:6]							
Reset	0x3FFF							
Access Type	Write, Read, Ext							

BIT	7	6	5	4	3	2	1	0
Field	CSAOVTHSET[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read, Ext						–	–

BITFIELD	BITS	DESCRIPTION
CSAOVTHSET	15:2	CSA Overvoltage Alert Set Threshold 14-bit threshold value above which the ALRTCSAOV alerts will be set/ asserted. Bipolar format. CSA ADC Measurements are made in bipolar mode with CSA Gain applied. Code 0x2000 indicates zero current, lesser codes indicate the pack is discharging, greater codes indicate the pack is charging. A value of 0x3FFF effectively disables over voltage checking.

CSAUVTHCLRREG (0x2E)

CSAUVTHCLR is a read and write accessible register which selects the CSA under voltage alert clear threshold used with ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	CSAUVTHCLR[13:6]							
Reset	0x0000							
Access Type	Write, Read, Ext							

BIT	7	6	5	4	3	2	1	0
Field	CSAUVTHCLR[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read, Ext						–	–

BITFIELD	BITS	DESCRIPTION
CSAUVTHCLR	15:2	CSA Undervoltage Alert Clear Threshold 14-bit threshold value at/above which ALRTCSAUV alerts will be cleared/ deasserted. Bipolar format. CSA ADC Measurements are made in bipolar mode with CSA Gain applied. Code 0x2000 indicates zero current, lesser codes indicate the pack is discharging, greater codes indicate the pack is charging. *Note: for proper operation, this value should always be greater than or equal to CSAUVTHSET.*

CSAUVTHSETREG (0x2F)

CSAUVTHSET is a read and write accessible register which selects the CSA under voltage alert set threshold used with ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	CSAUVTHSET[13:6]							
Reset	0x0000							
Access Type	Write, Read, Ext							

BIT	7	6	5	4	3	2	1	0
Field	CSAUVTHSET[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read, Ext						–	–

BITFIELD	BITS	DESCRIPTION
CSAUVTHSET	15:2	CSA Undervoltage Alert Set Threshold 14-bit threshold value below which the ALRTCSAUV alerts will be set/ asserted. Bipolar format. CSA ADC Measurements are made in bipolar mode with CSA Gain applied. Code 0x2000 indicates zero current, lesser codes indicate the pack is discharging, greater codes indicate the pack is charging. A value of 0x0000 effectively disables under voltage checking.

AUXROVTHCLRREG (0x30)

AUXROVTHCLR is a read and write accessible register which selects the over voltage (cold) alert clear threshold used with Ratiometric Auxiliary ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	AUXROVTHCLR[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AUXROVTHCLR[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
AUXROVTHCLR	15:2	Ratiometric Auxiliary Overvoltage (Cold) Alert Clear Threshold 14-bit over voltage (cold) clear threshold value, at/below which ALRTAUXOV alerts will be cleared/deasserted. This threshold is applied for Auxiliary measurements where AUXREFSELn=0 (Ratiometric). *Note: for proper operation, this value should always be less than or equal to AUXROVTHSET.*

AUXROVTHSETREG (0x31)

AUXROVTHSET is a read and write accessible register which selects the over voltage (cold) alert set threshold used with Ratiometric Auxiliary ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	AUXROVTHSET[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AUXROVTHSET[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
AUXROVTHSET	15:2	Ratiometric Auxiliary Overvoltage (Cold) Alert Set Threshold 14-bit over voltage (cold) set threshold value, above which ALRTAUXOV alerts will be asserted. This threshold is applied for Auxiliary measurements where AUXREFSELn=0 (Ratiometric). A value of 0x3FFF effectively disables over voltage checking.

AUXRUVTHCLRREG (0x32)

AUXRUVTHCLR is a read and write accessible register which selects the under voltage (hot) alert clear threshold used with Ratiometric Auxiliary ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	AUXRUVTHCLR[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AUXRUVTHCLR[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
AUXRUVTHCLR	15:2	Ratiometric Auxiliary Undervoltage(Hot) Alert Clear Threshold 14-bit undervoltage (hot) clear threshold value, at/above which ALRTAUXUV alerts will be cleared/deasserted. This threshold is applied for Auxiliary measurements where AUXREFSELn=0 (Ratiometric). *Note: for proper operation, this value should always be greater than or equal to AUXRUVTHSET.*

AUXRUVTHSETREG (0x33)

AUXRUVTHSET is a read and write accessible register which selects the under voltage (hot) alert set threshold used with Ratiometric Auxiliary ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	AUXRUVTHSET[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AUXRUVTHSET[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
AUXRUVTHSET	15:2	Ratiometric Auxiliary Undervoltage (Hot) Alert Set Threshold 14-bit undervoltage (hot) set threshold value, below which ALRTAUXUV alerts will be asserted. This threshold is applied for Auxiliary measurements where AUXREFSELn=0 (Ratiometric). A value of 0x0000 effectively disables under voltage checking.

AUXAOVTHCLRREG (0x34)

AUXOVTHCLR is a read and write accessible register which selects the over voltage alert clear threshold used with Absolute Auxiliary ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	AUXAOVTHCLR[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AUXAOVTHCLR[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
AUXAOVTHCLR	15:2	Absolute Auxiliary Overvoltage Alert Clear Threshold 14-bit overvoltage clear threshold value, at/below which ALRTAUXOV alerts will be cleared/deasserted. This threshold is applied for Auxiliary measurements where AUXREFSELn=1 (Absolute). *Note: for proper operation, this value should always be less than or equal to AUXAOVTHSET.*

AUXAOVTHSETREG (0x35)

AUXAOVTHSET is a read and write accessible register which selects the over voltage alert set threshold used with Absolute Auxiliary ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	AUXAOVTHSET[13:6]							
Reset	0x3FFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AUXAOVTHSET[5:0]						–	–
Reset	0x3FFF						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
AUXAOVTHSET	15:2	Auxiliary Overvoltage Alert Set Threshold 14-bit overvoltage set threshold value, above which ALRTAUXOV alerts will be asserted. This threshold is applied for Auxiliary measurements where AUXREFSELn=1 (Absolute). A value of 0x3FFF effectively disables over voltage checking.

AUXAUVTHCLRREG (0x36)

AUXAUVTHCLR is a read and write accessible register which selects the under voltage alert clear threshold used with Absolute Auxiliary ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	AUXAUVTHCLR[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AUXAUVTHCLR[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
AUXAUVTHCLR	15:2	Absolute Auxiliary Undervoltage Alert Clear Threshold 14-bit undervoltage clear threshold value, at/above which ALRTAUXUV alerts will be cleared/deasserted. This threshold is applied for Auxiliary measurements where AUXREFSELn=1 (Absolute). *Note: for proper operation, this value should always be greater than or equal to AUXAUVTHSET.*

AUXAUVTHSETREG (0x37)

AUXAUVTHSET is a read and write accessible register which selects the under voltage alert set threshold used with Absolute Auxiliary ADC measurements.

BIT	15	14	13	12	11	10	9	8
Field	AUXAUVTHSET[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AUXAUVTHSET[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
AUXAUVTHSET	15:2	Absolute Auxiliary Undervoltage Alert Set Threshold 14-bit undervoltage set threshold value, below which ALRTAUXUV alerts will be asserted. This threshold is applied for Auxiliary measurements where AUXREFSELn=1 (Absolute). A value of 0x0000 effectively disables under voltage checking.

COMPOVTHREG (0x38)

COMPOVTH is a read and write accessible register which selects the cell over voltage alert threshold for the redundant comparator.

BIT	15	14	13	12	11	10	9	8
Field	COMPOVTH[9:2]							
Reset	0x3FF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPOVTH[1:0]		–	–	–	–	–	–
Reset	0x3FF		–	–	–	–	–	–
Access Type	Write, Read		–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPOVTH	15:6	Comparator Cell Overvoltage Alert Threshold 10-bit threshold value, of a 5V input range, above which ALRTCOMPOV alerts will be set/asserted by comparator scans. A value of 0x3FF effectively disables over voltage checking. *Note: for proper operation, this value should always be greater than or equal to COMPUVTH.*

COMPUVTHREG (0x39)

COMPUVTH is a read and write accessible register which selects the cell under voltage alert threshold for the redundant comparator.

BIT	15	14	13	12	11	10	9	8
Field	COMPUVTH[9:2]							
Reset	0x000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPUVTH[1:0]		–	–	–	–	–	–
Reset	0x000		–	–	–	–	–	–
Access Type	Write, Read		–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPUVTH	15:6	Comparator Cell Undervoltage Alert Threshold 10-bit threshold value, of a 5V input range, below which ALRTCOMPUV alerts will be set/asserted by comparator scans. A value of 0x000 effectively disables under voltage checking. *Note: for proper operation, his value should always be less than or equal to COMPOVTH.*

COMPAUXROVTHREG (0x3A)

COMPAUXROVTH is a read and write accessible register which selects the over voltage (cold) alert threshold applied

during Ratiometric Auxiliary comparator measurements.

BIT	15	14	13	12	11	10	9	8
Field	COMPAUXROVTH[9:2]							
Reset	0x3FF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPAUXROVTH[1:0]		–	–	–	–	–	–
Reset	0x3FF		–	–	–	–	–	–
Access Type	Write, Read		–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPAUXROVTH	15:6	Comparator Ratiometric Auxiliary Overvoltage (Cold) Alert Threshold 10-bit overvoltage (cold) threshold value of a input range of V_{AA}, above which ALRTCOMPAUXOV alerts will be set/asserted by comparator scans. This threshold is applied for Auxiliary measurements where AUXREFSELn=0 (Ratiometric). A value of 0x3FF effectively disables over voltage checking. *Note: for proper operation, this value should always be greater than or equal to COMPAUXRUVTH.*

COMPAUXRUVTHREG (0x3B)

COMPAUXRUVTH is a read and write accessible register which selects the under voltage (hot) alert threshold applied during Ratiometric Auxiliary comparator measurements.

BIT	15	14	13	12	11	10	9	8
Field	COMPAUXRUVTH[9:2]							
Reset	0x000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPAUXRUVTH[1:0]		–	–	–	–	–	–
Reset	0x000		–	–	–	–	–	–
Access Type	Write, Read		–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPAUXRUVTH	15:6	Comparator Ratiometric Auxiliary Undervoltage (Hot) Alert Threshold 10-bit undervoltage (hot) threshold value of a input range of V_{AA}, below which ALRTCOMPAUXUV alerts will be set/asserted by comparator scans. This threshold is applied for Auxiliary measurements where AUXREFSELn=0 (Ratiometric). A value of 0x000 effectively disables under voltage checking. *Note: for proper operation, this value should always be less than or equal to COMPAUXROVTH.*

COMPAUXAOVTHREG (0x3C)

COMPAUXAOVTH is a read and write accessible register which selects the over voltage alert threshold applied during Absolute Auxiliary comparator measurements.

BIT	15	14	13	12	11	10	9	8
Field	COMPAUXAOVTH[9:2]							
Reset	0x3FF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPAUXAOVTH[1:0]		–	–	–	–	–	–
Reset	0x3FF		–	–	–	–	–	–
Access Type	Write, Read		–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPAUXAOVTH	15:6	Comparator Absolute Auxiliary Overvoltage Alert Threshold 10-bit overvoltage threshold value, of an input range of V_{REF}, above which ALRTCOMPAUXOV alerts will be set/asserted by comparator scans. This threshold is applied for Auxiliary measurements where AUXREFSELn=1 (Absolute). A value of 0x3FF effectively disables over voltage checking. *Note: for normal operation, this value should always be greater than or equal to COMPAUXAUVTH.*

COMPAUXAUVTHREG (0x3D)

COMPAUXAUVTH is a read and write accessible register which selects the under voltage alert threshold applied during Absolute Auxiliary comparator measurements.

BIT	15	14	13	12	11	10	9	8
Field	COMPAUXAUVTH[9:2]							
Reset	0x000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPAUXAUVTH[1:0]		–	–	–	–	–	–
Reset	0x000		–	–	–	–	–	–
Access Type	Write, Read		–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPAUXAUVTH	15:6	Comparator Absolute Auxiliary Undervoltage Alert Threshold 10-bit undervoltage threshold value, of an input range of V_{REF}, below which ALRTCOMPAUXUV alerts will be set/asserted by comparator scans. This threshold is applied for Auxiliary measurements where AUXREFSELn=1 (Absolute). A value of 0x000 effectively disables under voltage checking. *Note: for proper operation, this value should always be less than or equal to COMPAUXAOVTH.*

COMPOPNTHREG (0x3E)

COMPOPNTH is a read and write accessible register which selects the which selects the under voltage alert threshold applied to Unipolar Cell inputs in Open Diagnostic Mode.

BIT	15	14	13	12	11	10	9	8
Field	COMPOPNTH[9:2]							
Reset	0x000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPOPNTH[1:0]		–	–	–	–	–	–
Reset	0x000		–	–	–	–	–	–
Access Type	Write, Read		–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPOPNTH	15:6	Comparator Cell Open Undervoltage Alert Threshold 10-bit threshold of a 5V input range, below which ALRTCOMPUV alerts will be set/asserted by comparator scans performed on Unpolar Cell inputs in Open Diagnostic Mode (see CTSTCFG:CELLOPNDIAGSEL). A value of 0x000 effectively disables open under voltage checking.

COMPAUXROPNTHREG (0x3F)

COMPAUXROPNTH is a read and write accessible register which selects the under voltage alert threshold applied to Ratiometric Auxiliary inputs in Open Diagnostic Mode.

BIT	15	14	13	12	11	10	9	8
Field	COMPAUXROPNTH[9:2]							
Reset	0x000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPAUXROPNTH[1:0]		–	–	–	–	–	–
Reset	0x000		–	–	–	–	–	–
Access Type	Write, Read		–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPAUXROPNTH	15:6	Comparator Ratiometric Auxiliary Open Undervoltage Alert Threshold 10-bit undervoltage threshold value, of an input range of V_{AA}, below which ALRTCOMPAUXUV alerts will be set/asserted by comparator scans performed on Ratiometric Auxiliary inputs in Open Diagnostic Mode (see DIAGGENCFG:AUXDIAGSEL). This threshold is applied for Auxiliary measurements where AUXREFSELn=0 (Ratiometric). A value of 0x000 effectively disables under voltage checking.

COMPAUXAOPNTHREG (0x40)

COMPAUXAOPNTH is a read and write accessible register which selects the under voltage alert threshold applied to Absolute Auxiliary inputs in Open Diagnostic Mode.

BIT	15	14	13	12	11	10	9	8
Field	COMPAUXAOPNTH[9:2]							
Reset	0x000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPAUXAOPNTH[1:0]		–	–	–	–	–	–
Reset	0x000		–	–	–	–	–	–
Access Type	Write, Read		–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPAUXAOPNTH	15:6	Comparator Absolute Auxiliary Open Undervoltage Alert Threshold 10-bit undervoltage threshold value, of an input range of V_{REF}, below which ALRTCOMPAUXUV alerts will be set/asserted by comparator scans performed on Absolute Auxiliary inputs in Open Diagnostic Mode (see DIAGGENCFG:AUXDIAGSEL). This threshold is applied for Auxiliary measurements where AUXREFSELn=1 (Absolute). A value of 0x000 effectively disables under voltage checking.

COMPACCOVTHREG (0x41)

COMPACCOVTH is a read and write accessible register which selects the over voltage alert threshold applied during comparator accuracy diagnostics.

BIT	15	14	13	12	11	10	9	8
Field	COMPACCOVTH[9:2]							
Reset	0x3FF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPACCOVTH[1:0]		–	–	–	–	–	–
Reset	0x3FF		–	–	–	–	–	–
Access Type	Write, Read		–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPACCOVTH	15:6	End-of-Sequence Comparator Accuracy Diagnostic Over Voltage Alert Threshold 10-bit overvoltage threshold value of a 5V input range, used to validate the accuracy of the comparator at the end of any measurement sequence using the comparator if enabled (SCANCFG=001 or 010 and COMPACCEN=1). Tested for the Cell Signal Path with $COMP_{IN}$ = V_{REF} via LSA2 (gain=6/13) and DAC_{REF} = V_{REF}. A value above COMPACCOVTH will result in the ALRTCOMPACCOV bit being set/asserted. 0x1D8 is the ideal value. A precise value can be selected based on information from the Comparator Cell Signal Path Fault diagnostic. A value of 0x3FF effectively disables over voltage checking (default).

COMPACCUVTHREG (0x42)

COMPACCUVTH is a read and write accessible register which selects the under voltage alert threshold applied during comparator accuracy diagnostics.

BIT	15	14	13	12	11	10	9	8
Field	COMPACCUVTH[9:2]							
Reset	0x000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	COMPACCUVTH[1:0]		–	–	–	–	–	–
Reset	0x000		–	–	–	–	–	–
Access Type	Write, Read		–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
COMPACCUVTH	15:6	End-of-Sequence Comparator Accuracy Diagnostic Undervoltage Alert Threshold 10-bit undervoltage threshold value of a 5V input range, used to validate the accuracy of the comparator at the end of any measurement sequence using the comparator if enabled (SCANCFG=001 or 010 and COMPACCEN=1). Tested for the Cell Signal Path with $COMP_{IN}$ = V_{REF} via LSA2 (gain=6/13) and DAC_{REF} = V_{REF}. A value below COMPACCUVTH will result in the ALRTCOMPACCUV bit being set/asserted. 0x1D8 is the ideal value. A precise value can be selected based on information from the Comparator Cell Signal Path Fault diagnostic. A value of 0x000 effectively disables under voltage checking (default).

BALSHRTTHRREG (0x43)

BALSHRTTHR is a read and write accessible register which selects alert threshold used during the Balance Switch Short Diagnostic mode.

BIT	15	14	13	12	11	10	9	8
Field	BALSHRTTHR[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BALSHRTTHR[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BALSHRTTHR	15:2	Balance Switch Short Diagnostic Alert Threshold 14-bit undervoltage threshold used for the balancing switch short circuit diagnostic test (SCANCFG=100). Unipolar format. For BALSW Short Diagnostics, only cells with (POLARITYn=0 and CELLENn=1) are measured and checked. The unipolar ADC cell voltage results taken in this mode are compared against the threshold; if any result is below the threshold, it is flagged as a balancing switch alert (ALRTBALSW). Results above the threshold are considered normal. The threshold should be set by the system controller prior to making a diagnostic measurement.

BALLOWTHRREG (0x44)

BALLOWTHR is a read and write accessible register which selects alert low threshold used during the Balance Switch Open Diagnostic mode.

BIT	15	14	13	12	11	10	9	8
Field	BALLOWTHR[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BALLOWTHR[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BALLOWTHR	15:2	Balance Switch Open Diagnostic Alert Low Threshold 14-bit undervoltage threshold used for the balancing switch conducting and cell sense wire diagnostic tests (SCANCFG=101, 110, and 111). Bipolar format, typically a small positive value is selected. For BALSW Open Diagnostics, only cells with (POLARITYn=0 and BALSWENn=1) are measured and checked. For Cell-Sense Open Odd/Even Diagnostics, only odd/even cells at/below TOPCELL1/2 with POLARITYn=0 and are measured and checked. The bipolar ADC cell results in this mode are compared against the threshold; if any result is below the threshold, it is flagged as a balancing switch alert (ALRTBALSW). Results above the threshold are considered normal. The threshold should be set by the system controller prior to making a diagnostic measurement.

BALHIGHTHRREG (0x45)

BALHIGHTHR is a read and write accessible register which selects alert High threshold used during the Balance Switch Open Diagnostic mode.

BIT	15	14	13	12	11	10	9	8
Field	BALHIGHTHR[13:6]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	BALHIGHTHR[5:0]						–	–
Reset	0x0000						–	–
Access Type	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION
BALHIGHTHR	15:2	Balance Switch Open Diagnostic Alert High Threshold 14-bit over-voltage threshold used for the balancing switch conducting and cell sense wire diagnostic tests (SCANCFG=101, 110, 111). Bipolar format, typically a moderate positive value is selected, based on external resistor characteristics. For BALSW Open Diagnostics, only cells with (POLARITYn=0 and BALSWENn=1) are measured and checked. For Cell Sense Open Odd/Even Diagnostics, only odd/even cells at/below TOPCELL1/2 with POLARITYn=0 and are measured and checked. The bipolar ADC cell results in this mode are compared against the threshold; if any result is above the threshold, it is flagged as a balancing switch alert (ALRTBALSW). Results below the threshold are considered normal. The threshold should be set by the system controller prior to making a diagnostic measurement.

CSAREG (0x46)

CSA is a read accessible register which holds the current value for each enabled individual auxiliary measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CSA[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CSA[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CSA	15:2	Current Sense Amplifier Measurement Result CSA[13:0] contains the 14-bit CSA measurement result when CSAEN =1. CSA ADC Measurements are made in bipolar mode with the CSAGAIN setting. Code 0x2000 indicates zero current, lesser codes indicate the pack is discharging, greater codes indicate the pack is charging. Full Scale range is $-V_{REF}/2$ to $+V_{REF}/2$, after the selected CSAGAIN has been applied. If CSAEN=0, and the measurement was skipped during the latest ADC Scan, no internal data is updated, and ALU/IIR readback will be determined by RDFILT. Read only.

CELL1REG (0x47)

CELLn is a read accessible register which holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL1[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL1[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL1	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V If CELLEN=0, and the measurement was skipped during the latest ADC Scan, no internal data is updated, and ALU/IIR readback will be determined by RDFILT. Read only.

CELL2REG (0x48)

CELLn is a read accessible register which holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL2[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL2[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL2	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V If CELLEN=0, and the measurement was skipped during the latest ADC Scan, no internal data is updated, and ALU/IIR readback will be determined by RDFILT. Read only.

CELL3REG (0x49)

CELLn is a read accessible register which holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL3[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL3[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL3	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V If CELLEN=0, and the measurement was skipped during the latest ADC Scan, no internal data is updated, and ALU/IIR readback will be determined by RDFILT. Read only.

CELL4REG (0x4A)

CELLn is a read accessible register which holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL4[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL4[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL4	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V If CELLEN=0, and the measurement was skipped during the latest ADC Scan, no internal data is updated, and ALU/IIR readback will be determined by RDFILT. Read only.

CELL5REG (0x4B)

CELLn is a read accessible register which holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL5[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL5[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL5	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V If CELLEN=0, and the measurement was skipped during the latest ADC Scan, no internal data is updated, and ALU/IIR readback will be determined by RDFILT. Read only.

CELL6REG (0x4C)

CELLn is a read accessible register which holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL6[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL6[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL6	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V If CELLEN=0, and the measurement was skipped during the latest ADC Scan, no internal data is updated, and ALU/IIR readback will be determined by RDFILT. Read only.

CELL7REG (0x4D)

CELLn is a read accessible register which holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL7[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL7[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL7	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V If CELLEN=0, and the measurement was skipped during the latest ADC Scan, no internal data is updated, and ALU/IIR readback will be determined by RDFILT. Read only.

CELL8REG (0x4E)

CELLn is a read accessible register which holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL8[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL8[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL8	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V If CELLEN=0, and the measurement was skipped during the latest ADC Scan, no internal data is updated, and ALU/IIR readback will be determined by RDFILT. Read only.

CELL9REG (0x4F)

CELLn is a read accessible register which holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL9[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL9[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL9	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V If CELLEN=0, and the measurement was skipped during the latest ADC Scan, no internal data is updated, and ALU/IIR readback will be determined by RDFILT. Read only.

CELL10REG (0x50)

CELLn is a read accessible register which holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL10[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL10[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL10	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V If CELLEN=0, and the measurement was skipped during the latest ADC Scan, no internal data is updated, and ALU/IIR readback will be determined by RDFILT. Read only.

CELL11REG (0x51)

CELLn is a read accessible register which holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL11[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL11[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL11	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V If CELLEN=0, and the measurement was skipped during the latest ADC Scan, no internal data is updated, and ALU/IIR readback will be determined by RDFILT. Read only.

CELL12REG (0x52)

CELLn is a read accessible register which holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL12[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL12[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL12	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V If CELLEN=0, and the measurement was skipped during the latest ADC Scan, no internal data is updated, and ALU/IIR readback will be determined by RDFILT. Read only.

CELL13REG (0x53)

CELLn is a read accessible register which holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL13[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL13[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL13	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V If CELLEN=0, and the measurement was skipped during the latest ADC Scan, no internal data is updated, and ALU/IIR readback will be determined by RDFILT. Read only.

CELL14REG (0x54)

CELLn is a read accessible register which holds the current value for each individual cell measurement result.

BIT	15	14	13	12	11	10	9	8
Field	CELL14[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	CELL14[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
CELL14	15:2	Cell Voltage Measurement Result CELLn[13:0] contains the 14-bit measurement result for CELLn. Full-scale input range of 5V If CELLEN=0, and the measurement was skipped during the latest ADC Scan, no internal data is updated, and ALU/IIR readback will be determined by RDFILT. Read only.

BLOCKREG (0x55)

BLOCK is a read accessible register which holds the current value for the total block measurement result.

BIT	15	14	13	12	11	10	9	8
Field	VBLOCK[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	VBLOCK[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
VBLOCK	15:2	Block Voltage Measurement Result VBLOCK[13:0] contains the 14-bit measurement result for VBLK. Full-scale input range of 65V If BLOCKEN=0, and the measurement was skipped during the latest ADC Scan, no internal data is updated, and ALU/IIR readback will be determined by RDFILT. Read only.

TOTALREG (0x56)

TOTAL is a read accessible register which holds the current value for the sum of all enabled measurement results within the stack.

BIT	15	14	13	12	11	10	9	8
Field	TOTAL[15:8]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	TOTAL[7:0]							
Reset	0x0000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
TOTAL	15:0	Total Cell Voltage Measurement Result TOTAL[15:0] contains the 16-bit sum of all cell measurement results enabled during the last scan by MEASUREEN1. Full Scale range is 0.0 to 80.0V with a 1.22mV LSB (Unipolar). Read only. *Please make note of the following behavior:* *Since disabled measurements retain their last results, it is possible there will be data in the result registers which was not included in the TOTAL result calculated for the last scan.* *If Cell and Bus Bar (Unipolar & Bipolar) measurements are mixed within a scan, the summation will be handled accordingly.* *CSA measurements are not included in the Pack as measured by VBLOCK operations, and are thus not included in the TOTAL summation. Totals below 0V cannot be supported, and will be clipped at 0x0000 (may apply to scans using only Bipolar measurements).*

DIAG1REG (0x57)

DIAG1 is a read-only register which contains the Diagnostic result requested by the DIAGCFG:DIAGSEL1 selection taken during the last ADC acquistion.

BIT	15	14	13	12	11	10	9	8
Field	DIAG1[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	DIAG1[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
DIAG1	15:2	DIAG1 contains the 14-bit measurement result for the diagnostic selected by DIAGCFG:DIAGSEL1.

DIAG2REG (0x58)

DIAG2 is a read-only register which contains the Diagnostic result requested by the DIAGCFG:DIAGSEL2 selection taken during the last ADC acquistion.

BIT	15	14	13	12	11	10	9	8
Field	DIAG2[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	DIAG2[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
DIAG2	15:2	DIAG2 contains the 14-bit measurement result for the diagnostic selected by DIAGCFG:DIAGSEL2.

AUX0REG (0x59)

AUXn is a read accessible register which holds the current value for each enabled individual auxiliary measurement result.

BIT	15	14	13	12	11	10	9	8
Field	AUX0[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	AUX0[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
AUX0	15:2	Auxiliary Voltage Measurement Result AUXn[13:0] contains the 14-bit measurement result for AUXn. Full-scale input range of V_{AA} for ratiometric operation, V_{REF} for absolute operation If the port is not configured as an AUXINn input (see AUXGPIOCFG), the result will readback 0x0000 for the unused channel. Otherwise if AUXEN=0, and the measurement was skipped during the latest ADC Scan, the previously determined result will remain. Read only.

AUX1REG (0x5A)

AUXn is a read accessible register which holds the current value for each enabled individual auxiliary measurement result.

BIT	15	14	13	12	11	10	9	8
Field	AUX1[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	AUX1[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
AUX1	15:2	Auxiliary Voltage Measurement Result AUXn[13:0] contains the 14-bit measurement result for AUXn. Full-scale input range of V_{AA} for ratiometric operation, V_{REF} for absolute operation If the port is not configured as an AUXINn input (see AUXGPIOCFG), the result will readback 0x0000 for the unused channel. Otherwise if AUXEN=0, and the measurement was skipped during the latest ADC Scan, the previously determined result will remain. Read only.

AUX2REG (0x5B)

AUXn is a read accessible register which holds the current value for each enabled individual auxiliary measurement result.

BIT	15	14	13	12	11	10	9	8
Field	AUX2[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	AUX2[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
AUX2	15:2	Auxiliary Voltage Measurement Result AUXn[13:0] contains the 14-bit measurement result for AUXn. Full-scale input range of V_{AA} for ratiometric operation, V_{REF} for absolute operation If the port is not configured as an AUXINn input (see AUXGPIOCFG), the result will readback 0x0000 for the unused channel. Otherwise if AUXEN=0, and the measurement was skipped during the latest ADC Scan, the previously determined result will remain. Read only.

AUX3REG (0x5C)

AUXn is a read accessible register which holds the current value for each enabled individual auxiliary measurement result.

BIT	15	14	13	12	11	10	9	8
Field	AUX3[13:6]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	AUX3[5:0]						–	–
Reset	0x0000						–	–
Access Type	Read Only						–	–

BITFIELD	BITS	DESCRIPTION
AUX3	15:2	Auxiliary Voltage Measurement Result AUXn[13:0] contains the 14-bit measurement result for AUXn. Full-scale input range of V_{AA} for ratiometric operation, V_{REF} for absolute operation If the port is not configured as an AUXINn input (see AUXGPIOCFG), the result will readback 0x0000 for the unused channel. Otherwise if AUXEN=0, and the measurement was skipped during the latest ADC Scan, the previously determined result will remain. Read only.

POLARITYCTRL (0x5F)

POLARITYCTRL is a read and write accessible register which governs the measurement type used during scans. In general, Unipolar mode indicates a Cell and Bipolar mode indicates a Bus-Bar.

BIT	15	14	13	12	11	10	9	8
Field	MINMAXPOL	–	POLARITY[14:9]					
Reset	0b0	–	0x0000					
Access Type	Write, Read	–	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	POLARITY[8:1]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MINMAXPOL	15	MIN/MAX Operating Mode 0 = Only Unipolar Cell Measurements are included in MINCELL, MAXCELL, and ALRTMSMTCH calculations (default) 1 = Only Bipolar Cell Measurements are included in MINCELL, MAXCELL, and ALRTMSMTCH calculations (useful in fuel cell applications)

BITFIELD	BITS	DESCRIPTION
POLARITY	13:0	Cell Measurement Polarity Selection 0 = Unipolar 0V to 5V Input Range (default) 1 = Bipolar -2.5V to 2.5V Input Bipolar cells will be fault masked during BALSWDIAG ADC Measurement scans. MINMAXPOL determines whether Bipolar cells are included in MIN/MAXCELL and ALRTMSMTCH calculations. Bipolar cell measurements will be checked against BIPOVTH and BIPUVTH thresholds rather than OVTH and UVTH thresholds. Bipolar cells will not be included in Comparator Measurement scans: ALRTCOMPOV, ALRTCOMPUV, alerts will not be triggered.

AUXREFCTRL (0x60)

AUXREFCTRL is a read and write accessible register which governs the reference range used for enabled Auxiliary channels during ADC and COMP acquisition sequences.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AUXREFSEL[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read, Ext			

BITFIELD	BITS	DESCRIPTION
AUXREFSEL	3:0	Auxiliary Input Reference Selection 0 = Ratiometric, REF=V_{THRM} (default) 1 = Absolute, REF=V_{REF}=2.307V This bit selects the reference used and which set of AUX OV, UV, and OPN thresholds are used during ADC and Comparator acquisition sequences. *Note: If the I2CEN bit (Digital I2C mode, applies to [1:0] only), or the respective GPIOEN bit is set (GPIO mode), this bit is ignored, but will still read back the user setting.*

AUXTIMEREG (0x61)

AUXTIMEREG is a read and write accessible register which governs the settling time allowed for biasing AUX/GPIO pins prior to measurements.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	AUXTIME[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read	

BIT	7	6	5	4	3	2	1	0
Field	AUXTIME[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
AUXTIME	9:0	AUX Pre-Conversion Settling TIme Configures the pre-conversion settling time for all enabled AUXn inputs from 0µs (default) up to 6.138ms according to the equation: T_{Settle} = (AUXTIME[9:0])*6uS This is to allow extra settling time if the application circuit requires it since the THRM voltage is not driven out until the start of the acquisition (in auto mode). This time is inserted at the beginning of each requested scan. If AUXTIME has not expired, but no other scan measurement is active, the HVCP will be refreshed during the AUXTIME.

ACQCFG (0x62)

ACQCFG is a read and write accessible register which governs several aspects of the measurement and acquisition procedure.

BIT	15	14	13	12	11	10	9	8
Field	ADCZSFSEN	ADCCALEN	COMPACCEN	FOSR[1:0]		THRMMODE[1:0]		CSAGAIN[2]
Reset	0b0	0b0	0b0	0b00		0b00		0b000
Access Type	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read, Ext

BIT	7	6	5	4	3	2	1	0
Field	CSAGAIN[1:0]		–	–	–	–	–	–
Reset	0b000		–	–	–	–	–	–
Access Type	Write, Read, Ext		–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
ADCZSFSEN	15	End-of-Sequence ADC Stuck-At Fault Diagnostic Enable 0 = Disable ADC ZS/FS Diagnostics (default) 1 = Enable ADC ZS/FS Diagnostics If enabled, at the end of any measurement sequence using the ADC (SCANCFG != 010), the ADC will automatically be tested with over driven inputs designed to force outputs to Zero Scale and Full Scale. Any result other than 0x000 or 0xFFF will be reported a via ALRTADCZS and ALRTADCFS, respectively.
ADCCALEN	14	ADC Calibration Enable 0 = Calibration not applied to Scan results 1 = Calibration applied to Scan results *Does not impact Comparator operations.*

BITFIELD	BITS	DESCRIPTION
COMPACCEN	13	End-of-Sequence Comparator Accuracy Diagnostic Enable 0 = Disable COMPACC Diagnostics (default) 1 = Enable COMPACC Diagnostics If enabled, at the end of any measurement sequence using the comaprator (SCANCFG=001 or 010), the comparator will automatically be tested with $COMP_{IN}$ = V_{REF} via the LSA2 path (gain=6/13) and DAC_{REF} = V_{REF} against bracketing thresholds COMPACCOVTHR and COMPACCUVTHR. If an unexpected result is found, ALRTCOMPACCOV or ALRTCOMPACCUV will be issued.
FOSR	12:11	Oversampling Frequency Selection 00 = F_{OSR} = frequency determined by selected features 01 = F_{OSR} = 1.60kHz, useful for 50Hz rejection 1x = F_{OSR} = 1.92kHz, useful for 60Hz rejection For ADC and Comparator Scans, F_{OSR} sets a specific effective sampling frequency for use with oversampled acquisitions (OVSAMPL > 000). This can be used to place nulls at n*(F_{OSR}/OSR) to help reject noise at a given frequency. For example, with F_{OSR} = 1.60kHz and OSR = 32, noise at 50Hz and its harmonics can be attenuated. Selection 00 results in an arbitrary but maximum effective sampling frequency determined solely by the number of channels and diagnostics selected for measurement, in addition to analog overhead operations (HVCP refresh, etc.). Worst case is estimated at 2.2kHz with all features enabled.
THRMMODE	10:9	Thermistor Bias Control Mode Controls application of V_{AA} to the THRM pin via the internal switch, to bias external thermistors for measurement. 0x - Automatic Mode (switch ON during acquisition mode) 10 - Manual Off Mode (switch always OFF) 11 - Manual On Mode (switch always ON)
CSAGAIN	8:6	Current Sense Amplifier Gain Selection 000 = 4 V/V (default) 001 = 8 V/V 010 = 16 V/V 011 = 32 V/V 100 = 64 V/V 101 = 128 V/V 11x = 256 V/V

BALSWDLY (0x63)

BALSWDLY is a read and write accessible register which selects the delay intervals used within Manual and Automated Cell Balancing operations when ADC measurements are requested.

BIT	15	14	13	12	11	10	9	8
Field	CELLDLY[7:0]							
Reset	0x00							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	SWDLY[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CELLDLY	15:8	Cell Balancing Cell Path Recovery Delay Selection Time delay for C[n] (HVMUX) recovery from voltage drop during cell balancing prior to ADC Measurement. Values of 0µs (default) to 24.480ms can be realized (96µs step size). This delay is used in Manual Cell Balancing modes when using AUTOBALSWDIS=1 and ALTMUXSEL=0. Also used in Automatic Cell Balancing and Discharge modes after each pair of Even and Odd discharge cycles when CBMEASEN=1x and ALTMUXSEL=0.
SWDLY	7:0	Cell Balancing Switch Path Recovery Delay Selection Time delay for SW[n] (ALTMUX) recovery from voltage drop during cell balancing prior to ADC Measurement. Values of 0µs (default) to 24.480ms can be realized (96µs step size). This delay is used in Manual Cell Balancing modes when using AUTOBALSWDIS=1 and ALTMUXSEL=1. Also used in Automatic Cell Balancing and Discharge modes after each pair of Even and Odd discharge cycles when CBMEASEN=1x and ALTMUXSEL=1.

MEASUREEN1 (0x64)

MEASUREEN1 is a read and write accessible register which governs the channels measured during ADC and COMP acquisition sequences.

BIT	15	14	13	12	11	10	9	8
Field	CSAEN	BLOCKEN	CELLEN[14:9]					
Reset	0b0	0b0	0x0000					
Access Type	Write, Read, Ext	Write, Read	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	CELLEN[8:1]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CSAEN	15	Current Sense Amplifier Measurement Enable 0 = Disable CSA measurement (default) 1 = Enable CSA measurement CSA Measurement is always performed in ADC Bipolar mode. Applies to ADC scans only; the CSA block is not subject to comparator measurements.

BITFIELD	BITS	DESCRIPTION
BLOCKEN	14	Block Voltage Measurement Enable 0 = Disable VBLK/TOPBLOCK measurement and automatic divider connection (default) 1 = Enable VBLK/TOPBLOCK measurement and automatic divider connection Applies to ADC scans only; block is not subject to comparator measurements. In addition to enabling the ADC measurement, BLOCKEN will automatically engage the VBLOCK resistve divider for the duration of the scan. *Note: In Flex Pack applications (FLXPCKEN1/2=1), the resistive divider is connected to a selected Cn pin, and the resulting bias current will impact the Cn result. Therefore, in Flex Pack applications, it is generally recommended to set BLOCKEN=1 only for scans with ALTMUXSEL=1.*
CELLEN	13:0	Cell Voltage Measurement Enable 0 = Disable CELLn measurement (default) 1 = Enable CELLn measurement Enables measurement of the respective cell in the acquisition mode.

MEASUREEN2 (0x65)

MEASUREEN2 is a read and write accessible register which governs the auxiliary channels measured during ADC and COMP acquisition sequences, as well as IIR initialization.

BIT	15	14	13	12	11	10	9	8
Field	SCANIIRINIT	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AUXEN[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read, Ext			

BITFIELD	BITS	DESCRIPTION
SCANIIRINIT	15	Sequencer IIR Initialization Request 0 = IIR Filter Continuation (default) 1 = IIR Filter Initialized In Continuation mode, the current value in the IIR accumulators is kept (presumably from previous cell measurements) and sequencer measurements are ammended normally. In Initialization mode, the IIR accumulators will be re-initialized to the first meaurement taken, and further cell balancing measurements are ammended normally.

BITFIELD	BITS	DESCRIPTION
AUXEN	3:0	Auxiliary Input Measurement Enable 0 = Auxiliary ADC Measurement Disabled (default) 1 = Auxiliary ADC Measurement Enabled Enables measurement of the respective auxiliary inputs in acquisition mode. *Note: If the I2CEN bit (Digital I2C mode, applies to [1:0] only), or the respective GPIOEN bit is set (GPIO mode), this bit is ignored, but will still read back the user setting.*

SCANCTRL (0x66)

SCANCTRL is a read and write accessible register which governs the internal measurement acquisitions (scan) requested of the device. The register also manages the handling of data generated as a result of any scan request.

ADC Scans are used for precision measuremetns of cell and auxilary voltages.

COMP Scans are used for periodic safety/redundancy checking of ADC results, and in some cases, enhanced communication efficiency.

On Demand Calibration will run an internal calibration of the ADC and update the Calibration Data Registers. All ADC measurements requested by Scan and Diagnostic Configuration and Control settings will be ignored.

Balance Switch and Cell Sense Wire Open ADC Diagnostic Scans are a special class of ADC Scan. Use of these settings temporarily override other Scan and Diagnostic Configuration and Control settings. See BALSW and Cell Sense Wire Open Diagnotstics for details.

BIT	15	14	13	12	11	10	9	8
Field	SCANDONE	SCANTIMEOUT	DATARDY	AUTOBALSWDIS	ALRTFILTSEL	AMENDFILT	RDFILT	SCANCFG[2]
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b000
Access Type	Write 0 to Clear, Read	Write 0 to Clear, Read	Write, Read, Ext	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	SCANCFG[1:0]		OVSAMPL[2:0]			ALTMUXSEL	SCANMODE	SCAN
Reset	0b000		0b000			0b0	0b0	0b0
Access Type	Write, Read		Write, Read			Write, Read	Write, Read	Write, Read, Pulse

BITFIELD	BITS	DESCRIPTION
SCANDONE	15	Acquisition Complete Indicator Bit 0 = Indicates an SCAN acquisition is in progress if requested 1 = Indicates the SCAN acquisition has completed Once a SCAN acquisition is completed, the device will set this bit high to indicate completion. This bit is cleared by writing to zero. When this bit is high, further acquisitions requested using SCAN will be ignored. Writing to logic one has no internal effect.

BITFIELD	BITS	DESCRIPTION
SCANTIMEOUT	14	Scan Time Out Indicator Bit Indicates the acquisition did not complete in the expected period of time. The timeout threshold depends on the oversampling configuration. If a SCANTIMEOUT is issued, the resulting partial data should be treated as suspect and ignored. In applications using the IIR, SCANIIRINIT should be issued to avoid any corruption resulting from the timeout event. The acquisition watchdog can be disabled by setting SCANTODIS in the DEVCFG2 register. Cleared by writing to logic zero to allow detection of future timeout events. Writing to logic one has no internal effect.
DATARDY	13	Data Ready Indicator Bit Indicates the measurement data from the acquisition has been transferred from the ALU to the data registers and may now be read. Data for all measurement registers and MIN/MAX/TOTAL is transferred at the same time. Cleared by writing to logic zero to allow detection of the next data transfer. Writing to logic one has no internal effect.
AUTOBALSWDIS	12	Automatic Balancing Switch Disable 0 = Cell Balance operations not impacted by measurement sequences (default) 1 = Cell Balance Manual operations temporarily disabled during measurement sequences Enables automatic suspension of active manual cell balancing operations during measurement sequences. The delay for cell recovery settling time and for the diagnostic recovery is selected automatically, based on the ALTMUXSEL setting for the sequence as follows: 0 = CELLDLY is used 1 = SWDLY is used
ALRTFILTSEL	11	Alert Filtering Selection 0 = Alert Issuance based on Raw Sequencer Results (default) 1 = Alert Issuance based on IIR Filter Results Determines whether the Cell, CSA, and Block alerts are issued based on raw sequencer outputs (oversampling still applies) or IIR filtered outputs. If mode 1 is selected, MEASUREEN2:SCANIIRINIT should be used with the first scan to avoid triggering false alerts due to the IIR settling behavior. *Note: This bit is ignored for measurement scans taken in automated Cell Balancing modes (ALRTFILTSEL=1 is used).*

BITFIELD	BITS	DESCRIPTION
AMENDFILT	10	Amend IIR Filter Enable 0 = ADC result is not included in the IIR accumulator (default) 1 = ADC result is included in the IIR accumulator When set high, for ADC outputs which have IIR filters/accumaulators, the new ADC conversion in the ALU is automatically scaled and transferred into the IIR accumulator at the end of the sequence. This is most often used for normal measurement sequences. When set low, the new ADC conversion in the ALU is not transfered into the IIR accumulator at the end of the sequence. This is most often used for diagnostic measurement sequences where the ADC result would corrupt the settled normal data. *Note: This bit is ignored for measurement scans taken in automated Cell Balancing modes (AMENDFILT=1 is used).*
RDFILT	9	Read IIR Filter Selection 0 = Unfiltered ADC data is loaded into the output data registers (default) 1 = IIR Filtered ADC data is loaded into the output data registers This bit chooses the source for data loaded to the Cell, CSA, and Block registers for read back. The setting of this bit at the time of a measurement scan request (SCAN=1) also determines the source data (filtered/unfiltered) used for TOTAL, MINCELL, MAXCELL, MSMTCH, and all OV/UV alert computations.
SCANCFG	8:6	Scan Configuration Selects the type of scan to be performed based on the selections below. FOSR selection applies to all scans where oversampling applies. 000 = ADC Only Scan 001 = ADC + COMP Scan (Pyramid only) 010 = COMP Only Scan (Pyramid only) 011 = On Demand Calibration 100 = Balancing Switch Short 101 = Balancing Switch Open 110 = Cell Sense Open Odds 111 = Cell Sense Open Evens Some of these selections are formatted by other register content. Some of these selections will temporarily modify/override other register content. See register descriptions for further details. For COMP scans, Polarity is always defaulted to Unipolar, any cell measurements requested in Bipolar mode will be skipped. On Demand Calibration executes an automated routine which will update the contents of the CALOSADC, CALOSR, CALOSTHRM, CALGAINP, and CALGAINR correction coefficients. No other measurements are taken during this operation. *Note: This bitfield is ignored for measurement scans taken in automated Cell Balancing modes (SCANCFG=000 is used).*

BITFIELD	BITS	DESCRIPTION
OVSAMPL	5:3	Oversampling Selection for ADC Acquisitions 000 = Single Acquisition 001 = 4x Oversampling 010 = 8x Oversampling 011 = 16x Oversampling 100 = 32x Oversampling 101 = 64x Oversampling 11x = 128x Oversampling *Note: This bitfield is ignored during Calibration (SCANCFG=011) scans. This bitfield is ignored for measurement scans taken in automated Cell Balancing modes (OVSAMPL=011 is used).*
ALTMUXSEL	2	Cell Measurement Path Selection 0 = HVMUX Signal Path (default) 1 = ALTMUX Signal Path Refer to Diagnostics Section. *Note: Where ALTMUX settings disagree with SCANCFG (BALSWDIAG), SCANCFG takes precedence.*
SCANMODE	1	ADC Scan Mode Selection 0 = Pyramid Scan Mode (default) 1 = Ramp Scan Mode Ramp scan mode is not supported for scans using the Comparator or Calibration scan requests - the setting will be ignored in these modes. *Note: This bit is ignored for measurement scans taken in automated Cell Balancing modes (SCANMODE=0 is used).*
SCAN	0	Scan (Measurement Sequence) Request 0 - Used to initiate a data transfer and/or setup measurement conditions without initiating a measurement sequence 1 - Used to request a new measurement sequence (scan) and initiate a data transfer Acts as a strobe bit and therefore does not need to be cleared (self-clearing). Always reads logic zero. Writes to SCANCTRL with SCAN=1 requesting new scans are ignored if a scan is already in progress, or if SCANDONE is high. In this case, the content written to SCANCTRL[15:1] will be accepted, but the conflicting scan will not be executed and ALRTRJCT will be issued, notifying the user of the conflict. *Note: The intended use of this bit is to enter/exit BALSWDIAG modes using SCANCFG, and allow the alternate conditions to settle prior to requesting the measurement (with a subsequent write to SCANCRTL with SCAN=1). This bit can also be used to realize a variety of data move options (see DBLBUFEN and RDFILT for details) or to clear SCANDONE, SCANTIMEOUT, and DATARDY bits without requesting a measurement sequence/scan.*

ADCTEST1AREG (0x67)

ADCTEST1A is a read and write accessible register which contains user specified arguements used in ALU Diagnostics.

BIT	15	14	13	12	11	10	9	8
Field	ADCTSTEN	–	–	–	ADCTEST1A[11:8]			
Reset	0b0	–	–	–	0x000			
Access Type	Write, Read	–	–	–	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	ADCTEST1A[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ADCTSTEN	15	ADC/ALU Self Test Mode Enable 0 = Normal Operation (default) 1 = Enables the ALU test mode. This mode feeds 12-bit data from the ADCTEST registers directly into the ALU instead of the ADC conversion data. Scans can then be performed, confirming proper operation of the ALU and Calibration MAC. Notes: No calibration coefficients will be applied to ensure deterministic results (Gain =1.0, Offset = 0.0). ADCTESTEN is ignored for On-Demand Calibration scans (SCANCFG=011) to avoid mis-calibration, and all scans performed during Automated Cell Balancing modes to avoid inaccurate balancing results.
ADCTEST1A	11:0	ALU ADC Input Arguement 1A User-specified test data for the ALU diagnostic (ADCTESTEN=1). This 12-bit data is fed into the ALU during the first conversion of odd-numbered samples (e.g., first sample).

ADCTEST1BREG (0x68)

ADCTEST1B is a read and write accessible register which contains user specified arguements used in ALU Diagnostics.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	ADCTEST1B[11:8]			
Reset	–	–	–	–	0x000			
Access Type	–	–	–	–	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	ADCTEST1B[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ADCTEST1B	11:0	ALU ADC Input Arguement 1B User-specified test data for the ALU diagnostic (ADCTEST=1). This 12-bit data is fed into the ALU during the second conversion of odd-numbered samples (e.g., first sample).

ADCTEST2AREG (0x69)

ADCTEST2A is a read and write accessible register which contains user specified arguements used in ALU Diagnostics.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	ADCTEST2A[11:8]			
Reset	–	–	–	–	0x000			
Access Type	–	–	–	–	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	ADCTEST2A[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ADCTEST2A	11:0	ALU ADC Input Arguement 2A User-specified test data for the ALU diagnostic (ADCTEST=1). This 12-bit data is fed into the ALU during the first conversion of even-numbered samples in oversampling mode.

ADCTEST2BREG (0x6A)

ADCTEST2B is a read and write accessible register which contains user specified arguements used in ALU Diagnostics.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	ADCTEST2B[11:8]			
Reset	–	–	–	–	0x000			
Access Type	–	–	–	–	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	ADCTEST2B[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ADCTEST2B	11:0	ALU ADC Input Arguement 2B User-specified test data for the ALU diagnostic (ADCTEST=1). This 12-bit data is fed into the ALU during the second conversion of even-numbered samples in oversampling mode.

DIAGCFG (0x6B)

DIAGCFG is a read and write accessible register which governs diagnostic source and mode options applied to the internal measurement acquisitions (scans).

BIT	15	14	13	12	11	10	9	8
Field	CTSTDAC[3:0]				CTSTSRC	MUXDIAGBUS	MUXDIAGPAIR	MUXDIAGEN
Reset	0x0				0b0	0b0	0b0	0b0
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	DIAGSEL2[3:0]				DIAGSEL1[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
CTSTDAC	15:12	Current Level Configuration for all enabled test sources per the table below (6.25uA LSB for Cn, AUXIN, 3.125uA LSB for HVMUX) CTSTDAC [3:0] / Test Source: Cn, AUXIN / Current: HVMUX 0x0: 6.25uA / 3.125uA 0x1: 12.50uA / 6.250uA 0x2: 18.75uA / 9.375uA ... 0xD: 87.5uA / 43.75uA 0xE: 93.75uA / 46.875uA 0xF: 100uA / 50uA
CTSTSRC	11	Test Current Source Polarity 0 = Sink current to GND (default) 1 = Source current from VAA *Note: Polarity selection applies to AUX Test Current Sources only.*
MUXDIAGBUS	10	Selects the HVMUX output to which the HVMUX test current source is connected, if MUXDIAGPAIR is enabled. 0 = Output used for even cells, C0, and AGND 1 = Output used for odd cells and REF, and ALTREF
MUXDIAGPAIR	9	MUX Diagnostic Bus Configuration 0 = Both HVMUX test current sources are connected to both HVMUX outputs. (default) 1 = A single HVMUX test current source is connected to only one HVMUX output (as selected by MUXDIAGBUS).
MUXDIAGEN	8	HVMUX Test Current Source(s) Enable. 0 = Disable (default) 1 = Enable The current level is configured by CSTDAC and the connectivity is configured by MUXDIAGPAIR, and MUXDIAGBUS

BITFIELD	BITS	DESCRIPTION
DIAGSEL2	7:4	Acquisition Diagnostic2 Measurement Selection 0000 = No Diagnostic Requested 0001 = Die Temperature ($ADC_{IN}=V_{PTAT}$, $ADC_{REF}=V_{REF}$). 0010 = V_{AA} ($ADC_{IN}=V_{REF}$ via LSAmp, $ADC_{REF}=V_{AA}$) 0011 = Cell Signal Path ADC Fault, V_{ALTREF} ($ADC_{IN}=V_{ALTREF}$ via LSAmp, $ADC_{REF}=V_{REF}$) 0100 = Comparator Cell Signal Path Fault ($ADC_{IN}=V_{REF}$ via LSAmp2 - V_{DAC} at DAC_{CODE}=0x1D8 (6/13), $ADC_{REF}=DAC_{REF}=V_{REF}$, bipolar mode) 0101 = Cell Calibration ($ADC_{IN}=V_{REF}$ via LSAmp, $ADC_{REF}=V_{REF}$). Calibration gain and offset coefficients and chopping applied according to SCANMODE selection. 0110 = Offset Calibration (ADC_{IN}=Short (Pyramid) or ADC_{IN}=Short via LSAmp (Ramp), $ADC_{REF}=V_{REF}$, bipolar mode). Calibration offset coefficients applied according to SCANMODE selection. 0111 = 3/4-Scale DAC Test (DAC=0x2FF $ADC_{IN}=V_{DAC}$, $ADC_{REF}=DAC_{REF}=V_{REF}$). 1000 = 1/4-Scale DAC Test (DAC=0x100 $ADC_{IN}=V_{DAC}$, $ADC_{REF}=DAC_{REF}=V_{REF}$). 1001 = THRM Offset Calibration (ADC_{IN}=Short, $ADC_{REF}=V_{THRM}$, bipolar mode). CALOSTHRM coefficient applied. Selects the second diagnostic measurement appended to the acquisition, with the result stored in DIAG2. Appropriate calibrations (or factory defaults if ADCALEN=0) and chopping are applied as needed. *Detailed Diagnostics* *1010 = Zero-Scale ADC Test (0x0000, $ADC_{IN}=-V_{AA}$, $ADC_{REF}=V_{REF}$, bipolar mode), full result available via DIAG.* *1011 = Full-Scale ADC Test (0x3FFC, $ADC_{IN}=V_{AA}$, $ADC_{REF}=V_{REF}$, bipolar mode), full result available via DIAG.* *1100 = LSAMP Offset ($ADC_{IN}=V_{LSA_0V}$, $ADC_{REF}=V_{REF}$. bipolar mode)* *Detailed diagnostics are normally performed at the end of an acquisition (with the exception of LSAMP Offset, which is covered by the V_{ALTREF} diagnostic), and the pass/fail results are available in the FMEA2 BIST alerts. However, if it is deemed necessary to examine detailed results, these can be made available in the DIAG2 register using the modes above.*

BITFIELD	BITS	DESCRIPTION
DIAGSEL1	3:0	Acquisition Diagnostic1 Measurement Selection 0000 = No Diagnostic Requested 0001 = Die Temperature ($ADC_{IN}=V_{PTAT}$, $ADC_{REF}=V_{REF}$). 0010 = V_{AA} ($ADC_{IN}=V_{REF}$ via LSAmp, $ADC_{REF}=V_{AA}$) 0011 = Cell Signal Path ADC Fault, V_{ALTREF} ($ADC_{IN}=V_{ALTREF}$ via LSAmp, $ADC_{REF}=V_{REF}$) 0100 = Comparator Cell Signal Path Fault ($ADC_{IN}=V_{REF}$ via LSAmp2 - V_{DAC} at DAC_{CODE}=0x1D8 (6/13), $ADC_{REF}=DAC_{REF}=V_{REF}$, bipolar mode) 0101 = Cell Calibration ($ADC_{IN}=V_{REF}$ via LSAmp, $ADC_{REF}=V_{REF}$). Calibration gain and offset coefficients and chopping applied according to SCANMODE selection. 0110 = Offset Calibration (ADC_{IN}=Short (Pyramid) or ADC_{IN}=Short via LSAmp (Ramp), $ADC_{REF}=V_{REF}$, bipolar mode). Calibration offset coefficients applied according to SCANMODE selection. 0111 = 3/4-Scale DAC Test (DAC=0x2FF $ADC_{IN}=V_{DAC}$, $ADC_{REF}=DAC_{REF}=V_{REF}$). 1000 = 1/4-Scale DAC Test (DAC=0x100 $ADC_{IN}=V_{DAC}$, $ADC_{REF}=DAC_{REF}=V_{REF}$). 1001 = THRM Offset Calibration (ADC_{IN}=Short, $ADC_{REF}=V_{THRM}$, bipolar mode). CALOSTHRM coefficient applied. Selects the first diagnostic measurement appended to the acquisition, with the result stored in DIAG1. Appropriate calibrations (or factory defaults if ADCALEN=0) and chopping are applied as needed. *Detailed Diagnostics* *1010 = Zero-Scale ADC Test (0x0000, $ADC_{IN}=-V_{AA}$, $ADC_{REF}=V_{REF}$, bipolar mode), full result available via DIAG.* *1011 = Full-Scale ADC Test (0x3FFC, $ADC_{IN}=V_{AA}$, $ADC_{REF}=V_{REF}$, bipolar mode), full result available via DIAG.* *1100 = LSAMP Offset ($ADC_{IN}=V_{LSA_0V}$, $ADC_{REF}=V_{REF}$. bipolar mode)* *Detailed diagnostics are normally performed at the end of an acquisition (with the exception of LSAMP Offset, which is covered by the V_{ALTREF} diagnostic), and the pass/fail results are available in the FMEA2 BIST alerts. However, if it is deemed necessary to examine detailed results, these can be made available in the DIAG1 register using the modes above.*

CTSTCFG (0x6C)

CTSTCFG is a read and write accessible register which controls the application of diagnostic current sources to selected cell input channels.

BIT	15	14	13	12	11	10	9	8
Field	CELLOPNDIAGSEL	CTSTEN[14:8]						
Reset	0b0	0x0000						
Access Type	Write, Read	Write, Read						
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	CTSTEN[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CELLOPNDIAGSEL	15	Cell Open Diagnostic Mode Selection 0 - Normal Operation (default) 1 - Open Diagnostic Operation In Normal Mode (0), measured CELLn channels are selected by CELLEN and measured with standard thresholds, on a per channel basis for both ADC and Comparator acquisition sequences. In Open Diagnostic Mode (1), measured CELLn channels are selected by (CELLENn & !POLARITYn), on a per channel basis. Only low side Comparator checks will be performed using alternate Open (OPN) thresholds. Normally in Open Diagnostic Modes, pull-down current sources are enabled on all measured channels using CTSTEN, and only Comparator measurements are selcected (SCANCFG=010). This mode is most often used with an appropriate Auxiliary Open Diagnostic Mode (AUXDIAGSEL=010 or 011).
CTSTEN	14:0	Cell Diagnostic Current Source Enable Enables the current sources connected to the corresponding cell inputs for diagnostic testing. The current level is configured by the CTSTDAC in the DIAGCFG register.

AUXTSTCFG (0x6D)

AUXTSTCFG is a read and write accessible register which controls the application of diagnostic modes and current sources to selected Auxiliary and/or CSA input channels.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	AUXTSTEN[5:4]		AUXTSTEN[3:0]			
Reset	–	–	0x0		0x0			
Access Type	–	–	Write, Read, Ext		Write, Read, Ext			

BITFIELD	BITS	DESCRIPTION
AUXTSTEN	5:4	Auxiliary/CSA Diagnostic Current Source Enable Enables the current sources connected to the corresponding CSA input for diagnostic testing (AUXTSTEN[5:4] = CSAP, CSAN, respectively). The current level is configured by CTSTDAC, and only pull-up sources are available, DIAGCFG:CTSTSRC=1. *Note: If the respective GPIOEN bit is set (GPIO mode), this bit is ignored, but will still read back the user setting.*

BITFIELD	BITS	DESCRIPTION
AUXTSTEN	3:0	Auxiliary Diagnostic Current Source Enable Enables the current sources connected to the corresponding auxiliary input for diagnostic testing. The current level is configured by DIAGCFG:CTSTDAC and the current direction is configured by DIAGCFG:CTSTSRC. *Note: If the I2CEN bit (Digital I2C mode, applies to [1:0] only), or the respective GPIOEN bit is set (GPIO mode), this bit is ignored, but will still read back the user setting.*

DIAGGENCFG (0x6E)

DIAGGENCFG is a read and write accessible register which controls the application of general diagnostic modes to the selected Auxiliary and/or CSA input paths.

BIT	15	14	13	12	11	10	9	8
Field	AUXDIAGSEL[2:0]			CSATSTSEL[1:0]		–	–	–
Reset	0b000			0b00		–	–	–
Access Type	Write, Read			Write, Read, Ext		–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
AUXDIAGSEL	15:13	AUX Diagnostic Mode Selection 00x - Normal Operation (default) 010 - AUX Accelerated Discharge Operation (Ratiometric only) 011 - THRM Output Connected to AGND 100 - Reserved for Maxim Use Only 101 - Reserved for Maxim Use Only 110 - Reserved for Maxim Use Only 111 - Reserved for Maxim Use Only Control bits used for AUXINn pin diagnostic testing. Only to ports configured as AUXINn inputs are tested.

BITFIELD	BITS	DESCRIPTION
CSATSTSEL	12:11	CSA Diagnostic Mode Selection 00 = Normal Operation (default) 01 = CSA Offset Diagnostic (0x2000 expected) 10 = CSA Gain Low Diagnostic (0x3800 expected) 11 = CSA Gain High Diagnostic (0x3FFC expected) Control bits used for CSA diagnostic testing. In all active modes, the normal input path to the CSA will be opened, and a diagnostic input will be provided during the requested measurement scan. The result will be available in the CSA output data register. In CSA Offset Diagnostic mode (01): ADC_{IN}=Short via CSA, $ADC_{REF}=V_{REF}$, bipolar mode, calibration applied if enabled. In CSA Gain Low Diagnostic mode (10): $ADC_{IN}\approx+0.75V_{FS}$ using test DAC via CSA, $ADC_{REF}=V_{REF}$, bipolar mode, calibration applied if enabled, subject to test DAC accuracy. In CSA Gain High Diagnostic mode (11): $ADC_{IN}\approx+1.5V_{FS}$ using test DAC via CSA, $ADC_{REF}=V_{REF}$, bipolar mode, no calibration applied. *Note: Diagnostic results are automatically kept out of the CSA IIR accumulator and CSAOV/UV checking.*

BALSWCTRL (0x6F)

BALSWCTRL is a read and write accessible register which governs the behavior of the Charge Balacing Switches in Manual and Auto Cell Balacing modes.

Write access to this register is blocked during Automated Cell Balancing operations (CBMODE=001, 1xx).

BIT	15	14	13	12	11	10	9	8
Field	CBRESTART	–	BALSWEN[14:9]					
Reset	0b0	–	0x0000					
Access Type	Write, Read, Pulse	–	Write, Read, Ext					

BIT	7	6	5	4	3	2	1	0
Field	BALSWEN[8:1]							
Reset	0x0000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBRESTART	15	Watchdog Timer Restart for Manual Mode 0 - CBTIMER continues to run 1 - CBTIMER is reset to zero Acts as a strobe bit and therefore does not need to be cleared. Always reads logic zero. Accessible and applies in Manual Mode only. Writing 1 to CBRESTART after cell balancing timer expiration has no effect. To perform another Manual mode cell balancing event, user must issue a separate write to BALCTRL register.
BALSWEN	13:0	Balance Switch Enable BALSWEN[n] enables the balancing switch (allowing conduction) between SWn and SWn-1, balancing CELLn.

BALEXP1 (0x70)

BALEXPn is a read and write accessible register which holds the Cell Balacing Expiration Time for CELLn (using the switch across SWn and SWn-1).

BALEXP1 sets the Expiration Time for all Group Auto Cell Balancing and Discharge modes and the Watchdog time out for Manual Cell Balacing mode.

Write access to this register is blocked during all Cell Balancing operations (CBMODE!=000).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP1[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP1[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP1	9:0	Cell Balancing Expiration Time Cell Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. CBEXP1 is used as the master/watchdog time out setting for Manual, Discharge, and Auto Group cell balancing modes. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP2 (0x71)

BALEXPn is a read and write accessible register which holds the Cell Balacing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Auto Cell Balancing modes only.

Write access to this register is blocked during Automatic Cell Balancing operations (CBMODE=1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP2[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP2[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP2	9:0	Cell Balancing Expiration Time Cell Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP3 (0x72)

BALEXPn is a read and write accessible register which holds the Cell Balacing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Auto Cell Balancing modes only.

Write access to this register is blocked during Automatic Cell Balancing operations (CBMODE=1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP3[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP3[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP3	9:0	Cell Balancing Expiration Time Cell Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP4 (0x73)

BALEXPn is a read and write accessible register which holds the Cell Balacing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Auto Cell Balancing modes only.

Write access to this register is blocked during Automatic Cell Balancing operations (CBMODE=1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP4[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP4[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP4	9:0	Cell Balancing Expiration Time Cell Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP5 (0x74)

BALEXPn is a read and write accessible register which holds the Cell Balacing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Auto Cell Balancing modes only.

Write access to this register is blocked during Automatic Cell Balancing operations (CBMODE=1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP5[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP5[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP5	9:0	Cell Balancing Expiration Time Cell Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP6 (0x75)

BALEXPn is a read and write accessible register which holds the Cell Balacing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Auto Cell Balancing modes only.

Write access to this register is blocked during Automatic Cell Balancing operations (CBMODE=1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP6[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP6[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP6	9:0	Cell Balancing Expiration Time Cell Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP7 (0x76)

BALEXPn is a read and write accessible register which holds the Cell Balacing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Auto Cell Balancing modes only.

Write access to this register is blocked during Automatic Cell Balancing operations (CBMODE=1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP7[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP7[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP7	9:0	Cell Balancing Expiration Time Cell Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP8 (0x77)

BALEXPn is a read and write accessible register which holds the Cell Balacing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Auto Cell Balancing modes only.

Write access to this register is blocked during Automatic Cell Balancing operations (CBMODE=1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP8[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP8[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP8	9:0	Cell Balancing Expiration Time Cell Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP9 (0x78)

BALEXPn is a read and write accessible register which holds the Cell Balacing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Auto Cell Balancing modes only.

Write access to this register is blocked during Automatic Cell Balancing operations (CBMODE=1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP9[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP9[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP9	9:0	Cell Balancing Expiration Time Cell Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP10 (0x79)

BALEXPn is a read and write accessible register which holds the Cell Balacing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Auto Cell Balancing modes only.

Write access to this register is blocked during Automatic Cell Balancing operations (CBMODE=1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP10[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP10[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP10	9:0	Cell Balancing Expiration Time Cell Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP11 (0x7A)

BALEXPn is a read and write accessible register which holds the Cell Balacing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Auto Cell Balancing modes only.

Write access to this register is blocked during Automatic Cell Balancing operations (CBMODE=1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP11[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP11[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP11	9:0	Cell Balancing Expiration Time Cell Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP12 (0x7B)

BALEXPn is a read and write accessible register which holds the Cell Balacing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Auto Cell Balancing modes only.

Write access to this register is blocked during Automatic Cell Balancing operations (CBMODE=1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP12[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP12[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP12	9:0	Cell Balancing Expiration Time Cell Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP13 (0x7C)

BALEXPn is a read and write accessible register which holds the Cell Balacing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Auto Cell Balancing modes only.

Write access to this register is blocked during Automatic Cell Balancing operations (CBMODE=1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP13[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP13[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP13	9:0	Cell Balancing Expiration Time Cell Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALEXP14 (0x7D)

BALEXPn is a read and write accessible register which holds the Cell Balacing Expiration Time for CELLn (using the switch across SWn and SWn-1). Used in Individual Auto Cell Balancing modes only.

Write access to this register is blocked during Automatic Cell Balancing operations (CBMODE=1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBEXP14[9:8]	
Reset	–	–	–	–	–	–	0x000	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	CBEXP14[7:0]							
Reset	0x000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
CBEXP14	9:0	Cell Balancing Expiration Time Cell Balancing Expiration Time for CELLn; unit (LSB = hour, minute, or second) determined by CBMODE. Value 0x3FF operates balancing indefinitely (no timer expiration). Default value 0x000 disables cell balancing (preconfigured timer expiration).

BALAUTOUVTHR (0x7E)

BALAUTOUVTHR is a read and write accessible register which selects the cell under voltage exit threshold for the ADC when used in Automated Cell Balancing operations.

A write to this register allows direct setting or automatic selection of this threshold.

Write access to this register is blocked during Automatic Cell Balancing operations (CBMODE=1xx). Also, during active measurement scans, all writes with CBUVMINCELL=1 will be blocked and will result in ALRTRJCT being issued (since the MINCELL data may be altered as a result of the scan in progress).

A read from this register will display the current value of the threshold and the method used for its selection.

BIT	15	14	13	12	11	10	9	8
Field	CBUVTHR[13:6]							
Reset	0x3FFF							
Access Type	Write, Read, Ext							

BIT	7	6	5	4	3	2	1	0
Field	CBUVTHR[5:0]						–	CBUVMINCELL
Reset	0x3FFF						–	0b0
Access Type	Write, Read, Ext						–	Write, Read, Ext

BITFIELD	BITS	DESCRIPTION
CBUVTHR	15:2	Cell Balancing Under Voltage Threshold 14-bit ADC threshold,of a 5V input range, below which Cell Balancing Operations will be suspended on each CELL. Default of 0x3FFF, ensures no cell balancing will occur without prior configuration.

BITFIELD	BITS	DESCRIPTION
CBUVMINCELL	0	Cell Balancing Undervoltage Threshold Selection 0 = User-Defined CBUVTHR 1 = MINCELL-Defined CBUVTHR In mode 0, the value written to CBUVTHR during a valid write to BALAUTOUVTHR will be loaded to CBUVTHR. In mode 1, the current value in the CELLn register corresponding to the MINCELL address will be automatically loaded to CBUVTHR during a valid write to BALAUTOUVTHR (and the content in CBUVTHR during the write will be ignored). *Note: Automated Cell Balancing with CBUVTHR checking is only supported for unipolar cell measurements. If CBUVMINCELL=1 is written while MINMAXPOL=1, CBUVTHR will be set to 0x3FFF\h as a result.*

BALDLYCTRL (0x7F)

BALDLYCTRL is a read and write accessible register which selects the delay/timing intervals used within Automated Cell Balancing operations.

Write access to this register is blocked during Automated Cell Balancing operations (CBMODE=001, 1xx).

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	CBNTFYCFG[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read, Ext	

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	CBCALDLY[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read, Ext		

BITFIELD	BITS	DESCRIPTION
CBNTFYCFG	9:8	Cell Balancing Notification Alert Configuration 00 = Disable Cell Balancing Notification Alert (default) 01 = Nofication Issued every 1 Hr 10 = Nofication Issued every 2 Hr 11 = Nofication Issued every 4 Hr In Automatic and Discharge modes, the Cell Balancing Notification Alert (ALRTCBNTFY) can be issued to confirm normal progression of automated operations. The frequency of issuance is selected as described above, in real time (i.e. not CBDUTY-adjusted). Notification alerts will continue to be issued during HOLDSHDNL.

BITFIELD	BITS	DESCRIPTION
CBCALDLY	2:0	Cell Balancing Calibration Period Selection In Automatic and Discharge modes, after each pair of Even and Odd Cell Balancing periods, a superviosory ADC Measurement is taken (and checked against CBUVTHR, if enabled/applicable). CBCALDLY allows a calibration operation to be substituted in place of a measurement at the frequency indicted below. A value of 000 (default) disables CAL operations (only ADC operations are performed). 000 - Periodic Calibration Disabled 001 - 2 (every other) cycle 010 - 4 (every forth) cycle 011 - 8 cycles 100 - 12 cycles 101 - 16 cycles 110 - 24 cycles 111 - 32 cycles If CBMEASEN=0x (ADC/CAL Measurements Disabled), this bitfield is ignored and has no effect.

BALCTRL (0x80)

BALCTRL is a read and write accessible register which initiates and controls all internal Cell Balancing modes and operations.

Any write to this register to a mode other than CBMODE=000 (Disable) will restart the CBTIMER at zero and launch the requested mode of operation.

BIT	15	14	13	12	11	10	9	8
Field	CBACTIVE[1:0]		CBMODE[2:0]			CBIIRINIT	HOLDSHDNL[1:0]	
Reset	0b00		0b000			0b0	0b00	
Access Type	Read Only		Write, Read, Ext			Write, Read	Write, Read	

BIT	7	6	5	4	3	2	1	0
Field	CBDUTY[3:0]				CBDONEALRTEN	CBTEMPEN	CBMEASEN[1:0]	
Reset	0x0				0b0	0b0	0x0	
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION
CBACTIVE	15:14	Cell Balancing Timer Active Indicator 00 = Cell Balancing is Disabled (default) 01 = Cell Balancing Operations are Active 10 = Cell Balancing Completed normally due to reaching CBUVTHR or CBEXP exit conditions 11 = Cell Balancing Halted uxexpectedly due to Thermal Exit (ALRTCBTEMP), Time Out (ALRTCBTIMEOUT), or Calibration Fault (ALRTCBCAL) conditions Read only.

BITFIELD	BITS	DESCRIPTION
CBMODE	13:11	Cell Balancing Mode Selection 000 = Cell Balancing Disabled (default) 001 = Emergency/EOL Discharge by Hour 010 = Manual Cell Balancing by Second 011 = Manual Cell Balancing by Minute 100 = Auto Individual Cell Balancing by Second 101 = Auto Individual Cell Balancing by Minute 110 = Auto Group Cell Balancing by Second 111 = Auto Group Cell Balancing by Minute
CBIIRINIT	10	Cell Balancing IIR Initialization Request 0 = IIR Filter Continuation (default) 1 = IIR Filter Initialized If enabled, the IIR filter contents will be initialized during the first measurement scan and CBUVTHR checks will be suspended for 16 measurement scans, giving the IIR time to settle.
HOLDSHDNL	9:8	SHDNL Hold Mode Enable 00 = No Hold (default) 01 = SHDNL Held High for the duration of Automated Cell Balancing or Discharge operation 10 = SHDNL Held High for duration of Automated Cell Balancing or Discharge operations, plus 5 minutes or 6.25% of the maximum applicable CBEXP interval (whichever is greater) 11 = SHDNL Held High for duration of Automated Cell Balancing or Discharge operations, and until removed
CBDUTY	7:4	Cell Balancing Duty Cycle Sets the active duty-cycle within each T_{CBEO} period. 0000 = 6.25% (default) 0001 = 12.5% ... 1110 = 93.75% 1111 = 100%, less NOL and Measurement/Calibration overhead.
CBDONEALRTEN	3	Cell Balancing Complete Alert Enable 0 = ALRTCBDONE masked in STATUS1:ALRTCBAL (default) 1 = ALRTCBDONE included in STATUS1:ALRTCBAL Masking of this alert component allows the user the choice to be notified only for unexpected exits, or normal completions as well.
CBTEMPEN	2	Cell Balancing Thermal Exit Enable 0 = Cell Balancing not impacted by ALRTTEMP (default) 1 = Cell Balancing halts in response to ALRTTEMP
CBMEASEN	1:0	Cell Balancing Measurement Enable 0x = Embedded ADC/CAL Measurements and CBUVTHR checking disabled (default) 10 = Embedded ADC/CAL Measurements enabled, CBUVTHR checking disabled 11 = Embedded ADC/CAL Measurements enabled, CBUVTHR checking enabled *Note: Automated Cell Balancing with CBUVTHR checking is only supported for unipolar cell measurements.*

BALSTAT (0x81)

BALSTAT is a read accessible register which allows the monitoring of any Automated Cell Balancing operations

currently in progress.

Once a CBMODE is initiated, all status bits persist and are cleared only when CBMODE is written to 000 (Disabled) or when a new CBMODE operation is initiated via CBSTART.

BIT	15	14	13	12	11	10	9	8
Field	CBACTIVE_M1[1:0]		CBUNIT[1:0]		CBCNTR[1:0]		CBTIMER[9:8]	
Reset	0b00		0b00		0b00		0x000	
Access Type	Read Only		Read Only		Read Only		Read Only	

BIT	7	6	5	4	3	2	1	0
Field	CBTIMER[7:0]							
Reset	0x000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CBACTIVE_M1	15:14	Cell Balancing Timer Active Indicator (Mirror) 00 = Cell Balancing is Disabled (default) 01 = Cell Balancing Operations are Active 10 = Cell Balancing Completed normally due to reaching CBUVTHR or CBEXP exit conditions 11 = Cell Balancing Halted uxepectedly due to Thermal Exit (ALRTCBTEMP), Time Out (ALRTCBTIMEOUT), or Calibration Fault (ALRTCBCAL) conditions Read only.
CBUNIT	13:12	Cell Balancing Timer Unit Indicator 00 = Cell Balancing is Disabled (default) 01 = CBTIMER measures Seconds 10 = CBTIMER measures Minutes 11 = CBTIMER measures Hours Allows confirmation of Cell Balancing Timer operating mode (LSB weight). Read only,
CBCNTR	11:10	Cell Balancing Active Counter 1Hz Counter which can be read to verify CBTIMER operation/activity when the CBTIMER is operated in minute or hour modes. The counter counts from 0 to 3, rolling over to 0 approximately every 4 seconds in all active cell balancing modes (CBMODE!=000). Read only. *Notes:* *During Hold SHDNL extension periods (HOLDSHDNL=1x), CBCNTR will continue to run.* *If the governing CBEXP setting is set to 0x3FF (infinite), this counter will continue to run, even though it has no impact on the active cell balancing mode.*

BITFIELD	BITS	DESCRIPTION
CBTIMER	9:0	Cell Balancing Timer Value Reads the current Cell Balancing Timer value in seconds, minutes or hours, depending on CBMODE, as indicated by CBUNIT. Read only. *Notes:* *During SHDNL hold/extension periods (HOLDSHDNL=1x), CBTIMER will read back the governing expiration time (CBEXP), indicating that the requested balancing operation has completed.* *If the governing CBEXP setting is set to 0x3FF (infinite), this timer will still run and roll over, even though it has no impact on the active cell balancing mode.*

BALUVSTAT (0x82)

BALUVSTAT is a read accessible register which relates current summary information on the Cell voltages vs. the CBUVTHR undervoltage threshold.

BIT	15	14	13	12	11	10	9	8
Field	CBACTIVE_M2[1:0]		CBUVSTAT[14:9]					
Reset	0b00		0x0000					
Access Type	Read Only		Read Only					

BIT	7	6	5	4	3	2	1	0
Field	CBUVSTAT[8:1]							
Reset	0x0000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CBACTIVE_M2	15:14	Cell Balancing Timer Active Indicator (Mirror) 00 = Cell Balancing is Disabled (default) 01 =Cell Balancing Operations are Active 10 = Cell Balancing Completed normally due to reaching CBUVTHR or CBEXP exit conditions 11 = Cell Balancing Halted uxepectedly due to Thermal Exit (ALRTCBTEMP), Time Out (ALRTCBTIMEOUT), or Calibration Fault (ALRTCBCAL) conditions Read only.
CBUVSTAT	13:0	Cell Balance CBUVTHR Check Status CBUVSTAT[n]=1 indicates the corresponding CELLn result falls below the threshold specified by CBUVTHR and that Cell Balancing operations on that cell have ended. Cleared only when CBMODE is written to 000 (Disabled) or when a new CBMODE operation is initiated via a write to BALCTRL. Read only. *Note: Automated Cell Balancing with CBUVTHR checking is only supported for unipolar cell measurements in locations with BALSWENn=1. The user must also ensure CELLENn=1 and POLARITYn=0 to allow the required measurement updates; if the measurement is not supported, balancing of the cell automatically ends with a CBUVSTATn=1 exit condition.*

BALDATA (0x83)

BALDATA is a read accessible register which relates current summary information on the Cell voltages vs. the CBUVTHR undervoltage threshold.

BIT	15	14	13	12	11	10	9	8
Field	CBACTIVE_M3[1:0]		DATARDY_M	–	–	–	–	–
Reset	0b00		0b0	–	–	–	–	–
Access Type	Read Only		Write, Read, Ext	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	CBSCAN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read, Pulse

BITFIELD	BITS	DESCRIPTION
CBACTIVE_M3	15:14	Cell Balancing Timer Active Indicator (Mirror) 00 = Cell Balancing is Disabled (default) 01 = Cell Balancing Operations are Active 10 = Cell Balancing Completed normally due to reaching CBUVTHR or CBEXP exit conditions 11 = Cell Balancing Halted uxexpectedly due to Thermal Exit (ALRTCBTEMP), Time Out (ALRTCBTIMEOUT), or Calibration Fault (ALRTCBCAL) conditions Read only.
DATARDY_M	13	Data Ready Indicator Bit (Mirror) Indicates the measurement data from the acquisition has been transferred to the data registers and may now be read. Data for all measurement registers and MIN/MAX/TOTAL is transferred at the same time. Cleared by writing to logic zero to allow detection of the next data transfer. Writing to logic one has no internal effect. This is a mirror of the DATARDY bit in SCANCFG, provided to support readback of measurement results taken during Automated and Discharge Cell Balancing modes.
CBSCAN	0	Manually Transfer Measurement Results from IIR to Data registers 0 = No transfer requested 1 = Measurement transferred from the IIR (regardless of RDFILT setting) to data registers; once transfer is complete, DATARDY bit is set. Acts as a strobe bit and therefore does not need to be cleared (self-clearing). This bit has no effect in Cell Balancing Manual or Disable mode, or when CBMEASEN=0x. Always reads logic zero.

I2CPNTR (0x84)

I2CPTNR is a read and write accessible register which contains two Pointer bytes (Register Addresses) available for I2C Master transactions.

Once I2CSEND initiates a read or write transaction, attempts to write I2CPNTR during the transaction will be ignored and will cause an I2CRJCT fault to be issued.

BIT	15	14	13	12	11	10	9	8
Field	I2CPBYTE1[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	I2CPBYTE0[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
I2CPBYTE1	15:8	I2C Pointer Address Byte 1 This is the Pointer (Register) Address Byte 1 available for I2C Master transactions.
I2CPBYTE0	7:0	I2C Pointer Address Byte 0 This is the Pointer (Register) Address Byte 0 available for I2C Master transactions.

I2CWDATA1 (0x85)

I2CWDATA1 is a read and write accessible register which contains the upper data bytes available for I2C Master Write Mode transactions.

Once I2CSEND initiates an I2C read or write transaction, attempts to write I2CWDATA1 during the transaction will be ignored and will cause an I2CRJCT fault to be issued.

BIT	15	14	13	12	11	10	9	8
Field	I2CWBYTE3[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	I2CWBYTE2[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
I2CWBYTE3	15:8	I2C Write Data Byte 3 This is the 3rd (MS) Byte available for I2C Master Write Mode transactions.
I2CWBYTE2	7:0	I2C Write Data Byte 2 This is the 2nd Byte available for I2C Master Write Mode transactions.

I2CWDATA2 (0x86)

I2CWDATA2 is a read and write accessible register which contains the lower data bytes available for I2C Master Write Mode transactions.

Once I2CSEND initiates an I2C read or write transaction, attempts to write I2CWDATA2 during the transaction will be ignored and will cause an I2CRJCT fault to be issued.

BIT	15	14	13	12	11	10	9	8
Field	I2CWBYTE1[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	I2CWBYTE0[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
I2CWBYTE1	15:8	I2C Write Data Byte 1 This is the 1st Byte available for I2C Master Write Mode transactions.
I2CWBYTE0	7:0	I2C Write Data Byte 0 This is the 0th (LS) Byte available for I2C Master Write Mode transactions.

I2CRDATA1 (0x87)

I2CRDATA1 is a read accessible register which contains the upper data bytes received for I2C Master Read Mode transactions.

Note during I2C read transactions, data is updated as each byte is received/acknowledged, so reading back this register during active I2C read transactions will cause an I2CRJCT fault to be issued.

BIT	15	14	13	12	11	10	9	8
Field	I2CRBYTE3[7:0]							
Reset	0xFF							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	I2CRBYTE2[7:0]							
Reset	0xFF							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
I2CRBYTE3	15:8	I2C Read Data Byte 3 This is the 3rd (MS) Byte space available for use by I2C Master Read Mode transactions.
I2CRBYTE2	7:0	I2C Read Data Byte 2 This is the 2nd Byte space available for use by I2C Master Read Mode transactions.

I2CRDATA2 (0x88)

I2CRDATA2 is a read accessible register which contains the lower data bytes received for I2C Master Read Mode transactions.

Note during I2C read transactions, data is updated as each byte is received/acknowledged, so reading back this register during active I2C read transactions will cause an I2CRJCT fault to be issued.

BIT	15	14	13	12	11	10	9	8
Field	I2CRBYTE1[7:0]							
Reset	0xFF							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	I2CRBYTE0[7:0]							
Reset	0xFF							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
I2CRBYTE1	15:8	I2C Read Data Byte 1 This is the 1st Byte space available for use by I2C Master Read Mode transactions.
I2CRBYTE0	7:0	I2C Read Data Byte 0 This is the 0th (LS) Byte space available for use by I2C Master Read Mode transactions.

I2CCFG (0x89)

I2CCFG is a read and write accessible register which configures I2C Master modes and transaction formats.

Once I2CSEND initiates a read or write transaction, attempts to write I2CCFG during the transaction will be ignored and will cause an I2CRJCT fault to be issued.

BIT	15	14	13	12	11	10	9	8
Field	I2CFSCL	I2CWALT	I2CRFMT	I2C10BIT	I2CPNTRLNGTH	I2CALRTEN	–	–
Reset	0b1	0b0	0b1	0b0	0b0	0b0	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	I2CANACONTEN	I2CCONTEN	I2CGLITCHEN	I2CNOISEEN	I2CRDTREN	I2CTOEN
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
I2CFSCL	15	I^2C Master SCL Speed Selection 0 = F_{SCL} = 100kHz 1 = F_{SCL} = 400kHz (default) This bit determines F_{SCL} used for the transaction initiated by the I^2C Master in respose to a write to I2CSEND.
I2CWALT	14	I^2C Master Alternate Write Mode Selection 0 = Normal Mode (1, 2, 3, or 4 Byte Data) 1 = Alternate Mode (1, 2, 0, or 4 Byte Data) This bit determines the data lengths available in Write Mode using I2CDATALNGTH selection bits.

BITFIELD	BITS	DESCRIPTION
I2CRFMT	13	I2C Master Read Format Selection 0 = Normal Format 1 = Combined Format (default) This bit determines the format used for Read mode transactions initiated by the I2C Master in respose to a write to I2CSEND (does not impact Write mode transactions).
I2C10BIT	12	I2C Master Address Mode Selection 0 = 7 Bit Addressing (default) 1 = 10 Bit Addressing This bit determines the address format used for the transaction initiated by the I2C Master in respose to a write to I2CSEND.
I2CPNTRLNGTH	11	I2C Transaction Pointer Length Selection 0 - One Byte Pointer (default) 1 - Two Byte Pointer This is the pointer length used for the requested I2C Master transactions. If one byte pointer mode is used (default, standard), both pointer bytes are available for use in I2C Master transactions using I2CPNTRSEL (minimizing configuration time).
I2CALRTEN	10	I2C Alert Enable 0 = ALRTI2C Reporting Disabled (default) 1 = ALRTI2C Reporting Enabled If enabled, STATUS2:ALRTI2C reflects the bitwise OR of enabled/unmasked I2C Fault indicators I2CSTAT[8:0]. The alert can be masked by setting I2CALRTEN=0. The alert will be cleared when I2CSTAT is cleared and no new faults have been reported.
I2CANACONTEN	5	I2C Bus Analog Contention Report Enable 0 = Bus Contention Monitoring Masked (default) 1 = Bus Contention Monitoring Reported See data sheet for detailed explanations of bus monitoring operations and limitations (set up and hold timing violations, glitch detection, noise handling, etc). A zero selection will still allow the monitor circuitry to run and report results in I2CSTAT:I2CCONT, but the monitored condition will not trigger an ALRTI2C issuance or an I2CSTAT:I2CSTATUS Transaction Error (10).
I2CCONTEN	4	I2C Bus Digital Contention Report Enable 0 = Bus Contention Monitoring Masked (default) 1 = Bus Contention Monitoring Reported See data sheet for detailed explanations of bus monitoring operations and limitations (set up and hold timing violations, glitch detection, noise handling, etc). A zero selection will still allow the monitor circuitry to run and report results in I2CSTAT:I2CCONT, but the monitored condition will not trigger an ALRTI2C issuance or an I2CSTAT:I2CSTATUS Transaction Error (10).

BITFIELD	BITS	DESCRIPTION
I2CGLITCHEN	3	I2C Bus Glitch Report Enable 0 = Bus Glitch Monitoring Masked (default) 1 = Bus Glitch Monitoring Reported See data sheet for detailed explanations of bus monitoring operations and limitations (set up and hold timing violations, glitch detection, noise handling, etc). A zero selection will still allow the monitor circuitry to run and report results in I2CSTAT:I2CGLITCH, but the monitored condition will not trigger an ALRTI2C issuance or an I2CSTAT:I2CSTATUS Transaction Error (10).
I2CNOISEEN	2	I2C Bus Noise Report Enable 0 = Bus Noise Monitoring Masked (default) 1 = Bus Noise Monitoring Reported See data sheet for detailed explanations of bus monitoring operations and limitations (set up and hold timing violations, glitch detection, noise handling, etc). A zero selection will still allow the monitor circuitry to run and report results in I2CSTAT:I2CNOISE, but the monitored condition will not trigger an ALRTI2C issuance or an I2CSTAT:I2CSTATUS Transaction Error (10).
I2CRDTREN	1	I2C Redundant Read Check Enable 0 = Redundant Read Check Disabled (default) 1 = Redundant Read Check Enabled See data sheet for detailed explanation of redundant read check operations and limitations. This bit enables both Redundant Read transactions as well as discrepency reporting.
I2CTOEN	0	I2C Time Out Enable 0 = DIsable I2C Transaction Watchdog (default) 1 = Enable I2C Transaction Watchdog

I2CSTAT (0x8A)

I2CSTAT is a read and write accessible register which shows the current status of the I2C Master.

The I2CSTATUS bits are updated in real time, indicating the current state of the I2C Master and any requested transaction. This status content can be cleared by write operations and modified by transaction progress or subsequent transaction requests.

The second byte contains I2C Fault bits, indicating a fault was observed during an I2C transaction. These bits are updated as they occur and are only cleared by writing to zero. Several faults may occur during a corrupted transaction, so it is best to wait until I2CSTATUS reads 10 (Transaction Error) to ensure all errors have been reported.

While not advisable, if further I2C transactions are requested before the I2C Fault bits from previous transactions are read back and cleared, a cumulative history of faults will be listed, even if subsequent transactions are successful.

BIT	15	14	13	12	11	10	9	8
Field	I2CSTATUS[1:0]		–	–	–	–	–	I2CRJCT
Reset	0b00		–	–	–	–	–	0b0
Access Type	Write, Read, Ext		–	–	–	–	–	Write, Read, Ext

BIT	7	6	5	4	3	2	1	0
Field	I2CDEVNACK	I2CDATANACK	I2CANACONT	I2CCONT	I2CGLITCH	I2CNOISE	I2CRDTRERR	I2CTIMEOUT
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read

BITFIELD	BITS	DESCRIPTION
I2CSTATUS	15:14	I2C Status Indicator 00 - No Transaction Requested (default) 01 - Transaction in Progress 10 - Transaction Error 11 - Transaction Complete I2CSTATUS indicates the current status of the I2C Master. These status bits will be cleared when written to zero or when a new transaction is begun using I2CSEND. Writing to a logic one has no effect. Note specific clear/update behavior.
I2CRJCT	8	I2C Transaction Reject Error Inidcator 0 = No Error Reported (default) 1 = I2C Operation Rejected Indicates one or more I2C Master operations were rejected because 1) a User Write to I2CSEND requested a new I2C transaction during an active I2C transaction, 2) a User Write to a protected I2C Master register was attempted during an active I2C transaction, or 3) a User Read from an I2CRDATA register was requested during an active I2C Read transaction. See I2C Master register descriptions for complete details. Cleared only by writing to logic zero. Writing to a logic one has no effect.
I2CDEVNACK	7	I2C Device ID Not Acknowledged Inidcator 0 = No Error Reported (default) 1 = Slave Address Not Acknowledged Indicates the I2C transaction Device ID Byte(s) were not acknowledged by a slave. This may indicate the slave is malfunctioning or not present on the bus. For Combined Format Read transactions, both slave address acknowledge pulses are required to avoid an error. Cleared only by writing to logic zero. Writing to a logic one has no effect.
I2CDATANACK	6	I2C Data Not Acknowledged Inidcator 0 = No Error Reported (default) 1 = Data Byte Not Acknowledged Indicates one or more I2C transaction Data Byte(s) written were not acknowledged by a slave. This may indicate the slave is malfunctioning, not present on the bus, is busy, or has rejected an unsupported transaction. Cleared only by writing to logic zero. Writing to a logic one has no effect.

BITFIELD	BITS	DESCRIPTION
I2CANACONT	5	I²C Bus Analog Contention Error 0 = No Error Reported (default) 1 = I²C Bus Contention Error Reported Indicates an analog bus contention condition was observed. Analog contention is reported when the sampled SDA value does not match the value driven by the I²C Master. This monitor observes the analog-filtered SDA port sampled by the analog-filtered SCL port when driven by the I²C Master, emulating the filter circuitry typically used in I²C slave devices. Note that incoming SDA data from slaves in read mode is latched using the analog-filtered versions of SDA and SCL. Cleared only by writing to logic zero. Writing to a logic one has no effect.
I2CCONT	4	I²C Bus Digital Contention Error 0 = No Error Reported (default) 1 = I2C Bus Contention Error Reported Indicates a bus contention condition was observed. Digital contention is reported when a digital oversampled port result does not match the value driven by the I²C Master. This monitor observes the unfiltered SCL port and the SDA port when driven by the I²C Master during periods when the signals should be settled. Digitally oversampled contention is more sensitive than analog contention (which employs analog filters). Cleared only by writing to logic zero. Writing to a logic one has no effect.
I2CGLITCH	3	I²C Bus Glitch Error 0 = No Error Reported (default) 1 = I²C Bus Glitch Error Reported Indicates a bus glitch condition was observed. A glitch is reported when a digitally oversampled port monitor reports two or more consecutive samples that disagree with the digitally evaluated filter value. This condition may also be reported if slow transition times, setup time, or hold time violations occur (outside I²C specifications). This monitor observes the unfiltered SCL port and the SDA port outside specified transition intervals. Cleared only by writing to logic zero. Writing to a logic one has no effect.
I2CNOISE	2	I²C Bus Noise Error 0 = No Error Reported (default) 1 = I²C Bus Noise Error Reported Indicates a noisy bus condition was observed. A noise condition is reported when a digitally oversampled port monitor reports a large amount of samples (>25%) that disagree with the evaluated filter value. This condition may also be reported if slow transition times, setup time, or hold time violations occur (outside I²C specifications). This monitor observes the unfiltered SCL port and the SDA port outside specified transition intervals. Cleared only by writing to logic zero. Writing to a logic one has no effect.

BITFIELD	BITS	DESCRIPTION
I2CRDTRERR	1	I2C Redundant Read Error Inidcator 0 = No Error Reported (default) 1 = I2C Redundant Read Error Reported Indicates the results of an I2C Redundant Read Transaction Check failed. This means the data read back in the first read transaction did not match the data in the second read transaction. This function is only enabled if I2CRDTREN=1. Cleared only by writing to logic zero. Writing to a logic one has no effect.
I2CTIMEOUT	0	I2C Time Out Error Inidcator 0 = No Error Reported (default) 1 = I2C Transaction Timed Out Indicates the transaction did not complete in the expected period of time. This function is only enabled if I2CTOEN=1. Cleared only by writing to logic zero. Writing to a logic one has no effect.

I2CSEND (0x8B)

I2CSEND is a read and write accessible register which configures and initiates an I2C Master transaction.

A write to this register will initiate an I2C Master transaction. Only one transaction is supported at any given time. If a write to I2CSEND occurs during an active I2C transaction already in progress, the latest transaction request will be ignored and the I2CSEND contents will not be updated. If this occurs, an I2CRJCT fault will be issued.

A read from this register will readback the current contents. This will represent the last transaction request accepted by the I2C Master.

BIT	15	14	13	12	11	10	9	8
Field	I2CPNTRSEL	I2CDATALNGTH[1:0]		I2CDATASEL[1:0]		I2CDEVIDEXT[2:0]		
Reset	0b0	0b01		0b01		0b000		
Access Type	Write, Read	Write, Read		Write, Read		Write, Read		

BIT	7	6	5	4	3	2	1	0
Field	I2CDEVID[6:0]							I2CRWB
Reset	0x00							0b0
Access Type	Write, Read							Write, Read, Ext

BITFIELD	BITS	DESCRIPTION
I2CPNTRSEL	15	I2C Transaction Pointer Selection 0 - Use I2CPBYTE0 1 - Use I2CPBYTE1 Selects the Pointer Byte used for the requested I2C Master Write mode or Combined Format Read mode transaction. If I2CPNTRLNGTH=1 (two byte pointer mode), this bit is ignored and both bytes are sent.

BITFIELD	BITS	DESCRIPTION
I2CDATALNGTH	14:13	I2C Transaction Data Length 00 - 1 Byte Read and Write 01 - 2 Byte Read and Write (default) 10 - 3 Byte Read, 3 or 0 Byte Write 11 - 4 Byte Read and Write This is the data length used for the requested I2C Master transaction. When I2CWALT Mode is engaged, the 3 Byte Data Length option is replaced by a 0 Byte Data option for Write mode only.
I2CDATASEL	12:11	I2C Data Location Selection 00 - Byte 0 01 - Byte 1 (default) 10 - Byte 2 11 - Byte 3 Selects the location of the data bytes(s) to be transferred during Write transactions and the target location for data byte(s) used for storage during Read transactions. The selection indicates the location of the MSByte of the data space used during the transaction, the number of bytes used is set by I2CDATALNGTH. Some limitations do apply, see data sheet for details.
I2CDEVIDEXT	10:8	I2C Device ID Extension This is the 3 Bit Device ID Extension (Slave Address[9:7]) available for I2C Master transactions in 10 Bit Address mode. This content is ignored in 7 Bit Address mode.
I2CDEVID	7:1	I2C Device ID This is the Device ID (Slave Address[6:0]) used for the requested I2C Master transaction.
I2CRWB	0	I2C R/WB Master Transaction Type 0 = Write Mode Transaction (default) 1 = Read Mode Transaction This bit determines transaction type initiated by the I2C Master in respose to a write to I2CSEND.

ID1 (0x8C)

ID1 is a read accessible register which contains the 2 LSBytes of the unique Device ID stored in ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	DEVID[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	DEVID[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DEVID	15:0	Device ID (Partial) The two least-significant bytes of the 32-bit factory-programmed device ID. ID1[0] always reads logic one. A valid device ID has two or more bits set to logic one. Read only.

ID2 (0x8D)

ID2 is a read accessible register which contains the 2 MSBytes of the unique Device ID stored in ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	DEVID[31:24]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	DEVID[23:16]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DEVID	15:0	Device ID (Partial) The most-significant byte of the 32-bit factory-programmed device ID. A valid device ID has two or more bits set to logic one. Read only.

OTP2 (0x8E)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP2[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP2[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP2	15:0	Factory Calibration Data Read Only.

OTP3 (0x8F)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP3[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP3[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP3	15:0	Factory Calibration Data Read Only.

OTP4 (0x90)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP4[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP4[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP4	15:0	Factory Calibration Data Read Only.

OTP5 (0x91)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP5[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP5[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP5	15:0	Factory Calibration Data Read Only.

OTP6 (0x92)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP6[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP6[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP6	15:0	Factory Calibration Data Read Only.

OTP7 (0x93)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP7[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP7[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP7	15:0	Factory Calibration Data Read Only.

OTP8 (0x94)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP8[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP8[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP8	15:0	Factory Calibration Data Read Only.

OTP9 (0x95)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP9[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP9[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP9	15:0	Factory Calibration Data Read Only.

OTP10 (0x96)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP10[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP10[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP10	15:0	Factory Calibration Data Read Only.

OTP11 (0x97)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	OTP11[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP11[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP11	15:0	Factory Calibration Data Read Only.

OTP12 (0x98)

Factory Calibration Data ROM and subject to ROMCRC validation.

BIT	15	14	13	12	11	10	9	8
Field	ROMCRC[7:0]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	OTP12[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ROMCRC	15:8	ROM CRC Value 8-bit CRC value computed from the onboard read-only memory content. ID and OTP ROM output data content is protected by a 8-bit CRC with polynomial 0xA6 ($x^8+x^6+x^3+x^2+1$). Read only.
OTP12	7:0	Factory Calibration Data Read Only.

Applications Information

Vehicle Applications

Battery cells can use various chemistries such as NiMH, Li-ion (NMC, LFP, LTO), SuperCap or lead-acid. SuperCap cells are used in fast-charge applications such as energy storage for regenerative braking. An electric-vehicle system may require a high-voltage battery pack voltage from 400V to 800V, which translates from 100 to 200 Li-ion cells ,or up to 500 NiMH cells. A battery module is a number of cells connected in series that can be connected with other modules to build a high-voltage battery pack, as shown in Figure 111. The modularity allows for economy, configurability, quick assembly, and serviceability. The minimum number of cells connected to any one device is limited by the device's minimum operating voltage. The 9V (min) for V_{DCIN} usually requires at least two Li-ion, six NiMH or six SuperCap cells per module.

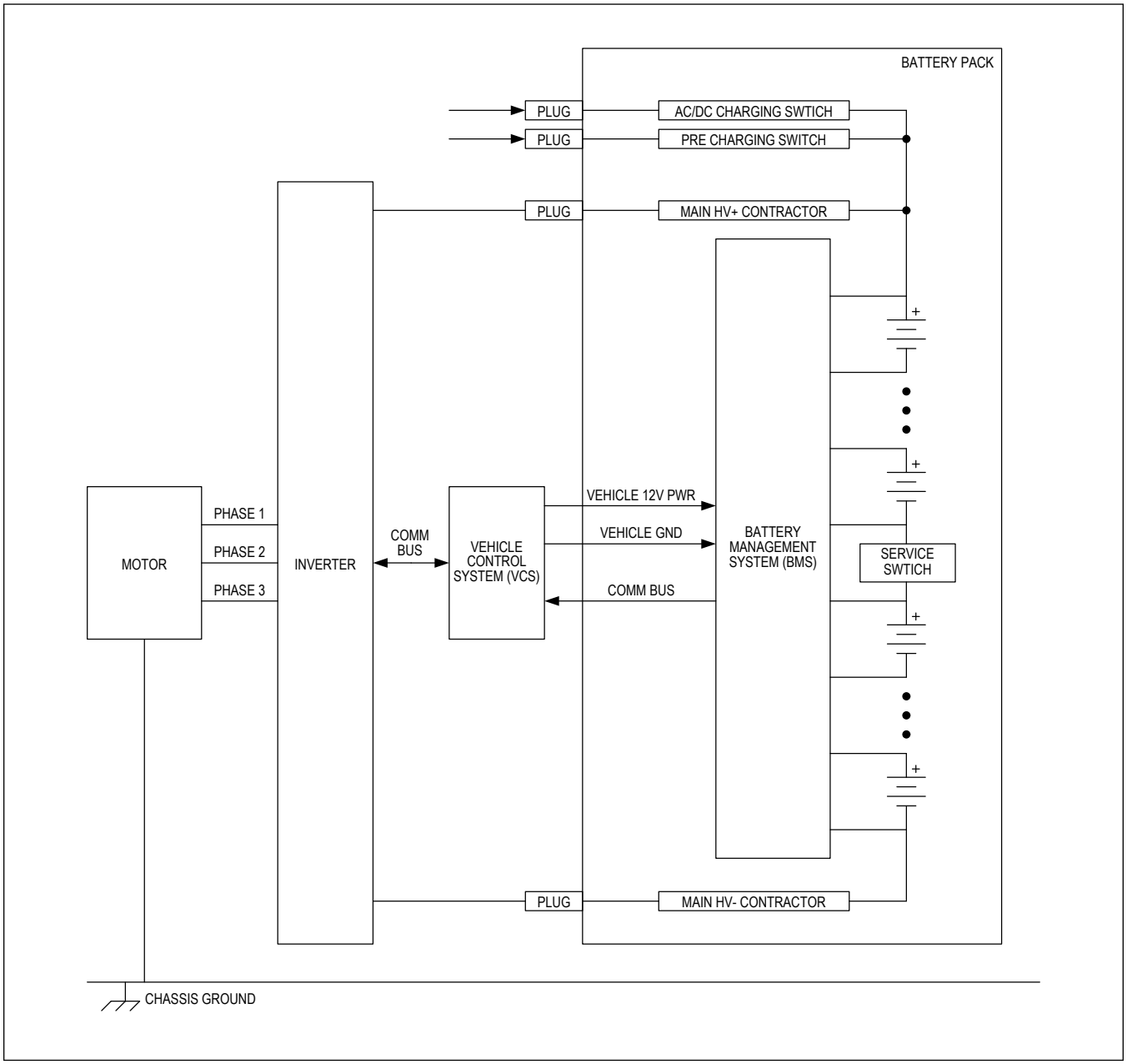


Figure 111. Electric Vehicle System

Battery Management Systems

Daisy-Chain System

A daisy-chain system employs a communication link between the host microcontroller and all the battery modules. The daisy-chain method reduces overall system cost as it requires only a single microcontroller, CAN PHY, and transformers between the lowest module and the host, whereas all components would require redundant implementation in a non-

daisy chain (distributed CAN system). Refer to the following Distributed CAN System section for further information regarding its implementation.

Daisy-Chain System

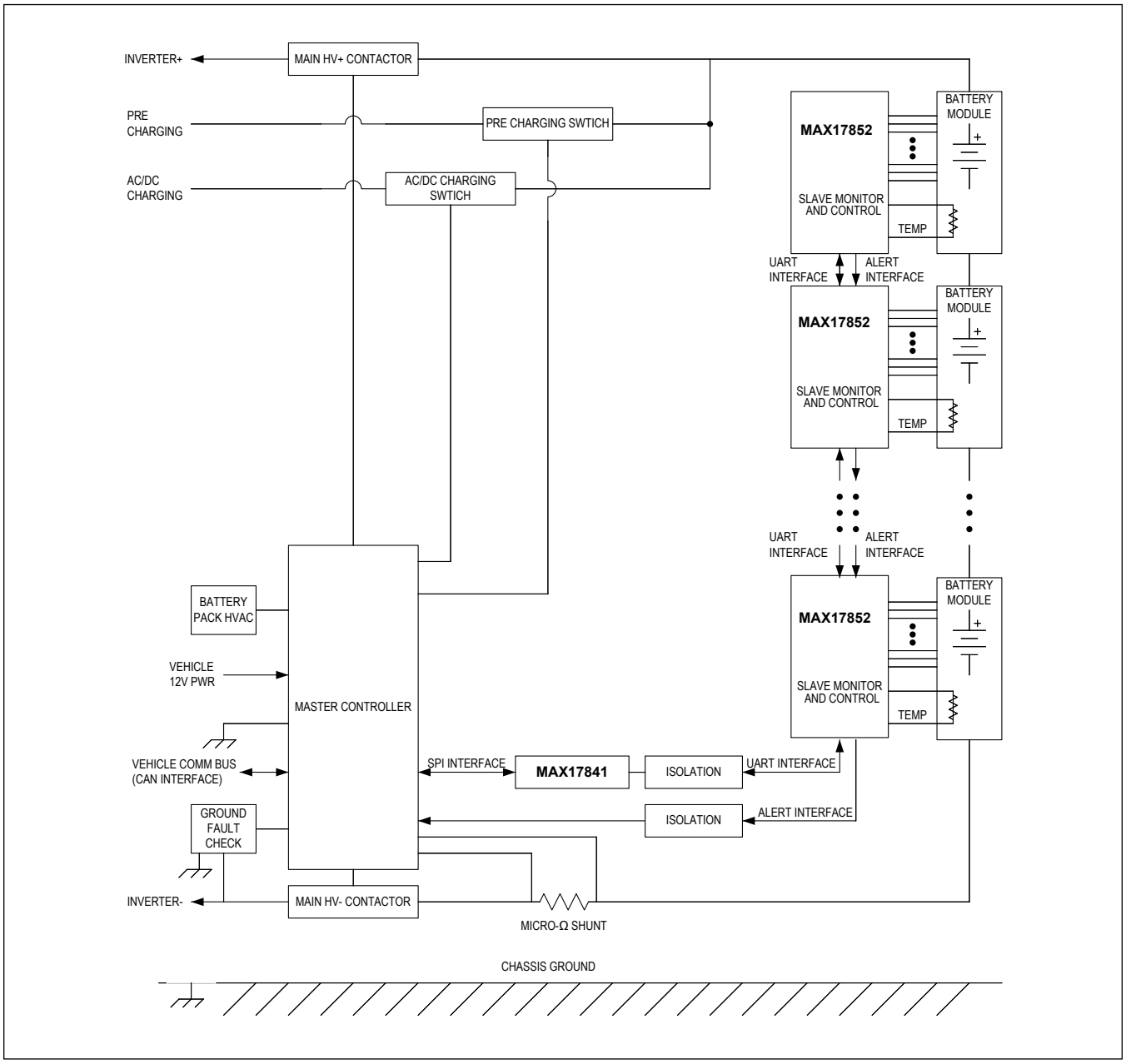


Figure 112. Daisy-Chain System

Daisy-Chain System with CSA

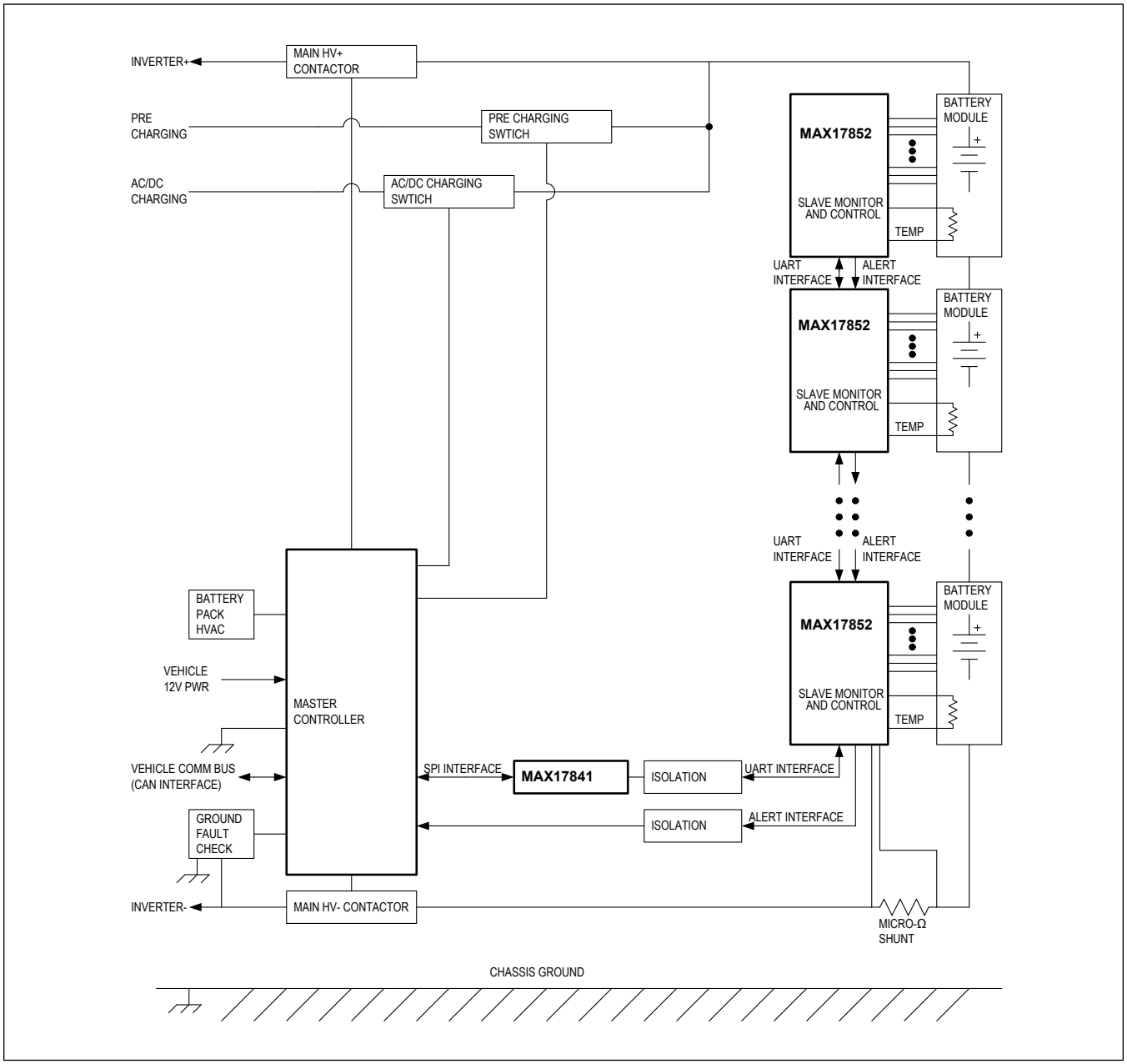


Figure 113. Figure: Daisy-Chain System with CSA

Distributed CAN Systems

A Distributed CAN System as shown below in Figure 114 employs an individual CAN communication interface, battery management microcontroller, and transformer isolation between each battery module and master controller/ECU. This system architecture, although realizable, yields increased system cost.

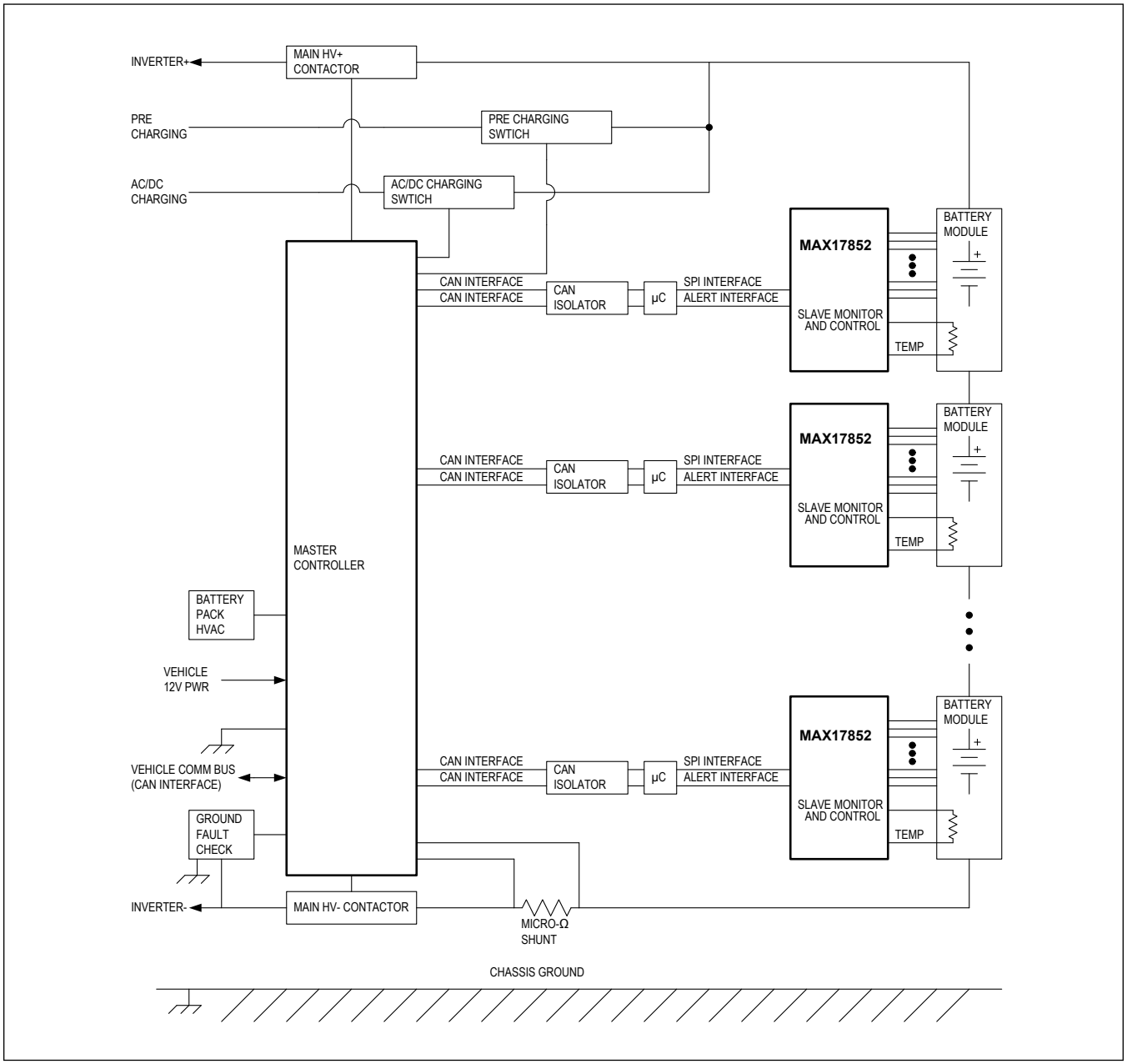


Figure 114. Distributed System

48V System

A 48V mild HEV battery system as shown in Figure 115 monitors a single battery pack typically using 13-14 cells. As such, the system requires only a single battery module that directly interfaces with the battery system micro-controller. Due to the intermediate voltage rating, there is no requirement for the interface isolation that is seen on the previous Daisy Chain and Distributed CAN systems.

The MAX17852 can be adapted to fit this application by appropriately configuring the UARTSEL pin to enable the SPI

communication interface. Additionally, the V_{DDL2} and V_{DDL3} supplies can be directly tied to the battery system microcontroller (3.3V -5V) to eliminate the need for any level shifting that would have otherwise been required.

The system can also take advantage of the internal push-pull or open-drain alert interface configuration to easily identify any number of safety critical faults.

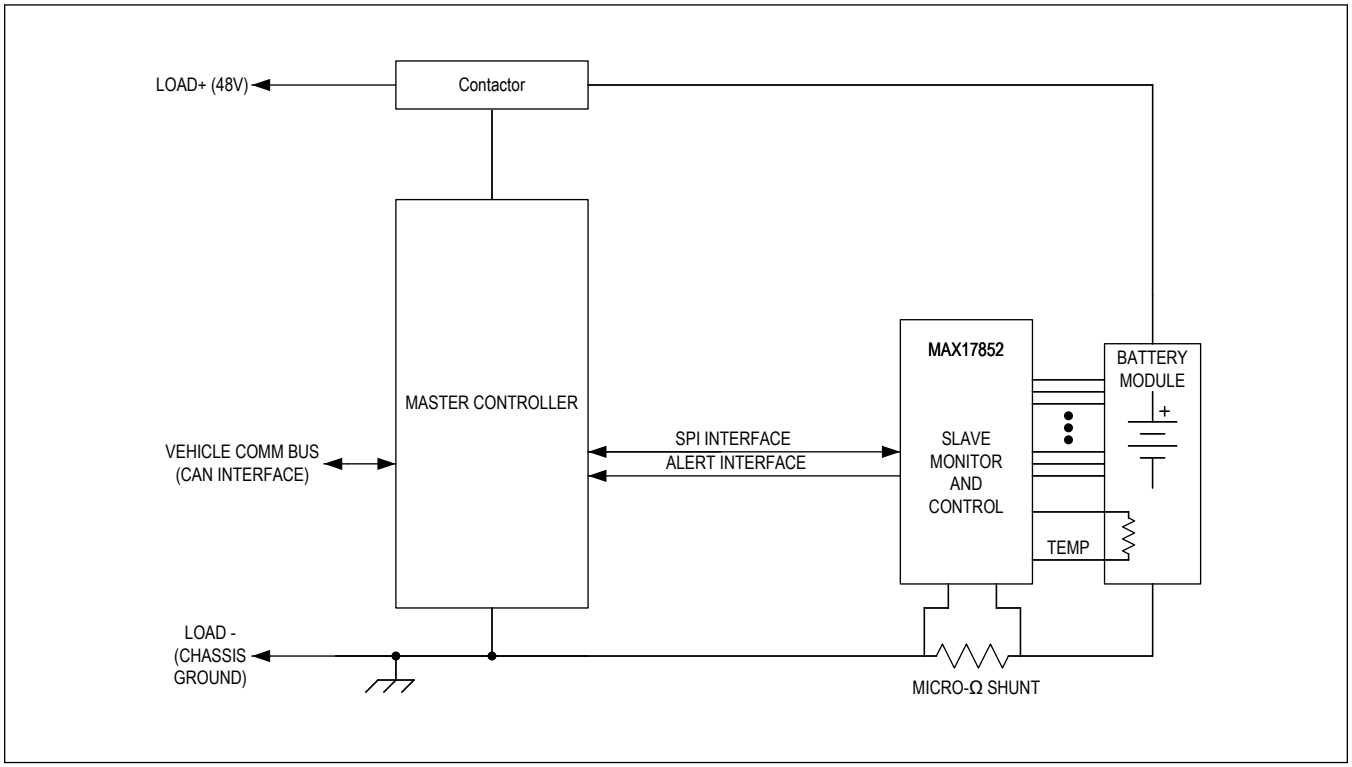


Figure 115. 48V System

Standard Module Configuration

Power Supply Connection

In a standard module configuration, both internal and external protection circuits permit the MAX17852 to derive its supply directly from the battery module voltage using a filter network connecting the DCIN input to the top cell of the battery pack. These protection circuits protect against transients such as those that can occur when the battery voltage is first connected to the device, when the vehicle inverter is connected to the battery stack, or during charge/discharge transitions such as regenerative braking. The internal circuits include 72V tolerant battery inputs and a high-noise rejection ratio (PSRR) for the internal low-voltage regulator.

The external protection circuit shown below in Figure 116 filters and clamps the DCIN input. During negative-voltage transients, the filter capacitor maintains power to the device through the transient.

For maximum measurement accuracy, dedicated wires separate from the cell sense wires should be used for the power-supply connection (Kelvin sense). This eliminates voltage drops in the sense wires induced by supply current. If the application can tolerate the induced error, the supply wires can serve as the sense wires to reduce the wire count.

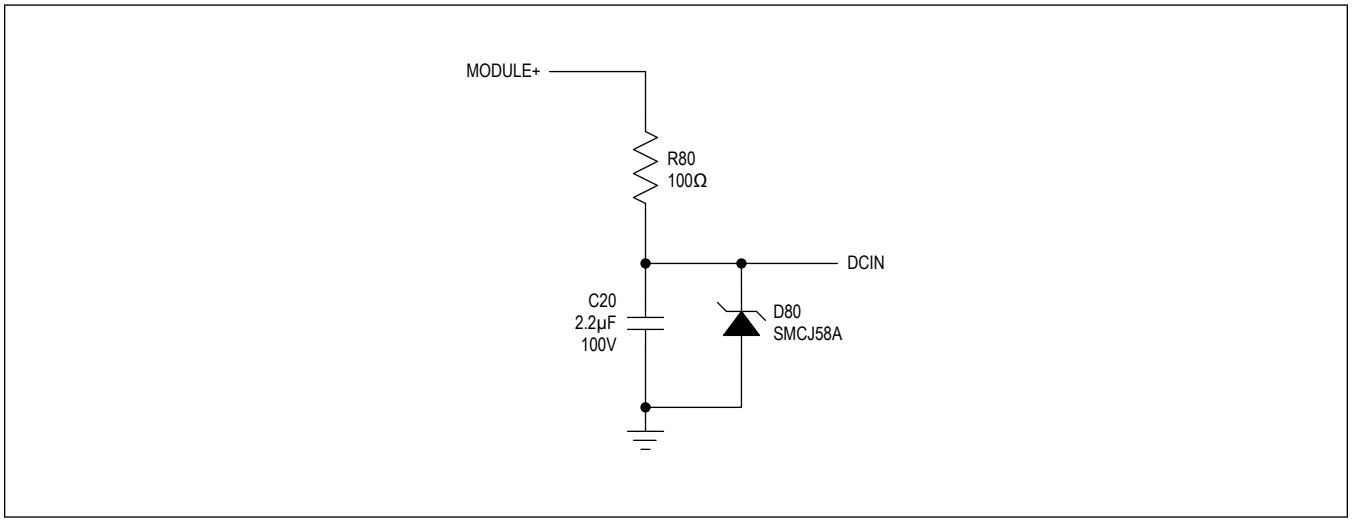


Figure 116. Power-Supply Connection

Connecting Cell Inputs

As mentioned in the previous section, the DCIN input should be connected to the battery module's top cell to prevent charge imbalance between cells. If the battery module contains less than 14 cells, the lowest order inputs (e.g., C1 and C0) should be utilized first and connected to the lowest common-mode signals. Any unused cell inputs should be shorted together, and unused switch inputs should also be shorted together. The TOPCELL register must also be configured for stacks with less than 14 cells to mask out any false alerts corresponding to the unused channels.

Flexible Pack Configuration

Power Supply, Cell Input Configuration

The Flexible Pack (Flex Pack) Configuration provides system flexibility such that a single MAX17852 can meet the requirements of: varying battery module configuration(s) used across multiple mild EV, HEV, BEV distributed daisy chain systems, as well as distributed daisy chain system which employ un-equal module sizes within a standard battery pack.

This flexibility is allowed through internal supply routing of the top battery cell as well as internal signal routing of the block voltage where these connection were otherwise required by a discrete external traces. Due to this internal routing, the BOM cost may be reduced through the elimination of the DCIN filter resistor as well as the block voltage measurement filter. Unused channels are left unconnected allowing for any battery wiring harness to connect to a standard battery module. Pleas refer to the Flexible Pack Configuration for further details on implementation.

For non-distributed daisy-chain systems (centralized systems), the Flex Pack eliminates the need to route external sense wires as the voltage drops from the cell cabling, which can be significantly reduced using the FLXPCKSCAN bit in the PACKCFG register, resulting in total BOM cost reduction, as well as eliminating system cost and constraints for calibration.

External Cell-Balancing

The cell-balancing current can be switched by external transistors if more power dissipation is required. The internal switches can be used to switch the external transistors and the power is limited by external current-limiting resistors.

External Cell-Balancing using FET Switches

An application circuit for cell-balancing that employs FET switches is shown in Figure 117. $Q_{BALANCE}$ is selected for low V_T that meets the minimum V_{CELLn} requirements of the application during balancing. D_{GATE} protects $Q_{BALANCE}$ from

reverse V_{GS} voltage during a hot-plug event. R_{GATE} protects the device by limiting the hot-plug inrush current. C_{GATE} may be added to attenuate transient noise coupled from the drain to the gate to maintain the transistor bias. The cell-balancing current is limited by $R_{BALANCE}$. The various external cell balancing summary components are as shown in Table 82.

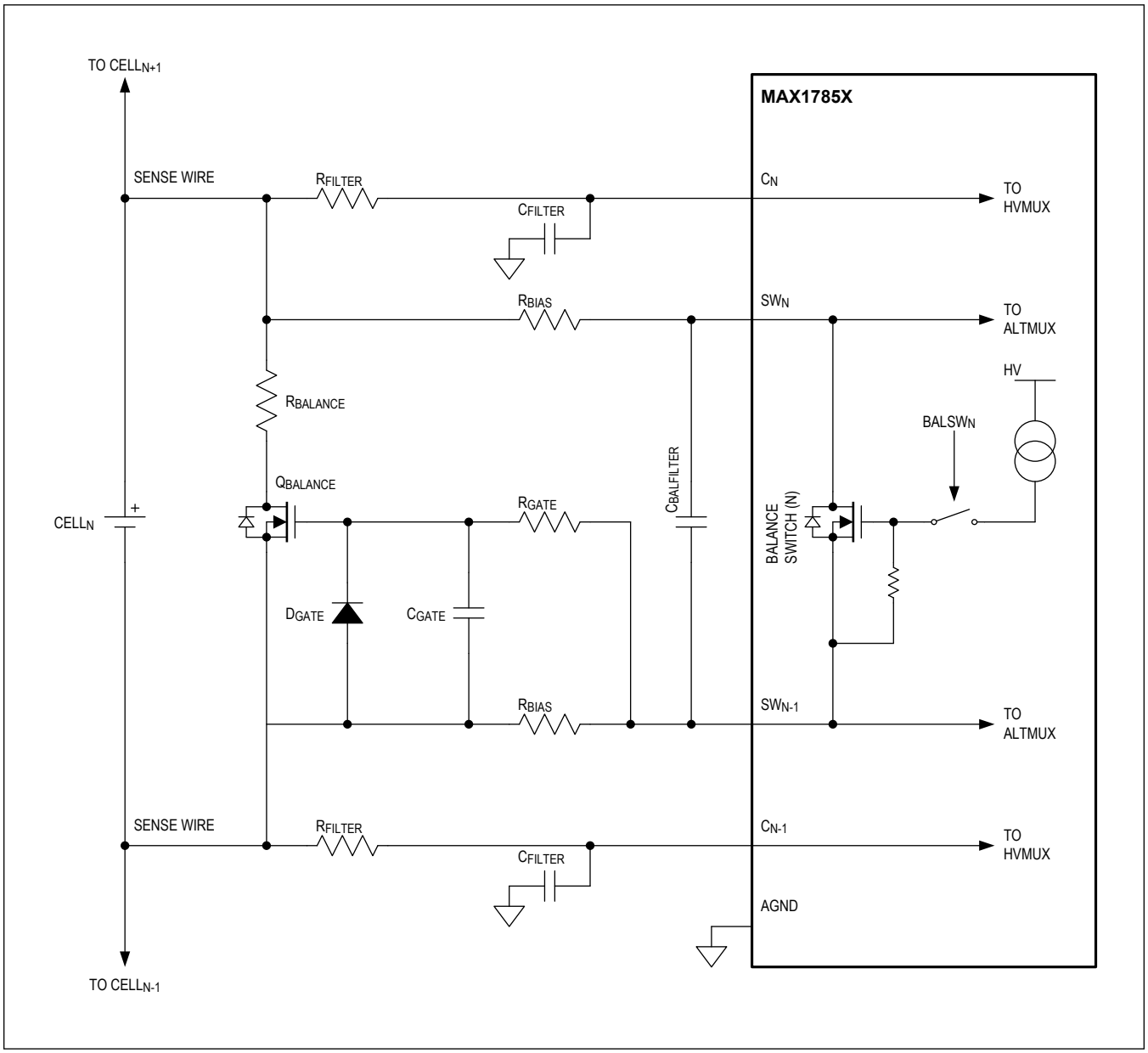


Figure 117. External Balancing-FET

Table 82. FET-Balancing Components

COMPONENT NAME	TYPICAL VALUE OR PART	FUNCTION
R_{BIAS}	1kΩ	Voltage-divider for transistor bias

Table 82. FET-Balancing Components (continued)

COMPONENT NAME	TYPICAL VALUE OR PART	FUNCTION
R_{GATE}	100Ω	Hot-plug current-limiting resistor
D_{GATE}	S1B	Reverse-voltage gate protection
C_{GATE}	1nF	Transient V_{GS} suppression
$R_{BALANCE}$	Per application	Balancing current-limiting resistor
$Q_{BALANCE}$	SQ2310ES	External switch

External Cell-Balancing using BJT Switches

An application circuit for cell-balancing that employs BJT switches is shown in Figure 118. $Q_{BALANCE}$ is selected for power dissipation based on the IB drive current available and the cell-balancing current. D_{BASE} protects $Q_{BALANCE}$ from negative V_{GS} during hot-plug events. R_{BASE} protects the device by limiting the hot-plug inrush current. The cell-balancing current is limited by $R_{BALANCE}$. The various external cell-balancing summary components are as shown in Table 83.

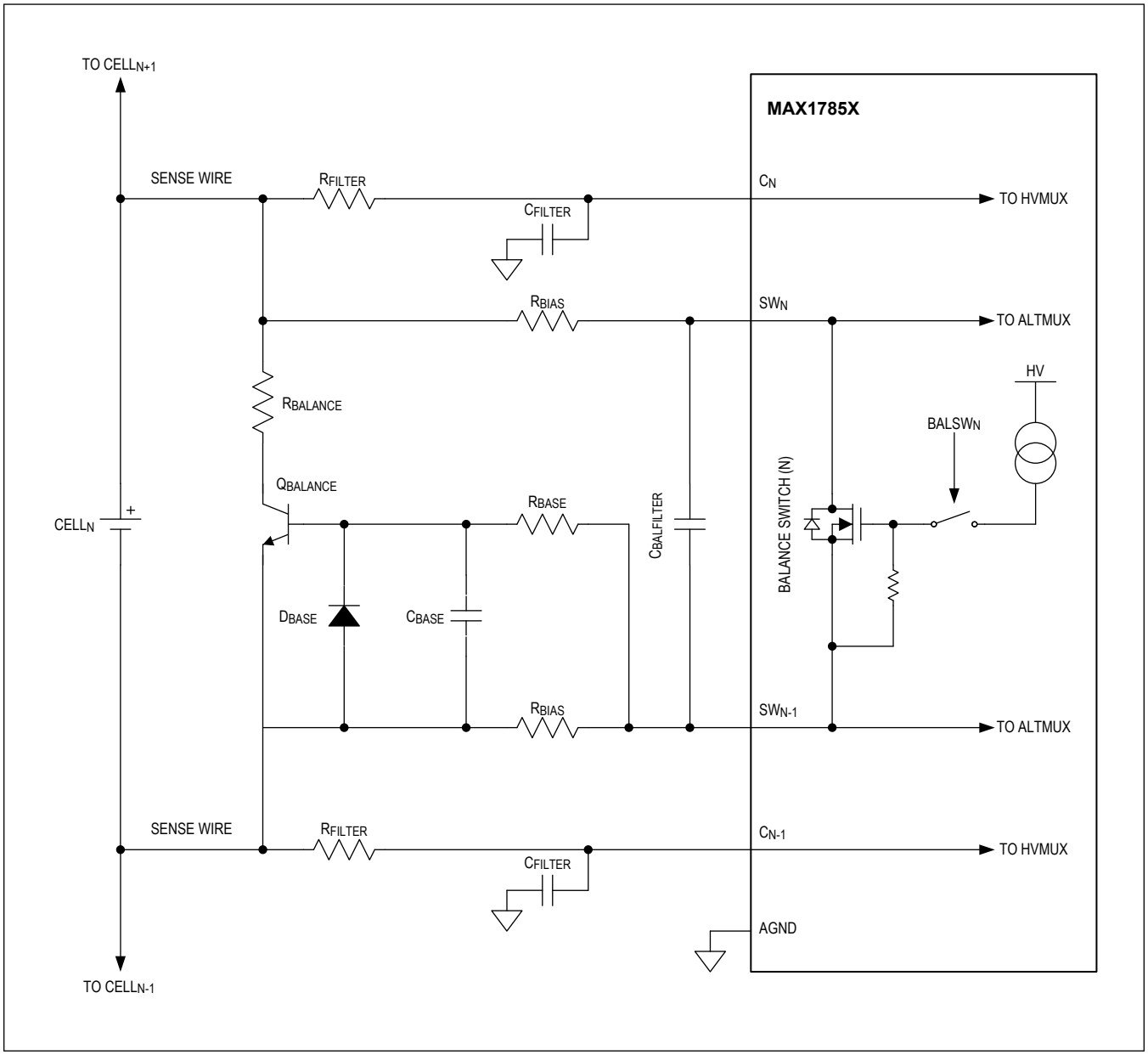


Figure 118. External Cell Balancing-BJT

Table 83. BJT Balancing Components

COMPONENT NAME	TYPICAL VALUE OR PART	FUNCTION
R_{BIAS}	22Ω	Voltage-divider for transistor bias
R_{BASE}	15Ω	Hot-plug current-limiting resistor
D_{BASE}	S1B	Reverse emitter-base voltage protection
C_{BASE}	1nF	Transient VBE suppression
$R_{BALANCE}$	Per balancing current requirements	Balancing current-limiting resistor

Table 83. BJT Balancing Components (continued)

COMPONENT NAME	TYPICAL VALUE OR PART	FUNCTION
$Q_{BALANCE}$	NST489AMT1	External switch

External Cell-Balancing Short-Circuit Detection

A short-circuit fault in the external balancing path results in continuous current flow through $R_{BALANCE}$ and $Q_{BALANCE}$. To detect this fault, the voltage drop across the sense-wire parasitic resistance must be measurable. A very small series resistor may added for this purpose.

UART Interface

The UART pins employ both internal and external circuits to protect against noise. The recommended external filters are shown in Figure 119. ESD protection is shown in Figure 121 and Figure 122.

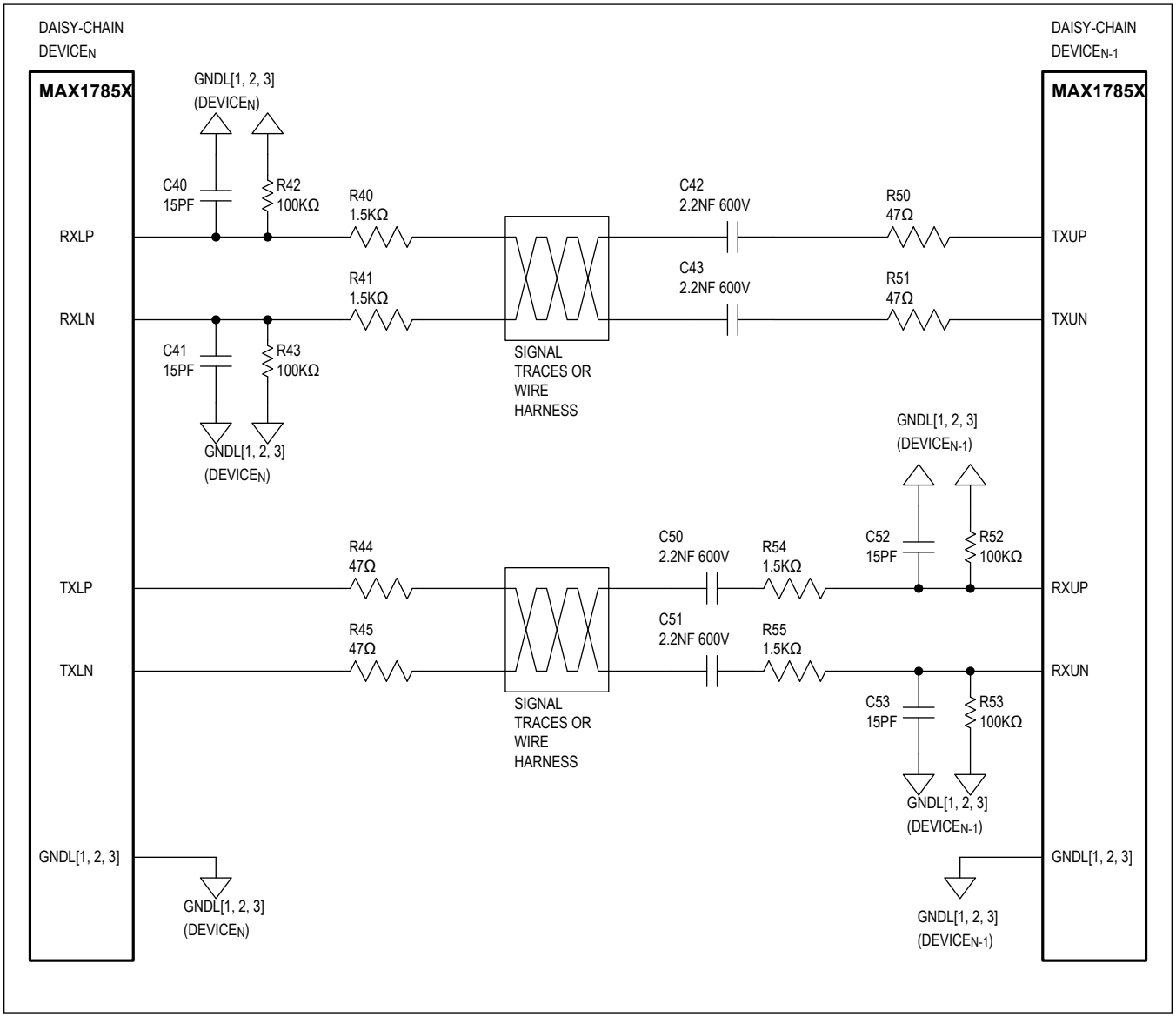


Figure 119. UART Connection

High-Z Idle Mode

The high-Z idle mode lowers radiated emissions from wire harnesses by minimizing the charging and discharging of the AC-coupling capacitors when entering and exiting the idle mode. The application circuit shown in Figure 120 uses a weak resistor-divider to bias the Tx lines to V_{DDL} during the high-Z idle period and pnp transistor clamps to limit the maximum voltage at the Tx pins during high noise injection. The resistor-divider and pnp clamps are not needed for applications utilizing only the low-Z mode. The low-Z and high-Z idle modes both exhibit a similar immunity to noise injection. Low-Z mode may be preferred for ports driving inductive loads to minimize ringing.

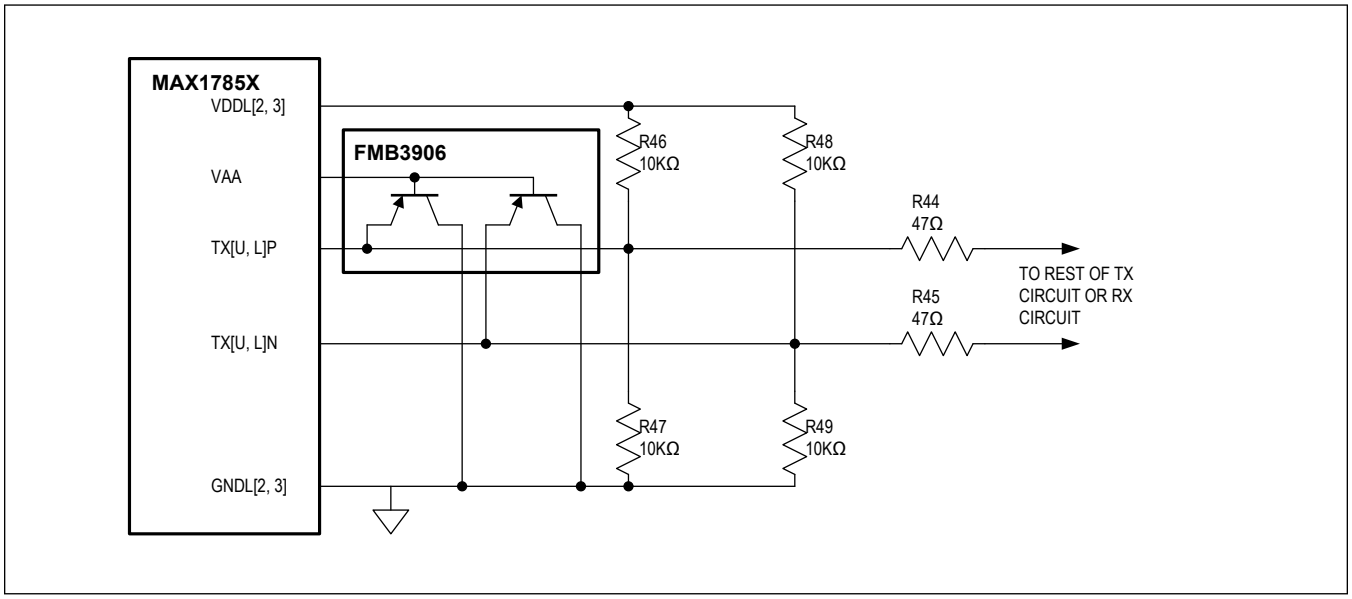


Figure 120. High-Z Idle Mode Application Circuit

UART Supplemental ESD Protection

The UART ports may require supplemental protection to meet IEC61000-4-2 requirements for contact discharge. The recommended circuits to meet ±8kV protection levels are shown in Figure 121 and Figure 122. The protection components should be placed as near as possible to the signal's entry point on the PCB.

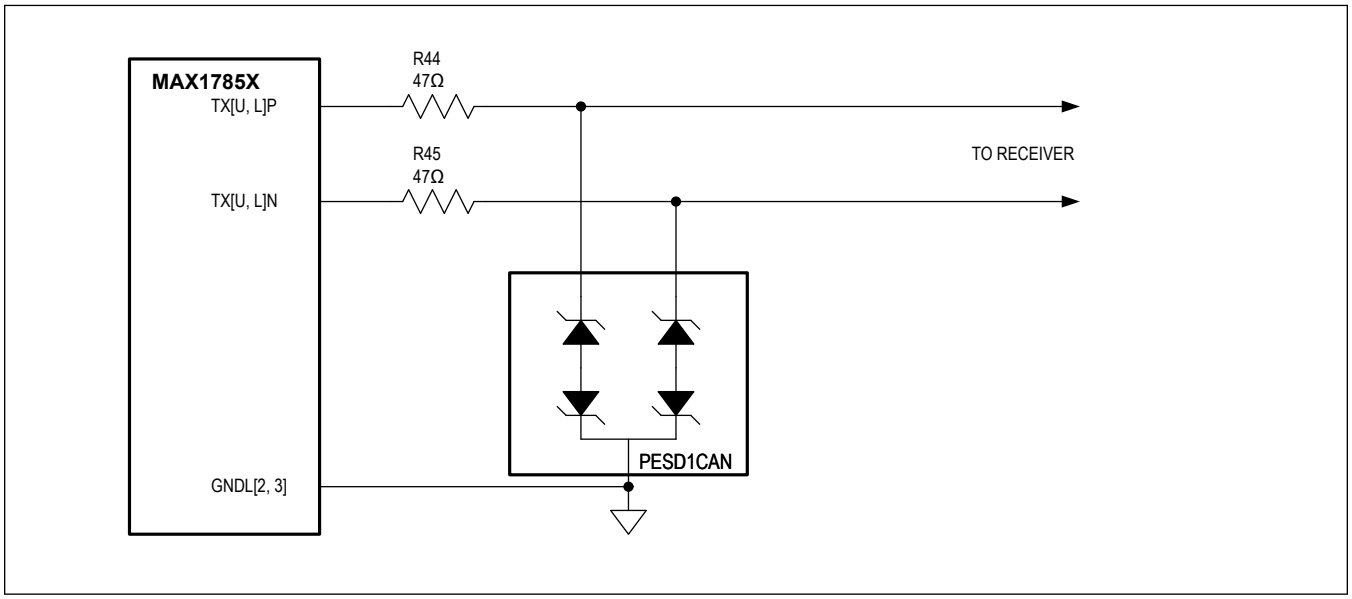


Figure 121. External ESD Protection for UART TX Ports

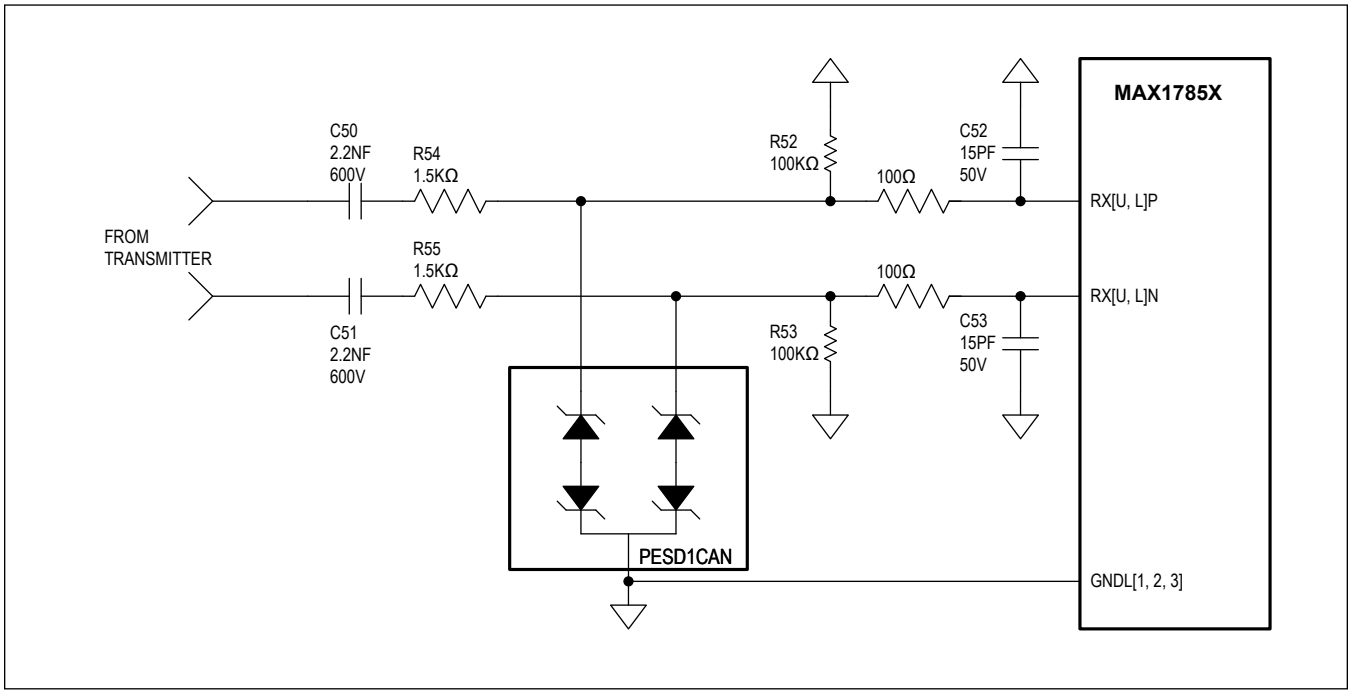


Figure 122. External ESD Protection for UART RX Ports

Single-Ended RX Mode

To configure the lower port for single-ended RX mode, the RXLP input is connected to digital ground and the RXLN input receives the inverted signal, just as it does for differential mode. If the host cannot transmit the inverted data, then the signal must be inverted as shown in Figure 123. Transmitter operation is not affected. If the up-stack device is single-ended, then only the TXUN signal is required.

Note: In single–ended mode, SHDNL must be driven externally.

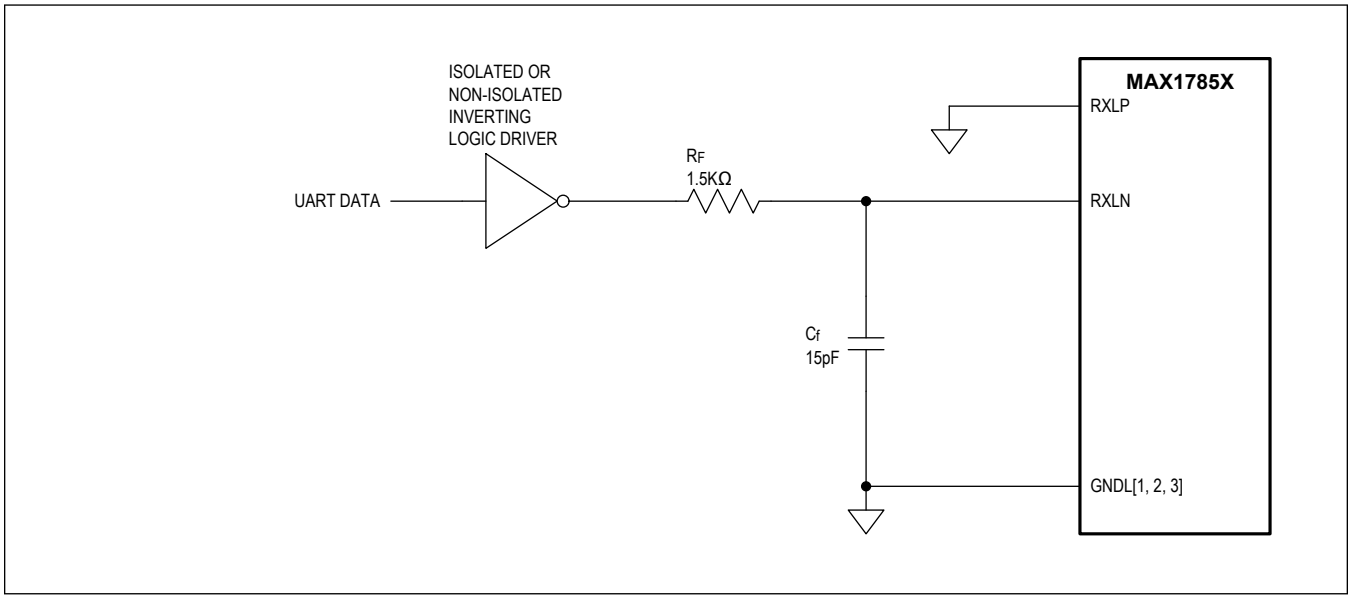


Figure 123. Application Circuit for Single-Ended UART Mode

UART Isolation

The UART is expected to communicate reliably in noisy high-power battery environments where both high dV/dt supply noise and common-mode current injection induced by electromagnetic fields are prevalent. Common-mode currents can also be induced by parasitic coupling of the system to a reference node such as a battery or vehicle chassis. The daisy-chain physical layer is designed for maximum noise immunity.

The AC-coupled differential communication architecture has a ±30V common-mode range and +6V differential swing. This range is in addition to the static common-mode voltage across the AC-coupling capacitors between modules. Transmitter drivers have low internal impedance and are source-terminated by the application circuit so that impedances are well matched in the high- and low-driver states. This architecture minimizes differential noise induced by common-mode current injection. The receiver inputs are filtered above the fundamental communication frequency to prevent high-frequency noise from entering the device. The system is designed for use with isolation transformers or optocouplers to provide an even higher degree of common-mode noise rejection in circuit locations where extremely large common-mode noise is present, such as between vehicle chassis and the high-voltage battery-pack terminals.

Since a mid-pack service disconnect safety switch is present in many battery packs, the device is designed to communicate with the entire daisy-chain whether the service-disconnect switch is engaged or open. This is possible with daisy-chains that employ capacitor isolation.

UART Transformer Isolation

The UART ports may be transformer-coupled because of their DC-balanced differential design. Transformer coupling between the MAX17841B interface and the MAX1785x provides excellent isolation and common- mode noise rejection. The center-tap of a signal transformer may be used to enhance common-mode rejection by AC-coupling the node to local ground. Common-mode currents that are able to pass through the parasitic coupling of the primary and secondary are shunted to ground to make a very effective common-mode noise filter.

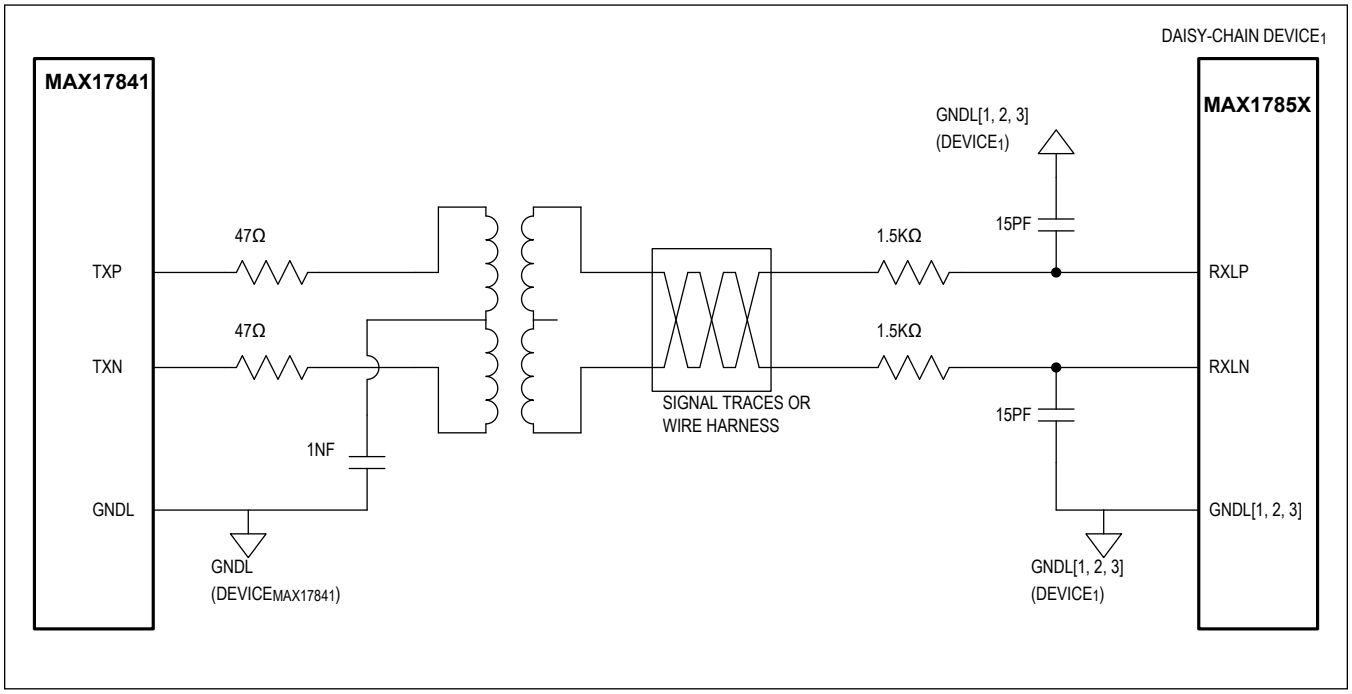


Figure 124. UART Transformer Isolation

UART Optical Isolation

The daisy-chain may use optical isolation instead of transformer or capacitor isolation as shown in Figure 125.

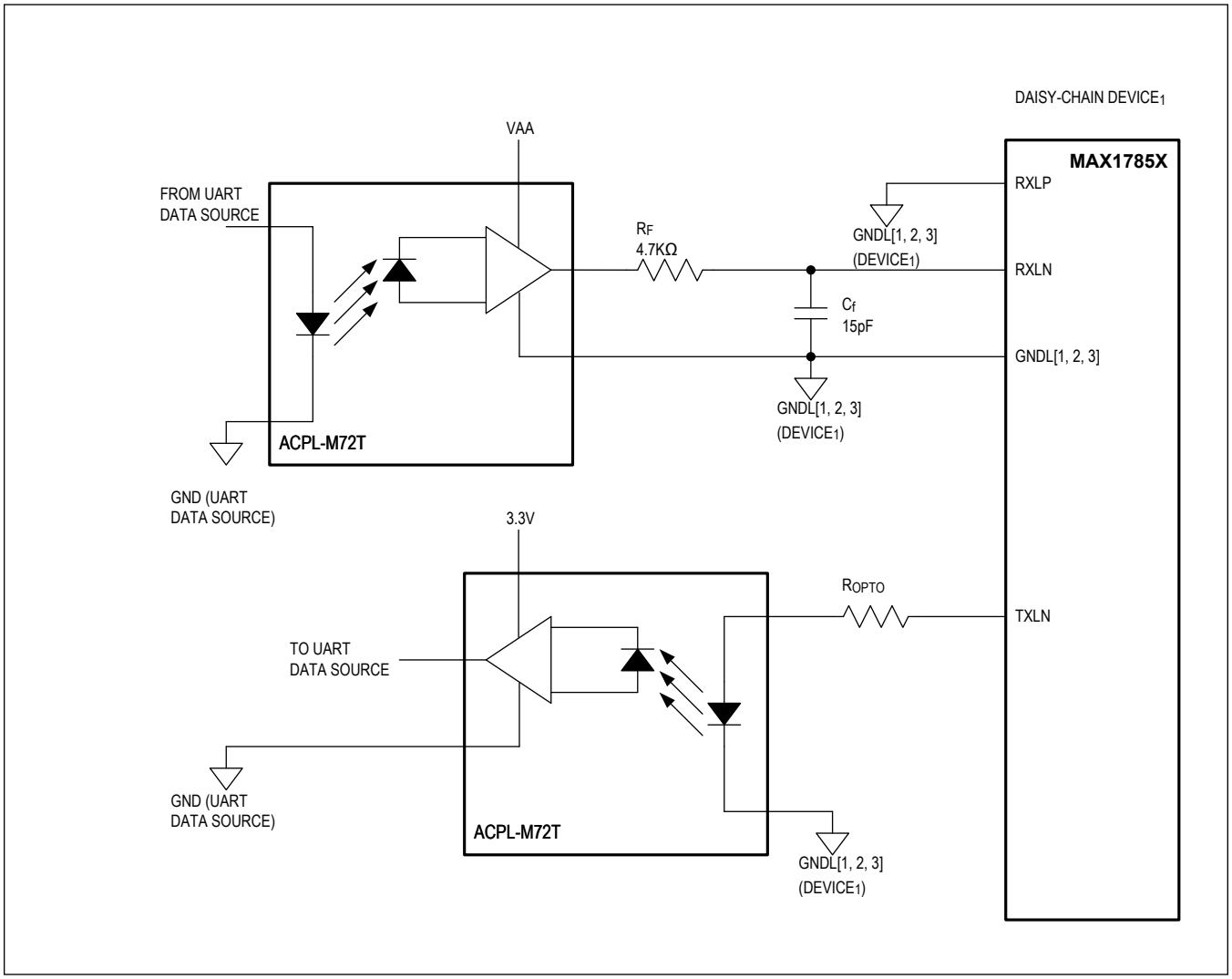


Figure 125. UART Optical Isolation

SPI Interface

V_{DDL2} and V_{DDL3} are the supply pins for the SPI communication. SPI communication supports both 5V and 3.3V. The SPI supply configuration with 5V provided by the system is shown in Figure 126.

The SPI supply configuration with 3.3V provided by the device's V_{AA} LDO output is shown in Figure 127.

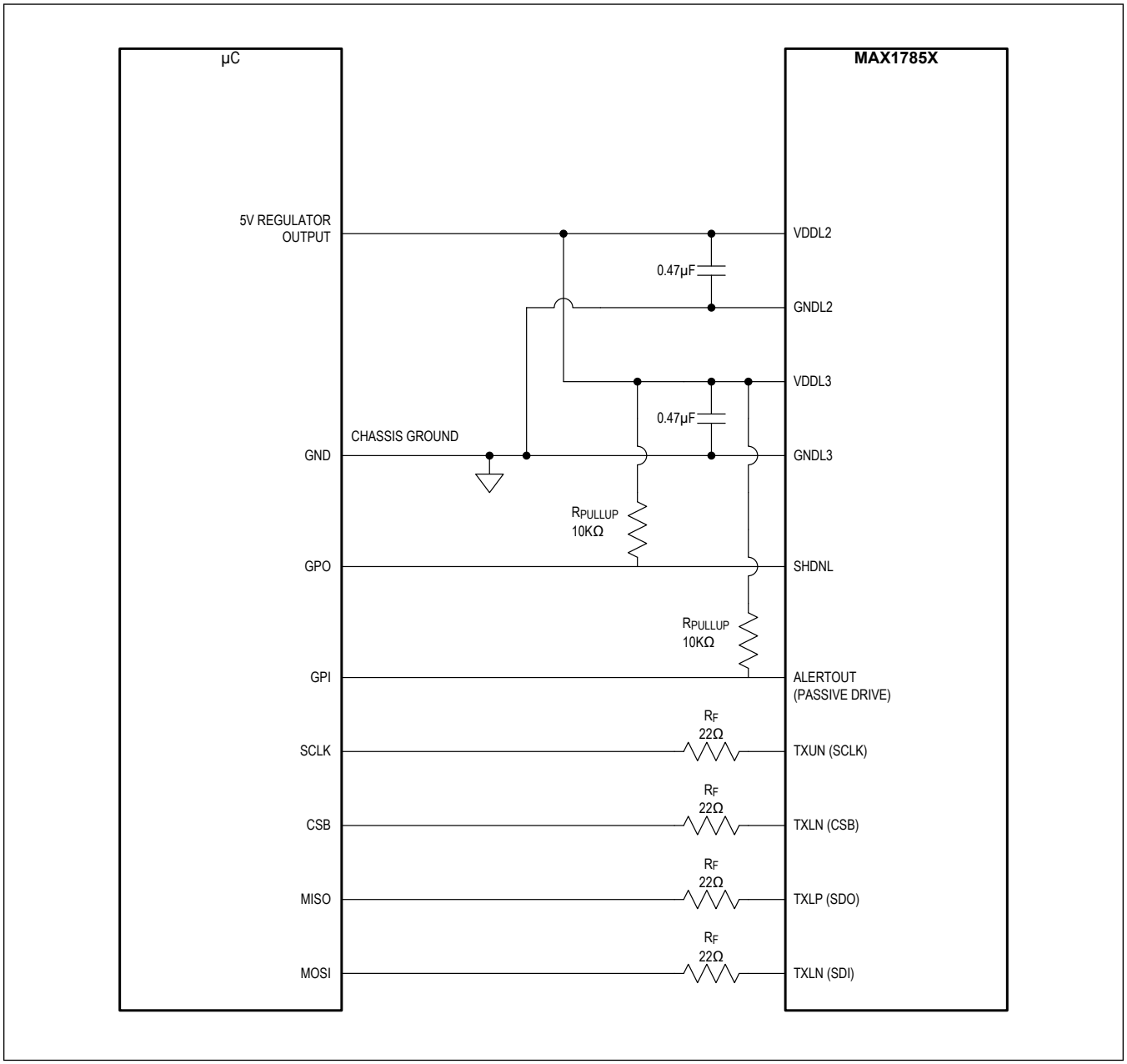


Figure 126. 5V SPI Supply from System

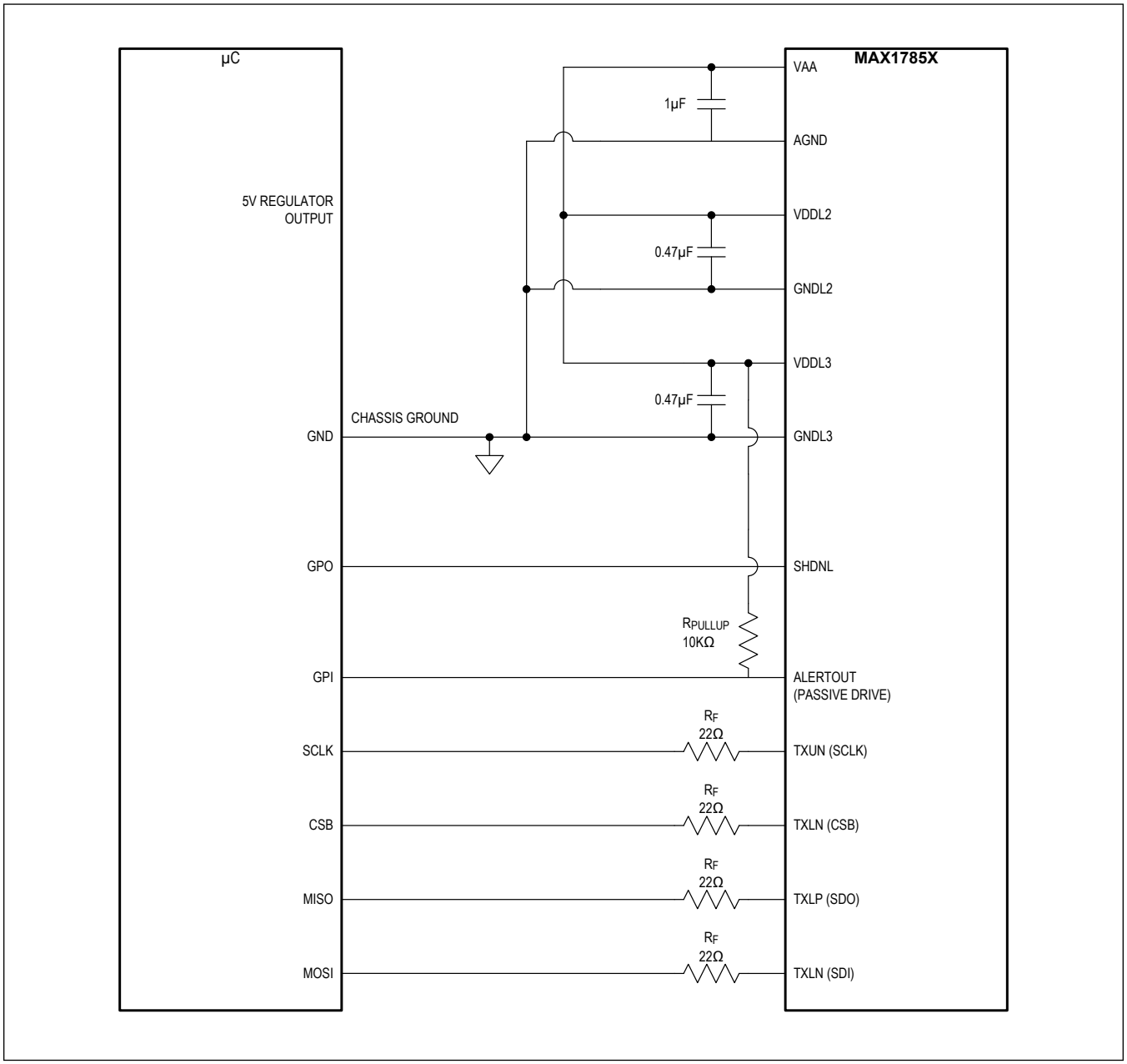


Figure 127. 3.3V SPI Supply from Device V_{AA} LDO

ALERT Interface

V_{DDL2} and V_{DDL3} are the supply pins for the ALERT interface. When using differential ALERT interface in the UART daisy chain configuration, the recommended external filters and ESD protection is same as the UART Interface. When using single-end ALERT interface (i.e., ALERTIN and ALERTOUT pins) in the UART daisy chain, optical isolation is used as shown in Figure 128.

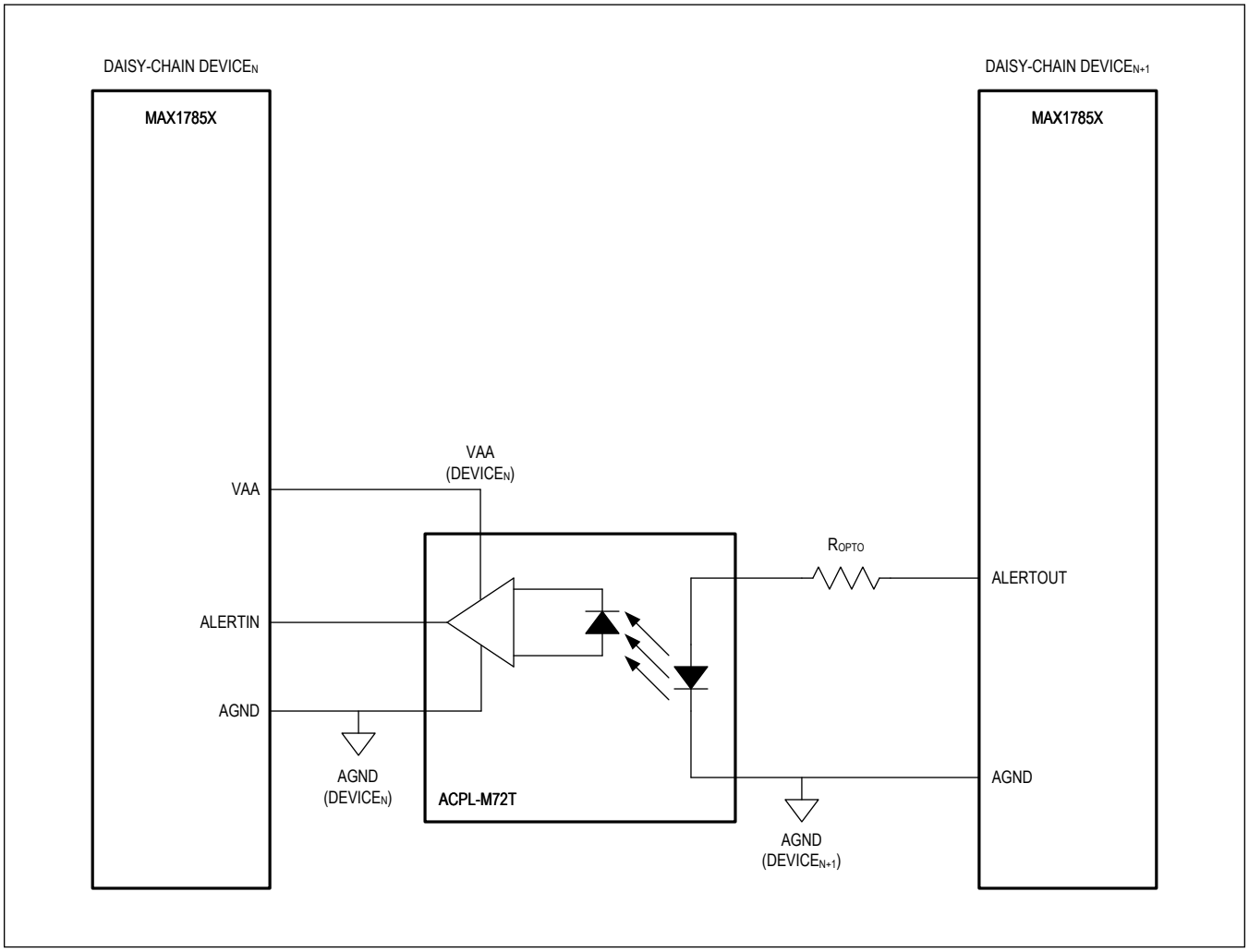


Figure 128. Single-End ALERT Interface in UART mode

In the SPI mode, one MAX1785X is applied in the system. System can choose to supply V_{DDL2} and V_{DDL3} from system's 5V or device's V_{AA} LDO output. An active CMOS ALERTOUT output setting in the system is shown in Figure 129.

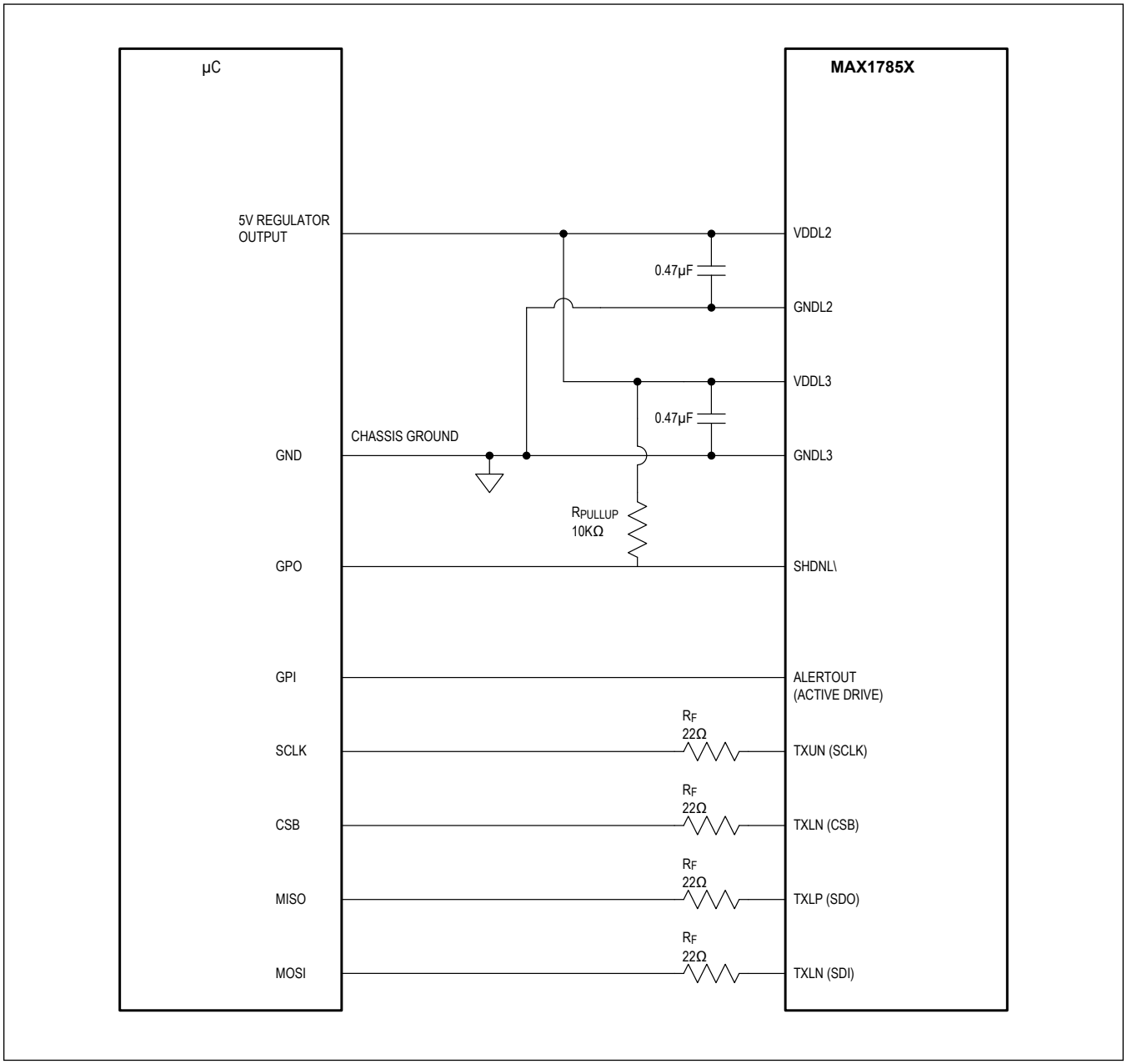


Figure 129. Single-End ALERT Interface in SPI mode - Active Drive

A passive pullup ALERTOUT setting in the system is shown in Figure 130.

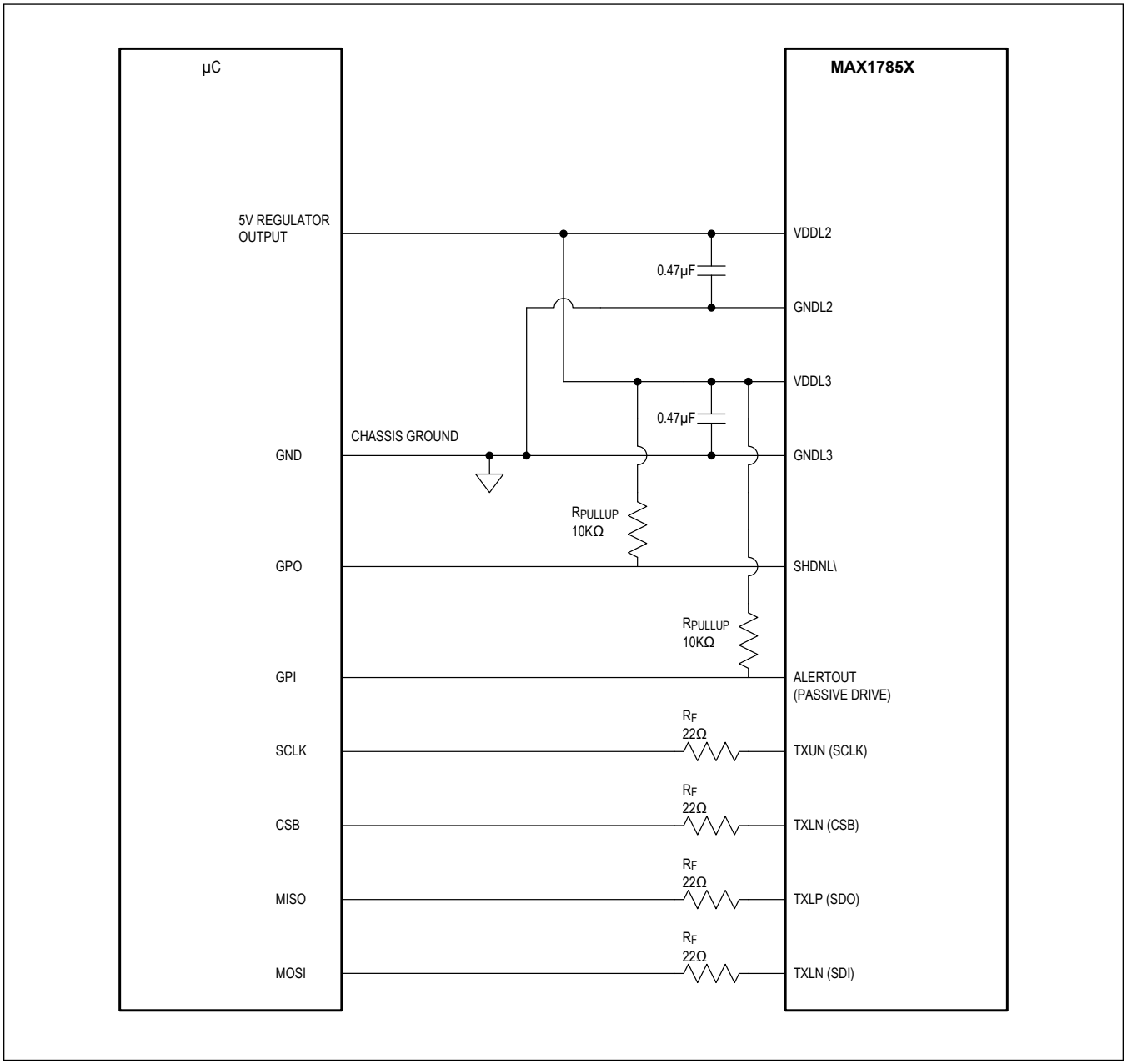


Figure 130. Single-End ALERT Interface in SPI mode - Passive Drive

Device Initialization Sequence

Immediately after reset, all device addresses are set to 0x00 and the UART baud rate and receive modes have not been auto-detected. Therefore the following initialization sequence is recommended after every reset or after any change to the hardware configuration:

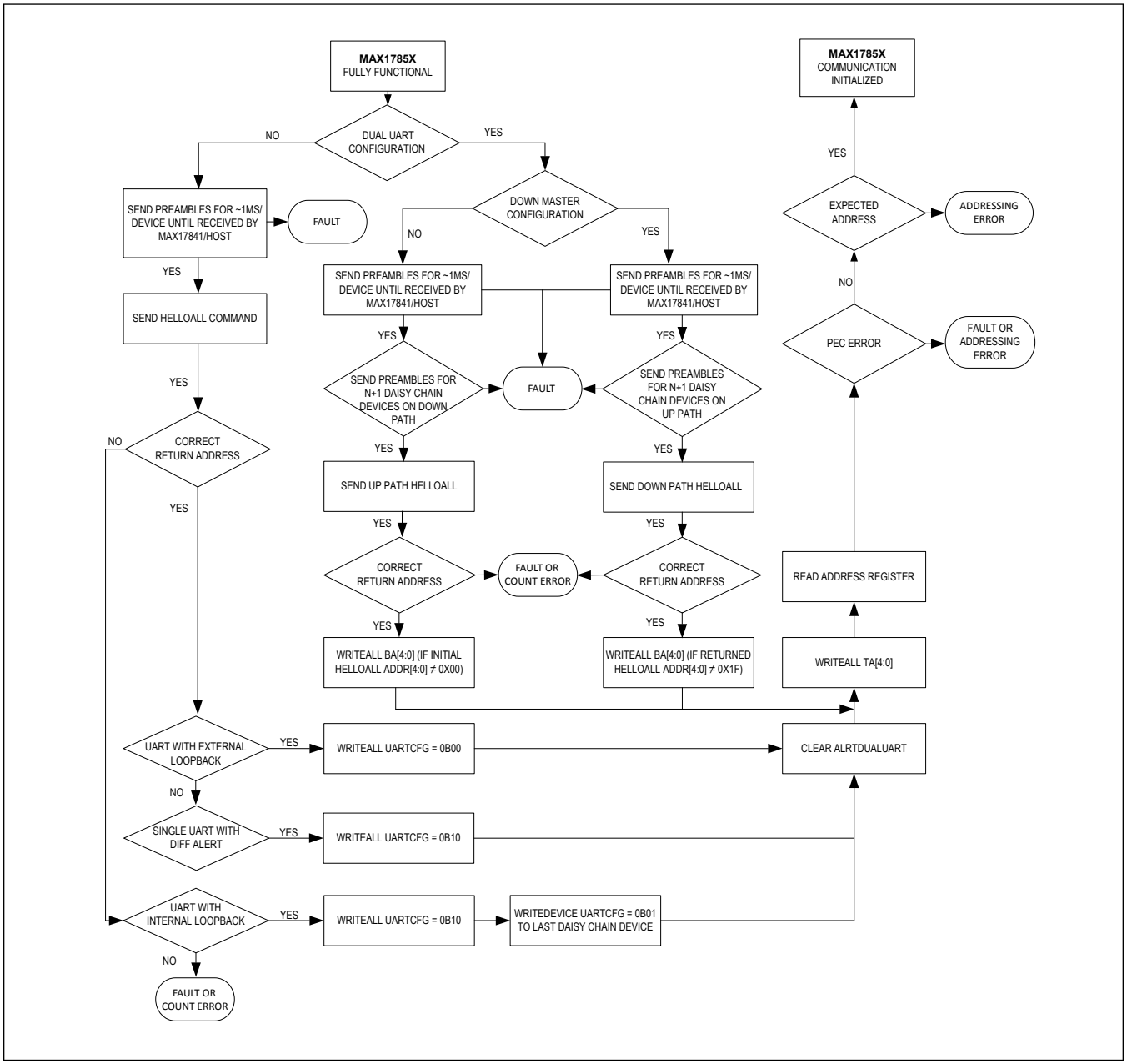


Figure 131. Device Initialization Sequence

Error Checking

Data integrity is provided by Manchester encoding, parity, character framing, and Packet-Error Checking (PEC). The combination of these features verifies stage-to-stage communication, in both the write and read directions, with an HD (Hamming Distance) value of 6 for commands with a length up to 247 bits (counted prior to Manchester encoding and character framing. This is equivalent to the longest possible command packet for a daisy chain of up to 13 devices. The data-check byte is present in the READALL and READDEVICE commands to verify that the entire command propagated

without errors. Using the data-check and PEC bytes, complete transaction integrity for READALL and READDEVICE command packets can be verified.

PEC Errors

If the MAX17852 receives an invalid PEC byte, the corresponding ALRTPECUP, or ALRTPECDN bit in the STATUS2 register, and the summary ALRTPEC bit in the STATUS1 register are set. All single-UART configurations set the ALRTPECUP bit, since the Up path is used for received transactions. In a dual-UART configuration, a PEC error in the Up path sets ALRTPECUP, and a PEC error in the Down path set the ALRTPECDN. The MAX17852 does not execute/accept any written commands unless the received PEC byte matches the calculated CRC Remainder, confirming the validity of the received command and data stream. To confirm the command was accepted, the host should perform an appropriate read transaction to verify the contents of the written register(s).

PEC Calculations

When directly communicating with the MAX17852 through the UART interface, the host must compute and send the PEC byte, protecting the data sent to the device. Likewise, for returned read packets, the host should store the received data, perform the CRC calculation, and compare the results to the received PEC byte provided by the MAX17852 before accepting the data received as valid. To support PEC-byte computation and checking, the host must implement a CRC-8 (8-bit cyclic-redundancy check) encoding and decoding algorithm based on the following polynomial (0xA6):

$$P(x) = x^8 + x^6 + x^3 + x^2 + 1$$

This polynomial is capable of protecting a data stream of up to 247 bits with a Hamming distance of three, meaning any data stream 247 bits or less in length with any combination of 3 bits of error or less is guaranteed to be identified. If more than 3 bits of error are encountered, the PEC operation will very likely identify the problem, though this cannot be mathematically guaranteed.

A hardware implementation of the CRC calculation is shown in Figure 132. The CRC Engine shown is implemented internally within the MAX17852; a similar implementation would be required in the host to support direct UART communication, for purposes of generating the PEC Bytes sent to the MAX17852, or for checking PEC Bytes received from the MAX17852. The incoming UART data stream is fed into the CRC Engine, LSB first. Once the data stream has been completely shifted into the engine, the CRC Remainder is known; this becomes the PEC Byte for both incoming and outgoing data, PEC[7:0] = BIT[7:0] as shown—be sure to note the ordering of the bits within the Remainder. Note all UART transactions supply the command and data stream LSB first.

For incoming UART data streams, the MAX17852 will first clear the CRC engine and then input the incoming data stream into the the CRC Engine, LSB first. After the final bit of data is processed (in this case, the MSB of the incoming data stream is applied to the Engine), the Engine is stopped and the CRC Remainder is known. The incoming PEC Byte as calculated by the host using its copy of the CRC Engine then follows within the UART transaction (also LSB first), and is internally compared against the CRC Remainder as calculated by the MAX17852. If the PEC Byte received matches the CRC Remainder calculated for the incoming data stream, the PEC operation is successful, and the transaction is accepted and executed by the MAX17852. If there is a mismatch, the MAX17852 will reject the transaction and issue the ALRTPEC status bit, notifying the host of the issue, so the transaction can be resent.

For outgoing UART data streams, the MAX17852 will first clear the CRC engine and then provide the outgoing data stream to the the CRC Engine, LSB first. After the final bit of data is processed (in this case, the MSB of the outgoing data stream is applied to the Engine), the Engine is stopped and the CRC Remainder is known, this becomes the outgoing PEC Byte. The outgoing PEC Byte, as calculated by the MAX17852 using its copy of the CRC Engine, then follows within the UART transaction (also LSB first). As the host receives the data stream from the MAX17852, it should apply the data to its copy of the CRC Engine (LSB first, in the order it arrives in the UART transaction, until the MSB of the data stream is applied to the engine). At this point, there are two equivalent ways the host can complete the PEC operation to establish the validity of the received data:

- Direct Comparison Method: The host stops the CRC Engine once the data stream MSB is applied and compares the resulting CRC Remainder to the PEC byte supplied by the MAX17852 (again, LSB first). If the two bytes match, the data is accepted as valid, otherwise it should be rejected. This is the method employed by the MAX17852 internally,

as described above.

- Zero-Remainder Method: The host continues CRC Engine computations after the data MSB is applied by appending the received PEC Byte to the end of the data stream, LSB first (i.e. in the order received during the UART transaction). Once the MSB of the PEC Byte arrives at the input of the CRC Engine, if the resulting CRC Remainder = 00h, the data is accepted as valid; otherwise, it should be rejected.

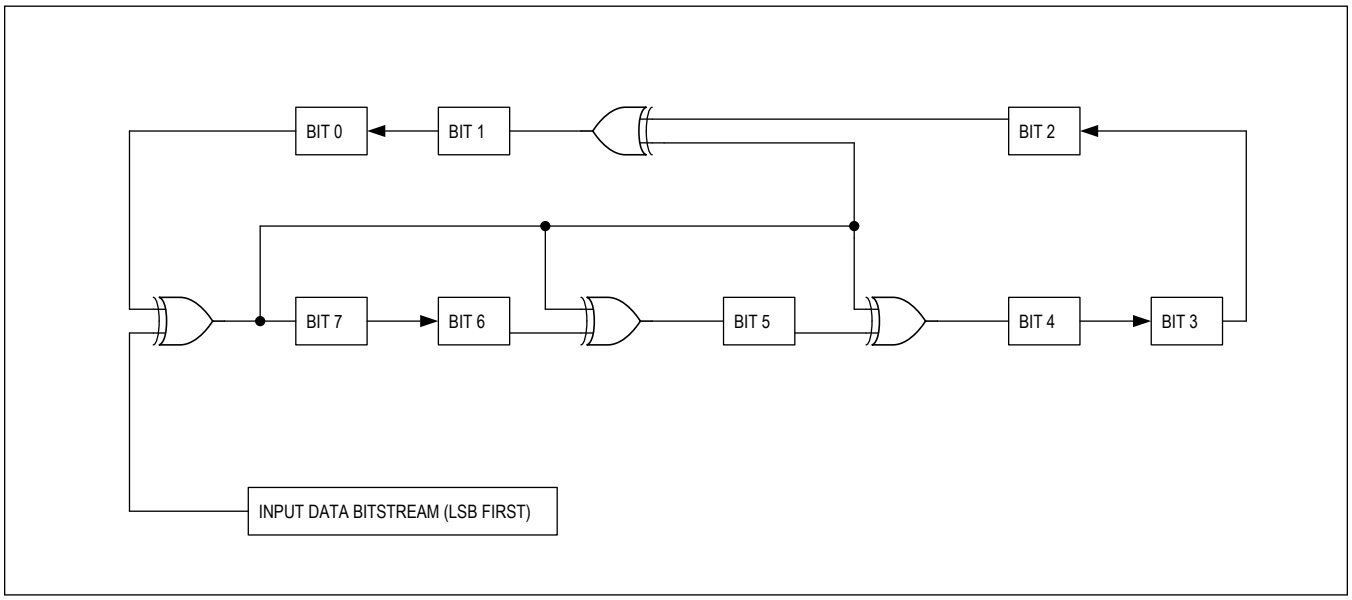


Figure 132. PEC CRC Calculation

PEC Calculation Psuedocode

The host uses the algorithm to process all bytes received in the command packet prior to the PEC byte itself. Neither the PEC nor the alive-counter bytes are part of the calculation. The bits are processed in the order they are received, LSB first. A byte-wise pseudo-code algorithm is shown below, but lookup table solutions are also possible to reduce host calculation time.

For commonly issued command packets, the host can pre-calculate (hard-code) the PEC byte. For commonly used partial packets, the CRC value of a partial calculation may be used as the initial value for a subsequent run-time calculation.

```
Function PEC_Calculation(ByteList(), NumberOfBytes, CRCByte)
{
// CRCByte is initialized to 0 for each ByteList in this implementation, where
// ByteList contains all bytes of a single command. It is passed into the
// function in case a partial ByteList calculation is needed. // Data is transmitted and calculate
// Polynomial = x^8+x^6+x^3+x^2+1 = 1010_0110_1 = 0xA6

POLY = 8'hB2 // 10110010b - Polynomial binary representation is from left to right for LSB first (

//Loop once for each byte in the ByteList
For ByteCounter = 0 to (NumberOfBytes - 1)
(
//Bitwise XOR the current CRC value with the ByteList byte
```

```
CRCByte = CRCByte XOR ByteList(ByteCounter)

//Process each of the 8 CRCByte remainder bits
For BitCounter = 1 To 8
(
// The LSb should be shifted toward the highest order polynomial
// coefficient. This is a right shift for data stored LSb to the right
// and POLY having high order coefficients stored to the right. // Determine if LSb = 1 prior to r

If CRCByte[1] = 1 Then
// When LSb = 1, right shift and XOR CRCByte value with 8 LSbs
// of the polynomial coefficient constant. "/ 2" must be a true right
// shift in the target CPU to avoid rounding problems. CRCByte = ((CRCByte / 2) XOR POLY)

Else
//When LSb = 0, right shift by 1 bit. "/ 2" must be a true right
// shift in the target CPU to avoid rounding problems. CRCByte = (CRCByte / 2)

End If

//Truncate the CRC value to 8 bits if necessary
CRCByte = CRCByte AND 8'hFF
//Proceed to the next bit
Next BitCounter
)
//Operate on the next data byte in the ByteList
Next ByteCounter
)
// All calculations done; CRCByte value is the CRC byte for ByteList() and
// the initial CRCByte value
Return CRCByte
}
```

ROMCRC Calculation

For safety purposes, the factory-trimmed ROM (OTP) content can be read back by the user and checked for errors using an 8-bit CRC (cyclic-redundancy check). ROMCRC is an 8-bit CRC Remainder computed using the ID/OTP content and stored in OTP12[15:8] at the factory. Both the ID and OTP output data content (excluding OTP12[15:8], which ROMCRC[7:0]) and is protected by the ROMCRC operation. To support ROMCRC computation and checking, the host must implement a CRC-8 encoding and decoding algorithm based on the following polynomial (0xA6):

$$P(x) = x^8 + x^6 + x^3 + x^2 + 1$$

This polynomial is capable of protecting the 200 bit ID/OTP content with a Hamming Distance of 3, meaning any combination of 3 bits of error or less is guaranteed to be identified. If more than 3 bits of error are encountered, the ROMCRC operation will very likely identify the problem, although this cannot be mathematically guaranteed.

A hardware implementation of the CRC calculation is shown in Figure 133. The CRC Engine shown would be implemented within the host. The same engine is used in the production trim software to compute and store the ROMCRC byte at the factory, using the computation method outlined below. Be sure to note the ordering of the bits within the Remainder, as shown in the figure (i.e. BIT[7:0] = ROMCRC [7:0]). Note that this is also the same CRC Engine used for

PEC Byte CRC operations in UART mode.

To complete the ROMCRC operation, the host would first clear the CRC Engine and then apply the entire 200-bit content of the ID/OTP data received from the MAX17852 concatenated in the in the following order: ID1[0:15], ID2[0:15], OTP2[0:15], OTP3[0:15], OTP4[0:15], OTP5[0:15], OTP6[0:15], OTP7[0:15], OTP8[0:15], OTP9[0:15], OTP10[0:15], OTP11[0:15], OTP12[0:7]. Note that this is essentially the entire ID/OTP content, provided LSB first—ID1[0] is the first bit applied to the CRC Engine and OTP12[7] is the last, and all 200 bits must be applied. At this point, there are two equivalent ways the host can complete the ROMCRC operation to establish the validity of the received ID/OTP data:

- Direct Comparison Method: The host stops the CRC Engine once the ID/OTP MSB is applied and compares the resulting CRC Remainder to the ROMCRC Byte supplied by the MAX17852 as ROMCRC[7:0] (OTP12[15:8]). If the two bytes match, the data is accepted as valid; otherwise, it should be rejected and retried in case of a communication fault. If the failure persists, this may indicate a problem within the MAX17852 ROM.
- Zero Remainder Method: The host continues CRC Engine computations after the data stream is applied by appending the received ROMCRC Byte to the end of the data stream, LSB first (i.e., continuing the concatenation pattern shown above with OTP12[8:15], with OTP12[15] now being the last bit applied). Once the MSB of the ROMCRC Byte arrives at the input of the CRC Engine, if the resulting CRC Remainder = 00h, the data is accepted as valid; otherwise, it should be rejected and retried in case of a communication fault. If the failure persists, this may indicate a problem within the MAX17852 ROM.

Note: When using direct UART communication and a Block ReadBack of the ID/OTP content, the ROMCRC operation can be computed on the arriving data stream in the order received directly from the MAX17852 (since the UART interface transmits data LSB-first). If using this method, only the 200-bit OTP content should be applied to the CRC Engine (with or without the trailing ROMCRC, depending on the validation method selected above). If using the MAX17852 in UART mode in conjunction with a MAX17841, or in SPI mode, the host should first gather the entire contents of the ID/OTP, and then concatenate it and apply it to the CRC Engine as described above (with or without the trailing ROMCRC, depending on the validation method selected above).

In all cases, the user-interface transactions issued to fetch the ID/OTP data will also be protected by PEC operations (UART) or CRC operations (SPI). If either the PEC or CRC checks fail for the transaction itself, an interface issue has been identified. The user should retry the failed transactions to ensure the ID/OTP data and ROMCRC have been accurately received prior to accepting the results of the ROMCRC operation.

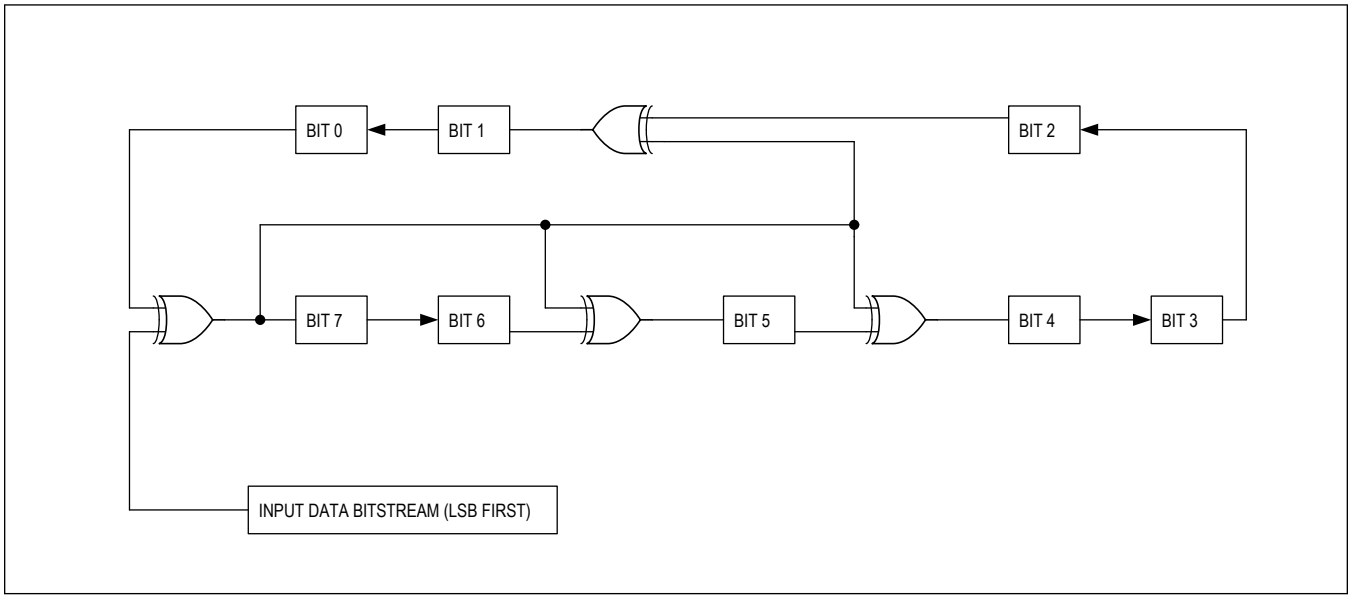


Figure 133. ROMCRC Calculation

Typical Application Circuits

PCB Layout Recommendations

Careful PCB layout is critical to achieving the best accuracy performance and robust performance against environmental conditions.

Layout Procedure

1. Place the charge-pump capacitor close to the CPP and CPN pins and on the same layer as the MAX17852. Care should be taken to avoid using vias to prevent unwanted coupling into adjacent signals and planes.
2. Place the decoupling capacitors on the V_{DCIN}, V_{AA}, V_{DDL1} close to the respective pins and on the same layer as the MAX17852. V_{DDL2} and V_{DDL3} should be placed close to the pins and on the same layer, if possible. All capacitors should not share a ground return and each should via directly to the AGND internal layer.
3. AGND, GNDL1, GNDL2, GNDL3, AUXGND should via directly to a solid AGND plane placed under the MAX17852. Traces and vias should not be shared within before they enter the AGND plane.
4. The DCIN input resistor must be sized depending on both device current consumption (I_{DCIN}) and board current consumption (I_{VAA_LOAD}) to prevent false ALRTHVHDRM alerts. Adjustment of the DCIN resistor due to external loading should following the following equation: $R_{DCIN_LOAD} = R_{DCIN_NOM} \times (1 - I_{DCIN} / I_{VAA_LOAD})$.
   - Note: Flex Pack operation the DCIN filter resistor is omitted
5. The SHDNL capacitor and associated trace routing should be kept away and shielded from potential noise sources and digital signals such as those present with the communication or alert interfaces, as these may affect the voltage seen by the SHDNL pin.
6. C_n traces are recommend to be routed on the same layer as the MAX17852 to avoid potential sources for noise injection into the primary measurement path. These traces carry a negligible current and can be kept at a minimum trace widths.
7. SW_n traces should be optimized for width in the permissible layout (20mil recommended) to eliminate excessive voltage drop due to the balancing operation.
8. UART RX and TX ports should be routed for a 100Ω differential impedance. If the MAX17852 is used in a distributed BMS system, it is recommended to place ESD protection close to the UART communication connector with the ground return via'ed directly to the AGND plane to clamp transient events before they can couple to other nodes, which may effect device performance. For centralized BMS systems, ESD components on the UART may be omitted.
9. SPI operation will be driven by a system microcontroller, which is located on the same ground plane as the MAX17852. Depending on trace length, optional source termination may be required to ensure that overshoot or undershoot does not violate the Absolute Maximum Operating Conditions. This source termination should be placed close to the TX pins of the device.

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX17852ACB/V+	-40°C to +125°C	64 LQFP

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/20	Initial release	—

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