Click here to ask about the production status of specific part numbers.

MAX17644

4.5V to 36V, 2.7A, High-Efficiency, Synchronous Step-Down DC-DC Converter

General Description

The Himalaya series of voltage regulator ICs, power modules, and chargers enable cooler, smaller, and simpler power supply solutions. The MAX17644 is a high-efficiency, high-voltage, Himalaya synchronous step-down DC-DC converter with integrated MOSFETs operating over an input-voltage range of 4.5V to 36V. The device can deliver up to 2.7A of current. The MAX17644 is available in three variants: MAX17644A, MAX17644B, and MAX17644C. The MAX17644A and MAX17644B are fixed 3.3V and fixed 5V output parts, respectively. The MAX17644C is an adjustable output voltage (from 0.9V up to 90% of V_{IN}) part. Built-in compensation across the output-voltage range eliminates the need for external compensation components.

The MAX17644 features peak-current mode control architecture. The device can be operated in the forced pulse-width modulation (PWM), or pulse-frequency modulation (PFM), or discontinuous-conduction mode (DCM) to enable high efficiency under full-load and light-load conditions. The MAX17644 offers a low minimum on-time that allows high switching frequencies and a smaller solution size.

The feedback-voltage regulation accuracy over -40°C to +125°C for the MAX17644A/MAX17644B/MAX17644C is ±1.2%.The device is available in a 16-pin (3mm x 3mm) TQFN package. Simulation models are available.

Applications

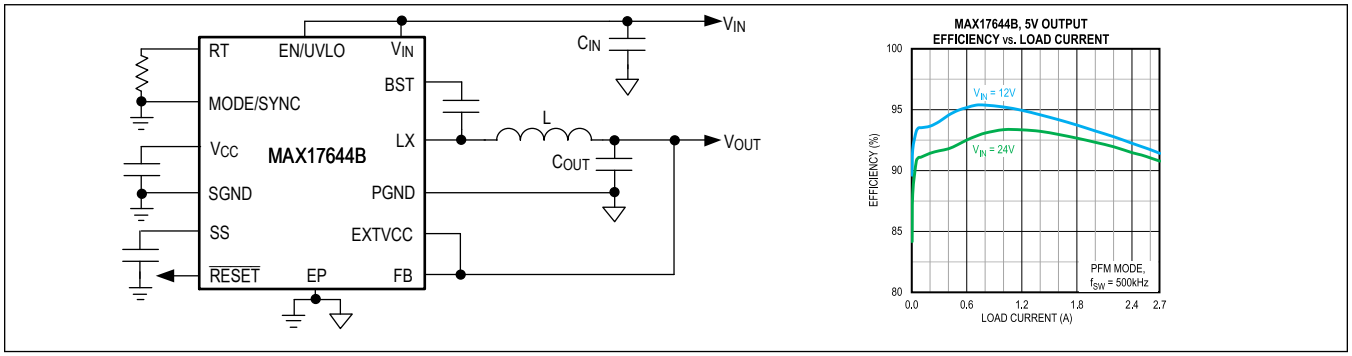
- Industrial Control Power Supplies
- General-Purpose Point-of-Load
- Distributed Supply Regulation
- Base Station Power Supplies
- Wall Transformer Regulation
- High Voltage Single-Board Systems

Benefits and Features

- Reduces External Components and Total Cost
  - No Schottky - Synchronous Operation
  - Internal Compensation Components
  - All-Ceramic Capacitors, Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4.5V to 36V Input
  - Adjustable Output Voltage Range from 0.9V up to 90% of V_{IN}
  - Delivers up to 2.7A Over the Temperature Range
  - 400kHz to 2.2MHz Adjustable Frequency with External Clock Synchronization
  - Available in a 16-Pin, 3mm x 3mm TQFN Package
- Reduces Power Dissipation
  - Peak Efficiency of 95.41%
  - PFM and DCM Modes Enable Enhanced Light-Load Efficiency
  - Auxiliary Bootstrap Supply (EXTVCC) for Improved Efficiency
  - 2.8µA Shutdown Current
- Operates Reliably in Adverse Industrial Environments
  - Hiccup-Mode Overload Protection
  - Adjustable and Monotonic Startup with Prebiased Output Voltage
  - Built-in Output-Voltage Monitoring with $\overline{\text{RESET}}$
  - Programmable EN/UVLO Threshold
  - Overtemperature Protection
  - CISPR32 Class B Compliant
  - Wide -40°C to +125°C Ambient Operating Temperature Range / -40°C to +150°C Junction Temperature Range

***Ordering Information* appears at end of data sheet.**

Simplified Application Circuit



Absolute Maximum Ratings

V_{IN} to PGND ..... -0.3V to +40V
EN/UVLO to SGND ..... -0.3V to V_{IN} + 0.3V
LX to PGND ..... -0.3V to V_{IN} + 0.3V
EXTVCC to SGND ..... -5.5V to +6.5V
BST to PGND ..... -0.3V to +46.5V
BST to LX ..... -0.3V to +6.5V
BST to V_{CC} ..... -0.3V to +40V
RESET, SS, MODE/SYNC, V_{CC}, RT to SGND ..... -0.3V to +6.5V
FB to SGND (MAX17644A & MAX17644B) ..... -5.5V to +6.5V
FB to SGND (MAX17644C) ..... -0.3V to +6.5V
PGND to SGND ..... -0.3V to +0.3V
LX Total RMS Current ..... ±3.5A
Output Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 23.10mW/°C above +70°C.) 1847.60mW
Operating Temperature Range (Note 1) ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 PIN TQFN

Package Code	T1633+5C
Outline Number	21-0136
Land Pattern Number	90-0032
THERMAL RESISTANCE, FOUR-LAYER BOARD (Note 2)	
Junction to Ambient (θ_{JA})	33°C/W
Junction to Case (θ_{JC})	4°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Note 2: Package thermal resistances were obtained using the MAX17644 evaluation kit with no airflow.

Electrical Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = unconnected (f_{SW} = 400 kHz), C_{VCC} = 2.2µF, $V_{MODE/SYNC}$ = V_{EXTVCC} = V_{SGND} = V_{PGND} = 0V, V_{FB} = 3.67V (MAX17644A), V_{FB} = 5.5V (MAX17644B), V_{FB} = 1V (MAX17644C), LX = SS = RESET = unconnected, V_{BST} to V_{LX} = 5V, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})						
Input-Voltage Range	V_{IN}		4.5		36	V
Input-Shutdown Current	I_{IN-SH}	$V_{EN/UVLO}$ = 0V (Shutdown mode)		2.8	4.5	µA

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = unconnected (f_{SW} = 400 kHz), C_{VCC} = 2.2µF, $V_{MODE/SYNC}$ = V_{EXTVCC} = V_{SGND} = V_{PGND} = 0V, V_{FB} = 3.67V (MAX17644A), V_{FB} = 5.5V (MAX17644B), V_{FB} = 1V (MAX17644C), LX = SS = $\overline{RESET}$ = unconnected, V_{BST} to V_{LX} = 5V, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input-Quiescent Current	I_{Q_PFM}	MODE/SYNC = Unconnected, V_{EXTVCC} = 5V		50		µA
		MODE/SYNC = Unconnected, R_{RT} = 50.8kΩ, V_{EXTVCC} = 5V		60		
	I_{Q_DCM}	DCM Mode, V_{LX} = 0.1V		1.2	1.8	mA
	I_{Q_PWM}	Normal Switching Mode, f_{SW} = 400kHz, V_{FB} = 3V (MAX17644A), V_{FB} = 4.4V (MAX17644B), V_{FB} = 0.8V (MAX17644C)		5		
ENABLE/UVLO (EN/UVLO)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.19	1.215	1.26	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.068	1.09	1.131	
EN Input-Leakage Current	I_{EN}	$V_{EN/UVLO}$ = 0V, T_A = +25ºC	-50	0	+50	nA
V_{CC} (LDO)						
V_{CC} Output-Voltage Range	V_{CC}	1mA ≤ I_{VCC} ≤ 15mA	4.75	5	5.25	V
		6V ≤ V_{IN} ≤ 36V, I_{VCC} = 1mA	4.75	5	5.25	
V_{CC} Current Limit	$I_{VCC-MAX}$	V_{CC} = 4.5V, V_{IN} = 7.5V	25	50		mA
V_{CC} Dropout	V_{CC-DO}	V_{IN} = 4.5V, I_{VCC} = 10mA			0.3	V
V_{CC} UVLO	V_{CC_UVR}	V_{CC} rising	4.05	4.2	4.3	V
	V_{CC_UVF}	V_{CC} falling	3.65	3.8	3.9	
EXTVCC						
EXTVCC Switchover Threshold		V_{EXTVCC} rising	4.56	4.7	4.84	V
		V_{EXTVCC} falling	4.3	4.45	4.6	
POWER MOSFETS						
High-Side nMOS On-Resistance	R_{DS-ONH}	I_{LX} = 0.3A, sourcing		125	250	mΩ
Low-Side nMOS On-Resistance	R_{DS-ONL}	I_{LX} = 0.3A, sinking		80	160	mΩ
LX Leakage Current	I_{LX_LKG}	V_{LX} = (V_{PGND} +1V) to (V_{IN} - 1V), T_A = +25°C	-2		+3	µA
SOFT-START (SS)						
Charging Current	I_{SS}	V_{SS} = 0.5V	4.7	5	5.3	µA

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = unconnected (f_{SW} = 400 kHz), C_{VCC} = 2.2µF, $V_{MODE/\overline{SYNC}}$ = V_{EXTVCC} = V_{SGND} = V_{PGND} = 0V, V_{FB} = 3.67V (MAX17644A), V_{FB} = 5.5V (MAX17644B), V_{FB} = 1V (MAX17644C), LX = SS = $\overline{RESET}$ = unconnected, V_{BST} to V_{LX} = 5V, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB-REG}	MODE/SYNC = SGND or MODE/SYNC = V_{CC}, for MAX17644A	3.26	3.3	3.34	V
		MODE/SYNC = SGND or MODE/SYNC = V_{CC}, for MAX17644B	4.94	5	5.06	
		MODE/SYNC = SGND or MODE/SYNC = V_{CC} for MAX17644C	0.889	0.9	0.911	
		MODE/SYNC = Unconnected for MAX17644A	3.26	3.36	3.43	
		MODE/SYNC = Unconnected for MAX17644B	4.94	5.09	5.20	
		MODE/SYNC = Unconnected for MAX17644C	0.89	0.915	0.936	
FB Input-Bias Current	I_{FB}	For MAX17644A		21		µA
		For MAX17644B		17		
		0 ≤ V_{FB} ≤ 1V, T_A = 25ºC For MAX17644C	-50		+50	nA
MODE/SYNC						
MODE Threshold	V_{M-DCM}	MODE/SYNC = V_{CC} (DCM mode)	V_{CC} - 0.65			V
	V_{M-PFM}	MODE/SYNC = Unconnected (PFM mode)		V_{CC}/2		
	V_{M-PWM}	MODE/SYNC = SGND (PWM mode)			0.75	
SYNC Frequency-Capture Range	f_{SYNC}	f_{SW} set by R_{RT}	1.1 x f_{SW}		1.4 x f_{SW}	kHz
SYNC Pulse Width			50			ns
SYNC Threshold	V_{IH}		2.1			V
	V_{IL}				0.8	
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$		3.45	4.0	4.6	A
Runaway Peak Current-Limit Threshold	$I_{RUNAWAY-LIMIT}$		4.0	4.7	5.3	A
PFM Peak Current-Limit Threshold	I_{PFM}	MODE/SYNC = Unconnected		1		A
Valley Current-Limit Threshold	$I_{VALLEY-LIMIT}$	MODE/SYNC = Unconnected or MODE/SYNC = V_{CC}	-0.15	0	+0.15	A
		MODE/SYNC = SGND, V_{FB} > 0.65		-1.8		

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = unconnected (f_{SW} = 400 kHz), C_{VCC} = 2.2µF, $V_{MODE/\overline{SYNC}}$ = V_{EXTVCC} = V_{SGND} = V_{PGND} = 0V, V_{FB} = 3.67V (MAX17644A), V_{FB} = 5.5V (MAX17644B), V_{FB} = 1V (MAX17644C), LX = SS = $\overline{RESET}$ = unconnected, V_{BST} to V_{LX} = 5V, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RT						
Switching Frequency	f_{SW}	R_{RT} = 50.8kΩ	380	400	420	kHz
		R_{RT} = 40.2kΩ	475	500	525	
		R_{RT} = 8.06kΩ	1950	2200	2450	
		R_{RT} = Unconnected	370	400	430	
V_{FB} Undervoltage Trip Level to Cause Hiccup	$V_{FB-HICF}$	For MAX17644A	2.05	2.13	2.2	V
		For MAX17644B	3.11	3.22	3.33	
		For MAX17644C	0.56	0.58	0.6	
HICCUP Timeout		(Note 4)		32768		Cycles
Minimum On-Time	t_{ON-MIN}			52	80	ns
Minimum Off-Time	$t_{OFF-MIN}$		140		160	ns
LX Dead Time	LX_{DT}			5		ns
$\overline{RESET}$						
$\overline{RESET}$ Output-Level Low	V_{RESETL}	$I_{\overline{RESET}}$ = 10mA			400	mV
$\overline{RESET}$ Output-Leakage Current	$I_{RESETLKG}$	T_A = T_J = 25ºC, $V_{\overline{RESET}}$ = 5.5V	-100		100	nA
FB Threshold for $\overline{RESET}$ Deassertion	V_{FB-OKR}	V_{FB} rising	93.8	95	97.8	%
FB Threshold for $\overline{RESET}$ Assertion	V_{FB-OKF}	V_{FB} falling	90.5	92	94.6	%
$\overline{RESET}$ Delay after FB Reaches 95% Regulation				1024		Cycles
THERMAL SHUTDOWN (TEMP)						
Thermal-Shutdown Threshold		Temperature rising		165		°C
Thermal-Shutdown Hysteresis				10		°C

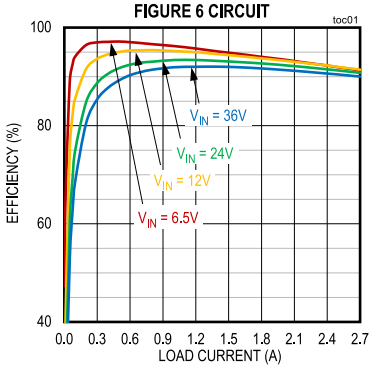
Note 3: Electrical specifications are production tested at T_A = +25ºC. Specifications over the entire operating temperature range are guaranteed by design and characterization.

Note 4: See the *Overcurrent Protection/Hiccup Mode* section for more details

Typical Operating Characteristics

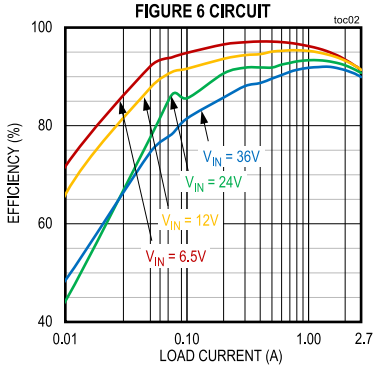
($V_{EN/UVLO}$ = V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = +25°C unless otherwise noted. All voltages are referenced to SGND, unless otherwise noted.)

MAX17644C, 5V OUTPUT EFFICIENCY vs. LOAD CURRENT FIGURE 6 CIRCUIT



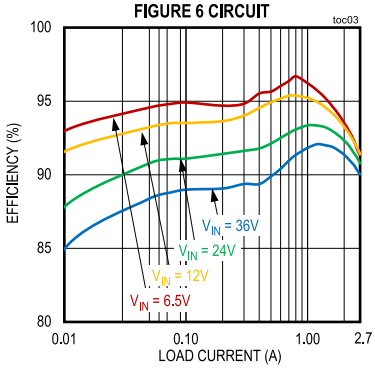
CONDITIONS: PWM MODE, f_{SW} = 500kHz

MAX17644C, 5V OUTPUT EFFICIENCY vs. LOAD CURRENT FIGURE 6 CIRCUIT



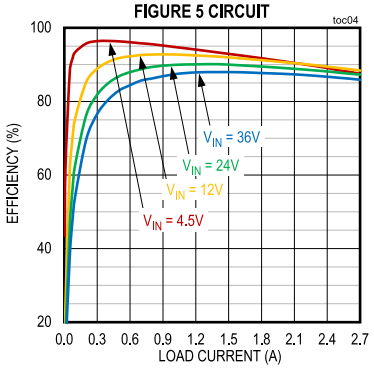
CONDITIONS: DCM MODE, f_{SW} = 500kHz

MAX17644C, 5V OUTPUT EFFICIENCY vs. LOAD CURRENT FIGURE 6 CIRCUIT



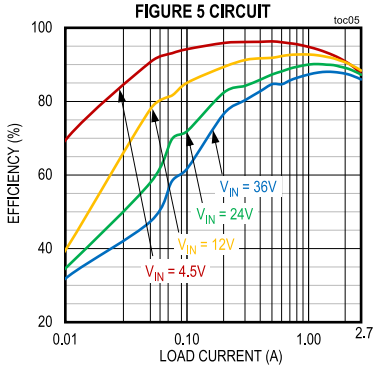
CONDITIONS: PFM MODE, f_{SW} = 500kHz

MAX17644C, 3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT FIGURE 5 CIRCUIT



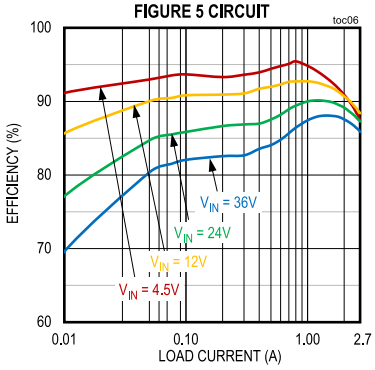
CONDITIONS: PWM MODE, f_{SW} = 500kHz

MAX17644C, 3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT FIGURE 5 CIRCUIT



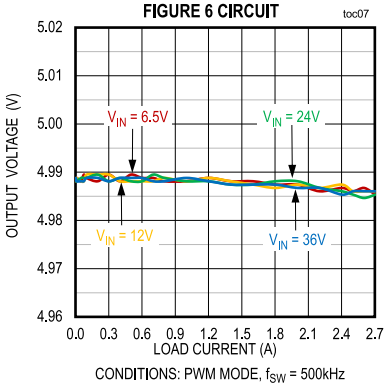
CONDITIONS: DCM MODE, f_{SW} = 500kHz

MAX17644C, 3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT FIGURE 5 CIRCUIT



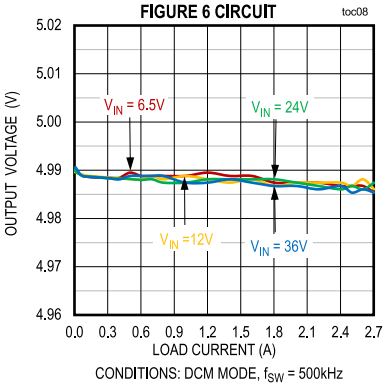
CONDITIONS: PFM MODE, f_{SW} = 500kHz

MAX17644C, 5V OUTPUT LOAD AND LINE REGULATION FIGURE 6 CIRCUIT



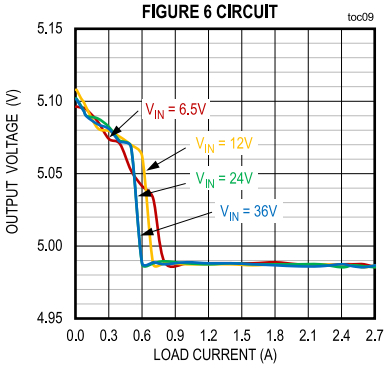
CONDITIONS: PWM MODE, f_{SW} = 500kHz

MAX17644C, 5V OUTPUT LOAD AND LINE REGULATION, FIGURE 6 CIRCUIT



CONDITIONS: DCM MODE, f_{SW} = 500kHz

MAX17644C, 5V OUTPUT LOAD AND LINE REGULATION FIGURE 6 CIRCUIT

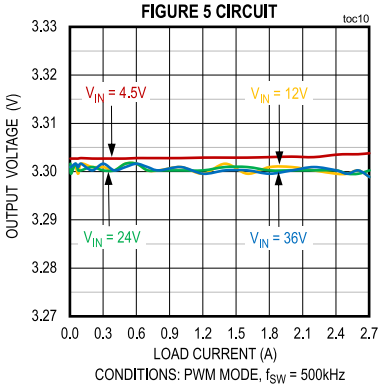


CONDITIONS: PFM MODE, f_{SW} = 500kHz

Typical Operating Characteristics (continued)

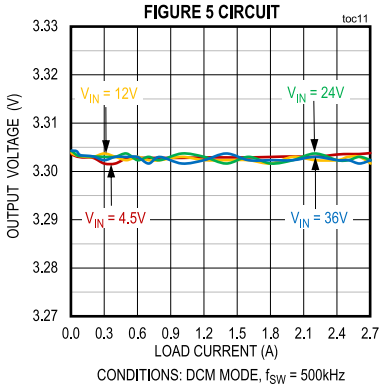
($V_{EN/UVLO}$ = V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = +25°C unless otherwise noted. All voltages are referenced to SGND, unless otherwise noted.)

MAX17644C, 3.3V OUTPUT LOAD AND LINE REGULATION, FIGURE 5 CIRCUIT



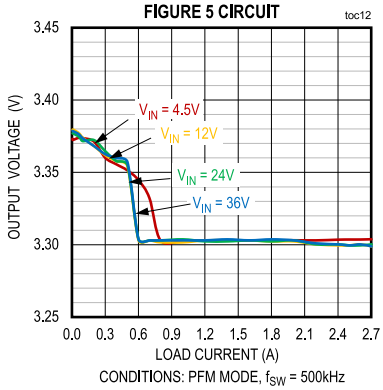
CONDITIONS: PWM MODE, f_{SW} = 500kHz

MAX17644C, 3.3V OUTPUT LOAD AND LINE REGULATION FIGURE 5 CIRCUIT



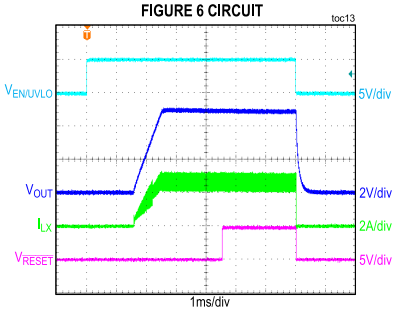
CONDITIONS: DCM MODE, f_{SW} = 500kHz

MAX17644C, 3.3 OUTPUT LOAD AND LINE REGULATION FIGURE 5 CIRCUIT



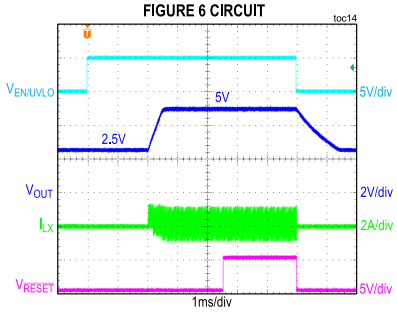
CONDITIONS: PFM MODE, f_{SW} = 500kHz

MAX17644C, 5V OUTPUT SOFT-START/SHUTDOWN THROUGH EN/UVLO FIGURE 6 CIRCUIT



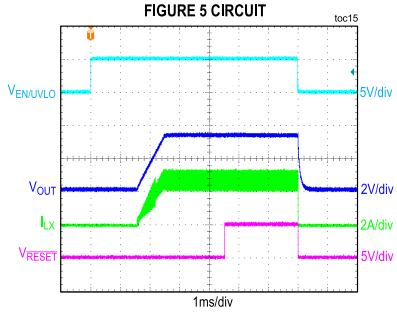
CONDITIONS: PWM MODE, 2.7A LOAD, f_{SW} = 500kHz

MAX17644C, 5V OUTPUT SOFT-START WITH PREBIAS VOLTAGE OF 2.5V FIGURE 6 CIRCUIT



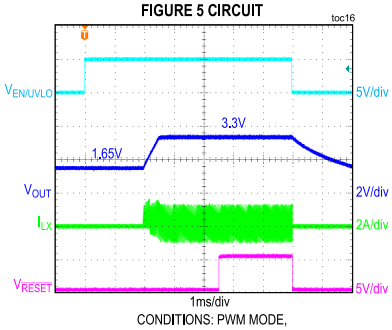
CONDITIONS: PWM MODE, 54mA LOAD, f_{SW} = 500kHz

MAX17644C, 3.3V OUTPUT SOFT-START/SHUTDOWN THROUGH EN/UVLO FIGURE 5 CIRCUIT



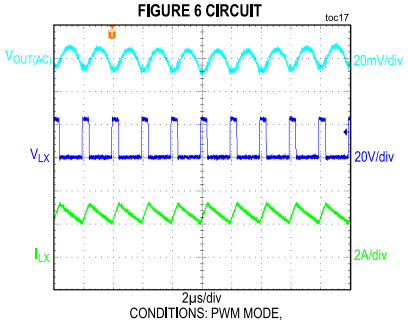
CONDITIONS: PWM MODE, 2.7A LOAD, f_{SW} = 500kHz

MAX17644C, 3V OUTPUT SOFT-START WITH PREBIAS VOLTAGE OF 1.65V FIGURE 5 CIRCUIT



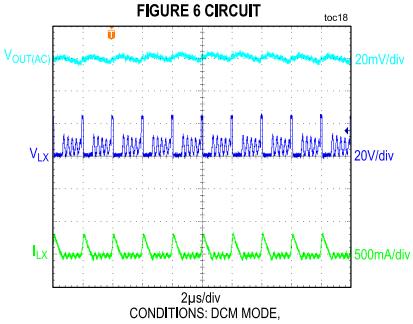
CONDITIONS: PWM MODE, 54mA LOAD, f_{SW} = 500kHz

MAX17644C, 5V OUTPUT STEADY STATE PERFORMANCE FIGURE 6 CIRCUIT



CONDITIONS: PWM MODE, 2.7A LOAD, f_{SW} = 500kHz

MAX17644C, 5V OUTPUT STEADY STATE PERFORMANCE FIGURE 6 CIRCUIT

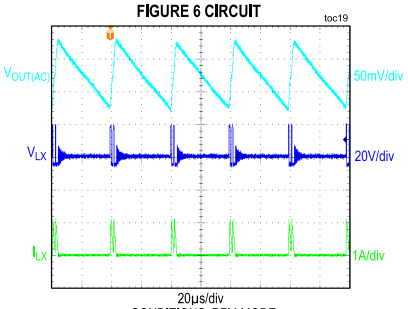


CONDITIONS: DCM MODE, 54mA LOAD, f_{SW} = 500kHz

Typical Operating Characteristics (continued)

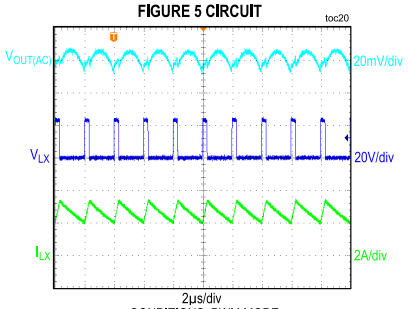
($V_{EN/UVLO}$ = V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = +25°C unless otherwise noted. All voltages are referenced to SGND, unless otherwise noted.)

MAX17644C, 5V OUTPUT STEADY STATE PERFORMANCE FIGURE 6 CIRCUIT



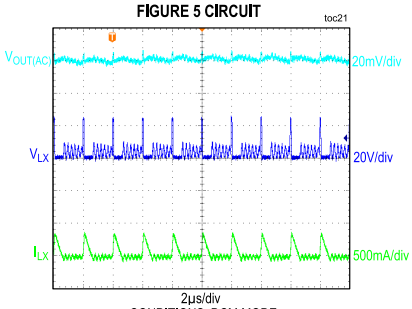
CONDITIONS: PFM MODE, 54mA LOAD, f_{SW} = 500kHz

MAX17644C, 3.3V OUTPUT STEADY STATE PERFORMANCE FIGURE 5 CIRCUIT



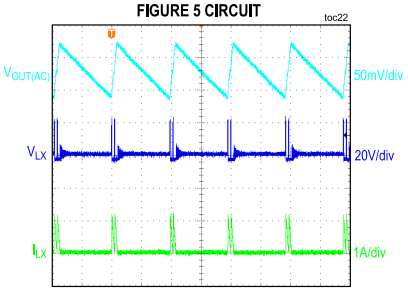
CONDITIONS: PWM MODE, 2.7A LOAD, f_{SW} = 500kHz

MAX17644C, 3.3V OUTPUT STEADY STATE PERFORMANCE FIGURE 5 CIRCUIT



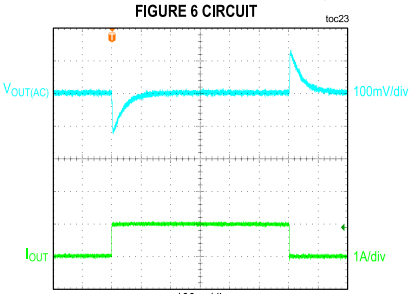
CONDITIONS: DCM MODE, 54mA LOAD, f_{SW} = 500kHz

MAX17644C, 3.3V OUTPUT STEADY STATE PERFORMANCE FIGURE 5 CIRCUIT



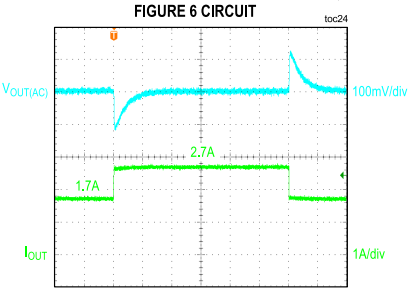
CONDITIONS: PFM MODE, 54mA LOAD, f_{SW} = 500kHz

MAX17644C, 5V OUTPUT LOAD TRANSIENT BETWEEN 0 AND 1A, FIGURE 6 CIRCUIT



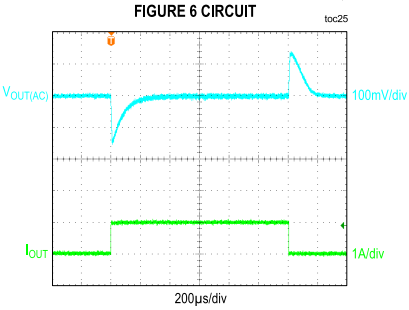
CONDITIONS: PWM MODE, f_{SW} = 500kHz

MAX17644C, 5V OUTPUT LOAD TRANSIENT BETWEEN 1.7A AND 2.7A, FIGURE 6 CIRCUIT



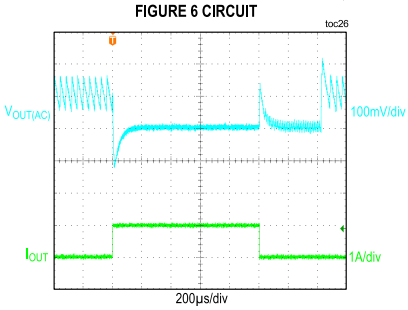
CONDITIONS: PWM MODE, f_{SW} = 500kHz

MAX17644C, 5V OUTPUT LOAD TRANSIENT BETWEEN 0.054A AND 1A, FIGURE 6 CIRCUIT



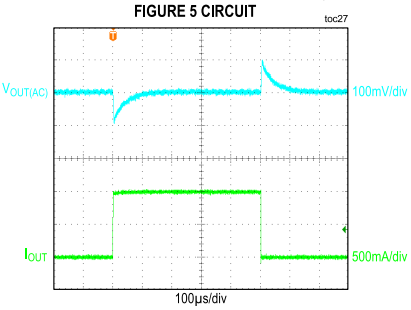
CONDITIONS: DCM MODE, f_{SW} = 500kHz

MAX17644C, 5V OUTPUT LOAD TRANSIENT BETWEEN 0.054A AND 1A, FIGURE 6 CIRCUIT



CONDITIONS: PFM MODE, f_{SW} = 500kHz

MAX17644C, 3.3V OUTPUT LOAD TRANSIENT BETWEEN 0 AND 1A, FIGURE 5 CIRCUIT

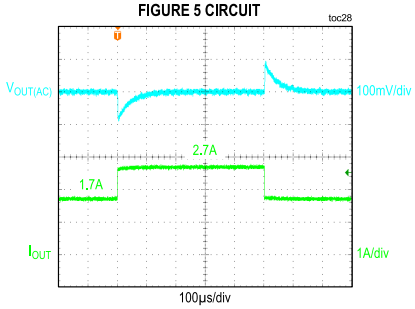


CONDITIONS: PWM MODE, f_{SW} = 500kHz

Typical Operating Characteristics (continued)

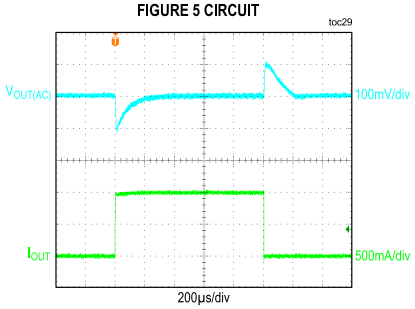
($V_{EN/UVLO}$ = V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = +25°C unless otherwise noted. All voltages are referenced to SGND, unless otherwise noted.)

MAX17644C, 3.3V OUTPUT
LOAD TRANSIENT BETWEEN 1.7A AND 2.7A,
FIGURE 5 CIRCUIT



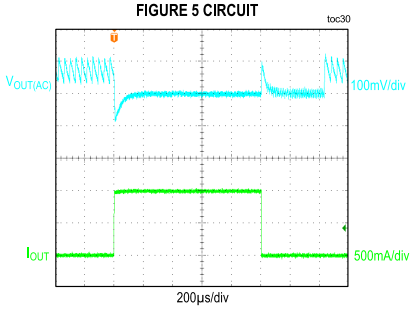
CONDITIONS: PWM MODE, f_{SW} = 500kHz

MAX17644C, 3.3V OUPUT
LOAD TRANSIENT BETWEEN 0.054A AND 1A,
FIGURE 5 CIRCUIT



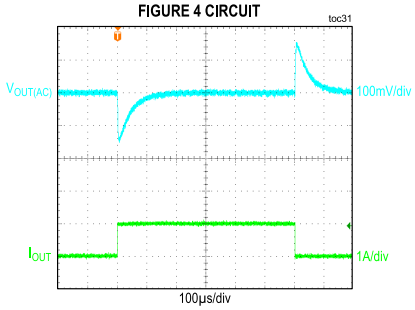
CONDITIONS: DCM MODE, f_{SW} = 500kHz

MAX17644C, 3.3V OUTPUT
LOAD TRANSIENT BETWEEN 0.054A AND 1A,
FIGURE 5 CIRCUIT



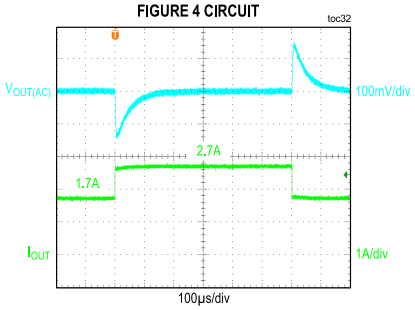
CONDITIONS: PFM MODE, f_{SW} = 500kHz

MAX17644B 5V OUTPUT
LOAD TRANSIENT BETWEEN 0 AND 1A,
FIGURE 4 CIRCUIT



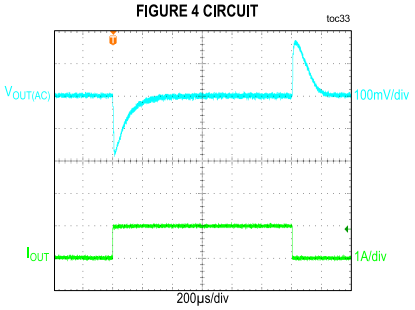
CONDITIONS: PWM MODE, f_{SW} = 500kHz

MAX17644B, 5V OUTPUT
LOAD TRANSIENT BETWEEN 1.7A AND 2.7A,
FIGURE 4 CIRCUIT



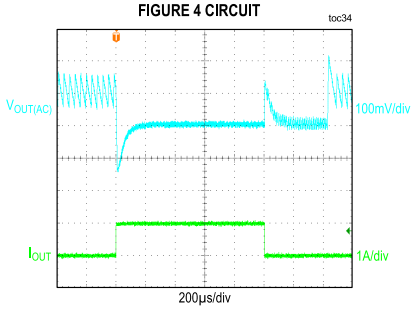
CONDITIONS: PWM MODE, f_{SW} = 500kHz

MAX17644B, 5V OUTPUT
LOAD TRANSIENT BETWEEN 0.054A AND 1A,
FIGURE 4 CIRCUIT



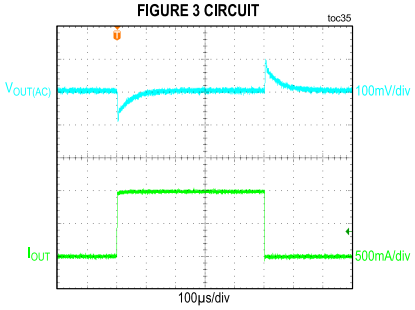
CONDITIONS: DCM MODE, f_{SW} = 500kHz

MAX17644B, 5V OUTPUT
LOAD TRANSIENT BETWEEN 0.054A AND 1A,
FIGURE 4 CIRCUIT



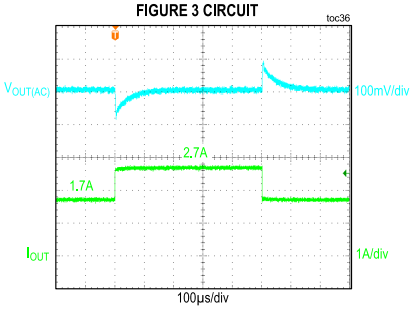
CONDITIONS: PFM MODE, f_{SW} = 500kHz

MAX17644A, 3.3V OUTPUT
LOAD TRANSIENT BETWEEN 0 AND 1A,
FIGURE 3 CIRCUIT



CONDITIONS: PWM MODE, f_{SW} = 500kHz

MAX17644A, 3.3V OUTPUT
LOAD TRANSIENT BETWEEN 1.7A AND 2.7A,
FIGURE 3 CIRCUIT

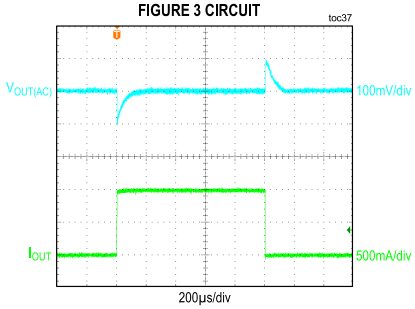


CONDITIONS: PWM MODE, f_{SW} = 500kHz

Typical Operating Characteristics (continued)

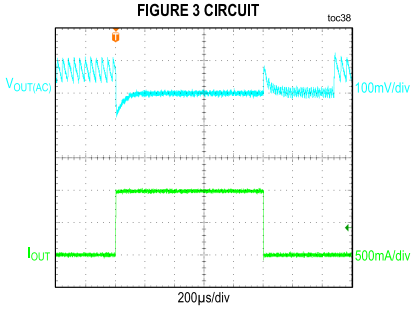
($V_{EN/UVLO}$ = V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = +25°C unless otherwise noted. All voltages are referenced to SGND, unless otherwise noted.)

MAX17644A, 3.3V OUTPUT
LOAD TRANSIENT BETWEEN 0.054A AND 1A,
FIGURE 3 CIRCUIT



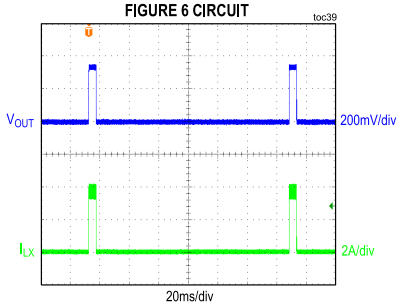
CONDITIONS: DCM MODE, f_{SW} = 500kHz

MAX17644A, 3.3V OUTPUT
LOAD TRANSIENT BETWEEN 0.054A AND 1A,
FIGURE 3 CIRCUIT



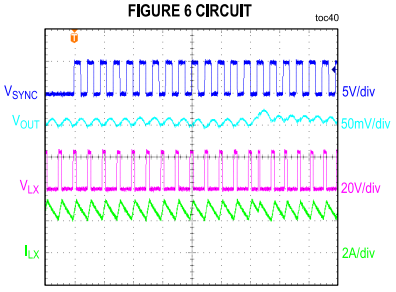
CONDITIONS: PFM MODE, f_{SW} = 500kHz

MAX17644C, 5V OUTPUT
OVERLOAD PROTECTION
FIGURE 6 CIRCUIT



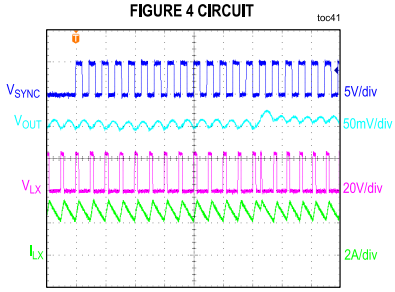
CONDITIONS: PWM MODE, f_{SW} = 500kHz

MAX17644C, 5V OUTPUT
EXTERNAL CLOCK SYNCHRONIZATION
FIGURE 6 CIRCUIT



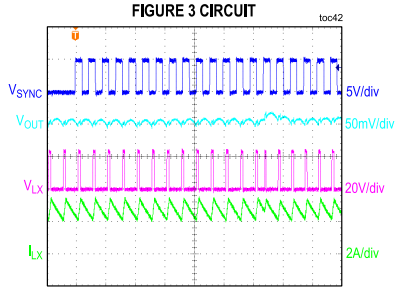
CONDITIONS: PWM MODE, 2.7A LOAD CURRENT
f_{SW} = 500kHz, EXTERNAL CLOCK FREQUENCY = 550kHz

MAX17644B, 5V OUTPUT
EXTERNAL CLOCK SYNCHRONIZATION
FIGURE 4 CIRCUIT



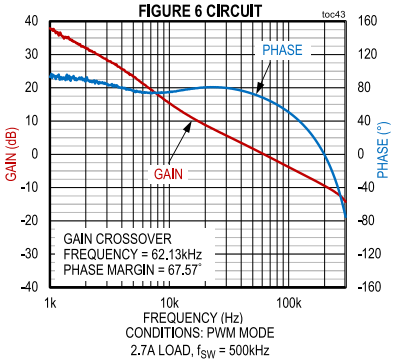
CONDITIONS: PWM MODE, 2.7A LOAD CURRENT
f_{SW} = 500kHz, EXTERNAL CLOCK FREQUENCY = 550kHz

MAX17644A, 3.3V OUTPUT
EXTERNAL CLOCK SYNCHRONIZATION
FIGURE 3 CIRCUIT



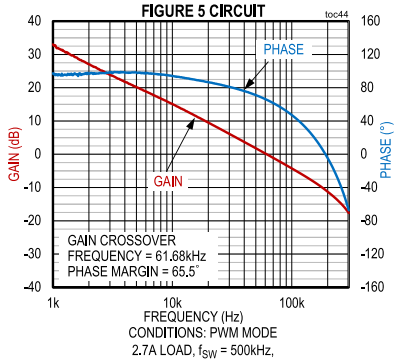
CONDITIONS: PWM MODE, 2.7A LOAD CURRENT
f_{SW} = 500kHz, EXTERNAL CLOCK FREQUENCY = 550kHz

MAX17644C, 5V OUTPUT
BODE PLOT
FIGURE 6 CIRCUIT



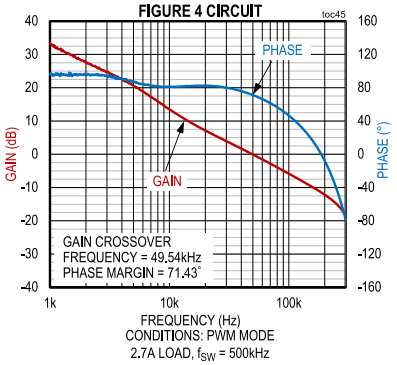
CONDITIONS: PWM MODE
2.7A LOAD, f_{SW} = 500kHz

MAX17644C, 3.3V OUTPUT
BODE PLOT
FIGURE 5 CIRCUIT



CONDITIONS: PWM MODE
2.7A LOAD, f_{SW} = 500kHz,

MAX17644B, 5V OUTPUT
BODE PLOT
FIGURE 4 CIRCUIT

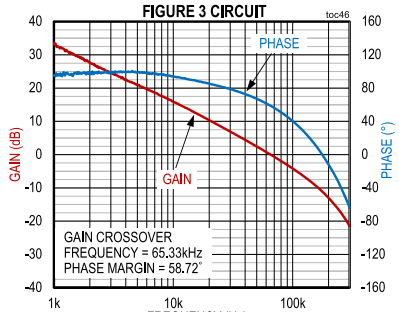


CONDITIONS: PWM MODE
2.7A LOAD, f_{SW} = 500kHz

Typical Operating Characteristics (continued)

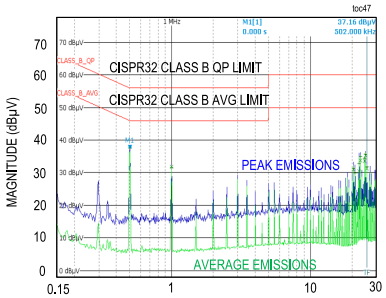
($V_{EN/UVLO}$ = V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = +25°C unless otherwise noted. All voltages are referenced to SGND, unless otherwise noted.)

MAX17644A, 3.3V OUTPUT
BODE PLOT
FIGURE 3 CIRCUIT



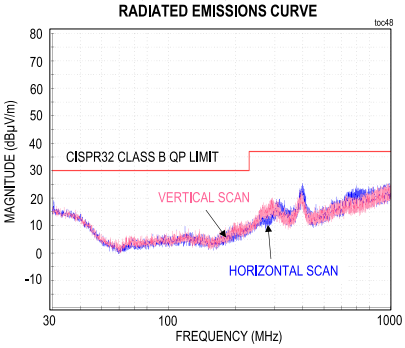
CONDITIONS: PWM MODE, 2.7A LOAD, f_{SW} = 500kHz

MAX17644C, 5V OUTPUT, 2.7A LOAD CURRENT
CONDUCTED EMISSIONS CURVE



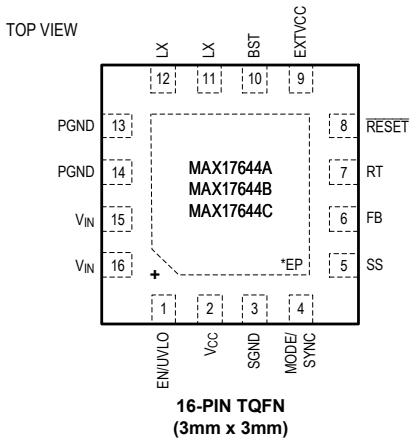
MEASURED ON MAX17644C5EVKIT# with L302 = 15µH, C315 = C316 = C317 = 4.7µF/50V/1206/X7R

MAX17644C, 5V OUTPUT, 2.7A LOAD CURRENT
RADIATED EMISSIONS CURVE



MEASURED ON MAX17644C5EVKIT#

Pin Configuration

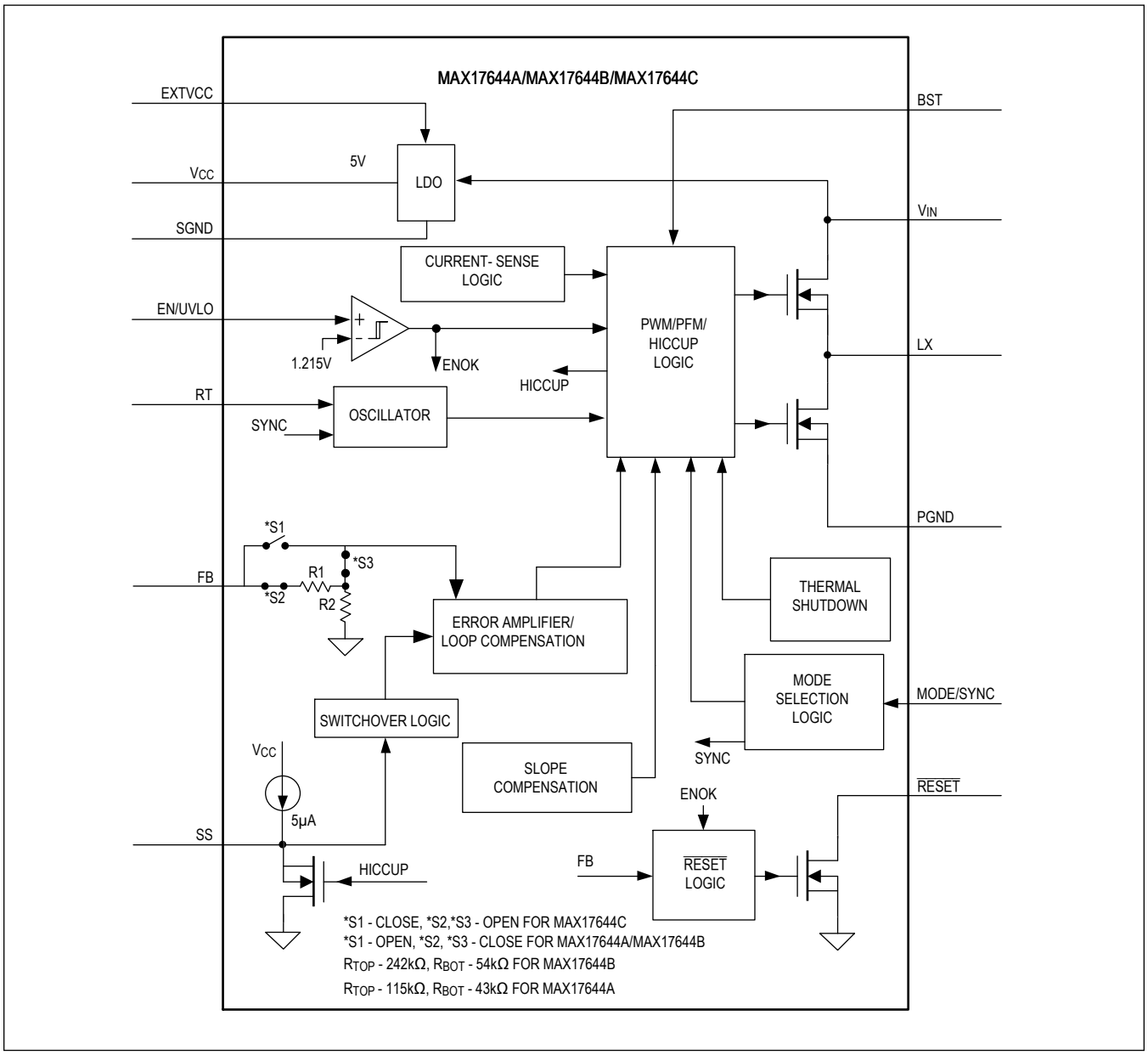


16-PIN TQFN
(3mm x 3mm)

Pin Description

PIN	NAME	FUNCTION
1	EN/UVLO	Enable/Undervoltage Lockout Pin. Drive EN/UVLO high to enable the output. Connect to the center of the resistor-divider between V_{IN} and SGND to set the input voltage at which the part turns on. Connect to V_{IN} pins for always on operation. Pull low (lower than V_{ENF}) to disable the device.
2	V_{CC}	5V LDO Output. Bypass V_{CC} with a 2.2µF ceramic capacitance to SGND. LDO doesn't support the external loading on V_{CC}.
3	SGND	Signal Ground.
4	MODE/SYNC	MODE/SYNC Pin Configures the Device to Operate either in PWM, PFM, or DCM Modes of Operation. Leave MODE/SYNC open for PFM operation (pulse skipping at light loads). Connect MODE/SYNC to SGND for constant-frequency PWM operation at all loads. Connect MODE/SYNC to V_{CC} for DCM operation at light loads. The device can be synchronized to an external clock using this pin. See the *Mode Selection and External Clock Synchronization (MODE/SYNC)* section for more details.
5	SS	Soft-Start Input. Connect a capacitor from SS to SGND to set the soft-start time.
6	FB	Feedback Input. Connect the output voltage node (V_{OUT}) to FB for MAX17644A and MAX17644B. Connect FB to the center node of an external resistor-divider from the output to SGND to set the output voltage for MAX17644C. See the *Adjusting Output Voltage* section for more details.
7	RT	Programmable Switching Frequency Input. Connect a resistor from RT to SGND to set the regulator's switching frequency between 400kHz and 2.2MHz. Leave RT Unconnected for the default 400kHz frequency. See the *Setting the Switching Frequency (RT)* section for more details.
8	$\overline{\text{RESET}}$	Open-Drain $\overline{\text{RESET}}$ Output. The $\overline{\text{RESET}}$ output is driven low if FB drops below 92% of its set value. $\overline{\text{RESET}}$ goes high 1024 cycles after FB rises above 95% of its set value.
9	EXTVCC	External Power Supply Input Reduces the Internal-LDO Loss. Connect it to buck output when it is programmed to 5V only. When EXTVCC is not used, connect it to SGND.
10	BST	Boost Flying Capacitor. Connect a 0.1µF ceramic capacitor between BST and LX.
11, 12	LX	Switching Node Pins. Connect LX pins to the switching side of the inductor.
13, 14	PGND	Power Ground Pins of the Converter. Refer to the MAX17644 EV kit datasheet for recommended PCB layout and routing.
15, 16	V_{IN}	Power-Supply Input Pins. 4.5V to 36V input-supply range. Decouple to PGND with a 2.2µF capacitor; place the capacitor close to the V_{IN} and PGND pins.
*	EP	Exposed Pad. Connect EP to the SGND. Refer to the MAX17644 EV kit datasheet for the recommended method of PCB layout, routing, and thermal vias.

Functional Block Diagram



Detailed Description

The MAX17644 is a high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operating over an input-voltage range of 4.5V to 36V. The device can deliver up to 2.7A of current. MAX17644A and MAX17644B are fixed 3.3V and fixed 5V output parts, respectively. MAX17644C is the adjustable output voltage (from 0.9V up to 90% of V_{IN}) part. Built-in compensation across the output-voltage range eliminates the need for external compensation components. The feedback-voltage regulation accuracy over -40°C to +125°C is ±1.2% for MAX17644.

The device features a peak-current mode control architecture. An internal transconductance error amplifier produces an integrated error voltage at an internal node, which sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator. At each rising edge of the clock, the high-side MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected. During the high-side MOSFET's on-time, the inductor current ramps up. During the rest of the switching cycle, the high-side MOSFET turns off and the low-side MOSFET turns on. The inductor releases the stored energy as its current ramps down and provides current to the output.

The device features a MODE/SYNC pin that can be used to operate the device in PWM, PFM, or DCM control modes. The device also features adjustable-input undervoltage lockout, adjustable soft-start, open-drain $\overline{\text{RESET}}$, and external clock synchronization features. The MAX17644 offers a low minimum on-time that enables to design converter at high switching frequencies and a small solution size.

Mode Selection and External Clock Synchronization (MODE/SYNC)

The MAX17644 supports PWM, PFM, and DCM mode of operation. The device enters the required mode of operation based on the setting of the MODE/SYNC pin as detected within 1.5ms after V_{CC} and EN/UVLO voltages exceed their respective UVLO rising thresholds (V_{CC_UVR}, V_{ENR}). If the MODE/SYNC pin is unconnected, the device operates in PFM mode at light loads. If the state of the MODE/SYNC pin is low (less than V_{M-PWM}), the device operates in constant-frequency PWM mode at all loads. If the state of the MODE/SYNC pin is high (greater than V_{M-DCM}), the device operates in constant-frequency DCM mode at light loads.

During external clock synchronization, the device operates in PWM mode irrespective of the mode of operation detected. When 16 external clock rising edges are detected on the MODE/SYNC pin, the internal oscillator frequency set by the RT pin (f_{SW}) changes to the external clock frequency, and the device transitions to PWM mode. The device remains in PWM mode until EN/UVLO or input power is cycled. The external clock frequency must be between 1.1 x f_{SW} and 1.4 x f_{SW}. The minimum external clock pulse width should be greater than 50ns. The off-time duration of the external clock should be at least 160ns. See the MODE/SYNC section in the *Electrical Characteristics* table for details.

PWM Mode Operation

In PWM mode, the inductor current is allowed to go negative. PWM operation provides constant frequency operation at all loads, and is useful in applications sensitive to switching frequency. However, the PWM mode of operation has lower efficiency at light loads compared to PFM and DCM modes of operation.

PFM Mode Operation

PFM mode of operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak of I_{PFM} (1A, typ) every clock cycle until the output rises to 102.3% of the set nominal output voltage. Once the output reaches 102.3% of the set nominal output voltage, both the high-side and low-side FETs are turned off and the device enters hibernate operation until the load discharges the output to 101.1% of the set nominal output voltage. Most of the internal blocks are turned off in hibernate operation to reduce quiescent current. After the output falls below 101.1% of the set nominal output voltage, the device comes out of hibernate operation, turns on all internal blocks, and again commences the process of delivering pulses of energy to the output until it reaches 102.3% of the set nominal output voltage. The advantage of the PFM mode is higher efficiency at light loads because of lower quiescent current drawn from the supply. However, the output-voltage ripple is higher compared to PWM or DCM modes of operation and switching frequency is not constant at light loads.

DCM Mode Operation

DCM mode of operation features constant frequency operation down to lighter loads than PFM mode, not by skipping pulses, but by disabling negative inductor current at light loads. DCM operation offers efficiency performance that lies between PWM and PFM modes. The output-voltage ripple in DCM mode is comparable to PWM mode and relatively lower compared to PFM mode.

Linear Regulator (V_{CC} and EXTVCC)

The MAX17644 has an internal low dropout (LDO) regulator that powers V_{CC} from V_{IN}. This LDO is enabled during power-up or when EN/UVLO is recycled. When V_{CC} is above its UVLO, if EXTVCC is greater than 4.7V (typ), internal V_{CC} is powered by EXTVCC and LDO is disabled from V_{IN}. Powering V_{CC} from EXTVCC increases efficiency at higher input voltages. The typical V_{CC} output voltage is 5V. Bypass V_{CC} to SGND with a 2.2µF low-ESR ceramic capacitor. V_{CC} powers the internal blocks and the low-side MOSFET driver and recharges the external bootstrap capacitor.

The MAX17644 employs an undervoltage-lockout circuit that forces the buck converter off when V_{CC} voltage falls below V_{CC_UVF} (3.8V, typ). The buck converter enables when the V_{CC} voltages rises above V_{CC_UVR} (4.2V, typ). The 400mV UVLO hysteresis prevents chattering on power-up/power-down.

In applications where the buck-converter output is connected to the EXTVCC pin, if the output is shorted to ground, then the transfer from EXTVCC to internal LDO happens seamlessly without any impact to the normal functionality. Connect EXTVCC pin to SGND when not in use.

Setting the Switching Frequency (RT)

The switching frequency of the device can be programmed from 400kHz to 2.2MHz by using a resistor connected from the RT pin to SGND. The switching frequency (f_{SW}) is related to the resistor connected at the RT pin (R_{RT}) by the following equation:

$$R_{RT} = \frac{21000}{f_{SW}} - 1.7$$

where R_{RT} is in kΩ and f_{SW} is in kHz. Leaving the RT pin unconnected makes the device operate at the default switching frequency of 400kHz. See Table 1 for RT resistor values for a few common switching frequencies.

Table 1. Switching Frequency vs. RT Resistor

SWITCHING FREQUENCY (kHz)	RT RESISTOR (kΩ)
400	Unconnected
400	50.8
500	40.2
2200	8.06

Operating Input-Voltage Range

The minimum and maximum operating input voltages for a given output voltage setting should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + \left(I_{OUT(MAX)} \times \left(R_{DCR(MAX)} + R_{DS\text{-}ONL(MAX)}\right)\right)}{1 - \left(f_{SW(MAX)} \times t_{OFF\text{-}MIN(MAX)}\right)} + \left(I_{OUT(MAX)} \times \left(R_{DS\text{-}ONH(MAX)} - R_{DS\text{-}ONL(MAX)}\right)\right)$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON\text{-}MIN(MAX)}}$$

where:

V_{OUT} = Steady-state output voltage

$I_{OUT(MAX)}$ = Maximum load current

$R_{DCR(MAX)}$ = Worst-case DC resistance of the inductor

$f_{SW(MAX)}$ = Maximum switching frequency

$t_{OFF\text{-}MIN(MAX)}$ = Worst-case minimum switch off-time (160ns)

$t_{ON\text{-}MIN(MAX)}$ = Worst-case minimum switch on-time (80ns)

$R_{DS\text{-}ONL(MAX)}$ and $R_{DS\text{-}ONH(MAX)}$ = Worst-case on-state resistances of low-side and high-side internal MOSFETs, respectively.

Overcurrent Protection (OCP)/Hiccup Mode

The device has a robust overcurrent-protection (OCP) scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit of $I_{PEAK\text{-}LIMIT}$ (4A, typ). A runaway peak current limit on the high-side switch current at $I_{RUNAWAY\text{-}LIMIT}$ (4.7A, typ) protects the device under output short-circuit conditions at high input voltage when there is insufficient output voltage available to restore the inductor current that built up during the on period of the step-down converter. One occurrence of the runaway current limit triggers a hiccup mode. In addition, if feedback voltage drops to $V_{FB\text{-}HICF}$ due to a fault condition, hiccup mode is triggered 1024 clock cycles after soft-start time is completed. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 32,768 clock cycles of half the programmed switching frequency. Once the hiccup timeout period expires, soft-start is attempted again. When soft-start is attempted under overload condition, if feedback voltage does not exceed $V_{FB\text{-}HICF}$, the device continues to switch at half the programmed switching frequency for the time duration of the programmed soft-start time and 1024 clock cycles. The hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

$\overline{\text{RESET}}$ Output

The device includes a $\overline{\text{RESET}}$ comparator to monitor the status of the output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high (high impedance) 1024 switching cycles after the regulator output increases above 95% of the designed nominal regulated voltage. $\overline{\text{RESET}}$ goes low when the regulator output voltage drops to below 92% of the set nominal output voltage. $\overline{\text{RESET}}$ also goes low during thermal shutdown or when the EN/UVLO pin goes below V_{ENF}.

Prebiased Output

When the device starts into a prebiased output, both the high-side and the low-side switches are turned off so that the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse, at which point switching commences. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

Thermal-Shutdown Protection

Thermal-shutdown protection limits junction temperature of the device. When the junction temperature of the device exceeds +165ºC, an on-chip thermal sensor shuts down the device, allowing the device to cool. The device turns-on with soft-start after the junction temperature reduced by 10°C. Soft-start gets de-asserted during thermal shutdown and it initiates the start-up operation when the device recovers from thermal shutdown. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal shutdown during normal operation.

Applications Information

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where $I_{OUT(MAX)}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so

$$I_{RMS(MAX)} = \frac{I_{OUT(MAX)}}{2}$$

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times \left(1 - D\right)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where:

D = V_{OUT}/V_{IN} is the duty ratio of the converter

f_{SW} = Switching frequency

ΔV_{IN} = Allowable input-voltage ripple

η = Efficiency

In applications where the source is located distant from the device input, an appropriate electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). The switching frequency and output voltage determine the inductor value as follows:

$$L = \frac{V_{OUT}}{1.25 \times f_{SW}}$$

where V_{OUT} and f_{SW} are nominal values and f_{SW} is in Hz. Select an inductor whose value is nearest to the value calculated by the previous formula. Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit value of $I_{PEAK-LIMIT}$.

Output-Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitors are sized to support a step load of 1A in the application, so the output-voltage deviation is contained to 3% of the output-voltage change. The minimum required output capacitance can be calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \frac{0.35}{f_C}$$

where:

I_{STEP} = Load current step

$t_{RESPONSE}$ = Response time of the controller

ΔV_{OUT} = Allowable output-voltage deviation

f_C = Target closed-loop crossover frequency

f_{SW} = Switching frequency

Select f_C to be 1/8th of f_{SW} if the switching frequency is less than or equal to 640kHz. If the switching frequency is more than 640kHz, select f_C to be 80kHz. Actual derating of ceramic capacitors with DC bias voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor manufactures.

Soft-Start Capacitor Selection

The device implements adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to SGND programs the soft-start time. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 28 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = \frac{C_{SS}}{5.55 \times 10^{-6}}$$

For example, to program a 1ms soft-start time, a 5.6nF capacitor should be connected from the SS pin to SGND. Note that during start-up, the device operates at half the programmed switching frequency until the output voltage reaches 64.4% of set output nominal voltage.

Setting the Input Undervoltage-Lockout Level

The device offers an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from V_{IN} to SGND (see Figure 1). Connect the center node of the divider to EN/UVLO. Choose R1 to be 3.3MΩ and then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.215}{\left(V_{INU} - 1.215\right)}$$

where V_{INU} is the input-voltage level at which the device is required to turn on. Ensure that V_{INU} is higher than 0.8 x V_{OUT} to avoid hiccup during slow power up (slower than soft start)/power down. If the EN/UVLO pin is driven from an external signal source, a series resistance of minimum 1kΩ is recommended to be placed between the output pin of signal source and the EN/UVLO pin, to reduce voltage ringing on the line.

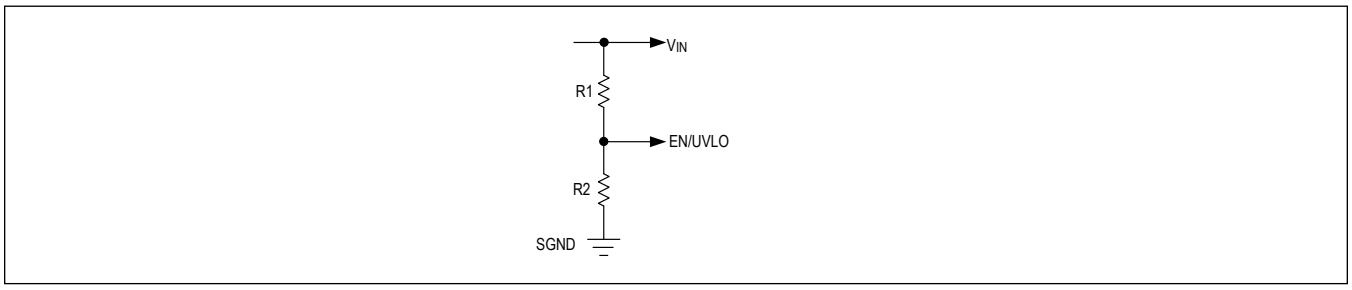


Figure 1. Setting the Input Undervoltage Lockout

Adjusting Output Voltage

Set the output voltage with a resistive voltage-divider connected from the output-voltage node (V_{OUT}) to SGND (see Figure 2). Connect the center node of the divider to the FB pin for MAX17644C. Connect output voltage node (V_{OUT}) to FB pin for MAX17644A and MAX17644B. Use the following procedure to choose the resistive voltage-divider values:

Calculate resistor R_T from the output to the FB pin as follows:

$$R_T = \frac{255}{\left(f_C x C_{OUT\_SEL}\right)}$$

where:

R_T is in kΩ

f_C = Crossover frequency is in Hz

C_{OUT_SEL}= Actual capacitance of selected output capacitor at DC-bias voltage in F

Calculate resistor R_B from the FB pin to SGND as follows:

$$R_B = \frac{R_U \times 0.9}{\left(V_{OUT} - 0.9\right)}$$

R_B is in kΩ

Select an appropriate f_C and C_{OUT} so that the parallel combination of R_B and R_T is less than 50kΩ.

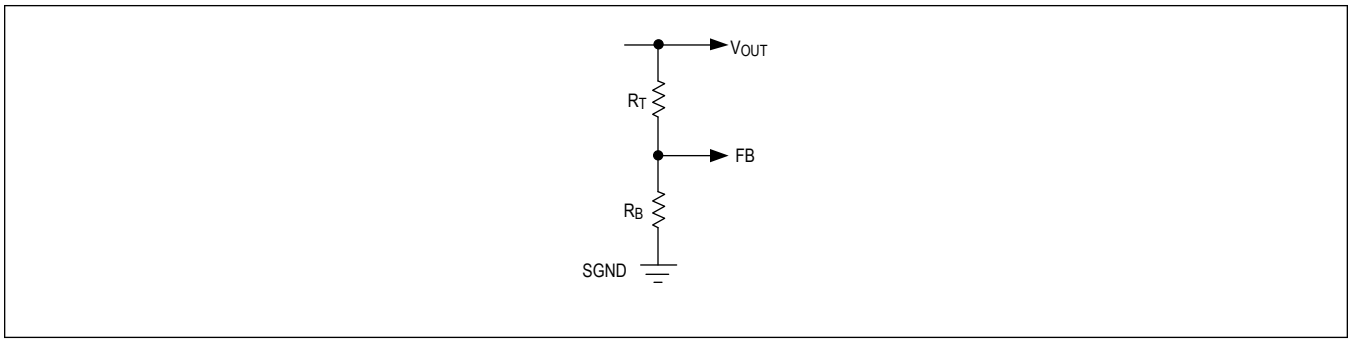


Figure 2. Setting the Output Voltage

Power Dissipation

At a particular operating condition, the power losses that lead to a temperature rise of the part are estimated as follows:

$$P_{LOSS} = \left(P_{OUT} \times \left(\frac{1}{\eta} - 1\right)\right) - \left(I_{OUT}^2 \times R_{DCR}\right) P_{OUT} = V_{OUT} \times I_{OUT}$$

where:

P_{OUT} = Output power

η = Efficiency of the converter

R_{DCR} = DC resistance of the inductor (see the *Typical Operating Characteristics* for more information on efficiency at typical operating conditions)

For a typical multilayer board, the thermal performance metrics for the package are given below:

θ_{JA} = 33ºC/W θ_{JC} = 4ºC/W

The junction temperature of the device can be estimated at any given maximum ambient temperature ($T_{A(MAX)}$) from the following equation:

$$T_{J(MAX)} = T_{A(MAX)} + \left(\theta_{JA} \times P_{LOSS}\right)$$

If the application has a thermal-management system that ensures that the exposed pad of the device is maintained at a given temperature ($T_{EP(MAX)}$) by using proper heat sinks, then the junction temperature of the device can be estimated at any given maximum ambient temperature as:

$$T_{J(MAX)} = T_{EP(MAX)} + \left(\theta_{JC} \times P_{LOSS}\right)$$

Note: Junction temperatures greater than +125°C degrades operating lifetimes.

PCB Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since the inductance of a current-carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small-current loop areas reduce radiated EMI.

A ceramic input filter capacitor should be placed close to the V_{IN} pins of the IC. This eliminates as much trace inductance effects as possible and gives the IC a cleaner voltage supply. A bypass capacitor for the V_{CC} pin also should be placed close to the pin to reduce the effects of trace impedance.

When routing the circuitry around the IC, the analog small signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is minimal. This helps keep the analog ground quiet. The ground plane should be kept continuous (unbroken) as far as possible. No trace carrying high switching current should be placed directly over any ground plane discontinuity.

PCB layout also affects the thermal performance of the design. A number of thermal throughputs that connect to a large ground plane should be provided under the exposed pad of the part, for efficient heat dissipation.

For a sample layout that ensures first pass success, refer to the MAX17644 evaluation kit layout available at www.maximintegrated.com.

Typical Application Circuits

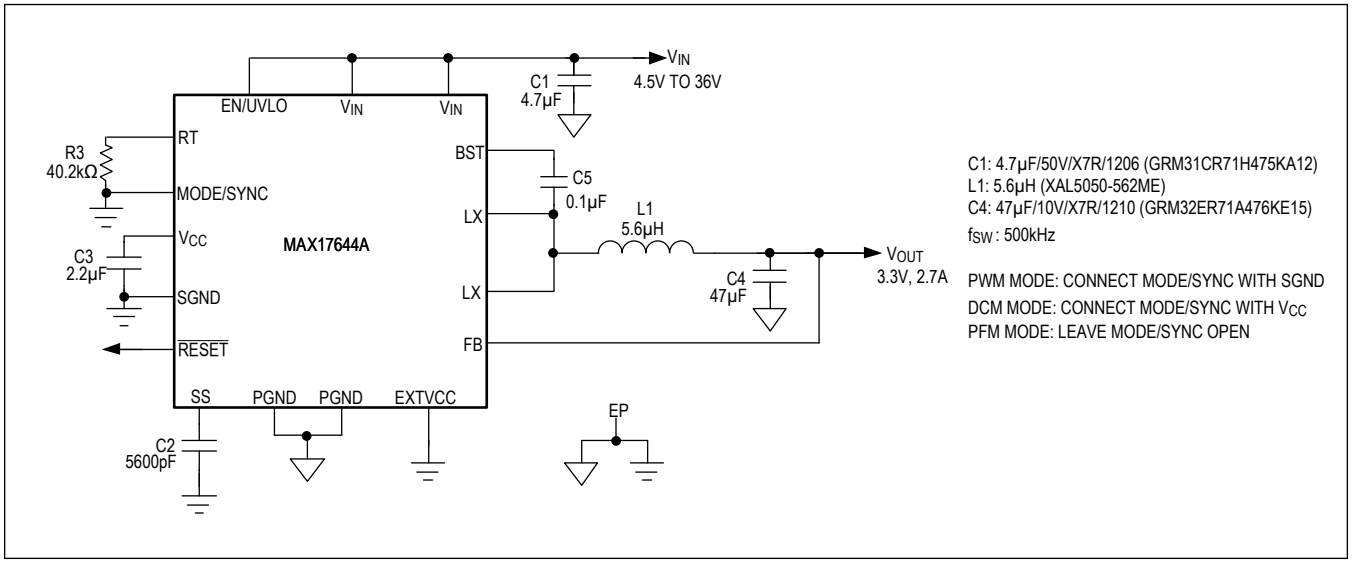


Figure 3. Fixed 3.3V Output with 500kHz Switching Frequency

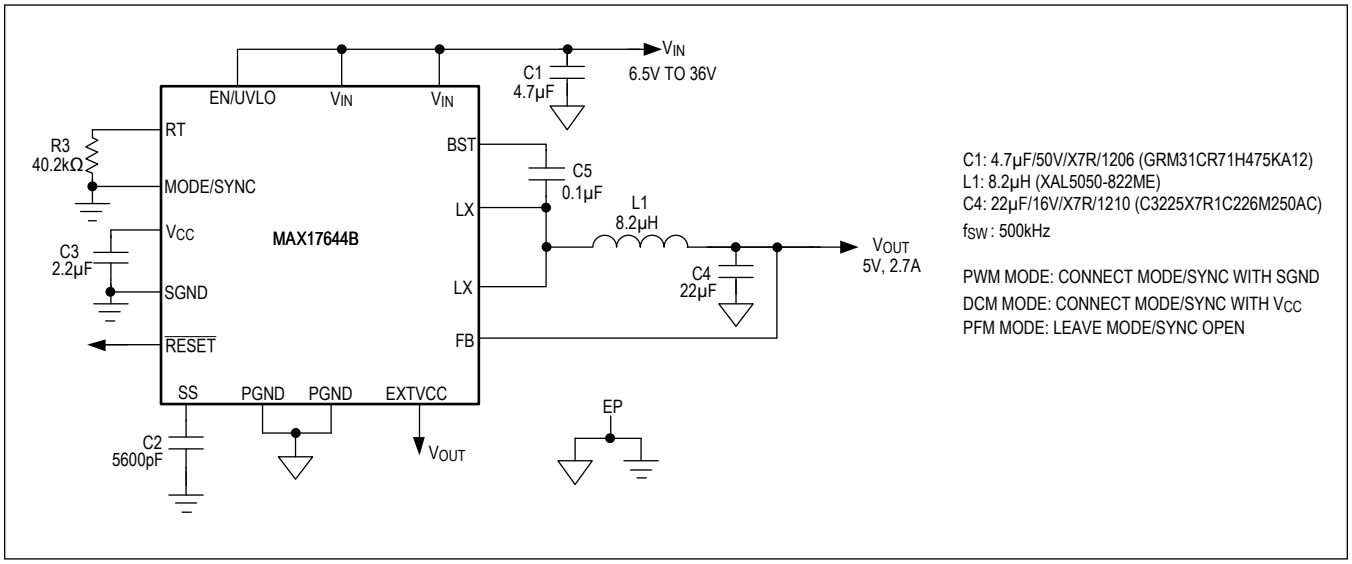


Figure 4. Fixed 5V Output with 500kHz Switching Frequency

Typical Application Circuits (continued)

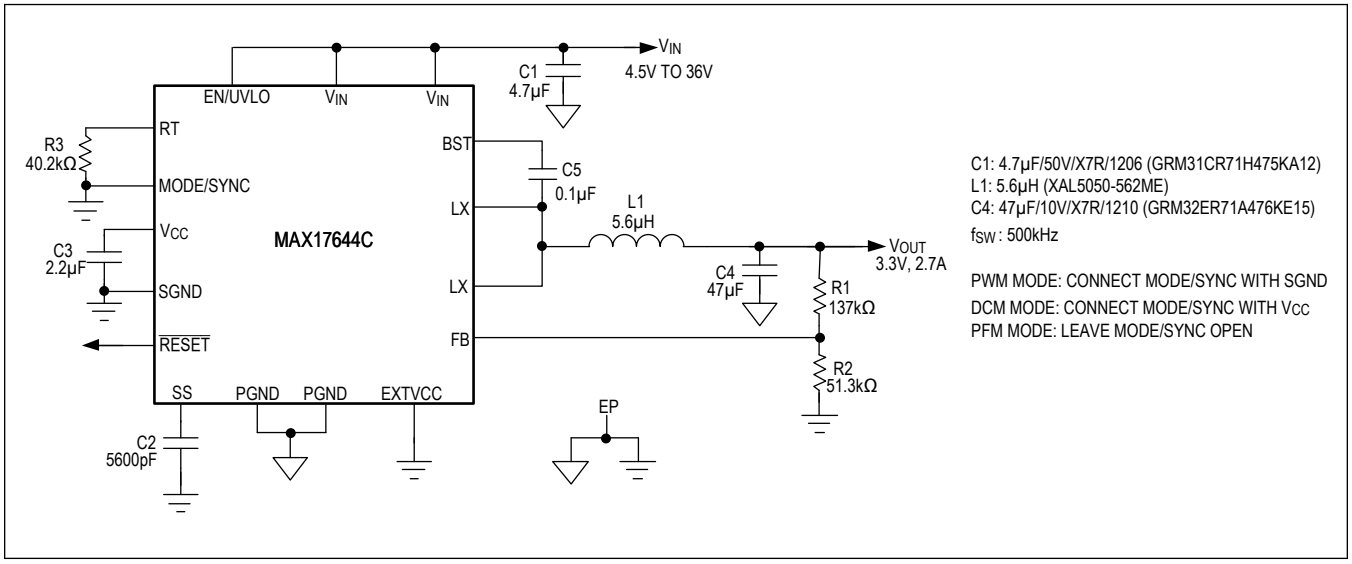


Figure 5. Adjustable 3.3V Output with 500kHz Switching Frequency

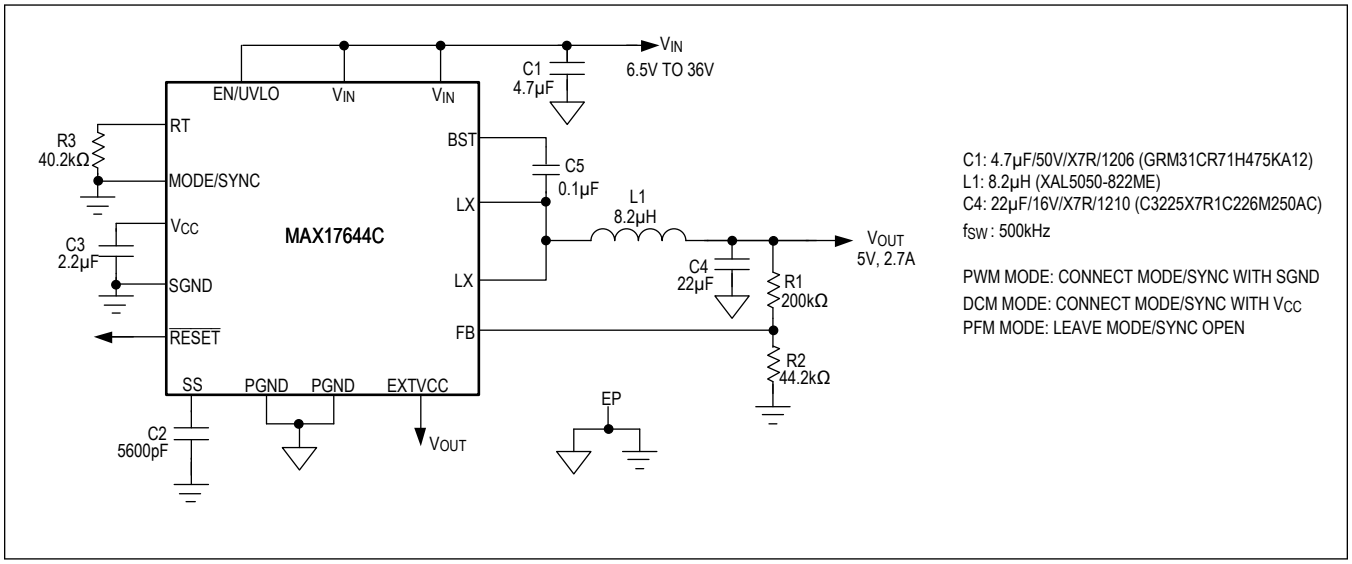


Figure 6. Adjustable 5V Output with 500kHz Switching Frequency

Ordering Information

PART NUMBER	OUTPUT VOLTAGE (V)	PIN-PACKAGE
MAX17644AATE+	3.3	16 TQFN 3mm x 3mm
MAX17644AATE+T	3.3	16 TQFN 3mm x 3mm
MAX17644BATE+	5	16 TQFN 3mm x 3mm
MAX17644BATE+T	5	16 TQFN 3mm x 3mm
MAX17644CATE+	Adjustable	16 TQFN 3mm x 3mm
MAX17644CATE+T	Adjustable	16 TQFN 3mm x 3mm

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed Pad.*

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/21	Release for Market Intro	—

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX17644AATE+ MAX17644BATE+ MAX17644CATE+