Integrated Protection IC on 12V Bus with an Integrated MOSFET, Lossless Current Sensing, and PMBus Interface

General Description

The MAX16550/MAX16551 are protection ICs with an integrated low-resistance MOSFET and lossless current-sense circuitry featuring SMBus/PMBus™ control and reporting. The ICs are designed to provide the optimum solution for distribution, control, monitoring and protection of the system's 12V power supply. An internal LDO provides the supply voltage for the protection IC.

If no fault is detected, the ICs initiate the startup and have been designed to provide controlled, monotonic startup. Programmable soft-start ramp and delay is implemented to limit the in-rush current during startup.

The ICs monitor the current and voltage of the 12V system power rail and provide multiple levels of protection with fast turn-off if a fault is detected. The MAX16551 also provides PMBus-programmable 240VA overpower-fault protection.

Maxim's patented, lossless current sense provides high accuracy current sensing over load and temperature, improving overall system-energy efficiency, and reducing dissipation.

Output voltage is monitored at all times. If at any time the output voltage falls below the programmable output undervoltage-lockout threshold, the PWRGD signal is asserted low. If at any time the input voltage falls below the programmable input undervoltage-lockout threshold, the PWRGD signal is asserted low. The ICs can be programmed through PMBus to provide input overvoltage protection. Input overvoltage protection is disabled by default. When enabled through PMBus, if the input voltage exceeds a programmable overvoltage threshold, the MOSFET is latched off and a fault indicated.

See the *Basic Application Circuit* utilizing the MAX16550/MAX16551 ICs.

PMBus is a trademark of SMIF, Inc.

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Two Options: MAX16550—30A Protection IC
  MAX16551—240VA Power Protection
- High-Density (4mm x 4.5mm for 30A): Less than 25% of the Board Area of Conventional Solutions
  - Monolithic Integration of Power, Control, and Monitoring
  - Integrated Power MOSFET with 1.9mΩ Total Resistance in 12V Power Path ($R_{DS(ON)}$ Including Package)
  - Integrated Lossless, Precise Current Sensing
  - Integrated LDO Provides V_{DD} Supply (1.8V Bias Suppy)
- Enables Advanced System Power Management—PMBus/SMBus Telemetry with Extensive Status Monitoring and Reporting
  - Load Current Indicator (ILOAD) Pin Provides Analog Output Current Reporting with High Accuracy
  - Programmable Soft-Start for Inrush Current Limiting
  - Increases Power-Supply Reliability with IC Self-Protection Features
    - Very Fast Fault Detection and Isolation
    - V_{IN} to V_{OUT} Short Protection During Startup
    - Overtemperature Protection
  - Three Levels of Overcurrent Protection
    - Programmable Moderate OCP
    - Programmable Severe OCP Provides Isolation < 5µs.
    - Fail-Safe Safe OCP Provides Isolation < 250ns.

Additional Features

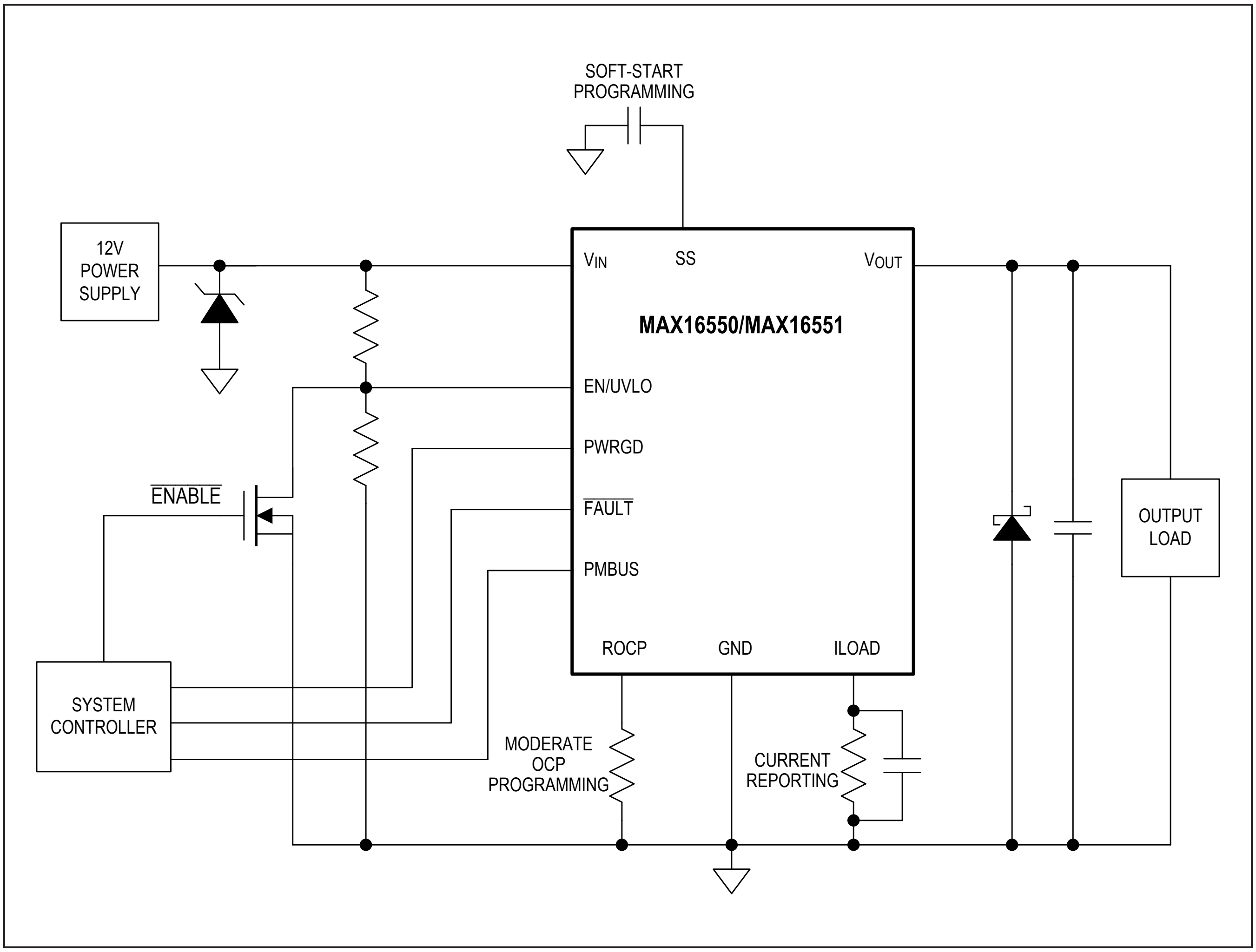
- Programmable Soft-Start and Delay
- Programmable Input Undervoltage-Lockout Threshold (UVLO)
- Programmable Power-Good Threshold
- PWRGD Pin for Output UVLO/Input UVLO Reporting
- $\overline{\text{FAULT}}$ Pin for Fault Reporting

Systems and Applications

Servers, Networking, Storage, Communication Equipment and AC/DC Power Supplies

- Integrated Protection IC on 12V
  - Circuit Breaker/E-Fuse, Hot Swap
  - 240VA

Basic Application Circuit



Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{IN}) DC ....-0.3V to +16V
Supply Voltage (V_{IN}) 150µs 22V
Bias Supply Voltage (V_{DD})..................................-0.3V to +2.5V
PWRGD, $\overline{FAULT}$..-0.3V to +5.5V
EN/UVLO, R_{OCP} ....-0.3V to +2.5V
SMBUS_CLK, SMBUS_DATA,
$\overline{SMBUS\_ALERT}$ 6V
SMBUS_ID ....-0.3V to +2.5V
ILOAD...-0.3V to +2.5V
Output Voltage (V_{OUT}) DC..................................-0.3V to +16V
BST (Relative to V_{OUT})......................................-0.3V to +2.5V
SS..-0.3V to +16V
Junction Temperature (T_J)...150°C
Storage Temperature Range .... -65°C to +165°C
Peak Reflow Temperature ....260°C

Operating Ratings

Supply Voltage (V_{IN}) .... 10.8V to 13.2V
Bias Supply Voltage (V_{DD})................................ 1.76V to 1.94V
Junction Temperature (T_J)..................................0°C to +125°C

Package Thermal Characteristics

Junction-to-Case Thermal Resistance (θ_{JC}, max).......0.31°C/W

Note 1: These products are completely Halogen-free and Pb-free, employing special materials sets: molding compounds/die attach materials and 100% matte tin plate including anneal. These products are RoHS compliant with an -e3 termination finish and are compatible with both SnPb and Pb-free soldering operations. These products are MSL classified at peak reflow temperatures that meet JEDEC JSTD-020.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{IN} = 12V ±10%, unless otherwise noted. T_J = 0 to +125°C, unless otherwise noted. Specifications are 100% production tested at T_A = +32°C. Limits over operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
12V SUPPLY (V_{IN})						
Supply Voltage Range	V_{IN}		10.8	12	13.2	V
Device Supply Current	I_{IN}	FET off	3.0		6.25	mA
		FET on: I_{OUT} = 0 (Note 2)	3.7		6.75	
		FET on: I_{OUT} = 30A (Note 2)			10	
INTEGRATED 1.8V LINEAR REGULATOR						
LDO Output Voltage Range	V_{DD}		1.76	1.85	1.94	V
V_{DD} Falling		(Note 2)	1.55	1.6	1.7	
V_{DD} Rising		(Note 2)	1.62	1.67	1.73	
Hysteresis		(Note 2)	30	60	80	mV
V_{DD} UVLO Response Time		(Note 2)		2		µs
UNDERVOLTAGE LOCKOUT: 12V SUPPLY (V_{IN})						
V_{IN}_UVLO Rising Threshold	V_{IN_UVLO}	At EN/UVLO pin	0.95	1	1.05	V
V_{IN}_UVLO Hysteresis				50		mV
Programmable 12V V_{IN} Undervoltage Threshold for Rising Input	V_{IN_UVLO}	Programmable through resistor-divider, measured at V_{IN}	8			V
Response Time	t_D	From EN/UVLO = 0V to FET off		2		µs

Electrical Characteristics (continued)

(V_{IN} = 12V ±10%, unless otherwise noted. T_J = 0 to +125°C, unless otherwise noted. Specifications are 100% production tested at T_A = +32°C. Limits over operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN_UVLO PIN INTERNAL PARAMETERS						
EN_UVLO Pin Leakage		EN_UVLO = 1.8V	5	6.7	11	µA
EN_UVLO Internal Pulldown Resistor			110	250	450	kΩ
BOOST VOLTAGE (V_{BST})						
V_{BST} Charging Time to 1.6V Above V_{OUT}	t_{CHARGE}	C_{BST} = 100nF		150		µs
BST Voltage Above V_{OUT}	V_{BST}			1.8		V
Rising UVLO Threshold Above V_{OUT}	BOOST UVLO	(Note 2)	0.8	1.2	1.6	V
Falling UVLO Threshold Above V_{OUT}	BOOST UVLO	(Note 2)	0.74	1.1	1.5	V
UVLO Hysteresis	BOOST UVLO	(Note 2)	60	130	400	mV
Falling Lockout Response Time	t_D			1.5		µs
INTEGRATED MOSFET CHARACTERISTICS						
On-Resistance	$R_{DS(ON)}$	(Note 2)		1.9		mΩ
COMMON OVERCURRENT PROTECTION						
Severe OCP Threshold, % Above Moderate OCP	$I_{OCP(SEVERE)}$	Digitally programmable		130 170		%
Severe OCP Threshold Accuracy	$I_{OCP(SEVERE)}$			±20		%
Severe OCP Delay	$t_{D(SEVERE)}$	From fault threshold exceeded to FET off (Note 3)		5		µs
Gain from ROCP Pin Current	G_{OCP}	(Note 2)		4		A/µA
Allowed Range for No-Fault Detection	ROCP		28		360	kΩ
Startup OCP Threshold	$I_{OCP\_STARTUP}$	Programmed through PMBus default setting = 8A (Note 2)		4 8 12 16		A
Startup OCP Threshold Accuracy		I_{OUT} = 4A I_{OUT} = 8A, 12A, 16A		±30 ±20		%
Safe OCP Threshold	I_{OCP_SAFE}	(Note 2)		60		A
Safe OCP Threshold Accuracy	I_{OCP_SAFE}	V_{IN} = 12V, T = +125°C		±20		%
Safe OCP Delay	t_{D_SAFE}	From fault threshold exceeded to FET off		250		ns

Electrical Characteristics (continued)

(V_{IN} = 12V ±10%, unless otherwise noted. T_J = 0 to +125°C, unless otherwise noted. Specifications are 100% production tested at T_A = +32°C. Limits over operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OVERCURRENT PROTECTION (MAX16550)						
Gain from ROCP Pin Current	G_{OCP}	Gain from ROCP pin current to I_{OUT} (Note 2)		4		A/µA
Moderate OCP Voltage Threshold	V_{OCPM}	Referred to voltage over ROCP (Note 2)		0.8		V
Moderate OCP Voltage Threshold Accuracy	V_{OCPM}	Referred to I_{OUT} using Equation 1		±12		%
Moderate OCP Threshold Range	$I_{OCP(MODERATE)}$	Analog programmable through ROCP	15		35	A
Allowable ROCP Range for ROCP_ Fault Detection at Power-Up	ROCP		28		360	kΩ
Moderate OCP Timeout	t_{OCPM}	I_{OUT} > moderate OCP, I_{OUT} < severe OCP, programmable default moderate OCP timeout = 100µs (Note 3)		12.5 100 100 250		µs µs ms ms
Moderate OCP Fault-Detect Delay Timeout Accuracy	t_{OCPM}	(Note 3)		±10		%
OVERCURRENT PROTECTION (MAX16551)						
Reference OCP Voltage Threshold	V_{OCP_REF}	Referred to voltage over R_{OCP} (Note 2)		0.8		V
POWER PROTECTION (MAX16551)						
Power Fault Threshold	P_{IN_FAULT}	R_{ILOAD} = 10.2kΩ (Note 2)		240		VA
Power Fault Threshold Accuracy	P_{IN_FAULT}			±4		%
Power Fault-Detection Delay Timeout	t_{FAULT}	P_{IN} > pin fault, I_{IN} < severe OCP threshold, programmable = 4ms (Note 2)		4 100 250		ms
Power Fault-Detection Delay Timeout Accuracy	t_{FAULT}	(Note 3)		±10		%
Startup OCP Delay	$td_{(STARTUP)}$	(Note 3)		7		µs
SOFT-START AND C_{OUT}						
Soft-Start Discharge Resistance	SS			1	2	kΩ
Soft-Start Charging Current	I_{SS}		20		39	µA
Soft-Start Capacitor Value Range	C_{SS}	Linear startup ramp	0		75	nF
Soft-Start Time	t_{SS}	C_{SS} = 0nF, I_{OUT} = 0A (Note 3)		1		ms
Soft-Start Capacitor Discharge Threshold			0.17	0.2	0.25	V
CSS Discharge Check Duration During Startup		(Note 3)		2.2		s
Recommended Output Capacitance Range	C_{OUT}	(Note 2)	10		10000	µF

Electrical Characteristics (continued)

(V_{IN} = 12V ±10%, unless otherwise noted. T_J = 0 to +125°C, unless otherwise noted. Specifications are 100% production tested at T_A = +32°C. Limits over operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FET V_{GS} UNDERVOLTAGE LOCKOUT						
V_{GS} Rising UVLO Threshold	V_{GS_UVLO}		0.87	1.3	1.61	V
V_{GS} Falling UVLO Threshold			0.74	1.17	1.50	
V_{GS} UVLO Hysteresis			87	100	466	mV
V_{GS} UVLO Masking Time		During startup (Note 3)		100		ms
V_{GS} UVLO Deglitching		(Note 3)		10		µs
PASS FET SHORT DETECTION DURING STARTUP						
Duration of V_{OUT} Discharge Check	$t_{DISCHARGE}$	(Note 3)		2.2		s
Pulldown Resistance on V_{OUT} During Self-Check	$R_{DISCHARGE}$		400	455	560	Ω
Threshold for Self-Check Procedure	$V_{OUT\_SELF CHECK}$	SMBus/PMBus programmable, default 9V (Note 2)	5.8 6.8 7.7 8.8	6 7 8 9	6.2 7.2 8.2 9.4	V
Delay from Self-Check Pass to Start V_{OUT} Ramp	t_D	Programmable (Note 3)		0 10 20		µs
PWRGD PIN						
Max Allowable PWRGD Output High Voltage	V_{OH}	External pullup leakage below 1µA		5.5		V
PWRGD Output Low Voltage	V_{OL}	Sinking 4Ma			0.4	V
Propagation Delay from V_{OUT_UVLO} Detect to PWRGD Pin Asserted Low	t_D	(Note 3)		3.2		µs
Threshold for PWRGD Asserted High	$V_{TH(PWRGD)}$	SMBus/PMBus programmable, default 11V (Note 2)		8 9 10 11		V
PWRGD Clear Timing Time Needed to Clear PWRGD after V_{OUT} Has Reached V_{IN}		(Note 3)		5		ms
PWRGD Hysteresis		(Note 2)	0.35	0.5	0.63	V
PWRGD Accuracy			-5		+5	%
OVERTEMPERATURE PROTECTION						
Overtemperature-Protection Threshold	T_{OTP}	PMBus programmable (Note 2)		140		°C

Electrical Characteristics (continued)

(V_{IN} = 12V ±10%, unless otherwise noted. T_J = 0 to +125°C, unless otherwise noted. Specifications are 100% production tested at T_A = +32°C. Limits over operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SMBus DATA (SMBUS_DATA) AND CLOCK (SMBUS_CLOCK) PINS						
Leakage Current		For pullup = 5.5V (Note 2)		5.3		µA
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.1			V
Output Low Voltage	V_{OL}	SMBUS_DATA, sinking 4mA			0.4	V
Max Allowable External Pullup Voltage	V_{OH} MAX			5.5		V
SMBus ALERT PIN						
Output Low Voltage	V_{OL}	Sinking 4mA			0.4	V
Leakage Current		For pullup = 5.5V (Note 2)			1	µA
Max Allowable External Pullup Voltage	V_{OH} MAX			5.5		V
FAULT-ISOLATION DELAY						
Fault-Detection Time	t_D	Fault detection to start of gate pulldown (Note 3)		60		ns
Pass FET Turn-Off Time	t_F	From start of gate pulldown to pass FET off (Note 3)		50		ns
$\overline{\text{FAULT}}$ PIN						
Input High Voltage	V_{IH}	(Note 2)	1			V
Input Low Voltage	V_{IL}	(Note 2)			0.66	V
Max Allowable $\overline{\text{FAULT}}$ Output High Voltage	V_{OH}	External pullup, leakage below 1µA		5.5		V
$\overline{\text{FAULT}}$ Output Low Voltage	V_{OL}	Sinking 4mA			0.4	V
Propagation Delay from Fault Detect to $\overline{\text{FAULT}}$ Asserted Low	t_D	(Note 3)		100		ns
V_{IN} OVERVOLTAGE PROTECTION						
Programmable Threshold for OVP	V_{IN_OVP}	Measured at V_{IN}, programmable (Note 2)		14 16		V
V_{IN} Overvoltage Accuracy	V_{IN_OVP}		-5		+5	%
Deglitching Time	t_{FILTER_OVP}	(Note 3)		20		µs
CURRENT REPORTING (ILOAD) PIN						
Linear I_{OUT} Reporting Range		Current-reporting range	0		30	A
Max Allowable Linear Voltage Range				1.35		V
Offset Current		I_{OUT} = 0A		0.32		µA

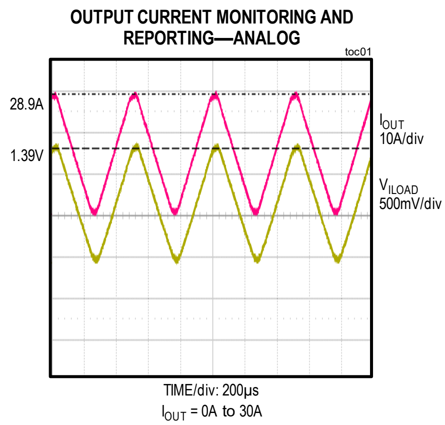
Electrical Characteristics (continued)

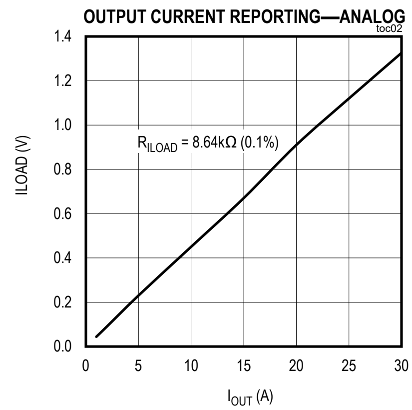
(V_{IN} = 12V ±10%, unless otherwise noted. T_J = 0 to +125°C, unless otherwise noted. Specifications are 100% production tested at T_A = +32°C. Limits over operating temperature range are guaranteed by design and characterization.)

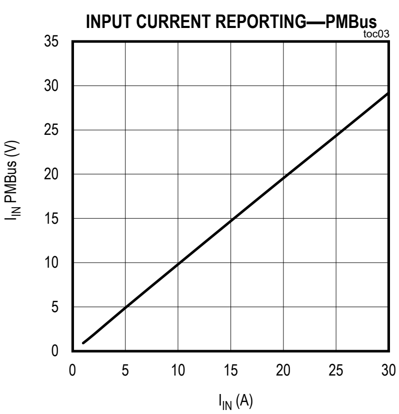
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Reporting Gain	G_{ILOAD}	ILOAD current divided by I_{OUT} current (Note 2)		5		µA/A
Bandwidth		No capacitor in parallel with R_{LOAD} resistor	100			kHz
ANALOG CURRENT-REPORTING ACCURACY						
Current-Reporting Accuracy (Notes 3, 4, 5)	I_{OUT}	I_{OUT} = 4A	-2.5		+2.5	%
		I_{OUT} = 30A	-1.8		+1.8	
SMBus/PMBus TELEMETRY						
Digital Current-Reporting Accuracy	READ_IOUT (8Ch), READ_IIN (89h)	I_{OUT} = 4A		±3		%
		I_{OUT} = 30A		±2		
Digital Power-Reporting Accuracy	READ_PIN (97h)	Digital, I_{OUT} = 4A, V_{IN} = 12V, R_{LOAD} = 9kΩ (MAX16550) R_{LOAD} = 10.2kΩ (MAX16551)		±5		%
		Digital, I_{OUT} = 30A, V_{IN} = 12V, R_{LOAD} = 9kΩ (MAX16550) R_{LOAD} = 10.2kΩ (MAX16551)		±3.5		
Digital Input-Voltage Reporting Accuracy	READ_VIN (88h)			±1.2		%
Digital Output-Voltage Reporting Accuracy	READ_VOUT (8Bh)			±1.2		%
Digital Temperature-Reporting Accuracy	READ_ TEMPERATURE_1 (8Dh)			±8		°C
Digital Energy-Reporting Accuracy	READ_EIN (86h)	I_{OUT} = 4A		±5		%
		I_{OUT} = 30A		±3		

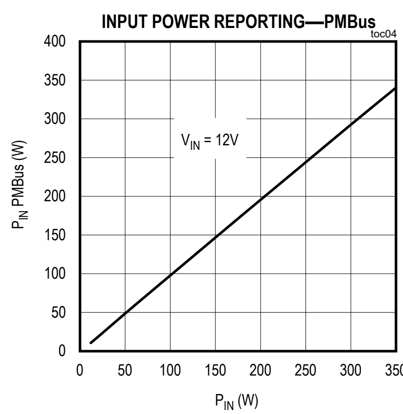
Note 2: Denotes specificaltion that apply for typical operating junction temperature (T_J = +25°C).
Note 3: Guaranteed by design, not production tested.
Note 4: Reporting accuracy presented includes 0.1% external resistor tolerance contribution.
Note 5: Min/max limits are ≥ 4σ about the mean.

Typical Operating Characteristics

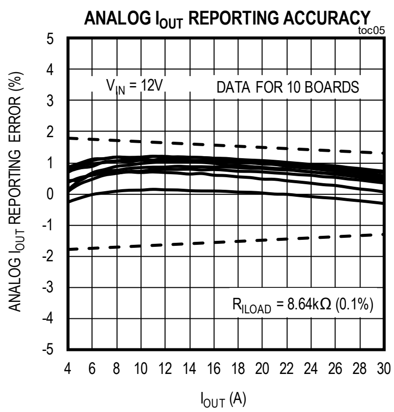


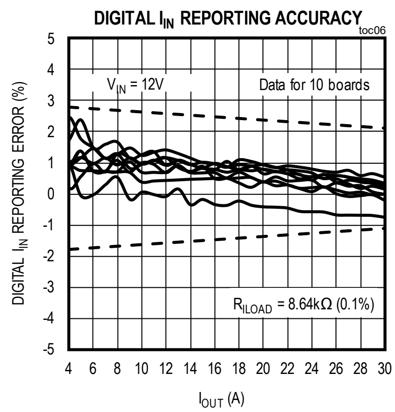


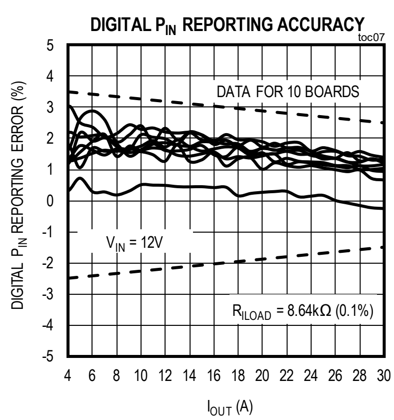


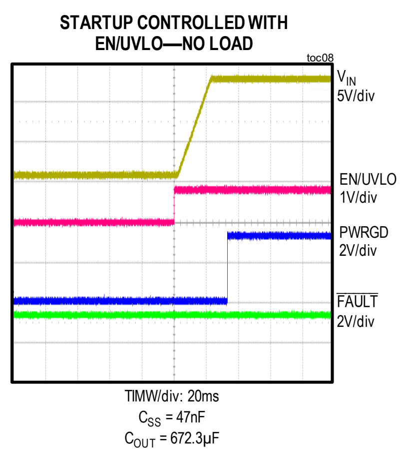


Typical Operating Characteristics (continued)



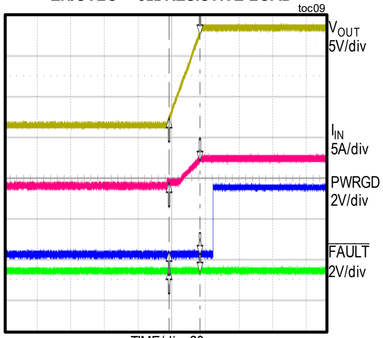






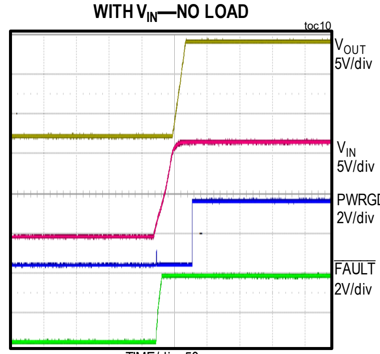
Typical Operating Characteristics (continued)

STARTUP INTO LOAD CONTROLLED WITH EN/UVLO—3Ω RESISTIVE LOAD



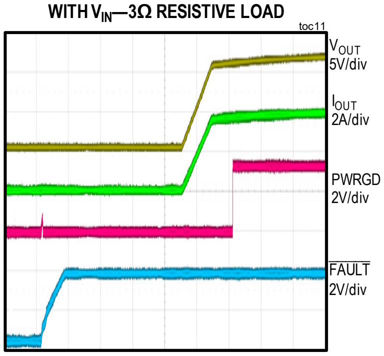
R_{LOAD} = 3Ω, PRESENT AT STARTUP
C_{SS} = 47nF
C_{OUT} = 672.3µF

STARTUP CONTROLLED WITH V_{IN}—NO LOAD



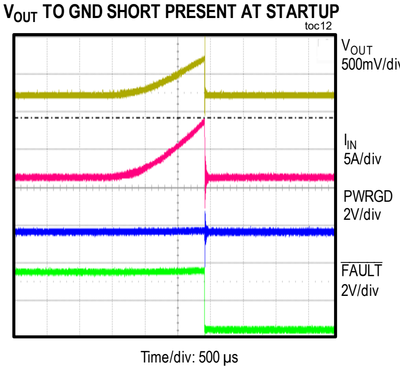
C_{SS} = 47nF
C_{OUT} = 0µF

STARTUP INTO LOAD CONTROLLED WITH V_{IN}—3Ω RESISTIVE LOAD



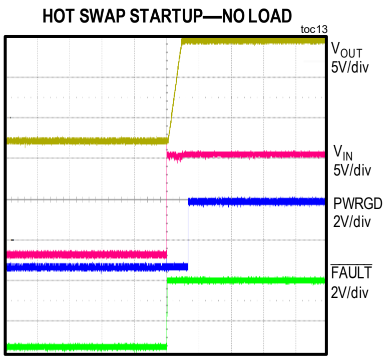
R_{LOAD} = 3Ω, PRESENT AT STARTUP
C_{SS} = 47nF
C_{OUT} = 0µF

START INTO SHORT CONDITION, V_{OUT} TO GND SHORT PRESENT AT STARTUP

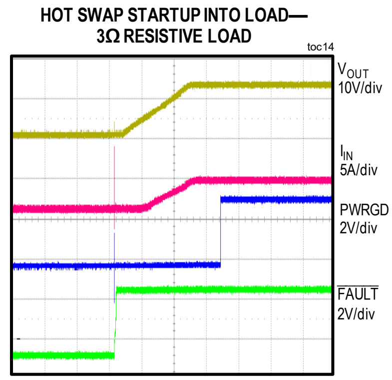


Time/div: 500 µs
V_{OUT} Shorted to GND Prior to Startup

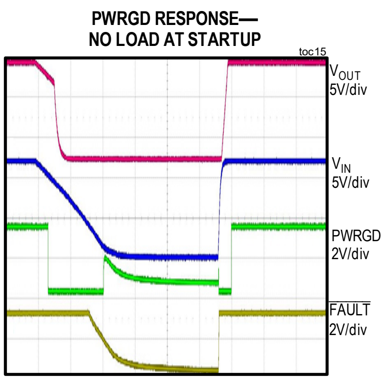
Typical Operating Characteristics (continued)



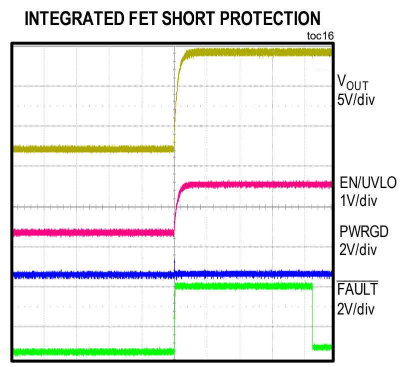
C_{SS} = 47nF
C_{OUT} = 672.3µF
NO LOAD AT STARTUP



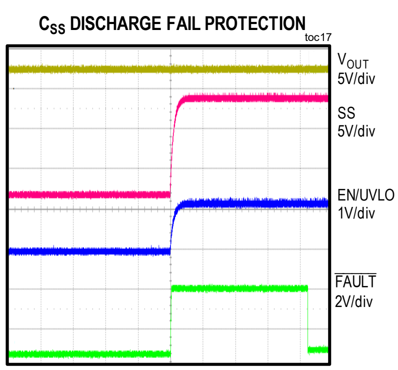
C_{SS} = 47nF
C_{OUT} = 0µF
NO INPUT CAPACITORS



TIME/div: 100ms
C_{SS} = 47nF
PWRGD THRESHOLD = 11V
VIN_UVLO THRESHOLD = 8V

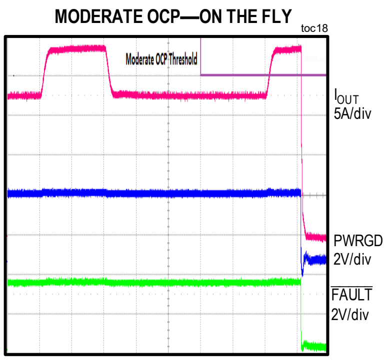


TIME/div: 500ms
V_{OUT} SHORTED TO V_{IN}
PRIOR TO STARTUP

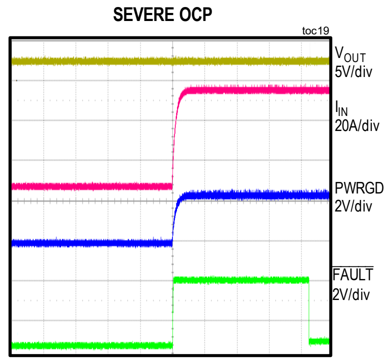


TIME/div: 500ms
C_{SS} = 47nF
SS SHORTED TO V_{IN}
PRIOR TO STARTUP

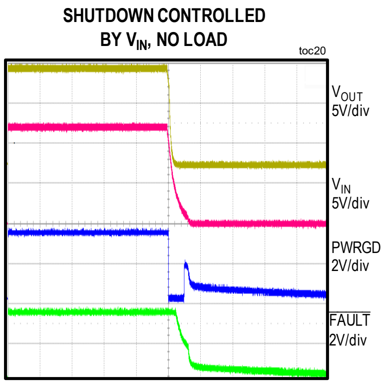
Typical Operating Characteristics (continued)



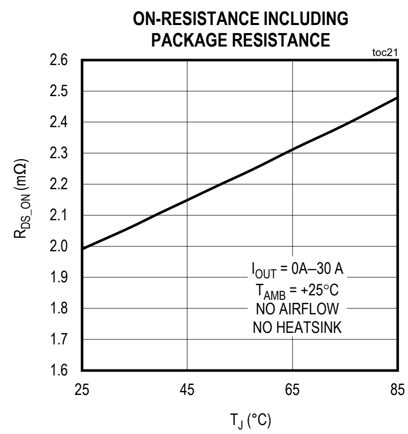
TIME/div: 100µs
OCPM_HIGH = 34 A; OCPM_LOW = 20 A;
I_{OUT} = 18A to 24A; t = 200µs;
MODERATE OCP TIMEOUT = 100µs

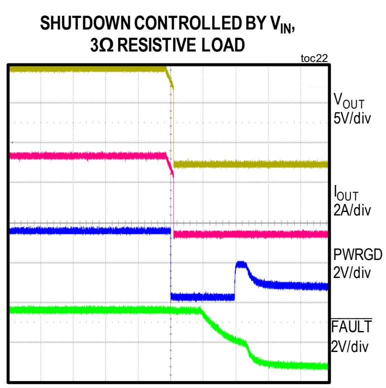


TIME/div: 1ms
I_{OUT} = 30A to 40A; OCPM = 34A;
MODERATE OCP TIMEOUT = 100µs;
SEVERE OCP SETTING = 130%



TIME/div: 200ms
I_{OUT} = 0A
FAULT AND PWRGD PULLUP VOLTAGES DERIVED FROM 12V SUPPLY

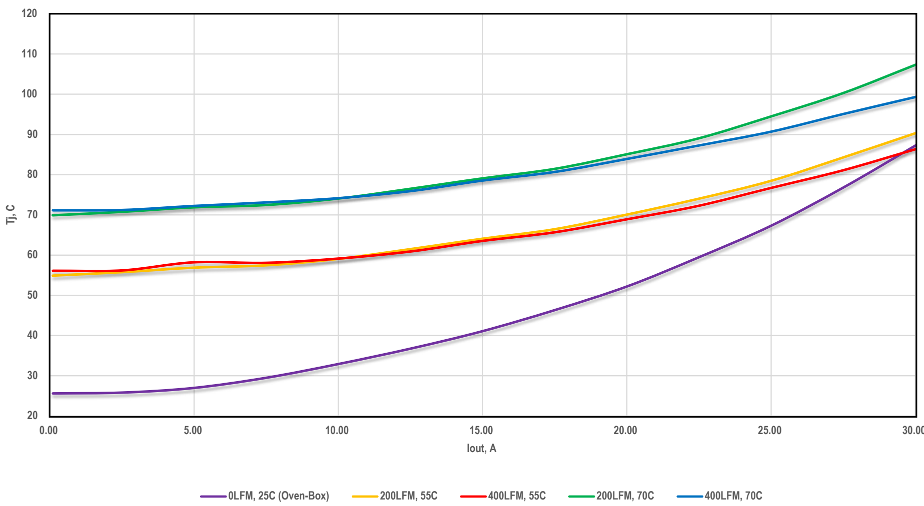




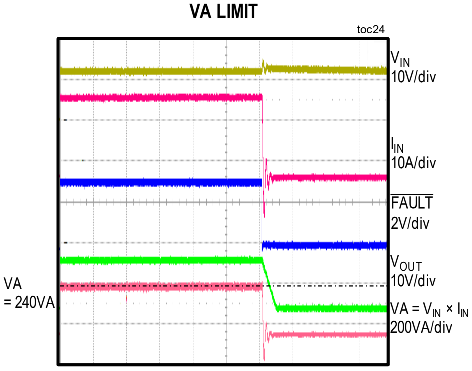
TIME/div: 50ms
R_{LOAD} = 3Ω

Typical Operating Characteristics (continued)

THERMAL EVALUATION

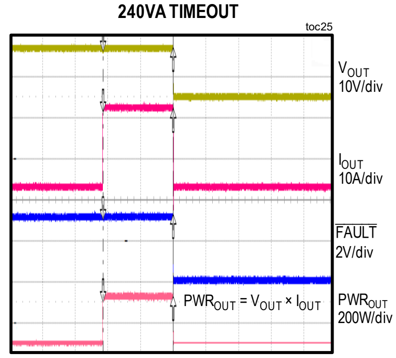


VA LIMIT



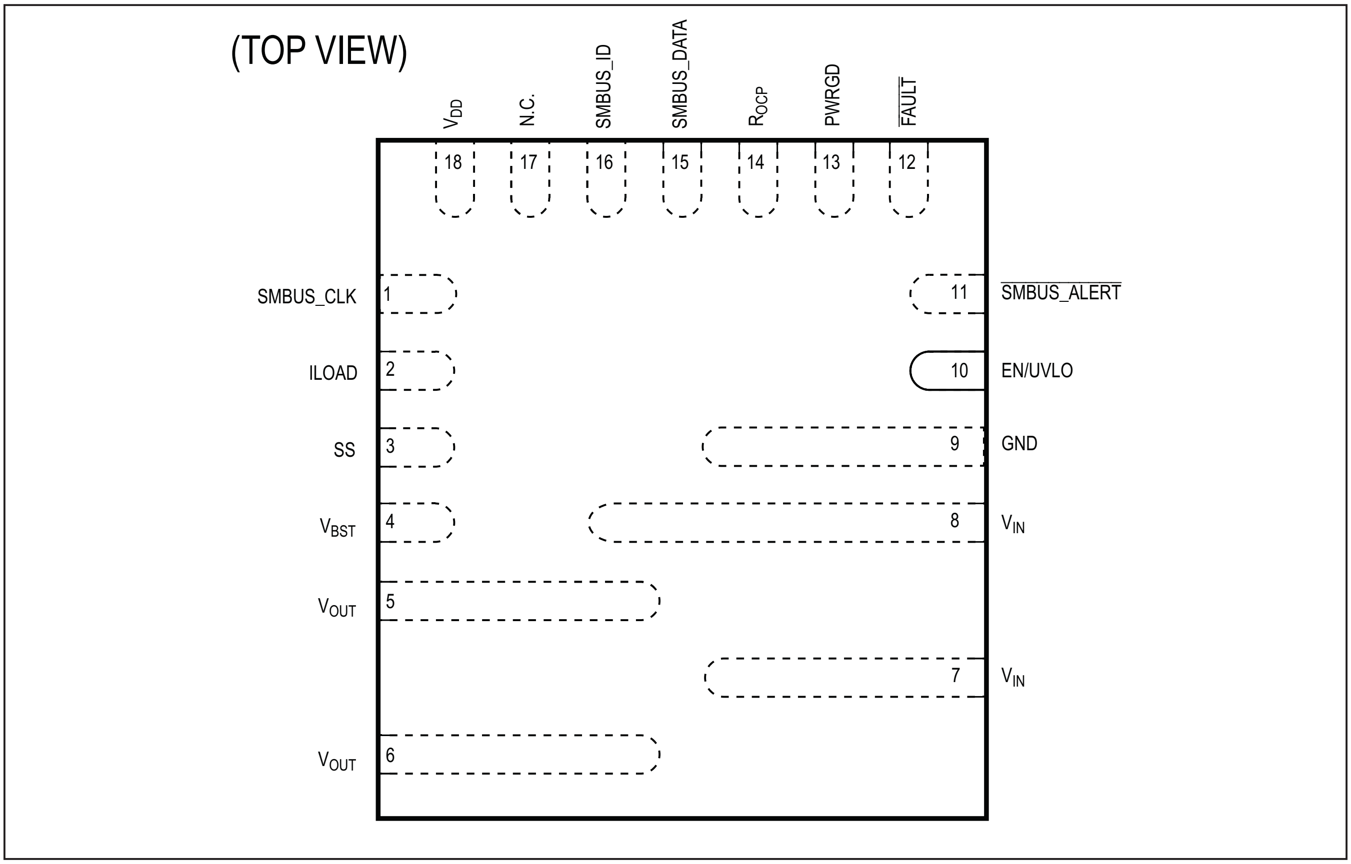
TIME/div: 1ms
V_{OUT} = 12V
I_{OUT} = 20A

240VA TIMEOUT



TIME/div: 50ms
I_{OUT} = 19.89A
t = 200ms
240 VA TIMEOUT = 100ms

Pin Configuration



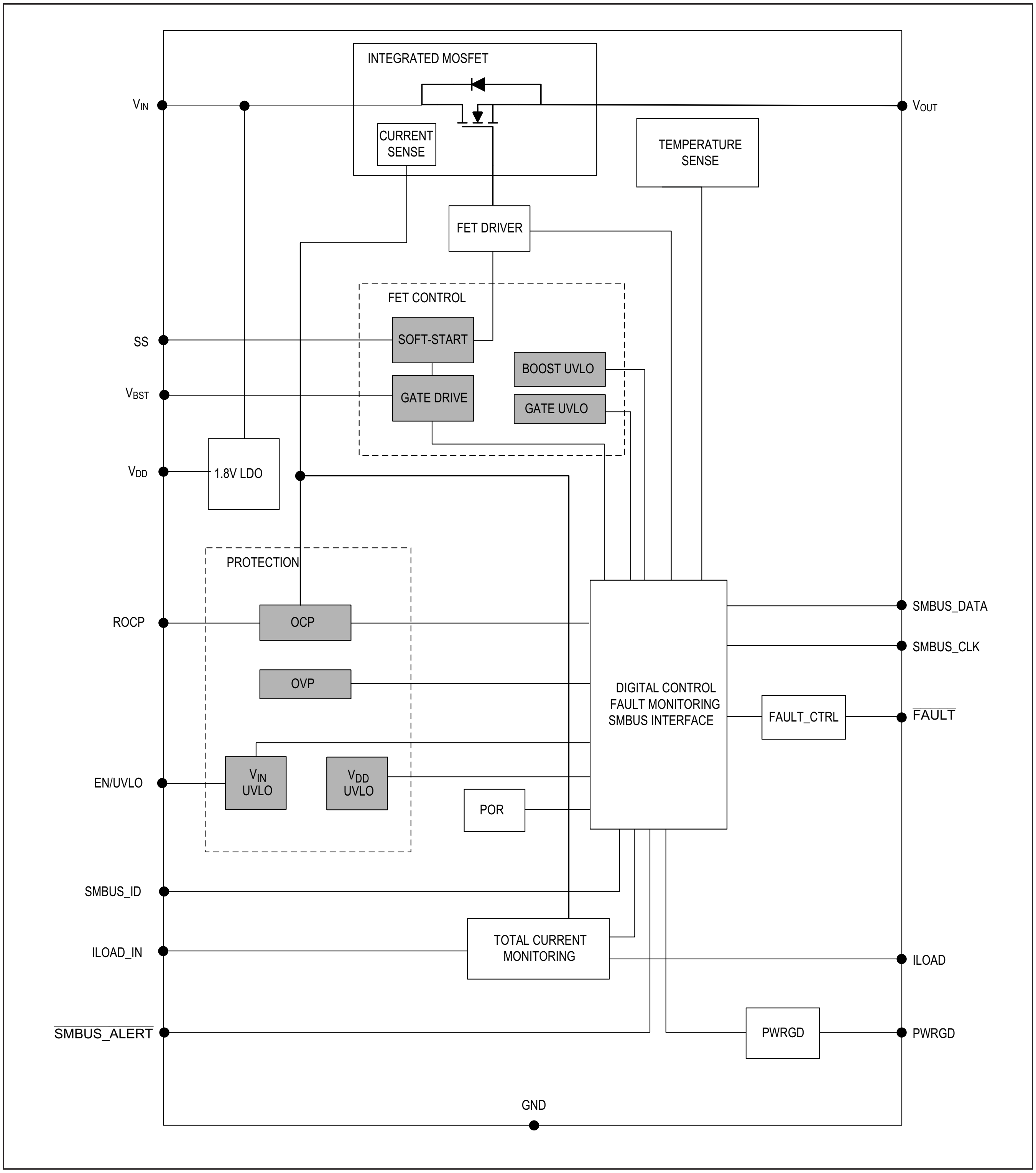
Pin Description

PIN	NAME	FUNCTION
1	SMBUS_CLK	SMBus Clock Pin.
2	ILOAD	Analog Current Representation of the Load Current. Connect the pin to ground through a properly sized resistor for proper voltage representation. Always keep this pin connected to ground through a resistor. A capacitor parallel to the R_{ILOAD} resistor is required; see Table 16 for the recommended value.
3	SS	Soft-Start Pin. A capacitor is connected from SS to GND to program soft-start. The soft-start program capacitor should not exceed 75nF. If a fast load transient (di/dt > 2.5A/ms) resulting in fast and large transient output-voltage deviation is possible in the application, an additional capacitor between SS and V_{OUT} is recommended to keep the pass FET V_{GS} above its UVLO threshold.
4	V_{BST}	Charge-Pump Supply for Pass FET Gate Drive. Connect this node to V_{OUT} through a 220nF bypass capacitor. This supply is designed to be used by the MAX16550/MAX16551 only. No additional load or external components other than a bypass capacitor are allowed on the V_{BST} pin.
5-6	V_{OUT}	12V Output Power Pins (Load Side).

MAX16550/MAX16551 Connection Information (continued)

PIN	NAME	FUNCTION
7-8	V_{IN}	12V Input Power Pins (Power Supply Side).
9	GND	IC Ground. Connect this node to GND plane through vias for proper operation.
10	EN/UVLO	12V Input Voltage and UVLO Pin. Normally connected to the center node of a resistor-divider connected from V_{IN} to ground. A properly sized capacitor can be placed in parallel to the bottom resistor of the resistor-divider for additional filtering. In addition to 12V UVLO programming, this node can be used to enable/disable the MAX16550/MAX16551.
11	$\overline{\text{SMBUS\_ALERT}}$	SMBus Alert, Open-Drain, Active-Low Pin.
12	$\overline{\text{FAULT}}$	Fault Communication, Bidirectional Pin. It is used to indicate/receive detection of latching fault. See the *$\overline{\text{FAULT}}$ Reporting* section for more details. Connect this pin to the system bias supply rail through a 10kΩ resistor. 5V compliant, active-low pin.
13	PWRGD	Power Good Pin. Used to report V_{IN} and V_{OUT} status. See the *Power Good (PWRGD) Output* section for more details. Connect this pin to system bias supply rail through a 10kΩ resistor. This pin is 5V compliant.
14	ROCP	Moderate OCP Threshold Programming Input. Connect this pin to GND using an appropriate programming resistor. See the *Moderate OCP Threshold* section for additional details. No other components are allowed on this pin.
15	SMBUS_DATA	SMBus Data Pin.
16	SMBUS_ID	SMBus Address Programming and Current Hysteresis Flag Pin. Connect this pin to GND through a properly sized resistor to select desired address setting.
17	N.C.	Not Connected. Connect to GND through a 10kΩ resistor.
18	V_{DD}	Internal 1.8V Linear Regulator (LDO) Output. Connect this pin to GND through a 1μF (or higher) capacitor. See Figure 6 for the correct value. No additional loads or components other than external properly sized capacitor are allowed on the V_{DD} pin.

Block Diagram



Detailed Description

The MAX16550/MAX16551 integrated power-protection ICs are designed to provide a complete single-chip 240VA (MAX16551) and circuit-breaker protection solution for the 12V power bus. They combine power monitoring and control functions with a low on-resistance pass FET device that acts as a disconnect switch to limit maximum power distributed to the load. The ICs implement Maxim's proprietary integrated lossless current sensing techniques to provide a highly accurate and compact protection solution. The ICs integrate PMBus/SMBus interface for digital control and monitoring.

Refer to the IC *Block Diagram*. An integrated N-channel power MOSFET is driven by the FET control circuit that includes a boost circuit to provide gate drive. An internal LDO provides V_{DD} IC bias supply, eliminating the need for external bias supply, enabling effective use of the device in hot-swap applications.

Startup

The ICs enable the integrated 1.8V V_{DD} LDO once the 12V supply voltage is high enough to guarantee LDO operation. Once V_{DD} is valid, the ICs read the SMBus_ID programming resistor value to set the PMBus address and initiate. During this period, the gate-drive supply capacitor becomes fully charged. Once these two functions are complete, the ICs can be controlled through the enable input.

The enable input (EN/UVLO) has a precise threshold and provides a V_{IN}_UVLO function, where the enable voltage is derived from V_{IN} through a resistor-divider, with an optional control signal used in conjunction with the divider, as shown in Figure 5. The EN/UVLO pin must not be pulled high externally other than to pull the EN/UVLO pin high through a propely sized resistor-divider from the input supply. Though the enable signal can be pulled low to disable the part, this should only be allowed to occur when the input-voltage supply is within operating range, as specified in the *Electrical Characteristics* table.

Startup Safe Operating Area (SOA)

During soft-start, it is important to keep the FET within its safe operating area. The peak current allowed during startup is shown in Figure 1. In case resistive short is possible in the application, it is required to use startup OCP feature to protect the device. The startup OCP threshold must be programmed to a value lower than safe peak current. Figure 1 assumes pure capacitive or RC load on the output.

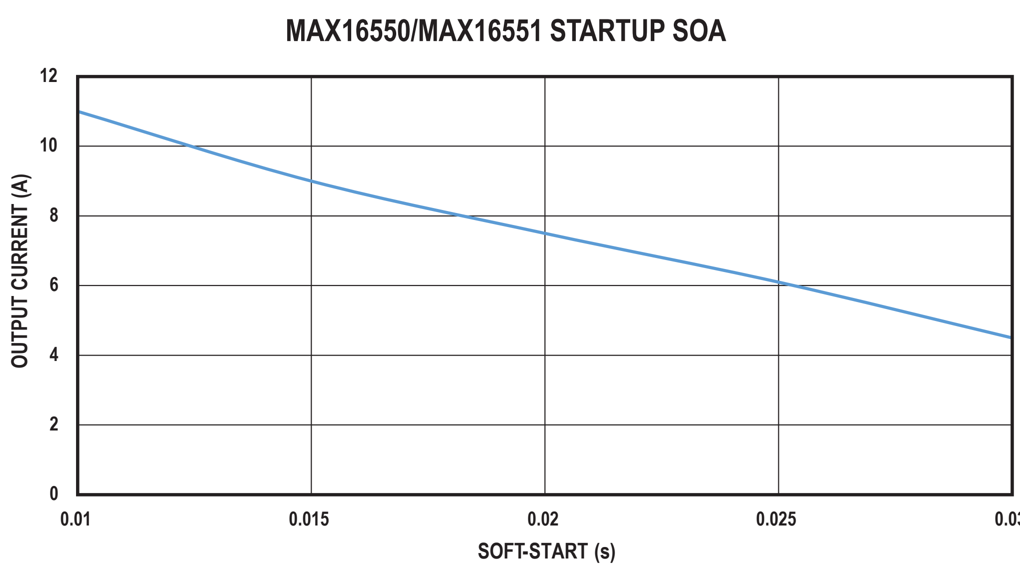


Figure 1. MAX16550/MAX16551 Startup SOA

Self-Check

Once V_{BST_UVLO} has been cleared, the internal V_{DD_LDO} is fully enabled and the EN/UVLO pin is above the enable threshold, the ICs initiate a timed output discharge as a self-check procedure. By default, the ICs initiate this procedure immediately after $V_{BST_}$UVLO has been cleared and the internal $V_{DD_}$LDO is fully enabled. Delay to start this procedure can be reprogrammed through PMBus. If the output does not fall below the programmed $V_{OUT_}$UVLO threshold after a fixed period, the pass FET could potentially be shorted, with the ICs asserting both $\overline{\text{FAULT}}$ and PWRGD pins low. The latched fault condition remains until restart (EN/UVLO or V_{IN} toggling, restarting through the OPERATIONS command). The threshold ($V_{OUT_}$UVLO) for the self-check procedure can be programmed to one of three different values through the PMBus. These values are programmed with the corresponding values for the PWRGD threshold. If the output voltage is below the programmed $V_{OUT_}$UVLO, the self-check is considered passed and the ICs proceed with startup.

In addition, a soft-start capacitor discharge procedure is performed during every restart. The ICs utilize an integrated resistive element, with resistance approximately 1.2kΩ, to discharge the C_{SS} capacitor. The ICs check if the voltage across the C_{SS} capacitor is below the soft-start threshold shown in the *Electrical Characteristics* table after a fixed period of time. If the voltage across the C_{SS} capacitor is not below the softstart threshold, the ICs latch the pass FET off and assert the $\overline{\text{FAULT}}$ pin low. The latched fault condition is kept until reset (EN/UVLO or V_{IN} toggling).

The ICs check the ROCP value at all times, including startup (after the bias supply is valid). This check ensures proper reference OCP threshold selection, which determines startup and severe OCP thresholds. If the wrong ROCP value is detected, the ICs report the fault by asserting the $\overline{\text{FAULT}}$ signal low. The latched fault condition is kept until restart (EN/UVLO or V_{IN} toggling/restarting through the OPERATIONS command).

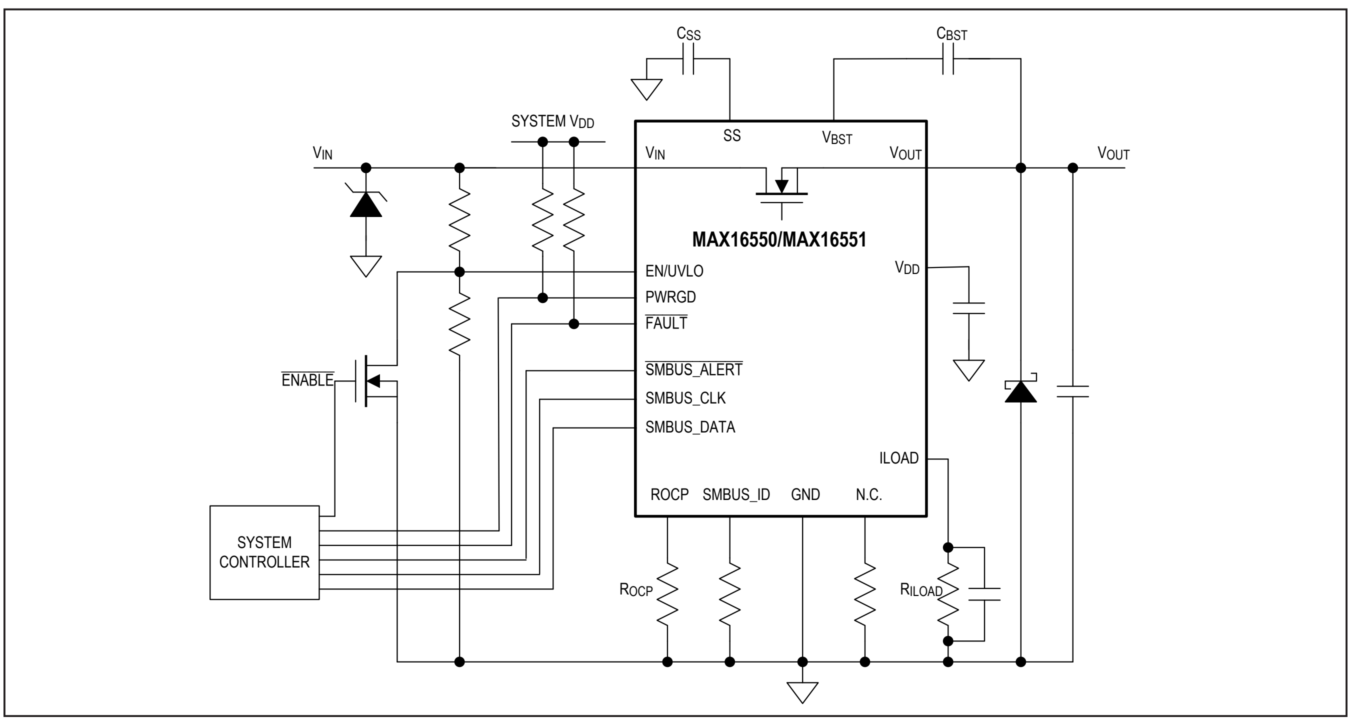


Figure 2. MAX16550/MAX16551 Configuration Example

Soft-Start

Once the self-check procedure is complete, the output-voltage soft-start ramp is initiated. During startup, the C_{SS} capacitor is charged using a constant-current source. Since the integrated FET is configured as a source follower, the output voltage is ramped monotonically at a rate determined by the external soft-start capacitor.

V_{DD} UVLO

The ICs implement V_{DD} UVLO fault monitor and protection. V_{DD} is monitored at all times. Startup procedures are not initiated until V_{DD} UVLO is cleared. If V_{DD} falls below V_{DD} UVLO during normal operation, this fault is latched and V_{IN} power cycle/toggle is required to reset this latching fault.

Current Hysteresis

The SMBUS_ID pin is used as a current-hysteresis flag after SMBUS_ID decoding is completed. If the output current is greater than the MFR_SPECIFIC_HYSTH level, the current-hysteresis flag is set to high. If output current is less than the MFR_SPECIFIC_HYSTL level, then the current-hysteresis flag is set to low.

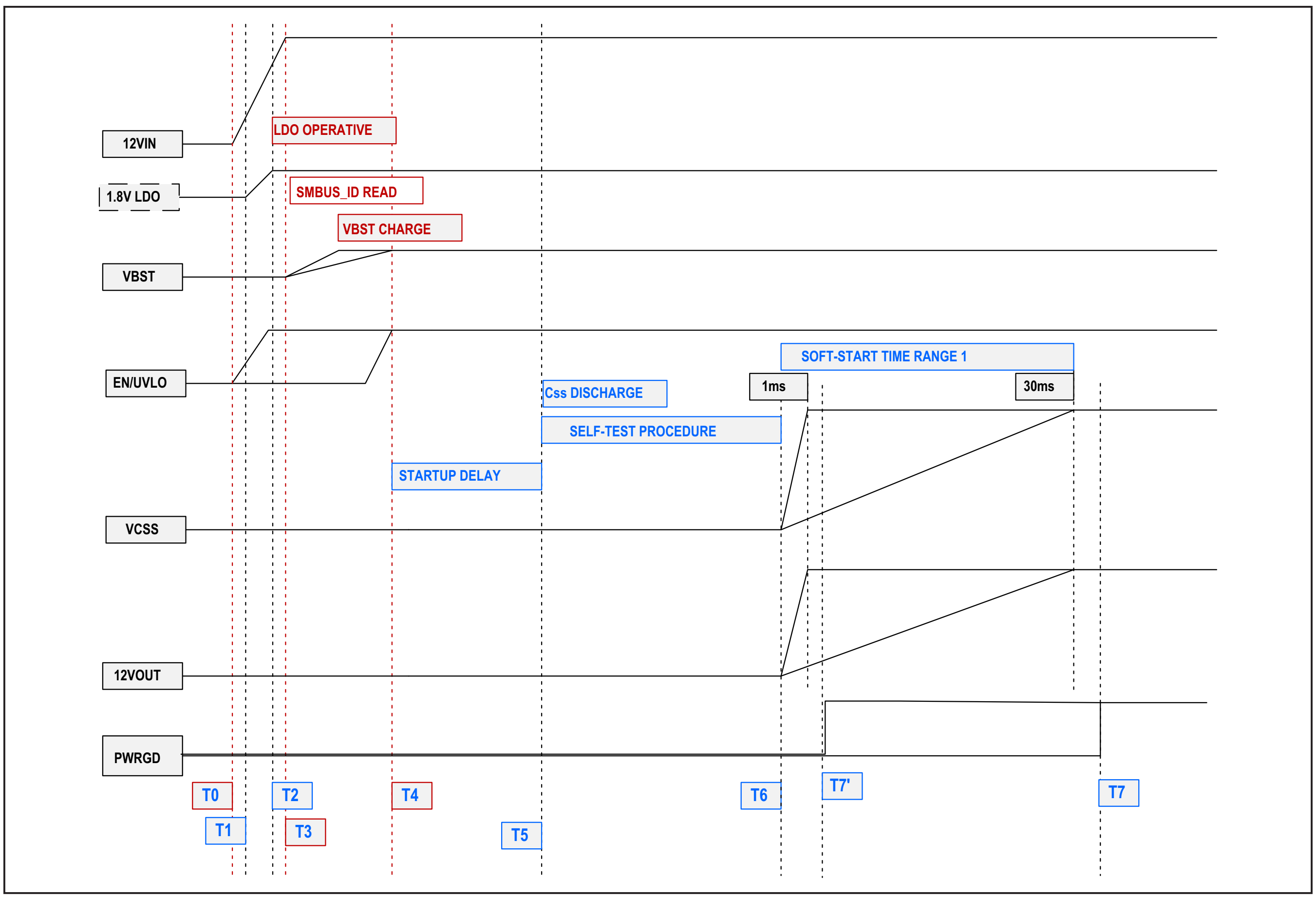


Figure 3. Startup Timing Diagram

Table 1. Timing Diagram Example Shown in Figure 5

POINT/ PERIOD	DESCRIPTION
t0	12V V_{IN} applied.
t1	The LDO has enough headroom to start up. V_{IN} > 2V (typ).
t2	The internal 1.8V LDO is ready and the MAX16550/MAX16551 logic is fully operational. External bypass capacitors connected to the V_{DD} pin are fully charged. 700μs (typ).
t3, t4	SMBus ID resistor reading and V_{BST} charging. EN/UVLO signal status is ignored from t3 to t4. 150μs (typ).
t4	EN/UVLO is active. Startup check-up procedures can be started after the EN/UVLO is cleared.
t4, t5	User-programmable startup delay (0 to 20μs).
t5, t6	Self-test procedure. C_{SS} discharge.
t6, t7	V_{OUT} ramp (1ms–30ms).
t7	Power-good (PWRGD) output asserted. 6ms (typ).
t7+	PWRGD is high, normal operation starts.

SMBus ID Resistor Out of Range

After V_{DD} UVLO is cleared, the SMBus ID programming resistor is read. If it is out of range, a latching fault is tripped. This fault can be cleared by EN/UVLO or V_{IN} toggling or restarting through the OPERATIONS command. The latter may mean pulling EN/UVLO above the threshold and then low after the fault is detected to reset the fault latch. The value is read again when EN/UVLO goes high for the second time.

V_{BOOST}, V_{GS} UVLO

V_{BOOST} UVLO is checked when EN/UVLO is above the enable threshold and remains active while the device is enabled. If V_{BOOST} UVLO is tripped before the FET is turned on, the latching fault can still be reset by EN/UVLO or V_{IN} toggling or restarting through the OPERATIONS command. The gate-drive (V_{GS}) UVLO protection has 10μs internal deglitching filtering, which prevents false tripping due to output-voltage overshoot if a large, fast unloading transient is present. An external capacitance can be placed between the V_{OUT} and V_{SS} pins for filtering. V_{BOOST} and V_{GS} UVLO are latching faults, which result in the pass FET being latched off and $\overline{\text{FAULT}}$ asserted low. V_{GS} UVLO is masked for 100ms during startup to avoid tripping a latching fault.

V_{IN} UVLO

The V_{IN} UVLO is fed through a resistor-divider to the EN/UVLO pin and therefore provides a programmable threshold on the 12V input rail. The EN/UVLO pin includes hysteresis and if the pin falls below the programmed value during operation, the device turns the integrated FET off and PWRGD is deasserted. The integrated FET is turned on again if the positive threshold is exceeded and performs self-test and soft-start for each cycle. V_{IN} UVLO warning is also provided through the PMBus.

Overcurrent Detection (MAX16550)

The MAX16550 actively monitors load current on the 12V power bus load at all times, including startup. Startup OCP is active during startup until the power-good (PWRGD) flag is set. Startup OCP threshold is 8A by default and has much faster reaction time. If, at any time during startup, load current rises above the startup threshold, the integrated pass FET turns off within 10μs and the $\overline{\text{FAULT}}$ pin is asserted low. This is a latching fault.

The MAX16550 provides three levels of overcurrent protection during normal operation (after the startup procedure is complete and the PWRGD flag is set high). The “moderate” OCP threshold is set using an analog external resistor and is therefore programmable over a wide continuous range. This OCP allows a higher current to be sustained for a period less than a programmable timeout period without shutting down the device to allow for short surges that pose no threat to the device and are normal operating conditions. If the load current on the 12V power bus exceeds the moderate OCP threshold for the entire timeout period, but its magnitude is less than a programmable severe overcurrent threshold (Table 3), the integrated pass FET switches off at the end of the timeout period and the $\overline{\text{FAULT}}$ pin is asserted low to indicate a moderate OCP fault condition. Restarting the system requires EN/UVLO or V_{IN} toggling or restarting through the OPERATIONS command. Moderate OCP timeout is user programmable through SMBus, with four different values.

The second level of OCP protection is a “severe OCP.” Severe OCP threshold is programmed relative to moderate OCP threshold using PMBus. If at any time the load current exceeds the severe OCP threshold, the MAX16550 turns the integrated pass FET off in less than 5μs, and asserts the $\overline{\text{FAULT}}$ pin low. Severe overcurrent protection is a latching fault.

The MAX16550 features a third level of protection against severe overload faults, called “safe OCP,” with 60A internally fixed threshold. It assures that the integrated pass FET is protected from exceeding its safe operating condition at all times. If at any time the load current on the 12V power bus exceeds the safe OCP threshold, the MAX16550 turns the pass FET off within 250ns and asserts the $\overline{FAULT}$ pin low. The severe OCP threshold should be set to a value less than the safe OCP threshold.

The MAX16550 supports on-the-fly moderate OCP threshold changes. The concept is shown in Figure 4. If the resistance seen by the ROCP pin is changed during the MAX16550 operation, the MAX16550 adjusts the moderate OCP threshold to match the value selected by the external resistive network.

Overvoltage Protection

The ICs includes V_{IN} overvoltage protection to protect the system from an overvoltage event that could harm the downstream circuitry. Overvoltage protection is disabled by default and can be enabled and programmed through PMBus. The input voltage is constantly monitored, and if at any time it rises above the PMBus programmed threshold, the pass FET is latched off, $\overline{FAULT}$ asserted low, and a fault reported. This is a latching fault.

240VA Protection (MAX16551)

The MAX16551 actively monitors power delivered to the load with default limit set to 240VA. The IEC-compliant system requires that the energy level in operator access areas should never exceed 240VA. This requirement is easily met using the MAX16551 protection IC.

If delivered power exceeds the 240VA threshold, the MAX16551 initiates a 240VA fault timer with PMBus programmable timeout. There are three timeout options: 4ms, 100ms, and 250ms. If power drawn by the load exceeds the 240VA threshold for the entire timeout period, but its magnitude is less than a programmable severe OCP threshold (described in the next section), the integrated pass FET is switched off at the end of the timeout period and $\overline{FAULT}$ asserted low to indicate a 240VA fault condition. Restarting the system after a 240VA fault requires EN/UVLO or V_{IN} toggling or restarting through the OPERATIONS command.

The 240VA protection threshold and timeout are programmed using PMBus registers F5h and D0h. See the *Configuration* section for more details.

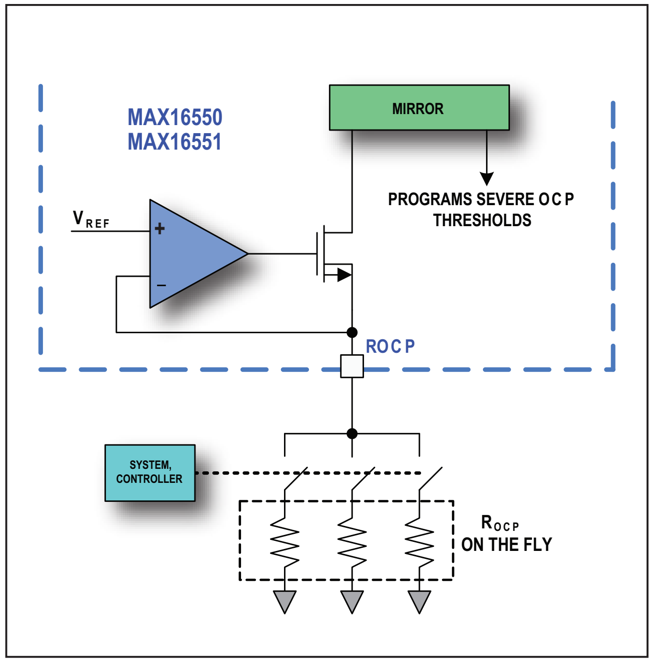


Figure 4. On-The-Fly Analog Programmable Reference OCP Threshold (MAX16551) or Moderate OCP Threshold (MAX16550)

Overcurrent Detection (MAX16551)

The MAX16551 actively monitors load current on 12V power bus, in addition to monitoring the delivered power. There are three levels of overcurrent protection, which are set independent of 240VA protection described in the previous section. The startup OCP is active during startup; severe and safe OCP are active during normal operation (after the startup procedure is complete and the PWRGD flag is set high). The startup and severe OCP thresholds are programmed relative to reference OCP threshold, set by the ROCP resistor.

The startup OCP threshold is active during startup and can be programmed by PMBus to one of four options. If, at any time during startup, load current rises above the startup threshold, the integrated pass FET is turned off and the $\overline{FAULT}$ pin asserted low. This is a latching fault.

Severe OCP threshold is active during normal operation and is programmed through PMBus relative to the reference OCP threshold. There are two options available for severe OCP threshold. Programmable timeout is supported for the severe OCP and is disabled by default. If at any time the load current exceeds the severe OCP threshold and the timeout is disabled, the MAX16551 turns the integrated pass FET off in less than 500ns, and asserts $\overline{\text{FAULT}}$ low. If timeout is enabled, the MAX16551 tolerates current exceeding the severe OCP threshold for the duration of the timeout. If the current is still higher than the severe OCP threshold by the end of the timeout, the MAX16551 turns off and asserts $\overline{\text{FAULT}}$ low. Severe overcurrent protection is a latching fault.

The MAX16551 features another level of protection against severe overload faults, called “safe OCP” with a 60A internally fixed threshold. It assures that the integrated pass FET is protected from exceeding its safe operating condition at all times. If at any time the load current on 12V power bus exceeds the safe OCP threshold, the MAX16551 turns the pass FET off within 250ns and asserts $\overline{\text{FAULT}}$ low. The severe OCP threshold should be set to a value less than the safe OCP threshold.

The MAX16551 supports “on-the-fly” reference-OCP threshold changes, which affects startup and severe OCP thresholds. This concept is shown in Figure 4. If the resistance seen by the ROCP pin is changed during the operation of the ICs, they adjust the reference OCP threshold, matching the value selected by the external resistive network.

Wrong ROCP Protection

The ICs are protected against out-of-range ROCP values. Protection is enabled at all operating conditions, including startup. Wrong ROCP is considered a severe, latching fault, so if at any time the ROCP value is detected out of the permitted range, the ICs latch the integrated FET off, and assert the $\overline{\text{FAULT}}$ pin low. An EN/UVLO or V_{IN} toggling or a restart through the OPERATIONS command must be performed to clear the fault and restart the ICs. If ROCP is changed during operation by the system (see Figure 4), the design must be such that ROCP is within range at all times.

Table 2. Faults Detected and Actions

PARAMETER	DESCRIPTION	$\overline{\text{FAULT}}$ ASSERTED	LATCHING
V_{DD} UVLO	Internal V_{DD} LDO UVLO	N/A*	N/A*
V_{BOOST} UVLO	UVLO for V_{BOOST} voltage	Yes	Yes
V_{GS} UVLO	UVLO for V_{GS} voltage	Yes	Yes
V_{IN} UVLO	EN/UVLO pin below threshold	No	No
R_{OCP}	R_{OCP} detected as being out of valid range	Yes	Yes
R_SMBus_ID	SMBus_ID resistor detected as being out of range	Yes	Yes
C_{SS} Discharge	Soft-start capacitor discharge failed	Yes	Yes
FET Short	Pass FET short detected during startup self-check	Yes	Yes
Startup OCP	Startup overcurrent fault detected	Yes	Yes
Severe OCP	Severe overcurrent fault detected	Yes	Yes
Safe OCP	Safe overcurrent fault detected	Yes	Yes
Power Fault	Power fault detected	Yes	Yes
OTP	Overtemperature-fault threshold exceeded	Yes	Yes
V_{IN} OVP	V_{IN} overvoltage detected	Yes	Yes

Note 1: *If V_{BST}_UVLO fault occurs before startup, $\overline{\text{FAULT}}$ is not reported and status registers are not updated.*

Note 2: *V_{IN} _UVLO clears $\overline{\text{FAULT}}$ and the latching event.*

Overtemperature Protection

The ICs include protection against overtemperature conditions. If the junction temperature exceeds the programmable threshold, the IC latches the integrated FET off and asserts the $\overline{\text{FAULT}}$ output low. To re-enable the IC, the following options are available:

- Toggling EN/UVLO or V_{IN}
- Restarting through the OPERATIONS command

The overtemperature threshold is user programmable through the PMBus.

$\overline{\text{FAULT}}$ Fault Reporting

The ICs provide a dedicated pin ($\overline{\text{FAULT}}$) for fault reporting. If at any time a latching fault is detected, the $\overline{\text{FAULT}}$ pin is immediately latched low. An EN/UVLO or V_{IN} toggling or restart through the OPERATIONS command is required to reset the ICs after a latching-fault detection.

Fault Input and $\overline{\text{FAULT}}$ Pullup

The $\overline{\text{FAULT}}$ pin is a bidirectional open-drain pin that can be used for fault communication from external circuitry to the ICs. To communicate a fault to the ICs, the external circuitry must pull the $\overline{\text{FAULT}}$ pin low. If $\overline{\text{FAULT}}$ is externally pulled low, the ICs treat it as a latching fault; therefore, the pullup voltage source must be considered to ensure the rail is operational and pulled high before the ICs' startup cycle.

These are the options for the pullup rail:

- MAX16550/MAX16551 V_{DD}: 1.8V internal LDO rail. This rail is limited to 1.8V, so the external system has to be compliant with that rail.
- System 3.3V or 5V Rail: FAULT is 5V compliant; therefore, an external higher voltage rail can be used for pullup. This rail has to be stable when the ICs are initiating their startup procedure. If it is not, a potential false-fault communication may occur.

Power-Good (PWRGD) Output

The ICs provide a dedicated pin for power-good reporting (PWRGD). PWRGD is asserted high after startup, when the output node is charged above the programmed PWRGD threshold and the FET is fully enhanced and operating in its resistive region. In all the other conditions, the PWRGD pin is deasserted low.

PWRGD is an open-drain pin; thus, an external pullup resistor connected to the pullup supply rail is needed. Different options are available for the pullup rail:

- MAX16550/MAX16551 V_{DD}: 1.8V internal LDO rail. This rail is limited to1.8V, so the external system has to be compliant with that rail.
- System 3.3V or 5V Rail:. PWRGD is 5V compliant; therefore, an external higher voltage rail can be used for pullup.

Table 3. Requirements for PWRGD Assertion

PARAMETER	CONDITION
V_{OUT}	V_{OUT} > PWRGD Threshold
V_{IN}	$V_{IN} > V_{IN\_UVLO}$
Self-Check	MOSFET (V_{IN} to V_{OUT}) short not detected during startup.
V_{GS}	FET on and in triode region. 5ms delay before PWRGD assertion after this condition is met.

Table 4. PMBus/SMBus Reporting

PARAMETER	CONDITION
V_{IN}	Input voltage (PMBus compliant)
I_{OUT}	Output current (PMBus compliant)
P_{IN}	Input power (PMBus compliant)
E_{IN}	Input energy (PMBus compliant)
Temperature	MAX16550/MAX16551 chip temperature (PMBus compliant)
Peak V_{IN}	Peak value of input voltage (direct reading)
Peak I_{OUT}	Peak value of output current (direct reading)
Peak P_{IN}	Peak value of input power (direct reading)
Peak Temperature	Peak value of IC temperature (direct reading)
Peak V_{OUT}	Peak value of output voltage (direct reading)

Table 5. MAX16550/MAX16551 Programmability

PARAMETER	PROGRAMMABILITY TYPE	COMPONENT	CONDITION
Reference (MAX16551)/ Moderate (MAX16550) OCP Threshold (sets reference/moderate and severe OCP)	Analog	ROCP	R_OCP
Soft-Start Ramp Rate	Analog	C_{SS}	SS
Input UVLO Threshold	Analog	Divider	EN/UVLO
PMBus Address	Programming Resistor	SMBus_ID Resistor	SMBus_ID
Power Fault Timeout	Digital	PMBus_Reg D0h[6:5]	SMB_DATA
Severe OCP Threshold	Digital	PMBus_Reg D0h[7]	SMB_DATA
Startup Delay	Digital	PMBus_Reg D0h[12:11]	SMB_DATA
Input OVP Threshold (OVP feature can be enabled/disabled)	Digital	PMBus_Reg D0h[3:2]	SMB_DATA
Output PWRGD Threshold (sets V_{OUT} UVLO and self-test thresholds)	Digital	PMBus_Reg D0h[9:8]	SMB_DATA
Self-Check Threshold	Digital	PMBus_Reg D0h[9:8]	SMB_DATA
Overtemperature Warning and Fault Thresholds	Digital	PMBus_Reg 51h, PMBus_Reg 4Fh	SMB_DATA
Input Overpower Warning Threshold and Fault Thresholds	Digital	PMBus_Reg 6Bh, PMBus_Reg F5h	SMB_DATA
Reporting and Warning Averaging Sample Size	Digital	PMBus_Reg DDh[3:0], PMBus_Reg D0h[1:0]	SMB_DATA
V_{IN} Undervoltage Warning and Fault Thresholds	Digital	PMBus_Reg 58h, PMBus_Reg 59h	SMB_DATA
Overcurrent Warning	Digital	PMBus_Reg 4Ah	SMB_DATA
V_{OUT} Undervoltage Warning Threshold	Digital	PMBus_Reg 43h	SMB_DATA
ILOAD Voltage Gain	Analog	ILOAD Resistor	ILOAD

Analog Load Current Signal Output

The ICs include an output pin (ILOAD) that allows the user to monitor the load current through the ICs. The current sourced by the ILOAD pin is proportional to the current through the device with the ratio shown in the *Electrical Characteristics* table. A properly sized resistor between the ILOAD pin and GND should be added. The ICs report zero current on the ILOAD pin during soft-start, and start reporting load current once the pass FET V_{GS} is above its UVLO threshold (i.e., the pass FET is in its resistive region).

PMBus/SMBus Reporting and Warning

The ICs provide PMBus-compliant digital telemetry through the PMBus, as shown in Table 4. The ICs include a digital multiply function that provides a reading for input power and input energy. For average values, the sample size is programmable. Peak values for input/output voltage, output current, input power, and temperature are stored in dedicated manufacturer-specific registers. The ICs also provide warning functions based on programmable warning thresholds, as specified in the PMBus specification. The sample size for warning flags is also programmable.

Configuration

The ICs are configured using both analog programming resistors and also through the PMBus. See Table 5 for programmable parameters.

Reference OCP Threshold (MAX16551)

The reference OCP threshold is externally programmable through a resistor connected to the ROCP pin. This threshold is used as reference for startup and severe OCP thresholds. The reference OCP threshold is programmed as shown in Equations 1 and 2 (see the *Electrical Characteristics* table for V_{OCPM} and G_{OCP}).

Equation 1:

$$I_{OCP\_REF} = \frac{V_{OCPM}}{ROCP} \times GOCP$$

where:

I_{OCP_REF} = Reference overcurrent-protection threshold (A)

V_{OCPM} = Overcurrent-rotection reference voltage shown in the *Electrical Characteristics* table (V)

GOCP = Overcurrent protection gain shown in the *Electrical Characteristics* table (µA/A)

R_{OCP} = Value of overcurrent-protection programming resistor (Ω)

Equation 2:

$$R_{OCP} = \frac{V_{OCPM}}{I_{OCP\_REF}} \times GOCP$$

where:

I_{OCP_REF} = Reference overcurrent-protection threshold (A)

V_{OCPM} = Overcurrent-protection reference voltage shown in the *Electrical Characteristics* table (V)

GOCP = Overcurrent-protection gain shown in the *Electrical Characteristics* table (A/A).

R_{OCP} = Value of overcurrent-protection programming resistor (Ω)

Design Example (MAX16551):

To set reference OCP to 20A nominal, using Equation 2:

$$R_{OCP} = \frac{0.8\,V}{20\,A} \times (4 \times 10^6)$$
$$= 160\,k\Omega$$

Design Example (MAX16550):

To set moderate OCP to 35A nominal, using Equation 2:

$$R_{OCP} = \frac{0.8\,V}{35\,A} \times (4 \times 10^6)$$
$$= 91.5\,k\Omega$$

Startup OCP Threshold

PMBus register DDh is used to set startup OCP threshold. See Table 14 for Reg_DDh settings.

Design Example:

To set Startup OCP to 4A, write 10b to bits Reg_DDh[5:4].

Power-Fault Threshold (MAX16551)

The input power-fault protection threshold is set to 240VA by default. If needed, it's possible to program it by changing the Reg_F5h. Equation 4 should be used to calculate the value to be written to Reg_F5h.

Equation 4:

$$P_{IN\_OP} = \frac{[X \times 111.45]}{R_{ILOAD}}$$

where:

P_{IN_OP} = Desired P_{IN_OP} threshold (VA)
R_{ILOAD} = External current reporting resistor (kΩ)
V_{IN_MAX} = Maximum input supply voltage (V)
X = Reg_F5h value

Soft-Start Capacitor (C_{SS})

During startup, the pass FET device is operated as a source follower. Soft-start capacitor C_{SS} is connected between the MOSFET's gate and ground and is charged from a fixed current source. The external C_{SS} capacitor therefore charges linearly and this produces a linear monotonic ramp for V_{OUT}. The ramp rate is programmable by selecting the appropriate value for C_{SS}.

The ramp rate for the voltage across C_{SS} and V_{OUT} is given by Equation 5.

Equation 5:

$$\frac{dV}{dt} = \frac{i_{SS}}{C_{SS}}$$

where:

dV/dt = Voltage ramp rate of V_{OUT} (V/μs)

i_{SS} = Soft-start current source (mA)

C_{SS} = External C_{SS} capacitor value (nF)

Assuming V_{IN} = 12V, Equation 5 can be used to derive the soft-start time given by Equation 6.

Equation 6:

$$t_{SS} = \frac{12V \times C_{SS}}{i_{SS}}$$

where:

t_{SS} = Ramp duration (μs)

i_{SS} = Soft-start current (mA)

C_{SS} = External soft-start capacitor value (nF)

Assuming the load inrush current is due to the input capacitance only, the load current is given by Equations 7 and 8.

Equation 7:

$$I_{IN} = I_{OUT} = C_{OUT} \text{ x } \frac{dV}{dt}$$

where:

I_{OUT} = Load inrush current(A)

C_{OUT} = Load capacitance (μF)

Equation 8:

$$I_{IN} = I_{OUT} = \frac{C_{OUT} \text{ x } i_{SS}}{C_{SS}}$$

where:

I_{OUT} = Load inrush current(A)

C_{OUT} = Load capacitance (μF)

C_{SS} = External soft-start capacitor value (nF)

i_{SS} = Soft-start current (mA)

Therefore, the soft-start capacitor can be selected based on the design value of inrush current using Equation 9.

Equation 9:

$$C_{SS} = \frac{C_{OUT} \text{ x } i_{SS}}{I_{INRUSH}}$$

where:

I_{INRUSH} = Desired maximum inrush current due to C_{LOAD} (A)

C_{OUT} = Load capacitance (mF)

C_{SS} = External soft-start capacitor value (nF)

i_{SS} = MAX16550/MAX16551 soft-start current (μA)

In order to achieve optimal low-loss operation of the pass FET, the ICs monitor the value of the pass FET V_{GS}. The V_{GS} UVLO is enabled approximately 100ms (according to the *Electrical Characteristics* table) after startup initiation. This places an upper limit on C_{SS} and t_{SS}.

Note that if load unloading transients with di/dt > 2.5A/ms large enough to cause output-voltage transients > ~100mV, an additional capacitor between SS and V_{OUT} is recommended to ensure the pass FET V_{GS} remains above its UVLO threshold. This capacitor has no noticeable effect on soft-start ramp time as the differential voltage from V_{OUT} to SS remains approximately constant in soft-start.

Design Example:

Assume a maximum design value for inrush current of 10A, and a load capacitance of 2mF.

$$C_{SS} = \frac{(2mF) \text{ x } (30\mu A)}{10A}$$
$$= 6nF \text{ minimum (to meet inrush maximum)}$$

Use Equation 6 to show that corresponding t_{SS} in this example is 2.4ms, which is well below the 100ms limit.

Input UVLO

The input UVLO is set using a resistor-divider circuit, as shown in Figure 5. The enable threshold, V_{IN_UVLO} is given in the *Electrical Characteristics* table. The corresponding value for the V_{IN} rail is given by Equation 10.

Equation 10:

$$V_{IN} = \frac{V_{IN\_UVLO}}{K}$$

or

Equation 11:

$$K = \frac{(V_{IN\_UVLO})}{V_{IN}}$$

where:

V_{IN} = 12V rail input voltage to enable device (V)

V_{IN_UVLO} = EN/UVLO threshold (V)

K = Resistor-divider rato, R2/(R1 + R2)

Design Example:

To guarantee system startup at 10.8V using Equation 11.

$$K = \frac{1.0V}{10.8V}$$
$$= 0.926$$
$$\text{set } R2 = 10k\Omega$$
$$R1 = 98k\Omega$$

PMBus Address Programming

The PMBus address is programmed to one of 16 values using the external resistor, as shown in Table 6.

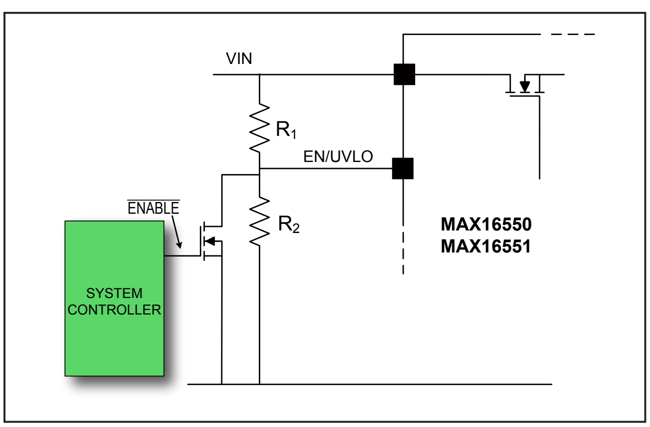


Figure 5. Programming Resistors for Input UVLO

Table 6. PMBus Address Programming Resistor Values

VALUE	R_SMBUS_ID (kΩ)	SMBus ID
0	1.78	40h
1	2.37	41h
2	3.16	42h
3	4.22	43h
4	5.62	44h
5	7.5	45h
6	9.76	46h
7	13	47h
8	17.4	10h
9	23.2	11h
10	30.9	12h
11	41.2	13h
12	54.9	50h
13	73.2	51h
14	97.6	52h
15	127	53h

Note: RSMBus_ID should be 1% or better.

Table 7. Parameters Programmed through PMBus and Default Values

PARAMETER	DEFAULT VALUE
Overtemperature-Protection Threshold	140°C
V_{OUT} PWRGD/Self-Check Thresholds	11V/9V
240VA OCP Timeout/ Moderate OCP Timeout	4ms (MAX16551)/ 100µs (MAX16550)
Startup Delay	0µs
Startup OCP Threshold	8A
Severe OCP Threshold	130%
Input OVP Threshold	14V (Disabled by Default)
Overtemperature Warning Threshold	220°C (Disabled by Default)
Pin Warning Threshold	(Disabled by Default)
Overcurrent Warning	(Disabled by Default)
V_{IN} Undervoltage Warning	(Disabled by Default)
V_{OUT} Undervoltage Warning	(Disabled by Default)
Current Hysteresis	(Disabled by Default)

ILOAD Reporting

The current-reporting voltage is set using an external resistor connected from ILOAD to ground. The maximum voltage is shown in the *Electrical Characteristics* table. The reporting voltage gain is given by Equation 12. Assuming a maximum signal voltage of 1.35V, Equation 14 can be used to select a value for R_{ILOAD} based on a desired full-scale current.

Equation 12:

$$V_{ILOAD} = R_{ILOAD} \times I_{LOAD} \times G_{ILOAD}$$

Equation 13:

$$R_{ILOAD} = \frac{1.35\,V}{I_{LOAD\_FSD} \times G_{ILOAD}}$$

where:

V_{ILOAD} = Current-reporting voltage (V)

R_{ILOAD} = External current-reporting resistor (kΩ)

I_{LOAD} = Load current I_{OUT} = I_{IN} (A)

I_{LOAD_FSD} = Desired full-scale of current reporting (A)

G_{ILOAD} = Current-reporting gain from the *Electrical Characteristics* table

For example, to set the full-scale current reported to 23A:

$$RILOAD = \frac{1.35V}{23A \times \left(5 \times 10^{-6}\right)} = 11.8K\Omega$$

MAX16550/MAX16551 PMBus Reporting and Warning Settings

The ICs provide single-sample, averaged and peak values for voltage, current, and power reporting, as well as single reading or averaged readings for warnings. The limits for these parameters and warnings should be set through PMBus prior to operation if a value other than the default is required.

Averaging for voltage, power, and current uses a "accumulate-and-dump" technique, whereas temperature uses a shifting window/rolling average. Power is calculated for every voltage and current sample (as opposed to using averaged voltage and current), and the result is accumulated in a dedicated register for averaging.

Two independently programmable averaging sample sizes are used for reporting and warning/status register use for voltage, current and power:

- Reporting: 2^N samples, with N = 0 to 16 (1 sample to 32K samples)
  - Sample size is set using Reg_DDh (CONFIG_2, manufacturer-specific register)
- Warning: 2^M samples, with M = 0 to 3 (1 sample to 8 samples)
  - Sample size is set using Reg D0h (CONFIG, manufacturer-specific register)

The ICs support fault and status reporting except for V_{BST}_UVLO fault at startup. If the V_{BST}_UVLO occurs at startup the device latches off, $\overline{FAULT}$ is not reported, and status registers are not updated.

Setting PMBus-Programmable Parameters

See Table 7 for parameters that are programmed through the PMBus. If a setting other than the default shown below is required, it must be programmed through PMBus. Note that some parameters have an enable bit as well as value bits.

SMBus/PMBus Registers

STATUS_MFR_SPECIFIC Register (80h)

This is a single-byte register used to read the status of the self-check and fault indicators.

ALERT Behavior

Any of the STATUS bits (with some exception) assert the alert line low.

Exceptions are:

- Bit OFF of STATUS_BYTE/STATUS_WORD
- Bit POWERGOOD#/MFR_SPECIFIC of STATUS_WORD

Alert line can be configured to mask any of the STATUS bits using the SMBALERT_MASK register.

The only ways to release the alert line are:

- CLEAR_FAULTS command
- ARA (refer to the SMBus spec v2.0)

The MFR_DATE register returns a byte from which it's possible to recover the manufacture date (monthly) with Table 10.

Table 8. PMBus/SMBus Registers

ADDRESS (HEX)	PROGRAMMABILITY (Note 1)	TYPE	BYTES	DEFAULT (HEX)
1	**OPERATION**	RW	1	80
3	**CLEAR_FAULTS**	WO	0	0
19	**CAPABILITY**	RO	1	B0
1B	**SMBALERT_MASK**	(Note 2)	2	0000
43	**VOUT_UV_WARN_LIMIT**	RW	2	0000
4A	**IOUT_OC_WARN_LIMIT**	RW	2	03FF
4F	**OT_FAULT_LIMIT**	RW	2	0358
51	**OT_WARN_LIMIT**	RW	2	03FF
58	**VIN_UV_WARN_LIMIT**	RW	2	0000
59	**VIN_UV_FAULT_LIMIT**	RW	2	0000
6B	**PIN_OP_WARN_LIMIT**	RW	2	0000
78	**STATUS_BYTE**	RO	1	0
79	**STATUS_WORD**	RO	2	0
7A	**STATUS_VOUT**	RO	1	0
7B	**STATUS_IOUT**	RO	1	0
7C	**STATUS_INPUT**	RO	1	0
7D	**STATUS_TEMPERATURE**	RO	1	0
7E	**STATUS_CML**	RO	1	0
80	**STATUS_MFR_SPECIFIC**	RO	1	0
86	**READ_EIN**	RO	7	0
88	**READ_VIN**	RO	2	0
89	**READ_IIN**	RO	2	0
8B	**READ_VOUT**	RO	2	0
8C	**READ_IOUT**	RO	2	0
8D	**READ_TEMPERATURE**	RO	2	0
97	**READ_PIN**	RO	2	0
98	**PMBUS_REVISION**	RO	1	2
99	**MFR_ID**	BLK	6	MAXIM
9A	**MFR_MODEL**	BLK	6	16550/ 16551
9B	**MFR_REVISION**	BLK	2	1
9D	**MFR_DATE**	RO	1	See Table 10
D0	CONFIG	RW	2	0
D1	PEAK_VIN	RO	2	0
D2	PEAK_IOUT	RO	2	0
D3	PEAK_PIN	RO	2	0
D4	PEAK_TEMP	RO	2	0

Table 8. PMBus/SMBus Registers (continued)

ADDRESS (HEX)	PROGRAMMABILITY (Note 1)	TYPE	BYTES	DEFAULT (HEX)
D5	CLEAR_PEAKS	WO	0	0
DD	CONFIG2	RW	1	0
F2	MFR_SPEC_HYSTL	RW	2	03FF
F3	MFR_SPECT_HYSTH	RW	2	03FF
F4	MFR_SPEC_HYST_STAT	RO	1	0
F5	PIN_OP_FAULT_LIMIT	RW	2	5540
FD	PEAK_VOUT	RO	2	0

Note 1: Registers shown in bold (1h - 9Dh) comply with PMBus Power Management Management Protocol Specifications. Refer to the PMBus specification and see Table 15 for more details.

Note 2: SMBALERT_MASK is written to a write_word command and read with a read from a write_block_read_process_call with a num_bytes field of 1.

Table 9. Register 80h

BIT #	BIT NAME	DESCRIPTION	READING	INDICATION
[7]	SELFCHECK_FAULT	Pass FET and Soft-Start Self-Check	0	Pass
			1	Fail
[6]	ROCP_FAULT	ROCP Check	0	Pass
			1	Fail
[5]	R_SMBUSID_FAULT	SMBus Programming Resistor Check	0	Pass
			1	Fail
[4]	FOLLOWER_FAULT	Fault Input	0	No Fault Input
			1	Fault Input
[3]	GATE_UVLO_FAULT	V_{GS} UVLO Fault	0	No Fault
			1	Fault
[2]	BST_UVLO_FAULT	V_{BOOST} UVLO Fault	0	No Fault
			1	Fault
[1]	—	Not Used	0	—
			1	—
[0]	PIN_OP_FAULT	PIN_OP_FAULT	0	Pass
			1	Fault

Table 10. Lookup Table for MFR_DATE Register 9Dh

MFR_DATE[5:0] BINARY	MONTH	YEAR
000000	Jan	2014
000001	Feb	2014
—	—	—
111101	Feb	2019
111110	Mar	2019
111111	Apr	2019

Table 11. MAX16550/MAX16551 PMBus Register Map

ADDRESS	DEC	NAME	TYPE	WIDTH	DEFAULT	LOW BYTE								HIGH BYTE							
						B7	B6	B5	B4	B3	B2	B1	B0	B15	B14	B13	B12	B11	B10	B9	B8
01	1	OPERATION	RW	1	80	enable	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—
03	3	CLEAR_ FAULTS	WO	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
19	25	CAPABILITY	CN	1	B0	1	0	1	1	0	0	0	0		—	—	—	—	—	—	—
1B	27	SMBALERT_ MASK	**	2	0000	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
43	67	VOUT_UV_ WARN_LIMIT	RW	2	0	vout_uv_w arn_th[7]	vout_uv_w arn_th[6]	vout_uv_w arn_th[5]	vout_uv_w arn_th[4]	vout_uv_w arn_th[3]	vout_uv_w arn_th[2]	vout_uv_w arn_th[1]	vout_uv_w arn_th[0]	0	0	0	0	0	0	vout_uv_w arn_th[9]	vout_uv_w arn_th[8]
4A	74	IOUT_OC_ WARN_LIMIT	RW	2	03FF	ocp_warn_ th[7]	ocp_warn_ th[6]	ocp_warn_ th[5]	ocp_warn_ th[4]	ocp_warn_ th[3]	ocp_warn_ th[2]	ocp_warn_ th[1]	ocp_warn_ th[0]	0	0	0	0	0	0	ocp_warn_ th[9]	ocp_warn_ th[8]
4F	79	OT_FAULT_ LIMIT	RW	2	03FF	ovt_fault _th[7]	ovt_fault _th[6]	ovt_fault _th[5]	ovt_fault_ th[4]	ovt_fault _th[3]	ovt_fault _th[2]	ovt_fault _th[1]	ovt_fault _th[0]	0	0	0	0	0	0	ovt_fault _th[9]	ovt_fault _th[8]
51	81	OT_WARN_ LIMIT	RW	2	03FF	ovt_warn_ th[7]	ovt_warn_ th[6]	ovt_warn_ th[5]	ovt_warn_ th[4]	ovt_warn_ th[3]	ovt_warn_ th[2]	ovt_warn_ th[1]	ovt_warn_ th[0]	0	0	0	0	0	0	ovt_warn_ th[9]	ovt_warn_ th[8]
57	87	VIN_OV_ WARN_LIMIT	RW	2	03FF	ov_ warn_t h[7]	ov_ warn_t h[6]	ov_ warn_t h[5]	ov_ warn_t h[4]	ov_ warn_t h[3]	ov_ warn_t h[2]	ov_warn_t h[1]	ov_ warn_t h[0]	0	0	0	0	0	0	ov_ warn_t h[9]	ov_ warn_t h[8]
58	88	VIN_UV_ WARN_LIMIT	RW	2	03FF	uv_warn_ th[7]	uv_warn_ th[6]	uv_warn_ th[5]	uv_warn_ th[4]	uv_warn_ th[3]	uv_warn_ th[2]	uv_warn_ th[1]	uv_warn_ th[0]	0	0	0	0	0	0	uv_warn_ th[9]	uv_warn_ th[8]
59	89	VIN_UV_ FAULT_LIMIT	RW	2	0	vin_uv_ fault_th[7]	vin_uv_ fault_th[6]	vin_uv_ fault_th[5]	vin_uv_ fault_th[4]	vin_uv_ fault_th[3]	vin_uv_ fault_th[2]	vin_uv_ fault_th[1]	vin_uv_ fault_th[0]	0	0	0	0	0	0	vin_uv_ fault_th[9]	vin_uv_ fault_th[9]
6B	107	PIN_OP_ WARN_LIMIT	RW	2	FFFF	op_warn_ th[7]	op_warn_ th[6]	op_warn_ th[5]	op_warn_ th[4]	op_warn_ th[3]	op_warn_ th[2]	op_warn_ th[1]	op_warn_ th[0]	op_warn_ th[15]	op_warn_ th[14]	op_warn_ th[13]	op_warn_ th[12]	op_warn_ th[11]	op_warn_ th[10]	op_warn_ th[9]	op_warn_ th[8]
78	120	STATUS_ BYTE	RO	1	0	0	OFF	0	IOUT_ OC_ FAULT	VIN_UV_ FAULT	TEMPE- RATURE	CML	NOA	—	—	—	—	—	—	—	—
79	121	STATUS_ WORD	RO	2	0	0	OFF	0	IOUT_ OC_ FAULT	VIN_UV_ FAULT	TEMPE- RATURE	CML	NOA	VOUT	IOUT/ POUT	INPUT	INPUT MFR_ SPECIFIC	POWER GOOD#	0	0	0
7A	122	STATUS_ VOUT	RO	1	0	VOUT_ OV_ FAULT	0	VOUT _UV _WARNIG	0	0	0	0	0	—	—	—	—	—	—	—	—
7B	123	STATUS_ IOUT	RO	1	0	IOUT_ OC_ FAULT	0	IOUT_ OC_ WARNING	0	0	0	0	POUT_ OP_ WARNING	—	—	—	—	—	—	—	—

Table 11. MAX16550/MAX16551 PMBus Register Map (continued)

ADDRESS	DEC	NAME	TYPE	WIDTH	DEFAULT	LOW BYTE								HIGH BYTE							
						B7	B6	B5	B4	B3	B2	B1	B0	B15	B14	B13	B12	B11	B10	B9	B8
7C	124	STATUS_ INPUT	RO	1	0	VIN_ OV _FAULT	0	VIN_ UV_ WARNING	0	0	IIN_ OC_ FAULT	IIN_ OC_ WARNING	PIN_ OP_ WARNING	—	—	—	—	—	—	—	—
7D	125	STATUS _TEMPERATURE	RO	1	0	OT_ FAULT	OT_ WARNING	0	0	0	0	0	0	—	—	—	—	—	—	—	—
7E	126	STATUS_CML	RO	1	0	invalid/un-supported cmd	invalid/un-supported data	PEC Failed	0	0	0	Other communica-tion fault	0	—	—	—	—	—	—	—	—
80	128	STATUS_MFR _SPECIFIC	RO	1	0	SELF CHECK_ FAULT	ROCP_ FAULT	R_SMBUS _ID_ FAULT	R_SMBUS _ID_ FAULT	GATE_ UVLO_ FAULT	BST_ UVLO _FAULT	0	PIN_OP _FLT	—	—	—	—	—	—	—	—
86	134	READ_EIN	BLK	7	0	8'h06	enrgy_ cnt [7:0]	enrgy_ cnt[15:8]	roll_ cnt[7:0]	samp_ cnt[7:0]	samp_ cnt[15:8]	samp_ cnt[23:16]	—	—	—	—	—	—	—	—	—
88	136	READ_VIN	RO	2	0	vadc_ ave[7]	vadc_ ave[6]	vadc_ ave[5]	vadc_ ave[4]	vadc_ ave[3]	vadc_ ave[2]	vadc_ ave[1]	vadc_ ave[0]	0	0	0	0	0	0	vadc_ ave[9]	vadc_ ave[8]
89	137	READ_IIN	RO	2	0	iadc_ ave[7]	iadc_ ave[6]	iadc_ ave[5]	iadc_ ave[4]	iadc_ ave[3]	iadc_ ave[2]	iadc_ ave[1]	iadc_ ave[0]	0	0	0	0	0	0	iadc_ ave[9]	iadc_ ave[8]
8B	139	READ_VOUT	RO	2	0	vadc_ ave[7]	vadc_ ave[6]	vadc_ ave[5]	vadc_ ave[4]	vadc_ ave[3]	vadc_ ave[2]	vadc_ ave[1]	vadc_ ave[0]	0	0	0	0	0	0	vadc_ ave[9]	vadc_ ave[8]
8C	140	READ_IOUT	RO	2	0	iadc_ ave[7]	iadc_ ave[6]	iadc_ ave[5]	iadc_ ave[4]	iadc_ ave[3]	iadc_ ave[2]	iadc_ ave[1]	iadc_ ave[0]	0	0	0	0	0	0	iadc_ ave[9]	iadc_ ave[8]
8D	141	READ_ TEMPERATURE _1	RO	2	0	tadc_ ave[7]	tadc_ ave[6]	tadc_ ave[5]	tadc_ ave[4]	tadc_ ave[3]	tadc_ ave[2]	tadc_ ave[1]	tadc_ ave[0]	0	0	0	0	0	0	tadc_ ave[9]	tadc_ ave[8]
97	151	READ_PIN	RO	2	0	pwr_ calc[7]	S	pwr_ calc[5]	pwr_ calc[4]	pwr_ calc[3]	pwr_ calc[2]	pwr_ calc[1]	pwr_ calc[0]	pwr_ calc[15]	pwr_ calc[14]	pwr_ calc[13]	pwr_ calc[12]	pwr_ calc[11]	pwr_ calc[10]	pwr_ calc[9]	pwr_ calc[8]
98	152	PMBUS_ REVISION	CN	1	22	0	1	0	0	0	0	1	0								
99	153	MFR_ID	BLK	6	0	8'h04	"M"	"A"	"X"	"I"	"M"										
9A	154	MFR_MODEL	BLK	6	0	8'h05	1	6	5	5	0/1										
9B	155	MFR_ REVISION	RO	1	1	0	0	0	0	0	mfr_ rev[2]	mfr_ rev[1]	mfr_ rev[0]								
9D	157	MFR_DATE	RO	1	0	0	MFR_ DT<5>	MFR_ DT<4>	MFR_ DT<3>	MFR_ DT<2>	MFR_ DT<1>	MFR_ DT<0>									

Table 11. MAX16550/MAX16551 PMBus Register Map (continued)

ADDRESS	DEC	NAME	TYPE	WIDTH	DEFAULT	LOW BYTE								HIGH BYTE							
						B7	B6	B5	B4	B3	B2	B1	B0	B15	B14	B13	B12	B11	B10	B9	B8
D0	208	CONFIG	RW	2	0	ocp_cfg	mocp_cfg[1]	mocp_cfg[0]	enable_ovp	ovp_th[1]	ovp_th[0]	num_aves_alert[1]	num_aves_alert[0]	ocp_severe_filter[1]	ocp_severe_filter[0]	disable_iadc	ss_cfg[1]	ss_cfg[0]	0	pwrgd_cfg[1]	pwrgd_cfg[0]
D1	209	PEAK_VIN	RO	2	0	vadc_peak[7]	vadc_peak[6]	vadc_peak[5]	vadc_peak[4]	vadc_peak[3]	vadc_peak[2]	vadc_peak[1]	vadc_peak[0]	0	0	0	0	0	0	vadc_peak[9]	vadc_peak[8]
D2	210	PEAK_IOUT	RO	2	0	iadc_peak[7]	iadc_peak[6]	iadc_peak[5]	iadc_peak[4]	iadc_peak[3]	iadc_peak[2]	iadc_peak[1]	iadc_peak[0]	0	0	0	0	0	0	iadc_peak[9]	iadc_peak[8]
D3	211	PEAK_PIN	RO	2	0	pwr_peak[7]	pwr_peak[6]	pwr_peak[5]	pwr_peak[4]	pwr_peak[3]	pwr_peak[2]	pwr_peak[1]	pwr_peak[0]	pwr_peak[15]	pwr_peak[14]	pwr_peak[13]	pwr_peak[12]	pwr_peak[11]	pwr_peak[10]	pwr_peak[9]	pwr_peak[8]
D4	212	PEAK_TEMP	RO	2	0	tadc_peak[7]	tadc_peak[6]	tadc_peak[5]	tadc_peak[4]	tadc_peak[3]	tadc_peak[2]	tadc_peak[1]	tadc_peak[0]	0	0	0	0	0	0	tadc_peak[9]	tadc_peak[8]
D5	213	CLEAR_PEAKS	WO	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
D8	216	TRANS0	RO	1	0	0	trans0[6]	trans0[5]	trans0[4]	trans0[3]	trans0[2]	trans0[1]	trans0[0]	—	—	—	—	—	—	—	—
D9	217	TRANS1	RO	1	0	0	trans1[6]	trans1[5]	trans1[4]	trans1[3]	trans1[2]	trans1[1]	trans1[0]	—	—	—	—	—	—	—	—
DA	218	TRANS2	RO	1	0	0	trans2[6]	trans2[5]	trans2[4]	trans2[3]	trans2[2]	trans2[1]	trans2[0]								
DB	219	TRANS3	RO	1	0	0	trans3[6]	trans3[5]	trans3[4]	trans2[3]	trans3[2]	trans3[1]	trans3[0]								
DC	220	TRANS4	RO	1	0	0	trans4[6]	trans4[5]	trans4[4]	trans2[3]	trans4[2]	trans4[1]	trans4[0]								
DD	221	CONFIG_2	RW	2	0	0	0	0	0	num_aves_reporting [3]	num_aves_reporting [2]	num_aves_reporting [1]	num_aves_reporting [0]								
F2	242	MFR_SPECIFIC_HYST_L	RW	2	03FF	hystl[7]	hystl[6]	hystl[5]	hystl[4]	hystl[3]	hystl[2]	hystl[1]	hystl[0]							hystl[9]	hystl[8]
F3	243	MFR_SPECIFIC_HYST_H	RW	2	03FF	hystl[7]	hystl[6]	hystl[5]	hystl[4]	hystl[3]	hystl[2]	hystl[1]	hystl[0]							hystl[9]	hystl[8]
F4	244	MFR_SPECIFIC_HYST_STATUS	RO	1	0	0	0	0	0	Iout > oc_warn_limit	HYST pin status	HYST > reg_F3	HYST > reg_F2								
F5	245	PIN_OP_FAULT_LIMIT	RW	2	5540	pin_op_flt<7>	pin_op_flt<6>	pin_op_flt<5>	pin_op_flt<4>	pin_op_flt<3>	pin_op_flt<2>	pin_op_flt<1>	pin_op_flt<0>					pin_op_flt<11>	pin_op_flt<10>	pin_op_flt<9>	pin_op_flt<8>
FD	253	PEAK_VOUT	RO	2	0	vout_peak[7]	vout_peak[6]	vout_peak[5]	vout_peak[4]	vout_peak[3]	vout_peak[2]	vout_peak[1]	vout_peak[0]	0	0	0	0	0	0	vout_peak[9]	vout_peak[8]

CONFIG Register (D0h)

This is a 2-byte register used to configure the MAX16550/MAX16551 ICs. The default value is 0000h. The meaning of the bits of this register are shown in Table 12.

CONFIG_2 Register (DDh)

This single-byte register allows the selection of the number of samples to average for voltage, current and power reporting. Only bits 3:0 are used; bits 7:4 have no effect and should be left as 0000b. The meaning of the bits of this register are shown in Table 13.

Peak Voltage, Current, and Power Reporting

The 2-byte registers shown in Table 14 provides readings of the peak values for input voltage, output current, input power, and temperature in 10 bits direct format.

These registers can be reset with the CLEAR_PEAKS command (send byte D5h) or power cycling the part.

Table 12. CONFIG Register (D0h)

BIT NO.	BIT NAME	SETTINGS	DESCRIPTION
[15:14]	Ocp_severe_ filter[1:0]		Severe OCP deglitch time
		0	0µs
		1	1µs
		10	2µs
		11	10µs
[13]	I-ADC disable	0	I-ADC Enabled (default value)
		1	I-ADC Disabled
[12:11]	ss_cfg[1:0]	0	Soft-Start Delay = 0ms (default value)
		1	Soft-Start Delay = 10ms
		10	Soft-Start Delay = 20ms
		11	Not Used
[10]	Not Used	0	—
		1	—
[9:8]	pwrgd_th[1:0] (Notes 3, 4)	0	Power-Good Threshold = 11V, Self-Check Threshold = 9V
		1	Power-Good Threshold = 10V, Self-Check Threshold = 8V
		10	Power-Good Threshold = 9V, Self-Check Threshold = 7V
		11	Power-Good Threshold = 8V, Self-Check Threshold = 6V
[7]	ocp_cfg	0	Severe OCP = 130% of Reference OCP (default value)
		1	Severe OCP = 170% of Reference OCP
[6:5]	mocp_cfg[1:0]	0	**MAX16550 –** Moderate OCP timeout = 100µs (default value) **MAX16551 –** 240VA Power Fault-Detect timeout < 4ms (default value)
		1	**MAX16550 –** Moderate OCP timeout = 250ms **MAX16551 –** 240VA Power Fault-Detect timeout = 250ms
		10	**MAX16550 –** Moderate OCP timeout = 100ms **MAX16551 –** 240VA Power Fault-Detect timeout = 100ms
		11	**MAX16550 –** Moderate OCP timeout = 10µs **MAX16551 –** 240VA Power Fault-Detect timeout < 4ms
[4]	enable_ovp	0	V_{IN} OVP Protection Disabled (default value)
		1	V_{IN} OVP Protection Enabled

Table 12. CONFIG Register (D0h) (continued)

BIT NO.	BIT NAME	SETTINGS	DESCRIPTION
[3:2]	ovp_th[1:0]	0	Set V_{IN} OVP Threshold = 14V (default value)
		1	Set V_{IN} OVP Threshold = 16V
		10	Set V_{IN} OVP Threshold = 18V
		11	Not used
[1:0]	num_aves_alert[1:0]	0	Sets Averaging for PMBus Warning Levels to 1 Sample (default value)
		1	Sets Averaging for PMBus Warning Levels to 2 Samples
		10	Sets Averaging for PMBus Warning Levels to 4 Samples
		11	Sets Averaging for PMBus Warning Levels to 8 Samples

Table 13. Averaging Sample Size Settings Using Register DDh

BITS #	SETTING	STARTUP OCP, NUMBER OF SAMPLES USED FOR REPORTING AVERAGING FOR VOLTAGE, CURRENT AND POWER
[5:4]	su_ocp_cfg	8A 12A 4A 16A
[3:0]	0	1 sample
	1	2 samples
	10	4 samples
	11	8 samples
	100	16 samples
	101	32 samples
	110	64 samples
	111	128 samples
	1000	256 samples
	1001	512 samples
	1010	1024 samples
	1011	2048 samples
	1100	4096 samples
	1101	8192 samples
	1110	16384 samples
	1111	32768 samples

PMBus Reporting

For readings other than direct readings (e.g., Registers D1h, D2h, D3h, D4h, and FDh) PMBus specifications specify that the actual readings in their respective units correlate with the numerical values read from registers, as shown in Equation 14.

- Current/Voltage/Temperature: 10-bit resolution
- Power: 16-bit resolution

Equation 14:

$$X = \frac{1}{m}(Y \times 10^{-R} - b)$$

where:

X = Calculated, “real world” value in the appropriate units (A, V, °C, etc.)

m = Slope coefficient (a 2-byte, two’s complement integer)

Y = 2-byte two’s complement integer received from the PMBus device

b = Offset (a 2-byte, two’s complement integer)

R = Exponent (a 1-byte, two’s complement integer)

The values used in the ICs for the parameters above are shown in Table 15. Note that current and power readings depend on the value of R_{LOAD}, the external current reporting resistor.

Table 14. Manufacturer-Specific Direct Reporting Registers

REGISTER ADDRESS	REGISTER NAME	PARAMETER
D1h	PEAK_VIN	Peak Input Voltage
D2h	PEAK_IOUT	Peak Output Current
D3h	PEAK_PIN	Peak Input Power
D4h	PEAK_TEMP	Peak Temperature
FDh	PEAK_VOUT	Peak Output Voltage

Table 15. PMBus Equation Parameters

PMBUS REGISTER	FORMAT	DATA BYTES	m	b	R	UNITS
READ_IOUT (8Ch)*, READ_IIN (89h)*	Direct	2	3.824 x R_{LOAD}	-4300	-3	A
READ_VOUT (8Bh), READ_VIN (88h)	Direct	2	7578	0	-2	V
READ_ TEMPERATURE_1 (8Dh)	Direct	2	199	7046	-2	°C
READ_PIN (97h)	Direct	2	0.895 x R_{LOAD}	-9100	-2	W
READ_EIN (86h)**	Direct	2	3.505 x R_{LOAD}	0	-5	**

Input Capicitance (C_{IN}) Selection

Use of input capacitors is highly recommended to guarantee the input voltage is stable and noise free. For applications requiring no input capacitors before the MAX16550 and MAX16551, the input-voltage ripple should be less than 300mV peak-to-peak.

Output Capacitance (C_{OUT}) selection

The maximum output capacitance can be calculated as shown in Equation 15.

Equation 15:

$$C_{OUT} = \frac{(I_{INRUSH} \times C_{SS})}{I_{SS}}$$

where:

C_{SS} = Soft-start programming capacitance.

I_{SS} = Soft-start current, 30µA (typ).

C_{OUT} = Maximum load capacitance that can be used at soft-start with a purely capacitive load.

I_{INRUSH} = Desired maximum inrush current during start-up. Select I_{INRUSH} lower than programmed MAX16550/MAX16551 startup OCP ($I_{OCP(STARTUP)}$) and within MAX16550/MAX16551 startup SOA, refer to Figure 2.

Design Example

Assume a design value for maximum inrush current of 10A, and a soft-start capacitance of 25nF.

Assume 12V application and 30µA (typ) soft-start current; soft-start time in this case is 0.01ms. The maximum safe operating output current is 11A at 0.01ms (refer to the Startup SOA in Figure 2) and the default Startup OCP level is 8A (refer to Table 4).

The designed maximum inrush current of 5A is lower than 8A Startup OCP and within Startup SOA. The designed value is valid. Hence, the maximum load capacitance is calculated as shown in Equation 16.

Equation 16:

$$C_{OUT} = \frac{(5A \times 25nF)}{30\mu A} = 4.17mF$$

Input TVS Diode Selection

The use of a transient voltage suppression (TVS) diode at input is necessary to clamp input-voltage transient within rating of V_{IN} pin of MAX16550/MAX16551 (see the *Absolute Maximum Ratings* section).

A general guide to select the proper TVS diode is listed below:

- Choose TVS diode reverse-standoff voltage (V_{RWM}) ≥ operating voltage of MAX16550/MAX16551, 12V (typ).
- Choose TVS diode peak-pulse current (I_{PPM}) ≥ maximumt transient peak-pulse current of the MAX16550/MAX16551, 30A (typ).
- Choose TVS clamping voltage (V_C) ≤ maximum voltage-handling capability of the MAX16550/MAX16551, 22V (typ) for 150µs.

Recommend SMCJ13A based on selection criteria above.

Output Schottky Diode Selection

The use of a Schottky diode at output is necessary to clamp the negative output-voltage spike within the rating of V_{OUT} pin of the MAX16550/MAX16551 (see the *Absolute Maximum Ratings* section). Select the proper Schottky diode with low forward-voltage drop (V_F) and peak forward-surge current (I_{FSM}) higher than the expected inductive current.

Table 16. R_{OCP} and R_{ILOAD} Selection

PART	R_{OCP}	R_{ILOAD}
MAX16550 (30A)	97kΩ	8.2kΩ
MAX16551 (240VA)	107kΩ	10.1kΩ

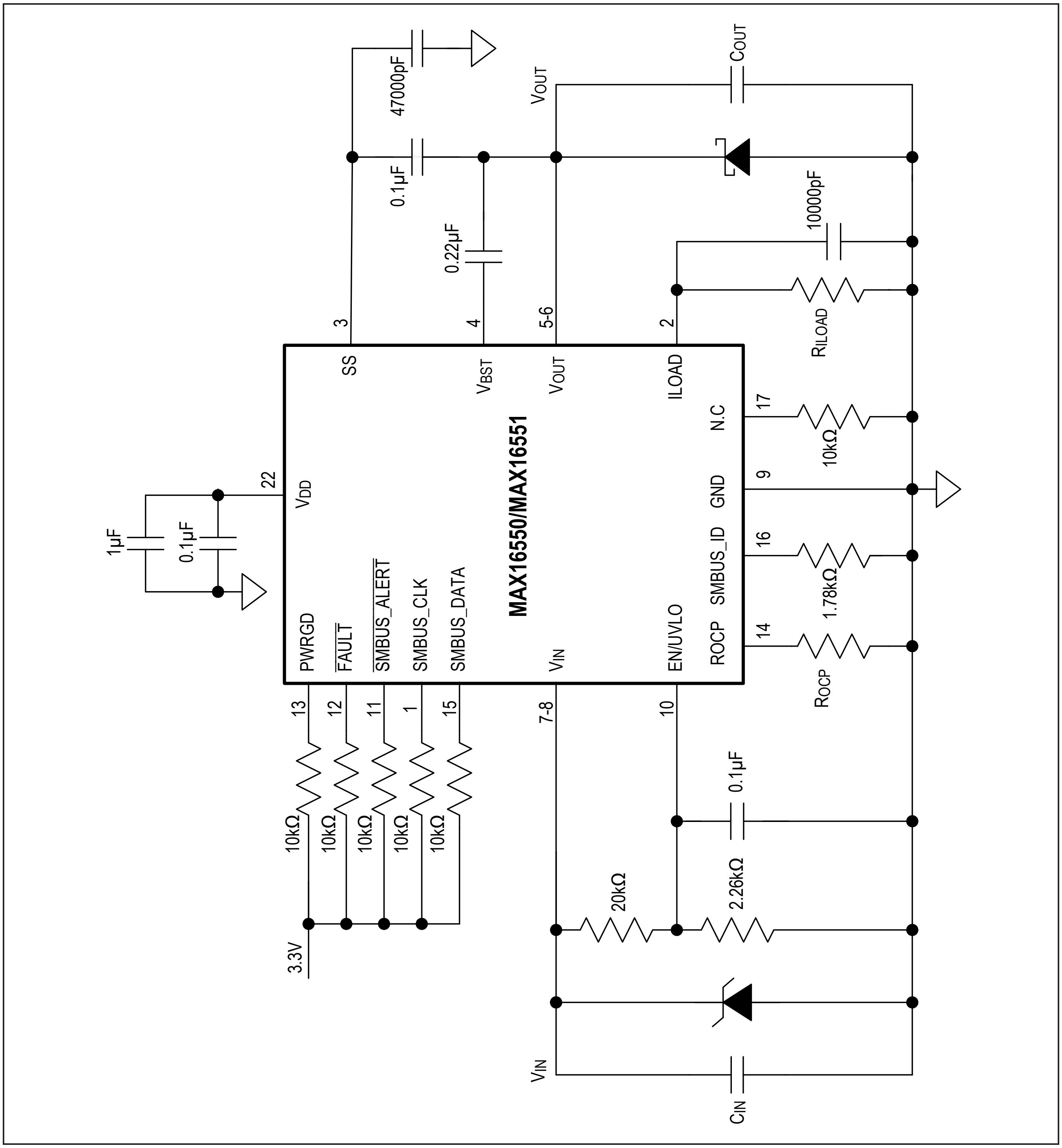


Figure 6. Reference Schematic

MAX16550/MAX16551 Layout Recommendations

V_{IN} and V_{OUT}

- Minimize input and output trace inductance by using wide and multiple V_{IN} and V_{OUT} planes for optimal thermal performance.
- Use multiple vias to connect interlaying power planes.
- Place input capacitors (where applicable) as close to the IC as possible.
- Place output capacitors as close to the IC as possible.
- Place TVS and Schottky diodes close to the IC for tighter coupling to V_{OUT}, and GND; V_{IN}, and GND.

Example

The EV kit layout in Figure 7 shows use of large, wide power planes for V_{IN} and V_{OUT} on the top layer. C_{IN} and C_{OUT} are close to the IC. The other V_{IN} and V_{OUT} power layers are connected with multiple vias between the pins.

Ground

- Use a trace approximately 1mm wide by 7mm long from the ground pin (pin 13) on the top layer to the underlying ground layers through at least two vias.
- Use a keepout to eliminate all metals directly under the MAX16550/MAX16551 package on the second layer.

Example

The EV kit layout in Figure 8 and 9 show the appropriate ground connection with vias and the ground keepout on Layer 2 (ground). The keepout should extend approximately 30mils outside the MAX16550/MAX16551 package.

V_{BST} and SS

Place the V_{BST} and SS capacitors on the top layer as close to the pins as possible.

V_{DD}

- Add a V_{DD} plane on the top layer to decouple the V_{DD} caps close to the IC to form a tighter loop to ground.
- Place V_{DD} ground far away from the output capacitor ground.

ROCP and ILOAD

The ROCP and ILOAD resistors should be placed as close to the IC as possible.

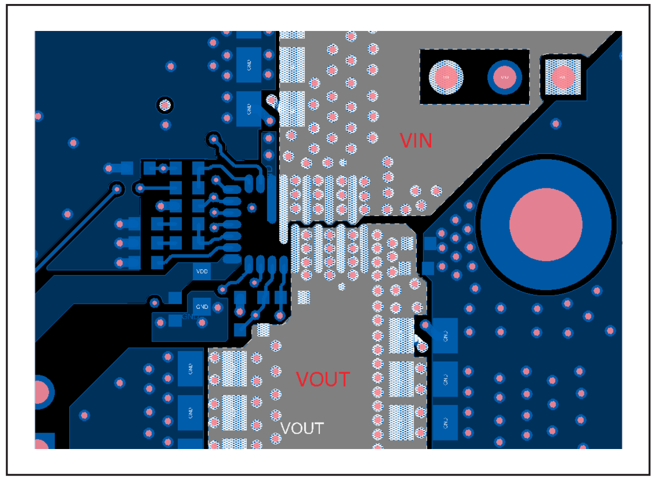


Figure 7. Top Layer (Power)

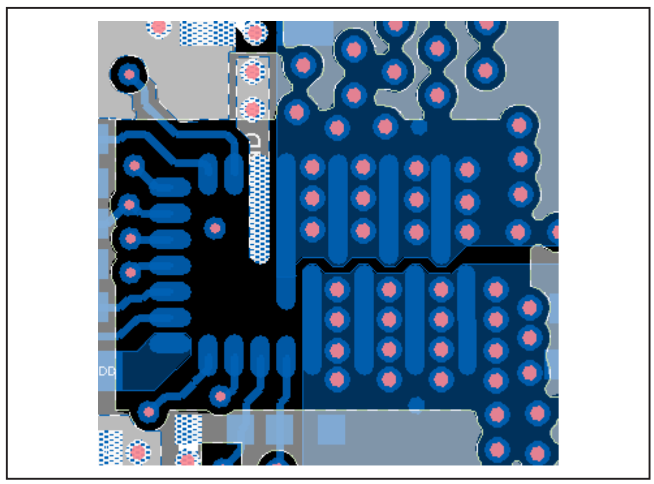


Figure 8. Top Layer (Power) and Layer 2 (GND) with Keepout

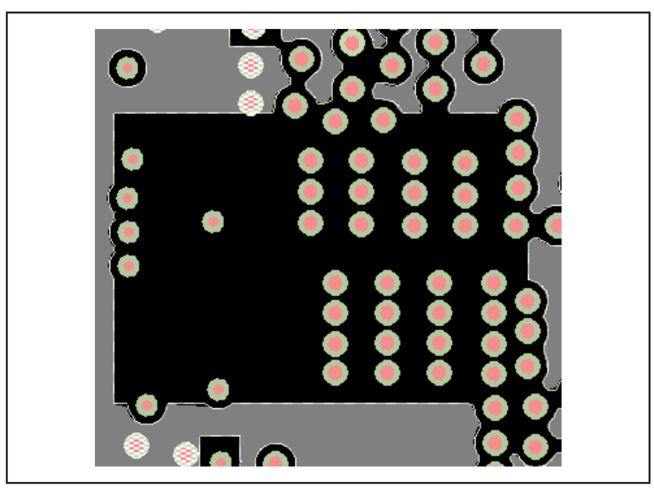


Figure 9. Second Layer (GND) with Keepout

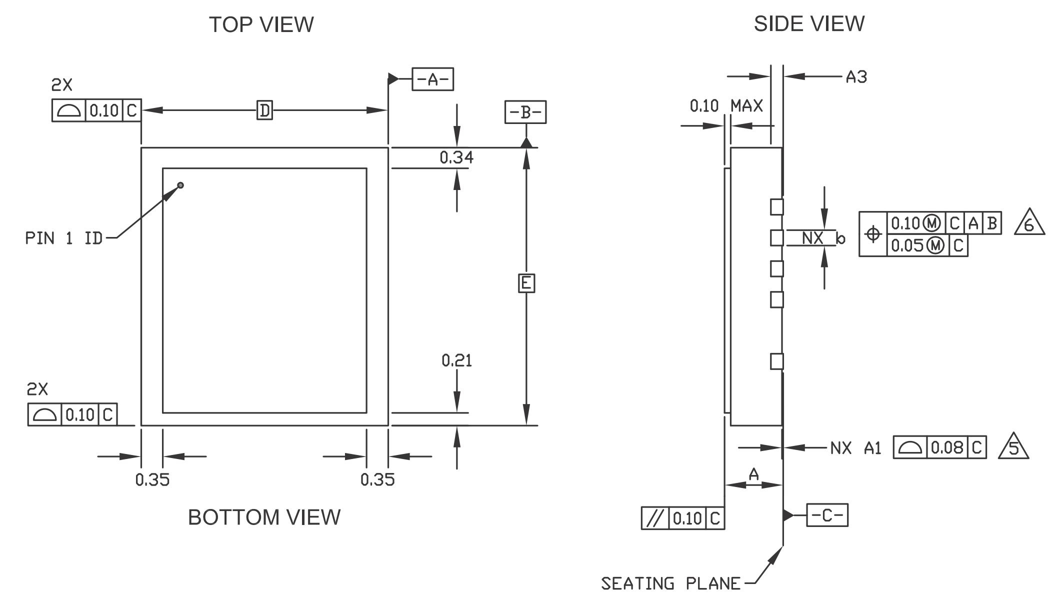
Ordering Information

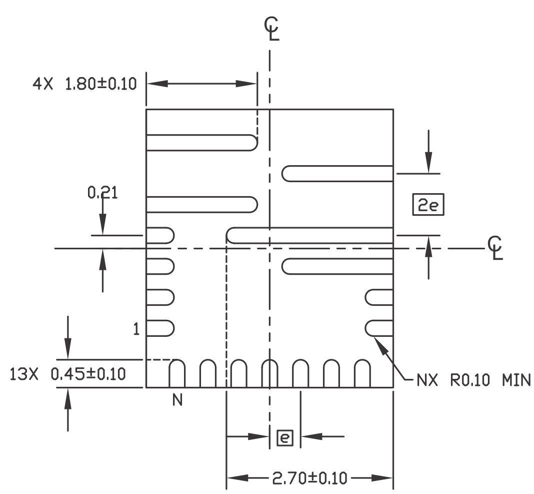
PART*	DESCRIPTION	PACKAGE	DRAWING NUMBER	SHIPPING METHOD	PACKAGE MARKING
MAX16550GPN+	Protection IC	18 QFN [Type E]	ES AP-3690	250u Tape & Reel	MAX16550
MAX16550GPN+T				2.5ku Tape & Reel	
MAX16551GPN+	240VA Protection IC	18 QFN [Type E]	ES AP-3690	250u Tape & Reel	MAX16551
MAX16551GPN+T				2.5ku Tape & Reel	

**These products are completely Halogen-free and Pb-free, employing special materials sets: molding compounds/die attach materials and 100% matte tin plate including anneal. These products are RoHS compliant with an -e3 termination finish and are compatible with both SnPb and Pb-free soldering operations. These products are MSL classified at peak reflow temperatures that meet JEDEC JSTD-020.*

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



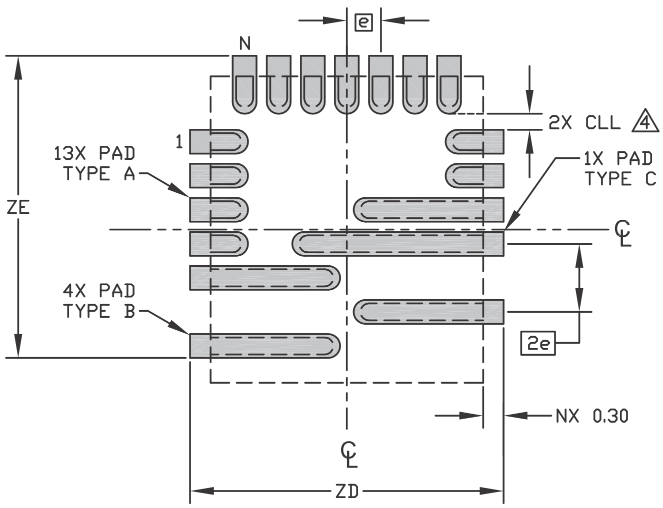


DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	0.95	1.00	0.035	0.037	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	4.00 BSC			0.157 BSC		
E	4.50 BSC			0.177 BSC		
e	0.50 BSC			0.020 BSC		
N	18 PINS			18 PINS		

NOTES:
1. Millimeters is the controlling dimension.
2. Drawing is not to scale.
3. N is the total number of terminals.
4. Dimensioning & tolerancing conform to ASME Y14.5-2009.
5. Coplanarity applies to the terminals and all other bottom surface metallization.
6. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.

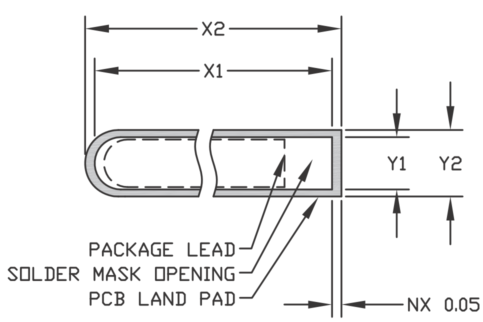
Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
CLL	0.24 REF			0.009 REF		
e	0.50 BSC			0.020 BSC		
N	18 PINS			18 PINS		
ZD	4.60 REF			0.181 REF		
ZE	4.44 REF			0.175 REF		

PAD DETAIL INFORMATION



	MILLIMETERS			INCHES		
DIM	TYPE A	TYPE B	TYPE C	TYPE A	TYPE B	TYPE C
Y1	0.28	0.28	0.28	0.011	0.011	0.011
Y2	0.35	0.35	0.35	0.014	0.014	0.014
X1	0.75	2.10	3.00	0.030	0.083	0.118
X2	0.85	2.20	3.10	0.033	0.087	0.122

NOTES:
1. Millimeters is the controlling dimension.
2. Drawing is not to scale.
3. N is the total number of terminals.
4. CLL is the corner pad edge to adjacent inside pad distance.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/16	Initial release	—
1	4/17	Updated *Benefits and Features, Absolute Maximum Ratings, Operating Ratings, Typical Operating Characteristics* sections, and Equations 2, 6, 9, Equation 9 *Design Example*, 11, and 13. Updated the *Pin Description* table, Table 11, and replaced the *Basic Application Circuit*, Figure 1, and Figure 6. Added *Soft-Start, Input Capacitance (C_{IN}) Selection, Output Capacitance (C_{OUT}) Selection*, *Input TVS Diode Selection, Output Schottky Diode Selection,* and *Layout Recommendations* sections.	1–3, 9–19, 27–29, 32-34, 38–40

For information on other Maxim Integrated products, visit Maxim Integrated’s website at www.maximintegrated.com.

