Click here for production status of specific part numbers.

MAX16543

Integrated Protection IC on a High-Power 12V Bus with an Integrated MOSFET and Lossless Current Sensing

General Description

The MAX16543 is an integrated follower protection IC that is used in parallel with a Maxim MAX16545B/MAX16545C master integrated protection IC for distribution, control, monitoring and protection of a system's 12V bus. The MAX16543 increases the current capability of the MAX16545B/MAX16545C. The MAX16545B/MAX16545C provide the reporting and fault protection circuits for the combined chipset. Up to two MAX16543s can be added to a MAX16545B/MAX16545C IC to provide DC current capability of more than 60A. The 1.8V bias supply and gate drive voltage supply of the MAX16543 are powered by the MAX16545B/MAX16545C.

All features of the MAX16545B/MAX16545C remain available when a MAX16543 is added to the circuit. The chipset provides monotonic startup with programmable ramp and delay to limit inrush current during startup. The total current is monitored and reported. Programmable system overcurrent protection is provided with several levels of protection.

The MAX16543 includes Maxim's patented lossless current sense to provide high accuracy current sensing through the MAX16545B/MAX16545C IC. The MAX16543 reports its current to the MAX16545B/MAX16545C, which then reports the total current.

The MAX16543 is controlled entirely by the MAX16545B/MAX16545C IC. The chipset input and output voltage fault protection is provided by the MAX16545B/MAX16545C, which enables and disables the MAX16543 as commanded by circuit conditions and command signals. *Master + 1 Follower Chipset* and *Master + 2 Follower Chipsets* show the basic application circuits for the master/follower chipset, with single and dual MAX16543s working in tandem to provide higher current ratings than a single MAX16545B/MAX16545C.

Benefits and Features

- Used with the MAX16545B/MAX16545C to Provide Integrated Protection for Loads > 60A On 12V Bus
- High Density: Industry's Smallest Circuit Breaker Solution Provides More Than 75% Board Area Savings
  - 12-Lead QFN Package
  - Integrated Power MOSFET with 1.5mΩ Total Resistance in 12V Power Path ($R_{DS(ON)}$, Including Package), Not Including Any Parallel Devices
- Lossless, Precise Total System Current Sensing and Reporting
- PMBus/SMBus Control and Reporting Through the MAX16545B/MAX16545C
- Increases Power-Supply Reliability with IC Self-Protection Features
  - Very Fast Fault Detection and Isolation
  - V_{IN} to V_{OUT} Short Protection During Startup
  - Overtemperature Protection
- Three Levels of Overcurrent Protection (OCP)
  - Programmable Moderate OCP
  - Programmable Severe OCP Provides Isolation < 5µs
  - Fail-Safe Safe OCP Provides Isolation < 250ns
- Modular Design, MAX16545B/MAX16545C with Single or Dual MAX16543 in Parallel Provide Different DC Current Capabilities
  - MAX16545B/MAX16545C + 1 MAX16543: 90A DC Capability
  - MAX16545B/MAX16545C + 2 MAX16543: 120A DC Capability

Systems and Applications

Servers, Networking, Storage, Communication Equipment and AC/DC Power Supplies

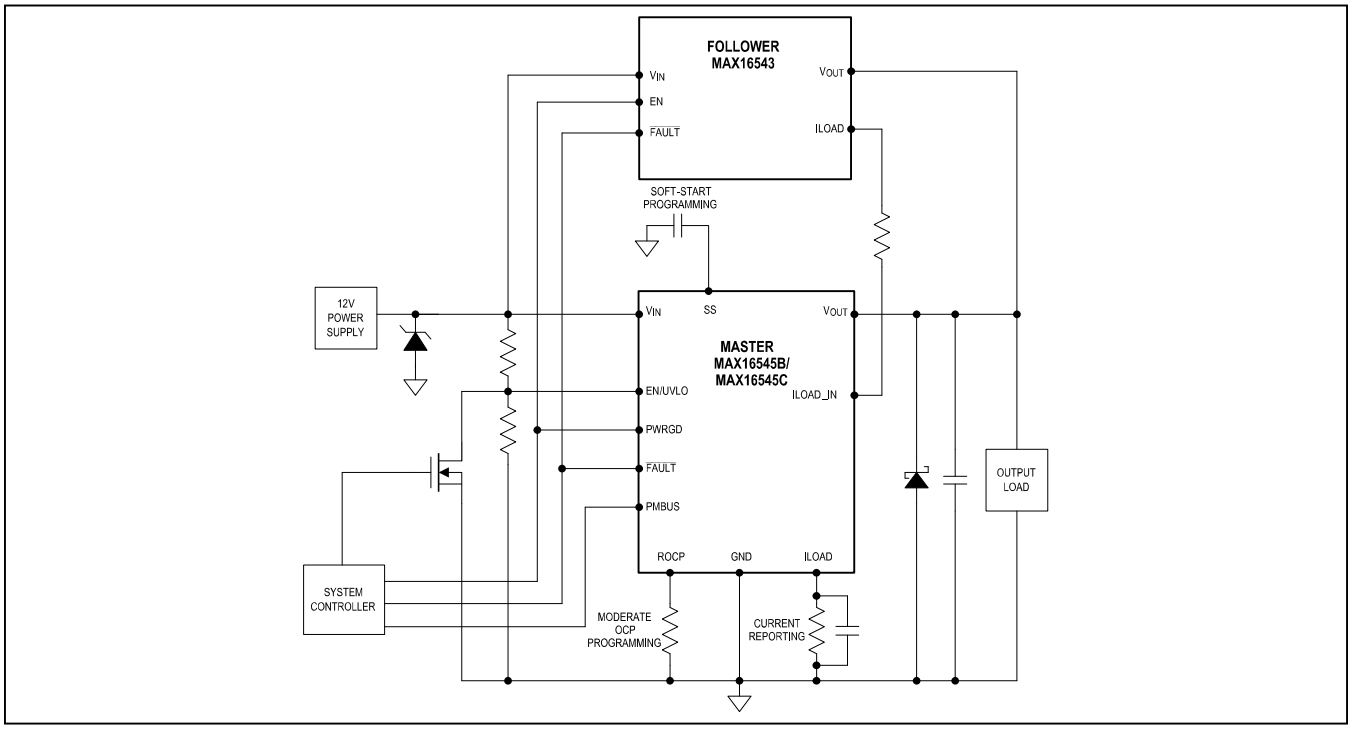
- Integrated Protection IC on 12V: Circuit Breaker/E-Fuse, Hot Swap

***Ordering Information* appears at end of data sheet.**

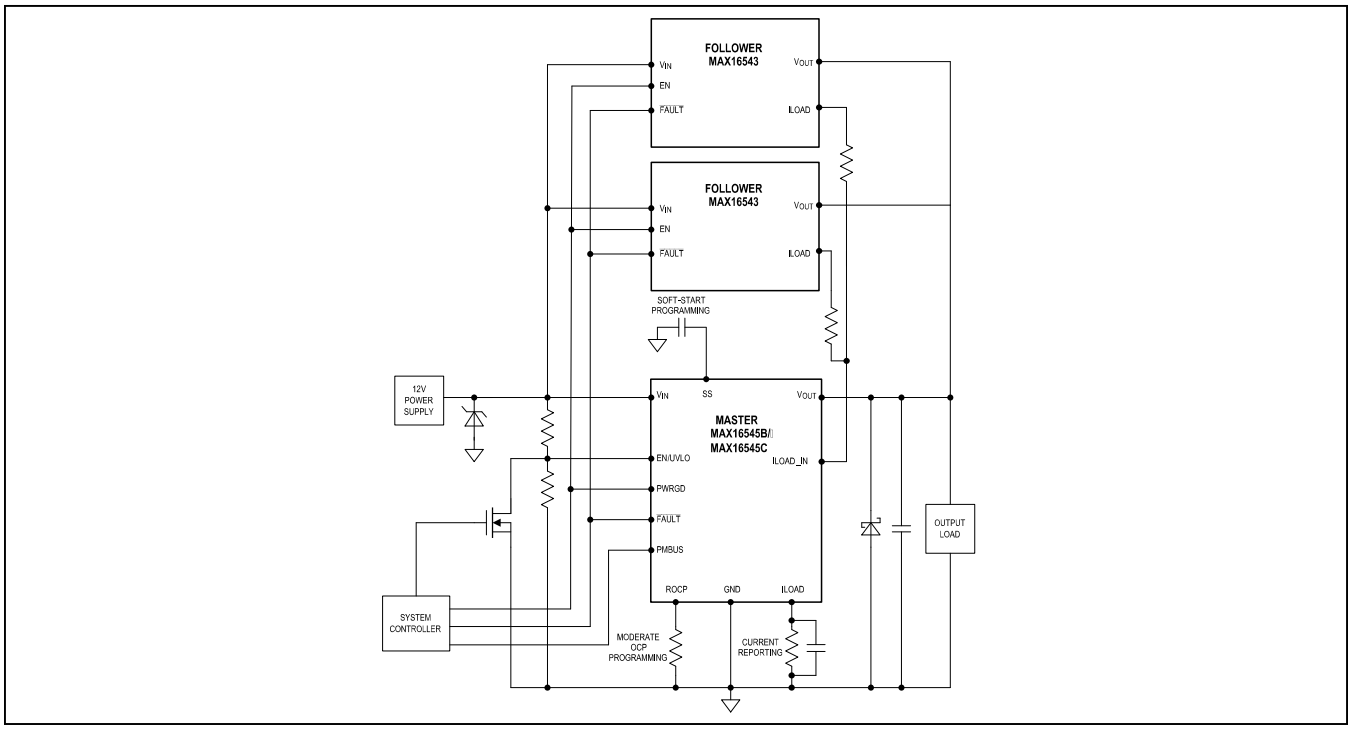
19-8742; Rev 3; 3/19

maxim integrated™

Master + 1 Follower Chipset



Master + 2 Follower Chipsets



Absolute Maximum Ratings

Supply Voltage (V_{IN}) DC.....-0.3V to +16V
Supply Voltage (V_{IN}) 150µs.....+22V
Bias Supply Pin Voltage (V_{DD}).....-0.3V to +2.5V
EN.....-0.3V to +5.5V
$\overline{FAULT}$..... -0.3V to +5.5V
ILOAD.....-0.3V to +2.5V
Output Voltage (V_{OUT}) DC.....-0.3V to +16V
V_{BST} (Relative to V_{OUT}).....-0.3V to +2.5V
Junction Temperature (T_J).....+150°C
Storage Temperature Range.....-65°C to +165°C
Peak Reflow Temperature.....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Ratings

Supply Voltage (V_{IN}).....+10.8V to +13.2V
EN..... 0V to +5.5V
Bias Supply Voltage (V_{DD}).....+1.75V to +1.94V
Junction Temperature (T_J).....0°C to +125°C

Package Information

12 FCQFN

Package Code	P123A4F+2
Outline Number	21-0973
Land Pattern Number	90-0477
THERMAL RESISTANCE	
Junction to Case (θ_{JC}) (max)	0.56°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(V_{IN} = 12V ±10%, unless otherwise specified. T_J = 0°C to +125°C, unless otherwise specified. Specifications are 100% production tested at T_A = +32°C. Limits over operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
12V SUPPLY (V_{IN})						
Supply Voltage Range	V_{IN}	(Note 1)	10.8	12	13.2	V
Supply Current	I_{IN}	FET ON, I_{OUT} = 0A		1.3	1.8	mA
1.8V LINEAR REGULATOR (V_{DD})						
Supply Voltage Range	V_{DD}	Supplied by the master IC (Note 1)	1.75	1.85	1.94	V
Supply Current	I_{DD}	FET ON, I_{OUT} = 0A		1.7	2.3	mA
UNDERVOLTAGE LOCKOUT: 1.8V SUPPLY (V_{DD})						
V_{DD} UVLO Rising Threshold			1.55	1.6	1.65	V
V_{DD} UVLO Falling Threshold			1.50	1.55	1.60	V
V_{DD} UVLO Hysteresis			20	50	80	mV
V_{DD} UVLO Response Time		From below threshold to FET OFF		2		µs

Electrical Characteristics (continued)

(V_{IN} = 12V ±10%, unless otherwise specified. T_J = 0°C to +125°C, unless otherwise specified. Specifications are 100% production tested at T_A = +32°C. Limits over operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BOOST VOLTAGE (V_{BST})						
Supply Voltage Range	V_{BST}	BST voltage above V_{OUT}. Supplied by the master IC (Note 1)		1.8		V
UNDERVOLTAGE LOCKOUT (V_{BST})						
V_{BST} UVLO Rising Threshold			1.2	1.3	1.4	V
V_{BST} UVLO Falling Threshold			0.9	1.1	1.3	V
V_{BST} UVLO Hysteresis			100	170	240	mV
V_{BST} UVLO Response Time		From falling threshold to FET OFF		2		µs
V_{BST} UVLO Digital Deglitch				10		µs
INTEGRATED MOSFET CHARACTERISTICS						
On-Resistance (Including Package Resistance)	$R_{DS(ON)}$	(Note 1)		1.5		mΩ
OVERCURRENT PROTECTION (OCP)						
MAX16543 Safe OCP Threshold	IOCP	(Notes 2, 3)	66	76	86	A
MAX16543 Safe OCP Delay	IOCP_Delay	(Note 2)		250		ns
CURRENT REPORTING (ILOAD)						
Linear Voltage Range		(Note 4)	0		1.35	V
Linear I_{OUT} Reporting Current Range		Current reporting range from a single MAX16543 device	0		35	A
I_{OUT} Reporting Gain	G_{ILOAD}	I_{LOAD} current divided by I_{OUT} current (Note 4)		5		µA/A
ANALOG CURRENT REPORTING ACCURACY						
Load Reporting Accuracy		I_{OUT} = 5A (Note 3)	-5.9		+5.9	%
		I_{OUT} = 10A (Note 3)	-4.1		+4.1	
		I_{OUT} = 16A (Note 3)	-2.4		+2.4	
		I_{OUT} = 35A (Note 3)	-1.8		+1.8	
OVERTEMPERATURE PROTECTION (OTP)						
Overtemperature Protection Threshold	T_{OTP}	(Notes 3, 5)	130	138	146	°C
ENABLE PIN (EN)						
Logic-High	V_{IH}		1.41			V
Logic-Low	V_{IL}				0.40	V
Hysteresis				450		mV
Internal Pulldown	R_{PD_EN}	(Note 1)		800		kΩ

Electrical Characteristics (continued)

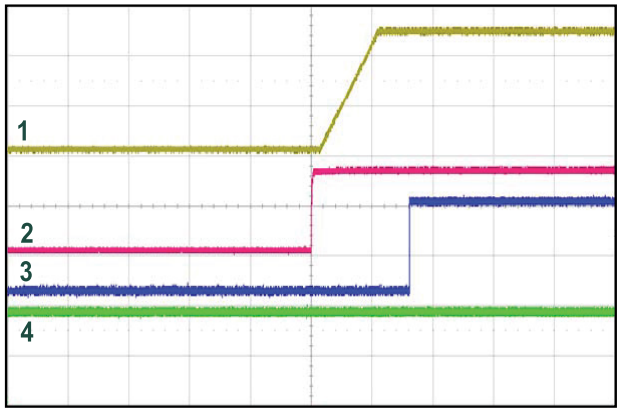
(V_{IN} = 12V ±10%, unless otherwise specified. T_J = 0°C to +125°C, unless otherwise specified. Specifications are 100% production tested at T_A = +32°C. Limits over operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{FAULT}}$ PIN (I/O)						
Logic High	V_{IH}		1.41			V
Logic Low	V_{IL}				0.40	V
Hysteresis				450		mV
Input Delay	$t_{D(IN)}$	From $\overline{\text{FAULT}}$ below V_{IL} to FET $V_{GS} < V_T$		100		ns
Internal Pulldown	R_{PD_FB}	(Note 1)		26		Ω
$\overline{\text{FAULT}}$ Output Low Voltage	V_{OL}	Sinking 4mA			0.4	V
Output Delay	$t_{D(OUT)}$	From fault to start of $\overline{\text{FAULT}}$ falling		100		ns

Note 1: Denotes specifications that apply for typical operation junction temperature (T_J = +32°C).
Note 2: The protection IC system comprising master and follower devices has three additional types of OCP. Refer to the MAX16545B/MAX16545C data sheet.
Note 3: Min/max limits are ≥ 4σ above the mean.
Note 4: Any current reported by the follower is added to the current reported by the master. The total protection IC system current reporting is 5µA/A.
Note 5: Guaranteed by design; not production tested.

Typical Operating Characteristics

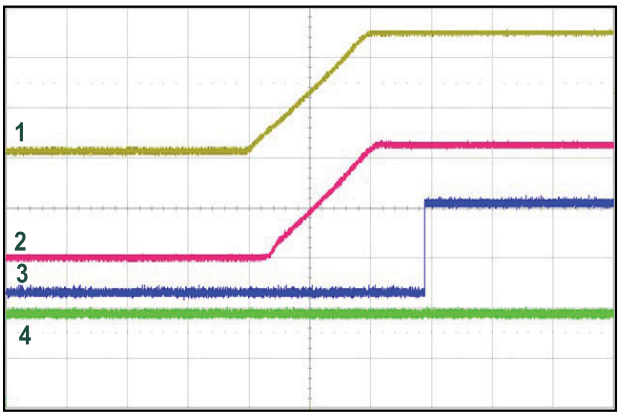
Startup Controlled With EN/UVLO (No Load)



Time: 20ms/div

Conditions: C_{SS} = 47nF
C_{OUT} = 373µF
1. V_{OUT} (5V/div)
2. EN/UVLO (500mV/div)
3. PWRGD (1V/div)
4. $\overline{FAULT}$ (1V/div)

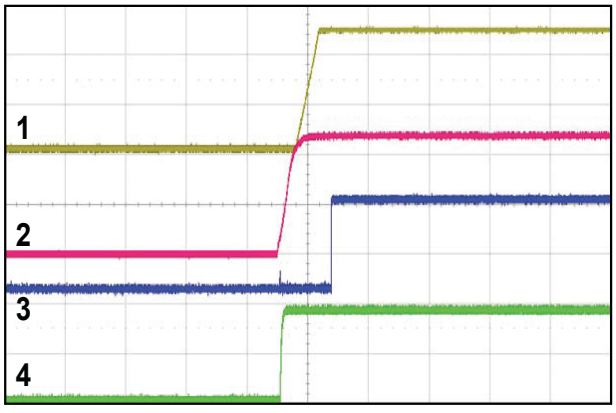
Startup Into Load, Controlled with EN/UVLO, 10Ω Resistive Load



Time: 10ms/div

Conditions: C_{SS} = 47nF,
C_{OUT} = 373µF
R_{LOAD} = 10Ω, Present at Startup
1. V_{OUT} (5V/div)
2. I_{OUT} (500mA/div)
3. PWRGD (1V/div)
4. $\overline{FAULT}$ (1V/div)

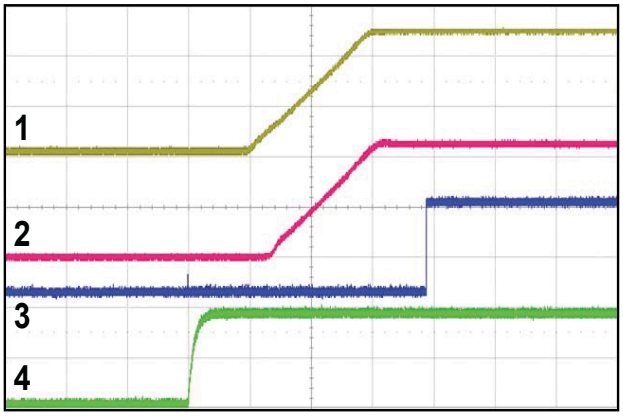
Startup Controlled with V_{IN} (No Load)



Time: 50ms/div

Conditions: C_{SS} = 47nF
C_{OUT} = 373µF
No Load at Startup
1. V_{OUT} (5V/div)
2. V_{IN} (5V/div)
3. PWRGD (1V/div)
4. $\overline{FAULT}$ (1V/div)

Startup Into Load, Controlled with V_{IN}, 10Ω Resistive Load

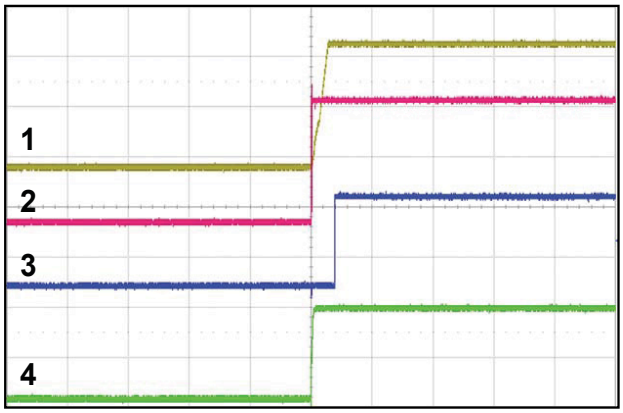


Time: 10ms/div

Conditions: C_{SS} = 47nF
C_{OUT} = 373µF
R_{LOAD} = 10Ω Present at Startup
1. V_{OUT} (5V/div)
2. I_{OUT} (500mA/div)
3. PWRGD (1V/div)
4. $\overline{FAULT}$ (1V/div)

Typical Operating Characteristics (continued)

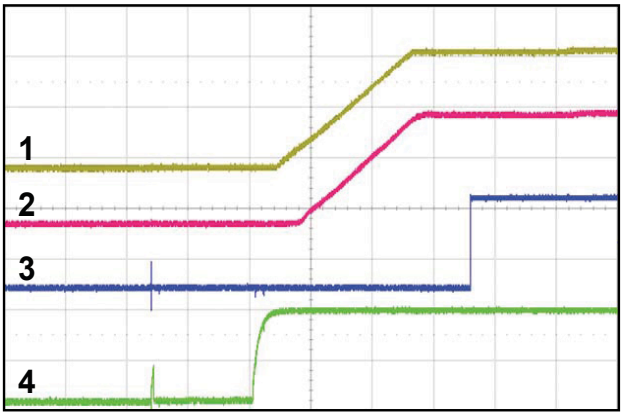
Hot Swap Startup (No Load)



Time: 50ms/div

Conditions: C_{SS} = 47nF
No Input Capacitors
No Load Present at Startup
1. V_{OUT} (5V/div)
2. V_{IN} (5V/div)
3. PWRGD (1V/div)
4. $\overline{FAULT}$ (1V/div)

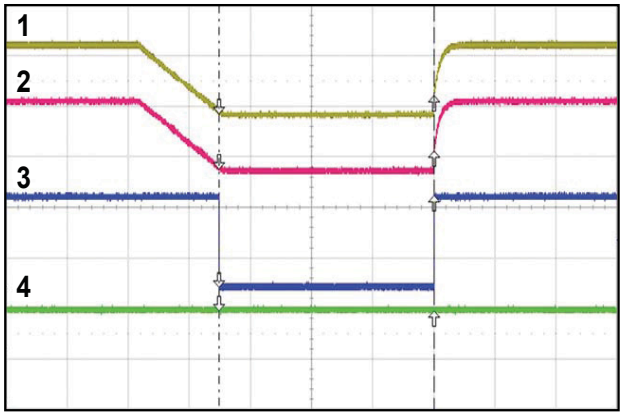
Hot Swap Startup Into Load, 10Ω Resistive Load



Time: 5ms/div

Conditions: C_{SS} = 47nF
R_{LOAD} = 10Ω Present at Startup
No Input Capacitors
1. V_{OUT} (5V/div)
2. I_{OUT} (5V/div)
3. PWRGD (1V/div)
4. $\overline{FAULT}$ (1V/div)

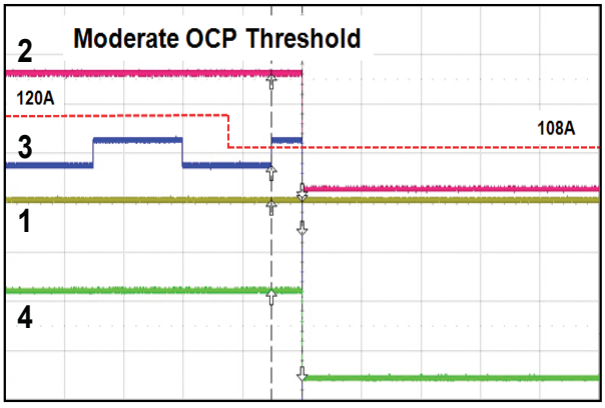
PWRGD Response



Time: 50ms/div

Conditions: C_{SS} = 47nF
PWR_GD Threshold = 10V
No Load
1. V_{OUT} (5V/div)
2. V_{IN} (5V/div)
3. PWRGD (1V/div)
4. $\overline{FAULT}$ (1V/div)

Moderate OCP – On-the-Fly

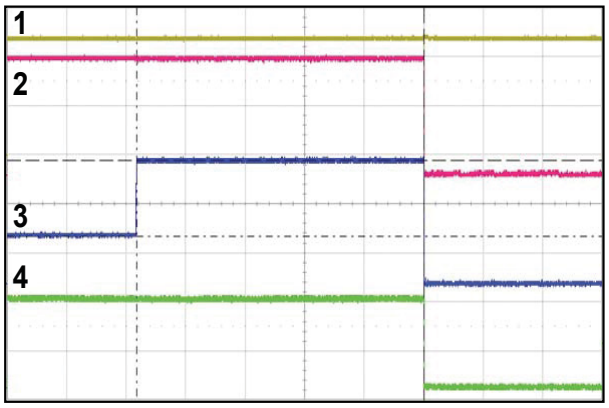


Time: 200ms/div

Conditions: I_{OUT} = 100A - 110A, 0.05A/µs
t = 300ms
Moderate OCP Timeout = 100ms
1. V_{IN} (10V/div)
2. V_{OUT} (5V/div)
3. I_{OUT} (20A/div)
4. $\overline{FAULT}$ (1V/div)
Master + Two Followers

Typical Operating Characteristics (continued)

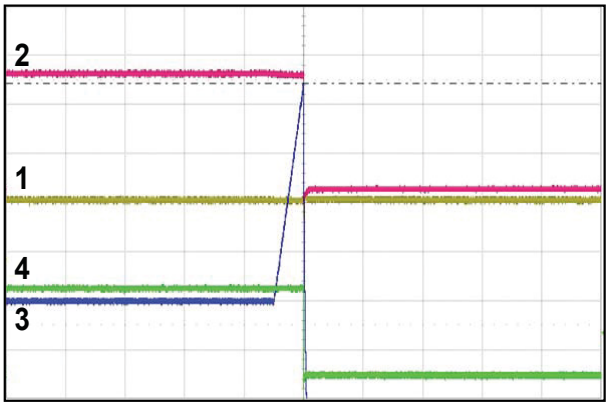
Moderate OCP – Timeout



Time: 50ms/div

Conditions: I_{OUT} = 50 - 125A
Moderate OCP Timeout = 250ms
Moderate OCP Threshold = 120A
1. V_{IN} (5V/div)
2. V_{OUT} (5V/div)
3. I_{OUT} (50A/div)
4. $\overline{FAULT}$ (1V/div)
Master + Two Followers

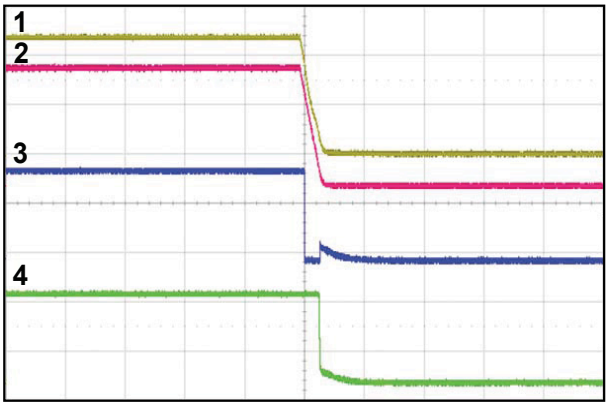
Severe OCP



Time: 2ms/div

Conditions: I_{OUT} = 50 - 150A
Moderate OCP Timeout = 250ms
Moderate OCP Threshold = 108A
Severe OCP Setting = 130%
1. V_{IN} (10V/div)
2. V_{OUT} (5V/div)
3. I_{OUT} (20A/div)
4. $\overline{FAULT}$ (1V/div)
Master + Two Followers

Shutdown Controlled by V_{IN}, No Load

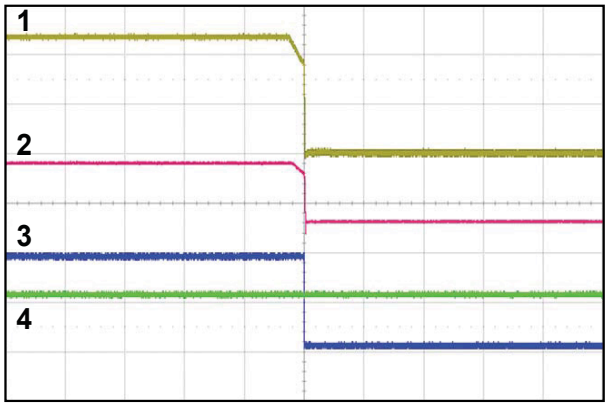


Time: 1s/div

Conditions: I_{OUT} = 0A
$\overline{FAULT}$ and PWRGD Pull-Up
Voltages Derived From 12V Supply
1. V_{OUT} (5V/div)
2. V_{IN} (5V/div)
3. PWRGD (1V/div)
4. $\overline{FAULT}$ (1V/div)

Typical Operating Characteristics (continued)

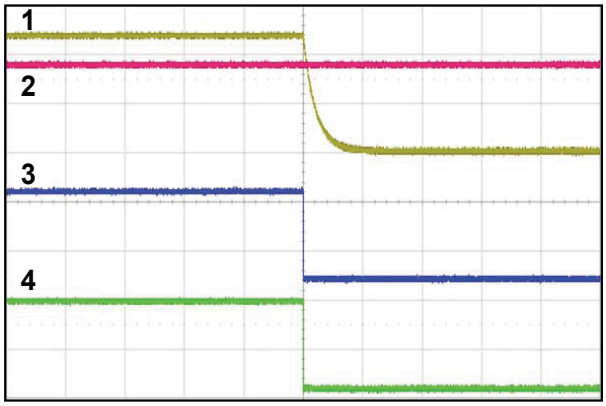
Shutdown Controlled by V_{IN}, 10Ω Resistive Load



Time: 20ms/div

Conditions: I_{OUT} = 0A
R_{LOAD} = 1Ω
1. V_{OUT} (5V/div)
2. I_{OUT} (10A/div)
3. PWRGD (1V/div)
4. $\overline{FAULT}$ (1V/div)

MAX16543 Fault Detection

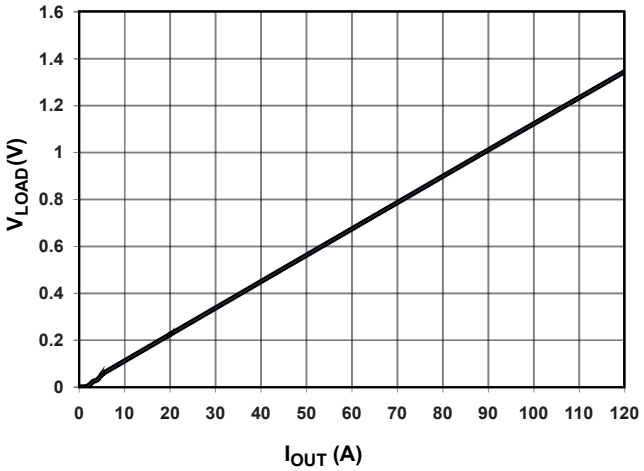


Time: 50ms/div

Conditions: Overtemperature Fault Detected by MAX16543
1. V_{OUT} (5V/div)
2. V_{IN} (5V/div)
3. PWRGD (1V/div)
4. $\overline{FAULT}$ (1V/div)

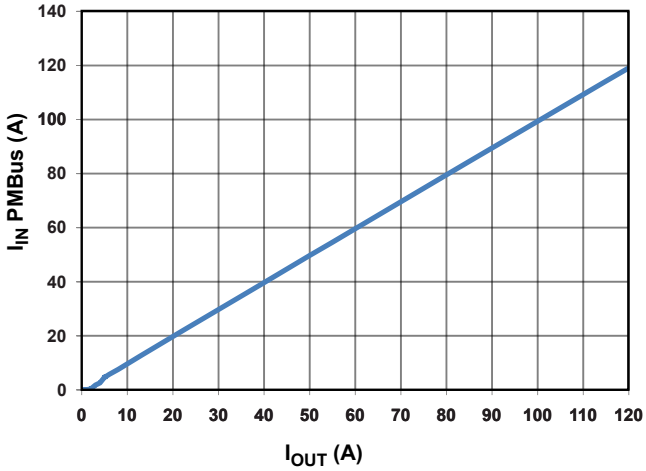
Typical Operating Characteristics (continued)

Output Current Monitoring and Reporting - Analog



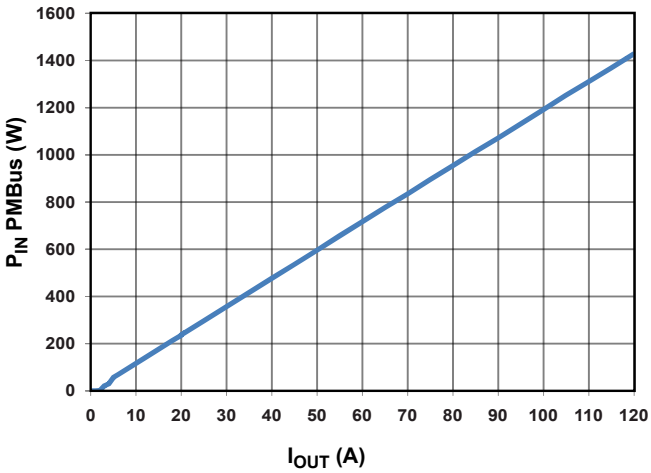
Conditions: I_{OUT} = 0 - 120A
R_{ILOAD} = 2.26kΩ
MAX16545B/C + 2 x MAX16543
Master + Two Followers

Input Current Reporting - PMBus



Conditions: I_{OUT} = 0 - 120A
MAX16545B/C + 2 x MAX16543
Master + Two Followers
Reporting of PMBus Register 89h

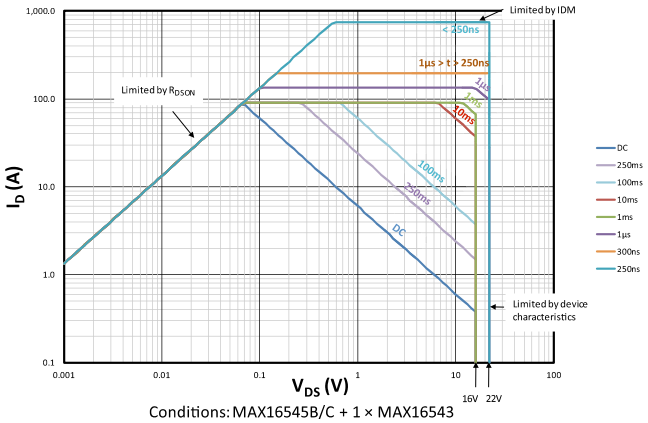
Input Power Reporting - PMBus



Conditions: I_{OUT} = 0 - 120A
V_{IN} =12V
MAX16545B/C + 2 x MAX16543
Master + Two Followers
Reporting of PMBus Register 97h

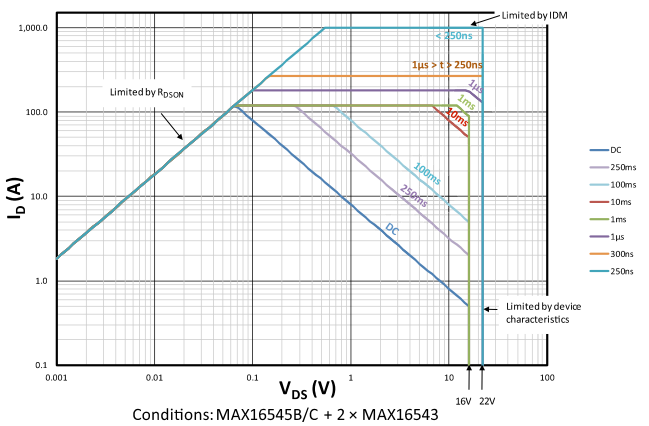
Typical Operating Characteristics (continued)

Normal Operation Safe Operating Area (SOA)



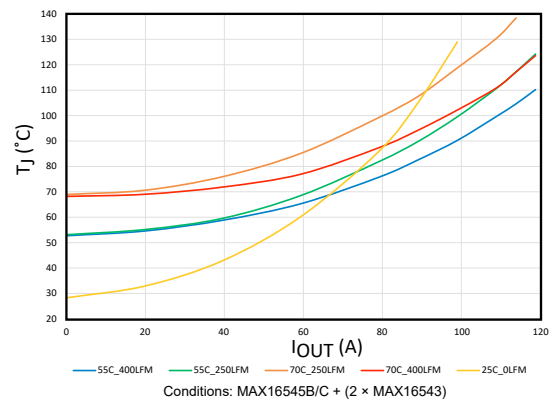
Conditions: MAX16545B/C + 1 × MAX16543

Normal Operation Safe Operating Area (SOA)



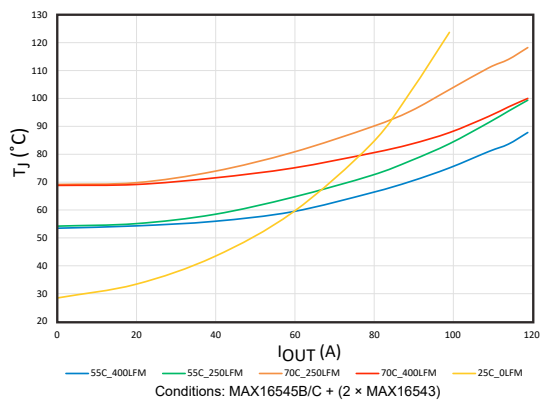
Conditions: MAX16545B/C + 2 × MAX16543

System Thermal Evaluation (No Heatsink)



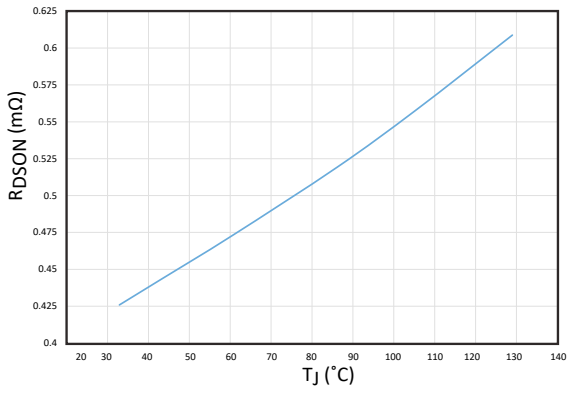
Conditions: MAX16545B/C + (2 × MAX16543)

System Thermal Evaluation (Heatsink)



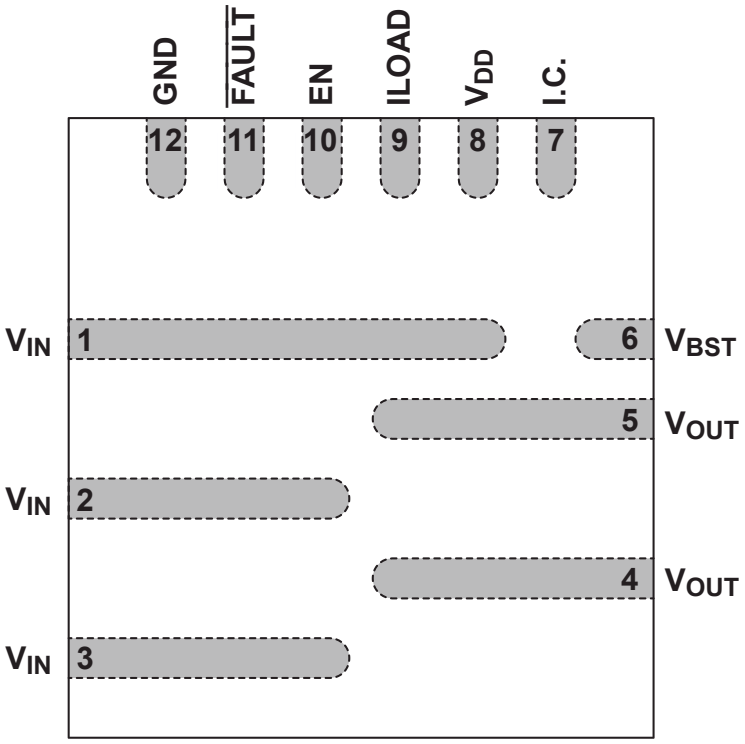
Conditions: MAX16545B/C + (2 × MAX16543)

System ON Resistance Including Package Resistance



Conditions: MAX16545B/C + (2 × MAX16543)

Pin Configuration



(TOP VIEW)

Pin Description

PIN	NAME	DESCRIPTION
1–3	V_{IN}	12V Input Power Pins, Power-Supply Side
4, 5	V_{OUT}	12V Output Power Pins, Load Side
6	V_{BST}	Power-Supply Pin for the Integrated FET Gate Drive. Connect this pin to the V_{BST} pin of MAX16545B/MAX16545C. Place a 1µF bypass capacitor between V_{BST} and V_{OUT} as close as possible, one for each MAX16543 device.
7	I.C.	Internally Connected. Connect this pin to GND through a 10kΩ resistor.
8	V_{DD}	Bias Supply Input. Connect this pin to the V_{DD} pin of the MAX16545B/MAX16545C.
9	ILOAD	Analog Current Representation of the Load Current. Connect this pin to the ILOAD_IN pin of the MAX16545B/MAX16545C through a 500Ω resistor.
10	EN	Enable Pin for MAX16543. Connect EN to the PWRGD pin of the MAX16545B/MAX16545C.
11	$\overline{FAULT}$	Fault Communication, Bidirectional Pin. $\overline{FAULT}$ is used to indicate/receive detection of latching faults. Connect this pin to the $\overline{FAULT}$ pin of the MAX16545B/MAX16545C, and to the system bias supply rail through a 10kΩ resistor. This pin is 5V compliant.
12	GND	IC Ground. Connect this pin to ground for proper device operation.

Detailed Description

Theory of Operation

The MAX16543 is designed to operate in conjunction with the MAX16545B/MAX16545C Integrated Protection IC to provide the same features as the MAX16545B/MAX16545C but for higher currents. The MAX16543 provides an analog load current signal output that is connected to the input on the MAX16545B/MAX16545C to allow the MAX16545B/MAX16545C to accurately report total system current using the lossless current sensing in both the MAX16545B/MAX16545C and MAX16543. In the event of a system fault, the MAX16545B/MAX16545C disable the MAX16543. The MAX16543 also includes a local fast overcurrent protection (safe OCP) and an overtemperature shutdown.

Startup

The MAX16545B/MAX16545C controls the output voltage ramp. The MAX16543 remains fully off until the output voltage has settled and the MAX16545B/MAX16545C power good signal goes high. The MAX16543 will then be enabled.

System Current Distribution

The distribution of the total input current between MAX16543 and MAX16545B/MAX16545C is determined by the on-resistances of both MAX16543 and MAX16545B/MAX16545C. See Maxim *Application Note 6754*. Under typical operation conditions:

- MAX16543 RDS_{ON} = 1.5mΩ (including package resistance)
- MAX16545B/MAX16545C RDS_{ON} = 0.9mΩ (including package resistance)

V_{DD} UVLO

Bias supply of MAX16543 is provided by MAX16545B/MAX16545C. MAX16543 implements V_{DD} UVLO fault monitor and protection. V_{DD} is monitored at all times. If V_{DD} falls below V_{DD} UVLO during normal operation, the MAX16543 turns off and recovers as soon as V_{DD} returns to normal value, if no other faults are detected.

V_{BOOST}, V_{GS} UVLO

Boost voltage is provided by the MAX16545B/MAX16545C. V_{BOOST} UVLO is checked by MAX16543 when EN and $\overline{FAULT}$ are above the enable threshold and remains active while the device is enabled.

Overcurrent Detection (Safe OCP)

The MAX16543 features a local, independent level of protection against severe overload faults with internally-fixed thresholds. It assures that the integrated FET is protected from exceeding its safe operating condition at all times. If at any time the load current through MAX16543 exceeds this safe OCP threshold, the MAX16543 turns the integrated FET off, asserts the $\overline{FAULT}$ low, and reports it to the MAX16545B/MAX16545C.

Overtemperature Protection (OTP)

The MAX16543 includes protection against overtemperature conditions. If the junction temperature exceeds the overtemperature threshold, the IC latches the integrated FET OFF and asserts the $\overline{FAULT}$ output low indicating it to the MAX16545B/MAX16545C.

$\overline{FAULT}$ Fault Reporting

The MAX16543 provides a dedicated pin for fault reporting, $\overline{FAULT}$. If at any time a latching fault is detected, $\overline{FAULT}$ pin is immediately latched LOW $\overline{FAULT}$_MS and reported to MAX16545B/MAX16545C. A MAX16545B/MAX16545C EN/UVLO or V_{IN} toggling, or a restart through the OPERATIONS command is required to reset the chipset after latching fault detection.

Fault Input and $\overline{FAULT}$ Pullup

$\overline{FAULT}$ pin is a bidirectional open-drain pin that can be used for fault communication, from the MAX16545B/MAX16545C or from an external circuitry to the MAX16543. To communicate a fault to the MAX16543, the $\overline{FAULT}$ pin must be pulled low. If $\overline{FAULT}$ is pulled low by an external circuit or by the MAX16545B/MAX16545C, the MAX16543 open its PASSFET until $\overline{FAULT}$ and PWRGD return high. The pullup voltage source must be considered to ensure the rail is operational and pulled high before the MAX16545B/MAX16545C and MAX16543 startup cycle.

Table 1. MAX16543 Faults Detected and Actions

PARAMETER	DESCRIPTION	$\overline{FAULT}$ ASSERTED	LATCHING
V_{BOOST} UVLO	UVLO For V_{BOOST} Voltage	Yes	Yes
MAX16543 Safe OCP	MAX16543 Safe Overcurrent Fault Detected	Yes	Yes
OTP	Overtemperature Fault Threshold Exceeded	Yes	Yes

Note: *Refer to the MAX16545B/MAX16545C data sheet for chipset/system faults and actions.*

These are the options for the pullup rail:

- MAX16543 V_{DD}: 1.8V internal LDO (MAX16545B/MAX16545C) rail. This rail is limited to 1.8V, thus the external system has to be compliant with that rail.
- System 3.3V or 5V Rail. FAULT is 5V compliant, and therefore an external higher voltage rail can be used for pullup. This rail has to be stable when the MAX16543 is initiating its startup procedure. If it is not, a potential false fault communication can occur.

ILOAD Reporting

The load current measured by the MAX16543 is sent as an analog signal to the MAX16545B/MAX16545C which then reports the total load. Refer to the MAX16545B/MAX16545C data sheet for more information. Equation 1 and Equation 2 apply to the total load and can be used whether one or two MAX16543s are present.

Equation 1:

$$V_{ILOAD} = R_{ILOAD} \times I_{LOAD} \times G_{ILOAD}$$

Equation 2:

$$R_{ILOAD} = \frac{V_{ILOAD}}{I_{LOAD\_FSD} \times G_{ILOAD}}$$

where:

V_{ILOAD} = current reporting voltage (V)

R_{ILOAD} = external current reporting resistor (Ω)

I_{LOAD} = load current $I_{OUT} = I_{IN}$ (A)

I_{LOAD_FSD} = desired full scale of current reporting (A)

G_{ILOAD} = current reporting gain from *Electrical Characteristics* table

For example to set the full-scale system current reported to 100A.

Equation 3:

$$R_{ILOAD} = \frac{1.35V}{100A \times \left(5 \times 10^{-6}\right)} = 2.7k\Omega$$

Programming Moderate OCP Threshold

The system moderate OCP threshold is externally programmable through a resistor connected to the R_OCP pin on the MAX16545B/MAX16545C. The value should be set to the correct system value taking into account the MAX16543 and MAX16545B/MAX16545C. Refer to the MAX16545B/MAX16545C data sheet for more details.

Equation 4:

$$I_{OCP} = \frac{V_{OCPM}}{R_{OCP}} \times GOCP$$

where:

I_{OCP} = moderate overcurrent protection threshold (A)

V_{OCPM} = overcurrent protection reference voltage shown in the MAX16545B/MAX16545C Electrical Characteristics table (V)

GOCP = overcurrent protection gain shown in the MAX16545B/MAX16545C Electrical Characteristics table (A/A)

R_{OCP} = Value of overcurrent protection programming resistor(Ω)

Equation 5:

$$R_{OCP} = \frac{V_{OCPM}}{I_{OCP}} \times GOCP$$

where:

I_{OCP} = moderate overcurrent protection threshold (A)

V_{OCPM} = overcurrent protection reference voltage shown in the MAX16545B/MAX16545C Electrical Characteristics table (V)

GOCP = overcurrent protection gain shown in the MAX16545B/MAX16545C Electrical Characteristics table (A/A)

R_{OCP} = Value of overcurrent protection programming resistor (Ω)

Design Example:

To set system moderate OCP to 100A nominal, using values from the MAX16545B/MAX16545C data sheet, see Equation 6.

Equation 6:

$$R_{OCP} = \frac{0.8V}{100A} \times \left(8 \times 10^{6}\right) = 64k\Omega$$

Input Capacitance (C_{IN}) Selection

Use of input capacitance is highly recommended to guarantee the input voltage is stable and noise free.

For applications requiring no input capacitors before the MAX16545B/MAX16545C + MAX16543 system, the input voltage ripple should be less than 300mV peak-to-peak.

Output Capacitance (C_{OUT}) Selection

The maximum output capacitance can be calculated as in Equation 7.

Equation 7:

$$C_{OUT} = \frac{I_{INRUSH} \times C_{SS}}{I_{SS}}$$

where:

C_{SS} = Soft-start programming capacitance.

I_{SS} = Soft-start current, 30µA typical.

C_{OUT} = Maximum load capacitance that can be used at soft-start with purely capacitive load

I_{INRUSH} = Desired maximum inrush current during start-up. Select I_{INRUSH} lower than programmed MAX16545B/MAX16545C startup OCP ($I_{OCP(STARTUP)}$) and within MAX16545B/MAX16545C startup SOA.

Design Example

Assume a design value for maximum inrush current of 10A, and a soft-start capacitance of 25nF.

Assume 12V application and typical 30µA soft-start current; soft-start time in this case is 0.01ms. The maximum safe-operating output current is 22A at 0.01ms. Assume the default startup OCP level is 16A.

The designed maximum inrush current of 10A is lower than 16A startup OCP and within startup SOA.

The designed value is valid. Hence, the maximum load capacitance is as shown in Equation 8.

Equation 8:

$$C_{OUT} = \frac{(10A \times 25nF)}{30\mu A} = 8.33mF\,(max)$$

Additionally, the recommended output capacitance should be less than 10mF to prevent false triggering of self-check during startup into precharged output.

Input TVS Diode Selection

The use of a transient voltage suppression (TVS) diode at input is necessary to clamp input-voltage transient within rating of the V_{IN} pins.

A general guide to select the proper TVS diode is:

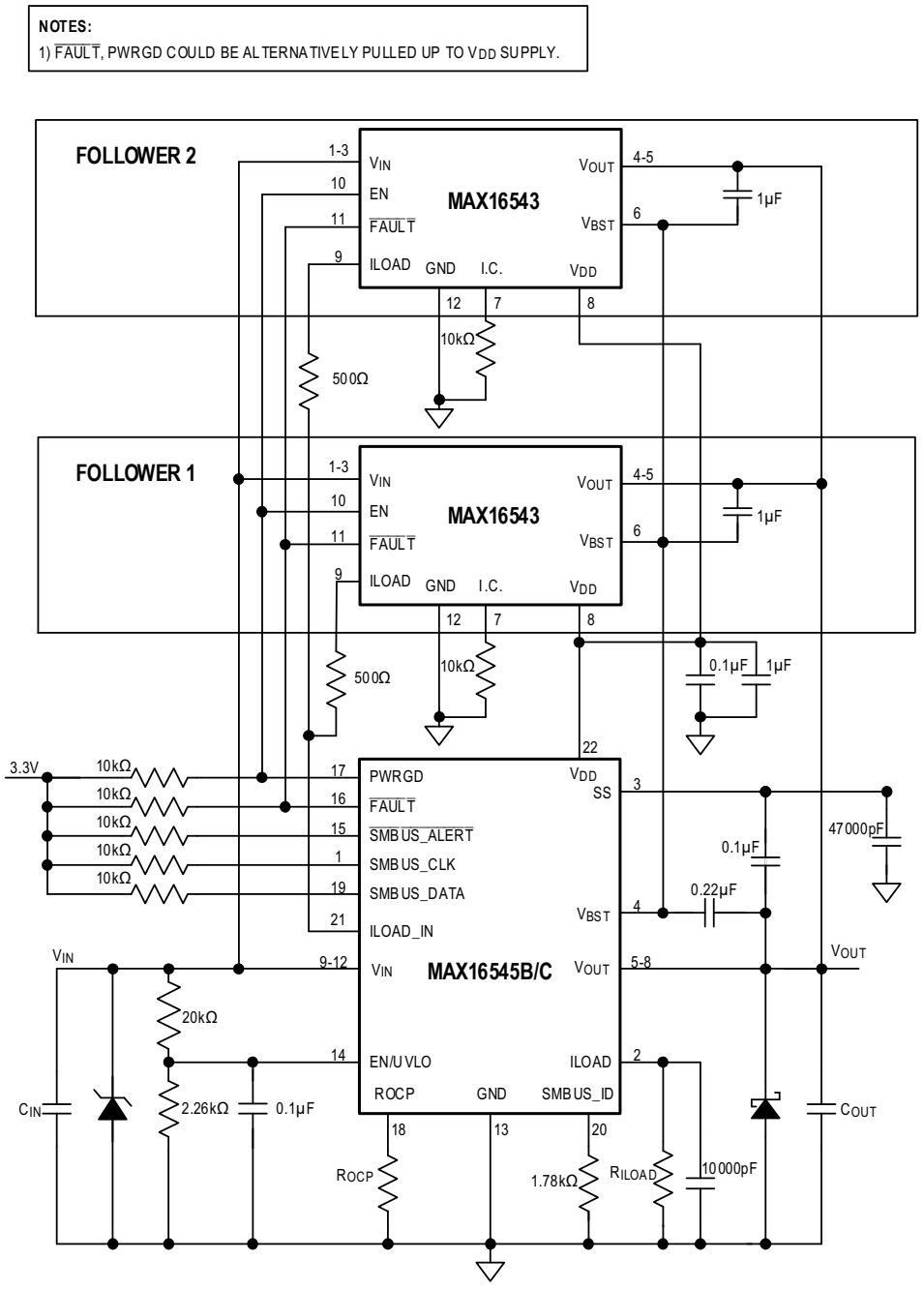
- Choose a TVS diode with reverse-standoff voltage (V_{RWM}) ≥ operating voltage of MAX16545B/MAX16545C + MAX16543 system (12V typ).
- Choose a TVS diode with peak-pulse current (I_{PPM}) ≥ maximum transient peak-pulse current of MAX16545B/MAX16545C + MAX16543 system (90A/120A typ).
- Choose a TVS diode with clamping voltage (V_C) ≤ maximum voltage handling capability of MAX16545B/MAX16545C + MAX16543 system (22V for 150µs typ)

2 × SMCJ13A is recommended based on selection criteria above.

Output Schottky Diode Selection

The use of Schottky diode at output is necessary to clamp the negative output-voltage spike within the Absolute Maximum rating of the V_{OUT} pin. Select the proper Schottky diode with low-forward voltage drop (V_F) and peak forward surge current (I_{FSM}) higher than the expected inductive current.

Master/Follower Reference Schematic: Single/Dual Configuration



See Maxim Application Note 6848

Layout Recommendations

(See *Maxim Application Note 6848*)

V_{IN} and V_{OUT}

- Minimize input and output trace inductance by using wide and multiple V_{IN} and V_{OUT} planes for optimal thermal performance.
- Use multiple vias to connect interlaying power planes.
- Place input capacitors (where applicable) as close to the IC as possible.
- Place output capacitors as close to the IC as possible.
- Place TVS and Schottky diodes close to the IC for tighter coupling to V_{OUT} and GND; V_{IN} and GND.

Example

The EV kit layout in Figure 1 shows use of large, wide power planes for V_{IN} and V_{OUT} on the top layer. C_{IN} and C_{OUT} are close to the IC. The other V_{IN} and V_{OUT} power layers are connected with multiple vias between the pins.

V_{BST} and SS

Place the V_{BST} and SS capacitors on the top layer as close to the pins as possible.

V_{DD}

- Add a V_{DD} plane on the top layer to decouple the V_{DD} caps close to the IC to form a tighter loop to ground.
- Create a quiet ground trace/plane connecting V_{DD} ground and GND pin together.

ROCP and ILOAD

The ROCP and ILOAD resistors should be placed as close to the IC as possible.

IC PIN

Connect a 10k resistor to ground.

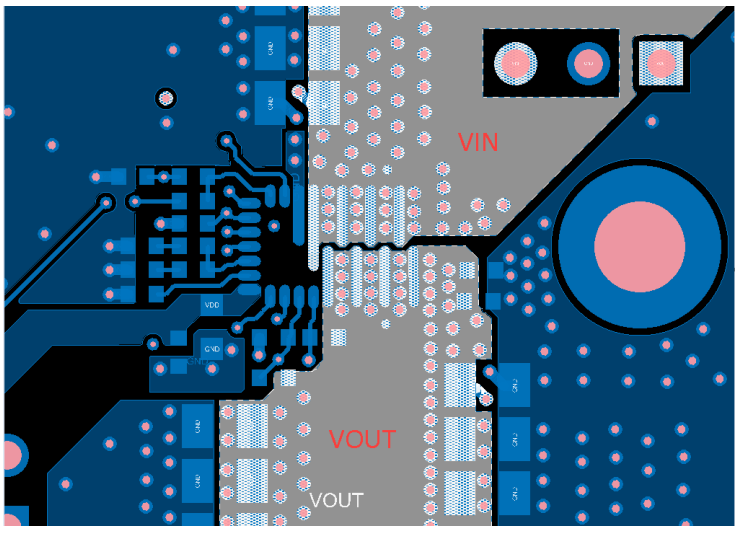


Figure 1. Top Layer (Power)

Ordering Information

PART NUMBER	DESCRIPTION	PACKAGE	SHIPPING METHOD	PACKAGE MARKING
MAX16543GPC+	Integrated Protection IC	12 FCQFN	Trays	MAX16543
MAX16543GPC+T			2.5ku Tape & Reel	

+Denotes a lead(Pb)-free/RoHS compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/16	Initial release	—
1	4/17	*General Description* section, *Master + 1 Follower Chipset and Master +2 Follower Chipsets* diagrams, *Typical Operating Characteristics*, *Pin Description* table, Figure 1, I*nput Capacitance (C_{IN}) Selection, Output Capacitance (C_{OUT}) Selection,* and *Input TVS Diode Selection* sections. Added *VT505/MAX16545 + MAX16543 System Layout Recommendations* section.	1–2, 6–8, 10–11, 16–19
2	9/18	Updated Figure 1	18
3	3/19	Change master IC part number to support MAX16543 and MAX16545B public introduction. Changed layout recommendations to align with AN6848. Changed N.C. pin to I.C. to indicate internal connection.	1–19

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