

## MAX16136

## High-Precision Supervisory ICs with Window Watchdog and Overvoltage Indicator

### General Description

The MAX16136, a low voltage,  $\pm 1\%$  accurate window-detector supervisor circuit monitors a single system supply voltage and the integrity of code execution by a microprocessor or microcontroller. This device features an active-low, open-drain output that asserts whenever the monitored supply rail falls outside of the factory-trimmed undervoltage/overvoltage window threshold. The reset output remain asserted for the programmed reset timeout period after the monitored supply voltage falls within the undervoltage/overvoltage window threshold.

The MAX16136 offers factory-trimmed voltage thresholds from 0.5V to 5V in approximately 20mV increment. A variety of factory trimmed undervoltage/overvoltage thresholds from  $\pm 4\%$  to  $\pm 11\%$  are available to accommodate different supply voltages and tolerances.

A window-watchdog timer circuit monitors microprocessor or microcontroller activity. During normal operation, the microprocessor or microcontroller must repeatedly toggle the watchdog input (WDI) low within the fast watchdog timeout ( $t_{WD\_F}$ ) and slow watchdog timeout ( $t_{WD\_S}$ ). If the microcontroller or microprocessor does not toggle WDI within the window-timeout period, the supervisor asserts the watchdog output (WDO) to signal that the system is not executing code as expected. The watchdog output pulse can be used to reset the microprocessor or microcontroller, or it may be used to interrupt the system to warn of execution errors.

In addition, the MAX16136 features an overvoltage fault output (OV) that latches low when the monitored rail exceeds the overvoltage threshold. The latched output can be cleared by pulling CLR low.

The MAX16136 is available in a small, 2mm x 2mm, 8-pin TDFN side-wettable package with exposed pad and operates over the automotive temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### Applications

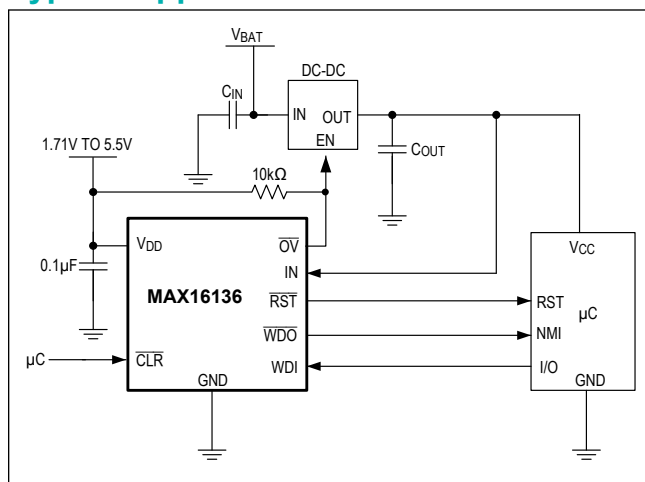
- Advanced Driver-Assistance Systems (ADAS)
- Automotive
- Multivoltage ASICs
- Servers
- Storage Equipment

### Benefits and Features

- $\pm 1\%$  Accuracy
- Enables ASIL Compliance at System Level
  - FMEDA Results Available upon Request
- 0.5V to 5V Threshold Range with 20mV Increments
- $\pm 4\%$  to  $\pm 11\%$  Undervoltage/Overvoltage Thresholds
- Latched Overvoltage Fault Output
- Clear Fault Input
- 5 $\mu\text{s}$  Overvoltage Fault Delay
- Window Watchdog Timeout
- Factory-Set Reset Timeout
- Open-Drain Reset Output
- 8-Pin TDFN Side-Wettable Package
- $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Operating Temperature Range

**Ordering Information** appears at end of data sheet.

### Typical Application Circuit



## Absolute Maximum Ratings

$V_{DD}$ to GND.....	-0.3V to +6V
IN, WDO, RST, CLR, OV, WDI to GND.....	-0.3V to +6V
Input/Output Continuous Current, $\overline{WDO}$ , $\overline{RST}$ , $\overline{CLR}$ , $\overline{OV}$ , WDI.....	$\pm 20$ mA
Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ ) TDFN (derate 11.7mW/°C above 70°C) .....	937.9mW

Operating Temperature Range .....	-40°C to +125°C
Junction Temperature .....	+150°C
Soldering Temperature (Reflow).....	+260°C
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (Soldering, 10s) .....	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Information

### 8 TDFN

Package Code	T822Y+3C
Outline Number	<a href="#">21-100185</a>
Land Pattern Number	<a href="#">90-100070</a>
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	85.3°C/W
Junction to Case ( $\theta_{JC}$ )	8.9°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

( $V_{DD} = 1.71\text{V}$  to 5.5V.  $T_A = T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$  under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLY</b>						
Operating Voltage Range	$V_{DD}$	Comparators functional	1.71		5.5	V
		Output guaranteed to be at known state	1.1			
Supply Current	$I_{DD}$	$\overline{RST}$ , $\overline{OV}$ , $\overline{WDO}$ not asserted		15	35	$\mu\text{A}$
Undervoltage Lockout Threshold	$V_{UVLO}$	$V_{DD}$ rising	1.3	1.50	1.68	V
Undervoltage Lockout Hysteresis	$V_{UVLO\_HYS}$	$V_{DD}$ falling		47		mV
<b>INPUT VOLTAGE (IN)</b>						
Nominal Input Threshold Voltage Range	$V_{IN\_NOM}$		0.5		5	V
Nominal Input Threshold Voltage Programming Step	$V_{IN\_NOM\_STEP}$			20		mV
Undervoltage/Overvoltage Programming Range	TOL	Reset occurs when $V_{IN\_NOM}$ falls outside of $V_{IN\_NOM} \times (1 \pm \text{TOL})$	$\pm 4$		$\pm 11$	% of $V_{IN\_NOM}$

## Electrical Characteristics (continued)

( $V_{DD} = 1.71V$  to  $5.5V$ .  $T_A = T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$  under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT THRESHOLD ACCURACY						
Undervoltage Threshold Accuracy	V <sub>UVTH_A</sub>	All V <sub>IN_TH</sub> setting, V <sub>IN_NOM</sub> falling, V <sub>UVTH</sub> = V <sub>IN_NOM</sub> x (T̄ - TOL%)	-1		+1	%
Overvoltage Threshold Accuracy	V <sub>OVTH_A</sub>	All V <sub>IN_TH</sub> setting, V <sub>IN_NOM</sub> rising, V <sub>OVTH</sub> = V <sub>IN_NOM</sub> x (T̄ + TOL%)	-1		+1	%
Undervoltage/Overvoltage Hysteresis	V <sub>HYS</sub>			0.25		%V <sub>TH</sub>
Input Current	I <sub>IN</sub>			1.3	5	μA
Overvoltage Fault-to- $\overline{OV}$ Assert Delay	t <sub>OV DLY</sub>	(V <sub>OVTH</sub> - 1%) to (V <sub>OVTH</sub> + 1%)		5		μs
$\overline{OV}$ Fault Glitch Immunity		V <sub>OVTH</sub> + 5%		200		ns
$\overline{RST}$ Leakage Current		V $\overline{RST}$ = V $\overline{OV}$ = V $\overline{WDO}$ = 5.5V		0.01	1	μA
CLEAR INPUT ( $\overline{CLR}$ )						
$\overline{CLR}$ Input Glitch Immunity			50			ns
$\overline{CLR}$ Minimum Input Pulse Width	t <sub>CLR</sub>	( <i>Note 1</i> ) ( <i>Note 2</i> )	0.4			μs
$\overline{CLR}$ Internal Pullup Resistance				50		kΩ
WATCHDOG						
Fast Watchdog Timeout Accuracy	t <sub>WD_F</sub>	V <sub>DD</sub> = 3.3V ( <i>Note 3</i> )	-20		+20	%
Slow Watchdog Timeout Accuracy	t <sub>WD_S</sub>	V <sub>DD</sub> = 3.3V ( <i>Note 3</i> )	-20		+20	%
Minimum Watchdog Input Pulse		After $\overline{WDO}$ asserts	24			μs
$\overline{WDO}$ Pulse Duration	t <sub>WDOF</sub>	WDI Input signal period < t <sub>WD_F</sub>		50		ms
	t <sub>WDOS</sub>	WDI Input signal period > t <sub>WD_S</sub>		100		
RESET OUTPUT ( $\overline{RST}$ )						
Reset Timeout Period Accuracy	t <sub>RP</sub>	From time V <sub>IN</sub> enters overvoltage/undervoltage threshold-window to time $\overline{RST}$ goes high, V <sub>DD</sub> = 3.3V	-20		+20	%
IN-to- $\overline{RST}$ Propagation Delay	t <sub>D</sub>	(V <sub>OVTH</sub> - 1%) to (V <sub>OVTH</sub> + 1%)		5		μs
IN-to- $\overline{RST}$ Reset Propagation Delay	t <sub>D</sub>	(V <sub>UVTH</sub> + 1%) to (V <sub>UVTH</sub> - 1%)		15		μs
INPUT VOLTAGE (WDI, $\overline{CLR}$ )						
WDI, $\overline{CLR}$ Input Voltage Low					0.3 x V <sub>DD</sub>	V
WDI, $\overline{CLR}$ Input Voltage High			0.7 x V <sub>DD</sub>			V
WDI, $\overline{CLR}$ Leakage Current			-1		+1	μA

**Electrical Characteristics (continued)**

( $V_{DD} = 1.71V$  to  $5.5V$ .  $T_A = T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$  under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>OUTPUT VOLTAGE ( <math>\overline{RST}</math>, <math>\overline{WDO}</math>, <math>\overline{OV}</math> )</b>						
Output Voltage Low	$V_{OL}$	$\overline{RST}$ , $\overline{OV}$ , $\overline{WDO}$	$V_{DD} = 5V$ , $I_{SINK} = 3mA$	0.1	0.3	V
			$V_{DD} = 1.71V$ , $I_{SINK} = 8\mu A$	0.1	0.3	
		$\overline{RST}$	$V_{DD} = 1.1V$ , $I_{SINK} = 8\mu A$	0.1	0.3	

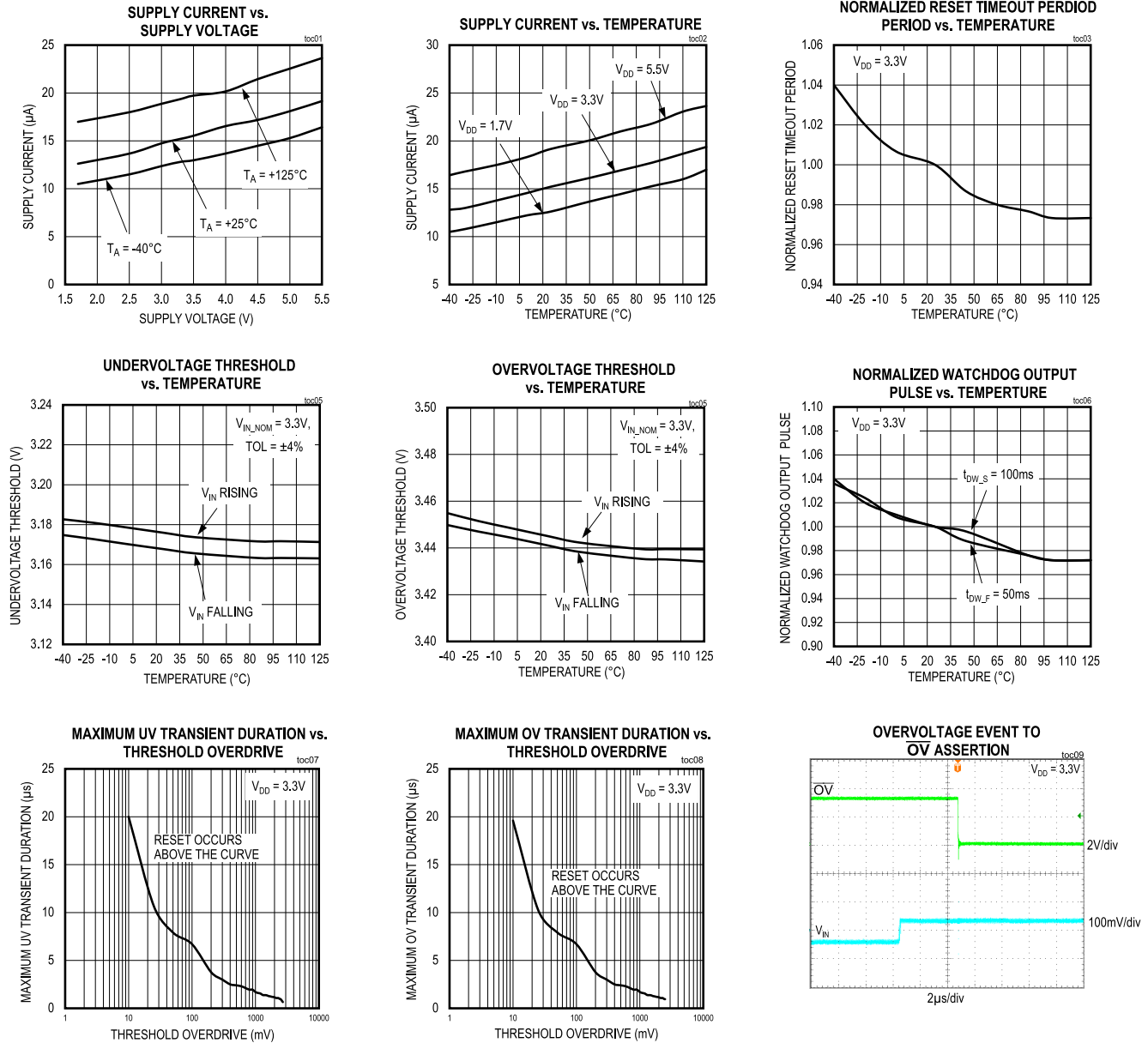
**Note 1:** Minimum pulse required to clear  $\overline{OV}$  latched state. No overvoltage fault present and  $\overline{RST} = \text{high}$ .

**Note 2:** Pulling  $\overline{CLR}$  low for a pulse width duration  $t_{CLR} > 5\mu s$  asserts  $\overline{RST}$ . A consecutive series of pulses on  $\overline{CLR}$  with low pulse width duration of  $t_{CLR} > 5\mu s$  must be separated by high pulse width duration  $> t_{RP}$  for valid reset operation.

**Note 3:** The margin for error will be an additional  $\pm 30\mu s$  due to the internal synchronization logic.

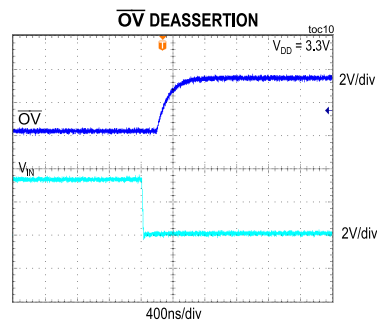
## Typical Operating Characteristics

( $V_{DD} = 1.71V$  to  $5.5V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ , Typical values are at  $V_{DD} = 3.3V$ , unless otherwise specified.)



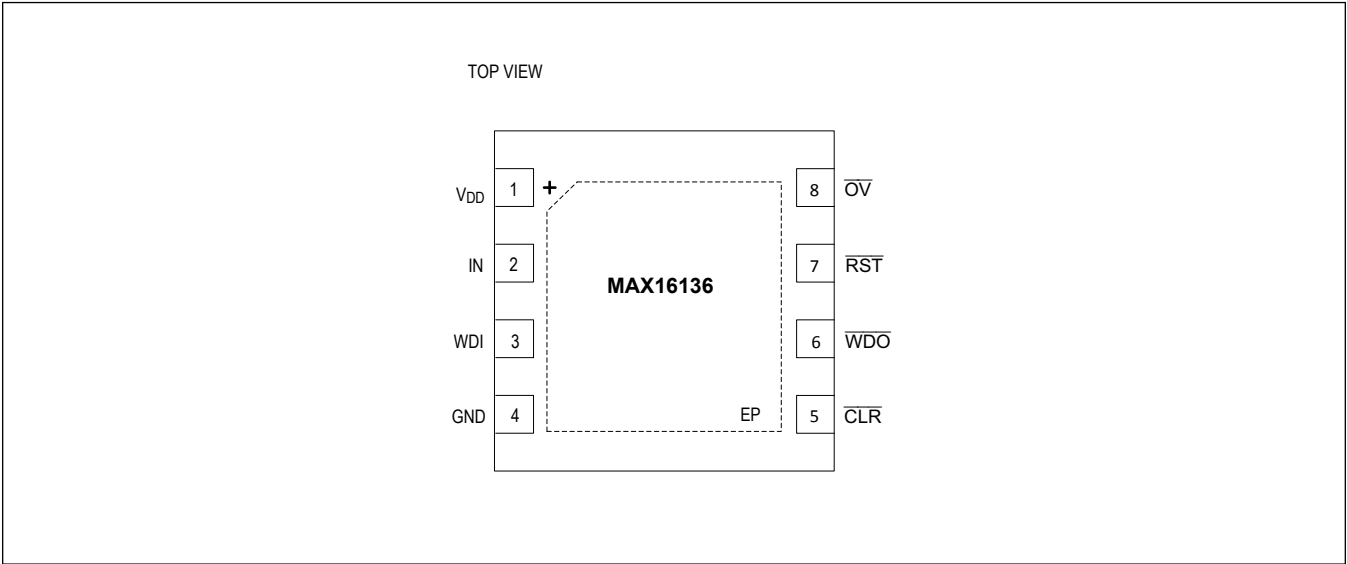
Typical Operating Characteristics (continued)

(V<sub>DD</sub> = 1.71V to 5.5V, T<sub>A</sub> = -40°C to +125°C, Typical values are at V<sub>DD</sub> = 3.3V, unless otherwise specified.)



Pin Configuration

8 TDFN



Pin Description

PIN	NAME	FUNCTION
1	V <sub>DD</sub>	Supply Input. Bypass V <sub>DD</sub> to ground with a 0.1μF capacitor.
2	IN	Monitoring Input. IN monitors for undervoltage/overvoltage faults with respect to nominal input threshold. When V <sub>IN</sub> falls outside the the undervoltage/overvoltage thresholds window, $\overline{\text{RST}}$ asserts and stays asserted for reset timeout period after V <sub>IN</sub> falls within undervoltage/overvoltage thresholds window.

## Pin Description (continued)

PIN	NAME	FUNCTION
3	WDI	Watchdog Input. The internal watchdog timer clears to zero on the falling edge of WDI or when $\overline{\text{RST}}$ goes high. If WDI sees another falling edge within the factory-trimmed watchdog window, $\overline{\text{WDO}}$ will remain de-asserted. Transitions outside this window, either faster or slower, will cause $\overline{\text{WDO}}$ to pulse low. WDI must not be left floating. Connect to ground with 100k $\Omega$ resistor to ensure proper device operation. See <a href="#">Window Watchdog Operation</a> for more detail.
4	GND	Ground
5	$\overline{\text{CLR}}$	Clear Input. Pull $\overline{\text{CLR}}$ low for a pulse duration of $t_{\text{CLR}}$ to clear the overvoltage fault output at ( $\overline{\text{OV}}$ ) after the overvoltage condition is removed. $\overline{\text{CLR}}$ has a 50k $\Omega$ internal pull up to $V_{\text{DD}}$ .
6	$\overline{\text{WDO}}$	Open-Drain Watchdog Output. $\overline{\text{WDO}}$ asserts low for 50ms when two consecutive falling transitions on WDI are shorter than $t_{\text{WD}_F}$ . $\overline{\text{WDO}}$ asserts low for 100ms when two consecutive falling transitions on WDI is longer than $t_{\text{WD}_S}$ . See <a href="#">Window Watchdog Operation</a> for more detail.
7	$\overline{\text{RST}}$	Open-Drain Reset Output. $\overline{\text{RST}}$ asserts low when $V_{\text{IN}}$ falls outside of the undervoltage/overvoltage threshold's window. The reset output deasserts after the reset timeout period when $V_{\text{IN}}$ enters the undervoltage/overvoltage threshold's window.
8	$\overline{\text{OV}}$	Overvoltage Fault Output. $\overline{\text{OV}}$ latches low when the voltage at IN exceeds the overvoltage threshold setting. To clear the latch, pull $\overline{\text{CLR}}$ low for $t_{\text{CLR}}$ pulse width duration.
-	EP	Exposed pad. Connect EP to GND to improve heat dissipation capability. Add thermal vias below the exposed pad.

The diagram illustrates the internal architecture of the MAX16136. Key components include:

- Inputs:**  $\overline{\text{CLR}}$ ,  $\text{IN}$ ,  $\text{VDD}$ ,  $\text{VREF}$ ,  $\text{WDI}$ , and  $\text{GND}$ .
- Internal Blocks:**
  - OV LATCH BLOCK:** Receives input from the  $\text{IN}$  pin and the  $\text{OV}$  pin.
  - OV and UV Comparators:** Two comparators that compare the  $\text{IN}$  pin voltage against  $\text{VREF}$  and  $\text{VDD}$  to detect overvoltage (OV) and undervoltage (UV) conditions.
  - AND Gate:** Combines the outputs of the OV and UV comparators.
  - RESET TIMEOUT PERIOD:** A timer block that generates a reset signal when the AND gate output is active.
  - WINDOW WATCHDOG TIMER:** A timer block that generates a watchdog signal when the reset timeout period expires.
  - TRANSITION DETECTOR:** A block that detects transitions in the  $\text{WDI}$  input and triggers the window watchdog timer.
- Outputs:**  $\text{OV}$ ,  $\text{RST}$ , and  $\text{WDO}$ .
- External Components:**
  - A resistor connected to  $\text{VDD}$  and the  $\text{CLR}$  pin.
  - A resistor connected to  $\text{VDD}$  and the  $\text{IN}$  pin.
  - A resistor connected to  $\text{VDD}$  and the  $\text{WDI}$  pin.
  - A capacitor connected to  $\text{VDD}$  and  $\text{GND}$ .
  - Two NPN transistors connected to the  $\text{RST}$  and  $\text{WDO}$  pins, respectively, with their emitters to  $\text{GND}$ .



## Detailed Description

The MAX16136 is a high-accuracy supervisory circuit that monitors a single system-supply voltage for factory-trimmed undervoltage/overvoltage window-threshold settings between  $\pm 4\%$  to  $\pm 11\%$  input tolerance. A reset output (RST) asserts when the input voltage exceeds the selected tolerance levels and stays asserted for the reset timeout period after the supply voltage falls back within the selected undervoltage/overvoltage window threshold. An overvoltage fault output (OV) latches low when the supply voltage exceeds the overvoltage threshold level. The latched output can be cleared by pulling the clear input (CLR) low for  $t_{CLR}$  pulse duration. See the [Electrical Characteristics](#) for more detail.

The MAX16136 includes a window-watchdog timer circuit that monitors microprocessor or microcontroller activity ([Figure 1](#)). During normal operation, the microprocessor or microcontroller toggles the watchdog input (WDI) low within the factory-set window of operation. If the watchdog input is strobed faster than the fast watchdog timeout period, the watchdog output (WDO) pulses low for 50ms (typ). If the watchdog input is strobed slower than the slow watchdog timeout period, the watchdog output pulses low for 100ms (typ).

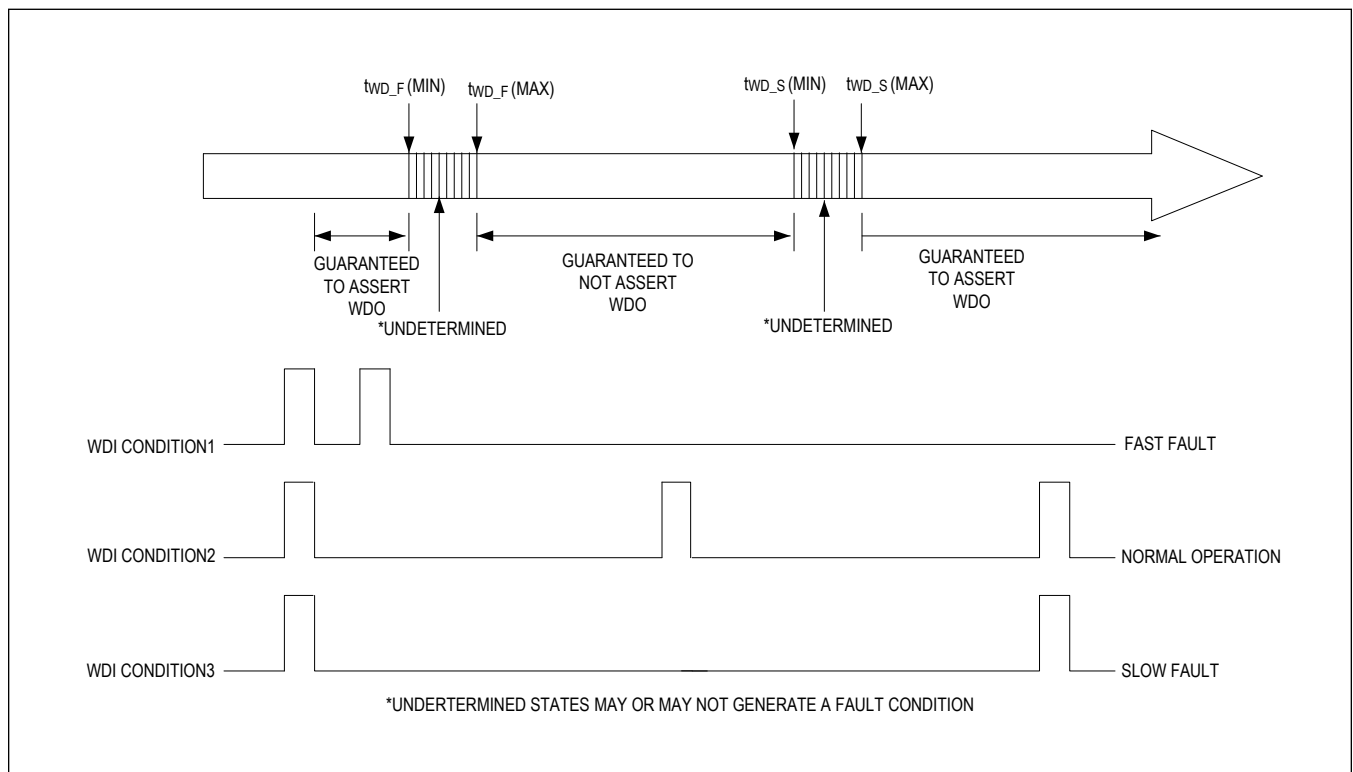


Figure 1. MAX16136 Detailed Watchdog Input Timing Relationship

## Nominal Input Threshold Range

The MAX16136 offers a wide range of thresholds for monitoring system voltages from 0.5V to 5V in approximately 20mV increments. Each threshold is factory-trimmed for undervoltage/overvoltage threshold-window between  $\pm 4\%$  to  $\pm 11\%$  symmetrically with respect to nominal input threshold voltage. Contact Maxim sales for options not listed in the [Ordering Information](#) table.

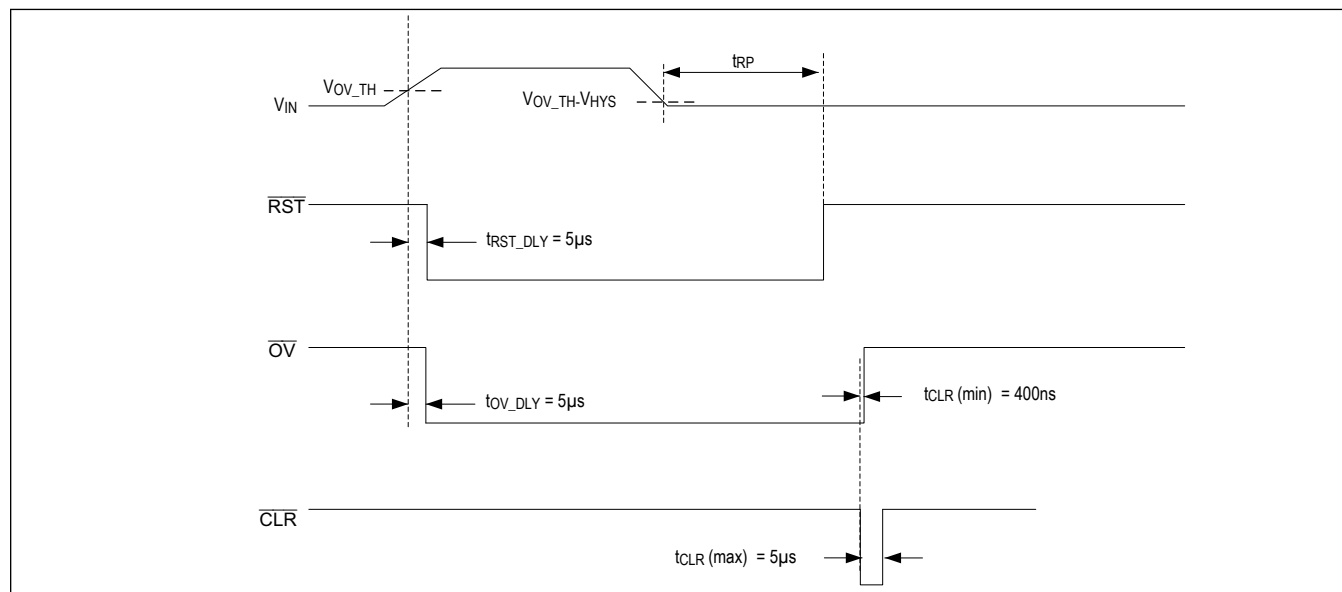
## Undervoltage/Overvoltage Thresholds

The MAX16136 monitors supply voltage for undervoltage/overvoltage faults with respect to nominal input voltage with  $\pm 1\%$  accuracy over the operating temperature and supply ranges. The undervoltage and overvoltage thresholds are factory-trimmed from  $\pm 4\%$  to  $\pm 11\%$  in  $\pm 1\%$  increments. Contact Maxim for threshold not listed in the [Ordering Information](#) table.

The MAX16136's monitoring input (IN) features undervoltage/overvoltage threshold hysteresis that provides immunity to short input transients. The input hysteresis is factory-set to either 0.25% or 0.5% and is applicable to both undervoltage and overvoltage thresholds. Contact Maxim for hysteresis option not listed in the [Ordering Information](#) table.

The MAX16136 features an open-drain, active-low overvoltage fault output ( $\overline{\text{OV}}$ ) that asserts low  $5\mu\text{s}$  after input voltage exceeds the overvoltage threshold level.  $\overline{\text{OV}}$  is a latched output and can be cleared by pulling  $\overline{\text{CLR}}$  input low for  $t_{\text{CLR}}$  pulse width duration. See [Figure 2](#) for more detail.

The MAX16136 provides an active-low input ( $\overline{\text{CLR}}$ ) to clear the latched overvoltage fault output ( $\overline{\text{OV}}$ ). Pulling  $\overline{\text{CLR}}$  low for  $t_{\text{CLR}}$  pulse duration clears the overvoltage fault after the overvoltage condition is removed. See the [Electrical Characteristics](#) for more detail. The MAX16136 ignores any activity on  $\overline{\text{CLR}}$  input while the device is in an overvoltage condition. See [Figure 2](#) for the timing diagram.



**Note:** Pulling  $\overline{\text{CLR}}$  low for a pulse width duration ( $t_{\text{CLR}}$ )  $> 5\mu\text{s}$  asserts  $\overline{\text{RST}}$ . A consecutive series of pulses on  $\overline{\text{CLR}}$  with a low pulse width duration of  $t_{\text{CLR}} > 5\mu\text{s}$  must be separated by a high pulse width duration  $> t_{\text{RP}}$  for a valid reset output.

The MAX16136 offers a window-watchdog circuit for monitoring the microprocessor or microcontroller activity. During normal operation the microprocessor or microcontroller repeatedly toggles the watchdog input WDI [low](#). If the signal on WDI has two consecutive falling edges too close to each other ( $t_{WD} < t_{WD\_F}$ ), the watchdog output, WDO pulses low for 50ms. If the signal on WDI has two consecutive falling edges too far apart ( $t_{WD} > t_{WD\_S}$ ) the watchdog output pulses low 100ms. Two falling transitions within fast watchdog timeout and slow watchdog timeout window clears the watchdog timer and keeps the watchdog output deasserted. See [Figure 3](#), [Figure 4](#), [Figure 5](#), and [Table 1](#) for more detail. Contact Maxim for a watchdog timeout not listed in [Table 1](#).

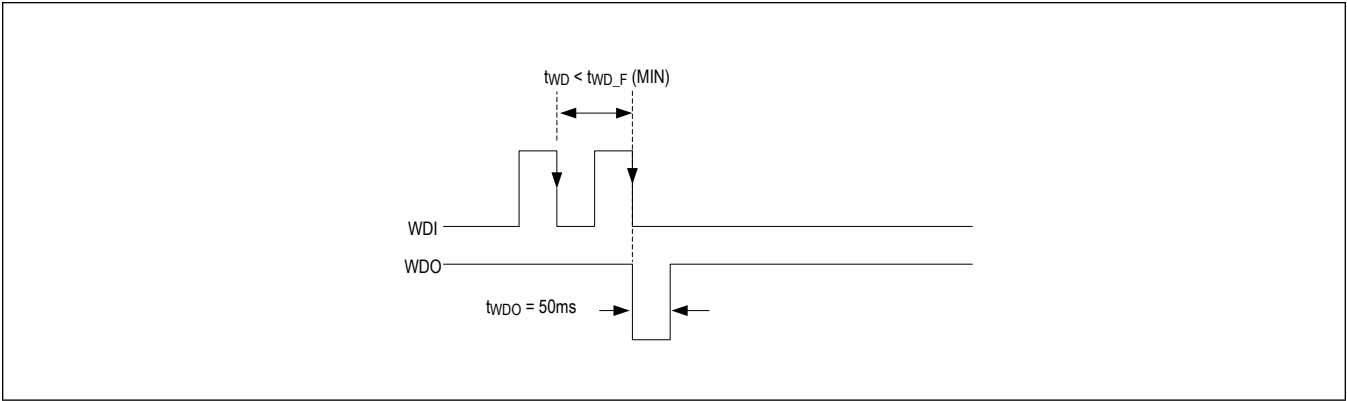


Figure 3. Fast Watchdog Fault Timing Characteristics

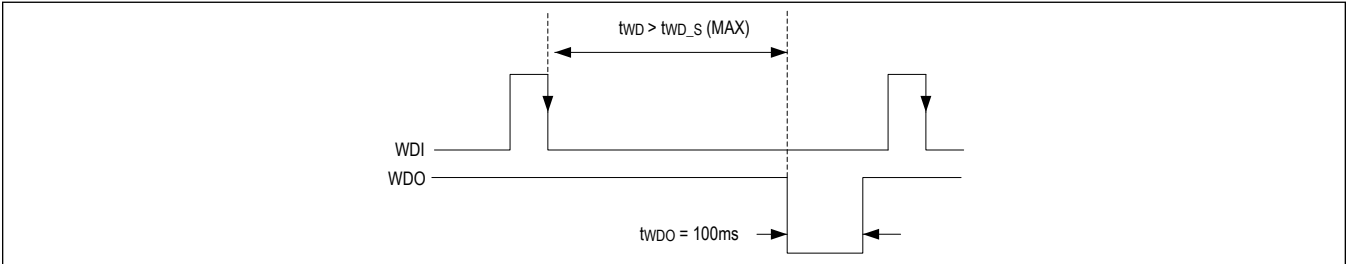


Figure 4. Slow Watchdog Timing Characteristics

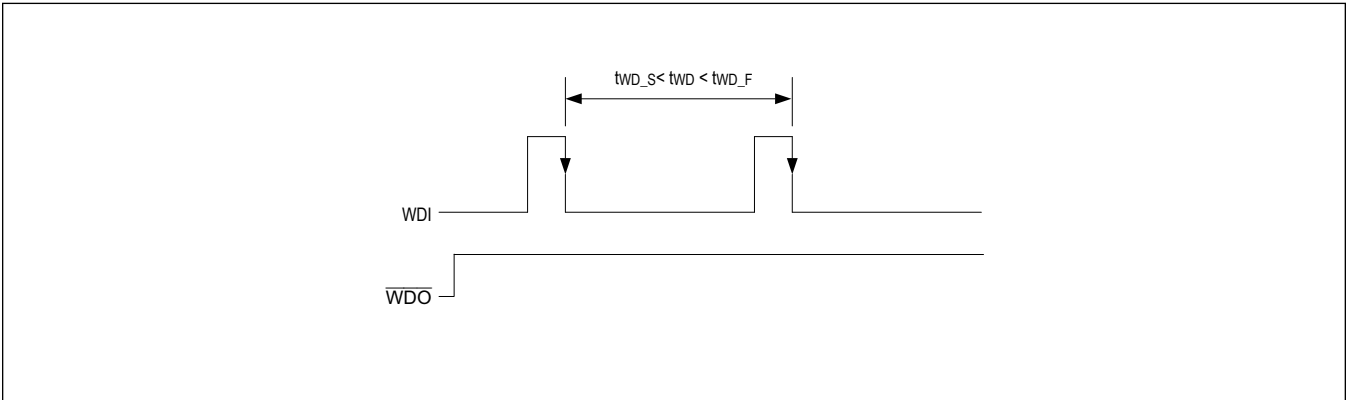


Figure 5. Normal Watchdog Operation (No Watchdog Output Pulse)

Table 1. Window Watchdog Available Options

OPTIONS	FAST WD TIMEOUT PERIOD (ms)	SLOW WD TIMEOUT PERIOD (ms)
1	1	10
2	2	20
3	4	40
4	8	80
5	16	160
6	32	320
7	64	640

**Table 1. Window Watchdog Available Options (continued)**

8	128	1280
9	256	2560
10	512	5120
11	1024	10240
12	2048	20480
13	4096	40960

**Reset Output**

The MAX16136 offers an active-low, open-drain reset output ( $\overline{\text{RST}}$ ) that asserts low when the supply voltage falls outside of the undervoltage/overvoltage window threshold. The reset output deasserts after the selected reset timeout period when the supply voltage falls back within the undervoltage/overvoltage window threshold. See [Table 2](#) for more details. Contact Maxim for reset timeout period options not listed in [Table 2](#).

**Table 2. Reset Timeout Period Available Options**

OPTIONS	RESET TIMEOUT PERIOD (ms)
1	1
2	5
3	10
4	15
5	20
6	50
7	100
8	150
9	200
10	250
11	300
12	500
13	750
14	1000
15	1500

## Applications Information

### Setting Input Thresholds

The MAX16136 monitors a system supply voltage for undervoltage/overvoltage window-threshold. Depending on the system supply tolerance requirement, the undervoltage/overvoltage thresholds can be factory-trimmed from  $\pm 4\%$  to  $\pm 11\%$ . The tolerance setting is symmetrical with respect to the selected nominal input threshold voltage ( $V_{IN\_NOM}$ ). A detailed calculation of how to determine the undervoltage/overvoltage threshold levels with  $\pm 1\%$  threshold accuracy for  $3.3V \pm 5\%$  supply voltage is presented here:

$$V_{IN\_NOM} = 3.3V$$

$$TOL = \pm 5\%$$

$$V_{UVTH} = V_{IN\_NOM} (1 - 5\%) = 3.3V (1 - 0.05) = 3.3V - 0.165V = 3.135V$$

$$V_{OVTH} = V_{IN\_NOM} (1 + 5\%) = 3.3V (1 + 0.05) = 3.3V + 0.165V = 3.465V$$

Where  $V_{IN\_NOM}$  is the selected nominal input threshold voltage, TOL is the input tolerance,  $V_{UVTH}$  is undervoltage threshold voltage, and  $V_{OVTH}$  is the overvoltage threshold voltage.

The MAX16136 monitors the supply voltage with  $\pm 1\%$  accuracy over the operating temperature and supply range. The accuracy range for the  $3.3V \pm 5\%$  is shown below:

$$V_{UVTH\_A} = V_{UVTH} (1 \pm 1\%) = 3.135V (1 \pm 0.03135V) = 3.135V \pm 0.03135V$$

$$V_{OVTH\_A} = V_{OVTH} (1 \pm 1\%) = 3.465V (1 \pm 0.03465V) = 3.465V \pm 0.03465V$$

Where  $V_{UVTH\_A}$  is the undervoltage threshold accuracy range and  $V_{OVTH\_A}$  is the overvoltage threshold accuracy range. See [Figure 6](#) for details.

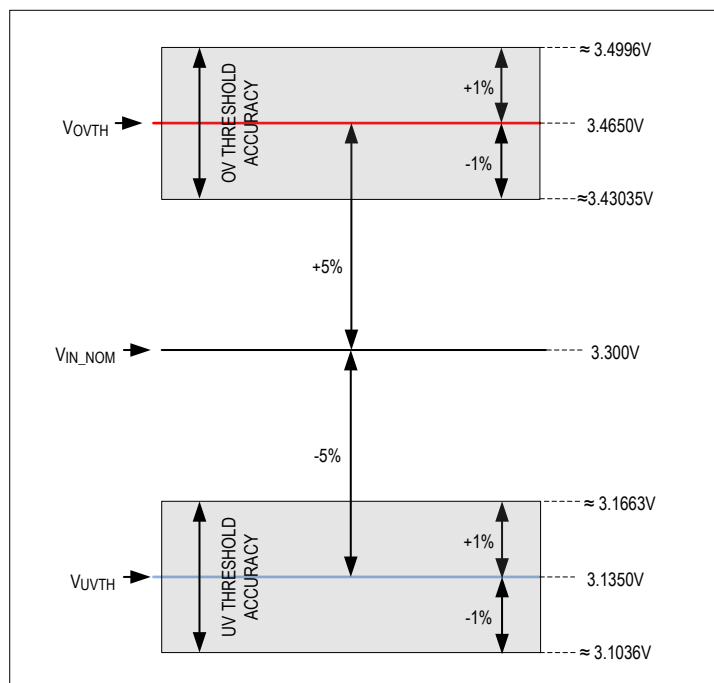


Figure 6. Undervoltage/Overvoltage Threshold Accuracy

Power Supply Bypassing/Noise Immunity

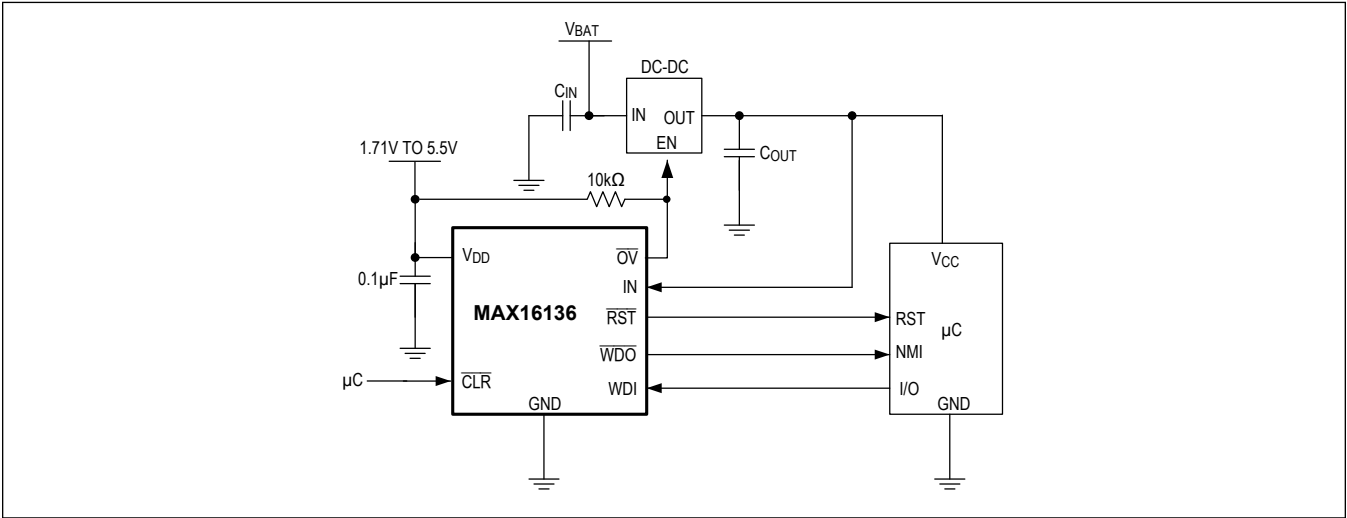
The MAX16136 operates from a 1.71V to 5.5V input supply range. An undervoltage lockout ensures that the outputs are in the correct states when the UVLO is exceeded. Bypass  $V_{DD}$  to ground with a 0.1 $\mu$ F capacitor as close to the device as possible. The additional capacitor improves transient immunity. For proper operation, limit  $V_{DD}$  noise within 200mV peak-to-peak.

Selector Guide Table

Table 3. Selector Guide

PART NUMBER	THRESHOLD VOLTAGE (V)	TOLERANCE (%)	HYSTERESIS (%)	RESET TIMEOUT (ms)	WINDOW WATCHDOG TIMEOUT (ms/ms)
MAX1613600/VY+T	3.3	±4	±0.25	10	8/80
MAX1613601/VY+T	1.0	±4	±0.25	20	32/320
MAX1613602/VY+T	3.3	±4	±0.25	1	16/160

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX1613600/VY+T	-40°C to +125°C	8 TDFN
MAX1613601/VY+T*	-40°C to +125°C	8 TDFN
MAX1613602/VY+T*	-40°C to +125°C	8 TDFN

/V Denotes automotive grade.  
Y Denotes side-wettable package.  
+Denotes a lead(Pb)-free/RoHS-compliant package.  
T = Tape and reel.  
\*Future product—contact factory for availability.

MAX16136

## High-Precision Supervisory ICs with Window Watchdog and Overvoltage Indicator

### Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/19	Initial release	—
1	6/21	Updated General Description, Pin Configuration, and Pin Description; added Table 1 and Table 2	1, 6, 7, 10–14

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