MAX14917

Industrial Octal High-Side Switch

General Description

The MAX14917 has eight high-side switches specified to deliver up to 700mA (min) continuous current per channel. The high-side switches have on-resistance of 120mΩ (typ) at 25°C ambient temperature.

The device has an SPI interface that can be daisy chained, allowing communication with multiple MAX14917 devices utilizing a common SPI chip select ($\overline{CS}$). There are also per-channel overload diagnostics provided through the SPI interface. Two watchdog timers provide an additional safety check of the master-to-device connectivity.

The MAX14917 features a 4 x 4 LED cross-bar matrix, which provides a visual indication of channel status and overload conditions for each channel, and an integrated line-to-ground and line-to-line surge protection provides robustness to the electrical stress as per IEC 61000-4-5 and requires only one TVS on V_{DD}. The MAX14917 is available in a compact 48-pin 6mm x 6mm FC2QFN package.

Applications

- Industrial Digital Outputs
- PLC Systems
- Factory Automation
- Building Automation
- Industrial IoT

Benefits and Features

- Robust Solutions
  - 65V Absolute Maximum Supply Range
  - CRC Error Checking on the SPI Interface
  - Watchdog Timers for Monitoring SPI and SYNCH
  - Per Channel Overload Diagnostic and Protection
  - Loss of V_{DD} or GND Protection
  - Thermal Shutdown Protection
  - Integrated ±1kV / 42Ω IEC 61000-4-5 Surge Protection
  - ±7kV / IEC 61000-4-2 Contact Discharge Method
  - ±30kV / IEC 61000-4-2 Air Discharge Method
  - -40°C to +125°C Operating Ambient Temperature
- Reduces Power and Heat Dissipation
  - 120mΩ (typ) On-Resistance at T_A = 25°C
  - 2.5mA (typ) Supply Current
  - Accurate Output Current Limiting
- Flexible
  - SYNCH Input for Simultaneous Update of Switches
  - LED Driver Matrix for 16 LEDs, Powered from 3.0V to 36V
  - Internal Clamps for Fast Inductive Load Demagnetization
  - Daisy Chainable SPI
  - Flexible Logic Voltage Interface from 2.5V to 5.5V
  - Pin Compatible with the MAX14915 and MAX14916 in Daisy-Chain Configuration
- Compact 6mm x 6mm FC2QFN Package

***Ordering Information* appears at end of datasheet.**

19-100741; Rev 0; 2/20

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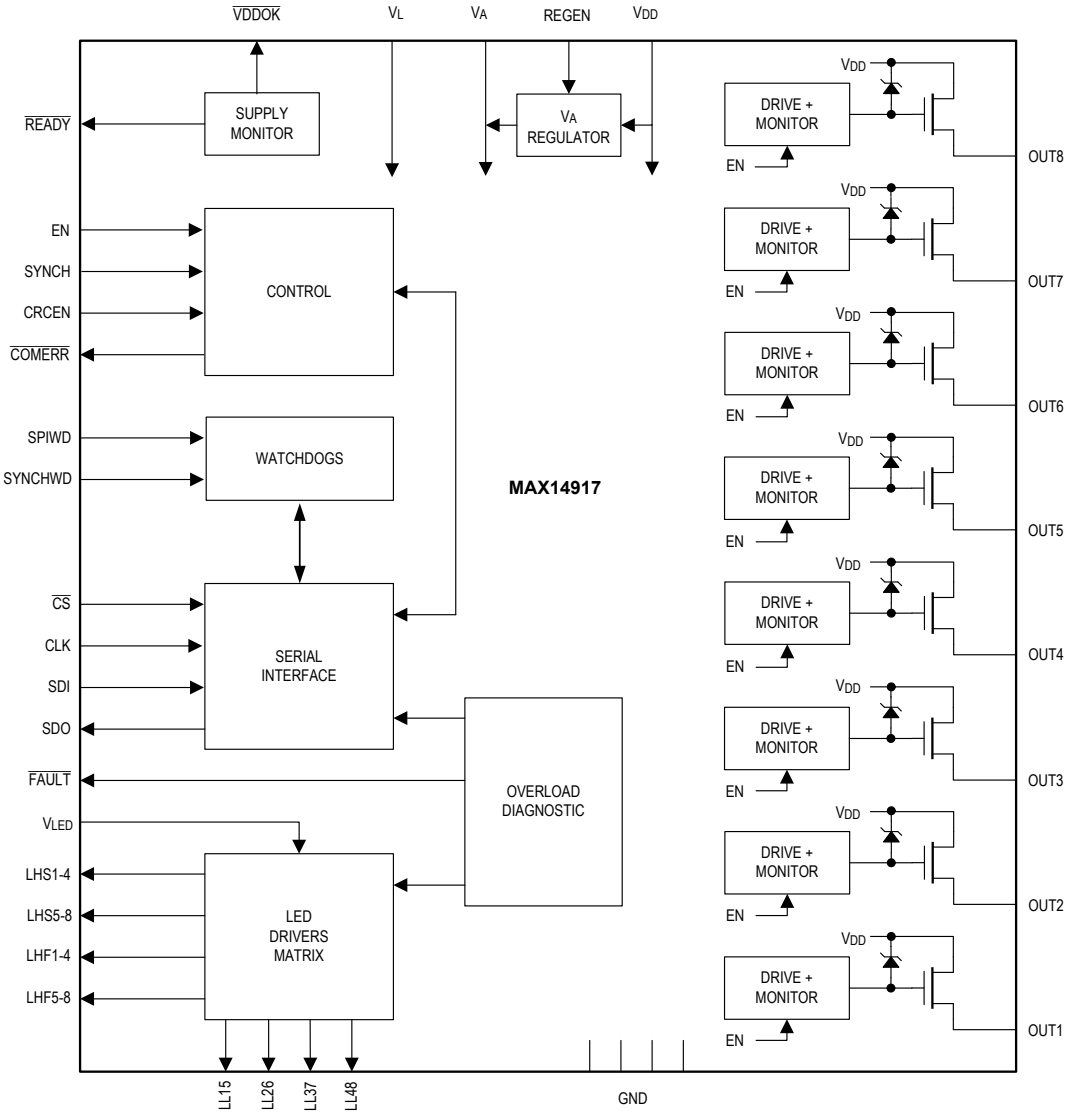
Simplified Block Diagram



Absolute Maximum Ratings

V_{DD} ..... -0.3V to +65V
OUT_ ..... (V_{DD} - 49V) to (V_{DD} + 0.3V)
V_A, V_L ..... -0.3V to +6V
SDO, $\overline{READY}$, $\overline{COMERR}$ ..... -0.3V to (V_L + 0.3V)
$\overline{REGEN}$ ..... -0.3V to +6V
$\overline{FAULT}$ ..... -0.3V to +6V
SDI, $\overline{CS}$, CLK, EN, SYNCH, CRCEN, SPIWD, SYNCHWD . -0.3V to +6V
V_{LED} ..... -0.3V to +70V
LH_, LL_, $\overline{VDDOK}$ ..... -0.3V to (V_{LED} + 0.3V)
OUT_ Load Current ..... Internally Limited
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 50mW/°C above +70°C) 3900mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... 260°C

Note 1: All voltages relative to GND.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

48 F2CQFN

Package Code	F486A6F+1
Outline Number	21-100232
Land Pattern Number	90-100077
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	20.5°C/W
Junction to Case (θ_{JC})	0.39°C/W (bottom)

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD} = +10V to +36V, V_{LED} = +3.0V to 36V, V_A = +3.0V to +5.5V, V_L = +2.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{LED} = 24V, V_A = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Characteristics / SUPPLY						
V_{DD} Supply Voltage	V_{DD}		10		36	V
V_{DD} Supply Current	I_{DD}	EN = high, OUT_ switches on, no load, V_A and V_L supplied externally		2	3	mA
		EN = low			3	
V_{DD} UVLO Rise Threshold	$V_{DD\_UVLO\_R}$	V_{DD} rising			9.6	V
V_{DD} UVLO Fall Threshold	$V_{DD\_UVLO\_F}$	V_{DD} falling, OUT_ disabled	7.9			V
V_{DD} UVLO Hysteresis	$V_{DD\_UVLO\_H}$			0.35		V
V_{DD} Warn Fall Threshold	$V_{DD\_WARN\_F}$	V_{DD} falling, $\overline{VDDOK}$ pin set Hi-Z	12	13		V
V_{DD} Good Rise Threshold	$V_{DD\_GOOD\_R}$	V_{DD} rising, $\overline{VDDOK}$ pin set low			17	V

Electrical Characteristics (continued)

(V_{DD} = +10V to +36V, V_{LED} = +3.0V to 36V, V_A = +3.0V to +5.5V, V_L = +2.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{LED} = 24V, V_A = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Good Fall Threshold	$V_{DD\_GOOD\_F}$	V_{DD} falling	15			V
V_{DD} Good Hysteresis	$V_{DD\_GOOD\_H}$			0.4		V
V_{DD} POR Rise Threshold	$V_{DD\_POR\_R}$	V_{DD} rising			6.8	V
V_{DD} POR Falling Threshold	$V_{DD\_POR\_F}$	V_{DD} falling	5.6			V
V_A Supply Voltage	V_A	When V_A is supplied externally; REGEN = GND.	3.0		5.5	V
V_A Supply Current	I_{VA}	EN = high, OUT_ are turned on, no load, no LEDs connected		0.5	0.85	mA
V_A Undervoltage Lockout Threshold	V_{A_UV}	V_{DD} = 24V, V_A rising	2.45		2.9	V
V_A Undervoltage Lockout Hysteresis	V_{A_UVHYST}	V_{DD} = 24V		0.1		V
V_L Supply Voltage	V_L		2.5		5.5	V
V_L Supply Current	I_{VL}	All logic inputs high or low		13	34	µA
V_L POR Threshold	V_{VL_POR}	V_L falling	0.87	1.32	1.5	V
DC Characteristics / SWITCH OUTPUTs (OUT_)						
On-Resistance	R_{OUT_HS}	$I_{OUT\_}$ = -600mA		120	250	mΩ
Current Limit	I_{LIM}		0.7	1	1.3	A
Off Leakage Current	I_{LKG}	Switch off, OUT_ = 0V	-10		+10	µA
DC Characteristics / LINEAR REGULATOR						
Output Voltage	V_A	REGEN open, C_{LOAD} = 1µF, 0mA < I_{VA} < 20mA	3.0	3.3	3.6	V
Current Limit	I_{CL_VA}	REGEN open	25			mA
Short Current	I_{SHRT_VA}	REGEN open, V_A = 0V			60	mA
REGEN Threshold	VT_{REGEN}		0.2			V
REGEN Leakage Current	I_{LK_REGEN}	REGEN = 0V	-50			µA
DC Characteristics / LOGIC I/O						
Input Voltage High	V_{IH}		0.7 x V_L			V
Input Voltage Low	V_{IL}				0.3 x V_L	V
Input Threshold Hysteresis	V_{IHYS}			0.11 x V_L		V
Input Pulldown Resistor	R_{IN_PD}	All logic input pins except SYNCH and $\overline{CS}$		200		kΩ
Input Pullup Resistor	R_{IN_PU}	SYNCH and $\overline{CS}$		200		kΩ
Output Logic-High (SDO)	V_{OH}	I_{LOAD} = -5mA	V_L - 0.6			V
Output Logic-Low	V_{OL}	I_{LOAD} = +5mA			0.33	V

Electrical Characteristics (continued)

(V_{DD} = +10V to +36V, V_{LED} = +3.0V to 36V, V_A = +3.0V to +5.5V, V_L = +2.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{LED} = 24V, V_A = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDO Output Tristate Leakage	I_{L_SDO}	$\overline{CS}$ = high	-1		+1	µA
DC Characteristics / OPEN-DRAIN OUTPUT ($\overline{FAULT}$, $\overline{COMERR}$, $\overline{READY}$, $\overline{VDDOK}$)						
READY Output Logic-High	V_{ODH}	I_{LOAD} = -5mA	V_L - 0.6			V
Output Logic-Low	V_{ODL}	I_{LOAD} = +5mA			0.33	V
Leakage	I_{ODL}	Open-drain output off, V_{OD} = 5.5V	-1		+1	µA
DC Characteristics / LED Drivers (LH_, LL_)						
LED Supply Voltage	V_{VLED}		3.0		V_{DD}	V
LH Voltage High	V_{OH_LH}	LH = on, V_{LED} = V_{DD}, I_{VLED} = -5mA	V_{LED} - 0.3			V
LH Off Leakage Current	I_{L_LH}	LH_ = off, V_{LED} = 0V			5	µA
LL Output Voltage Low	V_{OH_LL}	LL = on, I_{VLED} = 5mA			0.3	V
LL Off Leakage Current	I_{L_LL}	LL = off, V_{LED} = V_{DD}	-1		+1	µA
DC Characteristics / PROTECTION						
OUT_ Clamp Voltage	V_{CL}	V_{CL} = V_{DD} - V_{OUT}, $I_{OUT\_}$ = -500mA, OUT_ is off	49	56		V
Channel Thermal Shutdown Temperature	T_{JSHDN}	Junction temperature rising. Per channel.		150		°C
Channel Thermal Shutdown Hysteresis	T_{JSHDN_HYST}			15		°C
Chip Thermal Shutdown	T_{CSHDN}	Temperature rising.		150		°C
Chip Thermal Shutdown Hysteresis	T_{CSHDN_HYST}			10		°C
Timing Characteristics / OUT_						
Prop Delay LH	t_{PD_LH}	Delay from rising SYNCH edge to $V_{OUT\_}$ rising to 90%. R_L = 48Ω. V_{DD} = 24V. Figure 2		11	30	µs
Prop Delay HL	t_{PD_HL}	Delay from rising SYNCH edge to $V_{OUT\_}$ falling to 10% of V_{DD}, V_{DD} = 24V, R_L = 48Ω, Figure 2		11	30	µs
Rise Time	t_R	20% to 80% V_{DD}, V_{DD} = 24V, R_L = 48Ω, Figure 2		8		µs
Fall Time	t_F	80% to 20% V_{DD}, V_{DD} = 24V, R_L = 48Ω, Figure 2		8		µs
Timing Characteristics / GLITCH FILTERS						
Pulse Length of Rejected Glitch	t_{FPL_GF}	EN, SYNCH, SPIWD, SYNCHWD, CRCEN	0		80	ns
Passed Pulse Length	t_{FD_GF}	EN, SYNCH, SPIWD, SYNCHWD, CRCEN	300			ns

Electrical Characteristics (continued)

(V_{DD} = +10V to +36V, V_{LED} = +3.0V to 36V, V_A = +3.0V to +5.5V, V_L = +2.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{LED} = 24V, V_A = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Glitch Filter Delay Time	t_{D_GF}	EN, SYNCH		140	300	ns
	t_{D_GFL}	SPIWD, SYNCHWD, CRCEN		290	600	
Timing Characteristics / WATCHDOG						
Watchdogs Timeout Accuracy	t_{WD_ACC}	SPIWD/SYNCHWD = 1	-30		+30	%
Timing Characteristics / LED Matrix						
LED Driver Scan rate	FLED	Update rate for each LED		1		kHz
Timing Characteristics / SPI						
CLK Clock Period	t_{CH+CL}		100			ns
CLK Pulse Width High	t_{CH}		40			ns
CLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to CLK Rise Time	t_{CSS}		40			ns
SDI Hold Time	t_{DH}		10			ns
SDI Setup Time	t_{DS}		10			ns
SDO Propagation Delay	t_{DO}	C_{LOAD} = 10pF, CLK falling edge to SDO stable			30	ns
SDO Rise and Fall Times	t_{FT}			1		ns
$\overline{CS}$ Hold Time	t_{CSH}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSPW}	(Note 3)	40			ns
EMC						
ESD	V_{ESD_C}	OUT_ to GND, IEC 61000-4-2 Contact Discharge		±7		kV
	V_{ESD_A}	OUT_ to GND, IEC 61000-4-2 Air Discharge		±30		
	V_{ESD}	All other pins. Human Body Model (Note 4)		±2		
Surge Tolerance	V_{SURGE}	OUT_ to GND, IEC 61000-4-5 with 42Ω, TVS on V_{DD}. (Note 5)		±1		kV

Note 2: All units are production tested at T_A = +25°C. Specifications over temperature are guaranteed by characterization.

Note 3: Specification is guaranteed by design; not production tested.

Note 4: Bypass V_{DD} pin to GND with 1µF capacitor as close as possible to the device for high ESD protection.

Note 5: At typical application value of V_{DD} = 24V with a TVS protection on V_{DD} to GND.

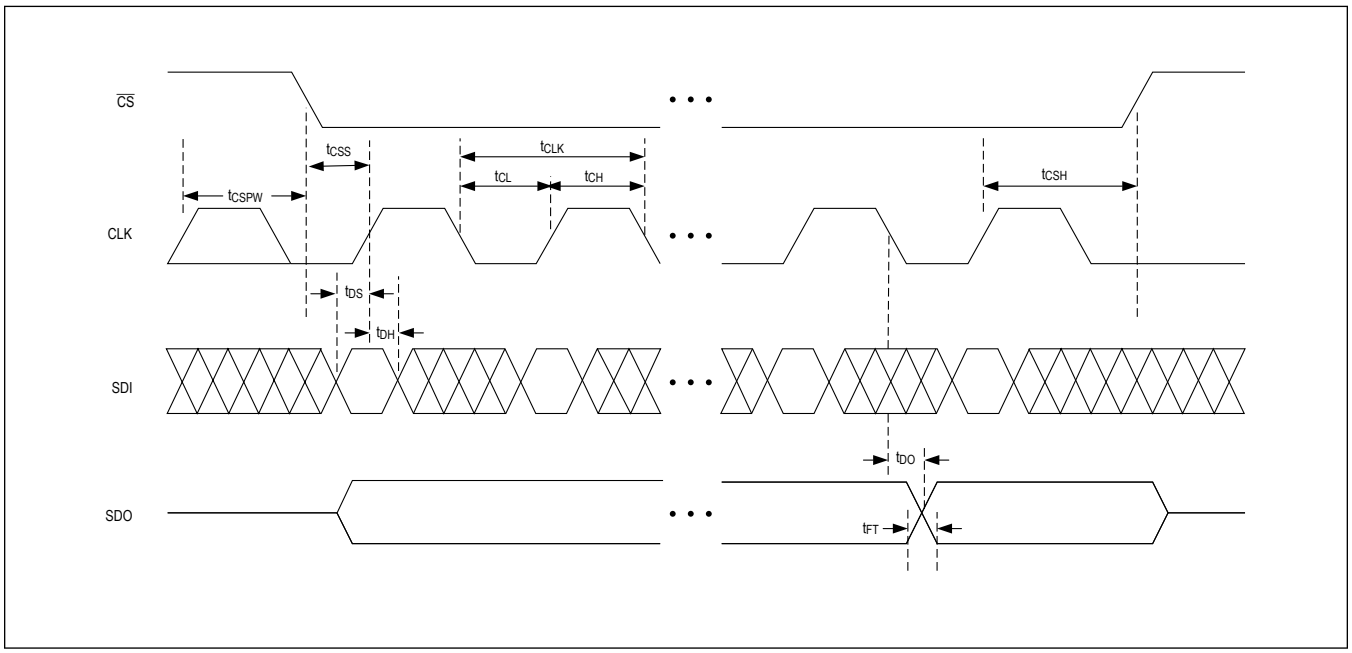


Figure 1. SPI TIming Diagram

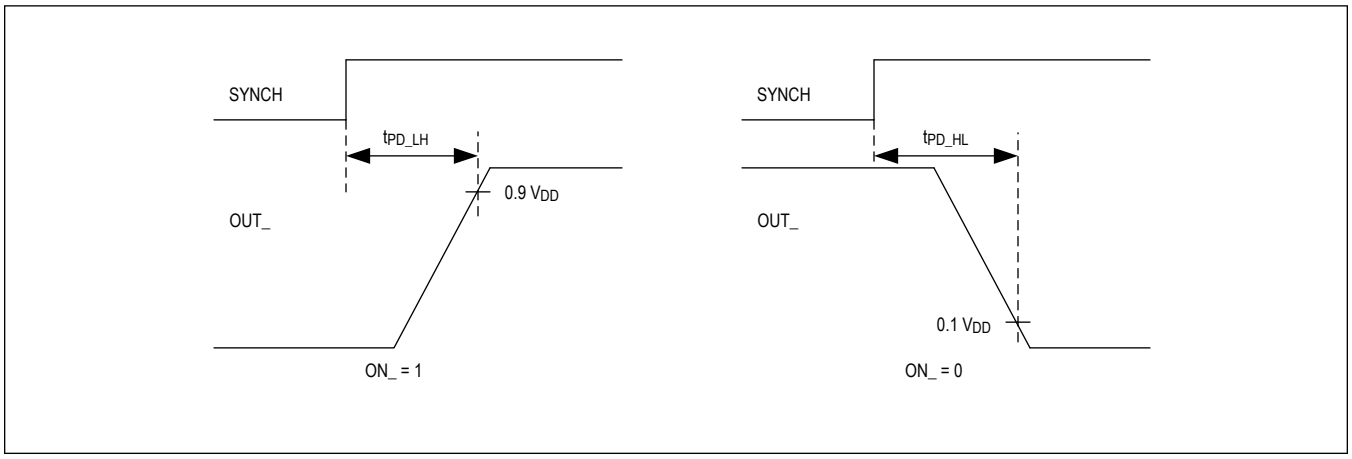
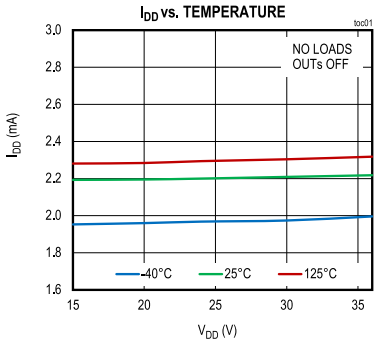
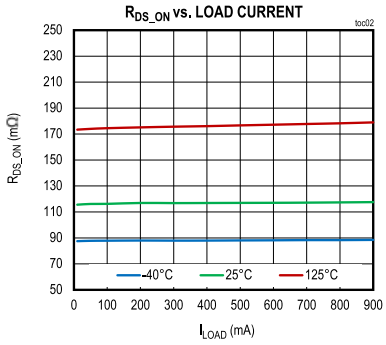


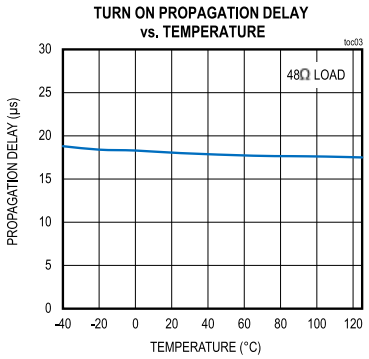
Figure 2. SYNCH to OUT_ Propagation Delay

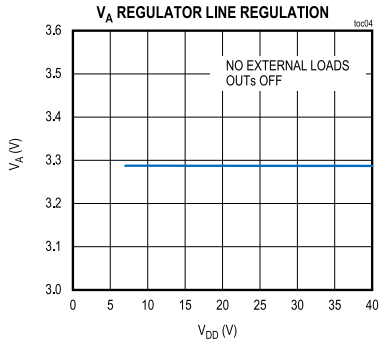
Typical Operating Characteristics

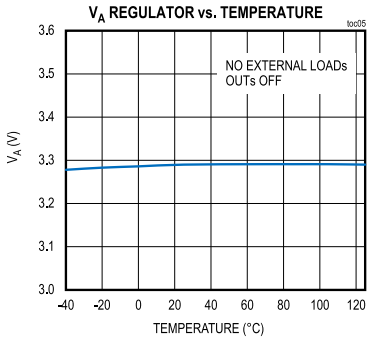
(V_{DD} = +24V, REGEN = open, V_L = +3.3V, T_A = +25°C, unless otherwise noted.)

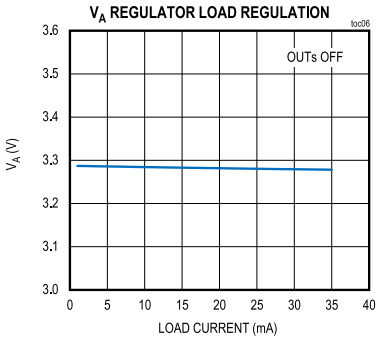


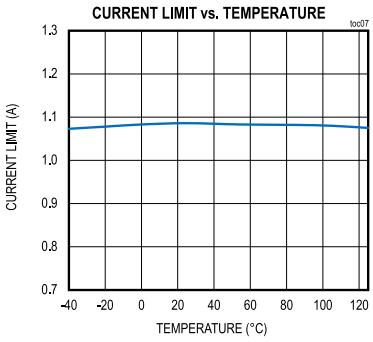






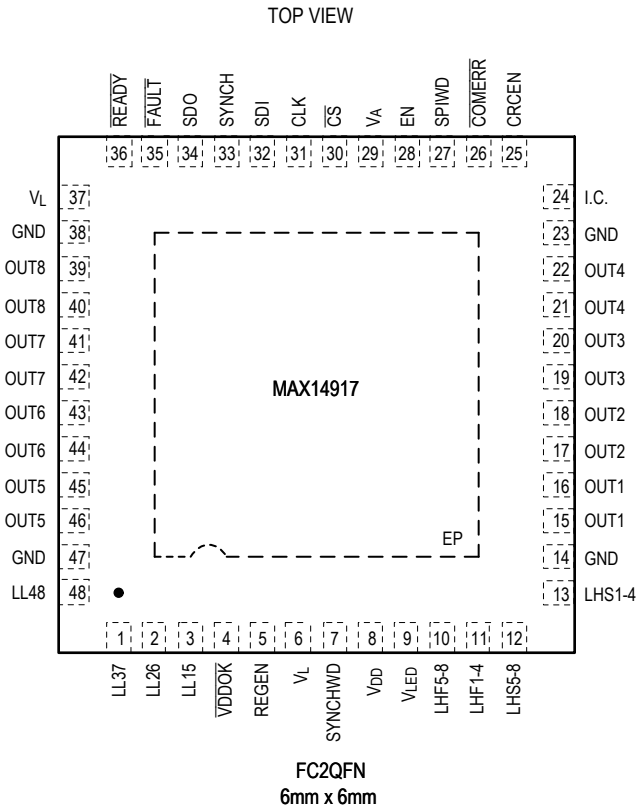






Pin Configuration

MAX14917



Pin Description

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
Power Supply				
EP, 8	V_{DD}	Supply Voltage, Nominally 24V. Connect all V_{DD} together. Bypass V_{DD} to GND through a 1µF capacitor.	GND	Supply
29	V_A	Analog Supply Input. Connect an external 3.0V to 5.5V supply to V_A or use the internal linear regulator by leaving REGEN open. Bypass V_A to GND through a 1µF ceramic capacitor.	GND	Supply
5	REGEN	V_A Regulator Enable Input. Connect REGEN to GND to disable V_A regulator. Leave REGEN open to enable the V_A regulator, which internally supplies V_A with 3.3V.	GND	Supply
14, 23, 38, 47	GND	Ground. Connect all GND pins together.	GND	GND

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
6, 37	V_L	Logic Supply Input. V_L defines the logic levels on all logic interface pins. Bypass V_L to GND through a 100nF ceramic capacitor.	GND	Supply
4	$\overline{VDDOK}$	Active-Low, Open-Drain Logic Output for the V_{DD} Supply. $\overline{VDDOK}$ turns on low when V_{DD} rises above 16V (typ) and turns off when V_{DD} falls below 13V (typ). Connect a LED with a pullup resistor to a voltage between 3.3V and V_{DD}.	GND	Logic
Switch Outputs				
15, 16	OUT1	High-Side Switch Output 1	V_{DD}	Power
17, 18	OUT2	High-Side Switch Output 2	V_{DD}	Power
19, 20	OUT3	High-Side Switch Output 3	V_{DD}	Power
21, 22	OUT4	High-Side Switch Output 4	V_{DD}	Power
45, 46	OUT5	High-Side Switch Output 5	V_{DD}	Power
43, 44	OUT6	High-Side Switch Output 6	V_{DD}	Power
41, 42	OUT7	High-Side Switch Output 7	V_{DD}	Power
39, 40	OUT8	High-Side Switch Output 8	V_{DD}	Power
Control Interface				
28	EN	Enable Logic Input. Drive EN high for normal operation. Drive EN low to disable/three-state all OUT_ drivers. Internal weak pulldown.	V_L	Logic
35	$\overline{FAULT}$	$\overline{FAULT}$ Global Diagnostics Open-Drain Output. The $\overline{FAULT}$ goes low in case of overload or undervoltage conditions. Connect a pullup resistor to V_L.	V_L	Logic
33	SYNCH	SYNCH Input. All eight output switches are updated simultaneously on the rising edge of SYNCH, as determined by the content of the SPI command. The OUT_ states do not change when SYNCH is held low. When SYNCH is high, the output states change immediately after a new SPI command. SYNCH has a weak pullup.	V_L	Logic
25	CRCEN	CRC Enable Select Input. Drive CRCEN high to enable CRC generation and error detection on the serial data. CRC has a weak pulldown.	V_L	Logic
36	$\overline{READY}$	Open-Drain Output. $\overline{READY}$ is passive low when the internal logic chip supply and V_L I/O supply are both higher than their respective UVLO thresholds, indicating that the part is ready for SPI communication. When the internal register supply falls below the UVLO threshold the OUTs are off and $\overline{READY}$ transitions active-high. Connect a pulldown resistor to $\overline{READY}$.	V_L	Logic
26	$\overline{COMERR}$	SPI Error Open-Drain Output. The $\overline{COMERR}$ transistor turns on low when an error occurs during a SPI transaction. Connect a pullup resistor to V_L.	V_L	Logic
7	SYNCHWD	SYNCH Watchdog Enable Logic Input. Set SYNCHWD high to enable the SYNCH watchdog.	V_L	Logic
27	SPIWD	SPI Watchdog Enable Logic Input. Set SPIWD high to enable the SPI watchdog.	V_L	Logic

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
Serial Interface				
32	SDI	Serial Data Input. SPI MOSI data from controller. SDI has a weak pulldown.	V_L	Logic
34	SDO	Serial Data Output. SPI MISO data output to controller.	V_L	Logic
31	CLK	Serial Clock Input. CLK has a weak pulldown.	V_L	Logic
30	$\overline{CS}$	Chip Select Input. $\overline{CS}$ has a weak pullup.	V_L	Logic
LED DRIVER MATRIX				
9	V_{LED}	Supply for LED Drivers. Apply supply voltage of 3.0V to V_{DD}.		
3	LL15	OUTs 1, 5 Status/Fault LED Cathode Output (Open-drain Low-Side). Connect a resistor in series to set the LED current.		
2	LL26	OUTs 2, 6 Status/Fault LED Cathode Output (Open-Drain Low-Side). Connect a resistor in series to set the LED current.		
1	LL37	OUTs 3, 7 Status/Fault LED Cathode Output (Open-Drain Low-Side). Connect a resistor in series to set the LED current.		
48	LL48	OUTs 4, 8 Status/Fault LED Cathode Output (Open-Drain Low-Side). Connect a resistor in series to set the LED current.		
13	LHS1-4	OUTs 1-4 Status LED Anode Outputs (Open-Drain High-Side). Connect a resistor in series to set the LED current.		
12	LHS5-8	OUTs 5-8 Status LED Anode Outputs (Open-Drain High-Side). Connect a resistor in series to set the LED current.		
11	LHF1-4	OUTs 1-4 Fault LED Anode Connections (Open-Drain High-Side). Connect a resistor in series to set the LED current		
10	LHF5-8	OUTs 5-8 Fault LED Anode Connections (Open-Drain High-Side). Connect a resistor in series to set the LED current.		
NO CONNECT				
24	I.C.	Internally Connected. Do not connect.		

Detailed Description

The MAX14917 is an octal high-side switch. The state of the high-side switches (OUT[1:8]) are set through the SPI interface. The OUT_ high-side switches have an on-resistance of 120mΩ (typ) at 700mA and T_A = 25°C, and 250mΩ (max) on-resistance at 700mA and T_A = 125°C. Watchdog timers (SPIWD and/or SYNCHWD) monitor SPI and/or SYNCH activity, and automatically turn the OUT_ pins off in case of missing SPI/SYNCH activity when enabled.

Global OUT Disable

When the EN pin input is low, all OUT_ switches are off independent of the level of the SYNCH input or the ON_ bits in the SPI command (Figure 6). Logic low on the EN pin also allows quick disable of all OUT_ switches in case of emergency. Note: logic high on the EN pin is required for normal operation.

Power-Up and Undervoltage Lockout

When the V_{DD}, V_A, V_L, or V_{INT} supply voltages are under their respective UVLO thresholds, all OUT_ switches are off. V_{INT} is an internal supply for the registers and logic that is derived from the V_A or V_{DD} supply.

When the V_{DD} supply or V_A supply rises, the internal logic supply (V_{INT}) rises. If V_L and V_{INT} are both above their UVLO thresholds, the chip is ready for communication and the $\overline{READY}$ pin becomes passive low to indicate that the part is ready to communicate through the SPI interface.

When V_{DD} rises above $V_{DD\_GOOD\_R}$ the $\overline{VDDOK}$ pin is turned active-low, indicating that the V_{DD} supply is high enough so the OUT_ switches can be operated normally.

When V_{DD} falls below 13V (typ) the $\overline{VDDOK}$ is turned high, but all the OUT_ switches continue operate normally until V_{DD} falls below the $V_{DD\_UVLO\_F}$ threshold. All OUT_ switches are off until V_{DD} reaches the $V_{DD\_GOOD\_R}$ threshold again as shown in Figure 3.

The $\overline{READY}$ and $\overline{VDDOK}$ pins are always active, but the $\overline{FAULT}$ pin does not signal supply conditions.

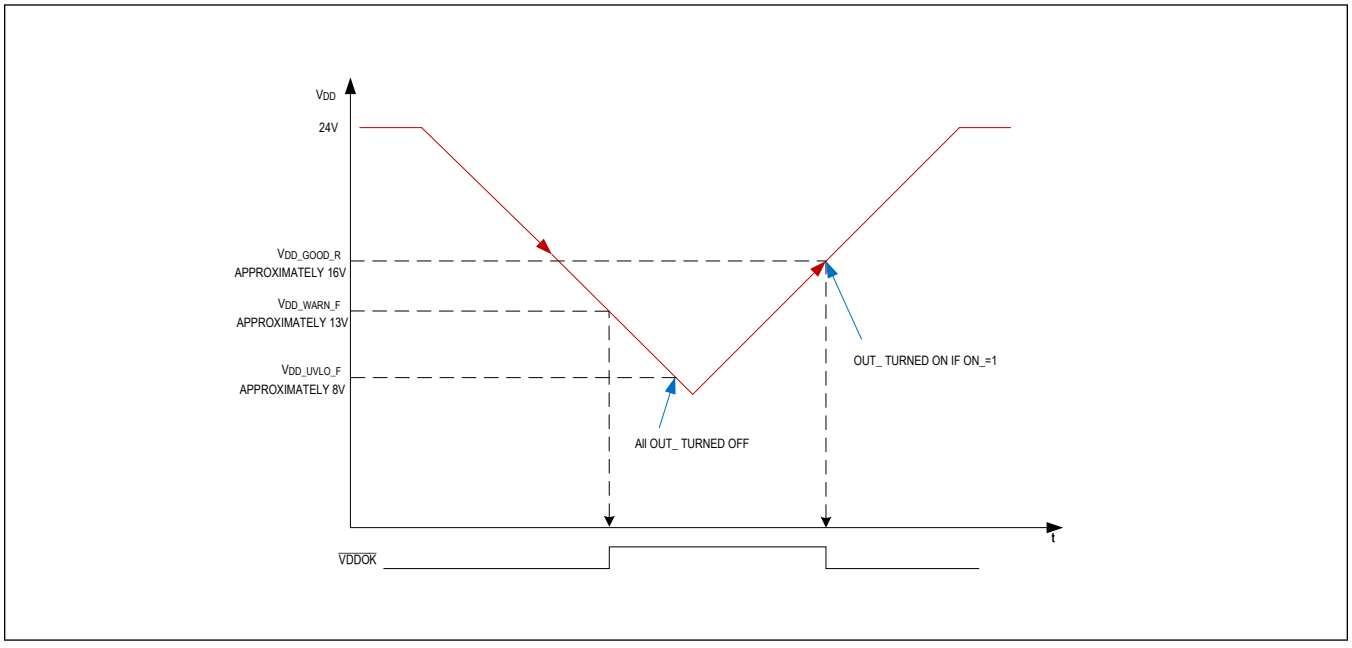


Figure 3. V_{DD} Supply Monitoring

Watchdog

The MAX14917 provides two watchdog timers to monitor activity: one on the SPI interface and the other on the SYNCH pin. SPIWD logic high input enables SPI watchdog functions and the SYNCHWD logic high input enables the SYNCH watchdog function.

- The SPI watchdog timer monitors clock activity on the CLK and inputs. At least one valid SPI cycle must be detected in the watchdog-timeout period. This means that the CLK input must have a multiple of 8 clock-cycles during a low period.
- The SYNCH pin watchdog checks if SYNCH is stuck low. At least a 1µs SYNCH pin high level must be present in the watchdog-timeout period. Driving the SYNCH pin high if SYNCH is not used ensures that the SYNCH watchdog is disabled.

If either watchdog criteria is not met, all OUT_ switches are automatically turned off. The watchdog timeout is 1.2s (typ). Note: the $\overline{FAULT}$ pin does not indicate the watchdog-timeout error. The CMERR bit is visible only on the second byte if CRC is enabled (CRCEN pin is high). If CRC is not enabled, the second byte is not reported and CMERR is not signaled through SPI, as shown in Figure 7 and Figure 9.

Chip Thermal Protection

When the chip temperature rises to above the thermal shutdown threshold of 150°C, the chip enters shutdown protection and all overloaded OUT switches are kept off until chip temperature drops below 140°C.

If an overload occurs on the V_A regulator or on the LED matrix, i.e., if the chip temperature rises above 165°C due to a short, then the V_A regulator and all OUT switches, as well as the LED matrix are shut down to prevent chip damage. In this condition, the $\overline{FAULT}$ pin output is driven low. All F_ bits in the SPI SDO data stream are set to 1. When the chip temperature then falls by the hysteresis amount, the V_A regulator turns on, and the LED matrix and OUT switches are restored to normal operation.

Channel Thermal Management

Every OUT switch temperature is constantly monitored. If the temperature of a switch rises above the thermal shutdown threshold of 150°C (typ), that OUT_ is automatically turned off for protection. After the temperature drops by 15°C, the OUT_ is turned on again. When an OUT_ turns off due to thermal shutdown, its associated F_ bit in the SDO stream and the $\overline{FAULT}$ pin is driven low.

Current Limiting

Each high-side switch features active current limiting. When the load current exceeds 1A (typ), the load current is limited by the high-side switch. If the load current exceeds the current limit, the voltage across the high-side FET switch increases and the temperature of the FET increases in accordance with the FET power dissipation. Increase of the switch temperature generally leads to thermal shutdown of that OUT switch.

Lamp Load Turn On

Incandescent lamps initially draw high currents while their filament is cold, then this turn-on current reduces as the filament heats up. The MAX14917 automatically detects the presence of a lamps loads. When a lamp load is detected, the overload signaling is masked for a duration of 200ms (typ).

LED Drivers

The 4x4 LED driver crossbar matrix offers an efficient configuration for driving up to 16 LEDs as shown in Figure 4. The LEDs are controlled by the MAX14917 autonomously to indicate per-channel status and fault conditions. A channel status LED (SLED) is automatically turned on when the corresponding OUT_ switch is on and there is no fault condition. If a fault is detected, its associated fault LED (FLED) is turned on and its associated status LED (SLED) is automatically turned off. For any OUT_ channel, its SLED and its FLED are never on simultaneously. The fault LEDs signal thermal overload shutdown of the switches and they are stretched by 2s (typ). The LED matrix is powered through the V_{LED} supply input, which can be in the range of the 3.0V (min) up to the V_{DD} field supply voltage.

For every current limiting resistor (R) each of the four LEDs in a column string is pulsed for a quarter of the time, so that current only flows through one LED and resistor at any one time. Thus, the resistors (R) determine the LED current through one LED during the pulse. Each LED is pulsed on at a rate of 1kHz (typ) and is on for 25% of the 1ms period. Thus, the average current flowing through a LED that is turned on is about 0.25 x (V_{LED} - V_F)/R. V_F is the forward voltage of the LED. The resistor value should be chosen according to the LED current/light intensity requirements.

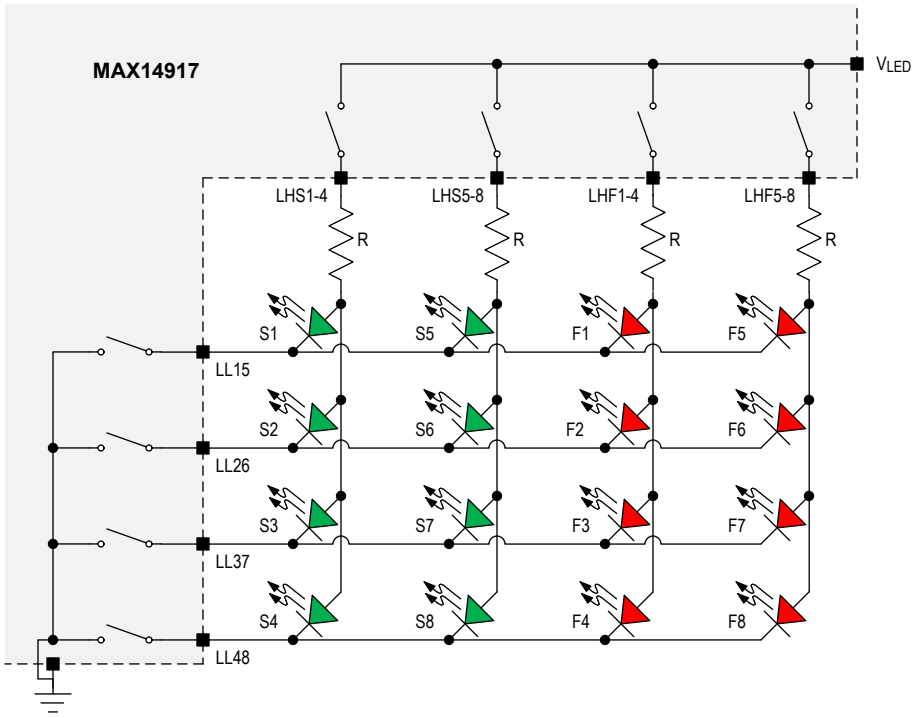


Figure 4. LED Matrix Scheme

Serial Interface

The MAX14917 communicates with the host controller through a high-speed SPI serial interface. The interface has three logic inputs: clock (CLK), chip select ($\overline{CS}$), serial data in (SDI), and one data out (SDO). The SDO is three-stated when $\overline{CS}$ is high. The maximum SPI clock rate is 10MHz. The SPI interface logic complies with SPI clock polarity CPOL = 0 and clock phase CPHA = 0.

The basic SPI command is 8 clock cycles and is extended to 16 clocks when CRC is enabled (CRCEN = high).

Note: while Figure 1, Figure 6, and Figure 7 show CLK to be low at the beginning of the SPI cycle, on the falling $\overline{CS}$ edge, the CLK can also be logic high. The MAX14917 ignores the initial CLK logic state and only acts on the first rising CLK edge and samples the first SDI bit.

Daisy-Chained SPI

Daisy-chained SPI mode allows communication with multiple MAX14917 devices using a common $\overline{CS}$ signal in one SPI cycle (refer to Figure 5). Figure 6 shows a single SPI cycle without CRC enabled (CRCEN = low) for one device.

If the ON_ bit is a 1 the high-side switch is turned on, and if it is 0, the high-side switch is turned off. The F_ bits are per-channel faults. The F_ bits are latched and are, therefore, only cleared on the following SPI cycle if the fault has disappeared before the following SPI cycle. The F_ bits do not go active when a lamp load is detected. In thermal chip shutdown, all F_ bits are set to 1.

CRC error detection is supported if the CRCEN pin is high, which lengthens the minimum SPI cycle to 16 CLK clocks per MAX14917. A single SPI command with CRC enabled is shown in Figure 7.

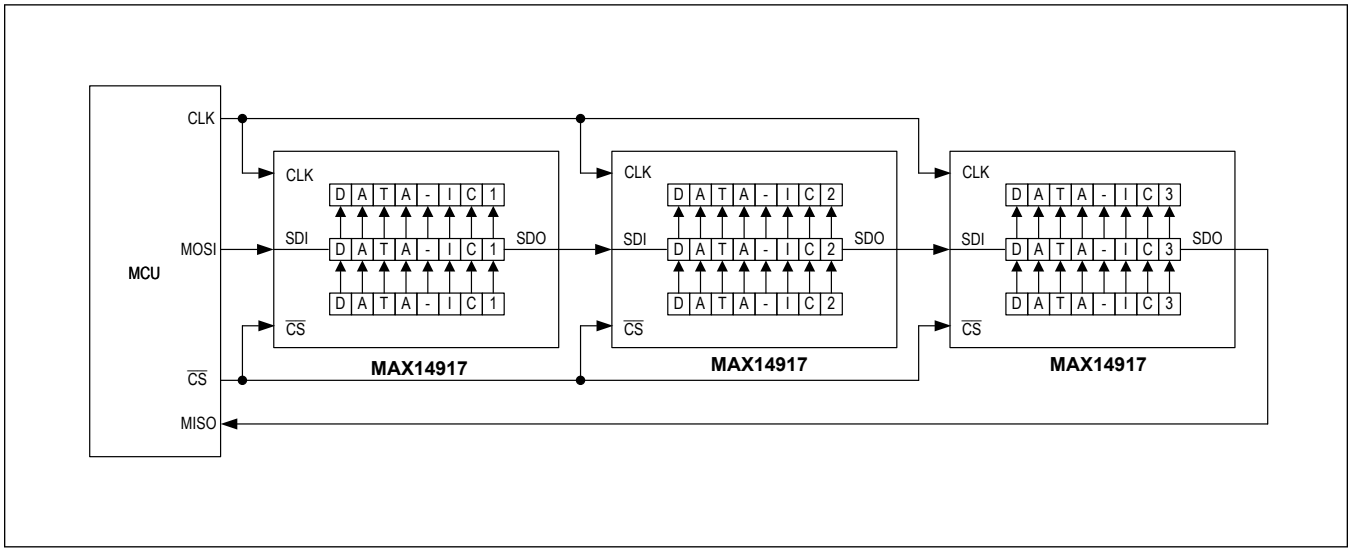


Figure 5. Diagram of Three MAX14917 Devices Daisy-Chained

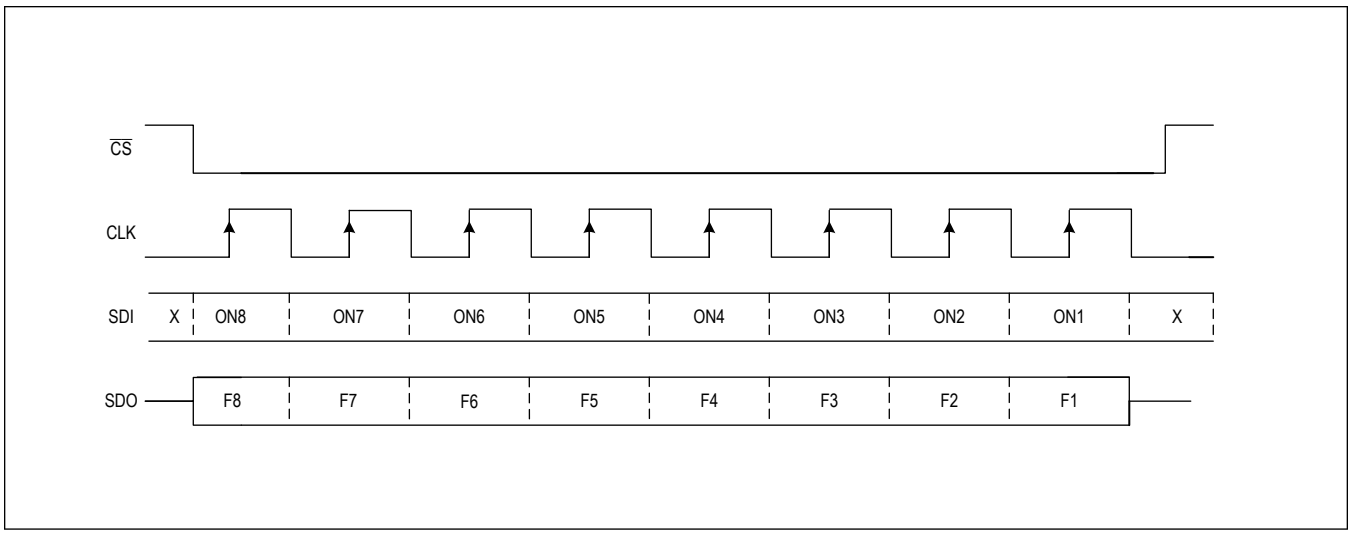


Figure 6. Single SPI Command

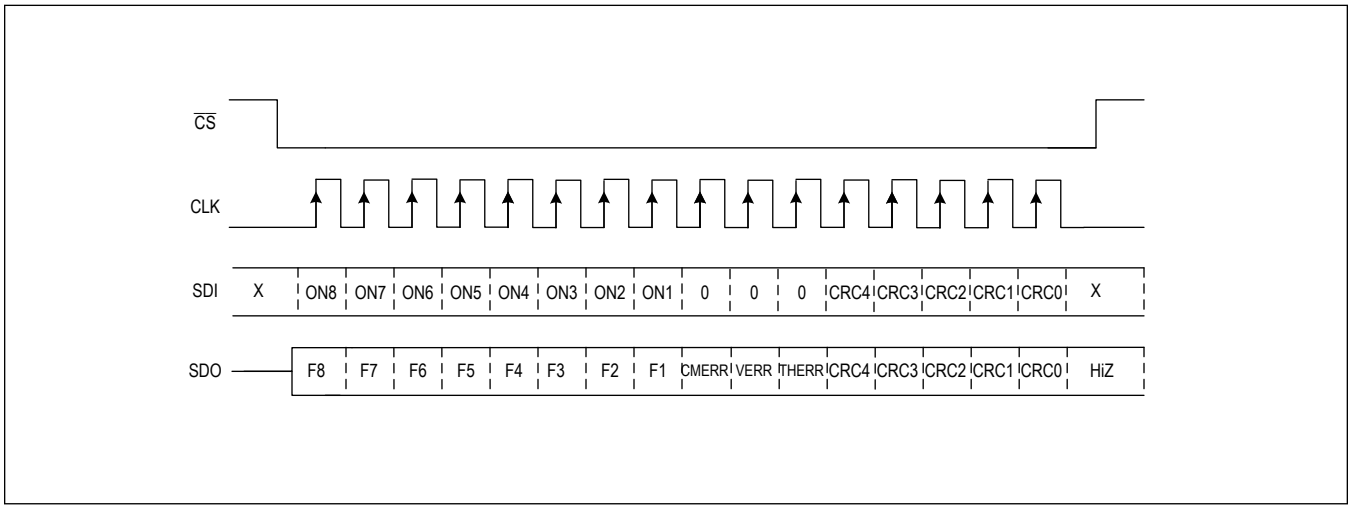


Figure 7. Single SPI Command with CRC

Checking of Clocks on the Serial Interface

The MAX14917 checks that the number of clock cycles in one SPI cycle (from falling edge of $\overline{CS}$ to rising edge of $\overline{CS}$) is a multiple of 8. The expected number of clocks is scaled according to CRCEN setting. If the number of clock cycles differs from the expected, then the SPI command is not executed and an SPI error is signaled through the $\overline{COMERR}$ pin.

CRC Error Detection on the Serial Interface

CRC error detection of the serial data can be enabled to minimize incorrect operation/misinformation due to data corruption of the SDI/SDO signals. If error detection is enabled, then the MAX14917:

1. Performs error detection on the SDI data that it receives from the controller, and
2. Calculates a CRC on the SDO data and appends a check byte to the SDO diagnostics/status data that it sends to the controller.

This ensures that both the data that it receives from the controller (OUT_ setting) and the data that it sends to the controller (F_ diagnostic) have a low likelihood of undetected errors.

Setting the CRCEN input high enables CRC error detection. A CRC frame check sequence (FCS) is then sent along with each serial transaction. The 5-bit FCS is based on the generator polynomial X5 + X4 + X2 + 1 with CRC starting value = 11111. When CRC is enabled, the MAX14917 expects a check byte appended to the SDI program/configure data that it receives. The check byte has the format shown in Figure 8. The five FCS bits (CR_) are calculated on all the data sent in one SPI command including the three “0” in the MSBs of the check byte. Therefore, the CRC is calculated from 8 bits + 3 bits. CR0 is the LSB of the FCS.

The MAX14917 verifies the received FCS. If no error is detected, the MAX14917 sets the OUT_ output switches per the SDI data. If a CRC error is detected, then the MAX14917 does not change the OUT_ outputs, but sets the $\overline{\text{COMERR}}$ logic output low (i.e., the open-drain COMERR NMOS output transistor is turned on).

In Figure 9, the format of the check byte that the device appends to the SDO data is shown: the CMERR bit is set when either an SPI or SYNCH watchdog event has occurred; the VERR bit is set if either of the V_{DD}, V_A, or internal voltages is below its nominal operational thresholds; and, the THERR bit is set when a chip thermal shutdown event has occurred. The CR_ are the CRC bits that the MAX14917 calculate on the SDO data, including the CMERR, VERR, and THERR bits. This allows the controller to check for errors on the SDO data received from the MAX14917.

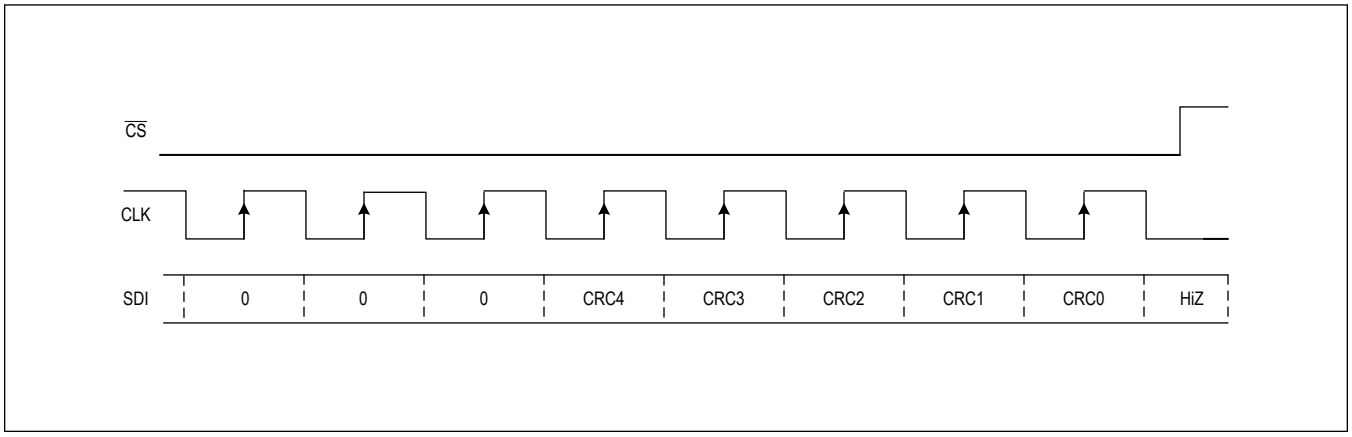


Figure 8. FCS Byte Expected from the SPI Master

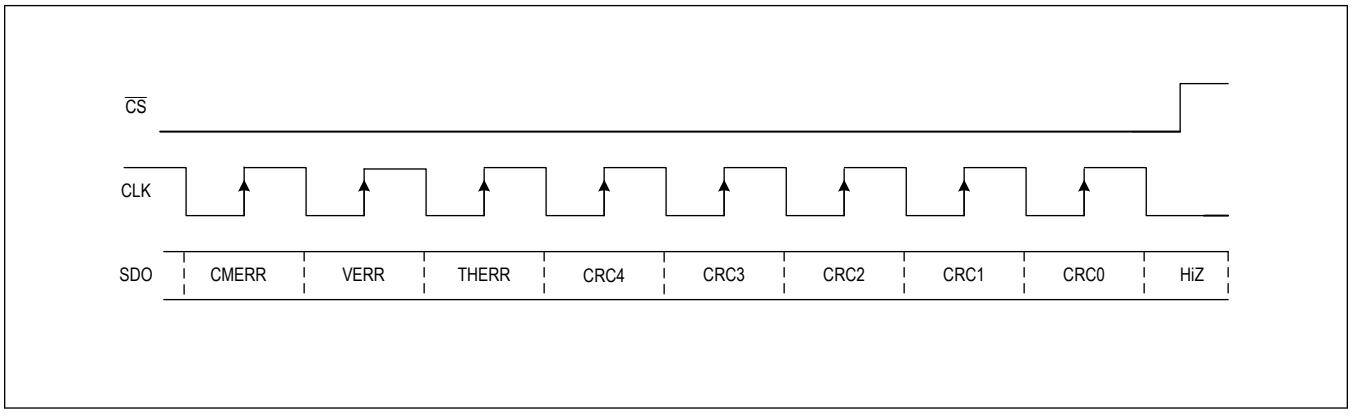


Figure 9. FCS Byte Sent by the MAX14917 to the SPI Master

Applications Information

Inductive Load Turn-Off Energy Clamping

During turn-off of inductive loads, the free-wheel energy is clamped by the internal V_{CL} clamps. This energy must be limited to 150mJ (max) at T_J = +125°C and $I_{OUT\_}$ = -600mA per channel, all channels switching simultaneously. Refer to Figure 10.

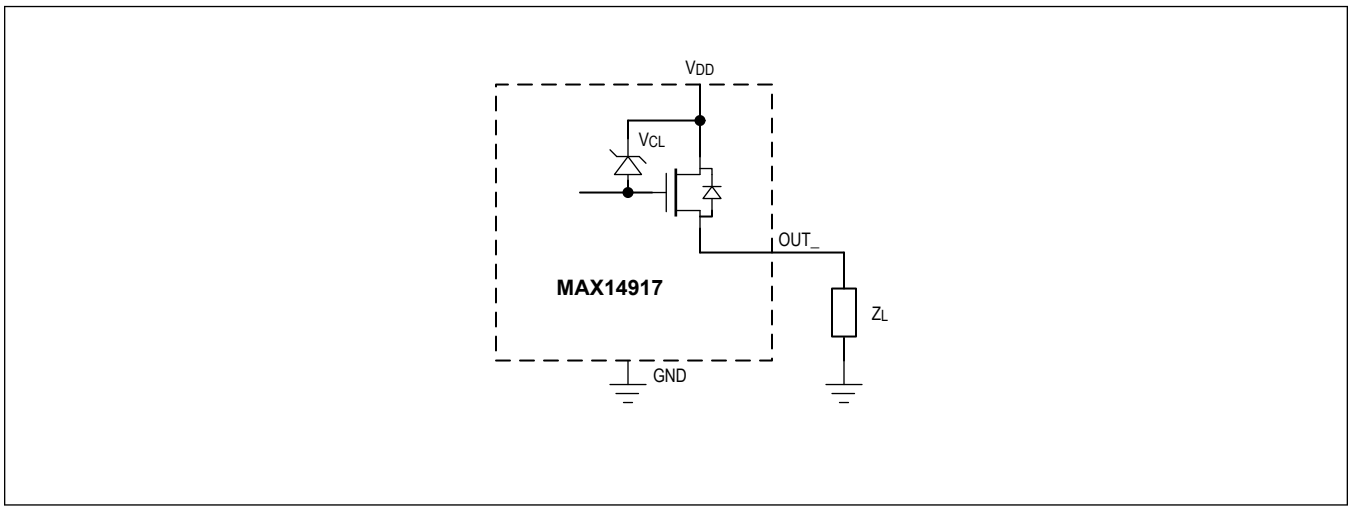


Figure 10. Inductive Load Clamping Scheme

Surge Protection

The MAX14917 has internal protection against ±1kV 42Ω/0.5µF 1.2µs/50µs surges on the OUT_ pins to GND, if the V_{DD} pins are protected with one TVS. Ensure that the peak voltage of the V_{DD} TVS is below 65V.

RF Conducted Immunity

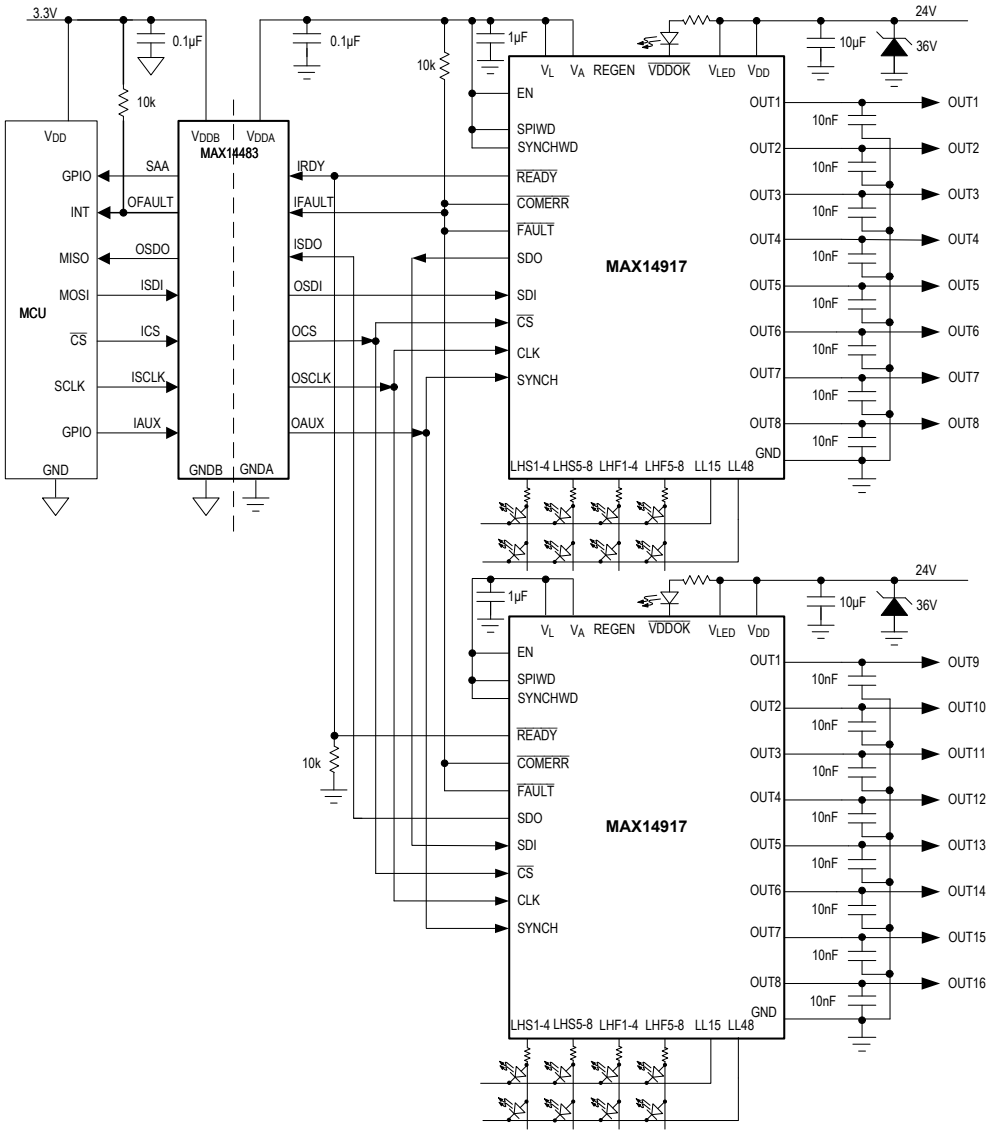
To ensure that the OUT_ pins do not produce wrong logic conditions while being off, during IEC61000-4-6 RF immunity testing, connect 10nF capacitors at each OUT_ to GND.

Reverse Currents into OUT_

If currents flow into the OUT_ pins, the device heats up due to internal currents that flow through the device from V_{DD} to GND. The internal currents are proportional to the reverse current into OUT_. The allowed reverse OUT_ current depends on V_{DD}, the ambient temperature and the thermal resistance. At 25°C ambient temperature, the reverse current into one OUT should be limited to 1A at V_{DD} = 36V and 1.5A at V_{DD} = 24V. Driving higher currents into OUT_ can destroy the device thermally.

Typical Application Circuits

16-Channel Isolated High-Side Switch



Ordering Information

PART	TEMP RANGE	PACKAGE	TOP MARKING	LEAD PITCH
MAX14917AFM+	-40°C to +125°C	48-Pin F2CQFN (6mm x 6mm)	MAX14917AFM	0.4mm
MAX14917AFM+T	-40°C to +125°C	48-Pin F2CQFN (6mm x 6mm)	MAX14917AFM	0.4mm

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/20	Initial release	—

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX14917AFM+ MAX14917AFM+T