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USB 2.0 Hi-Speed and Audio Switches with Negative Signal Capability and $\pm 15\text{kV}$ ESD

General Description

The MAX14531E–MAX14534E high ESD-protected DP3T switches multiplex Hi-Speed (480 Mbps) USB signals, low/full-speed USB signals, and analog signals such as AC-coupled audio or video through any of three channels. These devices combine the low on-capacitance (C_{ON}) and low on-resistance (R_{ON}) necessary for high-performance switching applications in portable electronics, and include an internal negative supply to pass AC-coupled audio signals that swing below ground (down to -2.0V). The MAX14531E–MAX14534E operate from a $+2.7\text{V}$ to $+5.5\text{V}$ supply.

The MAX14531E–MAX14534E have a shutdown function to reduce supply current and set all channels to high impedance. The MAX14531E–MAX14534E feature a VBUS detection function through the CB0 input to automatically switch to the default USB signal path upon detection of a valid VBUS signal. The MAX14532E/MAX14534E feature internal shunt resistors on audio channels to reduce clicks and pops heard at the output.

The MAX14531E–MAX14534E are available in a space-saving, 12-bump, $1.5\text{mm} \times 2.0\text{mm}$ WLP package and operate over the -40°C to $+85^{\circ}\text{C}$ temperature range.

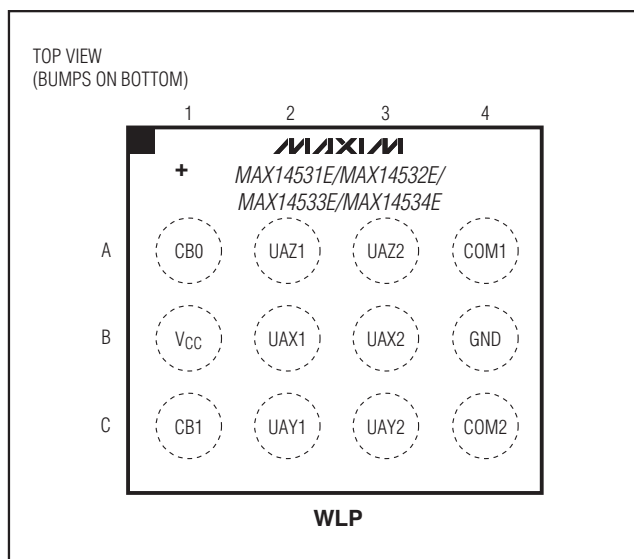
Applications

Cell Phones
MP3 Players
PDAs
Notebook Computers

Features

- ◆ Single $+2.7\text{V}$ to $+5.5\text{V}$ Supply Voltage
- ◆ Low $10\mu\text{A}$ (typ) Supply Current
- ◆ -3dB Bandwidth: 800MHz (typ)
- ◆ Low 2Ω (typ) On-Resistance
- ◆ 0.05% THD+N
- ◆ Internal Shunt Resistor for Click-and-Pop Reduction (MAX14532E/MAX14534E)
- ◆ VBUS Detection for Automatic Switch Path Selection
 - +28V Maximum Rated VBUS Detection Input (CB0)
- ◆ Space-Saving, 12-Bump, $1.5\text{mm} \times 2.0\text{mm}$ WLP Package

Pin Configuration



MAX14531E-MAX14534E

Ordering Information/Selector Guide

PART	PIN-PACKAGE	SHUNT RESISTORS	CB0 PULLDOWN RESISTOR	TOP MARK
MAX14531EWC+	12 WLP	NONE	No	AAT
MAX14532EWC+	12 WLP	UAZ_	Yes	AAU
MAX14533EWC+*	12 WLP	NONE	Yes	AAV
MAX14534EWC+*	12 WLP	UAY_UAZ_	Yes	AAW

Note: All devices are specified over the -40°C to $+85^{\circ}\text{C}$ operating temperature range.

+Denotes a lead(Pb)-free/RoHS-compliant package.

*Future product—contact factory for availability.



Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)

V_{CC} , CB1	-0.3V to +6.0V
CB0	-0.3V to +28.0V
COM_ (CB0 or CB1 > V_{IH})	-2.3V to +3.6V
COM_ (CB0 and CB1 < V_{IL})	-0.3V to +6.0V
UAX_, UAY_, UAZ_ (CB0 or CB1 > V_{IH})	-2.3V to +3.6V
UAX_, UAY_, UAZ_ (CB0 and CB1 < V_{IL})	-0.3V to +6.0V
Continuous Current into Any Terminal	$\pm 150\text{mA}$

50% Duty Cycle Current into Any Terminal	$\pm 250\text{mA}$
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$) (Note 1)	
12-Bump WLP (derate $8.5\text{mW}/^\circ\text{C}$ above $+70^\circ\text{C}$)	678mW
Operating Temperature Range	-40°C to $+85^\circ\text{C}$
Junction Temperature Range	-40°C to $+150^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{CC} = +2.7\text{V}$ to $+5.5\text{V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $V_{CC} = +3.0\text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Range	V _{CC}			2.7		5.5	V
Supply Current	I _{CC}	V _{CC} = +3.3V	V _{CB0} = V _{CB1} = 0 (shutdown)			1	μA
			V _{CB0} = V _{CC} or V _{CB1} = V _{CC}			20	
			V _{CB0} = +5.0V			20	
		V _{CC} = +5.0V	V _{CB0} = V _{CB1} = 0 (shutdown)			1	
			V _{CB0} = V _{CC} or V _{CB1} = V _{CC}			25	
			V _{CB0} = +5.5V			25	
Supply Current Increase	ΔI _{CC}	V _{CB0} = V _{CB1} = V _{IH} or V _{IL}				2	μA
VBUS Detect Threshold	V _{VBDET}	V _{CB0} rising		V _{CC} + 0.2		V _{CC} + 0.6	V
		V _{CB0} falling, hysteresis		0.2			
Analog Signal Range	V _{UAX_} , V _{UAY_} , V _{UAZ_} , V _{COM_}	V _{CB0} < V _{IL} and V _{CB1} < V _{IL} (shutdown)		0		V _{CC}	V
		V _{CB0} > V _{IH} or V _{CB1} > V _{IH}		-2.0		Min (V _{CC} , 3.3V)	
ANALOG SWITCH							
UAX_, UAY_, UAZ_ On-Resistance	R _{ON} (UAXYZ)	V _{CC} = +3.0V, V _{UAX_} = V _{UAY_} = V _{UAZ_} = 0, I _{COM_} = 10mA			2	3	Ω
UAX_, UAY_, UAZ_ On-Resistance Match Between Channels	ΔR _{ON}	V _{CC} = +3.0V, V _{UAX_} = V _{UAY_} = V _{UAZ_} = 0, I _{COM_} = 10mA (Note 3)				0.2	Ω
UAX_, UAY_, UAZ_ On-Resistance Flatness (Notes 4, 5)	R _{FLAT} (UAXYZ)	V _{CC} = +3.0V, V _{UAX_} = V _{UAY_} = V _{UAZ_} = -2.0V or +3.0V, I _{COM_} = 10mA			0.02	0.1	Ω

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MAX14531E-MAX14534E

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +2.7\text{V}$ to $+5.5\text{V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $V_{CC} = +3.0\text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Shunt Switch Resistance	R_{SH}	$I_{UAZ_} = 10\text{mA}$ (MAX14532E) or $I_{UAY_} = I_{UAZ_} = 10\text{mA}$ (MAX14534E)		100	200	Ω
UAX_ Off-Leakage Current	$I_{UAX(OFF)}$	$V_{CC} = 3.0\text{V}$, $\langle CB1, CB0 \rangle = 10$ (UAX_ open), $V_{UAX_} = +2.5\text{V}$ or 0, $V_{COM_} = -1.5\text{V}$ or $+2.5\text{V}$	-10		+10	nA
UAY_ Off-Leakage Current	$I_{UAY(OFF)}$	(MAX14531E-MAX14533E) $V_{CC} = 3.0\text{V}$, $CB1 = \text{GND}$, $CB0 = V_{CC}$ (UAY_ open), $V_{UAY_} = +2.5\text{V}$ or 0, $V_{COM_} = -1.5\text{V}$ or $+2.5\text{V}$	-10		+10	nA
UAZ_ Off-Leakage Current	$I_{UAZ(OFF)}$	(MAX14531E/MAX14533E) $V_{CC} = 3.0\text{V}$, $\langle CB1, CB0 \rangle = 01$ (UAZ_ open), $V_{UAZ_} = +2.5\text{V}$ or 0, $V_{COM_} = -1.5\text{V}$ or $+2.5\text{V}$	-10		+10	nA
COM_ On-Leakage Current	$I_{COM(ON)}$	$V_{CC} = +3.0\text{V}$, $V_{COM_} = -1.5\text{V}$ or $+2.5\text{V}$, $\langle CB1, CB0 \rangle = 01$, $V_{UAY_} = V_{UAZ_} = 0$, $+2.5\text{V}$, or unconnected	-100		+100	nA
		$\langle CB1, CB0 \rangle = 10$, $V_{UAX_} = V_{UAZ_} = 0$, $+2.5\text{V}$, or unconnected	-100		+100	
		$\langle CB1, CB0 \rangle = 11$, $V_{UAX_} = V_{UAY_} = 0$, $+2.5\text{V}$, or unconnected	-100		+100	
COM_ Off-Leakage Current	$I_{COM(OFF)}$	$V_{CC} = +3.0\text{V}$, $\langle CB1, CB0 \rangle = 00$, $V_{UAX_} = V_{UAY_} = V_{UAZ_} = 0$, $V_{COM_} = +3.6\text{V}$	-0.01		+2	μA
		$V_{COM_} = 0$	-10		+10	nA
Enable Turn-On Time	t_{ON}	From shutdown to UAX_, UAY_, or UAZ_ connected to COM_, $V_{CC} = +3.0\text{V}$, $V_{UA_} = +3.0\text{V}$, $R_L = 50\Omega$, $C_L = 10\text{pF}$ (Figure 1)			250	μs
Enable Turn-Off Time	t_{OFF}	From UAX_, UAY_, or UAZ_ connected to COM_ to shutdown, $V_{CC} = +3.0\text{V}$, $V_{UA_} = +3.0\text{V}$, $R_L = 50\Omega$, $C_L = 10\text{pF}$ (Figure 1)			6	μs
Address Transition Time	t_{TRANS}	Switching from one active channel to another, $V_{CC} = +3.0\text{V}$, $V_{UA_} = +3.0\text{V}$, $R_L = 50\Omega$, $C_L = 10\text{pF}$			250	μs
Transient to Shutdown Valid Time	t_{T00}	From UAX_, UAY_, or UAZ_ connected to COM_ to shutdown, $V_{CC} = +3.0\text{V}$	20		100	μs
VBUS Detection Time	t_{VBDET}	$V_{CC} = +3.0\text{V}$, $V_{UAXY_} = +3.0\text{V}$, $R_L = 50\Omega$, $C_L = 10\text{pF}$, $V_{CB1} = +3.0\text{V}$, $V_{CB0} = 0$ to $+5.0\text{V}$	15		200	μs
Break-Before-Make Time Delay	t_{BBM}	Time delay between one side of the switch opening and the other side closing, $R_L = 50\Omega$, $C_L = 10\text{pF}$ (Note 5)	1			μs
Output Skew Same Switch	$t_{SK(P)}$	t_{INRISE} , t_{INFALL} , $< 5\text{ns}$, $t_{OUTRISE}$, $t_{OUTFALL} < 5\text{ns}$, Figure 2 (Note 5)		40		ps

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +2.7\text{V}$ to $+5.5\text{V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $V_{CC} = +3.0\text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Skew Between Channels	$t_{SK(O)}$	$t_{INRISE}, t_{INFALL} < 5\text{ns}$, $t_{OUTRISE}, t_{OUTFALL} < 5\text{ns}$, Figure 2 (Note 5)		40		ps
UAX_, UAY_, UAZ_ Off-Capacitance	C_{COM_OFF}	$f = 240\text{MHz}$, $V_{COM} = 0.5\text{V}_{P-P}$, DC bias = 0 (Note 5)		5		pF
COM_ On-Capacitance	C_{COM_ON}	$f = 240\text{MHz}$, $V_{COM} = 0.5\text{V}_{P-P}$, DC bias = 0 (Note 5)		8		pF
AC PERFORMANCE						
-3dB Bandwidth	BW_{NO}	$V_{COM_} = 0\text{dBm}$, $R_L = 50\Omega$, $R_S = 50\Omega$ (Figure 3)		800		MHz
Off-Isolation	V_{ISO}	$f = 100\text{kHz}$, $V_{COM_} = 1\text{V}_{RMS}$, $R_L = 50\Omega$, $R_S = 50\Omega$ (Figure 3)		-65		dB
Crosstalk	V_{CT}	$f = 100\text{kHz}$, $V_{COM_} = 1\text{V}_{RMS}$, $R_L = 50\Omega$, $R_S = 50\Omega$ (Figure 3)		-70		dB
Power-Supply Rejection Ratio	PSRR	$f = 10\text{kHz}$, $V_{CC} = +3.0\text{V} \pm 0.3\text{V}$, $R_{COM_} = 50\Omega$		60		dB
Total Harmonic Distortion Plus Noise	THD+N	$f = 20\text{Hz}$ to 20kHz , $V_{COM_} = 0.5\text{V}_{P-P}$, DC bias = 0, $R_L = 32\Omega$		0.05		%
LOGIC INPUT						
Input Logic-High	V_{IH}		1.4			V
Input Logic-Low	V_{IL}			0.4		V
Input Logic Hysteresis	V_{HYST}	(Note 5)		100		mV
Input Leakage Current	I_{IN}	$V_{CB0} = V_{CC} = +3.3\text{V}$ (MAX14531E) (Note 5)		4		μA
		$V_{CB0} = 0$, $V_{CC} = +5.5\text{V}$	-250		+250	nA
		$V_{CB1} = 0$ or $+5.5\text{V}$	-250		+250	
CB0 Pulldown Resistor	R_{CB0}	MAX14532E/MAX14533E/MAX14534E	500	1000	1500	$\text{k}\Omega$
ESD PROTECTION						
All Pins		Human Body Model		± 2		kV
COM1, COM2		Human Body Model		± 15		kV

Note 2: All devices are 100% production tested at $T_A = +25^\circ\text{C}$. All temperature limits are guaranteed by design.

Note 3: $\Delta R_{ON} = \text{ABS}(R_{ON(CH1)} - R_{ON(CH2)})$

Note 4: Flatness is defined as the difference between the maximum and minimum value of on-resistance, as measured over specified analog signal ranges.

Note 5: Guaranteed by design.

MAX14531E-MAX14534E

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USB 2.0 Hi-Speed and Audio Switches with Negative Signal Capability and ±15kV ESD

Test Circuits/Timing Diagrams (continued)

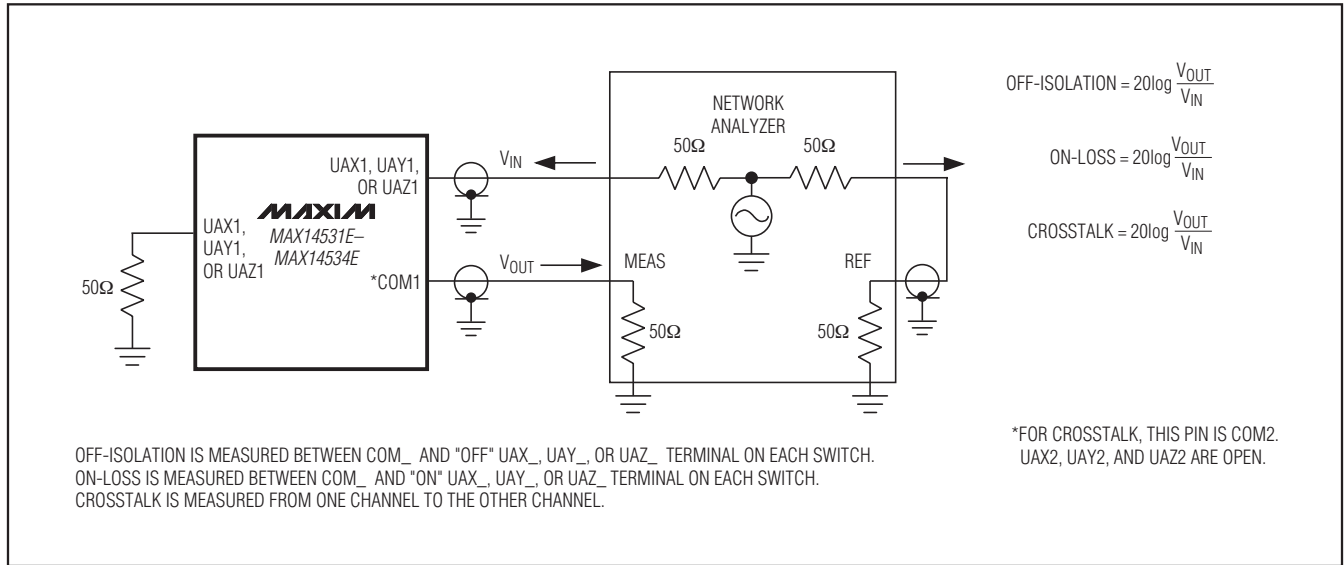


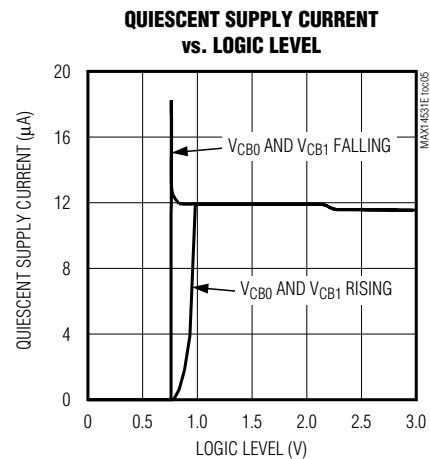
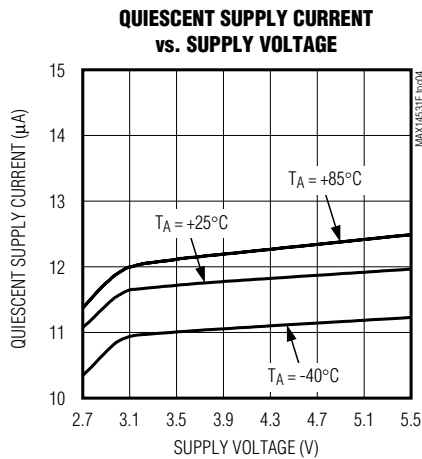
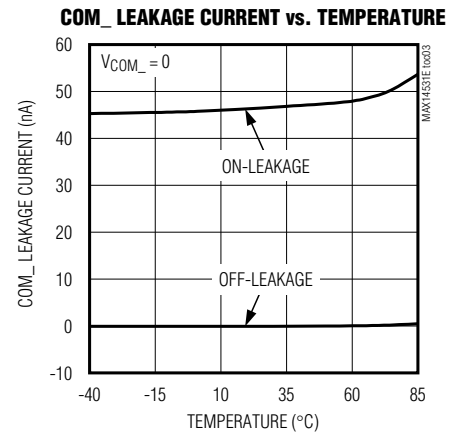
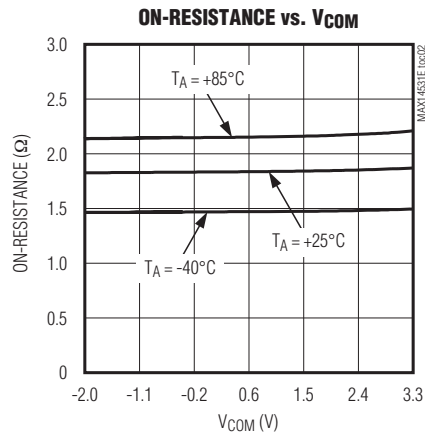
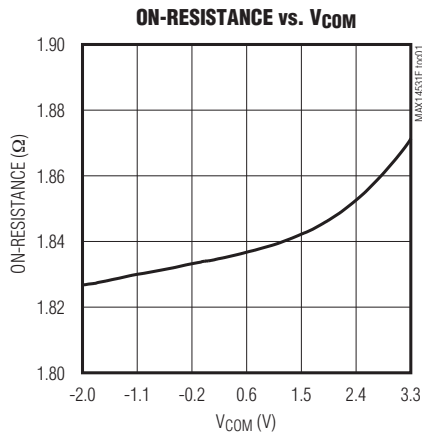
Figure 3. On-Loss, Off-Isolation, and Crosstalk

USB 2.0 Hi-Speed and Audio Switches with Negative Signal Capability and $\pm 15\text{kV}$ ESD

Typical Operating Characteristics

($V_{CC} = +3.0\text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

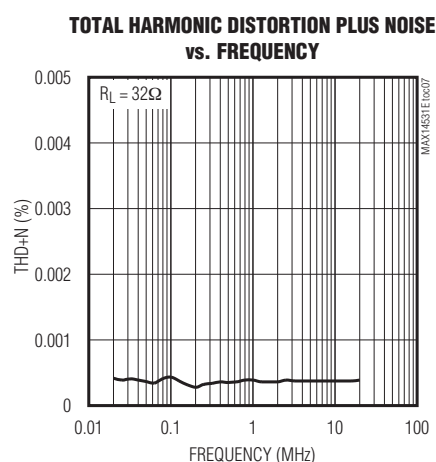
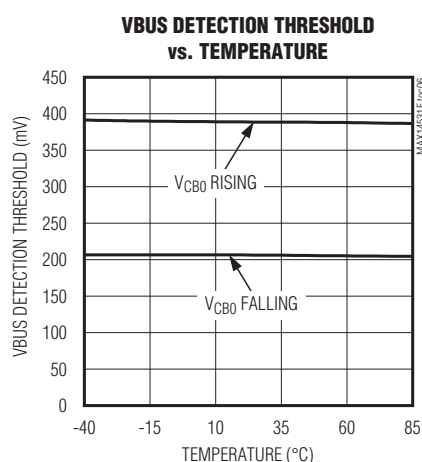
MAX14531E-MAX14534E



USB 2.0 Hi-Speed and Audio Switches with Negative Signal Capability and $\pm 15\text{kV}$ ESD

Typical Operating Characteristics (continued)

($V_{CC} = +3.0\text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
A1	CB0	Control Input 0
A2	UAZ1	USB/Audio Input Z1
A3	UAZ2	USB/Audio Input Z2
A4	COM1	Common Terminal 1
B1	VCC	Positive Supply Voltage Input. Bypass VCC to GND with a 0.1 μF ceramic capacitor as close as possible to the device.
B2	UAX1	USB/Audio Input X1
B3	UAX2	USB/Audio Input X2
B4	GND	Ground
C1	CB1	Control Input 1
C2	UAY1	USB/Audio Input Y1
C3	UAY2	USB/Audio Input Y2
C4	COM2	Common Terminal 2

USB 2.0 Hi-Speed and Audio Switches with Negative Signal Capability and $\pm 15\text{kV}$ ESD

Detailed Description

The MAX14531E-MAX14534E are high ESD-protected single DP3T switches that operate from a +2.7V to +5.5V supply and are designed to multiplex USB 2.0 Hi-Speed signals and AC-coupled analog signals. These switches combine the low on-capacitance (C_{ON}) and low on-resistance (R_{ON}) necessary for high-performance switching applications. These devices also meet the requirements for USB low-speed and full-speed signaling. The negative signal capability of all three channels allows signals below ground to pass through without distortion.

Analog Signal Levels

The MAX14531E-MAX14534E are bidirectional, allowing UAX_, UAY_, UAZ_, and COM_ to be configured as either inputs or outputs. Note that UAX_, UAY_, and UAZ_ are only protected against ESD up to $\pm 2\text{kV}$ (Human Body Model) and may require additional ESD protection if used as outputs. These devices feature a charge pump that generates a negative supply to allow analog signals as low as -2.0V applied to UAX_, UAY_, UAZ_, or COM_. The negative charge pump is only active when the part is enabled (CB0 or $\text{CB1} = 1$). Connect negative signals to UAX_, UAY_, UAZ_, or COM_ only when the device is enabled.

VBUS Detection

The MAX14531E-MAX14534E feature a VBUS detection input (CB0) that connects COM_ to UAX_ when VCB0 exceeds the VBUS detection threshold (VVBDET) (see the *Functional Diagram/Truth Table*). Note that the MAX14531E requires an external pulldown resistor when using this function.

Digital Control Inputs

The MAX14531E-MAX14534E provide control logic inputs, CB0 and CB1 , to control the switch position as shown in the *Functional Diagram/Truth Table*. Drive CB_rail -to-rail to minimize power consumption.

Shutdown Mode

The MAX14531E-MAX14534E feature a shutdown mode to reduce the supply current to less than $1\mu\text{A}$ and place the switches in high impedance. Drive both CB0 and CB1 low to place the devices in shutdown mode (see the *Functional Diagram/Truth Table*.)

Click-and-Pop Suppression

The switched 100Ω shunt resistors on the MAX14532E/MAX14534E automatically discharge any capacitance at the UAZ_ (MAX14532E) or UAY_ and UAZ_ (MAX14534E) inputs when they are unconnected from COM_ (see the *Functional Diagram/Truth Table*). This reduces audio click-and-pop sounds that may occur when switching to audio sources.

Applications Information

Extended ESD Protection

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges up to $\pm 2\text{kV}$ (Human Body Model) encountered during handling and assembly. COM1 and COM2 are further protected against ESD up to $\pm 15\text{kV}$ (Human Body Model) without damage. The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the MAX14531E-MAX14534E continue to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 4 shows the Human Body Model, and Figure 5 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a $1.5\text{k}\Omega$ resistor.

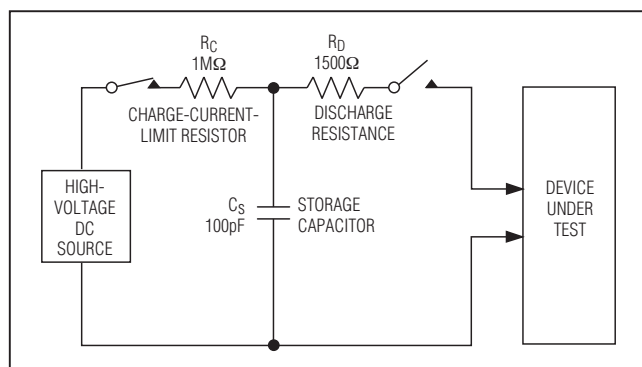


Figure 4. Human Body ESD Test Model

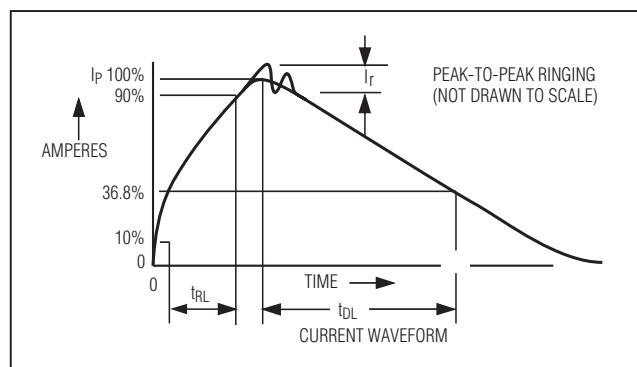


Figure 5. Human Body Current Waveform

USB 2.0 Hi-Speed and Audio Switches with Negative Signal Capability and $\pm 15\text{kV}$ ESD

Layout

USB Hi-Speed requires careful PCB layout with 45Ω single-ended/ 90Ω differential controlled impedance matched traces of equal lengths. Ensure that bypass capacitors are as close as possible to the device. Use large ground planes where possible.

Power-Supply Sequencing

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all devices. Apply V_{CC} before applying analog signals, especially if the analog signal is not current limited.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
12 WLP	W121A2-1	21-0009

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