

GENERAL DESCRIPTION

The DS21600/DS21602/DS21604 are multiple-rate clock adapters that convert between E-carrier and T-carrier clocks rates. A T1 or E1 clock output, CLKOUT1, is available, along with a higher multiple rate clock output, CLKOUT2. CLKOUT1 and CLKOUT2 are frequency locked to the clock input CLKIN. The clock outputs, along with frame-sync output, can be phase-aligned to a frame-sync input. The devices are fully compatible with the LXP600A, LXP602, and LXP604, and operate from either a 5V or 3.3V supply. All operation modes include a standard 8kHz output.

The DS21600/DS21602/DS21604 are available in 16-pin SO, and are rated for industrial temperatures.

ORDERING INFORMATION

| PART | TEMP RANGE | PIN-PACKAGE |
|------------------|----------------|-------------|
| DS21600SN | -40°C to +85°C | 16 SO |
| DS21600SN+ | -40°C to +85°C | 16 SO |
| DS21600N | -40°C to +85°C | 8 DIP |
| DS21600N+ | -40°C to +85°C | 8 DIP |
| DS21602SN | -40°C to +85°C | 16 SO |
| DS21602SN+ | -40°C to +85°C | 16 SO |
| DS21602N | -40°C to +85°C | 8 DIP |
| DS21602N+ | -40°C to +85°C | 8 DIP |
| DS21604SN | -40°C to +85°C | 16 SO |
| DS21604SN+ | -40°C to +85°C | 16 SO |
| DS21604N | -40°C to +85°C | 8 DIP |
| DS21604N+ | -40°C to +85°C | 8 DIP |

+ Denotes a lead(Pb)-free/RoHS-compliant device.

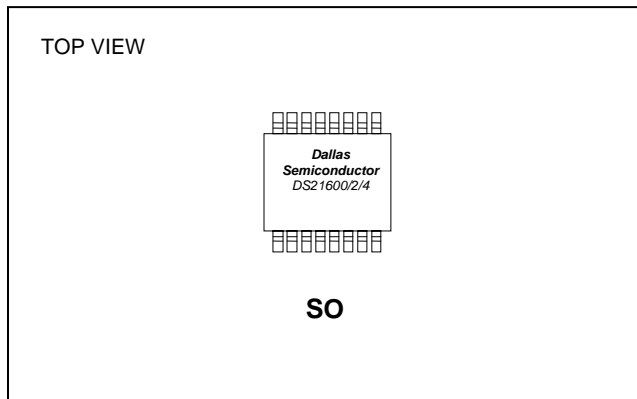
FREQUENCY CONVERSIONS (MHz)

| PART | CLKIN | CLKOUT1 | CLKOUT2 |
|----------------|-------|---------|---------|
| DS21600 | 1.544 | 2.048 | 6.144 |
| | 2.048 | 1.544 | 6.176 |
| DS21602 | 1.544 | 2.048 | 8.192 |
| | 2.048 | 1.544 | 6.176 |
| DS21604 | 1.544 | 4.096 | 8.192 |
| | 4.096 | 1.544 | 6.176 |

FEATURES

- Direct Drop-In Replacement for LXP600ASE, LXP602SE, and LXP604SE
- Converts E-Carrier Clock Rates to T-Carrier Clock Rates
- Converts T-Carrier Clock Rates to E-Carrier Clock Rates
- 3.3V or 5V Supply
- Low Jitter Output
- Multiple Output Clocks Synchronized to Input Clock
- 8kHz Frequency-Locked Output for All Operation Modes
- No External Components Required
- 16-Pin SO and 8-Pin DIP
- Industrial Temperature Range: -40°C to +85°C

PIN CONFIGURATION



Note: Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.

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1. PIN DESCRIPTION

Table 1-A. Pin Description

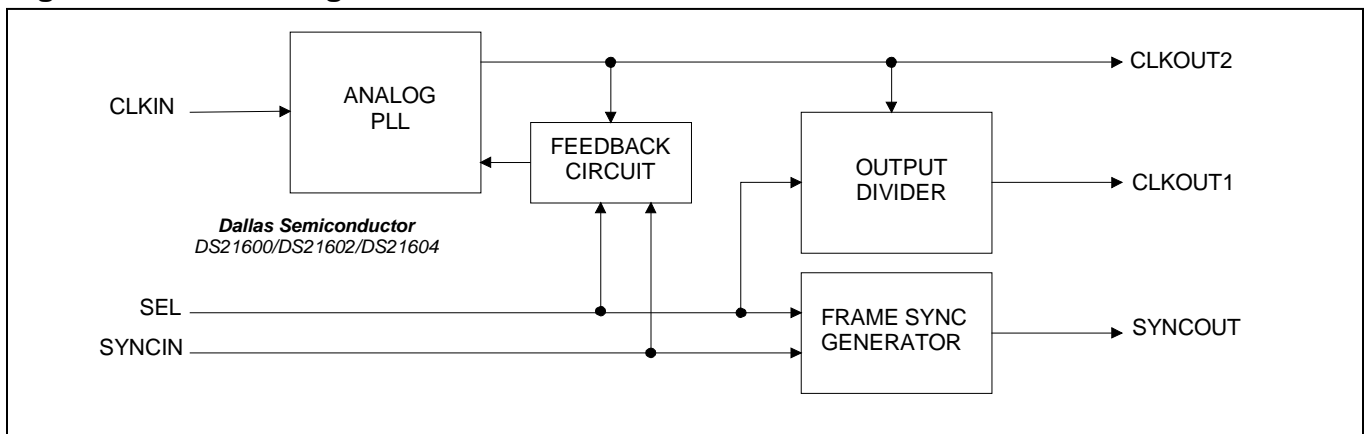
| PIN | | NAME | TYPE | FUNCTION |
|-----|----------------------------|-----------------|--------|--|
| DIP | SO | | | |
| — | 1, 3, 6, 8, 10, 11, 13, 15 | N.C. | — | No Connect |
| 1 | 2 | SYNCOUT | Output | Synchronization Output. An 8kHz output that can be synchronized to the clock outputs. |
| 2 | 4 | CLKOUT2 | Output | Clock Output 2. T1 or E1 carrier clock output referenced to CLKIN. |
| 3 | 5 | CLKIN | Input | Clock Input. Reference Clock Input. CLKOUT1 and CLKOUT2 will be referenced to this clock. |
| 4 | 7 | CLKOUT1 | Output | Clock Output 1. T1 or E1 carrier clock output referenced to CLKIN. |
| 5 | 9 | V _{SS} | Supply | Ground |
| 6 | 12 | SEL | Input | Clock Mode Select. Conversion mode select. |
| 7 | 14 | SYNCIN | Input | Synchronization Input. Used to synchronize the clock outputs and SYNCOUT to CLKIN and SYNCIN. SYNCIN should be tied high or low when not in use. |
| 8 | 16 | V _{DD} | Supply | Positive Supply, 3.3V or 5V ±5% |

1.1 Pin Name Cross-Reference to LXP60X

Table 1-B. Pin Name Cross-Reference to LXP60x

| DS21600/DS21602 /DS21604 | LXP600ALXP602/L XP604 | FUNCTION |
|--------------------------|-----------------------|------------------------------|
| SYNCOUT | FSO | Synchronization Pulse Output |
| CLKOUT2 | HFO | Clock 2 Output |
| CLKIN | CLKI | Clock Input |
| CLKOUT1 | CLKO | Clock 1 Output |
| V _{SS} | GND | Ground |
| SEL | SEL | Clock Mode Select |
| SYNCIN | FSI | Synchronization Pulse Input |
| N.C. | N.C. | No Connect |
| V _{DD} | V _{CC} | Positive Supply |

Figure 1-1. Block Diagram



2. FUNCTIONAL DESCRIPTION

A clock input at CLKIN is converted to an alternate clock rate available on CLKOUT1. A higher multiple-rate clock also is available on CLKOUT2. Additionally, an 8kHz clock locked to CLKIN is always available at the SYNCOUT pin. The SEL pin controls clock-rate conversion selection.

2.1 Mode Select

The SEL pin is used to select the operating frequencies. [Table 2-A](#) shows the SEL state for the various operating modes of the DS21600, DS21602, and DS21604.

Table 2-A. Frequency Conversions (MHz)

| PART | SEL | CLKIN | CLKOUT1 | CLKOUT2 |
|---------|-----|-------|---------|---------|
| DS21600 | 0 | 1.544 | 2.048 | 6.144 |
| | 1 | 2.048 | 1.544 | 6.176 |
| DS21602 | 0 | 1.544 | 2.048 | 8.192 |
| | 1 | 2.048 | 1.544 | 6.176 |
| DS21604 | 0 | 1.544 | 4.096 | 8.192 |
| | 1 | 4.096 | 1.544 | 6.176 |

2.2 Frame-Sync Input

In all cases, CLKOUT1 and CLKOUT2 are frequency-locked to CLKIN. CLKOUT1, CLKOUT2, and SYNCOUT are phased-locked to SYNCIN when SYNCIN is asserted. The signal applied to SYNCIN can be 8kHz or some integer subrate such as 1kHz, 2kHz, or 4kHz. Phase synchronization occurs within a maximum of 50ms when SYNCIN is 8kHz.

3. OUTPUT JITTER

[Table 3-A](#) shows the output jitter specifications for 2.048MHz (or 4.096MHz) to 1.544MHz conversions (SEL = 1) and 1.544MHz to 2.048MHz (or 4.096MHz) conversions (SEL = 0).

Table 3-A. Output Jitter Specifications

| CLKIN (MHz) | CLKOUT1 (MHz) | FREQUENCY BAND | SPECIFICATION | VALUE | TYP | MAX | UNITS |
|----------------|---------------|-----------------|---------------|-------|-------|-------|-------------------|
| 1.544 | 2.048 | 20Hz–100kHz | G.823 | 1.500 | 0.018 | 0.035 | UI _{P-P} |
| | | 18kHz–100kHz | G.823 | 0.200 | 0.012 | 0.025 | UI _{P-P} |
| 2.048 or 4.096 | 1.544 | No bandlimiting | TR62411 | 0.050 | 0.010 | 0.020 | UI _{P-P} |
| | | 10Hz–40kHz | TR62411 | 0.025 | 0.005 | 0.010 | UI _{P-P} |
| | | 8kHz–40kHz | TR62411 | 0.025 | 0.006 | 0.012 | UI _{P-P} |

3.1 Jitter Transfer

[Figure 3-1](#) and [Figure 3-2](#) show jitter transfer for 2.048MHz-to-1.544MHz conversions and vice versa.

Figure 3-1. Nominal Jitter Transfer for 2.048MHz-to-1.544MHz Conversion

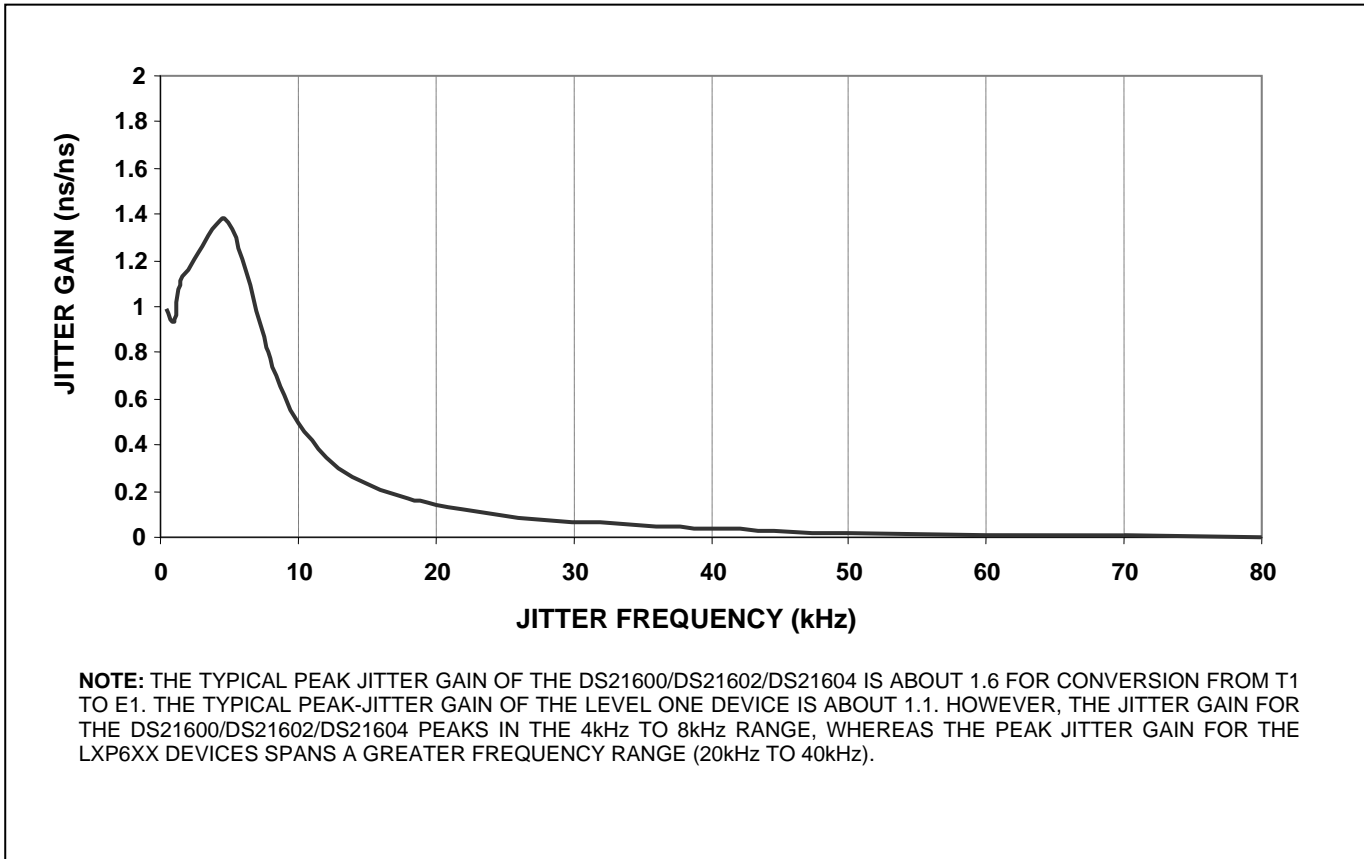
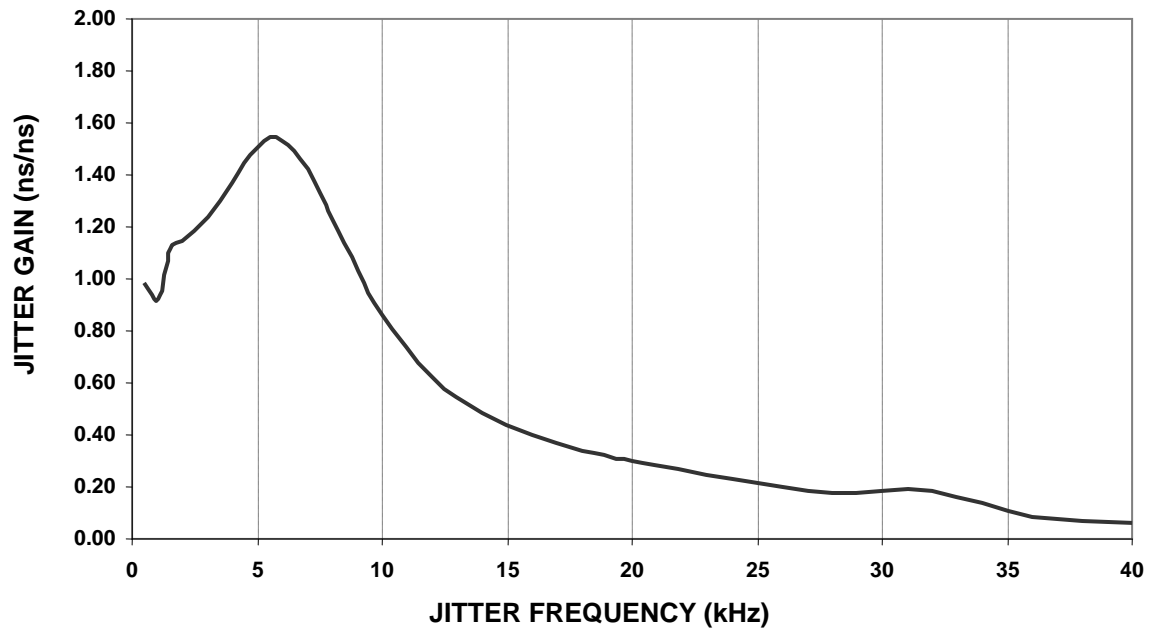


Figure 3-2. Nominal Jitter Transfer for 1.544MHz-to-2.048MHz Conversion



NOTE: THE TYPICAL PEAK JITTER GAIN OF THE DS21600/DS21602/DS21604 IS ABOUT 1.6 FOR CONVERSION FROM T1 TO E1. THE TYPICAL PEAK-JITTER GAIN OF THE LEVEL ONE DEVICE IS ABOUT 1.1. HOWEVER, THE JITTER GAIN FOR THE DS21600/DS21602/DS21604 PEAKS IN THE 4kHz TO 8kHz RANGE, WHEREAS THE PEAK JITTER GAIN FOR THE LXP6XX DEVICES SPANS A GREATER FREQUENCY RANGE (20kHz TO 40kHz).

4. OPERATING PARAMETERS

ABSOLUTE MAXIMUM RATINGS

| | |
|--|---------------------------------------|
| Voltage Range on Any Pin Relative to Ground..... | -1.0V to +6.0V |
| Operating Temperature Range for DS21600SN, DS21602SN, DS21604SN..... | -40°C to +85°C |
| Storage Temperature Range..... | -55°C to +125°C |
| Soldering Temperature..... | See IPC/JEDEC J-STD-020 Specification |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------|----------|------------|-------|-----|-------|-------|
| Logic 1 | V_{IH} | (Note 1) | 2.0 | | 5.5 | V |
| Logic 0 | V_{IL} | (Note 1) | -0.3 | | +0.8 | V |
| Supply Voltage | V_{DD} | 3.3V | 3.135 | 3.3 | 3.465 | V |
| | | 5V | 4.75 | 5 | 5.25 | |

DC CHARACTERISTICS

($V_{DD} = 3.3\text{V}/5\text{V} \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------|----------|------------|------|-----|------|---------------|
| Supply Current | I_{DD} | (Note 2) | | | 14 | mA |
| Input Leakage | I_{IL} | (Note 3) | -1.0 | | +1.0 | μA |
| Output Leakage | I_{LO} | | | | 1.0 | μA |
| Output Current (2.4V) | I_{OH} | | -1.0 | | | mA |
| Output Current (0.4V) | I_{OL} | | +4.0 | | | mA |

AC TIMING

(Figure 4-1, Figure 4-2, Figure 4-3, Figure 4-4, and Figure 4-5)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------|---------------|-----------------|-----|--------------|-------|
| Capture Range on CLKIN | | (Note 1) | ±10,000 | | | ppm |
| Lock Range on CLKIN | | (Note 1) | ±10,000 | | | ppm |
| CLKIN Duty Cycle | | (Note 1) | 35 | | 65 | % |
| SYNCIN Setup to CLKIN Rising | t_{SU} | (Note 1) | 46 | | | ns |
| SYNCIN Hold After CLKIN Rising | t_{HI} | (Note 1) | 30 | | | ns |
| SYNCIN Pulse Width | t_{PW} | (Note 1) | 76 | | CLKIN period | ns |
| CLKOUT1 Delay from CLKIN Rising | t_D | 3.3V (Note 1) | -15 | 0 | +41 | ns |
| | | 5V (Note 1) | -15 | 0 | +22 | |
| CLKOUT1 Duty Cycle | C_D | (Note 1) | 50 | | | % |
| SYNCOUT Delay from CLKOUT2 | t_{DF} | (Note 1) | -5 | | 30 | ns |
| SYNCOUT Pulse Width | t_{SPW} | (Note 1) | CLKOUT 1 period | | | ns |
| CLKOUT1 Delay from CLKOUT2 Rising | t_{DH} | 3.3V (Note 1) | -15 | 0 | +15 | ns |
| Rise/Fall Time on CLKIN, SYNCIN | t_{RF} | 3.3V (Note 1) | 60 | | | ns |
| | | 5V (Note 1) | 40 | | | |
| Rise/Fall Time on CLKOUT1, SYNCOUT, CLKOUT2 (Note 4) | t_{RF} | 3.3V (Note 1) | 75 | | | ns |
| | | 5V (Note 1) | 40 | | | |

Note 1: Guaranteed by design.

Note 2: 100pF load on all outputs.

Note 3: $0V < V_{IN} < V_{DD}$.

Note 4: 100pF load on CLKOUT1, SYNCOUT, CLKOUT2.

Figure 4-1. DS21600/DS21602 High-to-Low Frequency Conversion Frame-Sync Alignment

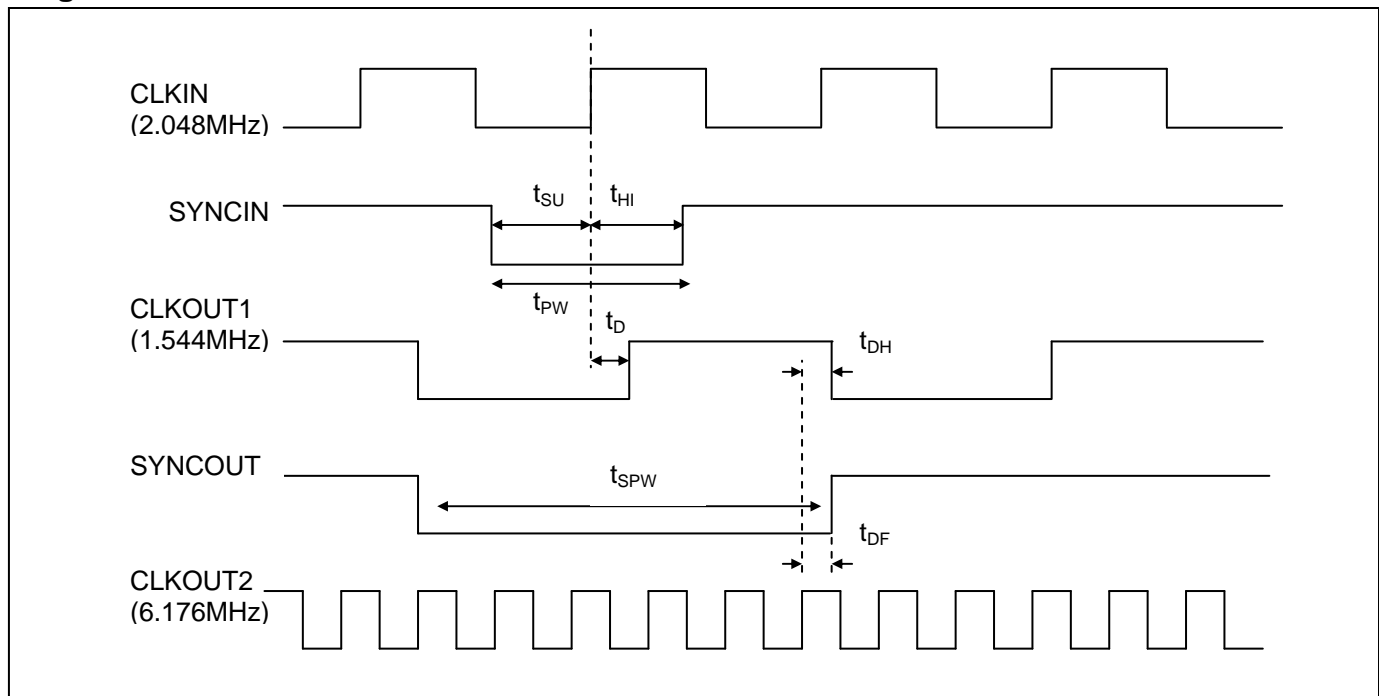


Figure 4-2. DS21604 High-To-Low Frequency Conversion Frame-Sync Alignment

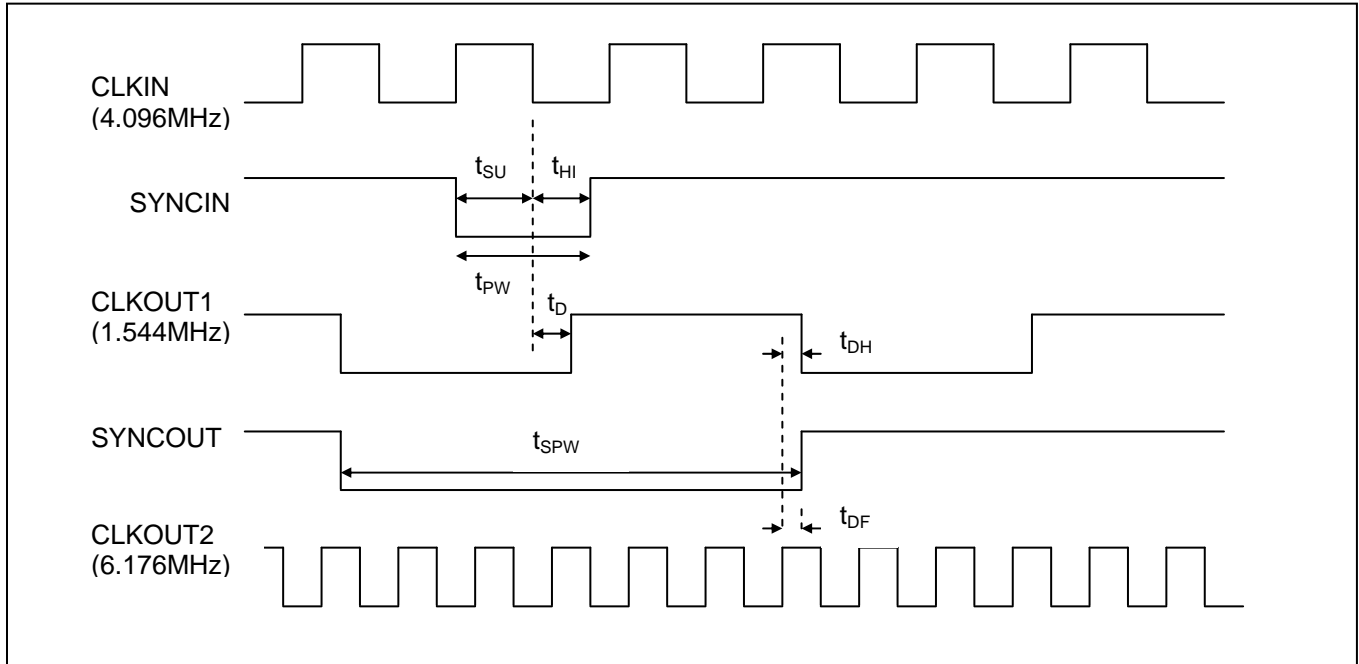


Figure 4-3. DS21600 Low-to-High Frequency Conversion Frame-Sync Alignment

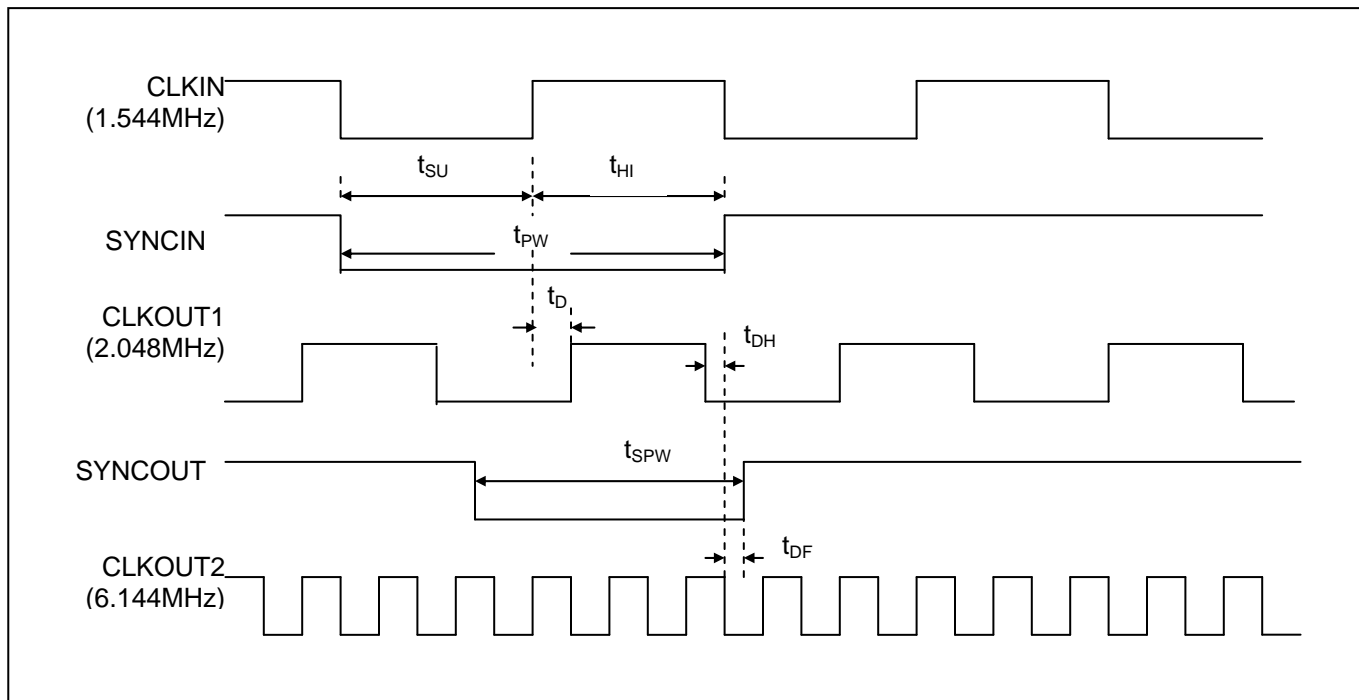


Figure 4-4. DS21602 Low-to-High Frequency Conversion Frame-Sync Alignment

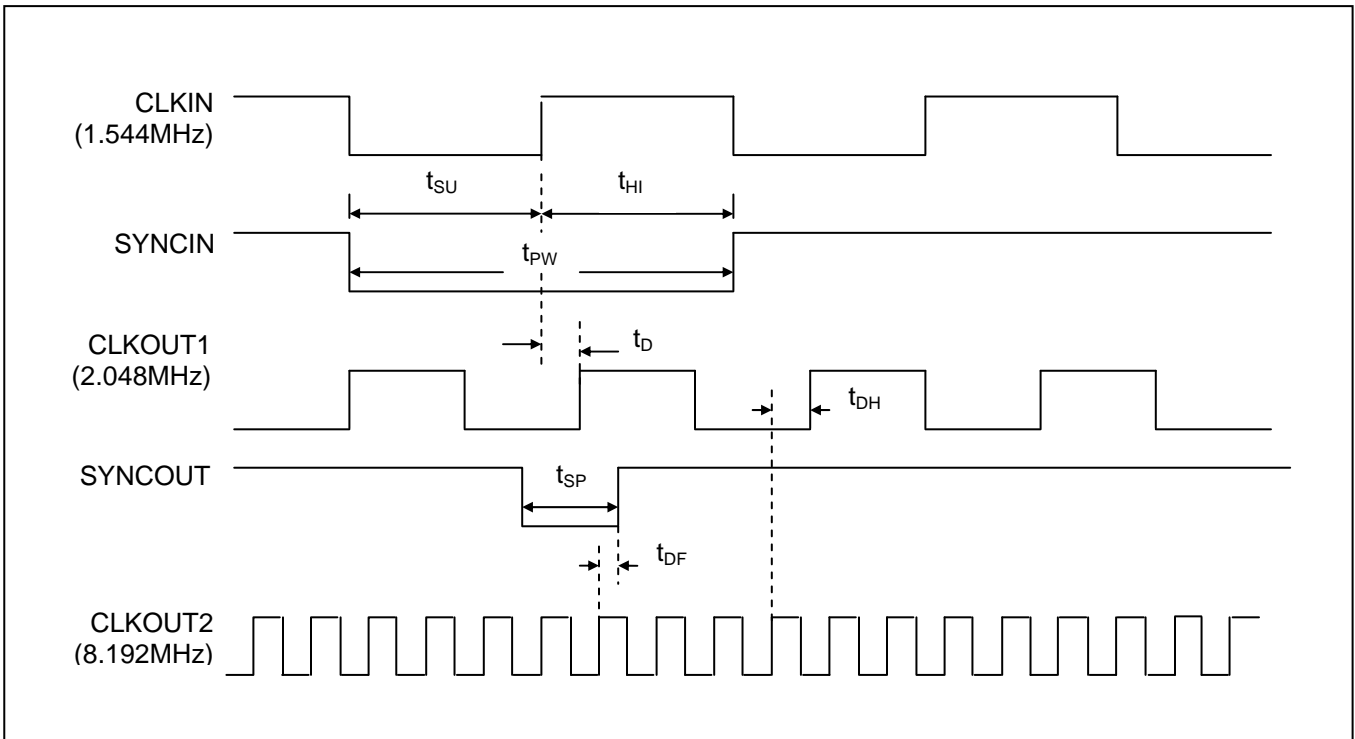
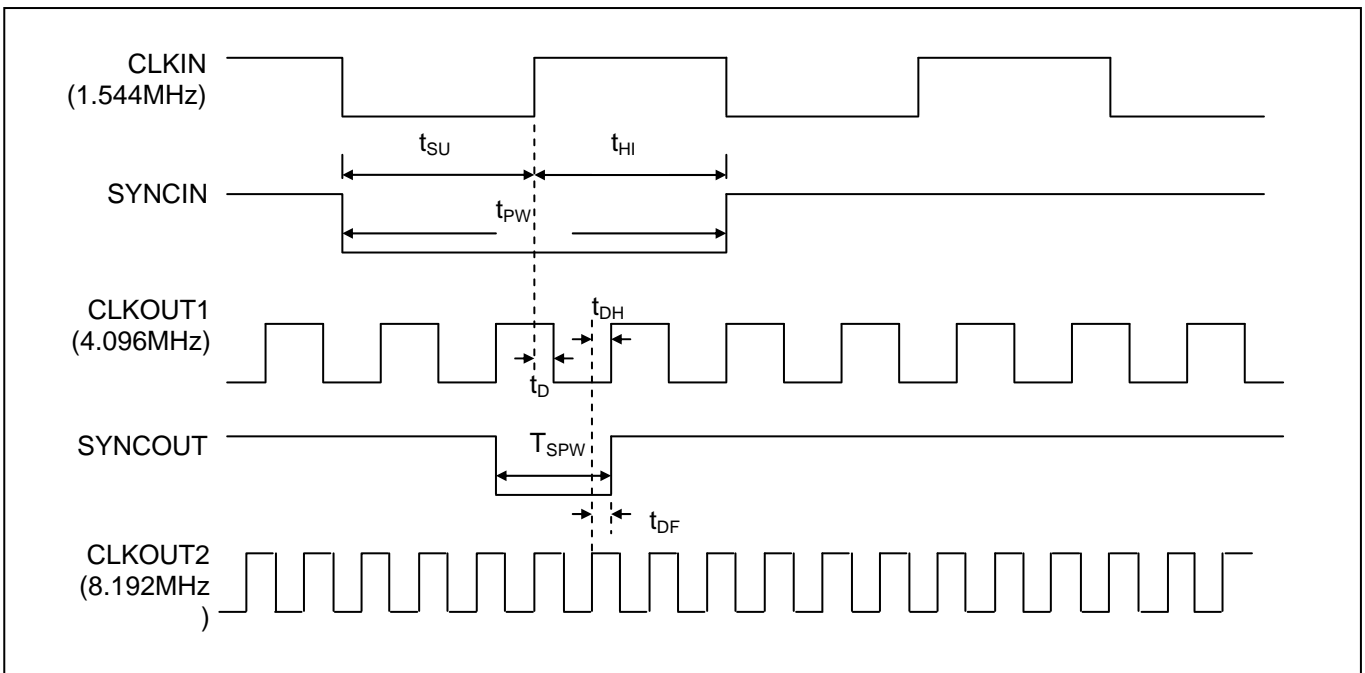


Figure 4-5. DS21604 Low-to-High Frequency Conversion Frame-Sync Alignment



5. PACKAGE INFORMATION

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|--------------|--------------|-------------------------|
| 16 SO | W16+11 | 21-0042 |
| 8 PDIP | P8+8 | 21-0043 |

6. REVISION HISTORY

| REVISION | DESCRIPTION |
|----------|--|
| 082100 | Preliminary release. |
| 083100 | Added package specifications. |
| 090100 | Correct operating voltage range. |
| 011101 | Added mechanical drawing for DIP package. |
| 092801 | Added jitter specifications and pin list for all packages; added timing diagrams. |
| 032002 | Updated jitter specifications. |
| 032803 | Added 3.3V operation specifications. |
| 113004 | Added the spec for soldering temperature in the <i>Absolute Maximum Ratings</i> section. |
| 112105 | Changed timing specs in DC Characteristics and AC Timing tables to guaranteed by design. |
| 011606 | Added lead-free packages to Ordering Information on page 1. |

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