Features

- +18 dBm Output Power
- -20 dBc Fundamental Leakage
- 100% RF, DC and Output Power Testing
- Lead-Free 3 mm 16-lead QFN Package
- RoHS* Compliant

Applications

- Point-to-Point Radio
- Microwave
- LMDS
- SATCOM
- VSAT

Description

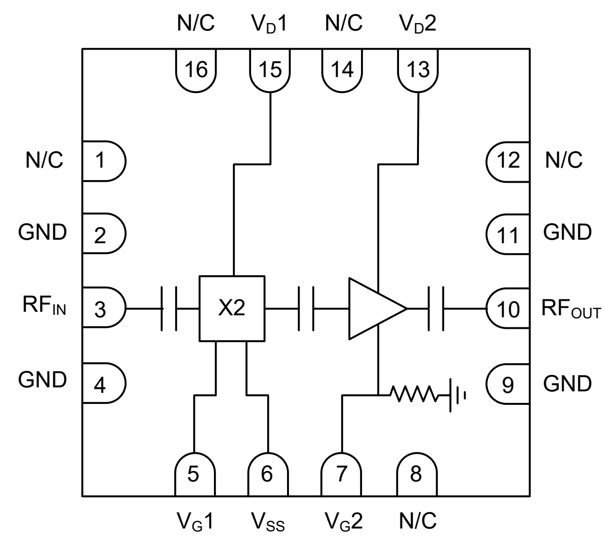
The XX1000-QT is a 7.5 - 22.5 / 15.0 - 45.0 GHz SMD active doubler that delivers +18 dBm of output power. The device combines an active doubler with an output buffer amplifier that delivers constant power over a range of input powers. The device has excellent rejection of the fundamental and harmonic products.

This device uses MACOM's 0.15 GaAs pHEMT device model technology to ensure high reliability and uniformity. The device comes in a lead-free 3 mm QFN surface mount plastic package offering excellent RF and thermal properties and is RoHS compliant.

Ordering Information

Part Number	Package
XX1000-QT-0G00	bulk quantity
XX1000-QT-0G0T	tape and reel
XX1000-QT-EV1	evaluation module

Functional Block Diagram



Pin Configuration[1]

Pin #	Pin Name	Function
1,8,12,14,16	N/C	Not Connected
2,4,9,11	GND	Ground
3	RF_{IN}	RF Input
5	V_G1	Gate Voltage 1
6	V_{SS}	Source Voltage
7	V_G2[1]	Gate Voltage 2
10	RF_{OUT}	RF Output
13	V_D2	Drain Voltage 2
15	V_D1	Drain Voltage 1
17[2]	GND	Ground Pad

1. V_G2 can be used for current regulating V_D2 or V_G2 can be set to GND with V_D2 self-biasing at approximately 140 mA.
2. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: Input Frequency = 7.5 - 22.5 GHz, T_A = +25°C

Parameter	Units	Min.	Typ.	Max.
Output Frequency Range	GHz	15	—	45
Input Return Loss	dB	—	15	—
Output Return Loss	dB	—	7	—
Saturated Output Power	dBm	—	18	—
RF Input Power	dBm	-10	—	+10
Fundamental Leakage	dBc	—	20	—
Third Harmonic Leakage	dBc	—	30	—
Fourth Harmonic Leakage	dBc	—	10	—
Drain Bias Voltage	VDC	—	+5.0	+5.5
Gate Bias Voltage 1	VDC	-0.8	-0.6	-0.4
Gate Bias Voltage 2	VDC	-1.2	0.0	+0.1
Supply Current (I_D1,2) (V_D = 5.0 V, V_G1 = -0.6 V, V_G2 = 0.0 V Typ.)	mA	—	265	280
Source Voltage	VDC	-5.5	-5.0	-2.0
Source Current	mA	25	50	60

Absolute Maximum Ratings[3]

Parameter	Absolute Maximum
Drain Voltage (V_D)	+6 V
Source Voltage (V_{SS})	-6 V
Drain Current (I_D)	320 mA
Source Current (I_{SS})	60 mA
Gate Voltage (V_G1)	-0.4 V
Gate Voltage (V_G2)	+0.1 V
RF Input Power	+15 dBm
Storage Temperature	-65°C to +165°C
Operating Temperature	-55°C to MTTF Table
Channel Temperature	MTTF Table

3. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

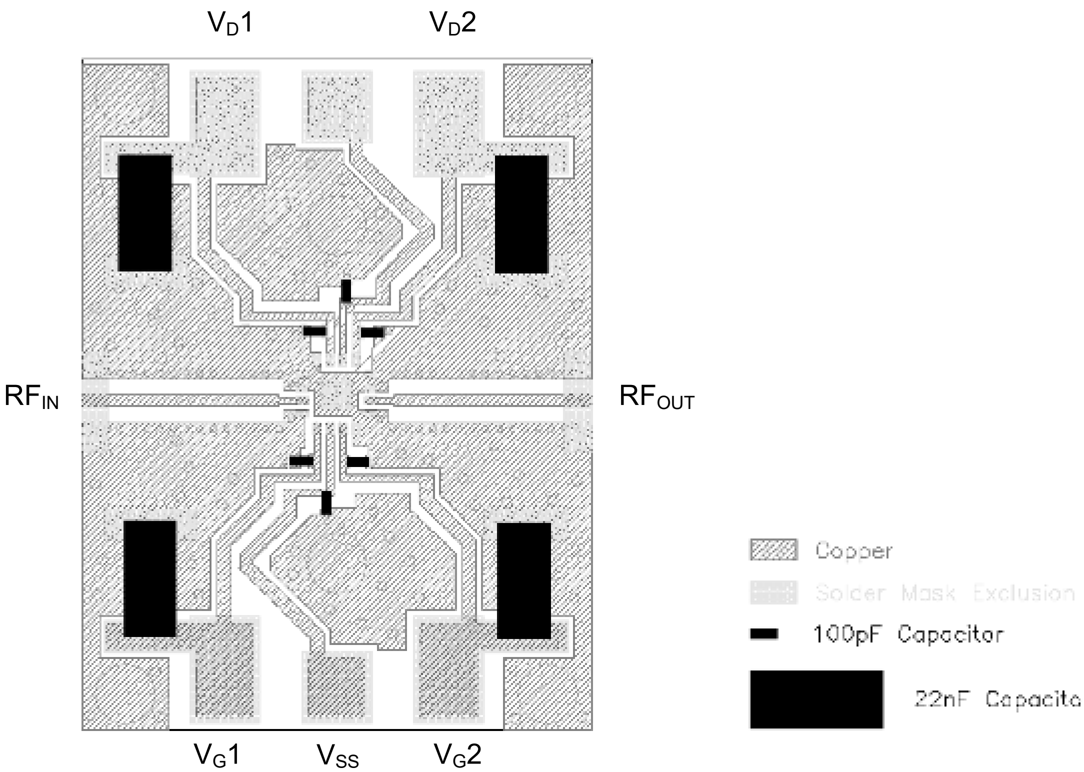
Handling Procedures

Please observe the following precautions to avoid damage:

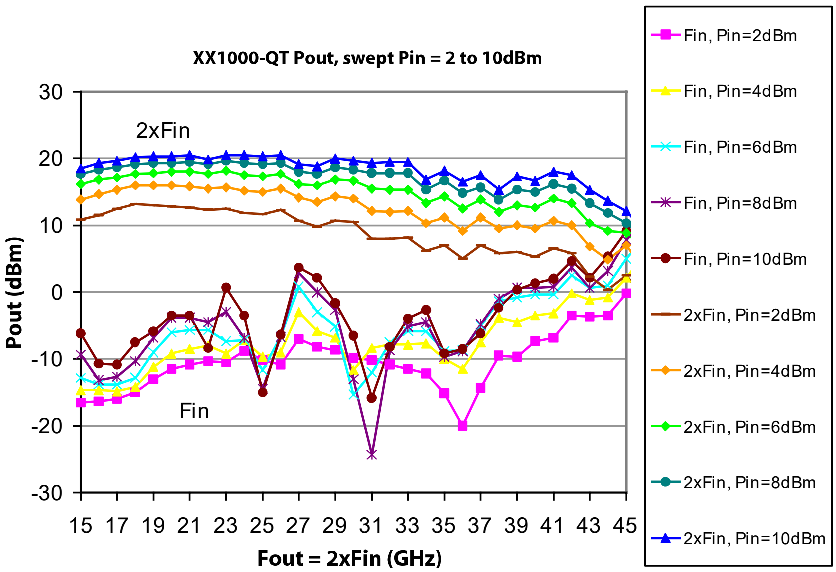
Static Sensitivity

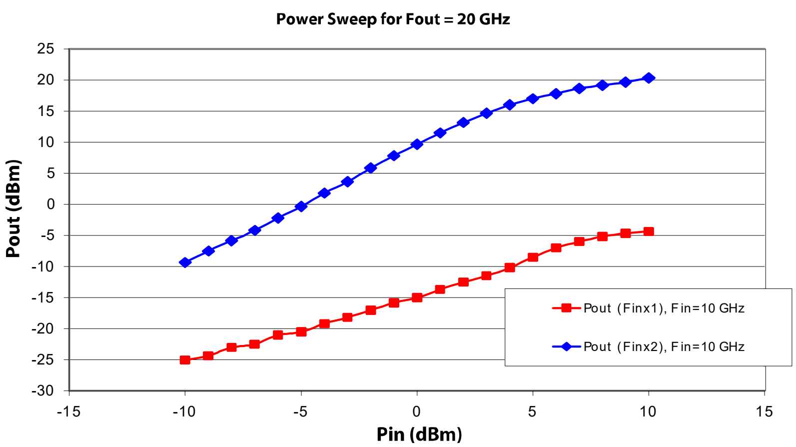
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 2 devices.

PCB Layout


V_D1
V_D2
RF_{IN}
RF_{OUT}
V_G1
V_{SS}
V_G2
Copper
Solder Mask Exclusion
100pF Capacitor
22nF Capacitor

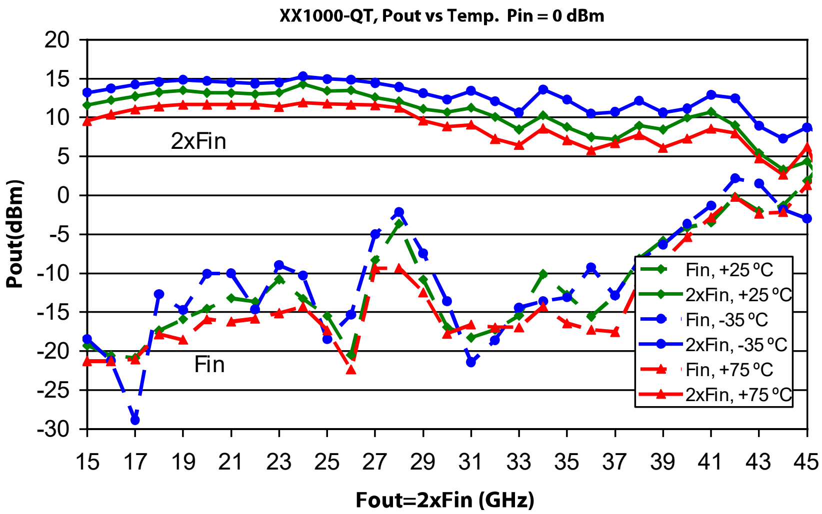
Typical Performance Curves: Nominal Bias Conditions

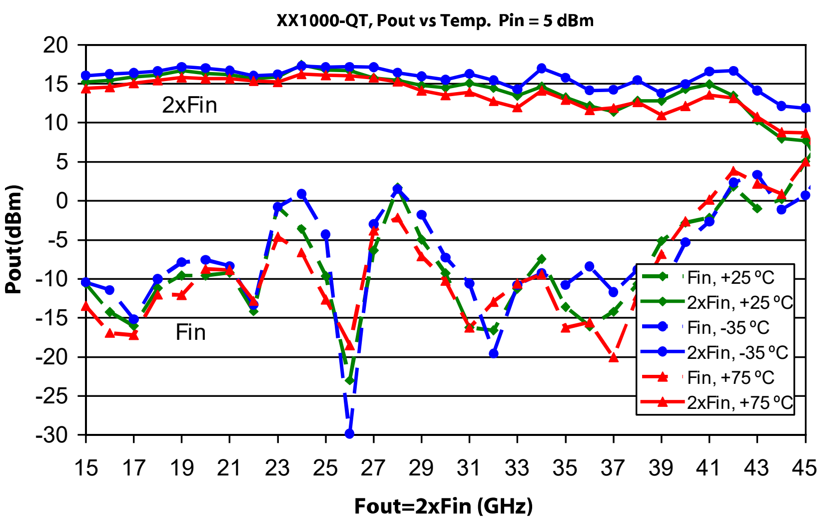




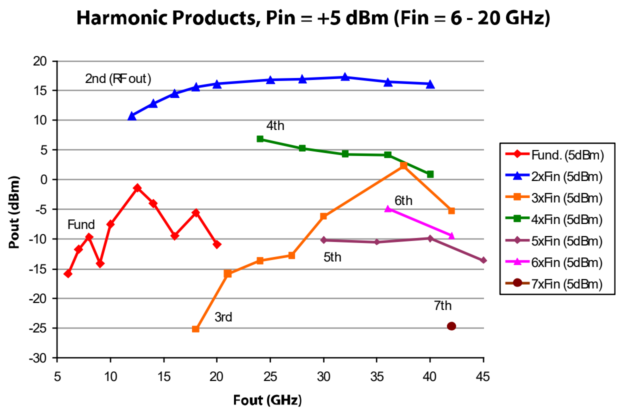
Measured results taken at room temperature in 40 GHz connectorized test fixture with no de-embedding.

Typical Performance Curves (cont.)

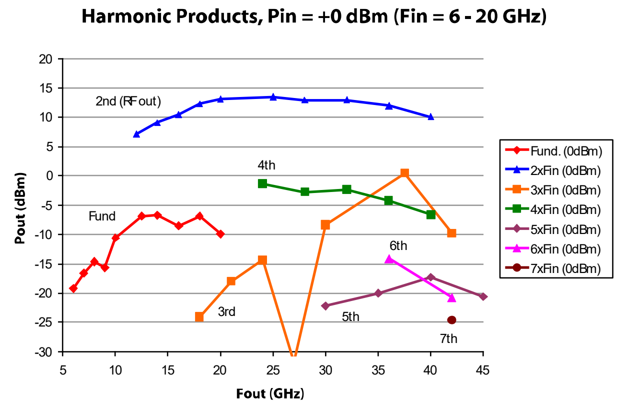




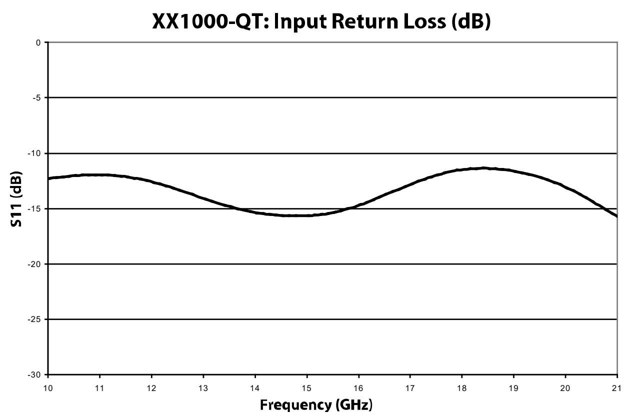
Typical Performance Curves (cont.)



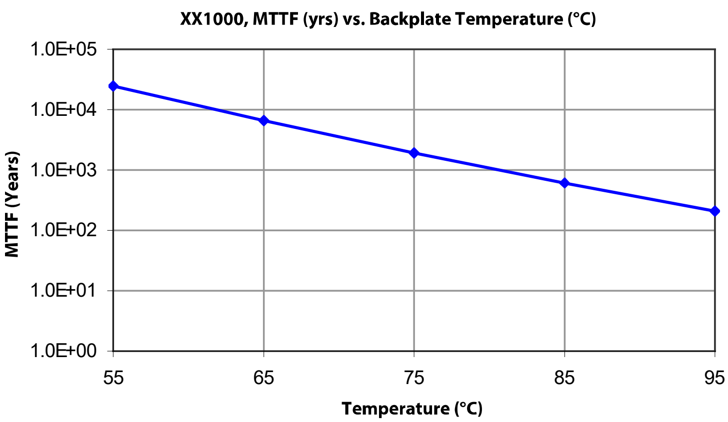
* Measured on-wafer with pre-packaging.



* Measured on-wafer with pre-packaging.



MTTF



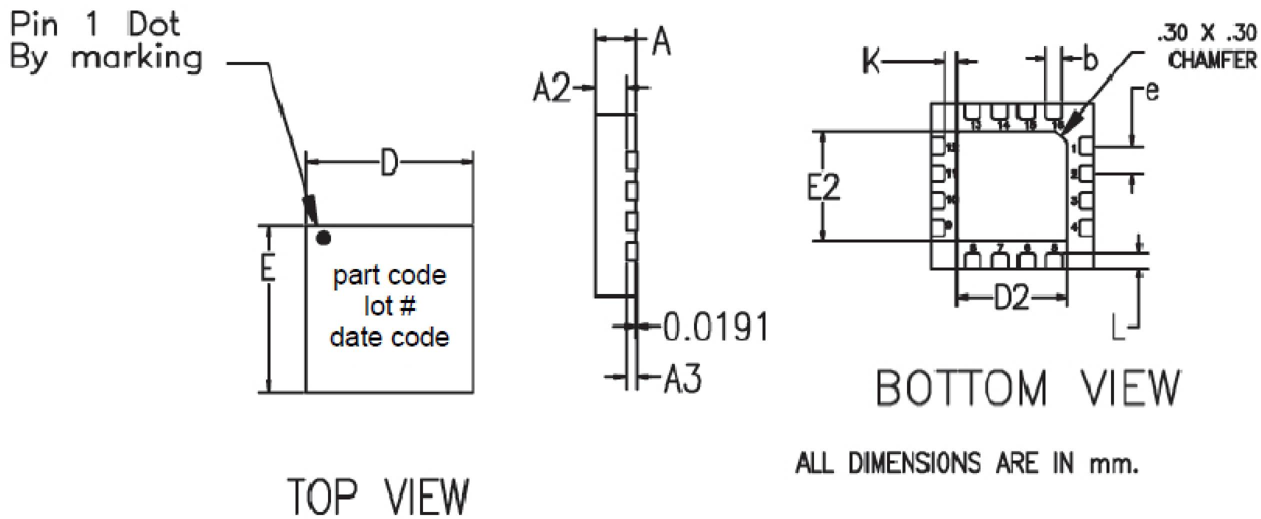
MTTF is calculated from accelerated life-time data of single devices and assumes isothermal back-plate.

Bias Conditions: V_D1,2 = 5 V, I_D1,2 = 220 mA, V_{SS} = -5 V, I_{SS} = 50 mA

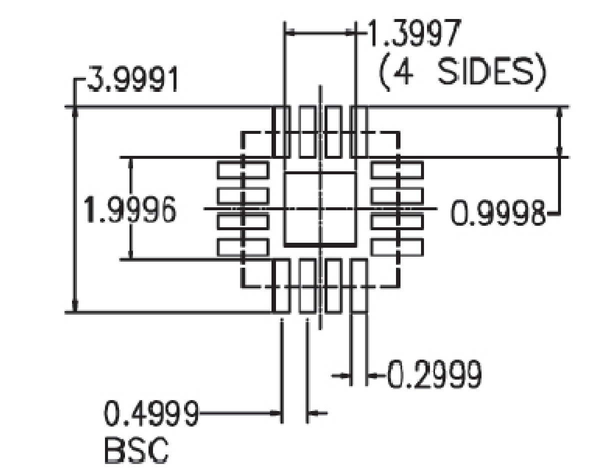
App Note [1] Biasing -
It is recommended to separately bias each doubler stage with fixed voltages of V_D(1,2) = 5 V, V_{SS} = -5 V and V_G1=-0.6 V. The typical DC currents are I_D1 = 80 mA, I_D2 = 140 mA and I_{SS} = 50 mA. V_G2 can be used for active control biasing of V_D2, or it can be set to GND and V_D2 will self bias at approximately 140 mA. Maximum output power is achieved with V_{SS} = -5 V and I_{SS} = 50 mA but the device will operate with reduced bias to V_{SS} = -2 V and I_{SS} = 25 mA. It is also recommended to use active biasing on V_D2 with V_G2 to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage for V_G2 = -0.1 V. Typically the gate is protected with silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

Lead-Free Package Dimensions/Layout

QT (3x3 mm)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



	MIN	TYP	MAX
A	0.80	0.90	1.00
A3	0.20 REF		
A2	0.00	0.65	1.00
b	0.20	0.25	0.30
K	0.20	–	–
D	3.00 BSC		
E	3.00 BSC		
e	0.50		
D2	1.50	1.65	1.80
E2	1.50	1.65	1.80
L	0.16	0.26	0.36

VIEWS ARE NOT TO SCALE: USE DIMENSIONS AND TABLE.

Plating is 100% matte tin over copper.