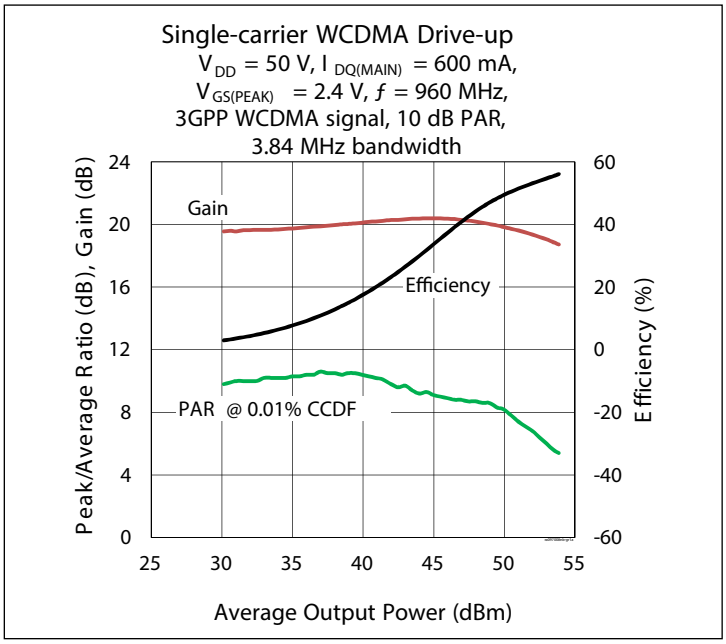
PTRA097008NB

Thermally-Enhanced High Power RF LDMOS FET
630 W, 48 V, 920 – 960 MHz

PTRA097008NB
Package PG-HB2SOF-6-1

Description

The PTRA097008NB is a 630-watt LDMOS FET intended for use in multi-standard cellular power amplifier applications in the 920 to 960 MHz frequency band. Features include input and output matching, high gain and thermally-enhanced package with earless flanges. Manufactured with an advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



Features

- Broadband internal input and output matching
- Asymmetric design
  - Main: P_{1dB} = 300 W typical
  - Peak: P_{1dB} = 400 W typical
- Typical pulsed CW performance (10 µs, 10% duty cycle, class AB test), 942 MHz, 48 V, combined outputs, Doherty configuration
  - Output power at P_{1dB} = 180 W
  - Output power at P_{3dB} = 600 W
  - Efficiency = 52%
  - Gain = 19 dB
- Capable of handing 10:1 VSWR at 48 V, 89 W (CW)output power
- Integrated ESD protection
- Human Body Model Class 2 (per ANSI/ESDA/JEDEC JS-001)
- Low thermal resistance
- Pb-free and RoHS-compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in the Doherty test fixture)
V_{DD} = 50 V, I_{DQ} = 600 mA, $V_{GS(PEAK)}$ = 2.4 V, P_{OUT} = 90 W avg, f_1 = 960 MHz, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	18.25	19	—	dB
Drain Efficiency	η_D	46.5	49	—	%
Adjacent Channel Power Ratio	ACPR	—	–29	–26	dBc
Output PAR @ 0.01% CCDF	OPAR	6.0	6.8	—	dB

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

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DC Characteristics (each side)

Characteristic		Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage		V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	105	—	—	V
Drain Leakage Current		V_{DS} = 50 V, V_{GS} = 0 V	I_{DSS}	—	—	1	µA
		V_{DS} = 105 V, V_{GS} = 0 V	I_{DSS}	—	—	10	µA
On-State Resistance	(Main)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.07	—	Ω
	(Peak)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.05	—	Ω
Operating Gate Voltage	(Main)	V_{DS} = 48 V, I_{DQ} = 600 mA	V_{GS}	3	3.65	4	V
	(Peak)	V_{DS} = 48 V, I_{DQ} = 0 mA	V_{GS}	—	2.4	—	V
Gate Leakage Current		V_{GS} = 14 V, V_{DS} = 0 V	I_{GSS}	—	—	1	µA

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	105	V
Gate-Source Voltage	V_{GS}	–6 to +12	V
Operating Voltage	V_{DD}	0 to +55	V
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	°C

1. Operation above the maximum values listed here may cause permanent damage. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For reliable continuous operation, the device should be operated within the operating voltage range (V_{DD}) specified above.
2. Parameters values can be affected by end application and product usage. Values may change over time.

Thermal Characteristics

Parameter		Symbol	Value	Unit
Thermal Resistance	Main (T_{CASE} = 70°C, P_{avg} = 90 W CW)	$R_{\theta JC}$	0.45	°C/W

Moisture Sensitivity Level

Level	Test Signal	Package Temperature	Unit
3	IPC/JEDEC J-STD-020	260	°C

Ordering Information

Type and Version	Order Code	Package Description	Shipping
PTRA097008NB V1 R2	PTRA097008NB-V1-R2	PG-HB2SOF-6-1	Tape & Reel, 250 pcs

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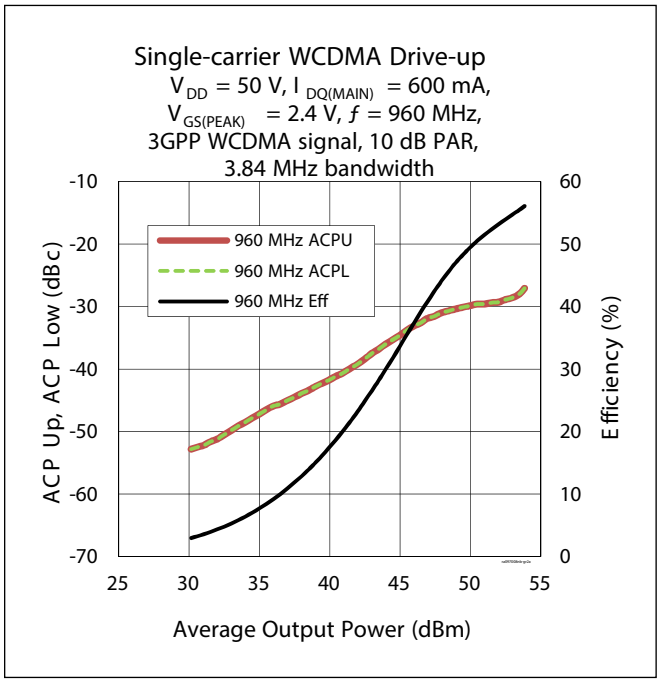
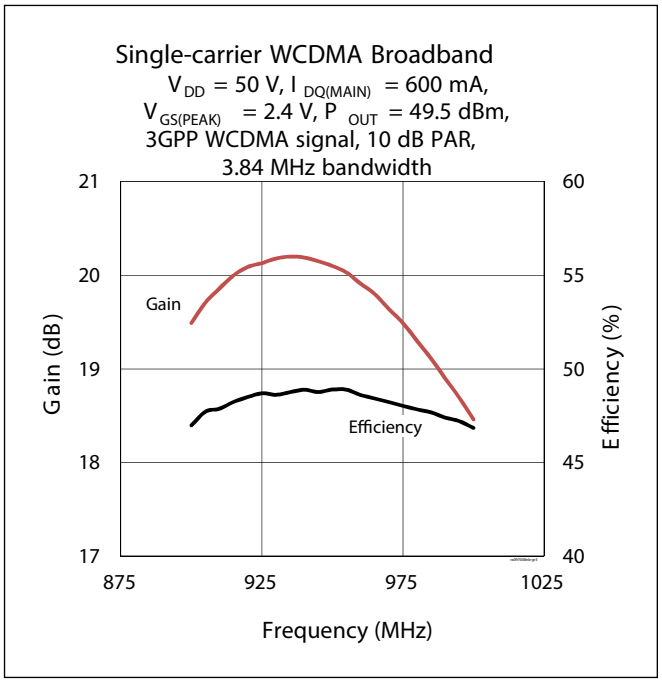
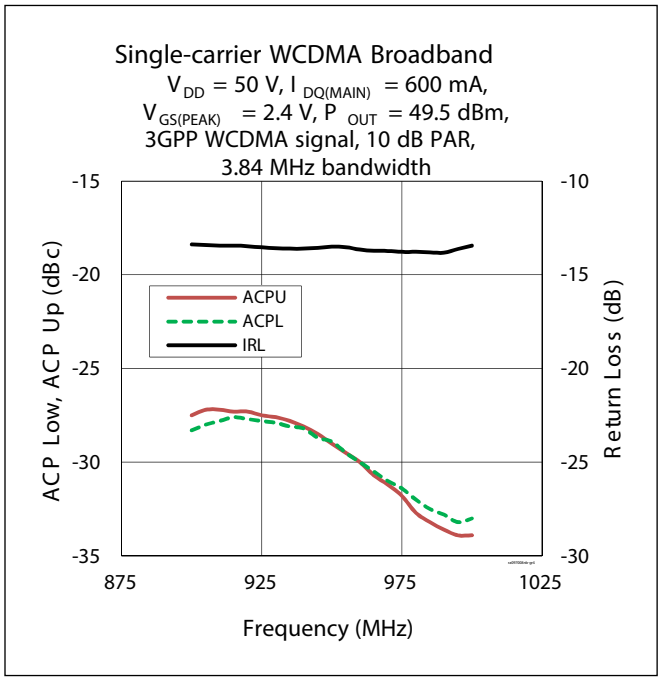
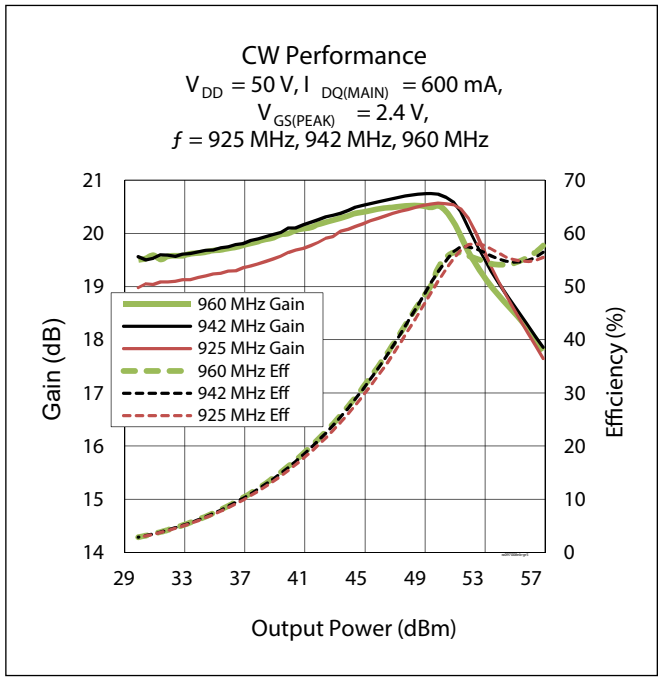
Typical Performance (data taken in a production test fixture)









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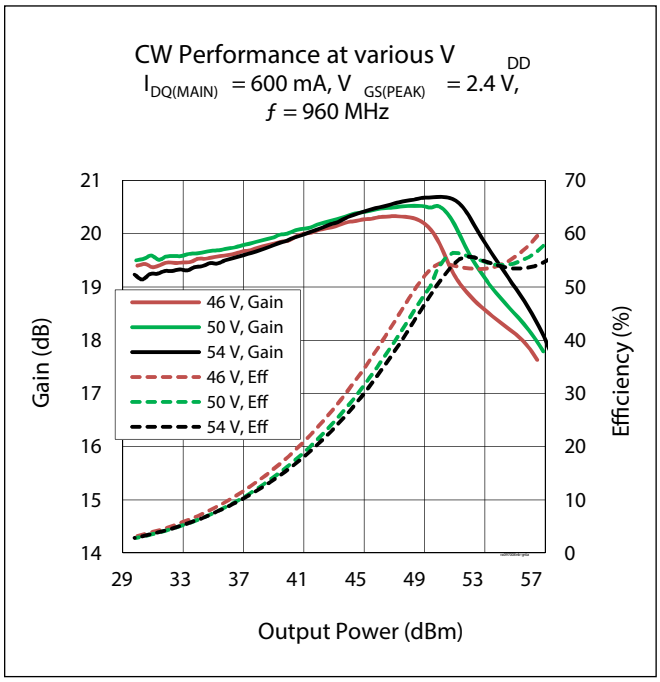
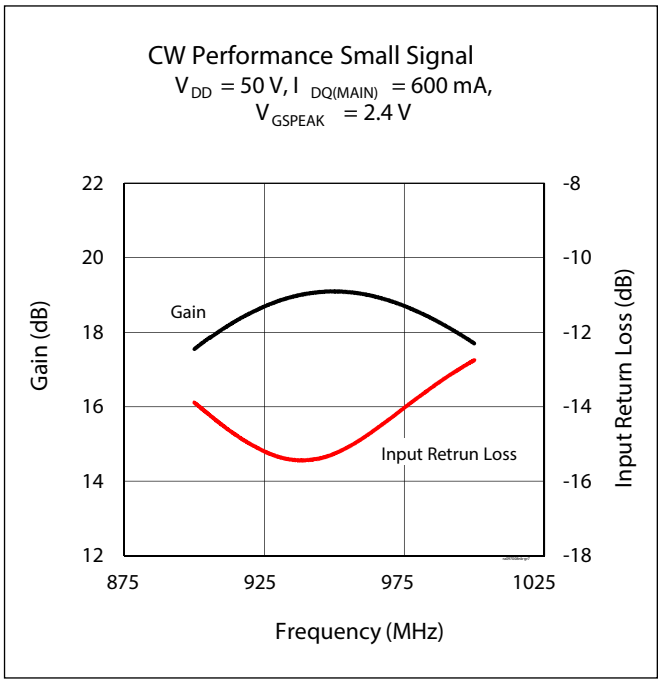
Typical Performance (cont.)





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Load Pull Performance

Main Side Load Pull Performance – Pulsed CW signal – 100 µsec, 10% duty cycle, 48 V, IDQ = 600 mA, class AB

		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]
925	3.3 – j4.4	1.4 – j1.0	21.0	54.85	305	62.5	1.9 + j0.4	22.3	52.43	175	68.4
960	2.9 – j5.1	1.1 – j1.0	20.7	54.73	297	60.0	1.8 - j0.2	22.1	53.05	201	68.5

		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]
925	3.3 – j4.4	1.18 – j1.06	18.3	55.53	357	60.6	1.7 + j0.1	20.5	53.54	225	70.5
960	2.9 – j5.1	1.12 – j1.22	18.6	55.40	346	59.1	1.8 - j0.2	20.1	53.80	239	70.7

Peak Side Load Pull Performance – Pulsed CW signal – 100 µsec, 10% duty cycle, 48 V, V_{GSPK} = 3.58 V, class AB

		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]
925	3.2 – j5.9	0.7 – j0.6	20.2	56.44	440	58.0	1.2 + j0.2	21.9	53.51	224	66.3
960	3.7 – j6.3	0.8 – j0.9	20.0	56.23	419	58.7	1.3 + j0.2	21.2	53.32	214	65.8

		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]
925	3.2 – j5.9	0.67 – j0.64	18.2	57.17	521	60.3	1.1 - j0.2	19.6	55.81	381	67.9
960	3.7 – j6.3	0.82 – j0.92	18.0	57.09	511	61.1	1.2 - j0.4	19.0	55.51	355	67.3

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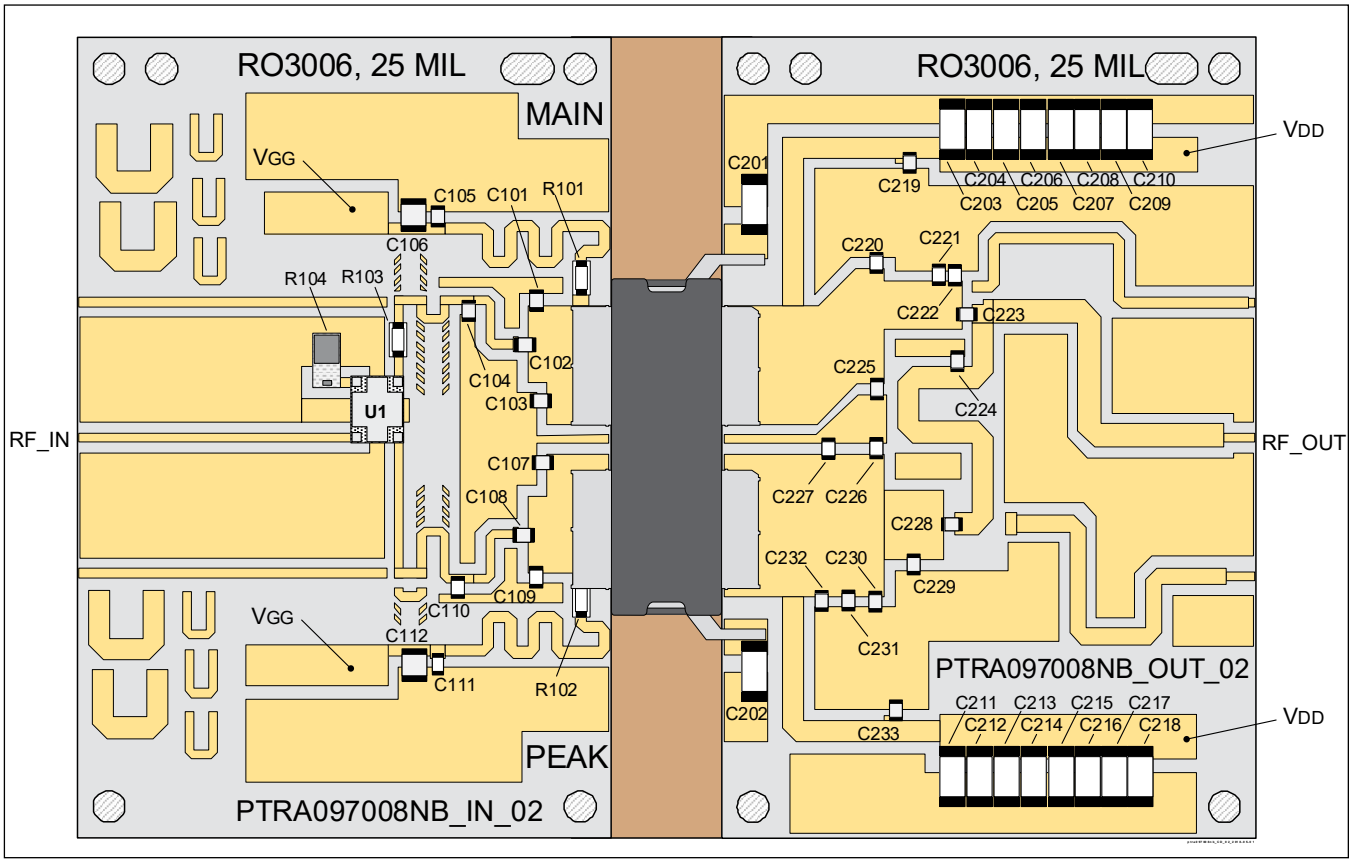
Reference Circuit tuned for 920 to 960 MHz

DUT	PTRA097008NB-V1
Reference Circuit Part No.	LTA/PTRA097008NB-V1
PCB	Rogers 3006, 0.064 mm [.025"] thick, 2 oz. copper, ε_r = 6.50



Reference circuit assembly diagram (not to scale)

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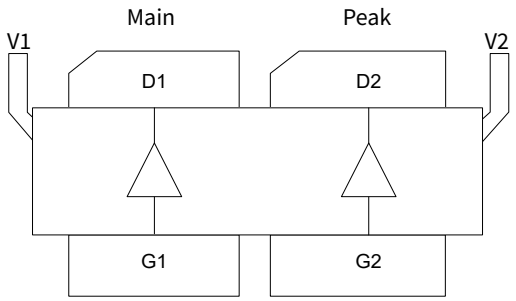
Reference Circuit (cont.)

Components Information

Component	Description	Manufacturer	P/N
Input			
C101, C103, C107	Capacitor, 4.7 pF	ATC	ATC600F4R7CT250X
C102, C108	Capacitor, 36 pF	ATC	ATC600F360JT250X
C104, C109	Capacitor, 3.0 pF	ATC	ATC600F3R0CT250X
C105, C111	Capacitor, 39 pF	ATC	ATC600F390JT250X
C106, C112	Capacitor, 10 µF, 50 V	Taiyo Yuden	UMK325C7106MM-T
C110	Capacitor, 2.4 pF	ATC	ATC600F2R4CT250X
R101, R102, R103	Chip resistor, 5.1 ohms	Panasonic	ERJ-8GEYJ5R1V
R104	Resistor, 50 ohms	Richardson	C16A50Z4
U1	Hybrid coupler	Anaren	X3C09P1-03S
Output			
C201, C202, C203, C204, C205, C206, C207, C208, C209, C210, C211, C212, C213, C214, C215, C216, C217, C218	Capacitor, 10 µF, 100 V	TDK Corporation	C5750X7S2A106M230KB
C219, C228, C233	Capacitor, 39 pF	ATC	ATC600F390JT250X
C220, C224, C225	Capacitor, 3.3 pF	ATC	ATC600F3R3CT250X
C221	Capacitor, 0.3 pF	ATC	ATC600F0R3CT250X
C222	Capacitor, 1.2 pF	ATC	ATC600F1R2CT250X
C223	Capacitor, 12 pF	ATC	ATC600F120JT250X
C226	Capacitor, 5.1 pF	ATC	ATC600F5R1CT250X
C227	Capacitor, 8.2 pf	ATC	ATC600F8R2CT250X
C229	Capacitor, 1.0 pF	ATC	ATC600F1R0CT250X
C230, C231	Capacitor, 2.0 pF	ATC	ATC600F2R0CT250X
C232	Capacitor, 7.5 pF	ATC	ATC600F7R5CT250X

Pinout Diagram (top view)



Pin	Description
D1	Drain Device 1 (main)
D2	Drain Device 2 (peak)
G1	Gate Device 1 (main)
G2	Gate Device 2 (peak)
Source	Bottom metallization
V1, V2	Drain video decoupling, no DC bias

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Package Outline Specifications

Package PG-HB2SOF-6-1 (top and side views)

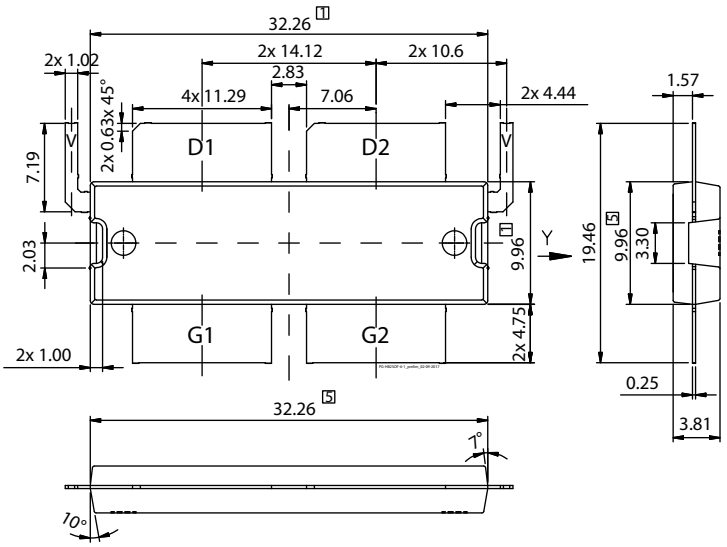

Diagram Notes—unless otherwise specified:

1. Mold/dam bar/metal protrusion of 0.30 mm max per side not included
2. Fillets and radii: all radii are 0.30t mm max
3. Interpret dimensions and tolerances per ISO 8015
4. Dimensions are mm
5. Does not include mold/dam bar and metal protrusion
6. All tolerances ± 0.1 mm
7. All metal surfaces tin pre-plated, except area of cut
8. Lead thickness: 0.25 mm
9. Pins: D1, D2 – drain; G1, G2 – gate; Source – bottom metallization;
   V – drain video decoupling, no DC bias

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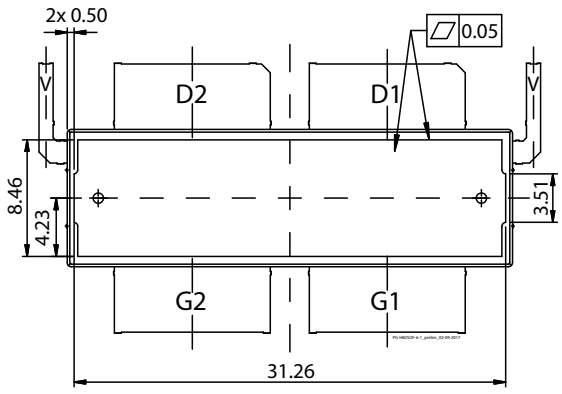
Package Outline Specifications

Package PG-HB2SOF-6-1 (bottom view)



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