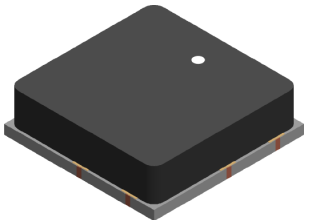
MSW310x-310

SP3T PIN Diode Switch

Rev. V2

Features

- Wide Frequency Range: 50 MHz to 4 GHz, in 2 bands
- Surface Mount SP3T Switch in Compact Outline: 8 mm L x 5 mm W x 2.5 mm H
- Higher Average Power Handling than Plastic Packaged
- MMIC Switches: 158 W CW
- High RF Peak Power: 500 W
- Low Insertion Loss: 0.45 dB
- High IIP3: 65 dBm
- Operates From Positive Voltage Only: 5 V & 28 V to 125 V
- RoHS* Compliant



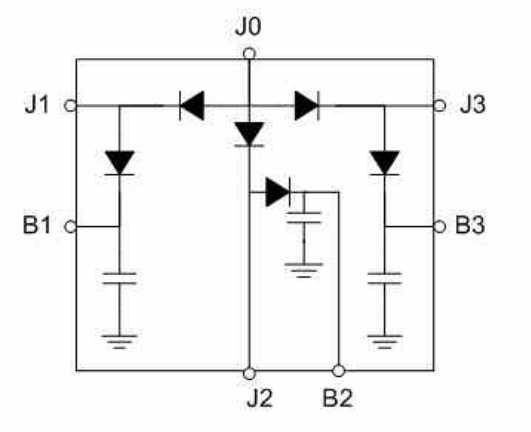
CS310

Description

The MSW3100-310 (50 MHz - 1 GHz) and MSW3101-310 (400 MHz - 4 GHz) series of surface mount silicon PIN diode SP3T switches can be used for high power transmit/receive (TR) symmetrical switching or active receiver protection. These switches are manufactured using a proven hybrid manufacturing process incorporating high voltage PIN diodes and passive devices integrated on a ceramic substrate. These low profile, compact, surface mount components offer superior small and large signal performance compared to that of MMIC devices in QFN packages. The SP3T switches are designed in a symmetrical topology to enable switched RF port to be used as the high-input-power -handling port, to minimize insertion loss and to maximize isolation performance. The very low thermal resistance (<25ºC/W) of the PIN diodes in these devices enables them to reliably handle RF incident power levels of 50 dBm CW and RF peak incident power levels of 57 dBm in cold switching applications. The thick I layers of the PIN diodes (>100 µm), coupled with their long minority carrier lifetime (>2 µs), produces input third order intercept point (IIP3) greater than 65 dBm.

These MSW310x-310 Series SP3T switches are designed to be used in high average and peak power switch applications, operating from 50 MHz to 4 GHz in two bands, which utilize high volume, surface mount, solder re-flow manufacturing. These products are durable and capable of reliably operating in military, commercial, and industrial environments.

Functional Schematic



Ordering Information

Part Number	Package
MSW3100-310-T	tube
MSW3100-310-R	250 or 500 piece reel
MSW3100-310-W	Waffle pack
MSW3101-310-T	tube
MSW3101-310-R	250 or 500 piece reel
MSW3101-310-W	Waffle pack
MSW3100-310-E	RF evaluation board
MSW3101-310-E	RF evaluation board

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

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MSW3100-310 Electrical Specifications: T_A = +25°C, P_{IN} = 0 dBm, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Frequency	—	MHz	50	—	1000
Insertion Loss	Bias State 1: port J0 to J1 Bias State 2: port J0 to J2 Bias State 2: port J0 to J3	dB	—	0.4	0.6
Return Loss	Bias State 1: port J0 to J1 Bias State 2: port J0 to J2 Bias State 2: port J0 to J3	dB	18	20	—
Isolation	Bias State 1: port J0 to J1 Bias State 2: port J0 to J2 Bias State 2: port J0 to J3	dB	50	53	—
CW Incident Power[1]	Source & Load VSWR = 1.5:1	dBm	—	—	50
Peak Incident Power[1]	Source & Load VSWR = 1.5:1 Pulse Width = 10 µs, Duty Cycle = 1%	dBm	—	—	57
Switching Time[2]	10% -90% RF Voltage, TTL rep rate = 100 kHz	µs	—	2	3
Input IP3	F1 = 500 MHz, F2 = 510 MHz P1 = P2 = 10 dBm Measure on path biased to low loss state	dBm	60	65	—

MSW3101-310 Electrical Specifications: T_A = +25°C, P_{IN} = 0 dBm, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Frequency	—	MHz	400	—	4000
Insertion Loss	Bias State 1: port J0 to J1 Bias State 2: port J0 to J2 Bias State 2: port J0 to J3	dB	—	0.6	0.8
Return Loss	Bias State 1: port J0 to J1 Bias State 2: port J0 to J2 Bias State 2: port J0 to J3	dB	14	15	—
Isolation	Bias State 1: port J0 to J1 Bias State 2: port J0 to J2 Bias State 2: port J0 to J3	dB	32	34	—
CW Incident Power[1]	Source & Load VSWR = 1.5:1	dBm	—	—	50
Peak Incident Power[1]	Source & Load VSWR = 1.5:1 Pulse Width = 10 µs, Duty Cycle = 1%	dBm	—	—	57
Switching Time[2]	10% -90% RF Voltage, TTL rep rate = 100 kHz	µs	—	2	3
Input IP3	F1 = 500 MHz, F2 = 510 MHz P1 = P2 = 10 dBm Measure on path biased to low loss state	dBm	60	65	—

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1. PIN diode DC reverse voltage to maintain high resistance in the OFF PIN diode is determined by RF frequency, incident power, and VSWR as well as by the characteristics of the diode. The minimum reverse bias voltage values are provided in this datasheet. The input signal level applied for small signal testing is approximately 0 dBm.
2. Switching Speed (50 % TTL – 10/90 % RF Voltage) is a function of the PIN diode driver performance as well as the characteristics of the diode. An RC "current spiking network" is used on the driver output to provide a transient current to rapidly remove stored charge from the PIN diode. Typical component values are: R = 50 to 220 Ω and C = 470 to 1,000 pF. MACOMs MPD3T28125-700 is the recommended PIN diode driver to interface with the MSW3100-310, MSW3101-310 SP3T switches.

Truth Table

Port J0 - J1	Port J0 - J2	Port J0 - J3	Bias: J1	Bias: J2	Bias: J2	Bias: B1	Bias: B2	Bias: B3	Bias: J0
Low Loss	Isolation	Isolation	0 V, -100 mA	+27 V, 0 mA	+27 V, 0 mA	+27 V, 0 mA	0 V, -25 mA	0 V, -25 mA	+5 V, +100 mA
Isolation	Low Loss	Isolation	+27 V, 0 mA	0 V, -100 mA	+27 V, 0 mA	0 V, -25 mA	+27 V, 0 mA	0 V, -25 mA	+5 V, +100 mA
Isolation	Isolation	Low Loss	+27 V, 0 mA	+27 V, 0 mA	0 V, -100 mA	0 V, -25 mA	0 V, -25 mA	+27 V, 0 mA	+5 V, +100 mA

RF Bias Network Component Values

Part #	Frequency (MHz)	Inductors	DC Blocking Capacitors	RF Bypass Capacitors
MSW3100-310	50 - 1000	4.7 µH	0.1 µF	0.1 µF
MSW3101-310	400 - 4000	82 nH	22 pF	270 pF

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Minimum Reverse Bias Voltage[3]: P_{INC} = 125 W CW, Z_0 = 50 Ω with 1.5:1 VSWR

Part #	20 MHz	100 MHz	200 MHz	400 MHz	1 GHz	4 GHz
MSW3100-310	125 V	25 V	85 V	55 V	28 V	N/A
MSW3101-310	N/A	N/A	125 V	85 V	55 V	28 V

3. N/A denotes the switch is not recommended for that frequency band.

The minimum reverse bias voltage required to maintain a PIN diode out of conduction in the presence of a large RF signal is given by:

$$|V_{DC}| = \frac{|V_{RF}|}{\sqrt{1+\left[\left(\frac{0.0142 \times f_{MHz} \times W_{mils}^2}{V_{RF} \times \sqrt{D}}\right) \times \left(1+\sqrt{1+\left(\frac{0.056 \times V_{RF} \times \sqrt{D}}{W_{mils}}\right)^2}\right)\right]^2}}$$

Where:

$|V_{DC}|$ = magnitude of the minimum DC reverse bias voltage
$|V_{RF}|$ = magnitude of the peak RF voltage (including the effects of the VSWR)
F_{MHz} = lowest RF signal frequency expressed in MHz
D = duty factor of the RF signal
W_{MILS} = thickness of the diode I layer, expressed in mils (thousands of an inch)

R. Caverly and G. Hiller, —Establishing the Minimum Reverse Bias for a PIN Diode in a High Power Switch, IEEE Transactions on Microwave Theory and Techniques, Vol.38, No.12, December 1990

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Absolute Maximum Ratings

Parameter	Conditions	Absolute Maximum
Forward Current	J1, J2, J3 port B1, B2, B3 port	250 mA 150 mA
Reverse Voltage	J1, J2, J3 port B1, B2, B3 port	125 V
Forward Diode Voltage	I_F = 250 mA	1.2 V
CW Incident Power Handling[4]	J0, J1, J2, J3 port Source & Load VSWR = 1.5:1, T_C = 85°C, cold switching	50 dBm
Peak Incident Power Handling[4]	J0, J1, J2, J3 port Source & Load VSWR = 1.5:1, T_C = 85°C, cold switching, Pulse Width = 10 µs, Duty Cycle = 1%	57 dBm
Total Dissipated RF & DC Power[4]	T_C = 85°C, cold switching	5 W
Junction Temperature	—	+175°C
Operating Temperature	—	-65°C to +125°C
Storage Temperature	—	-65°C to +150°C
Assembly Temperature	t = 10 s	+260°C

4. Backside RF and DC grounding area of device must be completely solder attached to the RF circuit board vias for proper electrical and thermal circuit grounding.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 1C (HBM) devices. The moisture sensitivity level (MSL) rating for this part is MSL 1.

Environmental Capabilities

The MSW204x-204 diode is capable of meeting the environmental requirements of MIL-STD-202 and MIL-STD-750.

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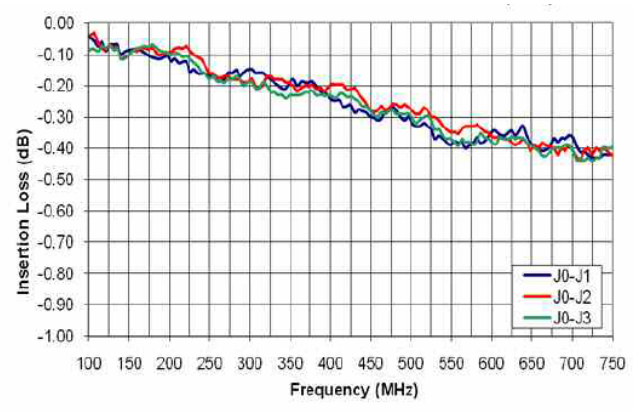
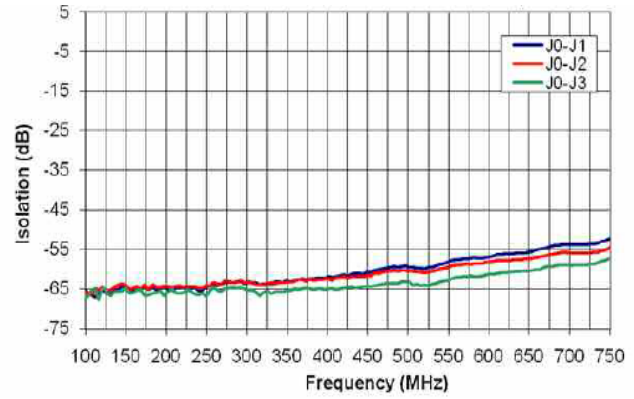
Typical Performance Curves

MSW3100-310

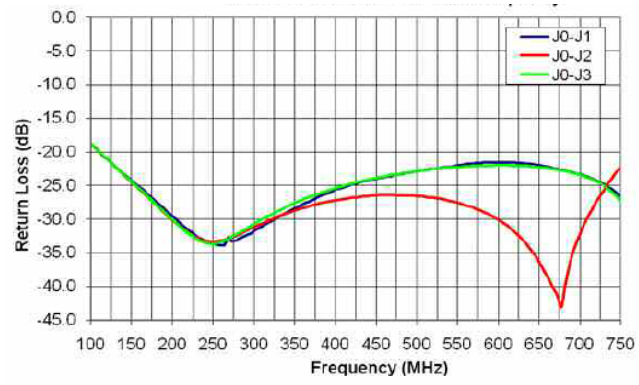
Insertion Loss



Isolation

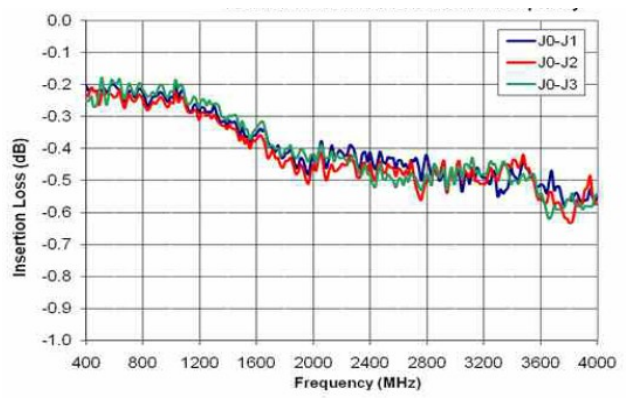


Return Loss

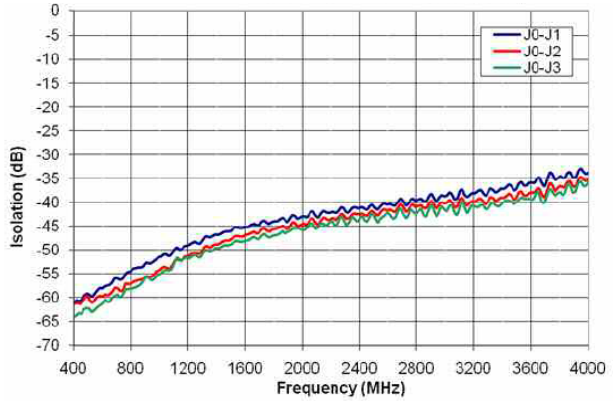


MSW3101-310

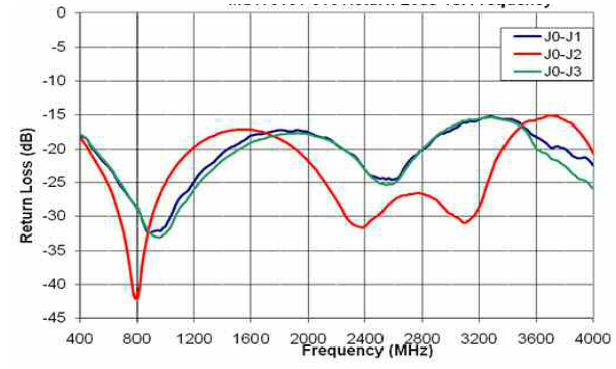
Insertion Loss



Isolation



Return Loss



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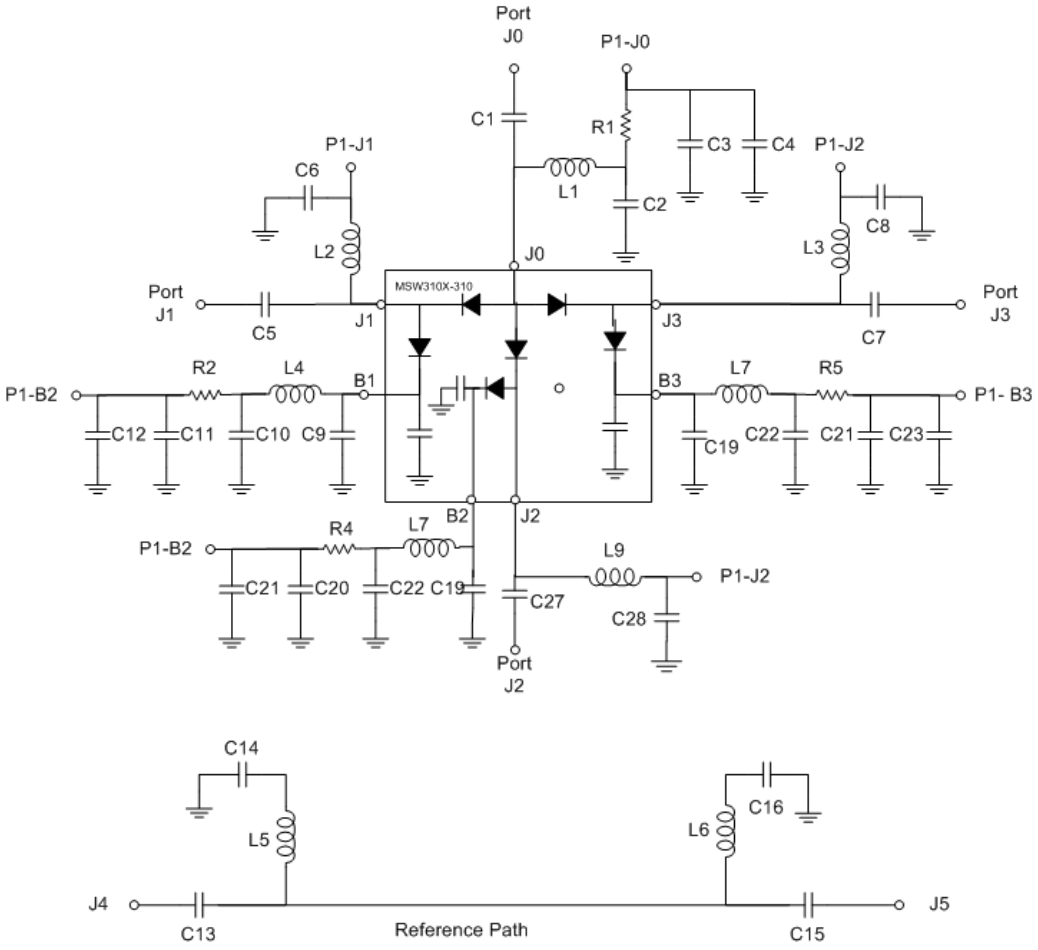
SP3T Switch Evaluation Board Schematic



SP3T Switch Evaluation Board Description

Below is the description of MSW310x-310 SP3T series shunt switch module control using MPD3T28125-701 three channel pin diode driver. The switch module can also be controlled by using external voltage sources accordingly. The MSW310x-310 series shunt three throw switch can be fully controlled using MPD3T28125-701 three channel pin diode driver. Each driver section is connected to bias the series diode and the shunt diode of the switch arms. For example, in the configuration described below for the control of a symmetrical SP3T switch, driver output V1A biases the series diode connected between switch ports J0 and J1, the driver output V1B biases the shunt diode connected between switch ports J1 and B1.

Similarly driver output V2A biases the series diode connected between switch ports J0 and J2, output V2B biases the shunt diode connected between switch ports J2 and B2 and output V3A biases the series diode connected between switch ports J0 and J3, the driver output V3B biases the shunt diode connected between switch ports J3 and B3. A typical symmetric switch with a driver interface is shown below. In this circuit, the MPD3T28125-701 driver is used to control the MSW3100-310 symmetrical SP3T switch. The switch is controlled to operate in one of three operational states, which are called State 1, State 2 and State 3. In the descriptions of States 1, 2 and 3 (below), it is assumed that +VCC1 = 5 V and + VCC2 = 28 V.

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State 1

In State 1, the path from port J0 to J1 is in its low insertion loss condition. The paths from port J0 to port J2, and port J0 to port J3, are in their high isolation states. In State 1, the control voltage applied to CTL 1 is TTL-logic high, and the control voltages applied to CTL 2 and CTL 3 are TTL-logic low. CTL 1 logic forward biases the series PIN diode between the J0 and J1 ports by applying 0 V to the J1 bias input port (P1-J1), CTL2 & CTL 3 will re-verse bias the series diodes connected from port J0 to port J2, and from port J0 to port J3. The magnitude of the resultant bias current through the forward-biased diode is primarily determined by the voltage applied to the J0 bias port (P1-J0) (5 V nominal), the magnitude of the forward voltage across the PIN diode and the resistance of R1. This current is nominally 100 mA. At the same time, the shunt PIN diodes connected between port J2 and B2 and between port J3 and B3 are also forward biased by applying a high bias voltage, nominally 28 V, to the J2 and J3 bias ports (P1-J2, P1-J3) and 0 V to the B2 and B3 bias ports (P1-B2, P1-B3). The magnitudes of the bias currents through these diodes are primarily determined by the voltage applied to the J2 and J3 bias ports, the magnitudes of the forward voltage across each of the PIN diodes and the resistances of R4 and R5.

These currents are nominally 25 mA each. Under this condition, the series PIN diodes connected between the J0 and J2 ports, between the J0 and J3 ports and the shunt diode between J1 and B1 are each reverse biased. The reverse bias voltage applied to non-conducting diodes must be sufficiently large to maintain each diode in its non- conducting, high impedance state when a large RF signal voltage may be present. For example, assume a large RF signal is present in the J0- to-J1 path. The reverse
bias voltage across each of the series diodes in the other paths is the arithmetic difference of the bias voltage applied to the J2 bias port or J3 bias port and the DC forward voltage of the forward-biased J0-to-J1 series PIN diode. The minimum voltage required to maintain the series diode between ports J0 and J2 and the series diode between ports J0 and J3 out of conduction is a function of the magnitude of the RF voltage present, the standing wave present at the se-ries diode's anode, the frequency of the RF signal and the characteristics of the series diode, among other factors. The minimum reverse bias voltage may be calculated as described in the "Minimum Reverse Bias Voltage" section.

Truth Table
SP3T Switch Operation with PIN Diode Driver (MPDT3T28125-701) Interface

CTRL 1	CTRL 2	CTRL 3	RF State	Path J0 - J1	Path J0 - J2	Path J0 - J2	Bias: J1	Bias: J2	Bias: J2	Bias: B1	Bias: B2	Bias: B3	Bias: J0
V_{HIGH}	V_{LOW}	V_{LOW}	1	Low Loss	High Isolation	High Isolation	0 V, -100 mA	+27 V, 0 mA	+27 V, 0 mA	+27 V, 0 mA	0 V, -25 mA	0 V, -25 mA	+5 V, +100 mA
V_{LOW}	V_{HIGH}	V_{LOW}	2	High Isolation	Low Loss	High Isolation	+27 V, 0 mA	0 V, -100 mA	+27 V, 0 mA	0 V, -25 mA	+27 V, 0 mA	0 V, -25 mA	+5 V, +100 mA
V_{LOW}	V_{LOW}	V_{HIGH}	3	High Isolation	High Isolation	Low Loss	+27 V, 0 mA	+27 V, 0 mA	0 V, -100 mA	0 V, -25 mA	0 V, -25 mA	+27 V, 0 mA	+5 V, +100 mA

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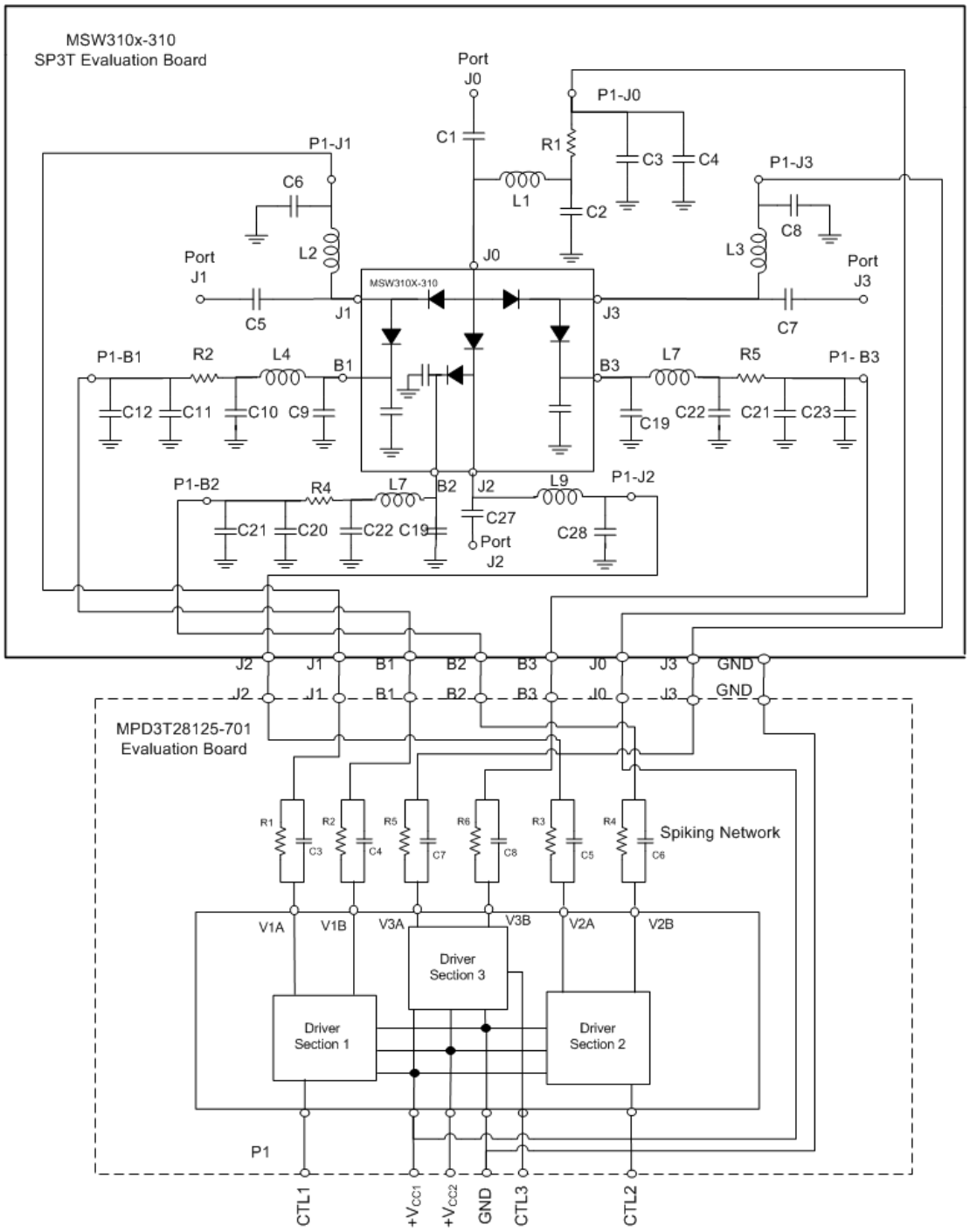
SP3T Switch Evaluation Board Description



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State 2

In State 2, the path from port J0 to J2 is in its low insertion loss condition. The path from port J0 to port J1, and the path from port J0 to port J3, are in their high isolation states. In State 2, the control voltage applied to CTL 2 is TTL-logic high, and the control voltages applied to CTL 1 and CTL 3 are TTL-logic low, which forward biases the series PIN diode between the J0 and J2 ports by applying 0 V to the J2 bias input port (P1-J2), while reverse-biasing the series diodes connected from port J0 to port J1, and from port J0 to port J3. The magnitude of the resultant bias current through the forward-biased diode is primarily determined by the voltage applied to the J0 bias port (P1-J0) (5 V nominal), the magnitude of the forward voltage across the PIN diode and the resistance of R1. This current is nominally 100 mA.

At the same time, the shunt PIN diodes connected between port J1 and B1 and between port J3 and B3 are also forward biased by applying a high bias voltage, nominally 28 V, to the J1 and J3 bias ports (P1-J1, P1-J3) and 0 V to the B1 and B3 bias ports (P1-B2, P1-B3). The magnitudes of the bias currents through these diodes are primarily determined by the voltage applied to the J1 and J3 bias ports, the magnitudes of the forward voltage across each of the PIN diodes and the resistances of R2 and R5. These currents are nominally 25 mA each. Under this condition, the series PIN diodes connected between the J0 and J1 ports, between the J0 and J3 ports and the shunt diode between J2 and B2 are each reverse biased.

The reverse bias voltage applied to non-conducting diodes must be sufficiently large to maintain each diode in its non-conducting, high impedance state when a large RF signal voltage may be present. For example, assume a large RF signal is present in the J0-to-J2 path. The reverse bias voltage across each of the series diodes in the other paths is the arithmetic difference of the bias voltage applied to the J1 bias port or J3 bias port and the DC forward voltage of the forward-biased J0-to-J2 series PIN diode.

State 3

In State 3, the path from port J0 to J3 is in its low insertion loss condition. The path from port J0 to port J1, and the path from port J0 to port J2, is in their high isolation states.

In State 3, the control voltage applied to CTL 3 is TTL-logic high, and the control voltages applied to CTL 1 and CTL 2 are TTL-logic low, which forward biases the series PIN diode between the J0 and J3 ports by applying 0 V to the J3 bias input port (P1-J3), while reverse-biasing the series diodes connected from port J0 to port J1, and from port J0 to port J2. The magnitude of the resultant bias current through the forward-biased diode is primarily determined by the voltage applied to the J0 bias port (P1-J0) (5 V nominal), the magnitude of the forward voltage across the PIN diode and the resistance of R1. This current is nominally 100 mA.

At the same time, the shunt PIN diodes connected between port J1 and B1 and between port J3 and B2 are also forward biased by applying a high bias voltage, nominally 28 V, to the J1 and J2 bias ports (P1-J1, P1-J2) and 0 V to the B1 and B2 bias ports (P1-B2, P1-B2). The magnitudes of the bias currents through these diodes are primarily determined by the voltage applied to the J1 and J2 bias ports, the magnitudes of the forward voltage across each of the PIN diodes and the resistances of R2 and R4. These currents are nominally 25 mA each. Under this condition, the series PIN diodes connected between the J0 and J1 ports, between the J0 and J2 ports and the shunt diode between J3 and B3 are each reverse biased.

The reverse bias voltage applied to non-conducting diodes must be sufficiently large to maintain each diode in its non-conducting, high impedance state when a large RF signal voltage may be present. For example, assume a large RF signal is present in the J0-to-J3 path. The reverse bias voltage across each of the series diodes in the other paths is the arithmetic difference of the bias voltage applied to the J1 bias port or J2 bias port and the DC forward voltage of the forward-biased J0-to-J3 series PIN diode.

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Calculations of Resistor Values

The magnitude of the forward bias current applied to the series diode is set by the magnitude of the supply voltage +VCC1, which is nominally 5 V, the value of resistor R1 and the forward voltage of the series diode, VDIODE, among other factors. Given the desired current value, the resistance is given by the formula:

$$R_1 = \frac{(+V_{CC1} - V_{DIODE})}{I_{BIAS}}$$

The magnitude of the current through the shunt diode is set by the magnitude of the supply voltage +VCC2, the value of resistor in series with the shunt diode (R2 or R4 or R5)and the forward voltage of the shunt diode, VDIODE, among other factors. Given the desired current value, this resistance is given by the formula:

$$R_{SHUNT} = \frac{(+V_{CC2} - 0.3 - V_{DIODE})}{I_{BIAS}}$$

It is important to note that the switch module evaluation board, as supplied from the factory, is not capable of handling RF input signals larger than 45 dBm. If performance of the switch under larger input signals is to be evaluated, an adequate heat sink must be properly attached to the evaluation board, and several of the passive components on the board must be changed in order to safely handle the dissipated power as well as the high bias voltage necessary for proper performance. Contact the factory for recommended components and heat sink.

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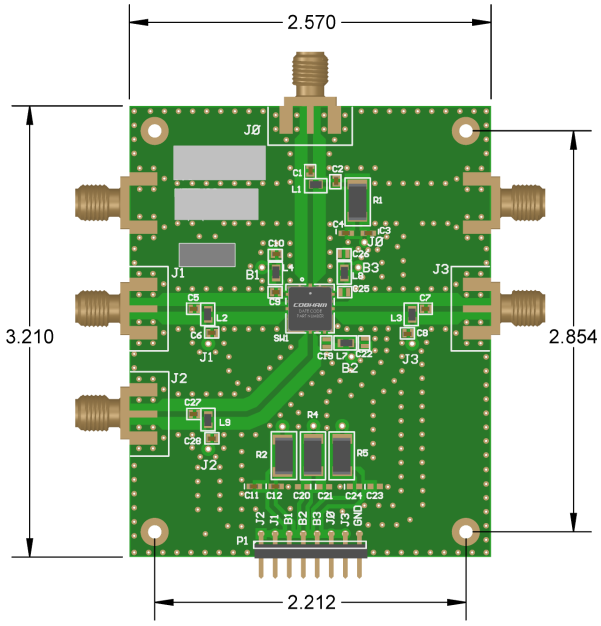
SP3T Switch Evaluation Board Layout



APPLIES TO THE FOLLOWING EVAL BOARDS:
CS310 - BAND 1 / BAND 2 / BAND 3

Evaluation Board Parts List

MSW3100-310 Band 1		
Part	**Value**	**Case Style**
C1, C2, C5 - C10, C14, C15, C16, C19, C22, C25 - C28	0.1 µF	0603
[5]C3, C4, C11, C12, C17, C18, C20, C21, C23, C24	0.1 µF	0603
L1 - L9	4.7 µH	0603
R1	39 Ω	2512
R2, R4, R5	1200 Ω	2512

MSW3101-310 Band 2		
Part	**Value**	**Case Style**
C1, C5, C7, C9, C13, C15, C19, C25, C27	22 pF	0603
C2, C6, C8, C10, C14, C16, C22, C26, C28	270 pF	0603
C3, C4, C11, C12, C17, C18, C20, C21, C23, C24	1000 pF	0603
L1 - L9	82 nH	0603
R1	39 Ω	2512
R2, R4, R5	1200 Ω	2512

5. Second bypass capacitor is optional.

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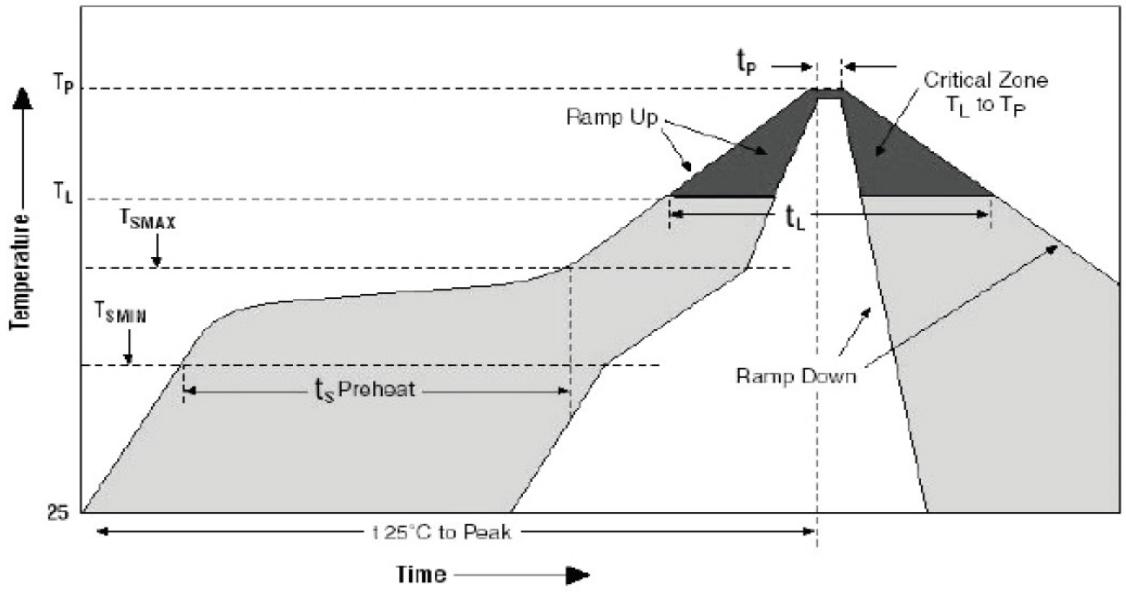
Assembly Instructions

SP3T PIN Diodes may be placed onto circuit boards with pick and place manufacturing equipment from tape and reel. The devices are attached to the circuit using conventional solder re-flow or wave soldering procedures with RoHS type or Sn 60 / Pb 40 type solders.

Table 1. Time-Temperature Profile for Sn60/Pb40 or RoHS Type Solders

Profile Feature	SnPb Solder Assembly	Pb-Free Solder Assembly
Average Ramp-Up Rate (T_L to T_P)	3°C /second maximum	3°C /second maximum
Preheat: - Temperature Min (T_{SMIN}) - Temperature Max (T_{SMAX}) - Time (min to max)(t_S)	 100°C 150°C 60-120 s	 150°C 200°C 60-180 s
T_{SMAX} to T_L - Ramp-Up Rate		3°C/s maximum
Time Maintained Above: - Temperature (T_L) - Time (t_L)	 183°C 60-150 s	 217°C 60-150 s
Peak temperature (T_P)	225 +0/-5°C	260 +0/-5°C
Time Within 5°C of Actual Peak Temperature (t_P)	10 – 30 s	20 – 40 s
Ramp-Down Rate	6°C /s maximum	6°C /s maximum
Time 25°C to Peak Temperature	6 minutes maximum	8 minutes maximum

Figure 1. Solder Re-Flow Time-Temperature Profile



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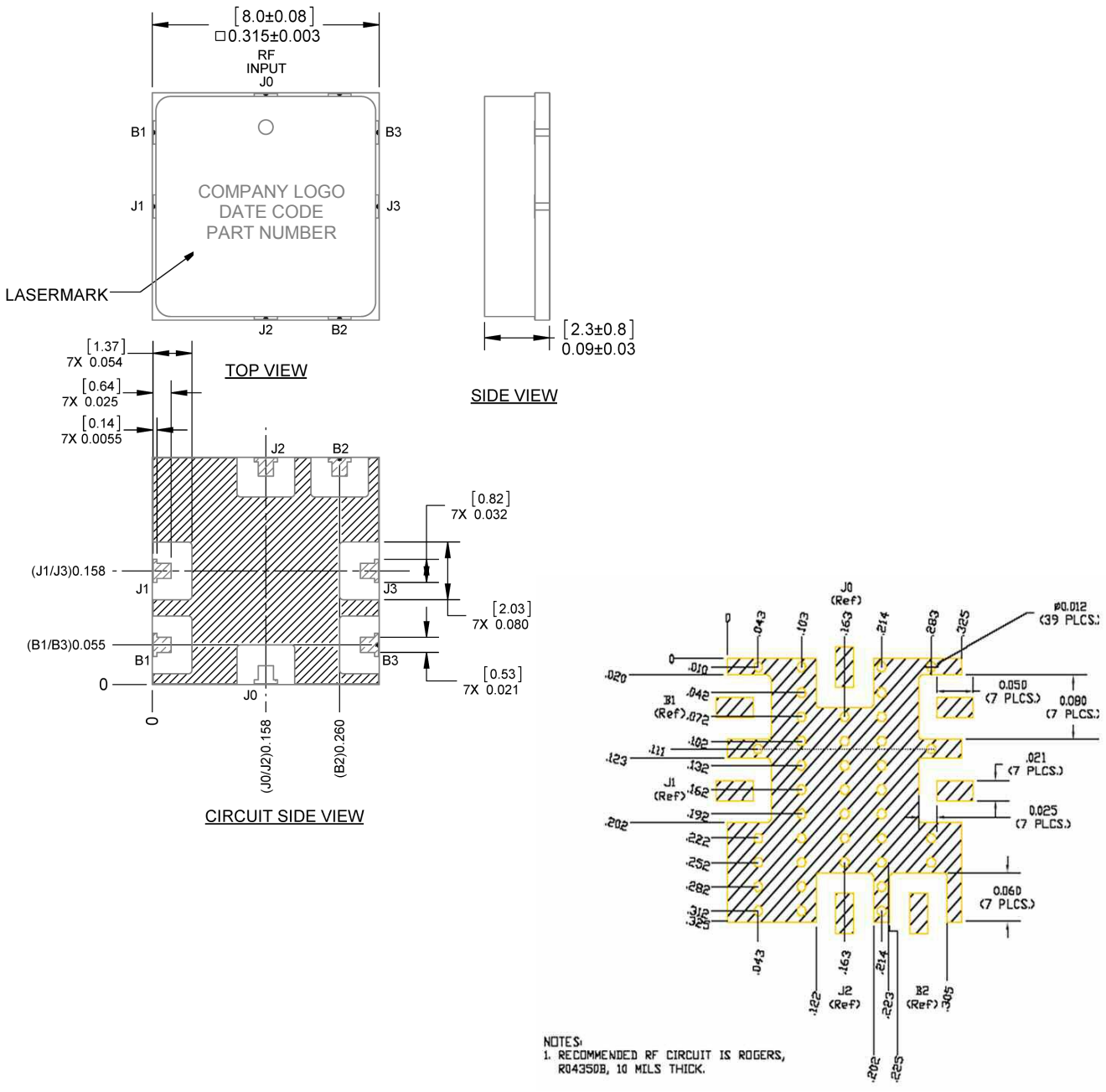
Outline (CS310)[6,7]



6. Hatched metal area on circuit side of device is RF, DC and thermal grounded.
7. Vias should be solid copper fill and gold plated for optimum heat transfer from backside of switch module through Circuit Vias to metal thermal ground.

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