

Features

- Wide Frequency Range: 50 MHz to 6 GHz, in 3 bands
- Surface Mount SP2T Switch in Compact Outline: 8 mm L x 5 mm W x 2.5 mm H
- Higher Average Power Handling than Plastic Packaged
- MMIC Switches: 100 W CW
- High RF Peak Power: 500 W
- Low Insertion Loss: 0.25 dB
- High IIP3: 65 dBm
- Operates From Positive Voltage Only: 5 V & 28 V to 125 V
- RoHS* Compliant

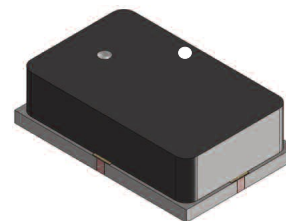
Applications

- High Power Transmit / Receive Switching
- Active Receiver Protection

Description

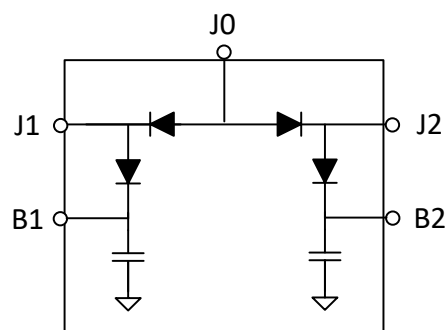
The MSW203x-203 series of surface mount silicon PIN diode SP2T switches handle high power signals from 50 MHz to 1 GHz (MSW2030), 400 MHz to 4 GHz (MSW2031) and 2 to 6 GHz (MSW2032), in transmit-receive (TR), active receiver protection and other applications. This series is manufactured using a proven hybrid manufacturing process incorporating high voltage PIN diodes and passive devices integrated within a ceramic substrate. These low profile, compact, surface mount components, offer superior small and large signal performance superior to that of MMIC devices in QFN packages. The SP2T switches are designed in an asymmetrical topology to minimize Tx-Ant loss and maximize Tx-Rx isolation performance. The very low thermal resistance (<25°C/W) of the PIN diodes in these devices enables them to reliably handle RF incident power levels of 50 dBm CW and RF peak incident power levels of 57 dBm in cold switching applications at $T_A = 85^\circ\text{C}$. The thick I-layers of the PIN diodes (>100 μm), coupled with their long minority carrier lifetime, (>2 μs), provides input third order intercept point (IIP3) greater than 65 dBm.

These MSW203x-203 series SP2T switches are designed to be used in high average and peak power switch applications, operating from 50 MHz to 6 GHz in three bands, which utilize high volume, surface mount, solder re-flow manufacturing. These products are durable and capable of reliably operating in military, commercial, and industrial environments.



CS203

Functional Schematic



Ordering Information

Part Number	Package
MSW2030-203-T	tube
MSW2030-203-R	250 or 500 piece reel
MSW2030-203-W	Waffle pack
MSW2031-203-T	tube
MSW2031-203-R	250 or 500 piece reel
MSW2031-203-W	Waffle pack
MSW2032-203-T	tube
MSW2032-203-R	250 or 500 piece reel
MSW2032-203-W	Waffle pack
MSW2030-203-E	RF evaluation board
MSW2031-203-E	RF evaluation board
MSW2032-203-E	RF evaluation board

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

MSW2030-203 Electrical Specifications: $T_A = +25^\circ\text{C}$, $P_{IN} = 0\text{ dBm}$, $Z_0 = 50\ \Omega$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Frequency	—	MHz	50	—	1000
Insertion Loss	bias state 1: port J0 to J1 bias state 2: port J0 to J2	dB	—	0.3	0.4
Return Loss	bias state 1: port J0 to J1 bias state 2: port J0 to J2	dB	20	22	—
Isolation	bias state 1: port J0 to J1 bias state 2: port J0 to J2	dB	50	52	—
CW Incident Power ¹	source & load VSWR = 1.5:1	dBm	—	50	51
Peak Incident Power ¹	source & load VSWR = 1.5:1 pulse width = 10 μs , duty cycle = 1%	dBm	—	57	—
Switching Time ²	10% - 90% RF Voltage, TTL rep rate = 100	μs	—	2	3
Input IP3	F1 = 500 MHz, F2 = 510 MHz, P1=P2=10 dBm measured on path biased to low loss state	dBm	60	65	—

MSW2031-203 Electrical Specifications: $T_A = +25^\circ\text{C}$, $P_{IN} = 0\text{ dBm}$, $Z_0 = 50\ \Omega$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Frequency	—	MHz	400	—	4000
Insertion Loss	bias state 1: port J0 to J1 bias state 2: port J0 to J2	dB	—	0.5	0.6
Return Loss	bias state 1: port J0 to J1 bias state 2: port J0 to J2	dB	14	16	—
Isolation	bias state 1: port J0 to J1 bias state 2: port J0 to J2	dB	32	35	—
CW Incident Power ¹	source & load VSWR = 1.5:1	dBm	—	50	51
Peak Incident Power ¹	source & load VSWR = 1.5:1 pulse width = 10 μs , duty cycle = 1%	dBm	—	57	—
Switching Time ²	10% - 90% RF Voltage, TTL rep rate = 100	μs	—	1	2
Input IP3	F1 = 1000 MHz, F2 = 1010 MHz, P1=P2=10 dBm measured on path biased to low loss state	dBm	60	65	—

Continued

MSW2032-203 Electrical Specifications: $T_A = +25^\circ\text{C}$, $P_{IN} = 0 \text{ dBm}$, $Z_0 = 50 \Omega$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Frequency	—	GHz	2	—	6
Insertion Loss	bias state 1: port J0 to J1 bias state 2: port J0 to J2	dB	—	0.6	0.8
Return Loss	bias state 1: port J0 to J1 bias state 2: port J0 to J2	dB	11	13	—
Isolation	bias state 1: port J0 to J1 bias state 2: port J0 to J2	dB	32	35	—
CW Incident Power ¹	source & load VSWR = 1.5:1	dBm	—	50	51
Peak Incident Power ¹	source & load VSWR = 1.5:1 pulse width = 10 μs , duty cycle = 1%	dBm	—	57	—
Switching Time ²	10% - 90% RF Voltage, TTL rep rate = 100	μs	—	1	2
Input IP3	F1 = 2000 MHz, F2 = 2010 MHz, P1=P2=10 dBm measured on path biased to low loss state	dBm	60	65	—

Bias State Conditions:
State 1:

(J0 - J1 in low insertion loss state,
J0 - J2 in isolation state)

- a. B1: V_{HIGH} (note 2), 0 mA
- b. B2: -25 mA, 0 V
- c. J1: -100 mA, 0 V
- d. J2: 25 mA, V_{HIGH} (note 2)
- e. J0: 100 mA, $\approx 0.9 \text{ V}$

State 2:

(J0 - J2 in low insertion loss state,
J0 - J1 in isolation state)

- a. B1: -25 mA, 0 V
- b. B2: V_{HIGH} (note 2), 0 mA
- c. J1: 25 mA, V_{HIGH} (note 2)
- d. J2: -100 mA, 0 V
- e. J0: 100 mA, $\approx 0.9 \text{ V}$

- Switching time (50% TTL - 10/90% RF Voltage) is a function of the PIN diode driver performance as well as the characteristics of the diode. An RC "current spiking network" is used on the driver output to provide a transient current to rapidly remove stored charge from the PIN diode. Typical component values are: $R = 50$ to 220Ω and $C = 470$ to $1,000 \text{ pF}$.
- PIN diode DC reverse voltage to maintain high resistance in the OFF PIN diode is determined by RF frequency, incident power, and VSWR as well as by the characteristics of the diode. The minimum reverse bias voltage values are provided in this datasheet.

Truth Table^{3,4} : +V_{CC1} = 5 V and +V_{CC2} = 28 V (unless otherwise noted)

J0 - J1	J0 - J2	Bias: J1	Bias: J2	B1	B2
Low Loss	Isolation	0 V, -100 mA	V _{HIGH} , 25 mA	V _{HIGH} , 0 mA	0 V, -25 mA
Isolation	Low Loss	V _{HIGH} , 25 mA	0 V, -100 mA	0 V, -25 mA	V _{HIGH} , 0 mA

3. $28\text{ V} \leq V_{\text{HIGH}} \leq 125\text{ V}$.

4. PIN diode minimum reverse DC voltage (V_{HIGH}) to maintain high resistance in the OFF PIN diode is determined by RF frequency, incident power, duty cycle, characteristic impedance and VSWR as well as by the characteristics of the diode. The recommended minimum reverse bias voltage (V_{HIGH}) values are provided in the Minimum Reverse Bias Voltage table.

RF Bias Network Component Values

Part #	Frequency (MHz)	Inductors	DC Blocking Capacitors	RF Bypass Capacitors	Secondary Bypass Capacitors
MSW2030-203	50 - 1000	Ferrite Bead, 600 Ω , 1A	470 pF	470 pF	470 pF
MSW2031-203	400 - 4000	43 nH	47 pF	220 pF	1000 pF
MSW2032-203	2000 - 6000	33 nH	22 pF	33 pF	1000 pF

Minimum Reverse Bias Voltage⁵: P_{INC} = 125 W CW, Z₀ = 50 Ω with 1.5:1 VSWR

Part #	20 MHz	100 MHz	200 MHz	400 MHz	1 GHz	4 GHz
MSW2030-203	120 V	110 V	85 V	55 V	28 V	N/A
MSW2031-203	N/A	N/A	110 V	85 V	55 V	28 V
MSW2032-203	(F = 1 GHz) 55 V	(F = 2 GHz) 28 V	(F = 3 GHz) 28 V	(F = 4 GHz) 28 V	(F = 5 GHz) 28 V	(F = 6 GHz) 28 V

5. N/A denotes the switch is not recommended for that frequency band.

The minimum reverse bias voltage required to maintain a PIN diode out of conduction in the presence of a large RF signal is given by:

$$|V_{DC}| = \frac{|V_{RF}|}{\sqrt{1 + \left[\left(\frac{0.0142 \times f_{\text{MHz}} \times W_{\text{mils}}^2}{V_{RF} \times \sqrt{D}} \right) \times \left(1 + \sqrt{1 + \left(\frac{0.056 \times V_{RF} \times \sqrt{D}}{W_{\text{mils}}} \right)^2} \right)^2 \right]}}$$

Where:

- |V_{DC}| = magnitude of the minimum DC reverse bias voltage
- |V_{RF}| = magnitude of the peak RF voltage (including the effects of the VSWR)
- F_{MHz} = lowest RF signal frequency expressed in MHz
- D = duty factor of the RF signal
- W_{MILS} = thickness of the diode I layer, expressed in mils (thousands of an inch)

R. Caverly and G. Hiller, —Establishing the Minimum Reverse Bias for a PIN Diode in a High Power Switch, IEEE Transactions on Microwave Theory and Techniques, Vol.38, No.12, December 1990

Absolute Maximum Ratings

Parameter	Conditions	Absolute Maximum
Forward Current	J0, J1, J2 Port B1, B2 Port	250 mA 150 mA
Reverse Voltage	J0, J1, J2, B1, B2 Port	200 V
Forward Diode Voltage	$I_F = 250$ mA	1.2 V
CW Incident Power Handling ⁶	Source & Load VSWR = 1.5:1, $T_C = 85^\circ\text{C}$, cold switching	50 dBm
Peak Incident Power Handling ⁶	Source & Load VSWR = 1.5:1, $T_C = 85^\circ\text{C}$, cold switching, Pulse Width = 10 μs , Duty Cycle = 1%	57 dBm
Total Dissipated RF & DC Power ⁶	$T_C = 85^\circ\text{C}$, cold switching	8 W
Junction Temperature	—	+175°C
Operating Temperature	—	-65°C to +125°C
Storage Temperature	—	-65°C to +150°C
Assembly Temperature	$t = 10$ s	+260°C

6. Backside RF and DC grounding area of device must be completely solder attached to the RF circuit board vias for proper electrical and thermal circuit grounding.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

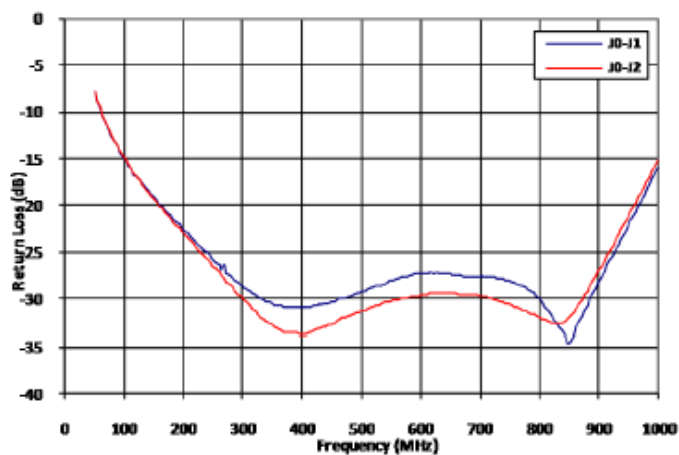
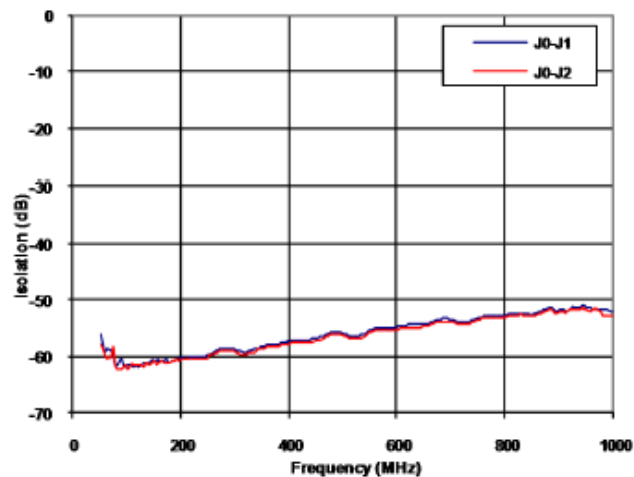
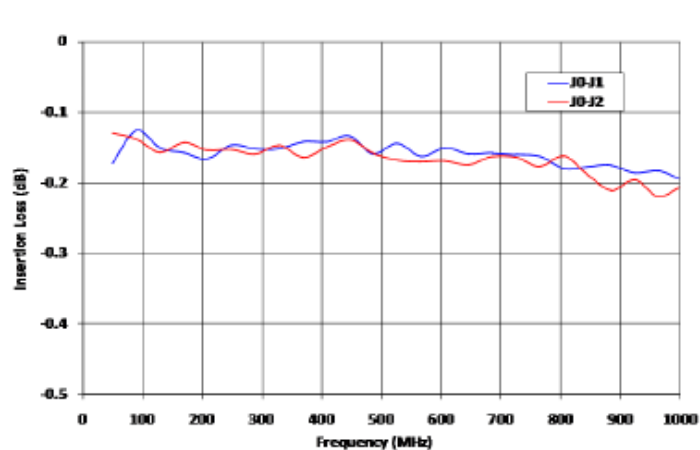
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 0 (HBM) devices. The moisture sensitivity level (MSL) rating for this part is 1.

Environmental Capabilities

The MSW203x-203 diode is capable of meeting the environmental requirements of MIL-STD-202 and MIL-STD-750.

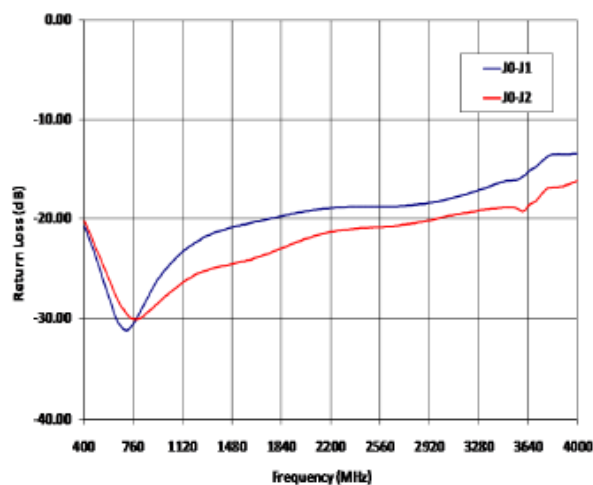
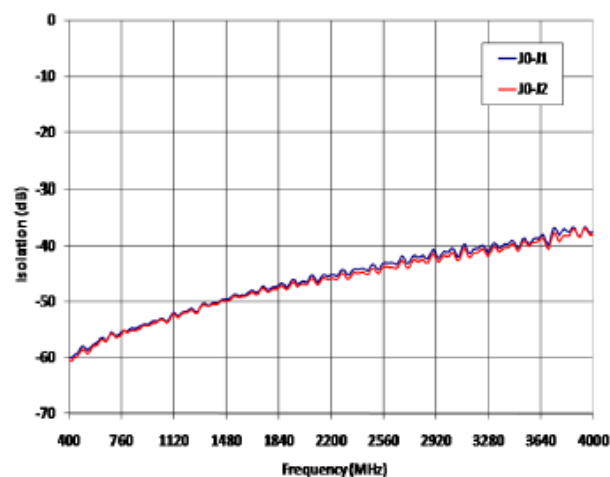
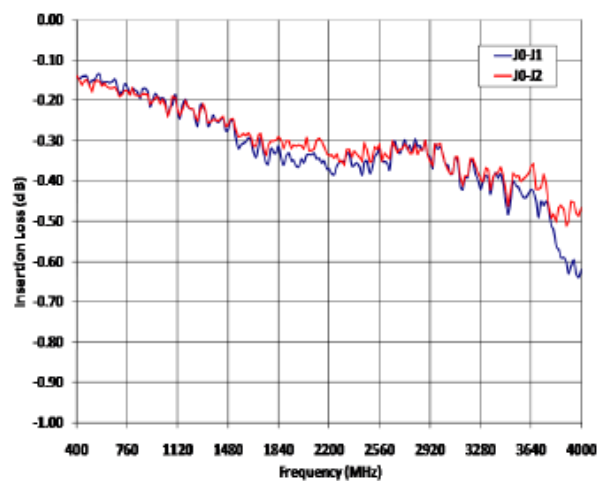
MSW2030-203 Small Signal Typical Performance

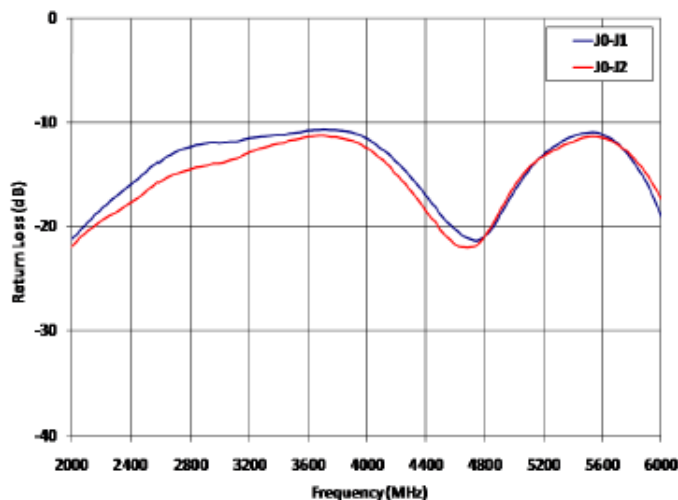
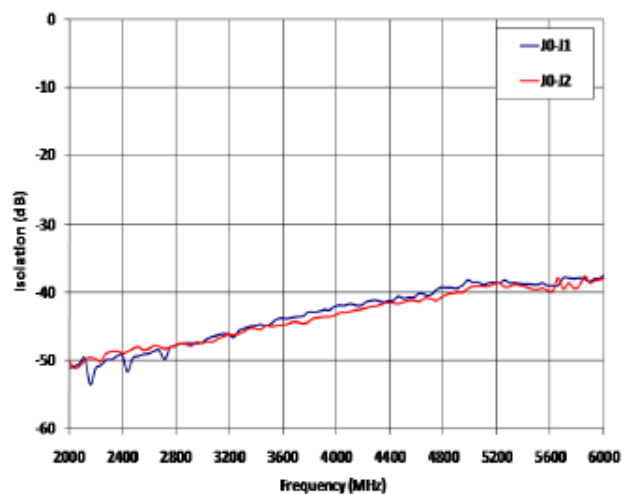
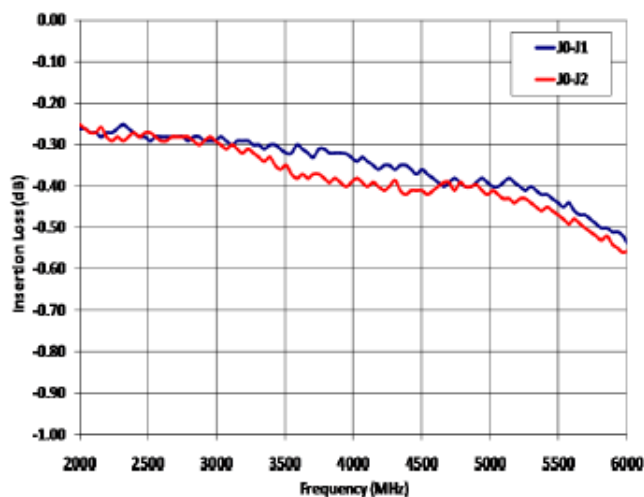
$Z_0 = 50 \Omega$, $T_A = +25^\circ\text{C}$ (Unless Otherwise Defined)



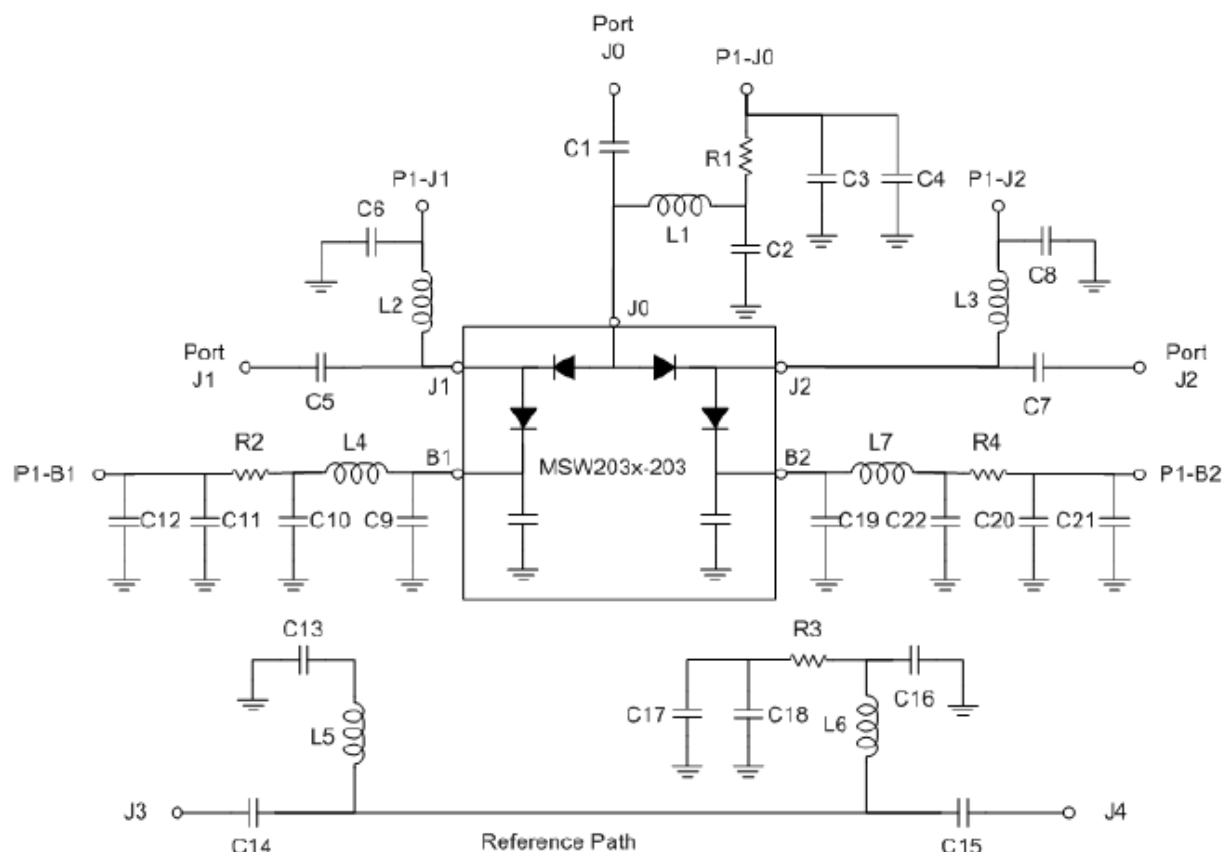
MSW2031-203 Small Signal Typical Performance

$Z_0 = 50 \Omega$, $T_A = +25^\circ\text{C}$ (Unless Otherwise Defined)



MSW2032-203 Small Signal Typical Performance $Z_0 = 50 \Omega$, $T_A = +25^\circ\text{C}$ (Unless Otherwise Defined)

SP2T Switch Evaluation Board Schematic



The evaluation boards for the MSW203x-203 family of surface mount silicon PIN diode SP2T T-R switches allow the full exercise of each switch for small signal performance analysis, as well as for large signal operation with maximum input signal power of 45 dBm (CW or peak power). Each evaluation board includes the appropriate MSW203x-203 switch, DC blocking capacitors at each RF port and bias decoupling networks at each RF port which allow DC or low frequency control signals to be applied to the switch.

Four complementary control signals are required for proper operation. Bias voltages are applied to the B1 and B2 bias ports, as well as to the J0, J1, and J2 RF ports to control the state of the switch. A fixed bias voltage must be applied to the J0 port (connect 5 V to pin 3 of multi-pin connector P1) whenever the switch is in operation.

Caution: the evaluation board, as supplied from the factory, is not capable of handling RF input signals larger than 45 dBm. If performance of the switch under larger input signals is to be evaluated, several of the passive components on the board must be changed in order to safely handle the dissipated power as well as the high bias voltage necessary for proper performance. The evaluation board must be connected to an adequate heat sink for large signal operation. Contact the factory for recommended components.

For the purposes of description, State 1 is defined to be the condition in which the evaluation board is biased to produce the low insertion condition between ports J0 and J1 while producing high isolation between ports J0 and J2. State 2 is the converse of State 1.

State 1

In State 1, the series PIN diode between J0 and J1 ports is forward biased by applying 0 V to the J1 bias input port (pin 1 of multi-pin connector P1). The magnitude of the resultant bias current through the diode is primarily determined by the voltage applied to the J0 bias port (pin 3 of P1), the magnitude of the forward voltage across the PIN diode and the resistance of R1. This current is nominally 100 mA. At the same time, the PIN diode connected between J2 and B2 ports is also forward biased by applying a higher bias voltage, nominally 28 V, to the J2 bias port (pin 7 of P1) and 0 V to the B2 bias port (pin 5 of P1). Under this condition, the PIN diode connected between the J0 and J2 port is reverse biased and the PIN diode connected between the J2 and B2 ports is forward biased. The magnitude of the bias current through this diode is primarily determined by the voltage applied to the J2 bias port, the magnitude of the forward voltage across the PIN diode and the resistance of R4. This current is nominally 25 mA.

The series PIN diode, which is connected between the J0 and J2 ports, must be reverse biased during the state 1. The reverse bias voltage must be sufficiently large to maintain the diode in its non-conducting, high impedance state when large RF signal voltage may be present in the J0-to-J1 path. The reverse voltage across this diode is the arithmetic difference of the bias voltage applied to the J0 bias port and the DC forward voltage of the forward-biased J0-to-J1 series PIN diode.

The minimum voltage required to maintain the series diode between J0 and J2 out of conduction is a function of the magnitude of the RF voltage present, the standing wave present at the series diode's anode, the frequency of the RF signal and the characteristics of the series diode, among other factors. Minimum control voltages for several signal frequencies are shown in the table "Minimum Reverse Bias Voltage", assuming the input power to the J0 or J1 port to be 100 W CW and the VSWR on the J0-J1 path to be 1.5:1.

State 2

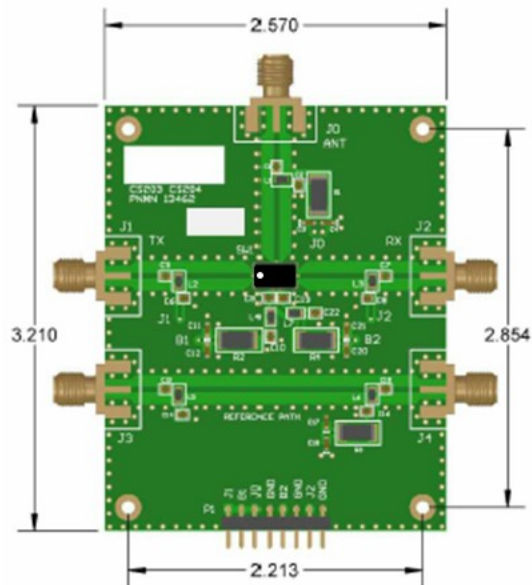
In State 2, the series PIN diode between the J0 and J2 ports is forward biased by applying 0 V to the J2 bias input port (pin 7 of multi-pin connector P1). The magnitude of the resultant bias current through the diode is primarily determined by the voltage applied to the J0 bias port (pin 3 of P1), the magnitude of the forward voltage across the PIN diode and the resistance of R1. This current is nominally 100 mA. At the same time, the PIN diode connected between J2 and B2 ports is reverse biased by applying a high bias voltage, nominally 28 V, to the B2 bias port (pin 5 of P1). A high voltage, nominally 28 V, is also applied to the J1 bias port (pin 1 of P1). Under this condition, the PIN diode connected between the J0 and J1 port is reverse biased thus isolating the J1 RF port from the RX signal path between J0 and J2. The reverse voltage across this diode is the arithmetic difference of the bias voltage applied to the J1 bias port and the DC forward voltage of the forward-biased J0-to-J2 series PIN diode. The minimum voltage required to maintain the series diode on the J0-to-J1 side of the switch out of conduction is a function of the magnitude of the RF voltage present, the standing wave present at the diode's anode, the frequency of the RF signal and the characteristics of the TX series diode, among other factors.

The values of the reactive components which comprise the bias decoupling networks as well as the signal path DC blocking are shown in the table RF Bias Network Component Values.

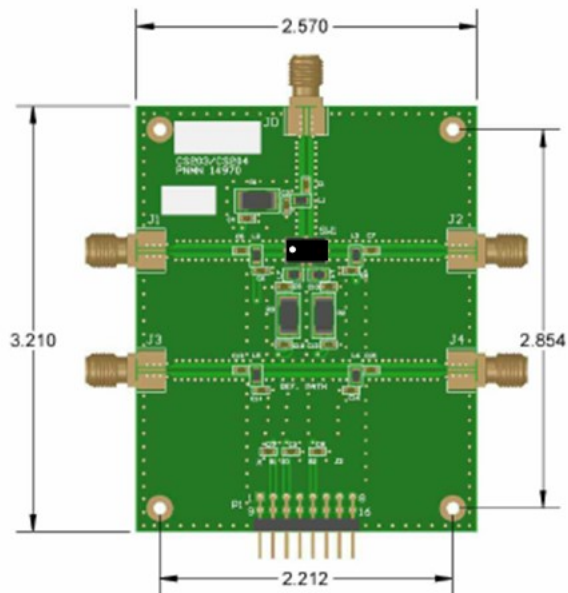
Reference Path

A reference path is provided on the evaluation board, complete with bias decoupling networks, so that the magnitude of the insertion loss of the microstrip transmission lines connected to the switch and the associated bias decoupling components can be measured and removed from the measured performance of the switch.

SP2T Switch Evaluation Board Layouts



APPLIES TO THE FOLLOWING EVAL. BOARDS:
CS203/CS204 - BAND 1/ BAND 2



APPLIES TO THE FOLLOWING EVAL BOARDS:
CS203/CS204 - BAND 3

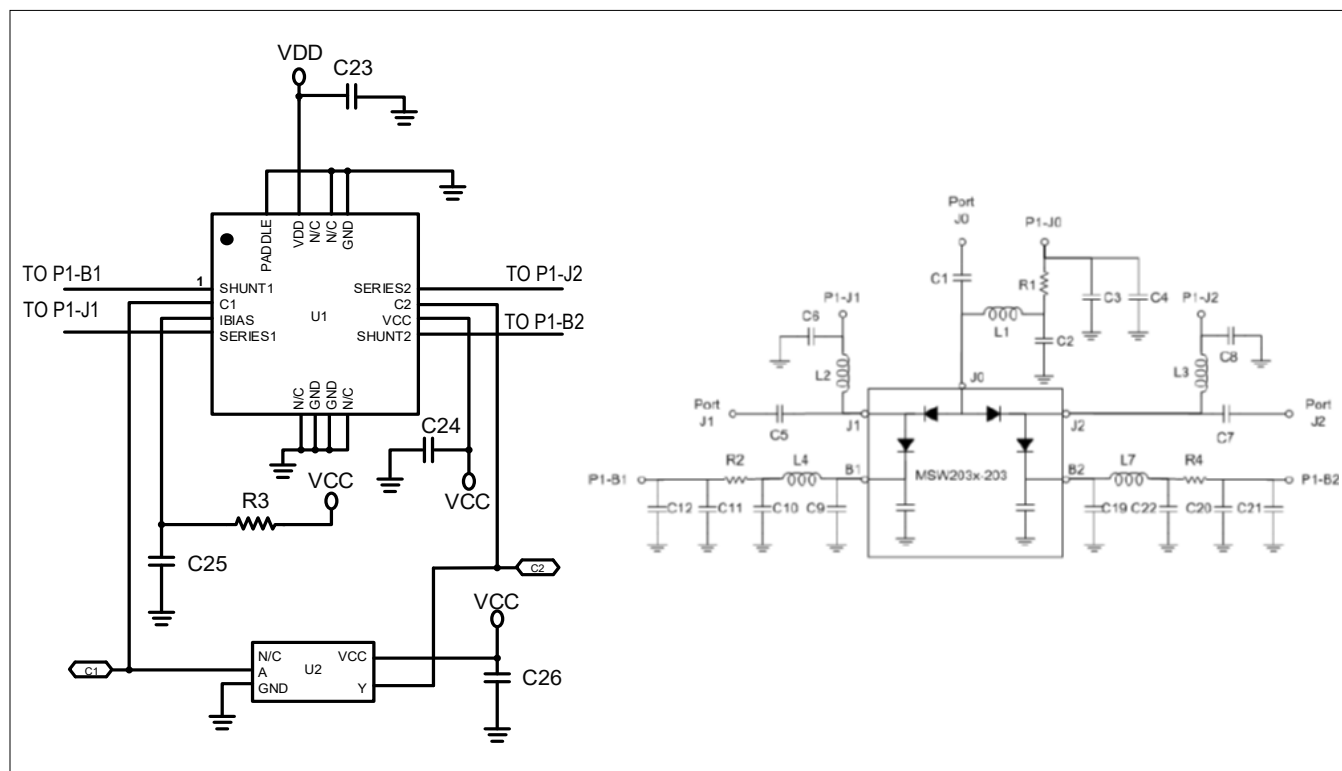
Evaluation Board Parts List

MSW2030-203 Band 1		
Part	Value	Case Style
C1, C5, C7, C13, C15	470 pF	0603
C2, C6, C8, C9, C10, C14, C16, C19	470 pF	0603
C3, C4, C11, C12, C17, C18, C20, C21	470 pF	0603
L1 - L7	600 Ω	0603
R1, R3	39 Ω	2512
R2	1200 Ω	2512

MSW2031-203 Band 2		
Part	Value	Case Style
C1, C5, C7, C13, C15	47 pF	0603
C2, C6, C8, C9, C10, C14, C16, C19, C22	220 pF	0603
C3, C4, C11, C12, C17, C18, C20, C21	1000 pF	0603
L1 - L7	43 nH	0603
R1, R3	39 Ω	2512
R2, R4	1200 Ω	2512

MSW2032-203 Band 3		
Part	Value	Case Style
C1, C5, C7, C13, C15	22 pF	0603
C2, C6, C8, C9, C10, C14, C16	33 pF	0603
C3, C4, C10, C11, C12, C17, C18	1000 pF	0603
L1 - L7	33 nH	0805
R1	39 Ω	2512
R2, R3	1200 Ω	2512

7. Second bypass capacitor is optional.

MSW203x-203 with MADR-010574 Driver Application Schematic⁸

8. See page 11 for R1, L1 - L7 and C1 - C22 values. P1-J0 set to V_{CC}.

Parts List

Part	Value
C23	0.01 μ F
C24 - C26	0.1 μ F
R2, R4 ⁹	12 K Ω
R3	499 K Ω
U2	SN74AHC1G

9. Resistor value calculated to provide ~10 mA of shunt diode bias current given V_{CC} = 5 V and V_{DD} = 120 V.

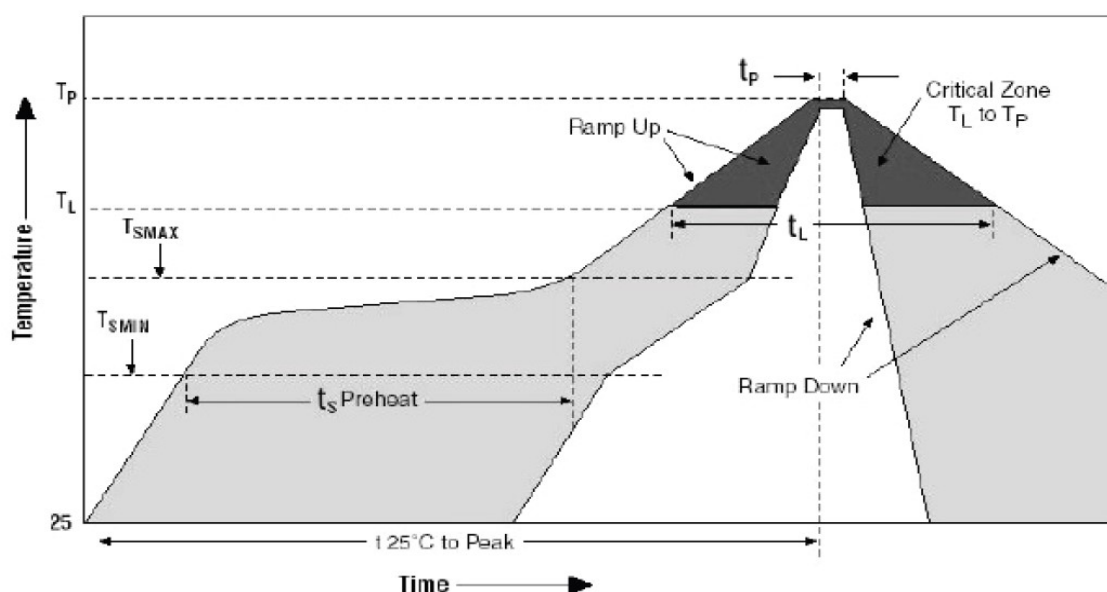
Assembly Instructions

SP2T PIN Diodes may be placed onto circuit boards with pick and place manufacturing equipment from tape and reel. The devices are attached to the circuit using conventional solder re-flow or wave soldering procedures with RoHS type or Sn 60 / Pb 40 type solders.

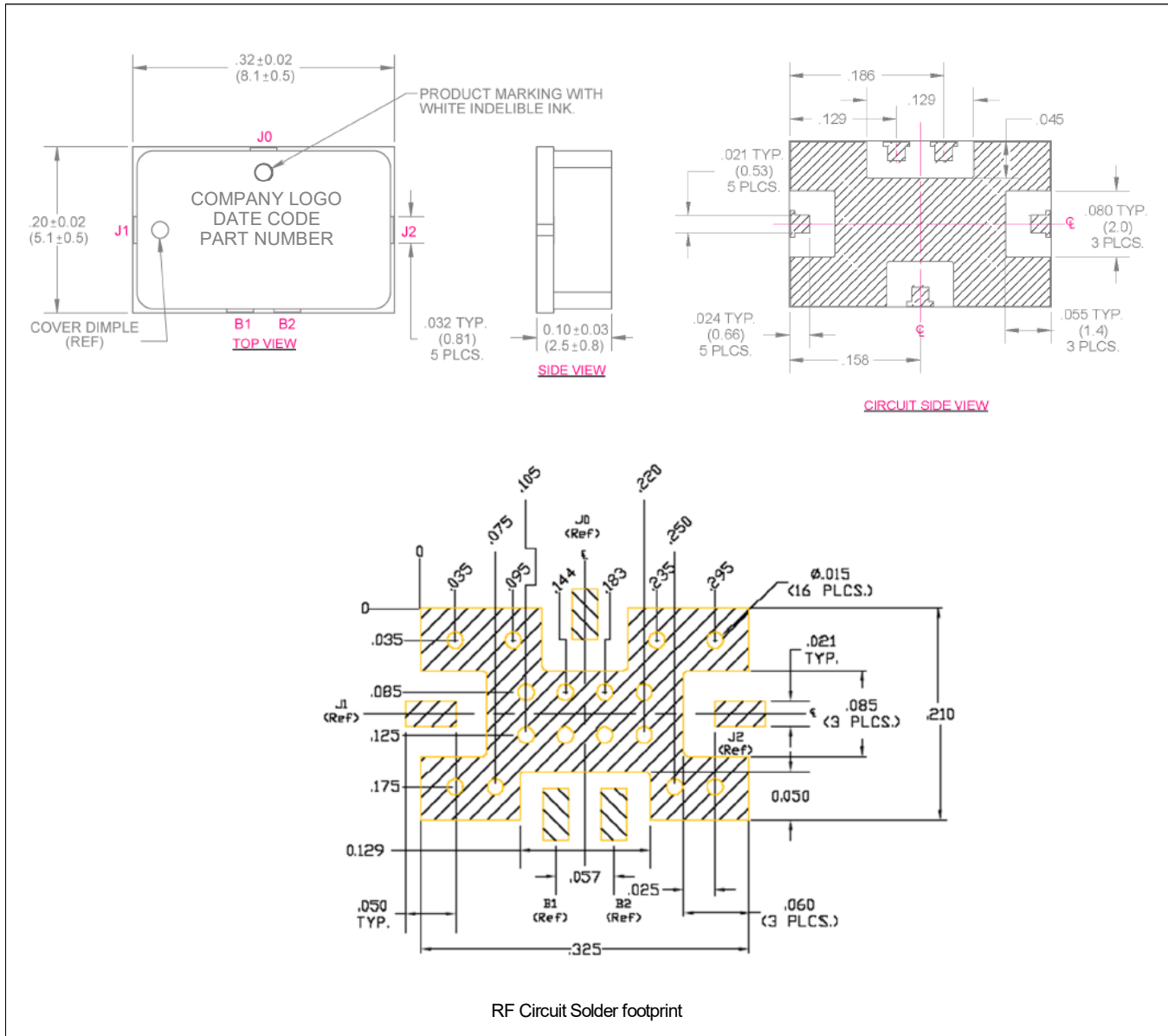
Table 1. Time-Temperature Profile for Sn60/Pb40 or RoHS Type Solders

Profile Feature	SnPb Solder Assembly	Pb-Free Solder Assembly
Average Ramp-Up Rate (T_L to T_P)	3°C /second maximum	3°C /second maximum
Preheat: <ul style="list-style-type: none"> - Temperature Min (T_{SMIN}) - Temperature Max (T_{SMAX}) - Time (min to max)(t_s) 	100°C 150°C 60-120 s	150°C 200°C 60-180 s
T_{SMAX} to T_L <ul style="list-style-type: none"> - Ramp-Up Rate 		3°C/s maximum
Time Maintained Above: <ul style="list-style-type: none"> - Temperature (T_L) - Time (t_L) 	183°C 60-150 s	217°C 60-150 s
Peak temperature (T_P)	225 +0/-5°C	260 +0/-5°C
Time Within 5°C of Actual Peak Temperature (t_p)	10 – 30 s	20 – 40 s
Ramp-Down Rate	6°C /s maximum	6°C /s maximum
Time 25°C to Peak Temperature	6 minutes maximum	8 minutes maximum

Figure 1. Solder Re-Flow Time-Temperature Profile



Outline (CS203)^{10,11}



10. Hatched metal area on circuit side of device is RF, DC and thermal grounded.
11. Vias should be solid copper fill and gold plated for optimum heat transfer from backside of switch module through circuit vias to metal thermal ground.

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