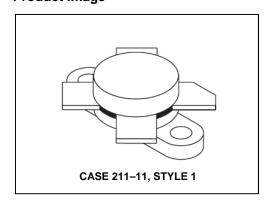


The RF Line NPN Silicon Power Transistor 100W(PEP), 30MHz, 28V

M/A-COM Products Released - Rev. 07.07

Designed primarily for application as a high-power linear amplifier from 2.0 Product Image to 30 MHz.

- Specified 12.5 V, 30 MHz characteristics Output power = 100 W (PEP) Minimum gain = 10 dB Efficiency = 40%
- Intermodulation distortion @ 100 W (PEP) IMD = -30 dB (min.)
- 100% tested for load mismatch at all phase angles with 30:1 VSWR



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V _{CEO}	20	Vdc
Collector-Base Voltage	V _{CBO}	45	Vdc
Emitter-Base Voltage	V _{EBO}	3.0	Vdc
Collector Current — Continuous	Ic	20	Adc
Withstand Current — 10 s	_	30	Adc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	290 1.66	Watts W/°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{0JC}	0.6	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I _C = 50 mAdc, I _B = 0)	V _{(BR)CEO}	20	_	_	Vdc
Collector-Emitter Breakdown Voltage (I _C = 200 mAdc, V _{BE} = 0)	V _{(BR)CES}	45	_	_	Vdc
Collector-Base Breakdown Voltage (I _C = 200 mAdc, I _E = 0)	V _{(BR)CBO}	45	_	_	Vdc
Emitter–Base Breakdown Voltage (I _E = 10 mAdc, I _C = 0)	V _{(BR)EBO}	3.0	_	_	Vdc
Collector Cutoff Current (V _{CE} = 16 Vdc, V _{BE} = 0, T _C = 25°C)	I _{CES}	_	_	10	mAdc

(continued)

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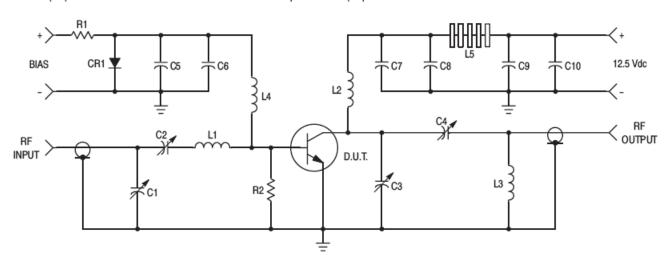
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ELECTRICAL CHARACTERISTICS - continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Тур	Max	Unit
ON CHARACTERISTICS		•			
DC Current Gain (I _C = 5.0 Adc, V _{CE} = 5.0 Vdc)	h _{FE}	10	70	_	_
DYNAMIC CHARACTERISTICS					
Output Capacitance (V _{CB} = 12.5 Vdc, I _E = 0, f = 1.0 MHz)	C _{ob}	_	550	800	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V _{CC} = 12.5 Vdc, P _{out} = 100 W, I _{C(max)} = 10 Adc, I _{CQ} = 150 mAdc, f = 30, 30.001 MHz)	GPE	10	12	_	dB
Collector Efficiency (V _{CC} = 12.5 Vdc, P _{out} = 100 W, I _{C(max)} = 10 Adc, I _{CQ} = 150 mA, f = 30, 30.001 MHz)	η	40	_	_	%
Intermodulation Distortion (1) (V _{CE} = 12.5 Vdc, P _{out} = 100 W, I _C = 10 Adc, I _{CQ} = 150 mA, f = 30, 30.001 MHz)	IMD	_	-33	-30	dB

1. To proposed EIA method of measurement. Reference peak envelope power.



C1, C2, C4 - 170-780 pF, ARCO 469

C3 - 80-480 pF, ARCO 466

C5, C7, C10 - ERIE 0.1 µF, 100 V

C6 - MALLORY 500 µF @ 15 V Electrolytic

C9 - 100 µF, 15 V Electrolytic

C8 - 1000 pF, 350 V UNDERWOOD

R1 - 10 Ω, 25 Watt Wirewound

R2 - 10 Ω, 1.0 Watt Carbon

CR1 - 1N4997

L1 - 3 Turns, #16 Wire, 5/16" I.D., 5/16" Long

L2 - 12 Turns, #16 Enameled Wire Closewound, 1/4" I.D.

L3 - 1-3/4 Turns, 1/8" Tubing, 3/8" I.D., 3/8" Long

L4 - 10 μH Molded Choke

L5 - 10 Ferrite Beads - FERROXCUBE #56-590-65/3B

Figure 1. 30 MHz Test Circuit Schematic

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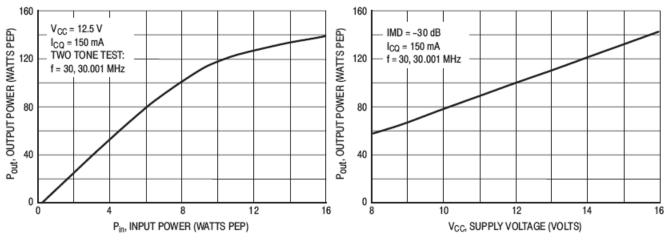


Figure 2. Output Power versus Input Power

Figure 3. Output Power versus Supply Voltage

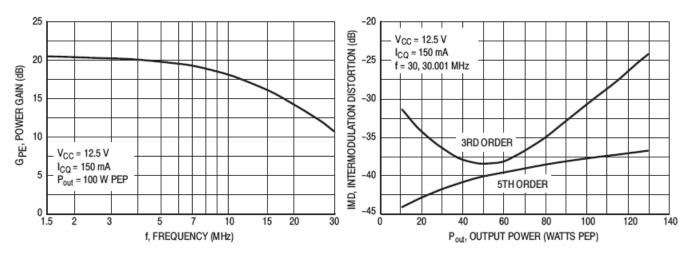


Figure 4. Power Gain versus Frequency

Figure 5. Intermodulation Distortion versus Output Power

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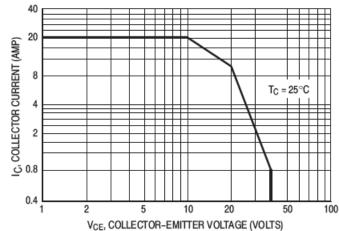


Figure 6. DC Safe Operating Area

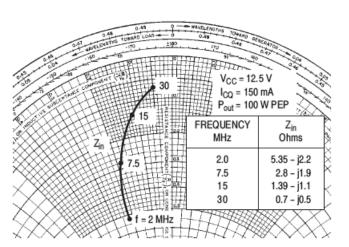


Figure 7. Series Equivalent Impedance

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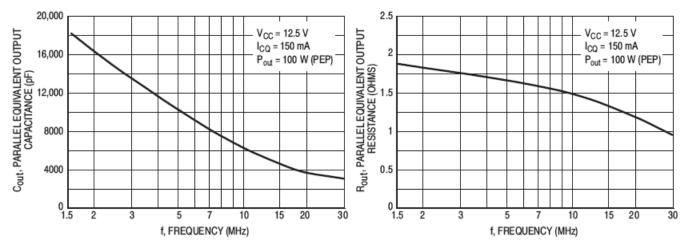
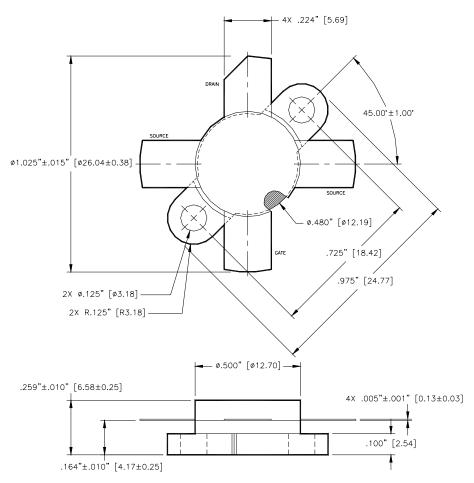


Figure 8. Output Capacitance versus Frequency

Figure 9. Output Resistance versus Frequency



Unless otherwise noted, tolerances are inches $\pm .005$ " [millimeters ± 0.13 mm]

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