## PIN Diode Shunt Switch Element 50 MHz to 10 GHz



MASW-011164

Rev. V2

#### **Features**

- · 3 Terminal LPF Broadband Shunt Structure
- 50 MHz 10 GHz Broadband Frequency
- >40 W Peak Power Handling
- <0.1 dB Shunt Insertion loss</li>
- >27 dB Shunt Isolation
- RoHS\* Compliant

## **Applications**

 Wireless Telecommunications Infrastructure & Test Instrument Applications

### **Description**

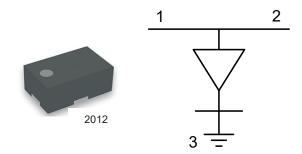
The MASW-011164 is a broadband, high linearity, medium power shunt switch element in a lead free 1.9 x 1.1 mm DFN surface mount plastic package.

This device is designed for wireless telecommunications infrastructure and test instrument applications. It is also suited for other applications in  $0.05 \sim 10$  GHz.

## **Ordering Information**

Part Number	Package
MASW-011164-20120T	500 Piece Reel

#### Pin Out / Schematic



## Pin Configuration<sup>3</sup>

Pin#	Pin Name Description		
1	RF <sub>IN</sub>	RF Input	
2	RF <sub>OUT</sub>	RF Output	
3	Paddle <sup>4</sup>	Ground	

- MACOM recommends connecting unused package pins to ground.
- The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

## Electrical Specifications: $T_A = +25$ °C

Parameter	Test Conditions	Units	Min.	Тур.	Max.
Breakdown Voltage (V <sub>B</sub> )	I <sub>R</sub> = 10 μA	V	400	600	_
Insertion Loss (I <sub>L</sub> )	V <sub>R</sub> = 25 V, 512 MHz V <sub>R</sub> = 25 V, 2.7 GHz	dB		0.08 0.10	_
Isolation (I <sub>SO</sub> )	I <sub>F</sub> = 10 mA, 512 MHz I <sub>F</sub> = 10 mA, 2.7 GHz	dB		28 27	_
Input / Output Return Loss	V <sub>R</sub> = 25 V, 512 MHz V <sub>R</sub> = 25 V, 2.7 GHz	dB		34 37	_
Minority Carrier Lifetime (T <sub>L</sub> )	I <sub>F</sub> = 10 mA, I <sub>R</sub> = 6 mA, @ 50%	ns	_	3000	_

<sup>\*</sup> Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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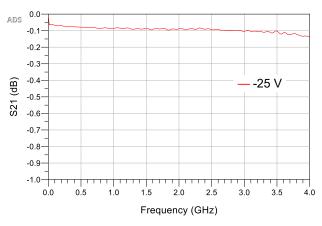
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## **Absolute Maximum Ratings**

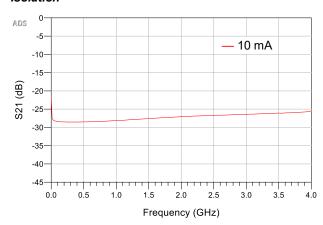
Parameter	Absolute Maximum		
Breakdown Voltage	600 V		
Forward Current	d Current 200 mA		
Junction Temperature	+175°C		
Storage Temperature	-65°C to +150°C		
Assembly Temperature	+260°C Per JEDEC STD-J-20C		

## **Typical Performance Curves**

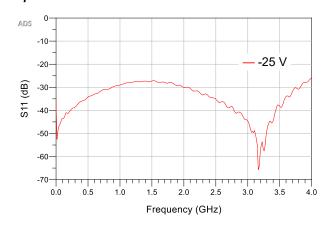
#### **Insertion Loss**



#### Isolation



#### Input Return Loss

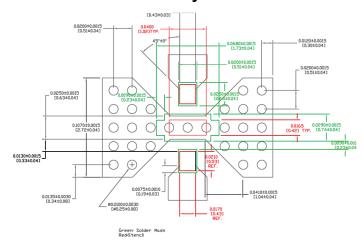




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### **Printed Circuit Board Layout**

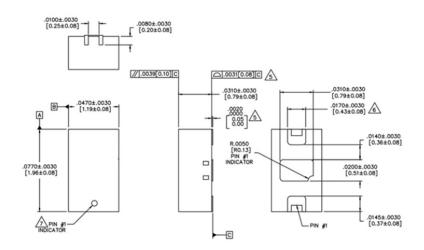


NOTE: If possible, use copper filled vias underneath pin 3 for better thermals; otherwise, use vias that are plated through, filled and plated over.

Solder mask should provide a 60 µm clearance between copper pad and soldermask. Rounded pkg pads should have matching rounded solder mask openings.

Use circles or squares for the thermal land stencil such that only get 50% to 80% solder paste coverage.

## **Outline (2012)**



#### NOTES

- 1. DIMENSIONS DO NOT INCLUDE MOLD FLASHING
- 2. BURRS AND DUMBAR SHALL NOT EXCEED 0.002" PER SURFACE
- 3, LEAD CO-PLANARITY IS 0,003" MAXIMUM

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