Digital Phase Shifter, 6-Bit
900 - 1200 MHz

MAPS-011021
Rev. V3

Features

- 6 Bit Digital Phase Shifter
- 360° Coverage with LSB = 5.625°
- Integrated Driver
- Serial or Parallel Control
- Low DC Power Consumption
- Minimal Attenuation Variation over Phase Shift Range
- 50 Ω Impedance
- Lead-Free 6 mm 28-Lead PQFN Package
- EAR99
- RoHS* Compliant

Applications

- Test & Measurement
- EW

Description

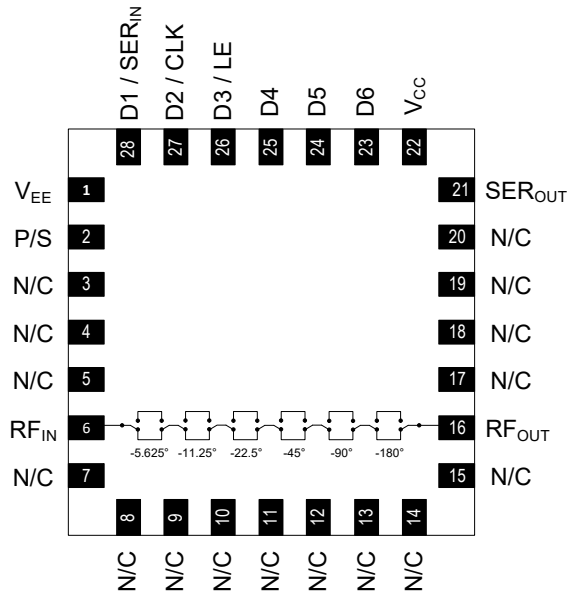
The MAPS-011021 is a GaAs pHEMT 6-bit digital phase shifter with an integrated driver in a 6 mm PQFN package. The step size is 5.625° providing phase shift from 0° to 360° in 5.625° steps. The rms phase error is only 1.5°. This design has been optimized to minimize variation in attenuation over the phase shift range.

The MAPS-011021 is ideally suited for use where high phase accuracy with minimum loss variation over the phase shift range are required.

Ordering Information

Part Number	Package
MAPS-011021-TR0500	500 Piece Reel
MAPS-011021-SMB	Evaluation Board

Functional Schematic



Pin Configuration[1,2,3]

Pin #	Name	Function
1	V_{EE}	Negative Supply
2	P/S	Parallel/Serial Select
3-5,7-15, 17-20	N/C	No Connection
6	RF_{IN}	RF Input
16	RF_{OUT}	RF Output
21	SER_{OUT}	Serial Output
22	V_{CC}	Positive Supply
23	D6	180° Bit
24	D5	90° Bit
25	D4	45° Bit
26	D3 or LE	22.5° Bit or LE
27	D2 or CLK	11.25° Bit or Clock
28	D1 or SER_{IN}	5.625° Bit or Serial Input

1. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.
2. Unused logic controls must be grounded.
3. MACOM recommends connecting unused package pins (N/C) to ground

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: Freq. = 0.9 - 1.2 GHz, T_A = 25°C, Z_0 = 50 Ω, V_{CC} = +5 V, V_{EE} = -5 V

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Operating Power [4]	0.9 to 1.2 GHz	dBm	—	—	25
Insertion Loss (Any Phase State)	Any Phase State	dB	—	3.5	3.8
Attenuation Variation	Peak to Peak Amplitude Change Across All Phase States	dB	—	—	0.5
RMS Attenuation Error [5]	All Values Relative to Insertion Loss at Reference Phase	dB	—	0.15	—
RMS Phase Error [5]	All Values Relative to Reference Phase	Deg.	—	2.0	—
Phase Accuracy Relative to Reference Loss State	5.6° Bit 11.2° Bit 22.5° Bit 45° Bit 90° Bit 180° Bit Sum of All Bits (354.4°)	Deg.	4.6 9.7 21.7 43.5 88.0 173.5 352.0	—-	6.6 13.5 25.3 46.8 96.0 181.5 358.0
VSWR	RF Input RF Output	Ratio	—	1.5:1 1.5:1	—
1 dB Compression	Reference State	dBm	—	29	—
Input IP3	Two-tones, +5 dBm, 10 MHz spacing	dBm	—	42	—
Phase Settling Time TRISE TFALL Ton Toff	 10% - 90% RF 90% - 10% RF 50% Control to +/-1° of final RF phase 50% Control to +/-1° of final RF phase	ns	—	 40 60 90 110	—
V_{CC} V_{EE}	—	V	+3.0 -5.5	—	+5.5 -3.0
V_{IL} V_{IH}	LOW-level input voltage HIGH-level input voltage	V	0.0 0.7 x V_{CC}	—	0.3 x V_{CC} V_{CC}
I_{IN} (Input Control Current)	V_{IN} = V_{CC} or GND	µA	—	1	—
V_{OH} V_{OL}	For serial out; I_{OH} = -100 µA For serial out; I_{OL} = +100 µA	V	V_{CC} - 0.2 —	—	— 0.2
I_{CC} (Quiescent Supply Current)	$V_{CONTROL}$ = V_{CC} or GND	µA	—	—	0.5
I_{EE}	V_{EE} min to max V_{IN} = V_{IL} or V_{IH}	mA	-0.5	—	—

4. Maximum operating power is the maximum power where the specifications are guaranteed.
5. RMS is calculated across all 64 amplitude or phase states relative to the amplitude or phase in the 0° phase state at a given frequency.

$$\delta phase\_RMS = \sqrt{\frac{1}{n}\sum_{m=1}^{n}\delta^2 phase - \left(\frac{1}{n}\sum_{m=1}^{n}\delta phase\right)^2}$$

Maximum Operating Conditions

Parameter	Absolute Maximum
Input Power	27 dBm
V_{CC}	0 V ≤ V_{CC} ≤ +6 V
V_{EE}	-6 V ≤ V_{EE} ≤ 0 V
D1-D6, P/S, LE, CLK or SER IN	0 V ≤ V_{IN} ≤ V_{CC}
SER OUT	0 V ≤ V_{OUT} ≤ V_{CC}
Operating Temperature	-40ºC to +85ºC

Absolute Maximum Ratings[6,7]

Parameter	Absolute Maximum
Input Power	28 dBm
V_{CC}	-0.5 V ≤ V_{CC} ≤ +7.0 V
V_{EE}	-7.0 V ≤ V_{EE} ≤ +0.5 V
D1-D6, P/S, LE, CLK or SER IN	-0.5 V ≤ V_{IN} ≤ V_{CC} + 0.5 V
SER OUT	-0.5 V ≤ V_{OUT} ≤ V_{CC} + 0.5 V
Storage Temperature	-65ºC to +150ºC

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.

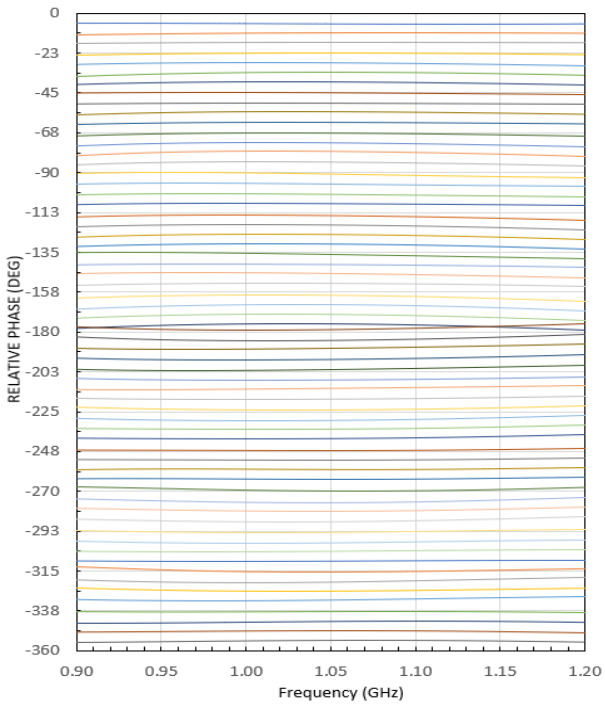
Handling Procedures

Please observe the following precautions to avoid damage:

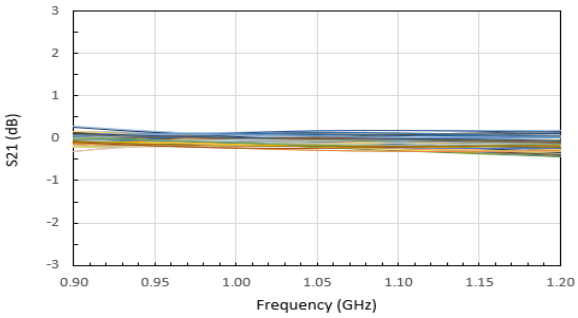
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

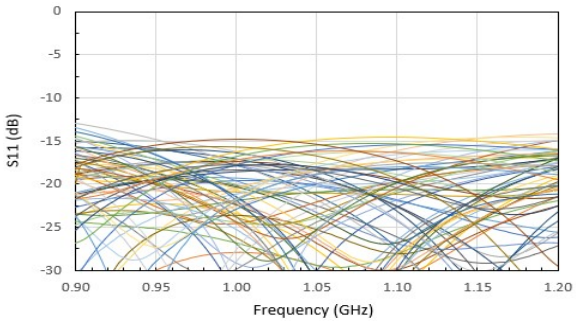
Normalized Phase Shift vs. Frequency



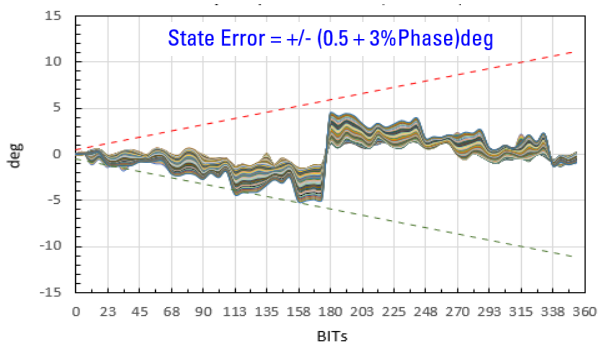
Normalized Attenuation Variation



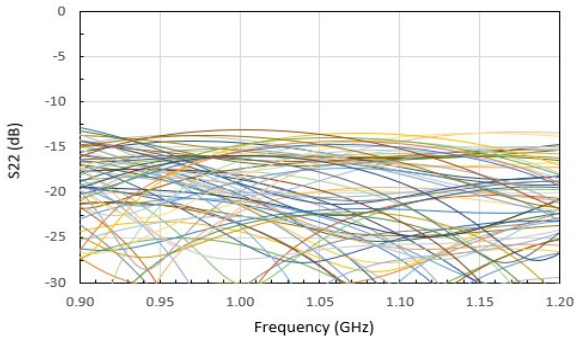
Input Return Loss (All States)



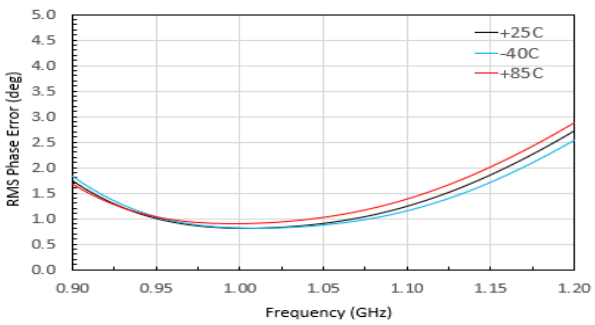
Phase Error vs State (All States)



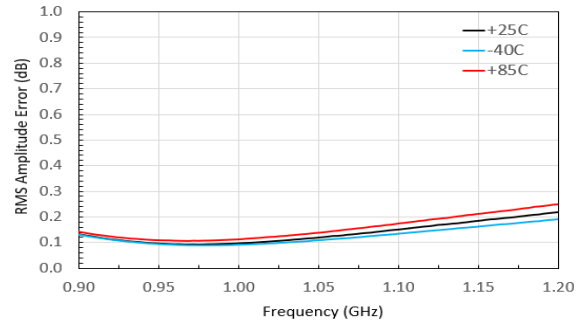
Output Return Loss (All States)



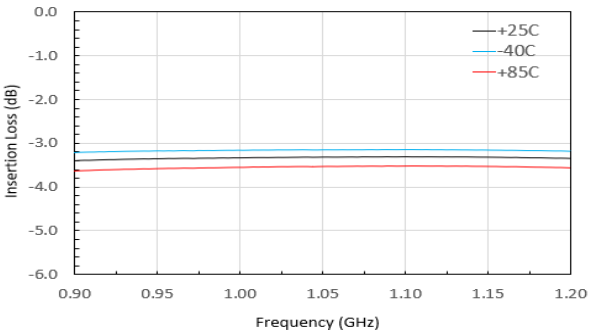
RMS Phase Error vs Temp



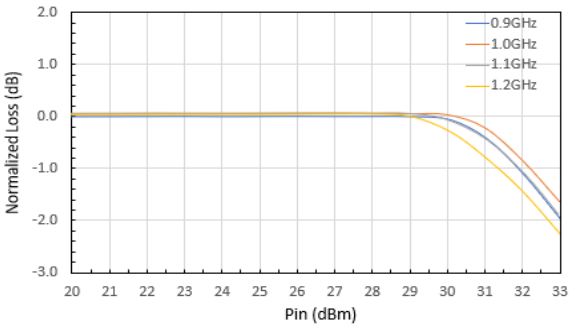
RMS Amplitude Error vs Temp



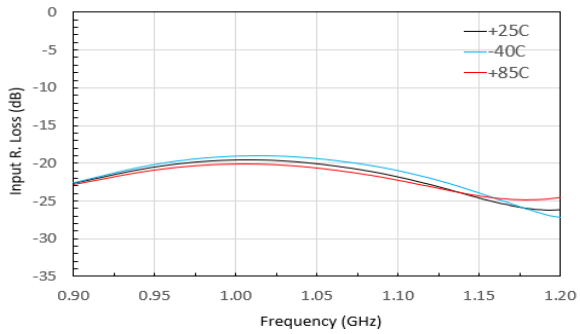
Insertion Loss vs Temp



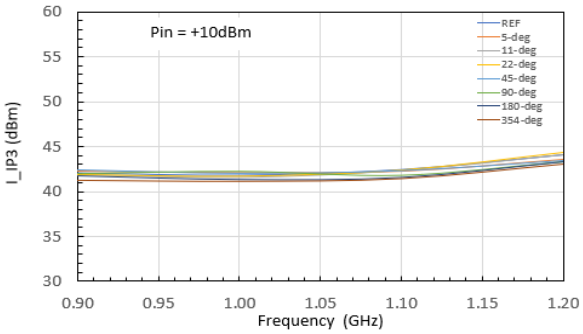
P1dB vs PIN and Frequency



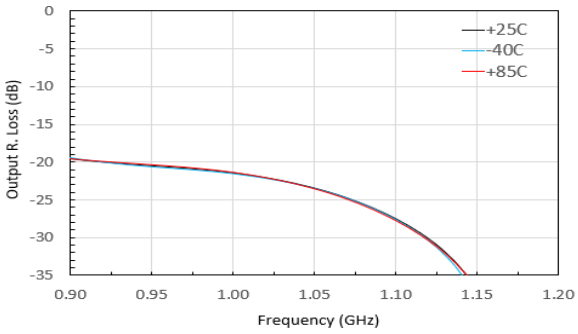
Input Return Loss vs Temp



I_IP3, Major States



Output Return Loss vs Temp



Modes of Operation: Serial and Direct Parallel

Bias Sequencing for both Modes

To avoid potential problems with application of supplies with floating controls, known logic levels (preferably 0 V) should be applied to the controls before the VDD and VEE are supplied. One easy way to do this is with pull down resistors. VDD an VEE can be applied in either order.

Serial Mode

The serial control interface (SERIN, CLK, LE, SEROUT) is compatible with the SPI protocol. SPI mode is activated when P/S is kept high. The 7-bit serial word must be loaded with the MSB first. After shifting in the 6 bit word, a rising edge on LE will set the phase shifter to the desired state. While LE is high the CLK is masked to protect the data while implementing the change. SEROUT is SERIN delayed by 6 clock cycles.

When P/S is low, the serial control interface is disabled. When P/S is set high, Pins 29, 30, and 31 have the LE, CLK, and SER IN function.

In serial mode operation, the outputs will stay constant while LE is kept low.

Direct Parallel Mode

The parallel mode is enabled when P/S is set low. In the direct parallel mode, the phase shifter is controlled by the parallel control inputs directly. When P/S is set low, Pins 29, 30, and 31 have the D3, D2, and D1 function.

Mode Truth Table

P/S	LE	Mode
1	X	Serial
0	N/A	Direct Parallel

Truth Table (Digital Phase Shifter)[8]

D6	D5	D4	D3	D2	D1	Phase Shift
0	0	0	0	0	0	Ref Phase
0	0	0	0	0	1	5.625°
0	0	0	0	1	0	11.25°
0	0	0	1	0	0	22.5°
0	0	1	0	0	0	45°
0	1	0	0	0	0	90°
1	0	0	0	0	0	180°
1	1	1	1	1	1	354.375°

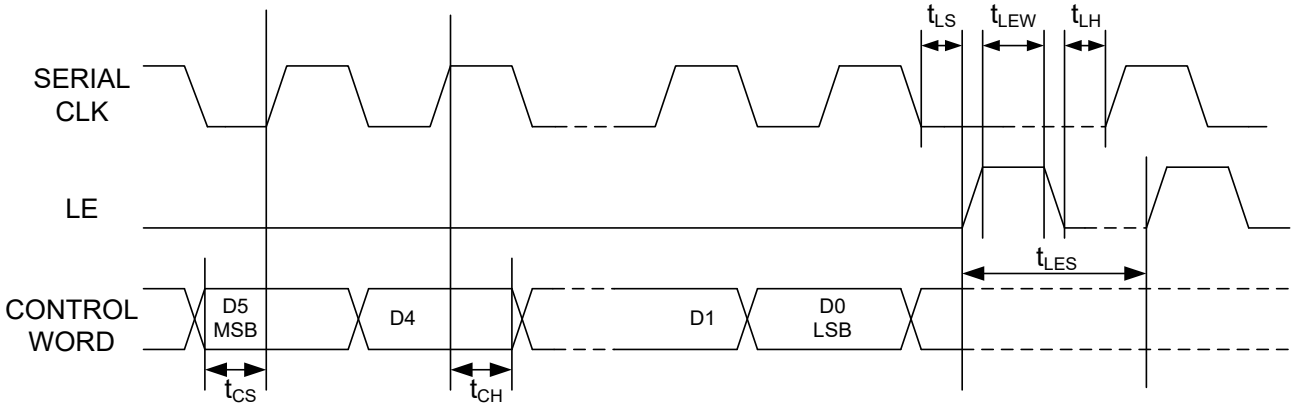
8. 0 = CMOS Low; 1 = CMOS High

Serial Interface Timing Characteristics

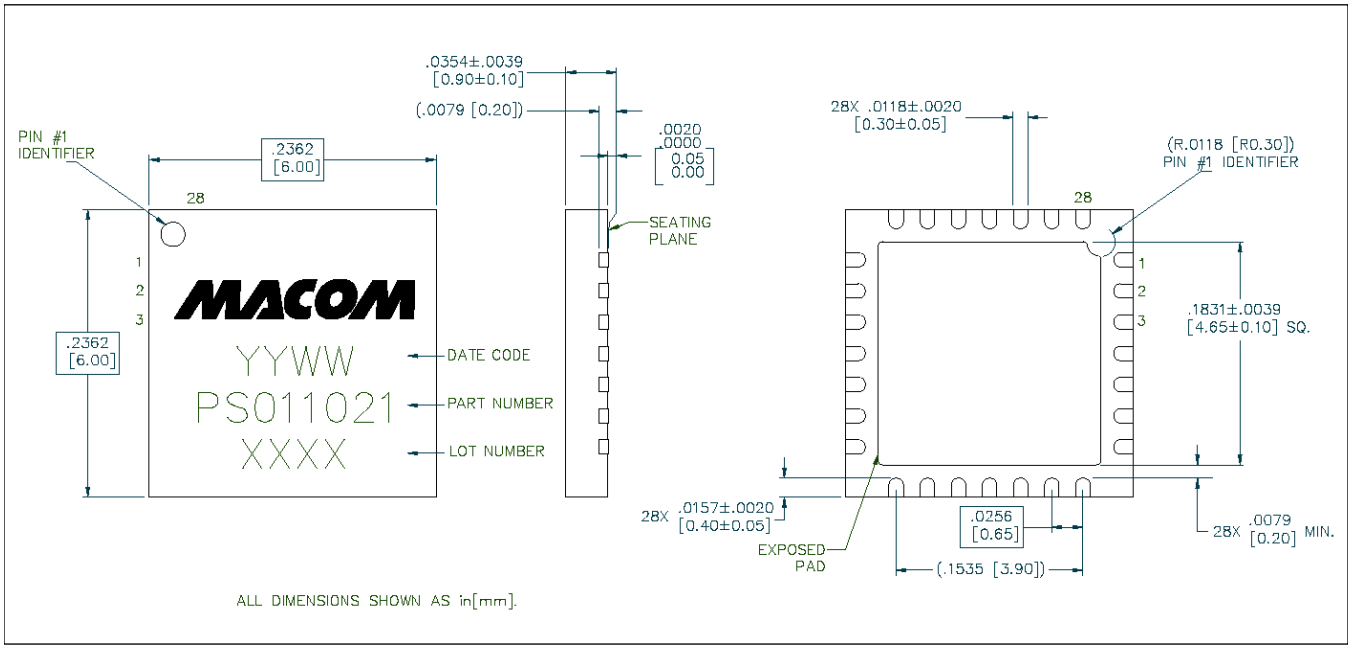
Symbol	Parameter	Typical Performance			Units
		-40°C	25°C	+85°C	
t_{SCK}	Min. Serial Clock Period	100	100	100	ns
t_{CS}	Min. Control Set-up Time	20	20	20	ns
t_{CH}	Min. Control Hold Time	20	20	20	ns
t_{LS}	Min. LE Set-up Time	10	10	10	ns
t_{LEW}	Min. LE Pulse Width	10	10	10	ns
t_{LH}	Min. Serial Clock Hold Time from LE	10	10	10	ns
t_{LES}	Min. LE Pulse Spacing	630	630	630	ns

Functionality
Modes of Operation: Serial and Direct Parallel

Serial Input Interface Timing Diagram



Lead Free 6 mm 28-Lead PQFN†



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level (MSL) 3 requirements.
Plating is 100% NiPdAuAg

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