0.5 W Ka-Band Power Amplifier
27 - 31.5 GHz

MAAP-011341
Rev. V1

Features

- 28 dB Gain
- 36 dBm Output IP3
- 27 dBm P1dB
- 28 dBm P3dB
- 5.5 V Drain Supply
- 4 mm, 24 lead AQFN Package
- RoHS* Compliant

Applications

- Satellite Communications

Description

The MAAP-011341 is a 1/2 W Ka-band power amplifier. The PA has a 27 dBm typical P1dB and a 28 dBm typical P3dB with 28 dB of gain. The drain bias supply is 5.5 V. The gate voltage is adjusted to set the drain current to 450 mA.

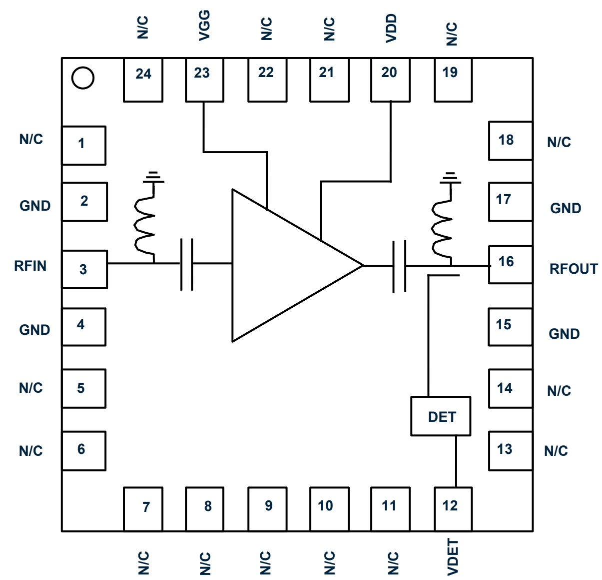
The MAAP-011341 is designed for medium power applications in the 27 - 31.5 GHz band. The 4 mm, 24 lead AQFN package is lead free and RoHS compliant.

It is also available as a bare DIE product under part number MAAP-011341-DIE.

Ordering Information

Part Number	Package
MAAP-011341-TR1000	1000 Piece Reel
MAAP-011341-TR3000	3000 Piece Reel
MAAP-011341-SMB	Sample Board

Block Diagram



Pin Configuration[1,2]

Pin #	Pin Name	Description
1,5-11, 13, 14, 18, 19, 21, 22, 24	N/C	No Connect
2,4,15,17	GND	Ground
3	RF_{IN}	RF Input
12	V_{DET}	Detector Voltage
16	RF_{OUT}	RF Output
20	V_{DD}	Drain Voltage
23	V_{GG}	Gate Voltage

1. It is recommended that all NC (No Connect) pins be grounded.
2. The exposed pad centered on the package bottom must be connected to RF, DC, and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: V_{DD} = +5.5 V, IDQ = 450 mA, T_A = 25°C, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	27 - 31.5 GHz	dB	24.5	28	—
Gain Flatness	27 - 31.5 GHz	dB	—	0.5	—
Input Return Loss	27 - 31.5 GHz	dB	—	10	—
Output Return Loss	27 - 31.5 GHz	dB	—	10	—
P1dB	27 - 31.5 GHz	dBm	—	27	—
P3dB	27 - 31.5 GHz	dBm	—	28	—
P_{OUT}	27 GHz, P_{IN} = 4.0 dBm 31.5 GHz, P_{IN} = 3.5 dBm	dBm	26.5 26.0	28.0 27.5	—
IP3	27 - 31.5 GHz, P_{OUT} = 16 dBm/tone 10 MHz	dBm	—	36	—
Noise Figure	27 - 31.5 GHz	dB	—	5	—
V_{DET}	3 dBm Output Power 27 dBm Output Power	V	—	0.1 1.5	—

Maximum Operating Conditions

Parameter	Maximum
Input Power	8 dBm
V_{DD}	+6 V
V_{GG}	-3 to 0 V
Junction Temperature[3,4]	+160°C
Operating Temperature	-40°C to +85°C

3. Operating at nominal conditions with T_J ≤ +160°C will ensure MTTF > 1 x 10^6 hours.
4. TX Junction Temp. (T_J) = T_C + Θjc * ((V * I) - (P_{OUT} - P_{IN})).
   Typical TX thermal resistance (Θjc) = 29.3°C/W.
   a) For T_C = +85°C and 31 GHz,
   T_J = 148°C @ 5.5 V, 460 mA, P_{OUT} = 26 dBm, P_{IN} = 4.5 dBm
   b) For T_C = +25°C and 31 GHz,
   T_J = 83°C @ 5.5 V, 460 mA, P_{OUT} = 27.5 dBm, P_{IN} = 3.5 dBm

Bias Sequence

All gate voltages must be applied prior to applying drain voltages.

1. Apply V_{GG} (about -1.5 V) to pin 23.
2. Apply V_{DD} (+5.5 V) to pin 20.
3. Adjust V_{GG} to set I_{DQ} to 450 mA.

Shut down by setting V_{DD} = 0 V first.

Absolute Maximum Ratings[5,6]

Parameter	Absolute Maximum
Input Power	10 dBm
V_{DD}	+6.5 V
V_{GG}	-5 to 0 V
Junction Temperature[7]	+180°C
Storage Temperature	-55°C to +150°C

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.
7. Junction temperature directly effects device MTTF. Junction temperature should be kept as low as possible to maximize lifetime.

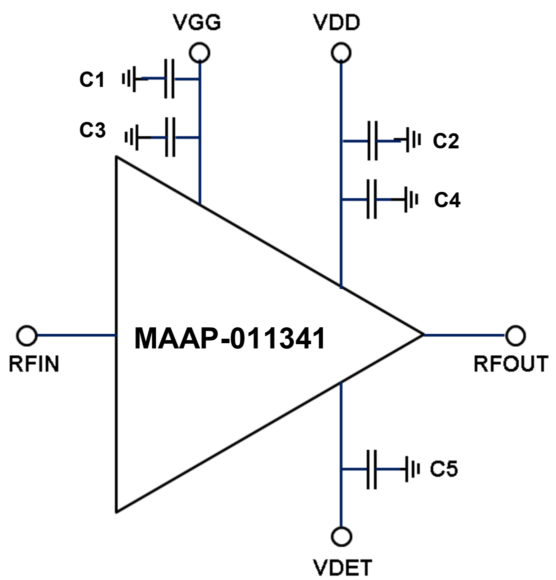
Handling Procedures

Please observe the following precautions to avoid damage:

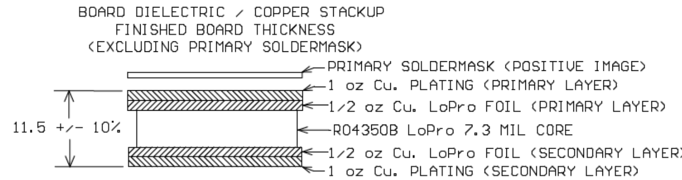
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1B devices.

Application Schematic

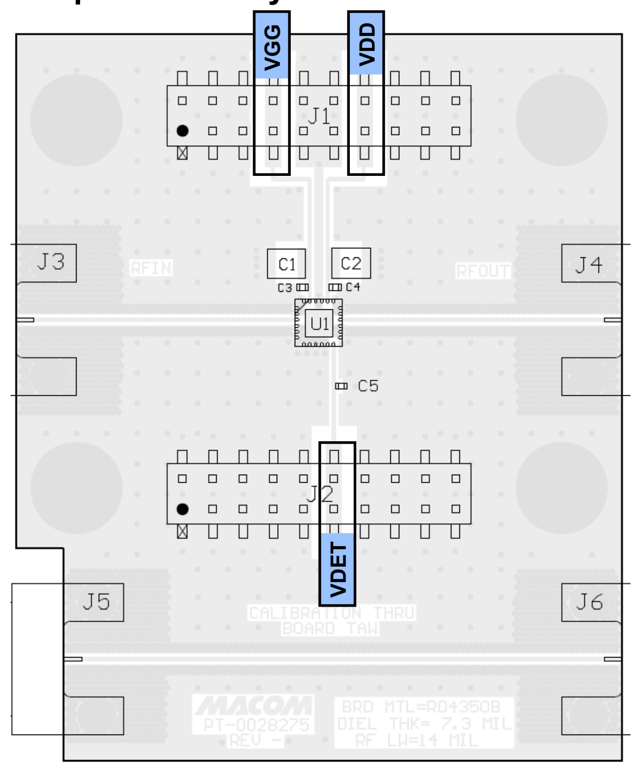


PCB Layout Stack-Up



Finished board thickness is in mils

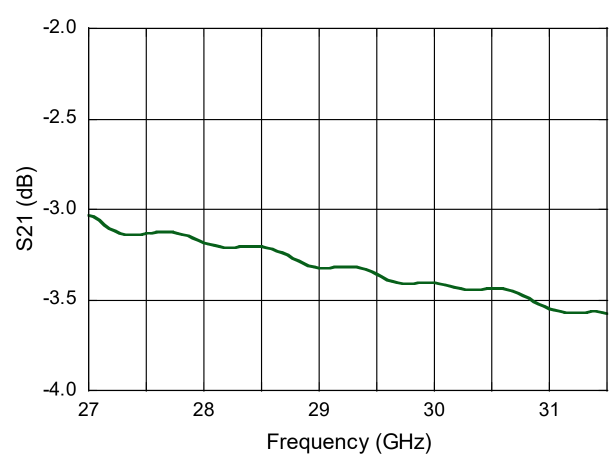
Sample Board Layout



Parts List

Part #	Value	Case Style
C1, C2	10 µF	1210
C3, C4	1000 pF	0402
C5	1 µF	0402
J1, J2	100-mil pitch double row DC header	
J3 - J6	Southwest 2.4 mm, 5 mil pin diameter	

Sample Board Thru Line Loss

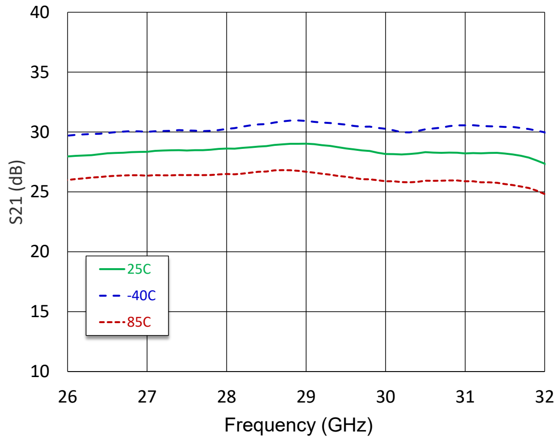


Recommended PCB Information

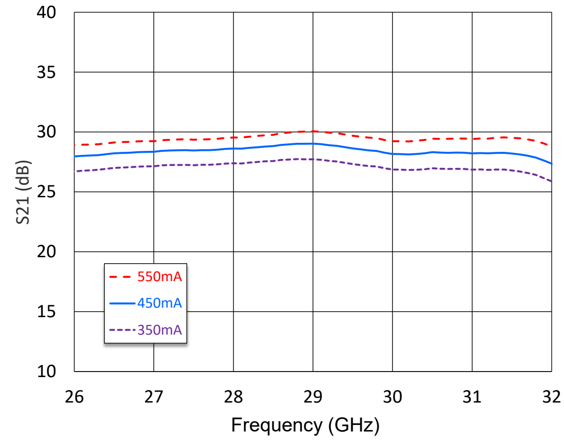
RF input and output are 50 Ω transmission lines on single layer 7.3 mil Rogers RO4350B LoPro with 1.5 oz. Cu. For best thermal management, use as many copper filled vias under the device as physically possible. The filled vias should be plated over. 8 mil diameter vias in a 5 x 5 array are used on this sample board.

Typical Performance Curves: V_{DD} = 5.5 V, I_{DQ} = 450 mA

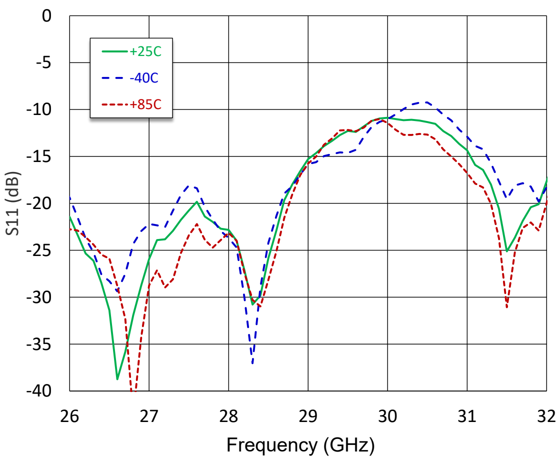
Small Signal Gain vs. Frequency over Temperature



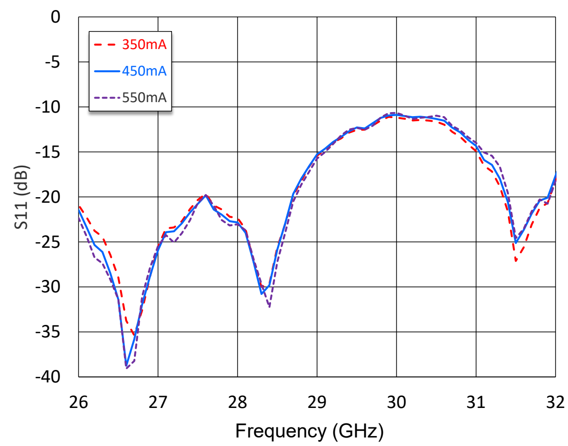
Small Signal Gain vs. Frequency over Bias Current



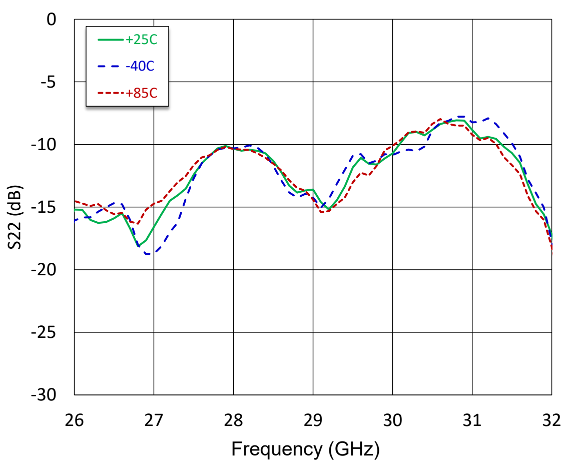
Input Return Loss vs. Frequency over Temperature



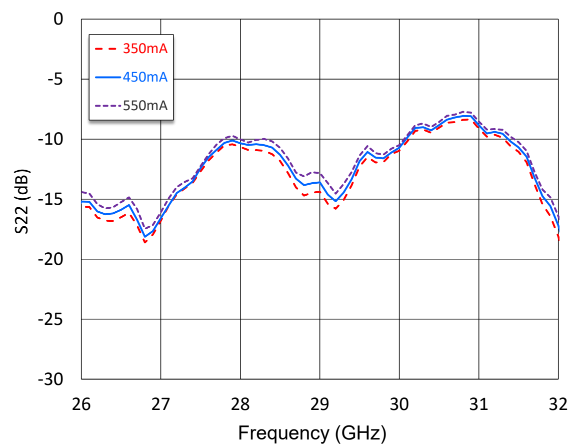
Input Return Loss vs. Frequency over Bias Current



Output Return Loss vs. Frequency over Temperature

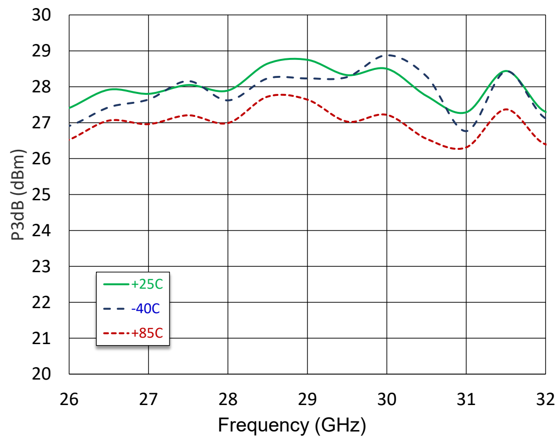


Output Return Loss vs. Frequency over Bias Current

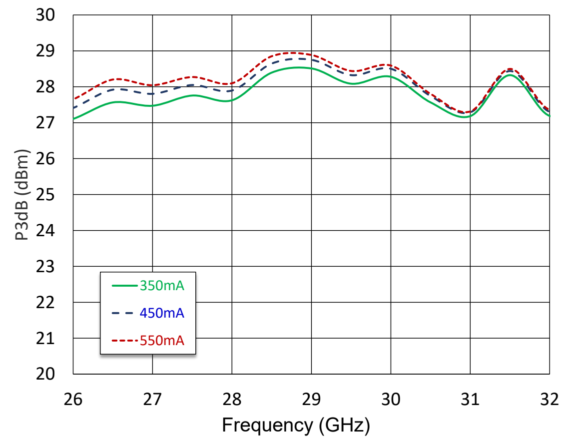


Typical Performance Curves: V_{DD} = 5.5 V, I_{DQ} = 450 mA

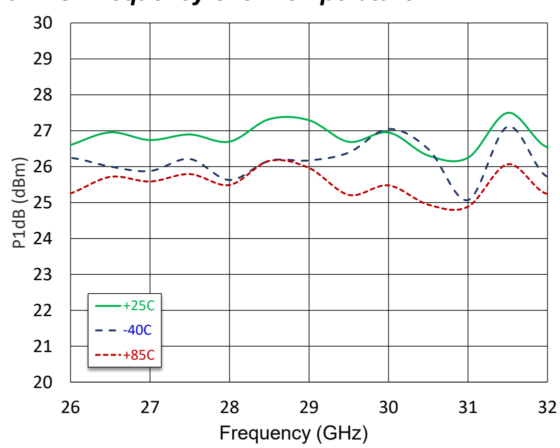
P3dB vs. Frequency over Temperature



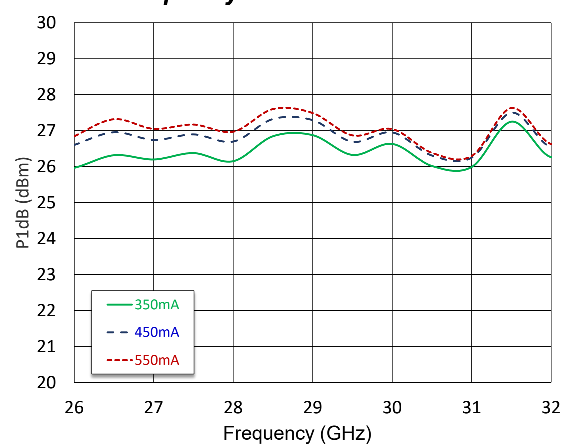
P3dB vs. Frequency over Bias Current



P1dB vs. Frequency over Temperature

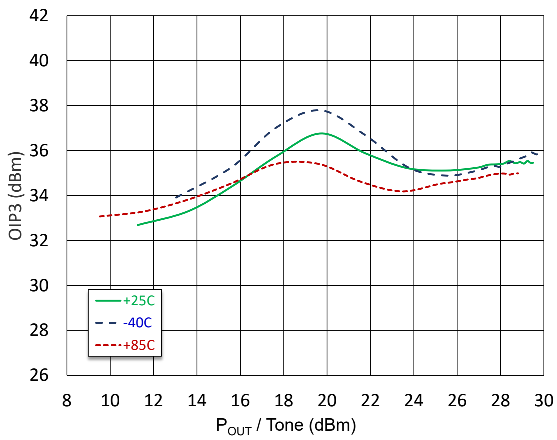


P1dB vs. Frequency over Bias Current

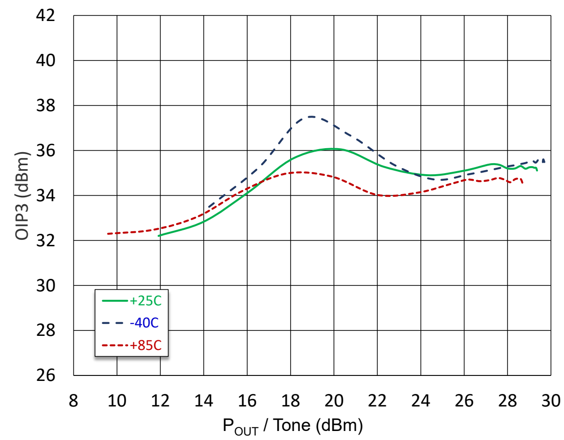


Typical Performance Curves: V_{DD} = 5.5 V, I_{DQ} = 450 mA

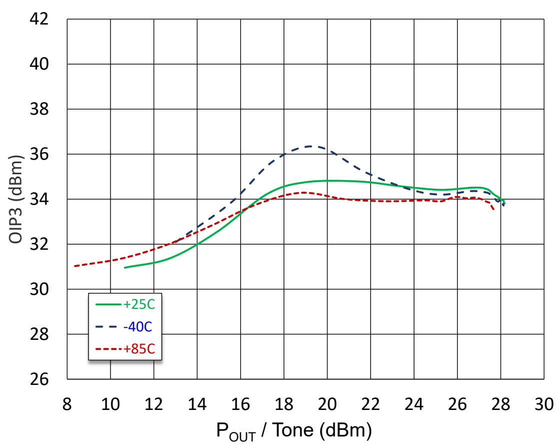
Output IP3 vs. Frequency over Temperature @ 27 GHz



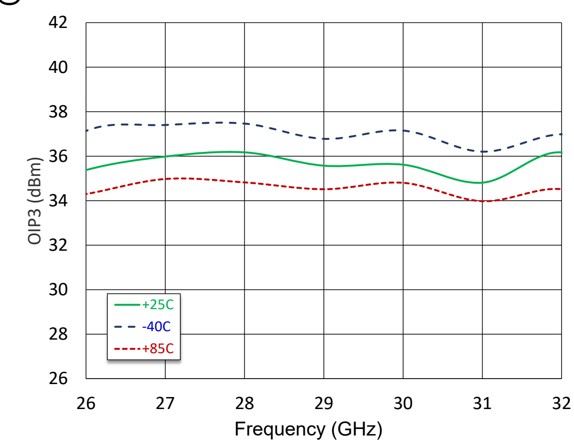
Output IP3 vs. Frequency over Temperature @ 29 GHz



Output IP3 vs. Frequency over Temperature @ 31 GHz

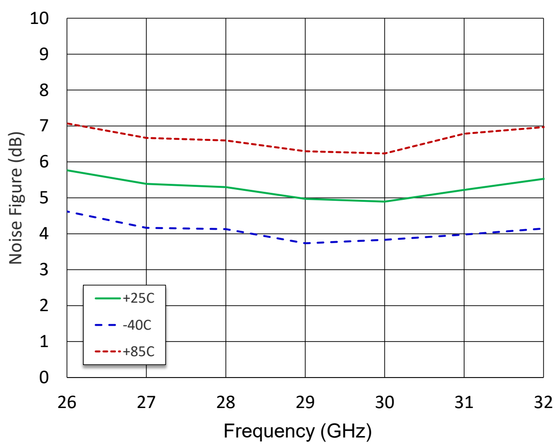


Output IP3 vs. Frequency over Temperature @ 19 dBm/TONE

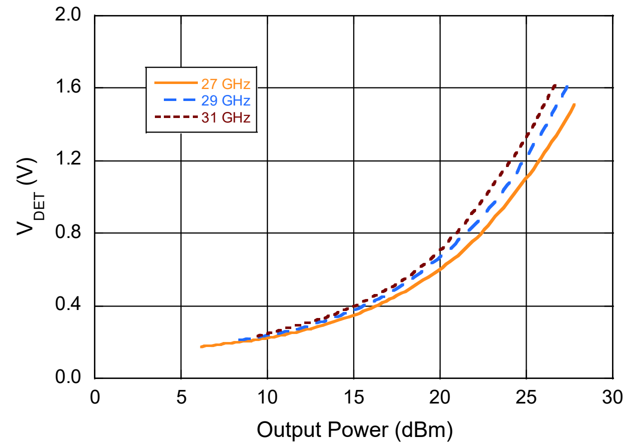


Typical Performance Curves: V_{DD} = 5.5 V, I_{DQ} = 450 mA

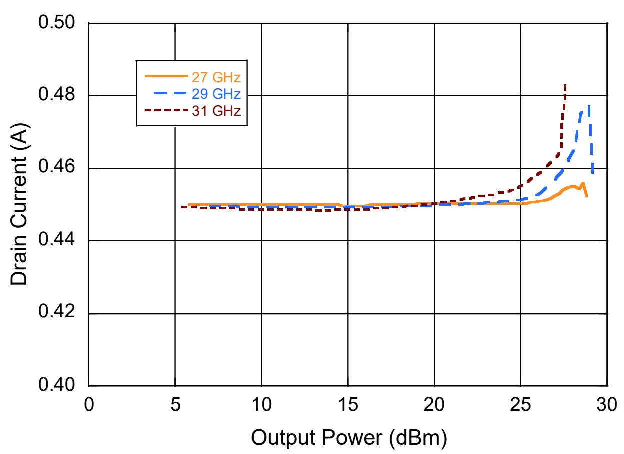
Noise Figure vs. Frequency over Temperature



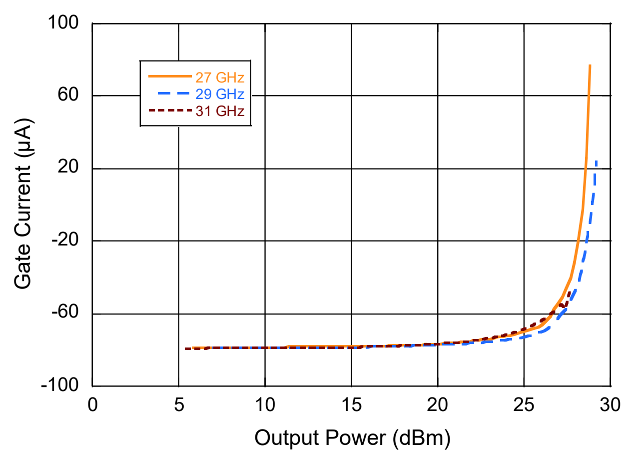
Detector Voltage vs. Output Power



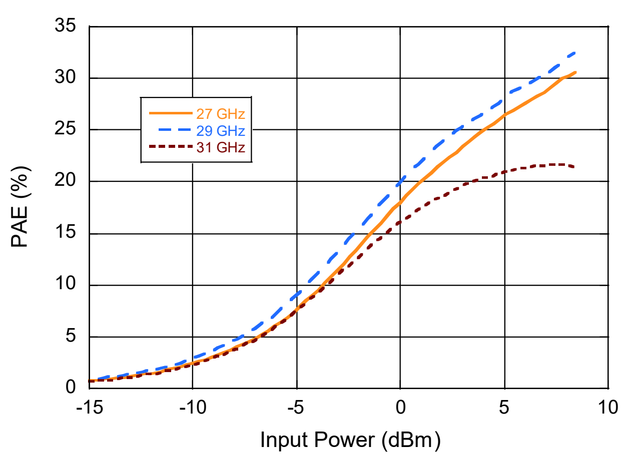
Drain Current vs Output Power



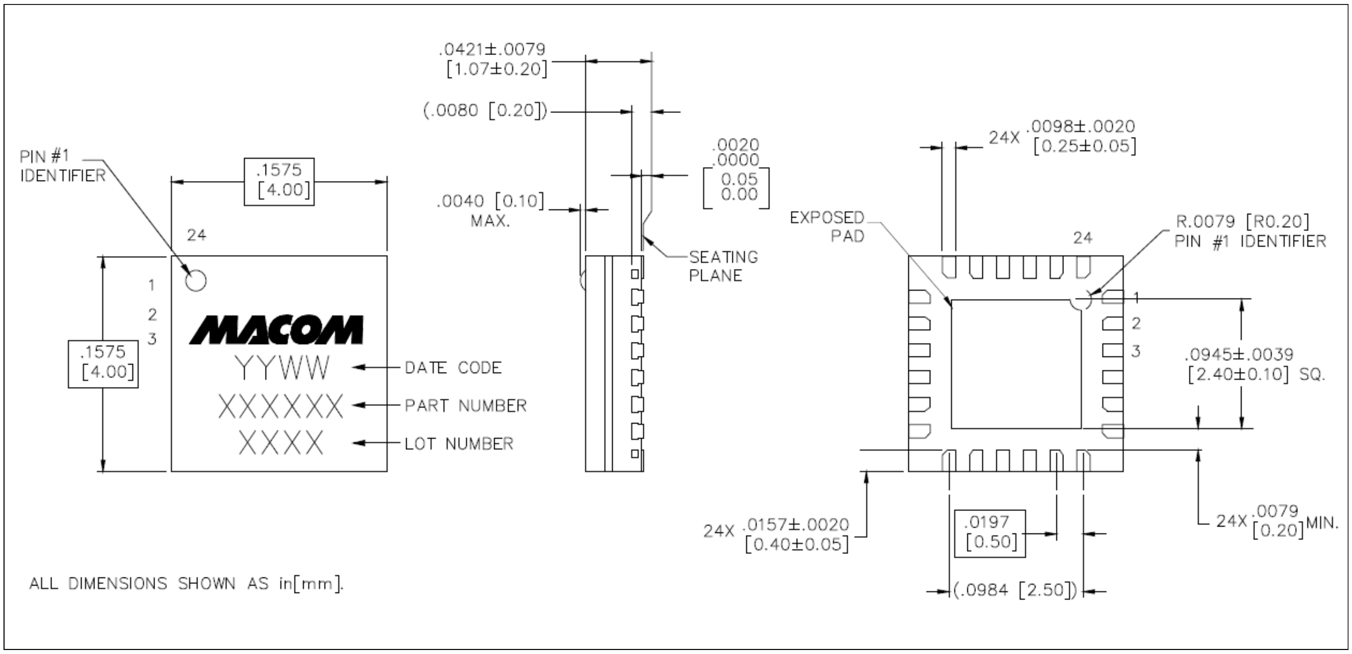
Gate Current vs Output Power



PAE vs Input Power



Lead-Free 4 mm 24-Lead AQFN Package†



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.
Plating is NiPdAuAg