# 0.25 W Ka-Band Amplifier
# 27 - 31.5 GHz



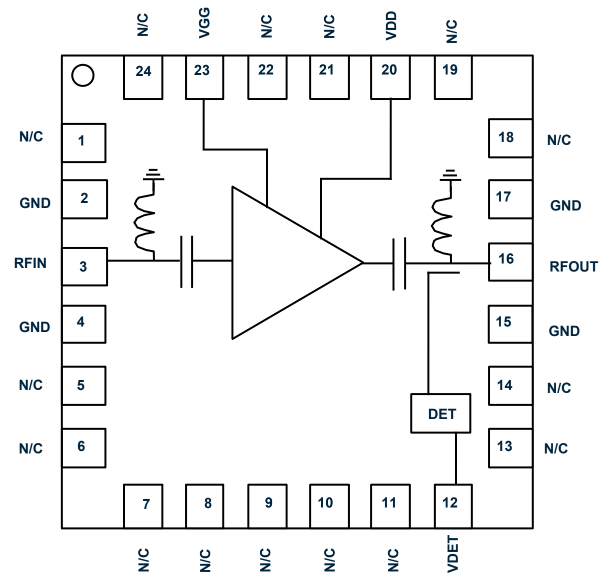
## Features
- 25 dB Gain
- 33 dBm Output IP3
- 24 dBm P1dB
- 25 dBm P3dB
- 5.5 V Drain Supply
- 4 mm, 24 lead AQFN Package
- RoHS* Compliant

## Applications
- Ka-Band Communication

## Description
The MAAP-011340 is a 1/4 W Ka-band amplifier. The amplifier has a 24 dBm typical P1dB and a 25 dBm typical P3dB with 25 dB of gain. The typical IP3 is 33 dBm. The drain bias supply is 5.5 V. The gate voltage is adjusted to set the drain current to 275 mA.

The MAAP-011340 is designed for Ka-band satellite communication applications. The 4 mm, 24 lead AQFN package is lead free and RoHS compliant.

## Block Diagram




## Ordering Information[1]

| Part Number | Package |
|---|---|
| MAAP-011340-TR1000 | 1000 Piece Reel |
| MAAP-011340-TR3000 | 3000 Piece Reel |
| MAAP-011340-SMB | Sample Board |

1. Reference Application Note M513 for reel size information.

## Pin Configuration[2,3]

| Pin # | Pin Name | Description |
|---|---|---|
| 1,5-11, 13, 14, 18, 19, 21, 22, 24 | N/C | No Connect |
| 2,4,15,17 | GND | Ground |
| 3 | RFIN | RF Input |
| 12 | VDET | Detector Voltage |
| 16 | RFOUT | RF Output |
| 20 | VDD | Drain Voltage |
| 23 | VGG | Gate Voltage |

2. It is recommended that all NC (No Connect) pins be grounded.
3. The exposed pad centered on the package bottom must be connected to RF, DC, and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

## Electrical Specifications:
## Freq. = 27.0 - 31.5 GHz, $V_{DD}$ = +5.5 V, $I_{DQ}$ = 275 mA, $T_A$ = 25°C, $Z_0$ = 50 Ω

| Parameter | Test Conditions | Units | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| Gain | — | dB | 22 | 25 | — |
| Gain Flatness | — | dB | — | ± 0.7 | — |
| Input Return Loss | — | dB | — | 10 | — |
| Output Return Loss | — | dB | — | 10 | — |
| P1dB | — | dBm | — | 24 | — |
| P3dB | — | dBm | — | 25 | — |
| $P_{OUT}$ | 27 GHz, $P_{IN}$ = 4.0 dBm<br>31.5 GHz, $P_{IN}$ = 4.0 dBm | dBm | 24.5<br>23.5 | 25.5<br>24.5 | — |
| Output IP3 | $P_{OUT}$ = 16 dBm per tone with 10 MHz spacing | dBm | — | 33 | — |
| Noise Figure | — | dB | — | 6.1 | — |
| $V_{DET}$ | 0 dBm Output Power<br>24 dBm Output Power | V | —<br>1.4 | 0.6<br>1.8 | —<br>2.1 |
| $V_{GG}$ | Small Signal | V | — | -0.68 | — |
| $I_{GG}$ | Small Signal<br>P3dB | mA | — | -0.7<br>-0.8 | — |
| $I_{DD}$ | P1dB<br>P3dB | mA | — | 300<br>320 | — |

## Bias Sequence

All gate voltages must be applied prior to applying drain voltages.

1. Apply $V_{GG}$ (about -0.75 V) to pin 23.
2. Apply $V_{DD}$ (+5.5 V) to pin 20.
3. Adjust $V_{GG}$ to set $I_{DQ}$ to 275 mA.

Shut down by removing $V_{DD}$ first.

## Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1C and CDM Class C2A devices.

## Maximum Operating Conditions

| Parameter | Maximum |
|---|---|
| TX Input Power | +5 dBm |
| $V_{DD}$ | +6 V |
| $V_{GG}$ | -3 to 0 V |
| Junction Temperature[4,5] | +160°C |
| Operating Temperature | -40°C to +85°C |

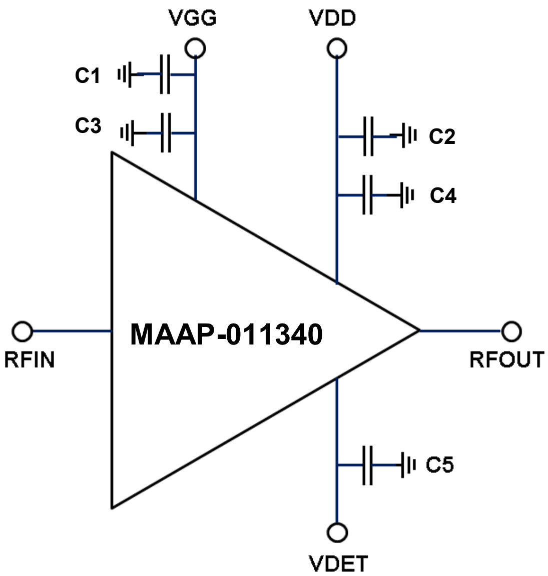
4. Operating at nominal conditions with $T_J \le$ +160°C will ensure MTTF > 1 x $10^6$ hours.
5. TX Junction Temp. ($T_J$) = $T_C$ + ϴjc * ((V * I) - ($P_{OUT}$ - $P_{IN}$)).
   Typical TX thermal resistance (ϴjc) = 42°C/W.
   a) For $T_C$ = +85°C,
   $T_J$ = 148.5°C @ 5.5 V, 275 mA

## Absolute Maximum Ratings[6,7]

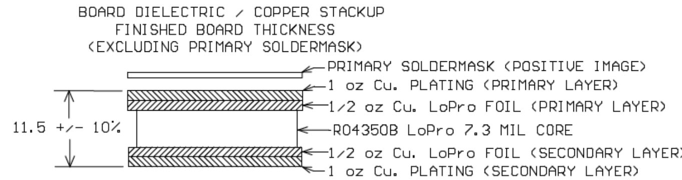
| Parameter | Absolute Maximum |
|---|---|
| TX Input Power | +8 dBm |
| $V_{DD}$ | +6.5 V |
| $V_{GG}$ | -5 to 0 V |
| Junction Temperature[8] | +175°C |
| Storage Temperature | -65°C to +125°C |

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.
8. Junction temperature directly effects device MTTF. Junction temperature should be kept as low as possible to maximize lifetime.

## Application Schematic

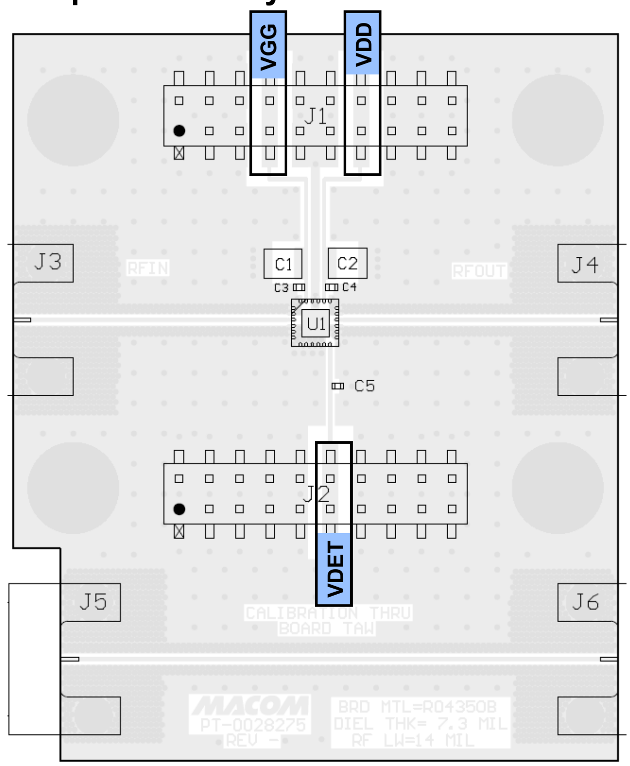



## PCB Layout Stack-Up




Finished board thickness is in mils

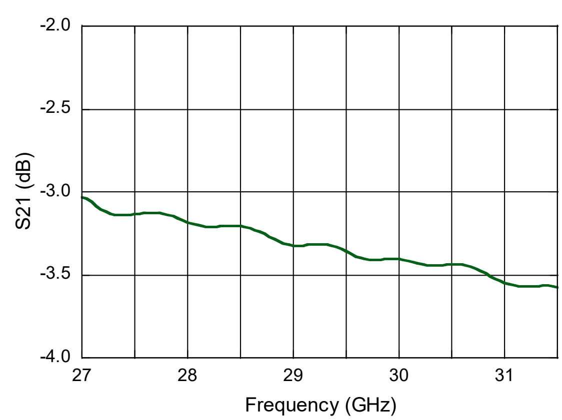
## Sample Board Layout




## Parts List

| Part # | Value | Case Style |
|---|---|---|
| C1, C2 | 10 µF | 1210 |
| C3, C4 | 1000 pF | 0402 |
| C5 | 1 µF | 0402 |
| J1, J2 | 100-mil pitch double row DC header | |
| J3 - J6 | Southwest 2.4 mm, 5 mil pin diameter | |

***Sample Board Thru Line Loss***

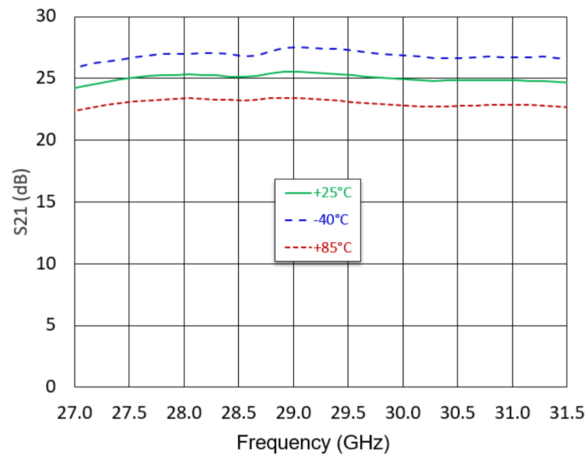



## Recommended PCB Information

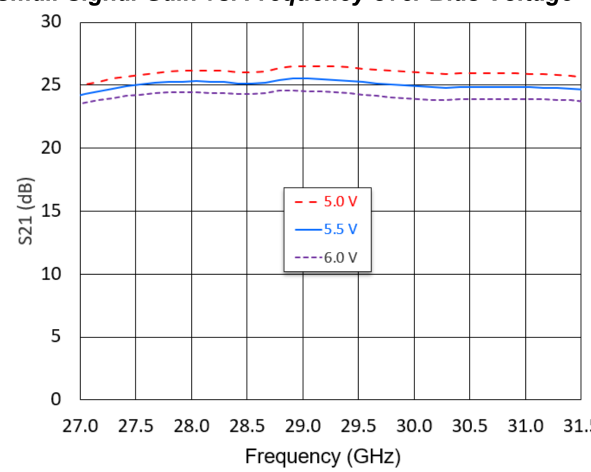
RF input and output are 50 Ω transmission lines on single layer 7.3 mil Rogers RO4350B LoPro with 1.5 oz. Cu. For best thermal management, use as many copper filled vias under the device as physically possible. The filled vias should be plated over. 8 mil diameter vias in a 5 x 5 array are used on this sample board.

## Typical Performance Curves:

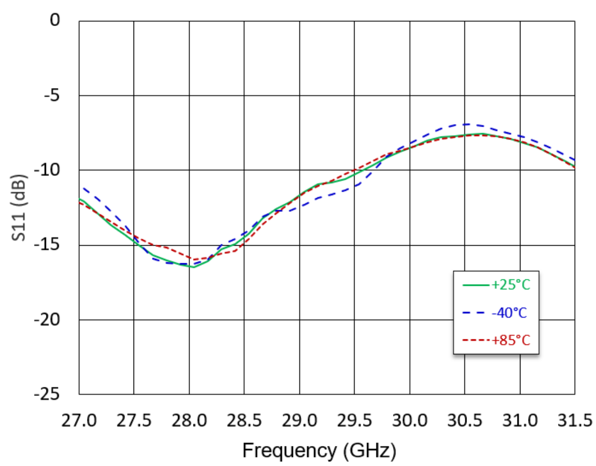
*Small Signal Gain vs. Frequency over Temperature*



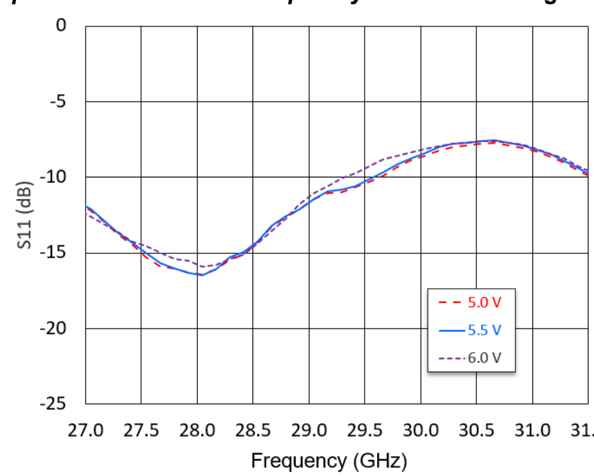

*Small Signal Gain vs. Frequency over Bias Voltage*



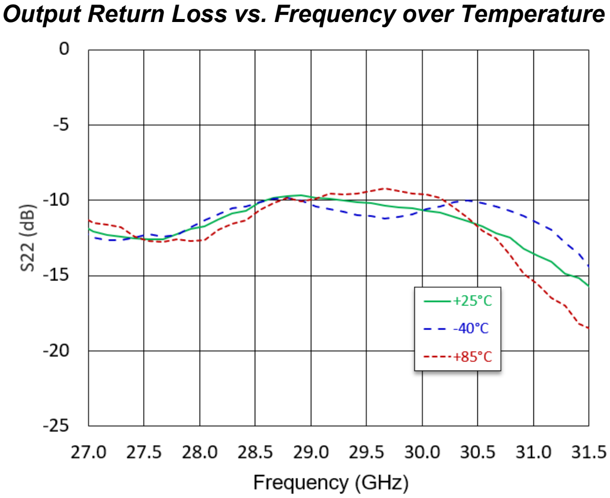

*Input Return Loss vs. Frequency over Temperature*



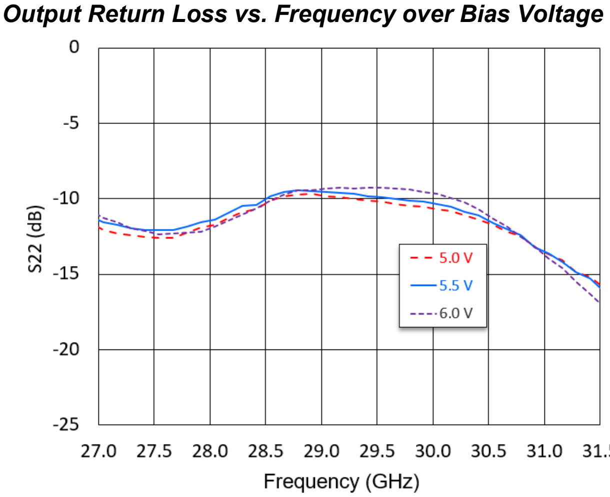

*Input Return Loss vs. Frequency over Bias Voltage*




*Output Return Loss vs. Frequency over Temperature*

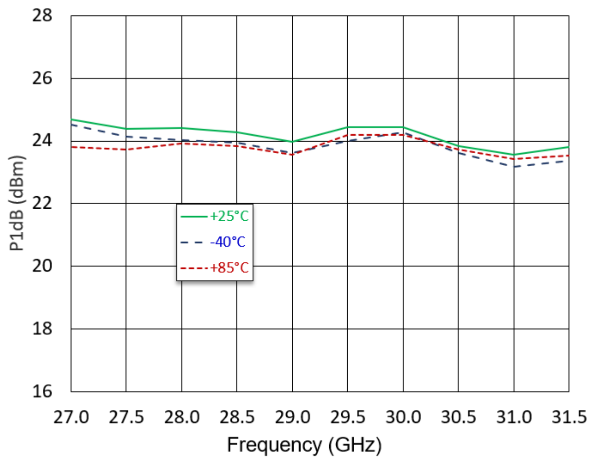



*Output Return Loss vs. Frequency over Bias Voltage*

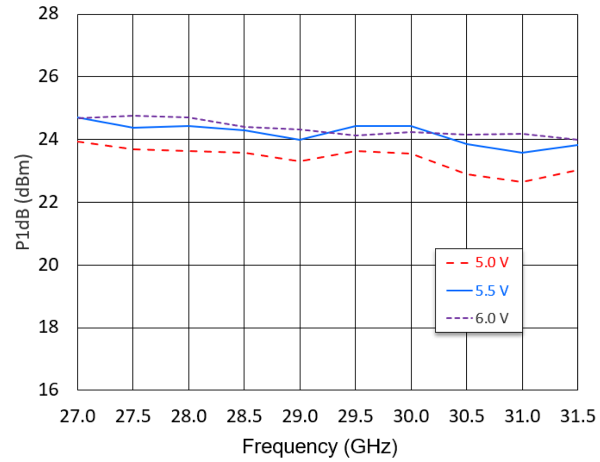


## Typical Performance Curves:

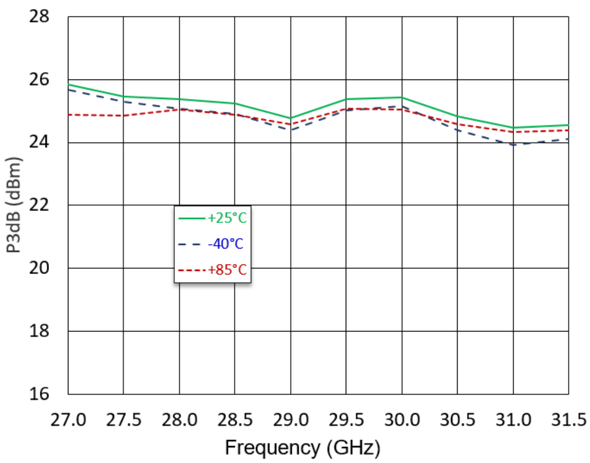
### *P1dB vs. Frequency over Temperature*



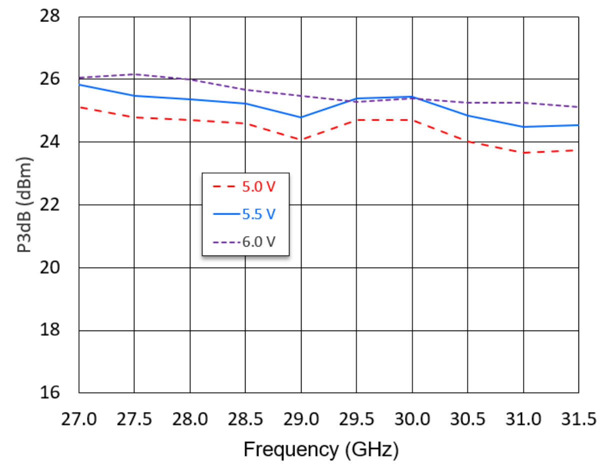

### *P1dB vs. Frequency over Bias Voltage*



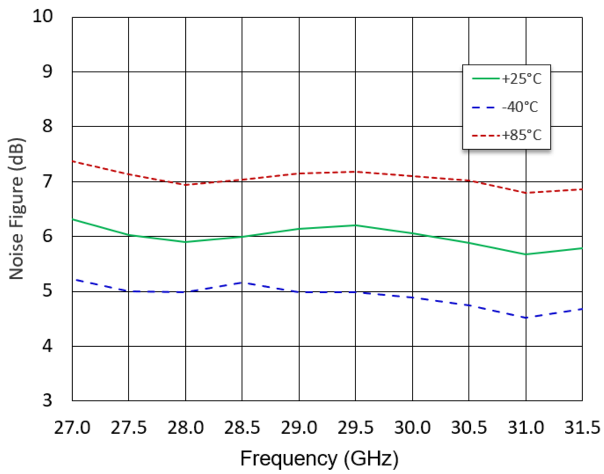

### *P3dB vs. Frequency over Temperature*



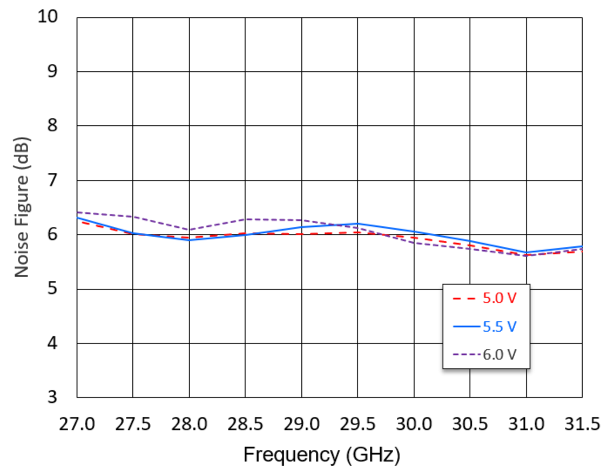

### *P3dB vs. Frequency over Bias Voltage*




### *Noise Figure vs. Frequency over Temperature*

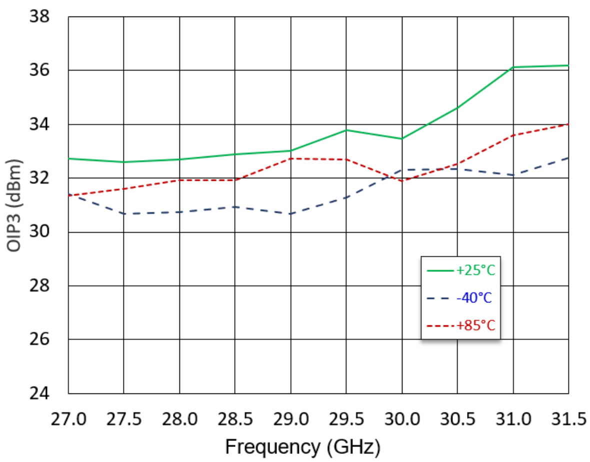



### *Noise Figure vs. Frequency over Bias Voltage*

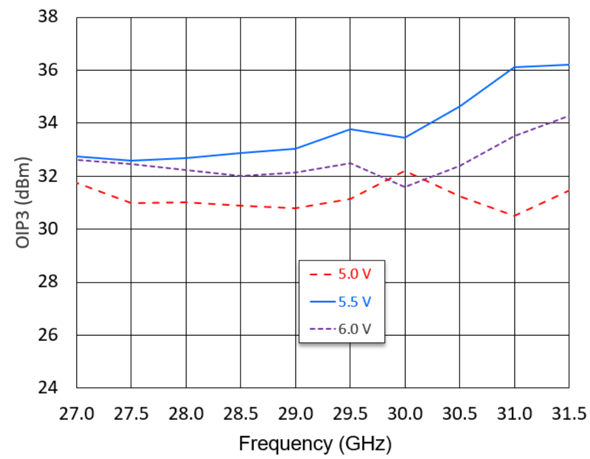


## Typical Performance Curves:

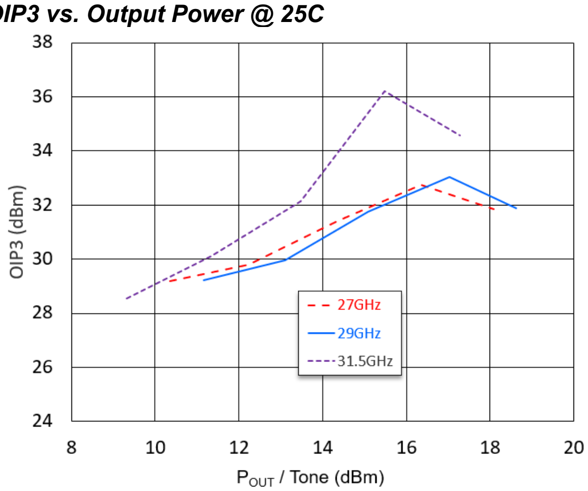
***OIP3 over Temperature ($P_{OUT}$ = 16 dBm / Tone)***



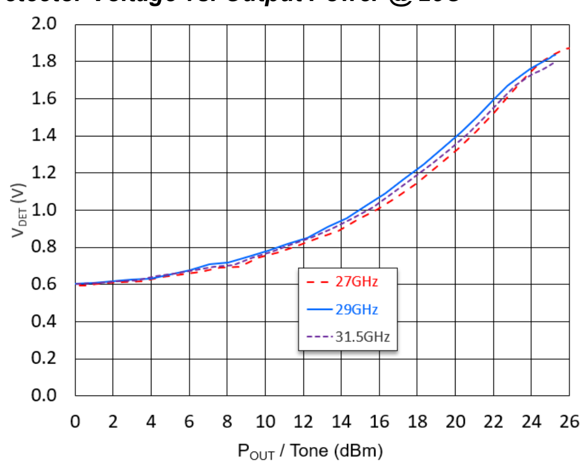

***OIP3 over Bias Voltage ($P_{OUT}$ = 16 dBm / Tone)***



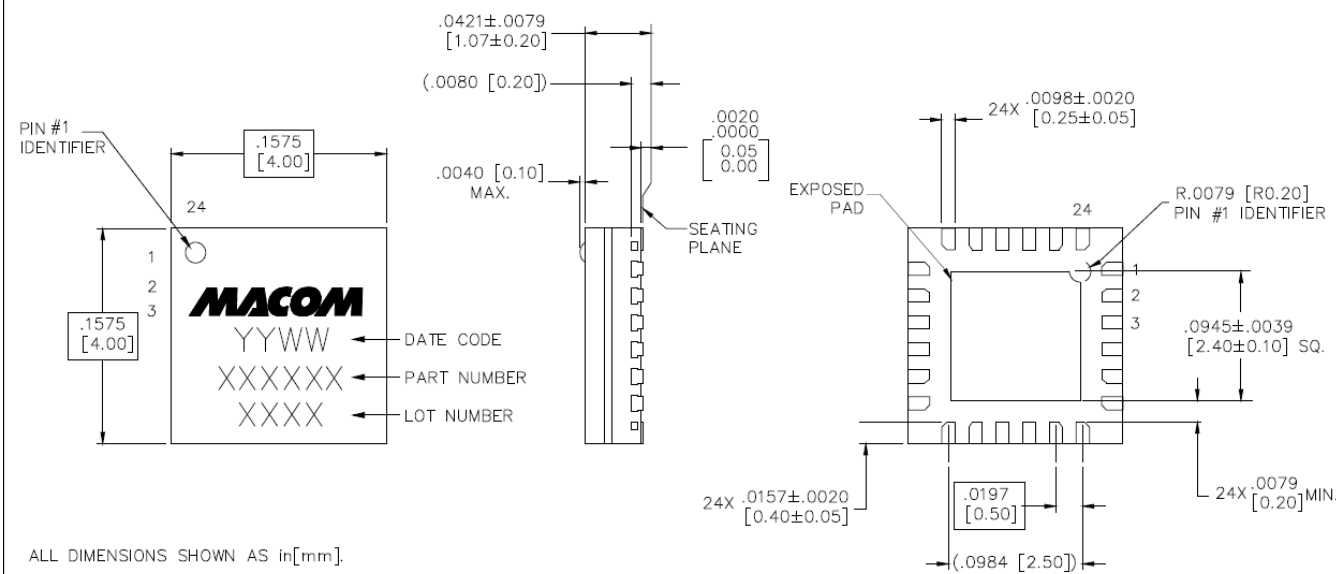

***OIP3 vs. Output Power @ 25C***




***Detector Voltage vs. Output Power @ 25C***



## Lead-Free 4 mm 24-Lead AQFN Package†




† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.
Plating is NiPdAu