eZ80F920020MOD

eZ80F92 Flash Module

Product Specification

PS018905-1203

PRELIMINARY

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Document Disclaimer

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The eZ80F92 Flash Module

The eZ80F92 Flash Module is a low-cost, general-purpose compact module specially designed for the rapid development and deployment of embedded systems. This expandable module is powered by ZiLOG's latest power-efficient, high-speed, optimized pipeline architecture eZ80F92 microcontroller. This microcontroller, the first device in ZiLOG's eZ80Acclaim! product line, features 128KB of on-chip Flash memory and 8KB of on-chip SRAM.

The eZ80F92 MCU is a high-speed single-cycle instruction-fetch microcontroller, which can operate with a clock speed of 20MHz. It can operate in Z80-compatible addressing mode (64KB) or full 24-bit addressing mode (16MB).

The rich peripheral set of the eZ80F92 Flash Module makes it suitable for a variety of applications, including industrial control, IrDA connectivity, communication, security, automation, and point-of-sale terminals.

Note: The eZ80F92 Flash Module incorporates the eZ80F92 MCU. The eZ80F92 can be replaced with the eZ80F93 MCU, which features 64KB of internal Flash memory and 4KB of internal SRAM.

Module Features

- eZ80Acclaim!™ Flash MCU with factory-default operating clock frequency at 20MHz
- 512KB zero-wait-state onboard SRAM
- 128KB on-chip Flash memory
- GoldCap backup for Real-Time Clock
- I/O connector provides 24 general-purpose 5V-tolerant I/O pinouts
- ZiLOG's industry-leading IrDA transceiver—ZiLOG ZHX1810
- In-circuit Flash programming circuitry
- Onboard connector provides I^2C 2-wire SDA/SCL interface
- Onboard connector provides I/O bus for external peripheral connections (IRQ, $\overline{CS}$, 24 address, 8 data)
- Low-cost adaptation to carrier board via two 2x25pin (2.54mm) headers
- Horizontal or vertical mounting onto the eZ80® Development Platform
- Small footprint 64x64mm

- 3.3V power supply
- Standard operating temperature range: 0ºC to +70ºC

Module Bill of Materials

Table 1 lists the installed components of the eZ80F92 Flash Module.

Table 1. Bill of Materials for the eZ80F92 Flash Module

Part Number	Part Name	Qty.	Jumper Location	Manufacturer
98C0873-001	FAB, eZ80F92/93 MODULE, Rev. A	1	—	Prime Technologies
35-0180-12	IC, SRAM, 512Kx8, 12ns, 3V, 36-SOJ	1	U1	Alliance Semi. AS7C34096-12JC
35-0016-05	IC, 74LVC04, 3.3V, GATE, 14-SOIC	1	U2	Texas Instruments SN74LVC04AD
35-0719-00	IC, MAX6328, RESET, SOT-23	1	U4	Maxim Inc. MAX6328UR29-T
ZHX1810	IC, IR Transceiver, low profile	1	U5	ZiLOG Inc. ZHX1810MV115THTR
35-0062-01	IC, 74LCX32, LV, QUAD or 14-TSSOP	1	U6	Fairchild Semi. 74LCX32MTC
EZ80F92	IC, eZ80F92AZ020SC, 20MHZ, 100VQFP	1	U8	ZiLOG Inc. EZ80F92AZ020SC
48-1013-01	DIODE, TVS ARRAY, XCVR PROT, 8-SOIC	1	U9	Semtec LCDA15C-6
17-2005-70	CAP, 1, 000pF, 50V, ceramic chip, 0603	5	C3, C5, C21–23	Panasonic ECJ-1VC1H102J
17-2005-66	CAP, 0.1µF, 16V, ceramic chip, 0603	9	C4, C6–9, C13–15, C18	Kemet Inc. C0603C104K5RAC
17-2005-54	CAP, 0.01µF, 50V, ceramic chip, 0603	1	C10	Panasonic ECJ-1VB1C103K
17-2005-83	CAP, 0.33µF, 16V, ceramic chip, 0603	1	C11	Panasonic ECJ-1VF1C334Z
17-2005-39	CAP, 560pF, 50V, ceramic chip, 0603	1	C12	Panasonic ECJ-1VC1H561J
17-2001-03	CAP, 12pF, 50V, ceramic chip, 0603	4	C16, C17, C20, C24	Panasonic ECJ-1VC1H120J

Table 1. Bill of Materials for the eZ80F92 Flash Module

Part Number	Part Name	Qty.	Jumper Location	Manufacturer
15-0100-01	CAP, 1.10F, 5.5V, GOLD, SD, COIN	1	C19	Panasonic EEC-SOHD104V
48-0030-04	Diode, Schottky, Power rectifier, SMT	1	D1	On Semiconductor MBR0520LT1
46-3001-03	Resistor, 10KΩ, 1%, 1/16W, 0603 SMT	9	R1, 11, 12, 17, 19, 29, 30, 34, 36	Sprague 420CK472X2PD
46-3000-00	Resistor, 0Ω, 1%, 1/16W, 0603 SMT	2	R2, C25	"
46-3000-71	Resistor, 2.21KΩ, 1%, 1/16W, 0603 SMT	3	R3, R10, R33	"
46-3000-35	Resistor, 68Ω, 1%, 1/16W, 0603 SMT	1	R5	"
46-1005-03	Resistor, 2.7Ω, 5%, 1/4W, 1206 SMT	1	R6	"
46-3001-03	Resistor, 4.75KΩ, 1%, 1/16W, 0603 SMT	4	R7, 8, 13, 22	"
46-3000-27	Resistor, 33.2Ω, 1%, 1/16W, 0603 SMT	1	R9	"
46-3000-39	Resistor, 100Ω, 1%, 1/16W, 0603 SMT	5	R20, 21, 26, 28, 32	"
46-3000-80	Resistor, 4.99KΩ, 1%, 1/16W, 0603 SMT	1	R23	"
46-3000-07	Resistor, 8.2Ω, 1%, 1/16W, 0603 SMT	2	R24, R25	"
46-3001-51	Resistor, 100KB, 1%, 1/16W, 0603 SMT	1	R27	"
23-0000-10	Internal crystal, 20.0000MHz, SER/RESN, HC-49S	1	Y1, Y2	Fox Series HC-49S 20.0000MHz
23-0006-00	Internal crystal, 32.768KHz, SER/RESN, TF CASE	1	Y3	NDK MX-38
21-0055-02	Connector, HDR/PIN,. 025SQ, double row	2	JP1, JP2	"

eZ80F92 Controller Features

- The eZ80F92 device contains 128KB of Flash memory and 8KB of SRAM
- Single-cycle instruction fetch, high-performance, pipelined eZ80® CPU core
- Low power features including SLEEP mode, HALT mode, and selective peripheral power-down control

- Two UARTs with independent baud rate generators and support for 9-bit operation
- SPI with independent clock rate generator
- I^2C with independent clock rate generator
- Infrared Data Association (IrDA)-compliant infrared encoder/decoder
- New DMA-like eZ80® CPU instructions for efficient block data transfer
- Glueless external memory interface with 4 chip selects, individual wait state generators, and an external WAIT input pin—supports Intel- and Motorola-style buses
- Fixed-priority vectored interrupts (both internal and external) and interrupt controller
- Real-time clock with on-chip 32KHz oscillator, selectable 50/60Hz input, and separate V_{DD} pin for battery backup
- Six 16-bit Counter/Timers with prescalers and direct input/output drive
- Watch-Dog Timer
- 24 bits of general-purpose I/O
- JTAG and ZDI debug interfaces
- 100-pin LQFP package
- 3.0–3.6V supply voltage with 5V tolerant inputs
- Standard operating temperature range: 0ºC to +70ºC

Note: All signals with an overline are active Low. For example, B/$\overline{W}$, for which WORD is active Low, and B/W, for which BYTE is active Low.

Block Diagram

Figure 1 illustrates a block diagram of the eZ80F92 Flash Module.

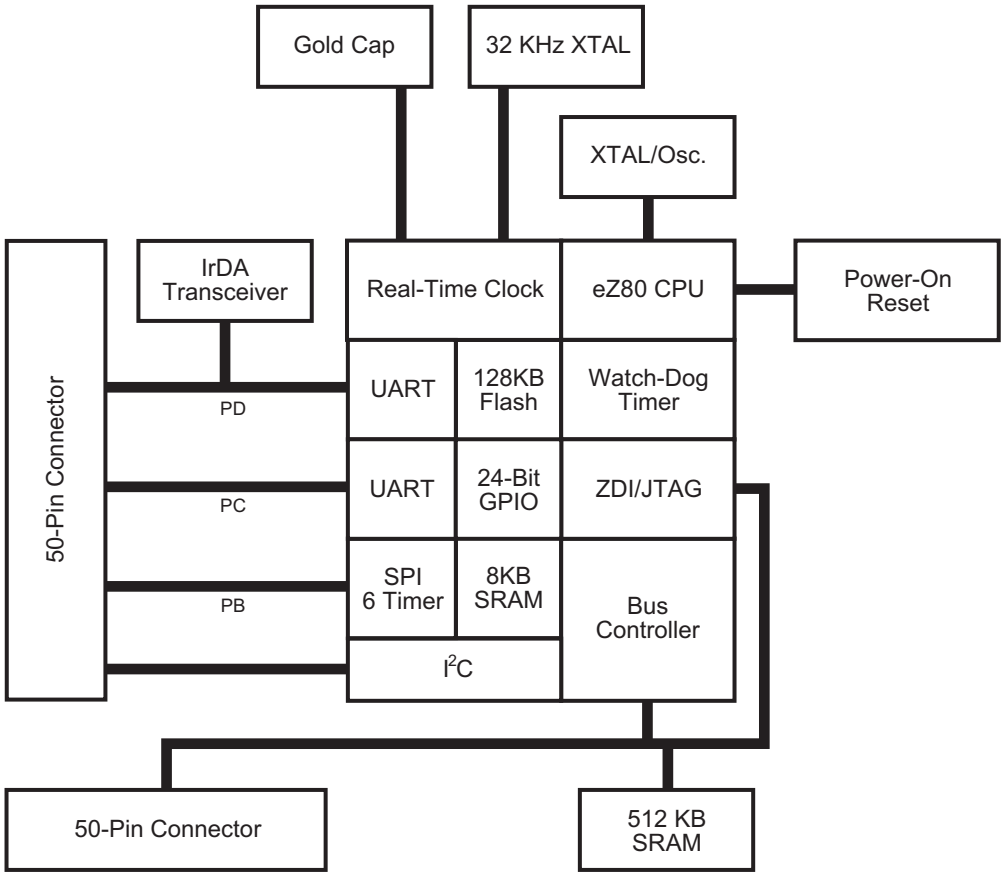


Figure 1. eZ80F92 Flash Module Functional Block Diagram

Pin Description

Peripheral Bus Connector

Figure 2 illustrates the pin layout of the eZ80F92 Flash Module's I/O Connector (JP1) in the 50-pin package. Table 3 describes the pins and their functions.

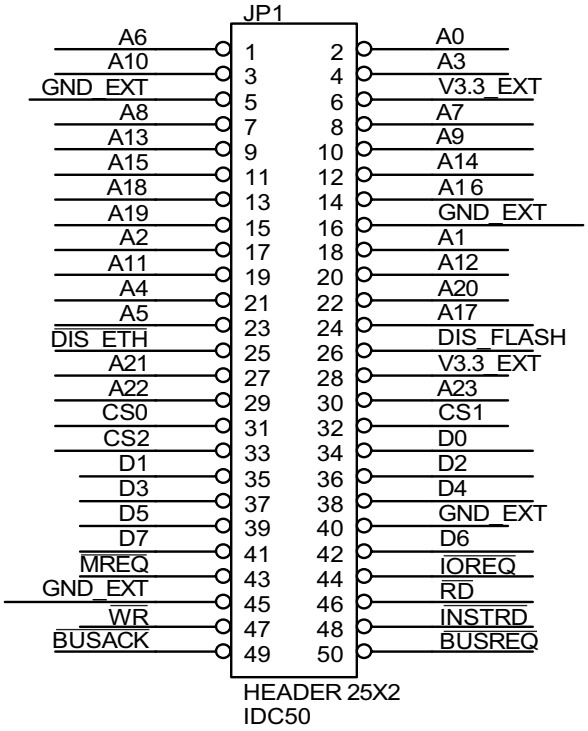


Figure 2. eZ80F92 Flash Module Peripheral Bus Connector Pin Configuration

Table 2. eZ80F92 Flash Module Peripheral Bus Connector Pin Identification*

Pin #	Symbol	Pull Up/Down*	Signal Direction	Comments
1	A6		Bidirectional	
2	A0		Bidirectional	
3	A10		Bidirectional	
4	A3		Bidirectional	
5	GND			V_{SS}/Ground (0V).
6	V_{DD}			3.3V Supply Input Pin.
7	A8		Bidirectional	
8	A7		Bidirectional	
9	A13		Bidirectional	
10	A9		Bidirectional	
11	A15		Bidirectional	
12	A14		Bidirectional	
13	A18		Bidirectional	
14	A16		Bidirectional	
15	A19		Bidirectional	
16	GND			V_{SS}/Ground (0V).
17	A2		Bidirectional	
18	A1		Bidirectional	
19	A11		Bidirectional	
20	A12		Bidirectional	
21	A4		Bidirectional	
22	A20		Bidirectional	
23	A5		Bidirectional	
24	A17		Bidirectional	

Notes: *External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity.
To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F92 Peripheral Power-Down Register.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 2. eZ80F92 Flash Module Peripheral Bus Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down*	Signal Direction	Comments
25	$\overline{\text{DIS\_ETH}}$	PU 10KΩ	Input	This pin is not used on the eZ80F92 Flash Module. However, it is connected to the pad of the CS8900 EMAC footprint.
26	$\overline{\text{DIS\_FLASH}}$	PU 10KΩ	Input	This pin is not used on the eZ80F92 Flash Module. However, it is connected to the pad of the external Flash footprint.
27	A21		Bidirectional	
28	V_{DD}			3.3V supply input pin.
29	A22		Bidirectional	
30	A23		Bidirectional	
31	$\overline{\text{CS0}}$		Output	
32	$\overline{\text{CS1}}$		Output	
33	$\overline{\text{CS2}}$		Output	
34	D0	PU 4k7	Bidirectional	
35	D1	PU 4k7	Bidirectional	
36	D2	PU 4k7	Bidirectional	
37	D3	PU 4k7	Bidirectional	
38	D4	PU 4k7	Bidirectional	
39	D5	PU 4k7	Bidirectional	
40	GND			V_{SS}/Ground (0V).
41	D7	PU 4k7	Bidirectional	
42	D6		Bidirectional	
43	$\overline{\text{MREQ}}$		Bidirectional	
44	$\overline{\text{IORQ}}$		Bidirectional	
45	GND			V_{SS}/Ground (0V).

Notes: *External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity.
To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F92 Peripheral Power-Down Register.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 2. eZ80F92 Flash Module Peripheral Bus Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down*	Signal Direction	Comments
46	$\overline{RD}$		Bidirectional	
47	$\overline{WR}$		Bidirectional	
48	$\overline{INSTRD}$		Output	
49	$\overline{BUSACK}$		Output	
50	$\overline{BUSREQ}$	PU 2k2	Input	

Notes: *External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity.
To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F92 Peripheral Power-Down Register.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

I/O Connector

Figure 3 illustrates the pin layout of the eZ80F92 Flash Module's I/O Connector (JP2) in the 50-pin package. Table 3 describes the pins and their functions.

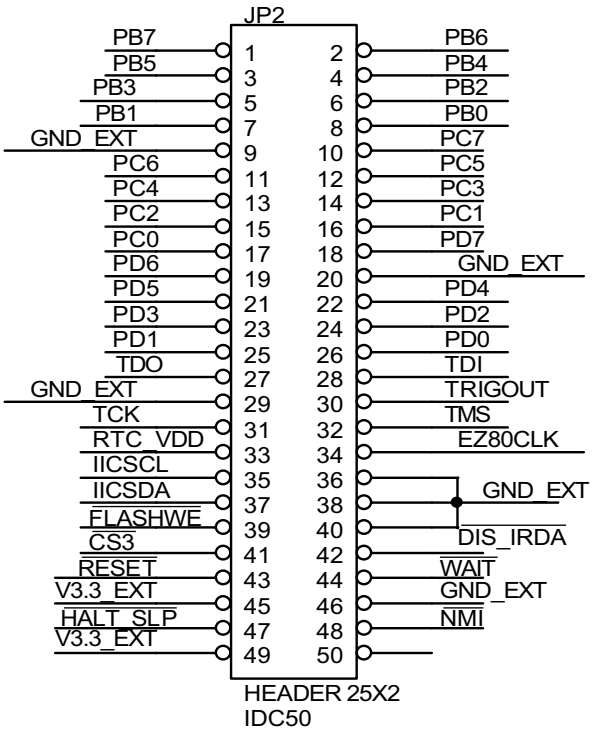


Figure 3. eZ80F92 Flash Module I/O Connector Pin Configuration

Table 3. eZ80F92 Flash Module I/O Connector Pin Identification*

Pin #	Symbol	Pull Up/Down	Signal Direction	Comments
1	PB7		Bidirectional	
2	PB6		Bidirectional	

Notes: *External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91 Peripheral Power-Down Register.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 3. eZ80F92 Flash Module I/O Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down	Signal Direction	Comments
3	PB5		Bidirectional	
4	PB4		Bidirectional	
5	PB3		Bidirectional	
6	PB2		Bidirectional	
7	PB1		Bidirectional	
8	PB0		Bidirectional	
9	GND			V_{SS}/Ground (0V).
10	PC7		Bidirectional	
11	PC6		Bidirectional	
12	PC5		Bidirectional	
13	PC4		Bidirectional	
14	PC3		Bidirectional	
15	PC2		Bidirectional	
16	PC1		Bidirectional	
17	PC0		Bidirectional	
18	PD7		Bidirectional	
19	PD6		Bidirectional	
20	GND			V_{SS}/Ground (0V).
21	PD5		Bidirectional	
22	PD4	PD 4k7	Bidirectional	
23	PD3		Bidirectional	
24	PD2		Bidirectional	
25	PD1		Bidirectional	
26	PD0		Bidirectional	

Notes: *External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91 Peripheral Power-Down Register.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 3. eZ80F92 Flash Module I/O Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down	Signal Direction	Comments
27	TDO		Output	JTAG Data Output pin.
28	TDI/ZDA		Input	JTAG Data Input pin.
	ZDA		Bidirectional	ZDI Data I/O.
29	GND			V_{SS}/Ground (0V).
30	TRIGOUT		Output	Active High trigger event indicator.
31	TCK	PU 10KΩ	Input	JTAG Input. High on reset enables ZDI mode; Low on reset enables OCI debug.
32	TMS	PU 10KΩ	Input	JTAG Test Mode Select Input.
33	RTC_V_{DD}			RTC supply from GoldCap (or external battery).
34	EZ80CLK		Output	20MHz synchronous CPU clock output.
35	SCL	PU 4k7	Bidirectional	I^2C Bus Clock.
36	GND			V_{SS}/Ground (0V).
37	SDA	PU 4k7	Bidirectional	I^2C Data Clock.
38	GND			V_{SS}/Ground (0V).
39	$\overline{\text{FlashWE}}$	PU 10KΩ	Input	This pin has no function on the eZ80F92 Flash Module. It is pulled up to V_{DD} and a connection is available on the external Flash memory pads.
40	GND			V_{SS}/Ground (0V).
41	CS3		Output	Chip select for onboard or external devices; CMOS output 3.3V.
42	$\overline{\text{DIS\_IRDA}}$	PU 10KΩ	Input	Low disables onboard IRDA transceiver to use PD0/PD1 UART pins externally.
43	$\overline{\text{RESET}}$	PU 2k2	Bidirectional	Reset Output from module or push-button reset.
44	$\overline{\text{WAIT}}$	PU 2k2	Input	Driving the $\overline{\text{WAIT}}$ pin Low forces the CPU to provide additional clock cycles for an external peripheral or external memory to complete its Read or Write operation.

Notes: *External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91 Peripheral Power-Down Register.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 3. eZ80F92 Flash Module I/O Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down	Signal Direction	Comments
45	V_{DD}			3.3V supply input pin.
46	GND			V_{SS}/Ground (0V).
47	$\overline{\text{HALT\_SLP}}$		Output, Active Low	A Low on this pin indicates that the CPU enters either HALT or SLEEP mode because of execution of either a HALT or SLP instruction.
48	$\overline{\text{NMI}}$	PU 10KΩ	Schmitt Trigger Input, Active Low	The $\overline{\text{NMI}}$ input is a higher priority input than the maskable interrupts. It is always recognized at the end of an instruction, regardless of the state of the interrupt enable control bits. This input includes a Schmitt trigger to allow RC rise times. This external NMI signal is combined with an internal NMI signal generated from the WDT block before being connected to the NMI input of the CPU.
49	V_{DD}			3.3V supply input pin.
50	Reserved			

Notes: *External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91 Peripheral Power-Down Register.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Onboard Component Description

Logic-Level I/Os

The I/O connector features 24 general-purpose 3.3V CMOS I/O pins that can be used as outputs or inputs interfacing to external logic. All I/Os are 5V tolerant. Some of the General-Purpose I/O pins support dual mode functions (SPI, Timer I/O, UARTs and bit I/O with edge- or level-triggered interrupt functions on each pin). For more information on eZ80F92 dual modes, please refer to the eZ80F92 Product Specification (PS0153).

Onboard Battery Backup

An onboard 0.1F capacitor (GoldCap) is used to bridge power outages of 2–4 hours if the power supply to the module is disconnected. The capacitor is charged to 3.1V during normal operation and is discharged through the on-chip Real Time Clock. The V_{RTC} pin is available on the I/O connector of the module to connect external components to a power supply or to a larger GoldCap.

Caution: Do not connect a Lithium Battery to the GoldCap capacitor, because onboard charging circuitry for the capacitor can destroy the lithium battery.

Memory

The eZ80F92 Flash Module offers external SRAM memory and the wait states selectable in the eZ80F92 MCU's support memory operations, as described in this section.

Wait States

To ensure that valid data is read from or written to slower memories, a number of wait states must be inserted into the memory or I/O access operations by the controller. The number of wait states that are required should be added by programming the chip select control registers. To calculate the minimum number of wait states required, refer to Table 4.

Table 4. Chip Frequency to Wait State Cycle Time Calculation

MHz	Cycle Time
12	83.3ns
20	50.0ns

Static RAM

The eZ80F92 Flash Module features 512KB of fast SRAM. Access speed is typically 50ns, allowing zero-wait-state operation at 20MHz. With the CPU at 20MHz, SRAM can be accessed with zero wait states in eZ80 mode. CS1_CTL (chip select CS1) can be set to 08h (no wait states).

Flash Memory

The eZ80F92 Flash Module allows NOR Flash memories between 4megabits (512KB) and 32 megabits (4MB) to be added. The chips are housed in wide TSOP40 cases. Flash ROM access times are 55–150ns; typically 90ns. The Flash Boot Loader, application code, and user configuration data are held permanently in NOR Flash memory.

NOR Flash should be operated in Intel bus mode to satisfy setup and hold times and to prevent bus contention with a WRITE cycle that could possibly follow. For proper CPU operation at 20MHz, first set the bus mode control register CS0_BMC (I/O address 0xF0h) to 82h, then set the Chip Select Control register CS0_CTL (I/O address 0xAAh) to 08h. These settings select Intel Bus Mode with two system clocks per bus cycle and zero wait states.

The eZ80F92 Flash Module features the following memory configurations:

- On-chip SRAM: 8KB
- Off-chip SRAM: 512KB
- On-chip Flash: 128KB
- Off-chip Flash: 1MB

IrDA Transceiver

An onboard IrDA transceiver (ZiLOG ZHX1810) is connected to PD0 (TX), PD1 (RX), and PD2 (Shutdown, R_SD). The IrDA transceiver is of the LED type 870nm Class 1.

The receiver supply current is 90–150 µA and the transmitter supply current is 260 mA when the LED is active.The IrDA transceiver is accessible via the IrDA controller attached to UART0 on the eZ80F92 device. The UART0 console and the IrDA transceiver cannot be used simultaneously.

To use the UART0 for console or to save power, the transceiver can be disabled by the software or by an off-board signal when using the proper jumper selection. The transceiver is disabled by setting PD2 (IR_SD) High or by pulling the DIS_IRDA pin on the I/O connector Low. The shutdown is used for power savings. To enable the IrDA transceiver, DIS_IRDA is left floating and PD2 is set to Low.

Reset Generator

The onboard Reset Generator Chip performs reliable Power-On Reset. The chip generates a reset pulse with a duration of 200 ms if the power supply drops below 2.93 V. This reset pulse ensures that the board always starts in a defined condition. The RESET pin on the I/O connector reflects the status of the RESET line. It is a bidirectional pin for resetting external peripheral components or for resetting the eZ80F92 Flash Module with a low-impedance output (e.g. a 100-Ohm push-button).

Serial Interface Ports

The controller contains two 16550-style UARTs with programmable baud rate generators. UART0 is typically used for console I/O and initial boot code upload or to connect remote peripherals that can be controlled and monitored via Ethernet. UART0 is connected to GPIO PD[0:3] on the I/O connector. There are no RS232-level shifters on the eZ80F92 Flash Module.

Note: Do not connect an RS-232 interface without level shifters.

UART1 can be used for modem attachment or as a communications port to a host computer, where the embedded Ethernet module emulates an AT-style modem for internet access. UART1 does not offer onboard RS232-level shifters.

Physical Dimensions

The size of the eZ80F92 Flash Module PCB is 64 x 64 mm. See Figure 4.

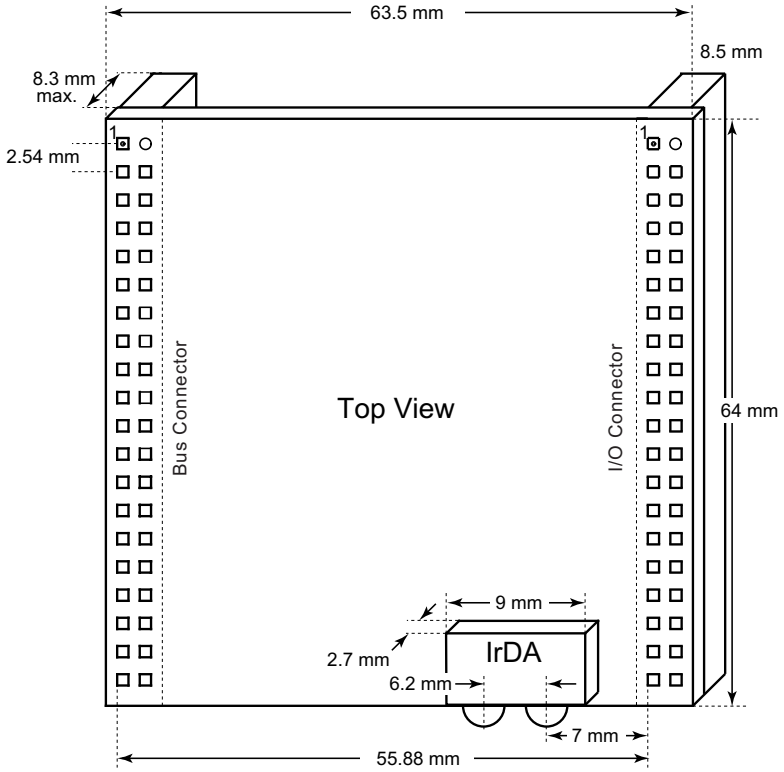


Figure 4. Dimension Drawing

Figure 5 illustrates a top view of the eZ80F92 Flash Module.

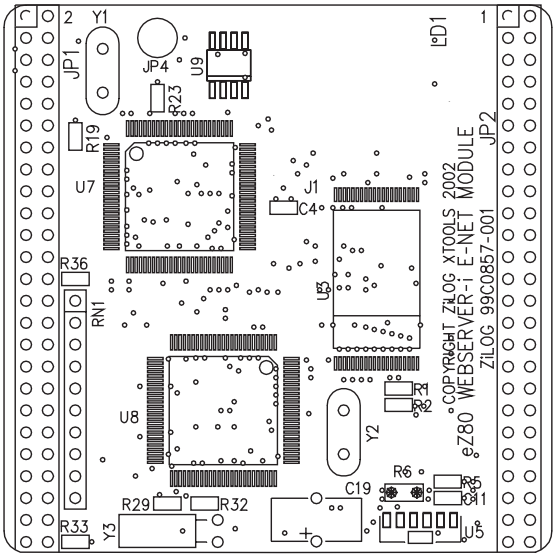


Figure 5. Top Layer

Figure 6 illustrates a bottom view of the eZ80F92 Flash Module.

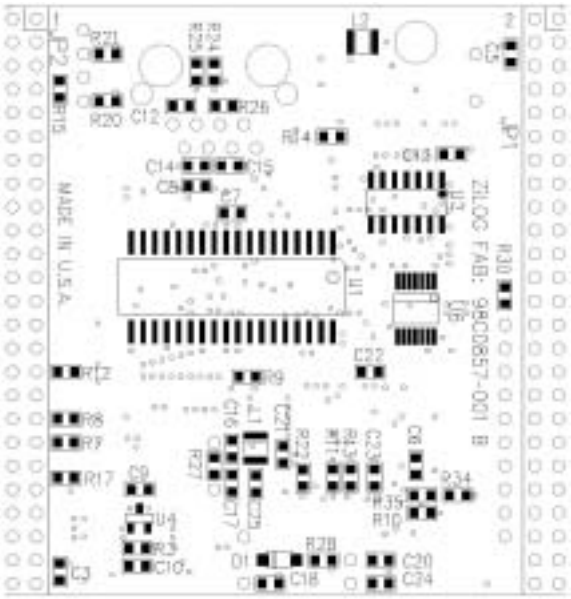
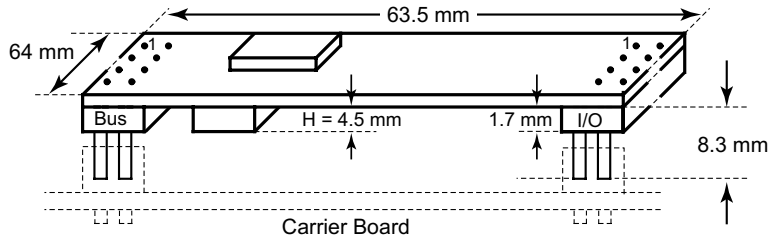


Figure 6. Bottom Layer

Mounting the Module onto the eZ80® Development Platform

The eZ80F92 Flash Module can be mounted in several positions. Depending on volume and area restrictions, it can be mounted horizontally or vertically with or without components between the connectors on the eZ80® Development Platform. See Figure 7 for examples.

Low Profile Mounting



Stacked Mounting

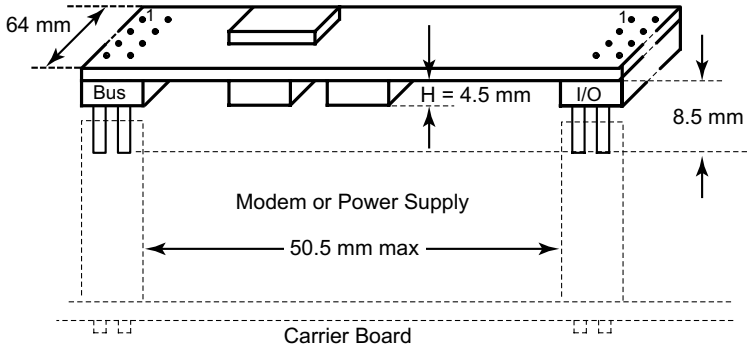


Figure 7. Mounting Examples

ESD/EMI Protection

Caution: The eZ80F92 Flash Module is a component that is intended to be part of a system design for end-user devices. Therefore, the user must exercise caution to use ESD protection on the I/O pins.

Caution: CMOS I/Os are ESD-sensitive and must be handled with care. Handling of the module should be performed in ESD-safe environments (for

example with a wrist-wrap attached). When developing applications, the user must provide for proper ESD protection on external, user-accessible I/Os (e.g. suppressor arrays for the I/Os).

The components are mounted on a multilayer PCB to provide a stable ground plane for onboard components. The module features several GND pins next to pins with higher switching frequency for short ground returns. If unused, the clock output can be separated from the module header by removing a series resistor on the module. Removing the series resistor further reduces electromagnetic emissions.

Absolute Maximum Ratings

Stresses greater than those listed in Table 5 can cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, unused inputs should be tied to one of the supply voltages (V_{DD} or V_{SS}).

Table 5. Absolute Maximum Ratings

Parameter	Min	Max	Units
Standard operating temperature	0	+70	ºC
Storage temperature	–45	+85	ºC
Operating Humidity (RH @ 50ºC)	25%	90%	
Operating Voltage (±5%)	—	3.3	V

Power Supply

The eZ80F92 Flash Module requires a regulated external 3.3VDC/0.5A power supply. You may use a Low Dropout Regulator (LDO) to get 3.3V from 5V or use the following switcher circuit to generate 3.3V from unregulated 10–28V power supply.

Power connections follow these conventional descriptions:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Figure 8 offers two typical power supply examples.

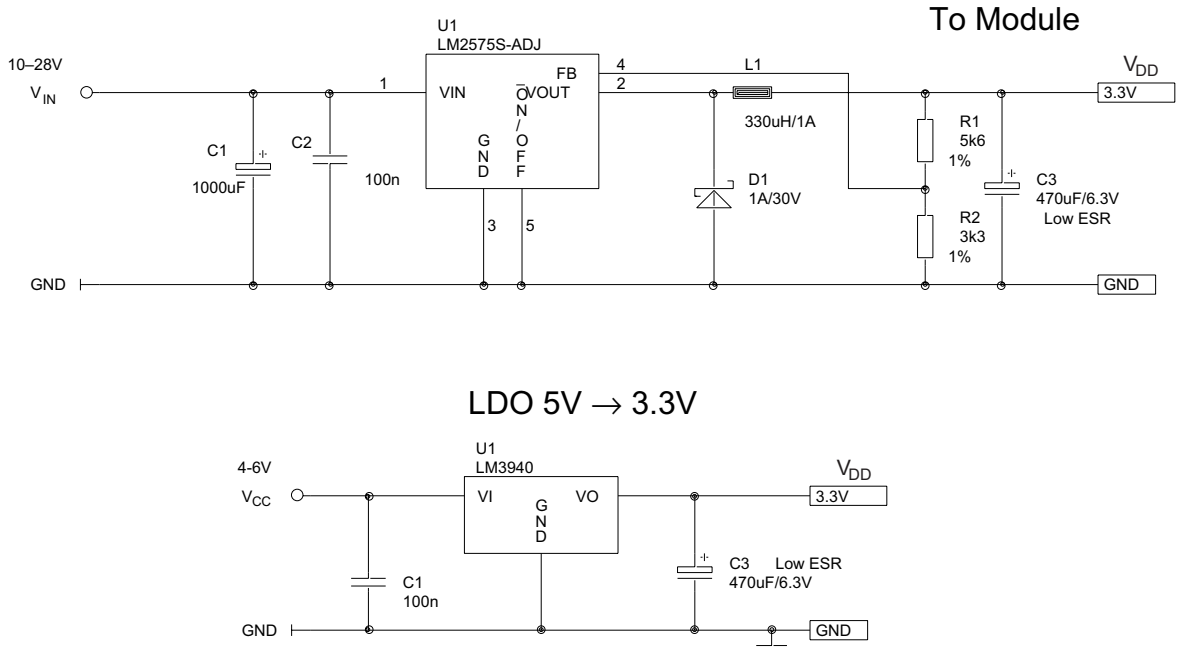


Figure 8. Power Supply Examples

Document Number Description

The Document Control Number that appears in the footer of each page of this document contains unique identifying attributes, as indicated in the following table:

PS	Product Specification
0189	Unique Document Number
05	Revision Number
1203	Month and Year Published

Change Log

Rev	Date	Purpose	By
01	November 2002	Original issue	S. Pope
02	January 2003	Minor modifications	R. Beebe
03	February 2003	Minor modifications	R. Beebe
04	August 2003	Minor modifications	R. Beebe
05	December 2003	Minor modifications	R. Beebe

Schematic Diagrams

Figures 9 through Figure 17 diagram the layout of the eZ80F92 Flash Module. Ethernet and external Flash circuiting devices are not loaded on the eZ80F92 Flash Module. However, these devices appear in the following schematics for reference purposes.

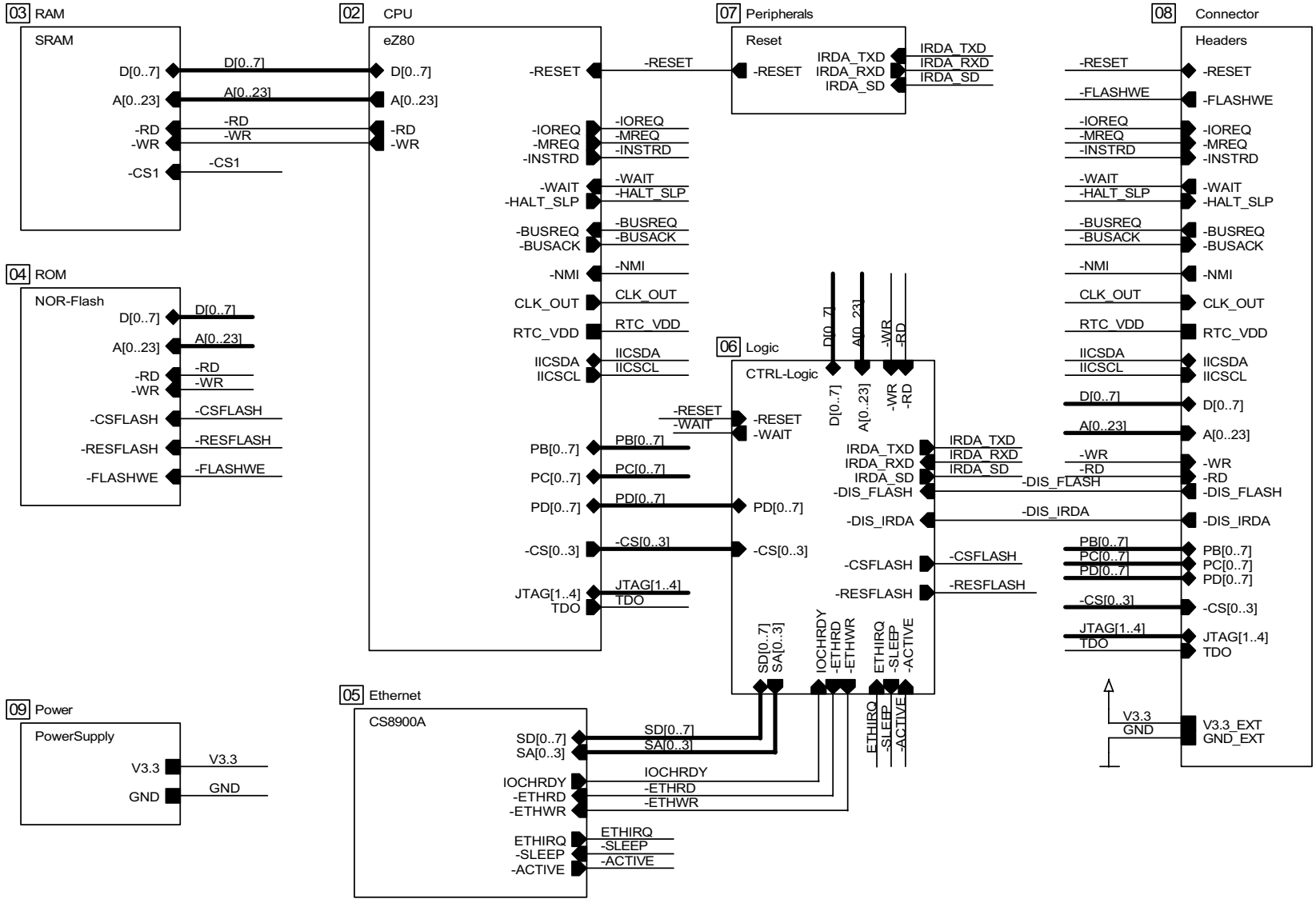


Figure 9. eZ80F92 Flash Module Schematic Diagram, #1 of 9—Top Level

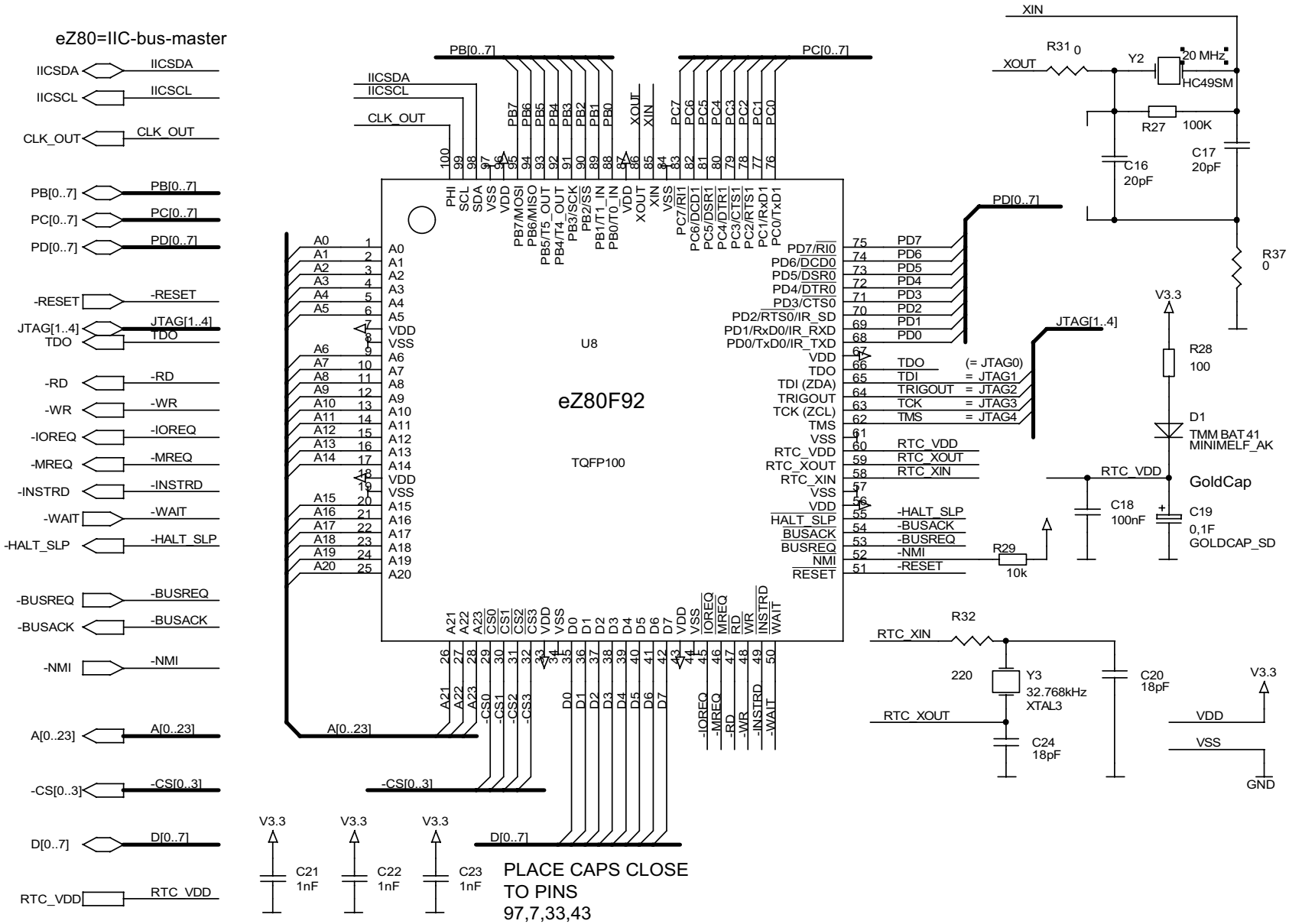


Figure 10. eZ80F92 Flash Module Schematic Diagram, #2 of 9—100-Pin QFP eZ80F92 Device

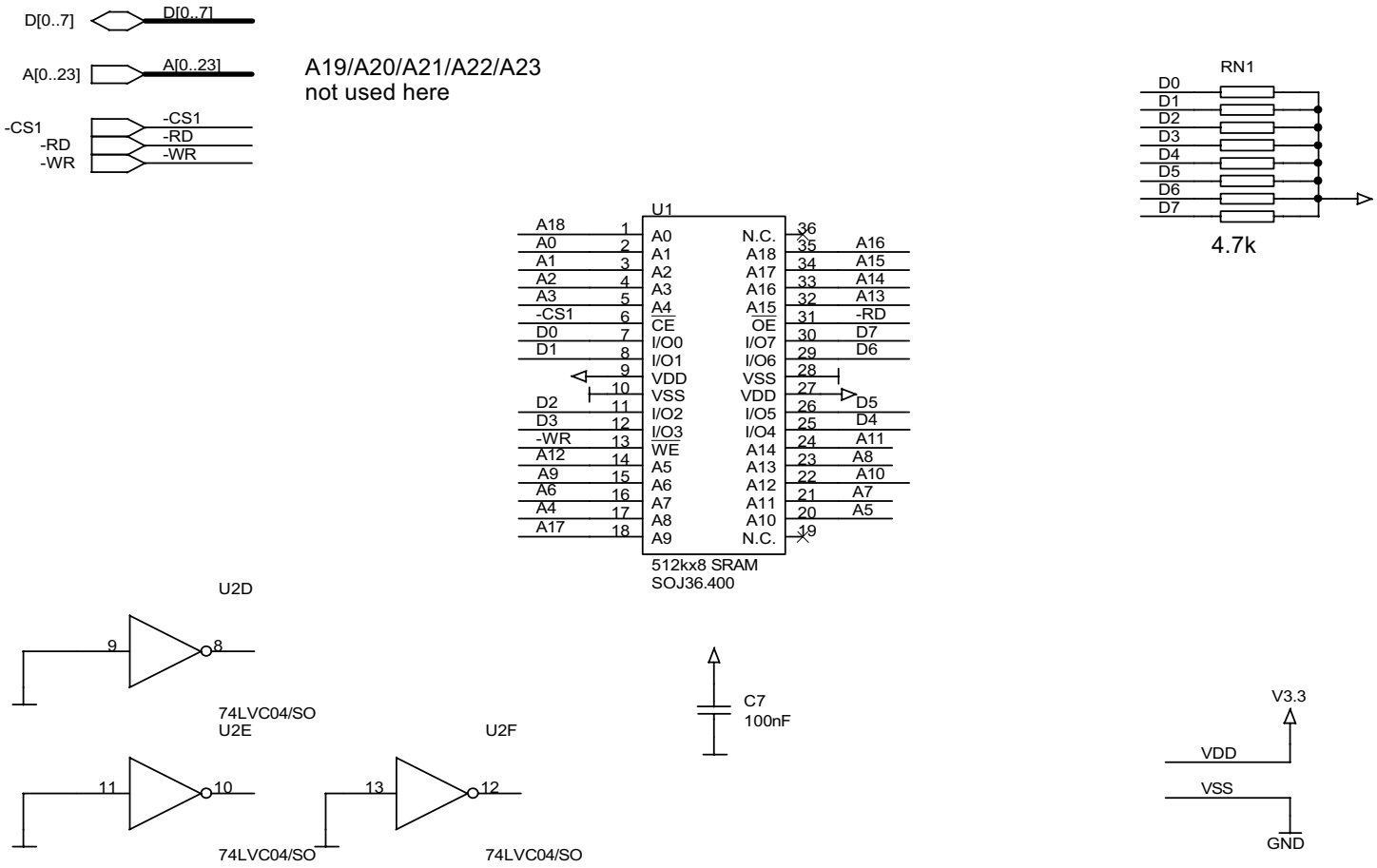


Figure 11. eZ80F92 Flash Module Schematic Diagram, #3 of 9—36-Pin SRAM Device

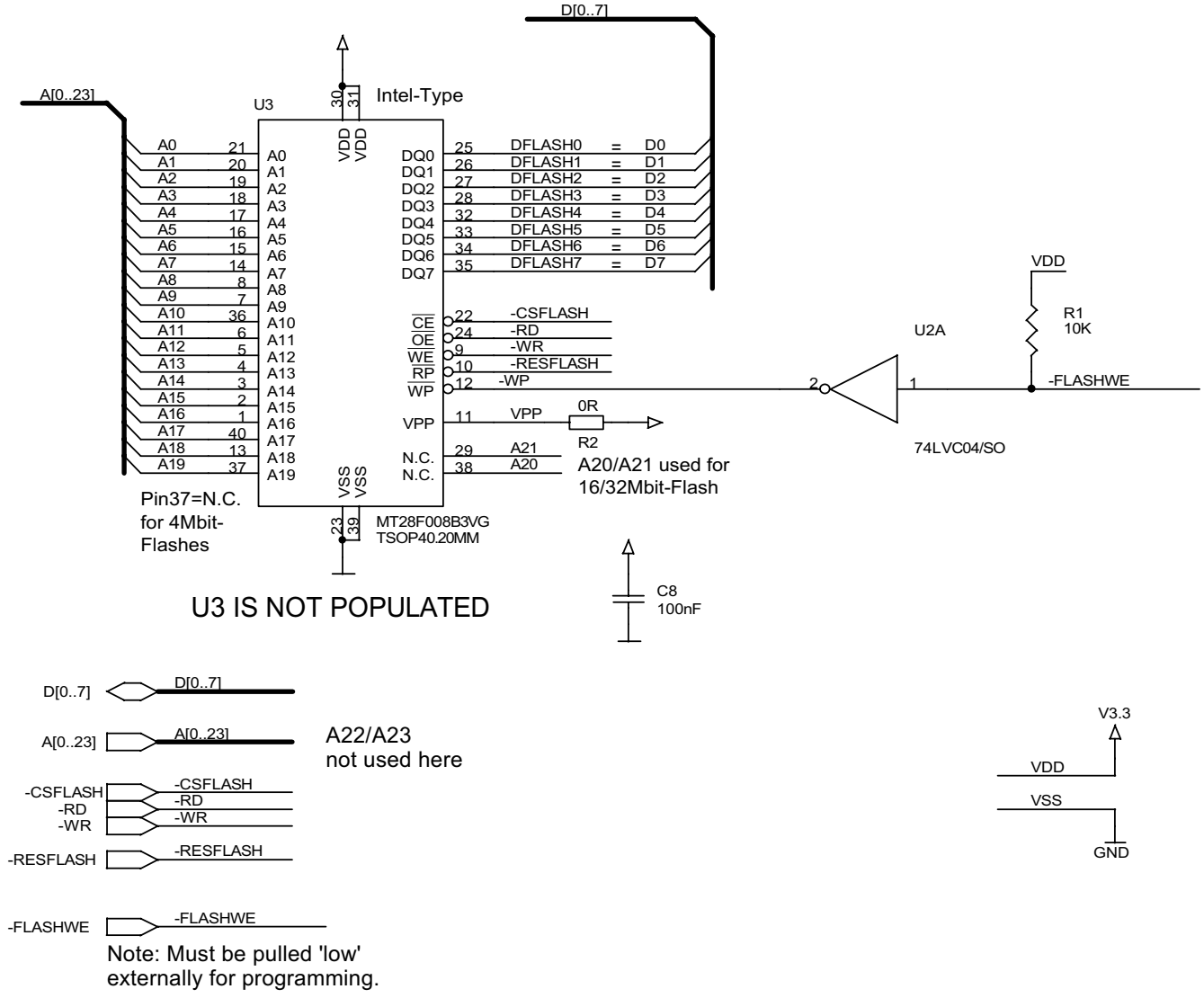


Figure 12. eZ80F92 Flash Module Schematic Diagram, #4 of 9—NOR Flash Device

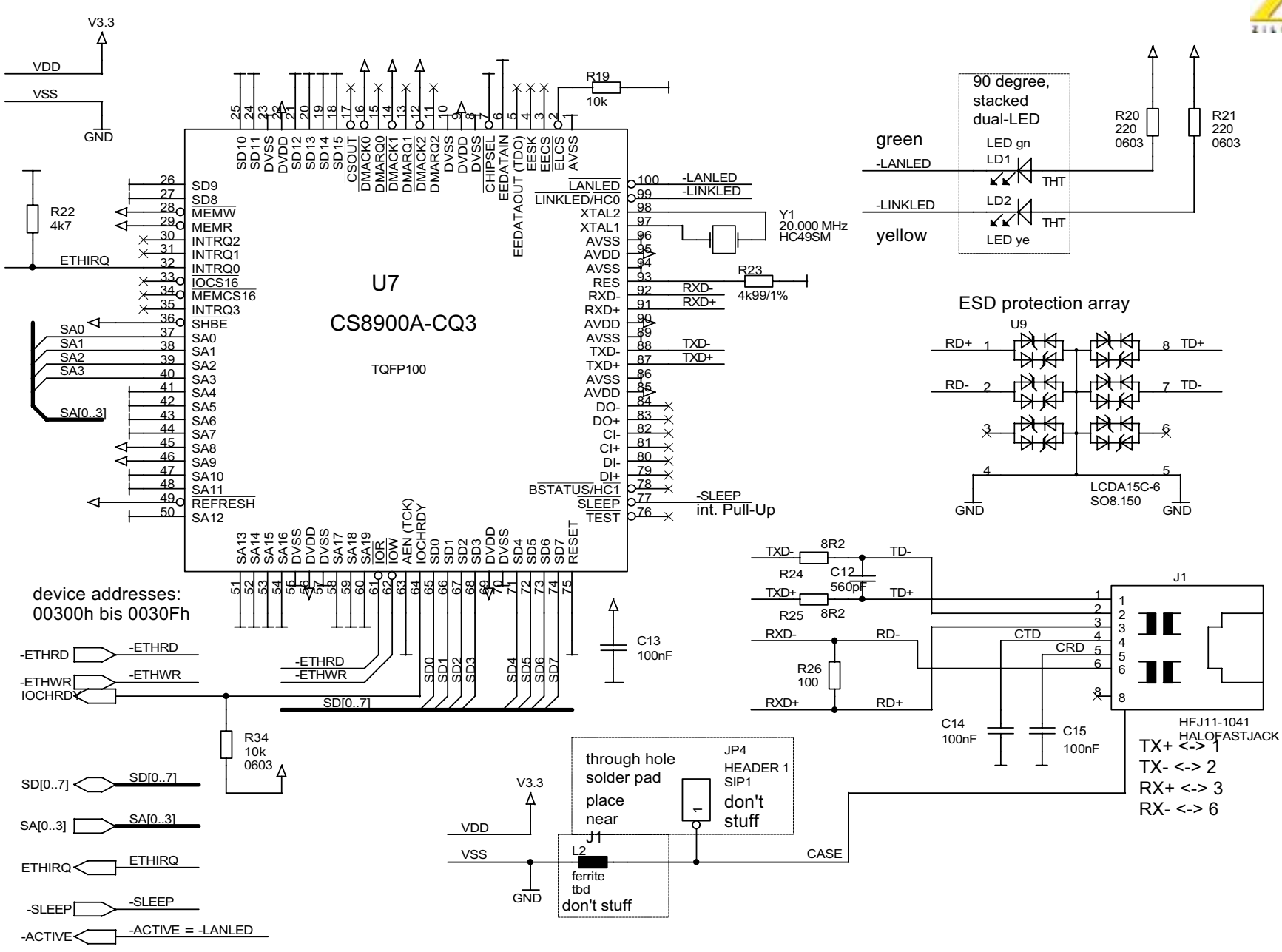


Figure 13. eZ80F92 Flash Module Schematic Diagram, #5 of 9—Module

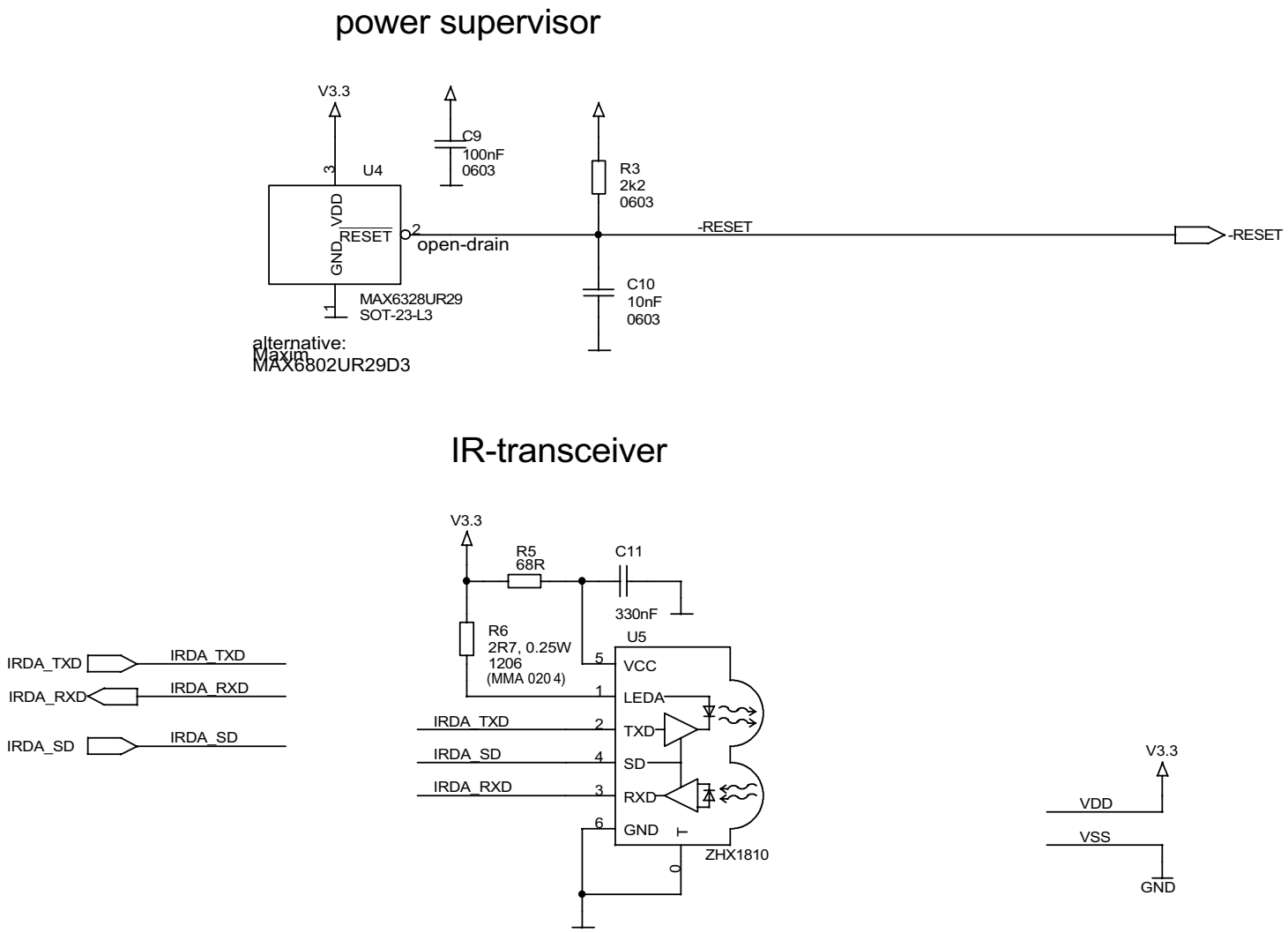


Figure 14. eZ80F92 Flash Module Schematic Diagram, #6 of 9—IrDA Reset

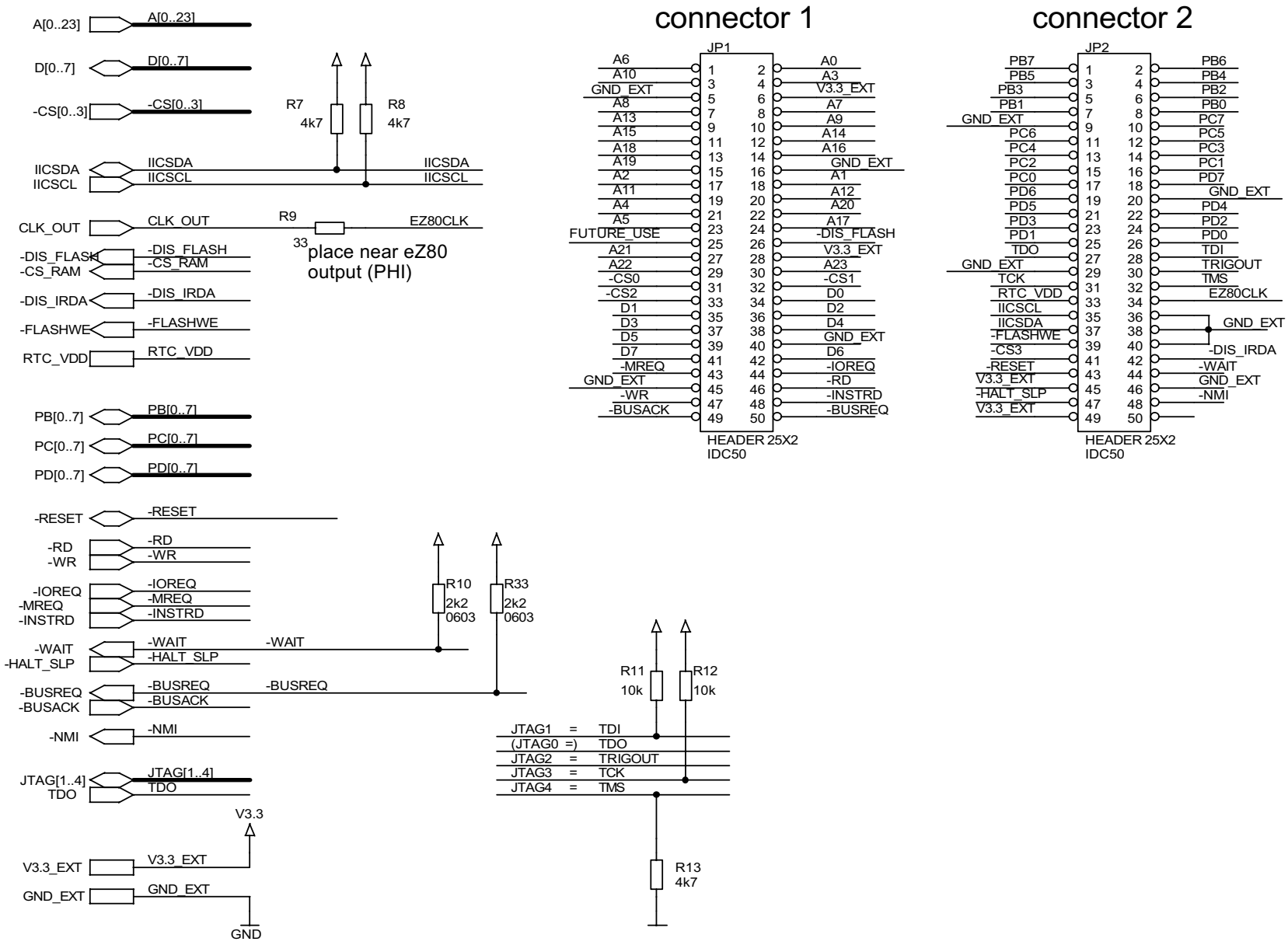
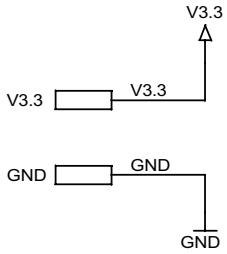
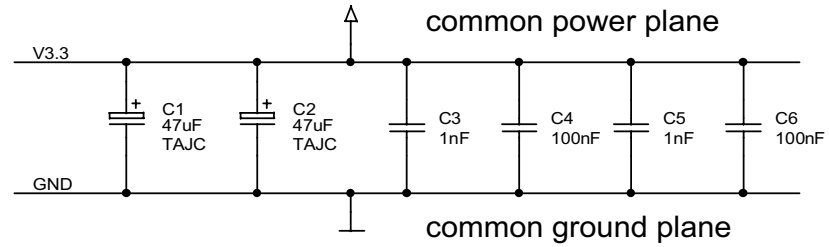


Figure 15. eZ80F92 Flash Module Schematic Diagram, #7 of 9—Headers





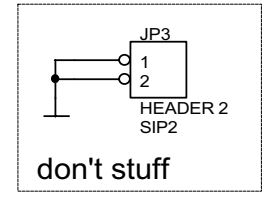
no power supply on board!

Input: VDD(=V3.3) = 3.3V ±5%

Power: Pmax = 1.6W
Ptyp = 0.4W

Current: Imax = 200mA (IrDA not in use)
Imax = 460mA (IrDA in use)
Ityp = 100mA

for test purposes



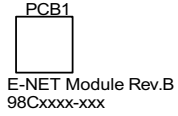


Figure 16. eZ80F92 Flash Module Schematic Diagram, #8 of 9—Power Supply

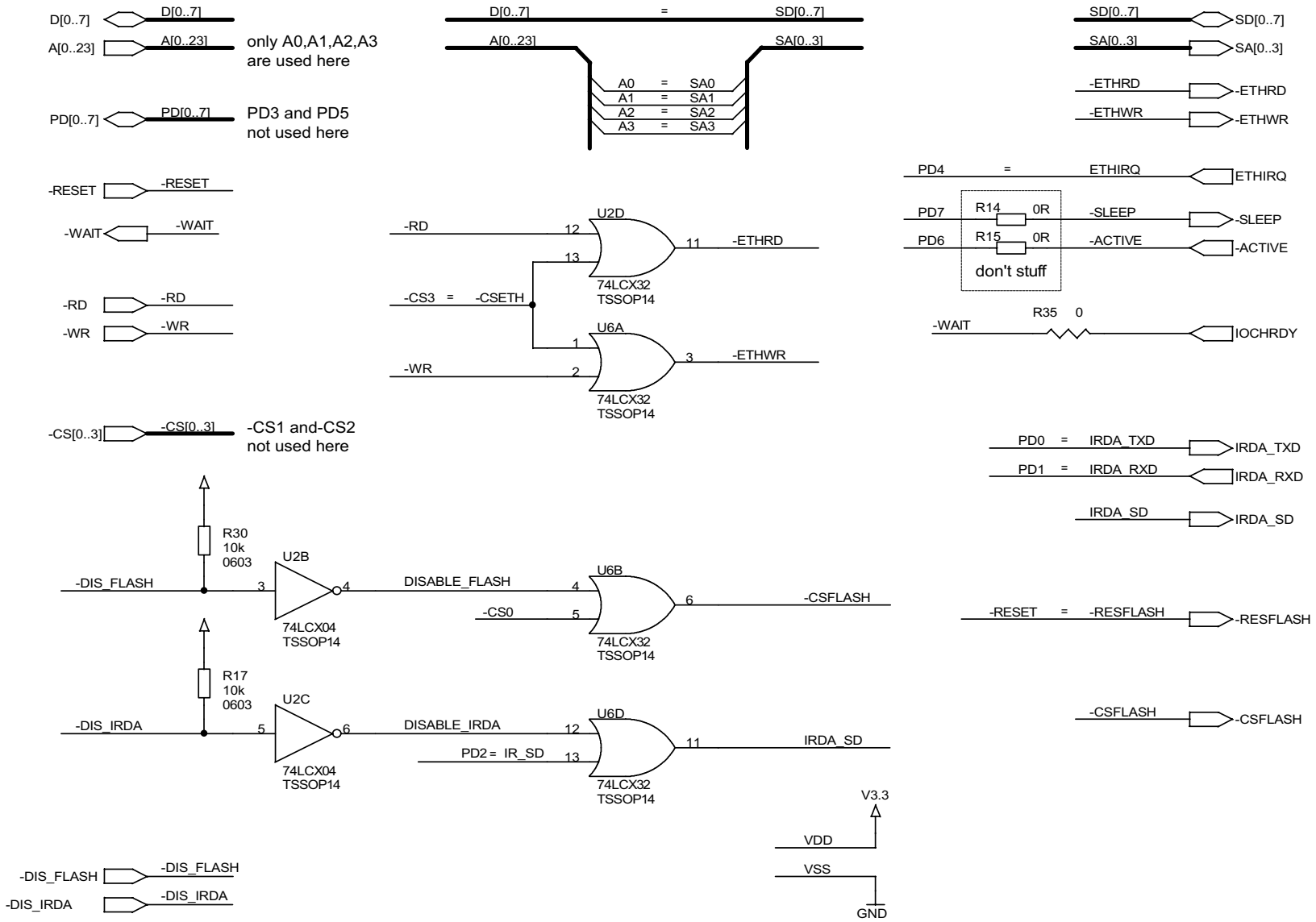


Figure 17. eZ80F92 Flash Module Schematic Diagram, #9 of 9—Control Logic

Customer Feedback Form

The eZ80F92 Flash Module Product Specification

If you experience any problems while operating this product, or if you note any inaccuracies while reading this Product Specification, please copy and complete this form, then mail or fax it to ZiLOG (see *Return Information*, below). We also welcome your suggestions!

Customer Information

Name	Country
Company	Phone
Address	Fax
City/State/Zip	Email

Product Information

Serial # or Board Fab #/Rev. #
Software Version
Document Number
Host Computer Description/Type

Return Information

ZiLOG
System Test/Customer Support
532 Race Street
San Jose, CA 95126
Phone: (408) 558-8500
Fax: (408) 558-8536
ZiLOG Customer Support

Problem Description or Suggestion

Provide a complete description of the problem or your suggestion. If you are reporting a specific problem, include all steps leading up to the occurrence of the problem. Attach additional pages as necessary.

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EZ80F920020MOD